Gate Quantum Capacitance Effects in Nanoscale Transistors

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KEYWORDS: Gate quantum capacitance, limited density of states, low dimensional gate, carbon nanotube gate, gate charge limited MOSFET, gate starvation, CNT gated SOI MOSFET

ABSTRACT

As the physical dimensions of a transistor gate continue to shrink to a few atoms, performance can be increasingly determined by the limited electronic density of states (DOS) in the gate and the gate quantum capacitance (C_Q). We demonstrate the impact of gate C_Q and the dimensionality of the gate electrode on the performance of nanoscale transistors through analytical electrostatics modeling. For low dimensional gates, the gate charge can limit the channel charge and the transfer characteristics of the device become dependent on the gate DOS. We experimentally observe for the first time, room-temperature gate quantization features in the transfer characteristics of single walled carbon nanotube (CNT) gated ultra-thin silicon-on-insulator (SOI) channel transistors; features which can be attributed to the Van Hove singularities in the 1-dimensional DOS of the CNT gate. In addition to being an important aspect of future transistor design, potential applications of this phenomenon include multi-level transistors with suitable transfer characteristics obtained *via* engineered gate DOS.

MAIN TEXT

Quantum mechanical effects play an increasing role in determining transistor performance at near atomic-scale dimensions [1-8]. The impact of low dimensionality and the resulting low electronic density of states (DOS) [9] has been studied in detail for a transistor channel [2, 4, 6, 7, 10]. Channel quantum

capacitance (C_Q) becomes especially important for large gate oxide capacitance (C_{OX}) resulting from aggressively scaled effective oxide thicknesses (EOT) [1, 3]. However, quantum mechanical effects on transistor performance arising from the small sizes and low dimensionality of other parts like the source-drain contacts and gate have not been well explored [11-15]. Similar to the case of a low dimensional channel, a finite number of atoms in atomic-scale gates can result in the problem of low gate DOS, which impacts transistor characteristics and performance.

The gate charge (Q_G) in an ideal MOSFET is always equal and opposite of the total channel charge (Q_{CH}) in the semiconductor [16]. An applied drain-source bias (V_{DS}) across the channel results in a flow of the inversion charge (Q_{INV}) and hence the drain current (I_D). For MOSFETs with large-volume metal gate electrodes, the gate has a large DOS and an almost infinite capacity to balance Q_{CH}. However, a low-dimensional atomic-scale gate with small DOS limits Q_G, thereby limiting Q_{CH}, especially in inversion when Q_{INV} is large. The starvation of DOS in the gate will dictate the I_D characteristics in this case.

The focus of this work is not to measure the DOS and C_Q of nanoscale materials like CNTs, but rather understand the impact of these low DOS materials on transistor characteristics when used as a gate. Here, we consider the impact of gate C_Q on the transistor characteristics by developing an analytical electrostatics model for a bulk silicon channel MOSFET [11]. This is studied by computing the functional dependence of the gate electrostatic potential (V_Q) and the value of Q_G on the gate DOS and the applied gate bias

(V_{GS}), for several different gate materials with different dimensionalities [11, 17]. Nanomaterials like graphene and carbon nanotubes (CNTs) have been proposed as potential gate electrode materials because of their large conductivity at atomic-scale [11, 13, 15]. We experimentally demonstrate for the first time, room-temperature gate C_Q effects on the I_D characteristics for a model system comprising of an ultra-thin silicon-on-insulator (SOI) channel transistor with a 1-dimensional (1D) single walled carbon nanotube (SWCNT) gate electrode. Quantization features resulting from the Van Hove singularities in the DOS of the CNT gate are observed in the transfer characteristics of the device. Finally, we discuss the potential of engineering the gate DOS to tailor the shape of the I_DV_{GS} characteristics of a device and the impact of gate C_Q on the performance of nanoscale transistors.

RESULTS AND DISCUSSION

The concept of gate C_Q limited transistors is illustrated in figure 1a using the example of a bulk silicon channel MOSFET with gate electrodes of varying dimensionality. Figure 1b shows the DOS for the specific case of carbon based gates; graphite for 3D, graphene for 2D and carbon nanotube for 1D gate [18-20]. In a MOSFET with a bulk 3D gate, the gate DOS is very large and thus it can accommodate any Q_G needed to support an equal and opposite charge in the channel ($Q_{CH} = Q_{INV} + Q_{DEP}$), where Q_{INV} and Q_{DEP} are the inversion and depletion charge densities respectively.

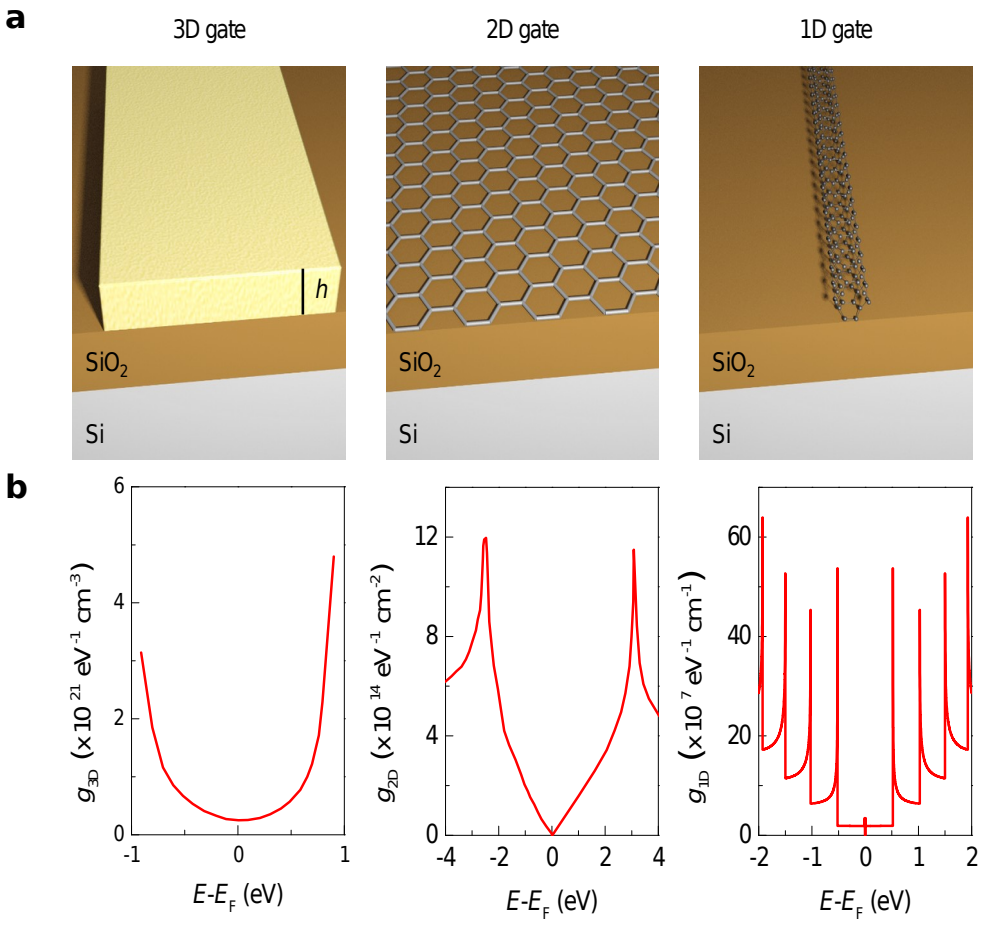

Figure 1: Gate quantum capacitance effects in nanoscale transistors: (a) Schematic of a bulk Si MOSFET and **(b)** the density of states for 3D (graphite, h = 100 nm), 2D (graphene) and 1D (CNT (n,m) = (18,18)) gate

As the dimensionality of the gate and the physical size reduces, the gate DOS is limited and in this case V_Q is related to Q_G by equation 1 [1, 11].

$$Q_G = \int_0^{V_Q} C_Q(V')\,dV' \quad \ldots (1)$$

Here C_Q represents the quantum capacitance of the gate and can be calculated using equation 2.

$$C_Q(V_Q) = q^2 \int_{-\infty}^{\infty} g(E)\left(-\frac{\partial f(E, E_{F,G})}{\partial E}\right) dE \quad \ldots (2)$$

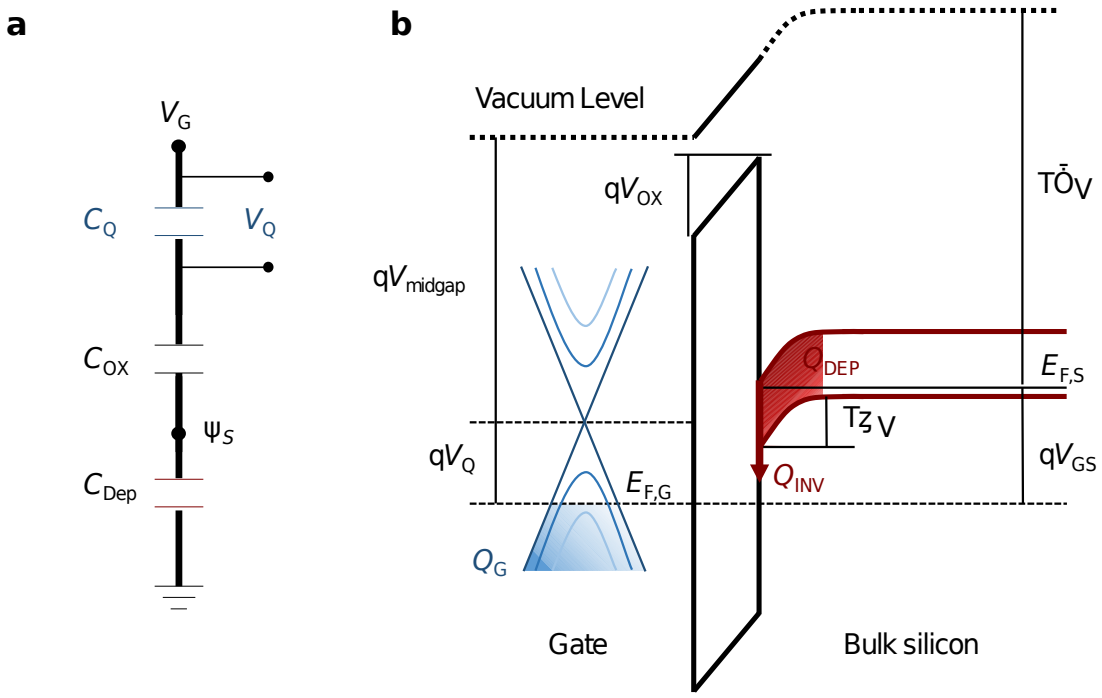

Figure 2: Equivalent model and energy band diagram: (a) Capacitance model for bulk Si MOSFET considering quantum capacitance of the gate electrode. **(b)** Energy band diagram showing the different model parameters

The electrostatic potential of the gate $V_Q = -(E_{F,G}/q)$, where $E_{F,G}$ is the Fermi level of the gate. $g(E)$ is the electronic density of states of the gate, $f(E, E_{F,G})$ is the Fermi-Dirac distribution and q is the electronic charge. The equivalent circuit model including the gate C_Q is shown in figure 2a. Figure

2b depicts the energy band diagram for the device (with p-doped bulk silicon) along the gate to channel direction. The first few energy bands of the gate material are schematically represented for the example case of a semi-metallic gate. V_{midgap} corresponds to the work function of the gate material in the intrinsic state. For example in the case of a graphene gate, V_{midgap} equals V_{Dirac} which corresponds to the Dirac point of graphene [11, 17]. In inversion, when a gate bias V_{GS} is applied to the MOSFET a potential difference V_Q develops across the gate corresponding to the charge Q_G. Equation 3 describes the relation among all the parameters mentioned here,

$$V_{GS} = V_Q + V_{OX} + (V_{midgap} - \Phi_s) + \psi_s \quad \ldots (3)$$

Here the voltage across the gate oxide $V_{OX} = (Q_G/C_{OX})$, ψ_s is the band bending in the channel near the interface and $\Phi_s = \left(\chi_{Si} + \frac{E_{G,Si}}{2} + \frac{kT}{q}\ln\left(\frac{N_A^-}{n_i}\right)\right)$ is the work function of bulk silicon with χ_{Si}, $E_{G,Si}$ n_i and N_A^- being the electron affinity, band gap, intrinsic carrier concentration and ionized acceptor ion concentration in bulk Si respectively [16]. In inversion, $\psi_s = 2\phi_f = \frac{2kT}{q}\ln\left(\frac{N_A^-}{n_i}\right)$ and Q_{INV} can be calculated using equation 4,

$$Q_{INV} = Q_G - Q_{DEP} = Q_G - qN_A^-\sqrt{\left(\frac{2\varepsilon_{Si}*2\phi_f}{qN_A^-}\right)} \quad \ldots (4)$$

Solving equations 1-4 numerically, V_Q, Q_G and Q_{INV} can be computed for a fixed value of the other parameters and for an applied bias V_{GS}. Details of the calculations are provided in the methods section and supporting information.

Using the electrostatic model developed here, V_Q, Q_G and Q_{INV} values are calculated as a function of V_{GS} for several different gate materials ranging from 3D, 2D to 1D gates (figure 3). The DOS for all the different gate materials used in the calculations are provided in figure S1. For 3D gates (figure 3a and 3d) we consider TiN and graphite gates with a thickness (h) of 100 nm. We observe that for bulk 3D gates like TiN and graphite having a large number of electronic states (obtained by the product of the DOS near the Fermi level and the volume of the gate electrode), V_Q is very small and almost zero (figure 3a) [18, 21, 22]. This is consistent with the case of a gate material with infinite DOS and hence infinite capacitance, for which $V_Q = 0$ for all values of Q_G. Correspondingly, Q_{INV} for 3D gates closely follows the expression for MOSFET inversion charge density given by $Q_{INV} = C_{OX} (V_{GS} - V_T)$ (figure 3d) [16]. Thus in the case of 3D gates, the gate DOS does not limit Q_{INV} and thus does not impact the MOSFET I_D characteristics.

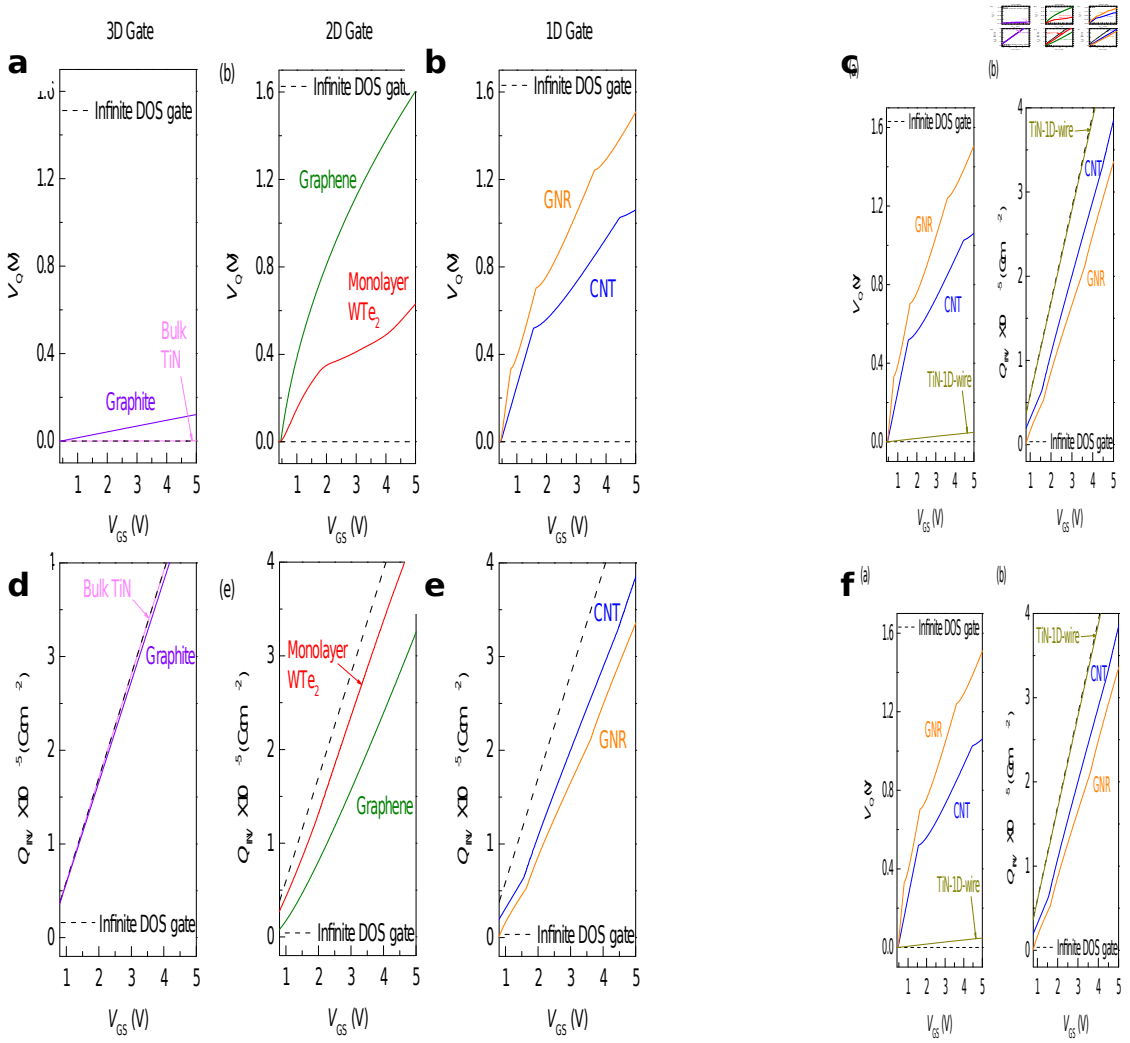

Figure 3: Electrostatic potential and charge calculations: (a-c) Electrostatic potential of the gate (V_Q) and **(d-f)** inversion charge density (Q_{INV}) versus V_{GS} for 3D, 2D and 1D gate electrode cases. 3D: 100 nm thick TiN and graphite, 2D: graphene and monolayer WTe_2, 1D: semiconducting GNR (n,m) = (15,0), metallic CNT (n,m) = (18,18) and 1x1 nm TiN wire. All calculations at T = 10 K. Dotted line indicates case for a gate with infinite DOS.

Figures 3b and 3e show the calculated values of V_Q and Q_{INV} for 2D gates, specifically for the case of graphene and monolayer WTe_2 which is metallic in the 1T phase [19, 23-25]. Due to the limited DOS for these gate materials and especially for graphene around the Dirac point, V_Q is a larger fraction of the applied V_{GS}, and correspondingly Q_{INV} is less than the value for the case of an ideal metal gate. Thus Q_{CH} is limited by the Q_G which is dictated by $g(E)$ for the gate. The impact of the gate DOS on Q_{INV} versus V_{GS} characteristics is most prominently visible for 1D gates. The specific cases considered here are a semiconducting graphene nanoribbon (GNR) with chirality (n,m) = (15,0) and a metallic CNT with chirality (n,m) = (18,18) as shown in figures 3c and 3f [20]. Quantization features resulting from the Van Hove singularities in the DOS for the GNR and CNT are visible in the V_Q versus V_{GS} and Q_{INV} versus V_{GS} characteristics in figures 3c and 3f respectively. Similar to the case of 2D gates the gate DOS limits the Q_{INV} and more interestingly the features of the gate DOS get capacitively mapped onto the transfer characteristics of the device because I_D is linearly proportional to Q_{INV}. Thus engineering the DOS of the gate is a useful technique to obtain desired transfer characteristics. All the calculations were performed for T = 10 K. The impact of temperature induced broadening is studied by calculating Q_G as a function of V_Q at T = 10 K and 300 K for the CNT and GNR cases mentioned earlier (see methods and figure S2).

The calculations for 1D gates and extension of the electrostatic model serves the purpose of relative comparison between materials. For the case of

finite 1D gates, obtaining exact electric field profiles from simulations and calculations are essential for quantitative accuracy. The assumptions are valid to the first order since L_{EFF} ~ the physical dimension of the gate especially in inversion which is the region of interest in this study. It is important to note that gate quantum capacitance effects would impact all devices but the level would depend on the material type. Metallic gates indeed show an effect similar to non-metal gates like graphene, CNTs and GNRs when their dimensions are comparable, albeit to a lower level due to the availability of much larger gate DOS as is shown for the example case of a 1x1 nm TiN 1D wire (figure 3 and S3). Large gate DOS is preferred for maximum Q_{INV} whereas a nanoscale low DOS gate would show more significant impact of C_Q on transistor characteristics. Another low-DOS material traditionally used in the semiconductor industry as a gate in the old generations of CMOS technology was polysilicon. Although poly-Si has lower DOS than metallic gates like TiN, it is important to consider that these materials will likely not scale to nanoscale dimensions compared to gates like CNT and GNR.

We experimentally demonstrate for the first time the effect of the gate C_Q on the I_DV_{GS} characteristics using an ultra-thin SOI channel (T_{SOI} ~ 2.5 – 3.5 nm, ~ 27.5 nm thick buried oxide (BOX) and ~ 3 nm thick Al_2O_3 top gate oxide) transistor with a single walled CNT top gate (L_G ~ 1 nm) (G), silicon substrate bottom gate (B) and nickel silicide source (S) and drain (D) contacts. The device structure is illustrated schematically in figure 4a. Figure

4b shows the top view optical microscope image of a representative device showing the Ni S/D fingers, the SOI channel and the Pd contacts to the CNT gate and the Ni S/D fingers. The CNTs are perpendicular to the CNT catalyst line seen in figure 4b [15], and can be clearly identified in a top view scanning electron microscope image (figure S4)

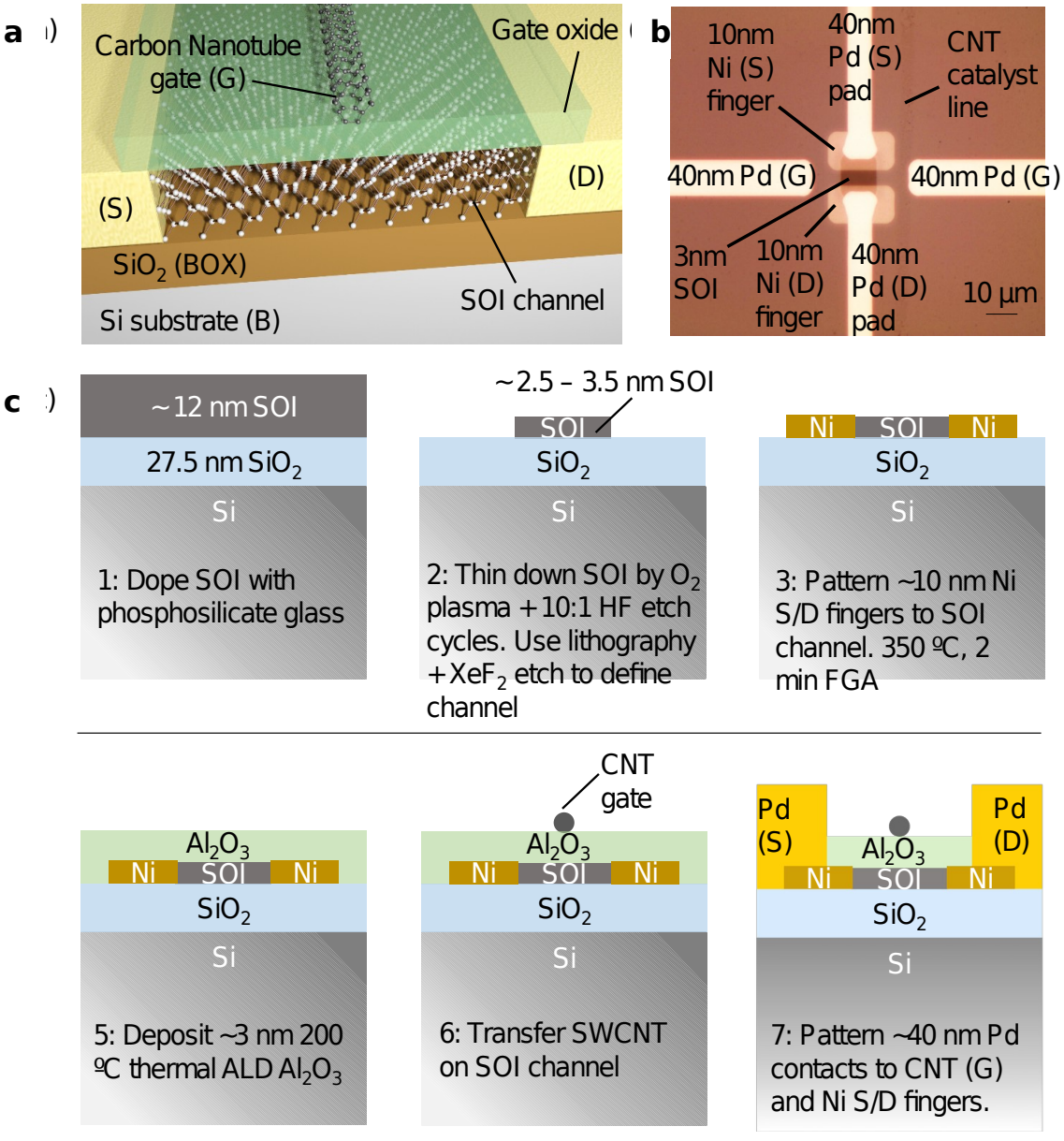

Figure 4: CNT gated SOI MOSFET device structure and process flow: **(a)** Schematic and **(b)** Optical microscope image of a representative device (top view). **(c)** Fabrication process flow

The fabrication process flow for the device is described in detail in figure 4c. The original SOI wafer has T_{SOI} ~ 12 nm which is heavily n-doped using phosphosilicate glass (PSG) (~ 5 × 19 cm^{-3} doping level) [26]. T_{SOI} is reduced using repeated cycles of O_2 plasma oxidation followed by etching of the oxide layer in 10:1 HF for 10 s [27]. A layer of SOI ~ 1.5 nm thick is removed for every cycle and T_{SOI} is monitored using ellipsometry, optical contrast and AFM measurements (figure S5). The impact of T_{SOI} on the $I_D V_{BS}$ characteristics is studied in figure S6 (for L_{CH} ~ 10 µm). I_D reduces dramatically as T_{SOI} decreases because of increasing contact and channel resistance (decreasing carrier mobility). An optimized device design with raised S/D (thicker SOI in the silicide contact regions) similar to modern commercial finFETs would help to lower the contact resistance and thus increase I_D. For T_{SOI} >> 3 nm, the bottom gate control is poor as evident from the low I_{ON}/I_{OFF} ratio in figure S6 indicating that the SOI layer is very heavily doped. The heavy doping of the SOI thus necessitates T_{SOI} ~ 3 nm to allow for good electrostatic control of both the gates on the entire thickness of the channel, and thus enable the observation of gate C_Q effects.

Once the SOI layer is of the desired thickness (T_{SOI} ~ 2.5 – 3.5 nm), the channel region is patterned using photolithography followed by XeF_2 vapor

etch. 10 nm thick Ni S/D finger contacts to the channel are patterned using photolithography followed by thermal evaporation and metal liftoff. The devices are annealed at this stage in 5% forming gas for 2 minutes at 350 ºC to form nickel silicide at the contacts which helps to reduce the contact resistance. Post silicidation, ~ 3 nm thick Al_2O_3 top gate oxide is deposited using thermal atomic layer deposition (ALD) at 200 ºC followed by the transfer of SWCNTs onto the devices [28]. Finally, ~ 40 nm thick Pd contacts are patterned to contact the CNTs as well as the Ni S/D fingers using photolithography followed by electron-beam evaporation and metal liftoff process. The rationale behind patterning the S/D contacts to the SOI in two steps using the 10 nm thick Ni S/D intermediary fingers is to minimize the topography height difference on the chip, which greatly impacts the yield of the CNT transfer step subsequently. All the details of the fabrication process flow are provided in the methods section.

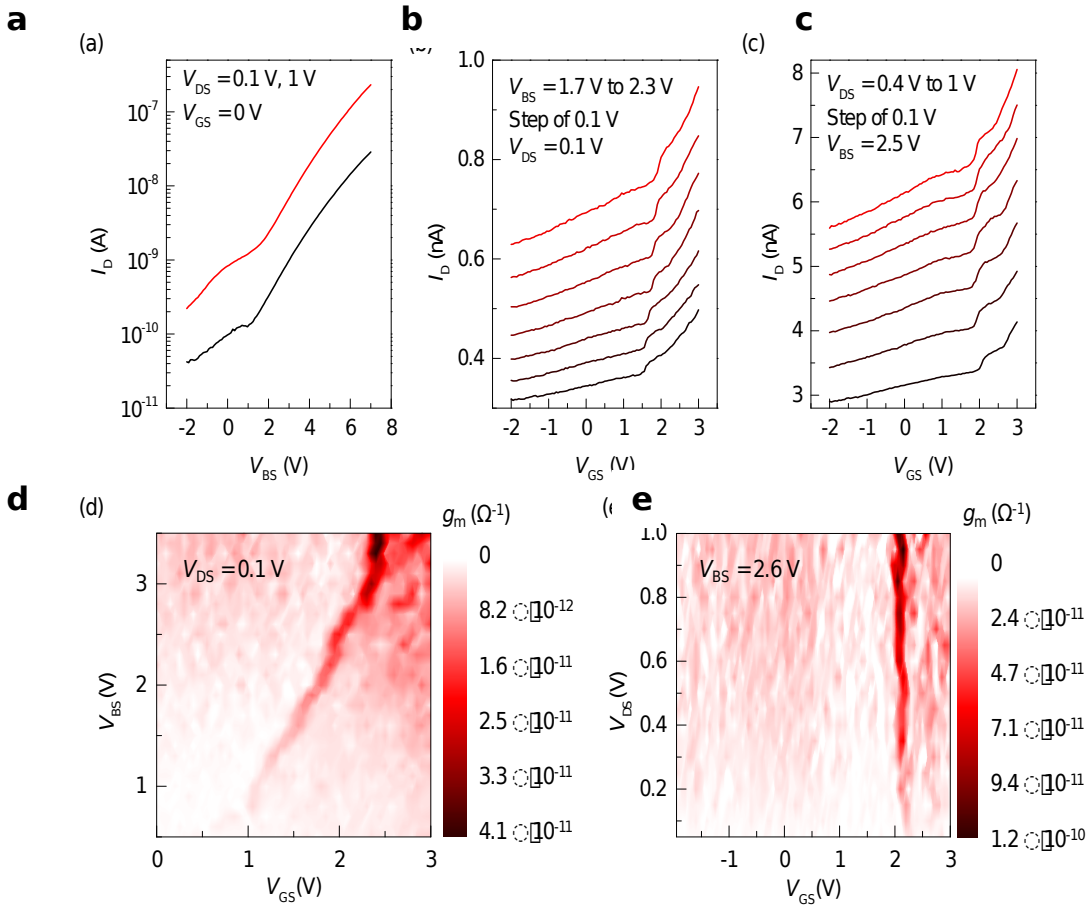

Figure 5: Electrical characteristics of CNT gated SOI MOSFET: (a) I_DV_{BS} **(b-c)** I_DV_{GS} for different V_{BS} and V_{DS} values respectively. g_m contour plots for **(d)** fixed V_{DS} and **(e)** fixed V_{BS} values respectively. Q_{CH} limited by Q_G due to finite DOS of CNT gate.

Figure 5 shows the room-temperature electrical characteristics measured for the CNT gated SOI MOSFET described in figure 4. The I_DV_{BS} characteristics for a fixed V_{GS} are shown in figure 5a. Figures 5b and 5c show the I_DV_{GS} characteristics for fixed V_{DS} and V_{BS} respectively, which have the quantization signature resulting from the Van Hove singularities and finite

DOS of the CNT gate as depicted in figure 3 and figure S2 [20]. The quantization features in $I_D V_{GS}$ correspond to the condition when the V_{GS} is large enough such that $E_{F,G}$ moves into the next higher sub-band of the CNT. This results in the observed jump in Q_G or Q_{INV} corresponding to the Van Hove singularity at the quantized energy level for the CNT. The influence of the bottom gate on the transfer characteristics can be qualitatively understood using figure 5b. As V_{BS} is increased Q_{CH} and Ψ_s both increase and a larger V_{GS} is required to surpass the same Van Hove singularity. Thus the position of the quantization features shift right with increasing V_{BS} as seen in figure 5b. This dependence of the position of the quantum energy levels on V_{BS} and V_{GS} can be mapped more directly using the g_m contour plot in figure 5d. V_{DS} does not alter the Q_{CH} and Ψ_s in the channel under the CNT significantly and hence does not affect the position of the quantization features as is evident from figure 5c and the g_m contour plot in figure 5e. The high contact resistance of the device due to thin (~ 3 nm) SOI in the silicided region also does not impact the transfer characteristics quantization features, except for lowering the overall value of I_D.

We note that the quantization features in the $I_D V_{GS}$ characteristics are not because of the ultra-thin nature of the SOI channel. This can be understood from the lack of quantization features in the long-channel $I_D V_{BS}$ characteristics in figure 5a as well as the T_{SOI} dependent $I_D V_{BS}$ measurements in figure S6. Two main sources of electron energy broadening exist in an electronic device, viz. thermal broadening and carrier scattering induced

distortion. The quantum-confined carriers present in the gate electrode are quasi-static and impact the I_D capacitively. Thus the carrier scattering induced distortion component is mitigated and would explain the observation of distinct quantization features in I_DV_{GS} at room temperature [6, 10]. The complete dataset for this device as well as electrical characteristics of other representative devices are provided in figures S7 – S9. The likely sources of hysteresis in the transfer characteristics shown in figures S7 – S9 are trapped charges in the ALD Al_2O_3 gate oxide and water molecules and contaminants on top of the CNT and the device which is unpassivated.

CONCLUSIONS

Thus we study the impact of gate C_Q on the electrical characteristics of nanoscale transistors using a bulk silicon MOSFET electrostatics model. For low-dimensional gates, Q_G can limit Q_{CH}. We experimentally observe for the first time at room-temperature, gate DOS limited I_DV_{GS} characteristics for a model system of an ultra-thin SOI channel transistor with a CNT gate. Further work would involve improving I_{ON} using raised S-D (thicker SOI to form nickel silicide), and increasing the prominence of quantization features by using a high-k top gate oxide to increase C_{OX}.

With continued scaling of transistors it will be of increasing importance to consider the impact of gate C_Q on transistor characteristics and I_D. This effect is generic in nature, independent of the device architecture (FinFET, Gate-all-around FET, etc.) and depends on gate DOS at very small

dimensions. A change of few percent in the On-current of a device is critical especially for high-performance technologies. Thus proper gate design and choice of the material will be important aspects in device design. By tailoring $g(E)$ in the gate, it would be possible to achieve desired transfer characteristics for the device. A specific example is the case of a 0D quantum dot gate on a 1D channel (figure S10). The δ-function gate DOS would result in step-like $I_D V_{GS}$ characteristics which can have potential applications like multi-state logic and memory [9]. Compared to other strategies for making multi-valued logic devices, for example: resonant tunneling transistor, FETs with multiple layers of quantum dots acting as floating gates and spatial-wave-function switched FET [29], the use of tailored DOS gate material may offer a simpler and more realizable device structure and gate stack. Additionally, the reduced total gate capacitance ($C_G^{-1} = C_{OX}^{-1} + C_Q^{-1}$) would affect the dynamic response of the device. It would be important to also consider the gate resistance of a low DOS material and its impact on the cut-off frequency (f_T), maximum frequency of oscillation (f_{max}), thermal noise and time response of the transistor, all of which also determine final circuit performance [30]. Proposals involving the use of low dimensional materials for other applications like the S/D contacts and interconnects, [12, 14] must also be investigated similarly.

METHODS

Device fabrication and characterization

The fabrication process starts with a silicon-on-insulator (SOI) wafer with ~ 12 nm thick SOI layer, ~ 27.5 nm thick buried oxide (BOX). Low-pressure chemical vapor deposition (LPCVD) phosphosilicate glass (PSG) is deposited on the wafer at 450 ºC, using silane, oxygen and 25% phosphine (in a Tystar furnace) [26]. Subsequently, rapid thermal annealing (RTA) was carried out at 1000 ºC for 30 s to drive dopants into the SOI layer. RTA was repeated 3 more times (total RTA time = 120 s), each time the wafer was rotated by 90º. This was performed to ensure the dopant drive-in and activation was uniform across the wafer, and to offset any non-uniformities in the RTA chamber heat profile. The PSG layer is then completely etched away in 10:1 HF. From ellipsometry, the thickness of the SOI layer post *n*-doping is ~ 9 – 9.5 nm.

The SOI layer is then thinned down using repeated cycles of silicon oxidation followed by removal of the oxide layer. The SOI layer is oxidized using O_2 plasma at 120 W power for 5 minutes. The oxide is then etched using a 10:1 HF dip for 10 s. This constitutes a single cycle, and removes ~ 1.5 nm thick SOI layer at a time. The process is repeated until the SOI layer is thinned down close to ~ 3 nm. Piranha / UV based oxidation may also be used to thin down the SOI layer controllably since it forms a self-limiting oxide layer ~ 1 nm thick similar to the O2 plasma method [27].

i-line photolithography process is used to pattern the SOI channel regions for the ~ 3 nm thick SOI layer. XeF_2 based etching (using Xactix system) is used to etch the unmasked SOI regions and form the channel. The

XeF_2 and N_2 pressures were set at 1 Torr and 7 Torr respectively, each etch cycle was 8 s long and 3 cycles were used. XeF_2 is highly selective against SiO_2, and this was the primary reason for selecting it as an etchant for the SOI channel step, because the BOX is relatively thin to start with. Post resist-removal, another photolithography step using a bilayer liftoff resist / i-line process is used to pattern the S/D fingers. Ni (10 nm) was deposited using thermal evaporation, and the contact finger regions were stripped of any native oxide in 50:1 HF for 25 s, immediately prior to loading the samples for evaporation. Post evaporation and metal liftoff in PG remover at 80 ºC for 30 min, the samples were annealed in 5% forming gas at 350 ºC for 2 minutes to form nickel silicide at the S/D finger regions and obtain good quality contacts to the SOI layer.

Al_2O_3 (~ 3 nm thick) is deposited on top of the device at 200 ºC using thermal ALD (Cambridge Fiji F200 system) based on TMA (Tri-methyl aluminum) and H_2O process. Single walled aligned carbon nanotubes (CNTs) (density of CNTs is ~ 1 – 3 CNTs per 5 µm) are then transferred on top of the device with the CNTs along the direction perpendicular to the SOI channel direction as described in the process details in reference [15, 28]. Finally, using bilayer resist photolithography, G contacts are patterned to the carbon nanotubes, and at the same time, pads to the Ni S/D fingers are also patterned. The sample is overdeveloped in the TMAH developer during this step in order to ensure that the ALD Al_2O_3 which is on top of the S/D fingers is completely etched away by the TMAH, ensuring that a good contact can be

formed between the S/D fingers and the S/D pads. Finally, 30 nm Pd is evaporated on the samples using electron beam evaporation, followed by metal liftoff in PG Remover at 80 ºC for 30 min to complete the device fabrication. The devices are characterized inside a Lakeshore vacuum probe station, at a pressure of ~ 1×10^{-5} mbar, using a B1500A / 4155C semiconductor parameter analyzer.

Electrostatic modeling and extraction of Q_{INV}

Q_{INV} is extracted from Q_G using equation 4. Q_G is obtained by solving equations 1 – 3. The units of C_Q are F cm^{-1}, F cm^{-2} and F cm^{-3} for 1D, 2D and 3D gates respectively. Q_{INV} and Q_G are charge densities per unit area. Hence for the case of 1D gates we use, $C_Q' = C_Q/L$ where, L is the length of the GNR or the diameter of the CNT. Similarly, for the case of 3D gates we use $C_Q' = C_Q*h$, where h is the thickness of the gate. For the examples considered in this work, L = 1.7217 nm for the GNR ((n,m) = (15,0)) and L = 2.4408 nm for the CNT ((n,m) = (18,18)) and h = 100 nm for the graphite and TiN 3D gates. V_{midgap} = 4.56 V (corresponding to the intrinsic work function of graphene) was assumed for all the materials in the calculations [17, 22, 31]. V_T = 4.56 V was also assumed when calculating Q_{INV} for an ideal MOSFET in figure 3. A different value of V_{midgap} would simply result in a lateral shift in the calculated plots in figure 3. Modified equations of bulk silicon properties were used in the calculations to account for the dependence on temperature [32].

$$N_C = 6.2\times10^{15}\times T^{3/2} cm^{-3}$$

$$N_V = 3.5 \times 10^{15} \times T^{3/2} cm^{-3}$$

$$E_{G,Si} = 1.17 - \frac{4.73 \times 10^{-4} T^2}{T + 636} eV$$

$$N_A^{-} = \sqrt{\frac{N_V N_A}{2}} e^{\frac{-E_A}{kT}}$$

Here N_A is the doping of bulk silicon, E_A corresponds to the Boron dopant activation energy in silicon which is 0.045 eV [33]. For all calculations, we assume $N_A = 10^{13}$ cm^{-3}, $T_{OX} = 2$ nm and dielectric constant of high-k oxide $k_{OX} = 25$.

Higher order effects in non-planar gates like CNTs, for example intra-CNT charge redistribution and electronic band structure modulation as a function of transverse electric fields must also be considered for achieving better quantitative accuracy [34-35]. The intra-CNT charge redistribution along its circumference is dependent on several factors, for example: CNT conductivity, DOS, polarization constant, electric field strength, chirality and diameter. Based on discussions in references 34-35, almost all Q_G would accumulate on the CNT circumference close to the CNT-oxide interface in strong inversion. Thus charge redistribution will likely not cause significant deviations from the simple analytical model used in this work which assumes Q_G to be at the gate-oxide interface. The impact of electric field on the band structure of the CNT, and hence the location of the quantization features in the device transfer characteristics however may be important, and requires

self-consistent first principle calculations with finite element method simulations to calculate exact electric field profiles.

ACKNOWLEDGEMENTS

The authors would like to thank Prof. Tsu-Jae King Liu, Juan Pablo Llinas and Dr. Angada Sachid for useful discussions. This work was supported by the Electronics Materials program funded by the Director, Office of Science, Office of Basic Energy Sciences, Material Sciences and Engineering Division of the U. S. Department of Energy under Contract No. DE-AC02-05CH11231. S.B.D. would like to acknowledge support from the Lam Research Graduate Fellowship.

Author contributions: S.B.D. and A.J. conceived the idea and wrote the manuscript. S.B.D., H.M.F. and T.L. fabricated the devices. S.B.D. performed the electrical characterization and electrostatic modeling with inputs from H.M.F. G.P. performed the growth of the single walled aligned carbon nanotubes. S.B.D. and H.K. obtained the images using a scanning electron microscope. S.B.D., H.M.F., and A.J. performed the data analysis. D.C. calculated the DOS for the TiN cases using Density Functional Theory (DFT). All authors revised the manuscript and did data analysis and interpretation.

Competing interests: The authors declare no competing financial interest

SUPPORTING INFORMATION

Supporting information accompanies this paper at:

Fig. S1: Density of states for different materials used in the calculations for figures 3 and S3

Fig. S2: Q_G – V_Q at T = 10 K, 300 K for CNT and GNR gate

Fig. S3: V_Q - V_{GS} and Q_{INV} - V_{GS} for 1D gate electrodes including case of 1x1 nm TiN 1D wire

Fig. S4: Scanning electron microscope (SEM) top-view images of a few representative devices

Fig. S5: Monitoring the thickness of SOI layer as a function of number of etch cycles

Fig. S6: $I_D V_{BS}$ characteristics for different values of T_{SOI} (L_{CH} ~ 10 μm)

Fig. S7: Additional data for device in figure 5

Fig. S8: Device data for device 2

Fig. S9: Device data for device 3

Fig. S10: Schematic for a conceptual device with a 0D quantum dot gate with a 1D CNT channel

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