Title

RD53A: A large-scale prototype chip for the phase II upgrade in the serially powered HL-LHC pixel detectors

Authors

Dimitrievska, Aleksandra

Stiller, Andreas

Collaboration, RD53

Publication Date

2020-04-01

DOI

10.1016/j.nima.2019.04.045

Peer reviewed

RD53A: a large-scale prototype chip for the phase II upgrade in the serially powered HL-LHC pixel detectors

Aleksandra Dimitrievska*

Lawrence Berkeley National Laboratory

Andreas Stiller

University of Applied Sciences and Arts Dortmund

on behalf of the RD53 Collaboration

Abstract

The phase II upgrade of the HL-LHC experiments within the LHC intends to deepen the studies of the Higgs boson and to allow the discovery of further particles by adding an integrated luminosity of about 4000 fb^{-1} over 10 years of operation. This upgrade would overwhelm the installed pixel detector readout chips with higher hit rates and radiation levels than ever before. To match these extreme requirements the RD53 collaboration, a joint effort between ATLAS and CMS, developed RD53A, a new generation pixel detector readout chip prototype manufactured in a 65 nm CMOS technology. It is half the size of the final pixel chips and designed to meet requirements in the face of 3 GHz/cm^2 hit rate after irradiation to 500 Mrad. The detector is able to use 50x50 μm^2 or 25x100 μm^2 pixels with high readout speed of up to 4 links per chip with 1.28 Gbit/s each. Shunt-LDO regulators integrated on the bottom of the chip provide the required voltages to the two power domains, analog and digital. These regulators enable serial powering of the pixel modules, which is the only feasible, radiation hard scheme to ensure acceptable power cable losses and to stay within the material budget for the future pixel detectors. An overview of the status and challenges of serial powering and the Shunt-LDO regulator development will be given.

Keywords: RD53A, front end electronics for detector readout, serial powering.

1. Introduction

The high luminosity LHC (HL-LHC) project [1] is foreseen to allow the detailed exploration of the TeV scale with total integrated luminosity of 4000 fb^{-1}. The HL-LHC will reach a factor of five larger instantaneous luminosity compared to the one at the LHC, enabling the ATLAS [2] and CMS [3] experiments to achieve the full physics potential beyond 2025: precision measurement in the Higgs sector, searches for new particles at high masses and studies of rare B-decays. The significant increase of the pile-up density requires replacement of the current tracking detectors with a new generation pixel detector in order to have fully performant experiments at HL-LHC. A new readout chip for the upgraded pixel detector has to meet specifications after 500 Mrad total dose received in the HL-LHC conditions.

In 2013 the RD53 Collaboration was constituent with the purpose to develop pixel readout integrated circuits for the next generation of pixel readout chips to be used for the ATLAS and CMS Phase II pixel detector upgrades [4]. The RD53 Collaboration consists of 24 Institutions from Europe and US with almost equal contributions from the ATLAS and CMS experiments [4].

A first large scale prototype, called RD53A [5], is produced in 65nm CMOS technology. RD53A is the basis for the production designs of ATLAS and CMS but it is not intended to be a final production chip and contains design variations for testing purposes, making the pixel matrix non-uniform. The RD53A chip size is 20.0 mm by 11.8 mm and the pixel matrix is 400 pixels wide by 192 pixel tall, where a pixel cell is 50x50 μm^2. The main specifications of the RD53A are derived from HL-LHC conditions: pixel hit rate 3 GHz/cm^2, trigger rate 1 MHz, total power per pixel less that 10 μW with low noise and low in-time threshold, the details can be found in [5, 6]. The RD53A chip was submitted in summer 2017 and the chip testing and characterization started in early 2018.

2. Serial Powering

Serial powering is the baseline choice for powering in CMS and ATLAS pixel detectors to reduce power losses on the supply lines and the amount of required cables. In these detectors pixel modules will be serially connected in chains of up to 13 units and supplied by a constant current source. Since the current is reutilized when flowing from one module to another the

*Speaker

Email addresses: adimitrievska@lbl.gov (Aleksandra Dimitrievska), andreas.stiller@fh-dortmund.de (Andreas Stiller)

supply current does not scale with number of installed modules in a chain. However, the current must be selected in such a way that the maximum module load current requirement can be reliably covered (Figure 1).

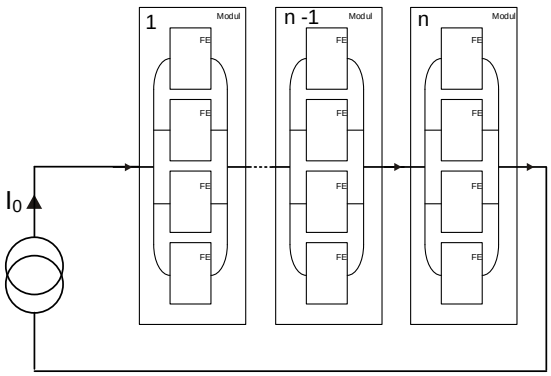

Figure 1: Example of a serial power chain.

RD53A achieves its serial powering capability using one on-chip Shunt-LDO regulator each for the analog and the digital domain. This regulator is characterized by a low mass, radiation hardness and robust parallel operation.

2.1. Shunt-LDO

The Shunt-LDO has been initially designed for the FE-I4[7] readout chip and has been redesigned in 65 nm technology with an increased shunt current capability of up to 2 A. As is shown in Figure 2 the IV-curve has a resistive characteristic to ensure that shunt current balancing across parallel connected regulators. The IV-curve slope is defined either by an internal or an external resistor. As a new feature the regulator comes with a configurable offset voltage, which is defined by means of an external resistor Rofs and is used as an additional parameter for the optimization of the power consumption (Figure 3). Another enhancement is addition of an improved control loop to assure stability even when driving high on-chip capacitive loads with low ESR.

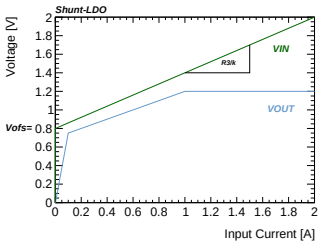

Figure 2: Simplified V-I curve of the RD53A Shunt-LDO.

The Shunt-LDO is a combination of a low drop-out linear voltage regulator and a shunt regulator (Figure 3) and as a result can operate in two possible modes. The first is the pure LDO regulator mode for use in conventional voltage-based powering schemes. The second mode is an extension to the first and adds dedicated shunt circuitry to enable current based powering in serially connected supply chains.

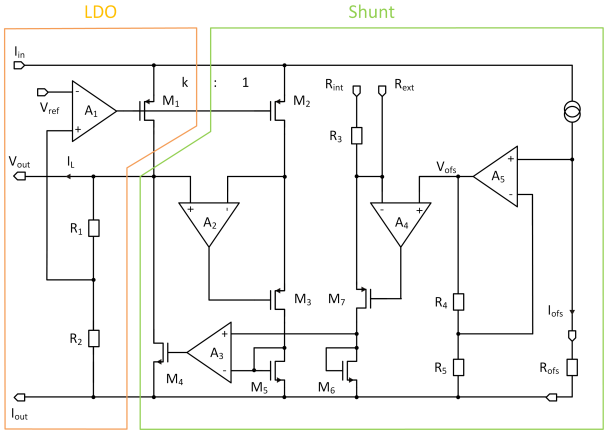

Figure 3: Simplified schematic of the Shunt-LDO: LDO (orange) Shunt (green).

For a balanced power distribution the pass device M1 and the shunt device M4 are split into four parts and spread across the pad frame.

2.1.1. Test Results

Measurements in LDO and Shunt-LDO modes and on analog and digital integrated regulators operated independent and in parallel, showed that the line regulation behavior is dominated by the bandgap voltages, used as references (Figure 4a,c). Using external references, the line regulation performance is enhanced by a factor of 10 (Figure 4b,d).

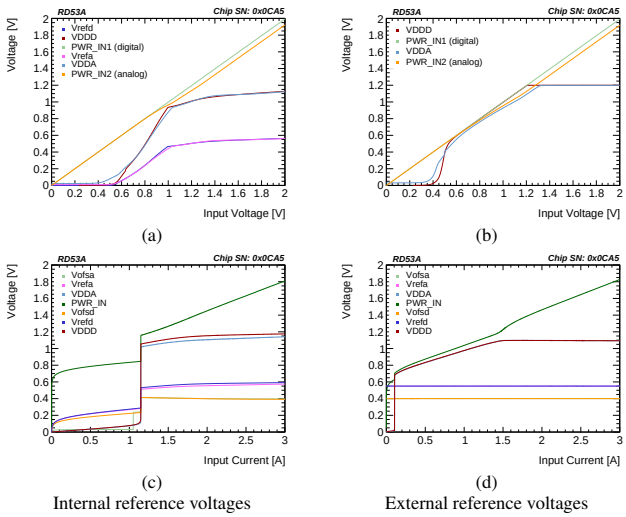

Figure 4: Line regulation measurements of (a,b) independent supplied regulators for analog and digital domain in LDO mode (c,d) parallel supplied regulator for analog and digital domain in Shunt-LDO mode

Further measurements show that the bandgap circuits have nearly no influence on the load regulation performance which is in the region of a few mV/A. Also, the transient response even during massive load changes of 0.5 A/ns shows small peaks of

about 50 mV which are regulated out in less than 1µs. Measurements of chip performance described in this note were made using the LDO mode with internal references.

3. The RD53A Characterization

3.1. Analog Front Ends

The RD53A pixel matrix is built up of 50 x 30 identical cores with 8 x 8 pixel each. Within one core the 64 front ends are placed as 16 analog islands with 4 fronts ends each, which are embedded in a flat digital synthesized "sea" [5]. One pixel core contains multiple pixel regions with shared logic and trigger latency buffering. The RD53A contains three different front end designs which are identified as synchronous, linear and differential.

The synchronous front end uses a baseline "auto-zeroing" scheme that requires periodic acquisition of a baseline instead of pixel-by-pixel threshold trimming.

The linear front end implements a linear pulse amplification in front of the discriminator, which compares the pulse to a threshold voltage.

The differential front end uses a differential gain stage in front of the discriminator and implements a threshold by unbalancing the two branches.

The front end designs share the pixel matrix area as shown in Figure 5. The synchronous front end is 16 core width while linear and differential are 17 core width. The detailed description of the different analog designs can be found in [5].

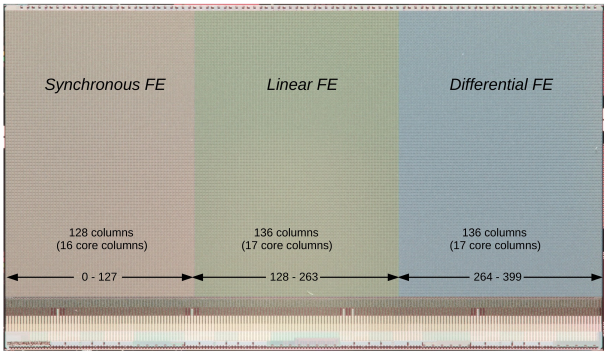

Figure 5: Arrangement of front end flavors in RD53A with indicated digital readout architecture. The pixel column number range of each flavor is shown along the bottom.

3.2. Test results

The RD53A testing and characterization started at the beginning of 2018. An extensive set of measurements were performed in order to characterize the performance of the different analog front end designs. All three front ends were tested independently. According to the conditions of the HL-LHC two operation points were defined corresponding to inner and outer layer of the pixel detector. Each front end was tuned individually for each operational point. After tuning, the equivalent noise charge (ENC) was measured for each front end as a function of per pixel current. Figure 6 shows noise for synchronous front end in orange, linear front end in green and differential front end in blue. The measurements were done at - 20 C with a bare chip.

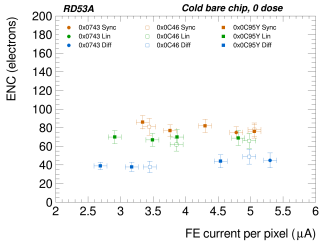

Figure 6: Measurement of noise as a function of per pixel current for different analog front end flavors for bare chip.

The same set of measurements were performed with irradiated chips. Multiple irradiation campaigns were performed during 2018. The bare irradiated chips which were included in this measurement were irradiated with x-rays at -20 °C to a total accumulated dose of 200 Mrad, 300 Mrad and 500 Mrad. The performance of the front ends after irradiation is shown on Figure 7, where the different front end flavors are shown separately: (a) synchronous, (b) linear and (c) differential, green points correspond to measurements of a non-irradiated chip, blue points represent the measurement with a bare chip which received total dose of 200 Mrad, black points refer to a measurement of a bare chip with 300 Mrad total dose received and red points are showing the measurement from a bare chip with total received dose of 500 Mrad. The performance of all front end flavors does not degrade with irradiation up to 500 Mrad, which validates a critical requirement.

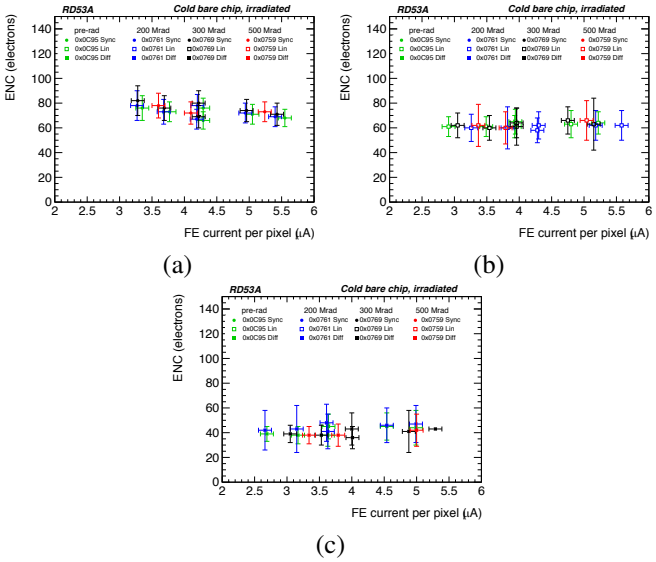

Figure 7: Measurement of noise as a function of per pixel current for different analog front end flavors (a) synchronous, (b) linear and (c) differential for bare chip. Measurement is performed with non irradiated chip, after 200 Mrad, 300 Mrad and 500 Mrad total received dose.

A requirement for the front end pixel readout chip is operation at low threshold since at the HL-LHC the sensors of the

pixel detectors will be thiner than in present detectors. Furthermore, the sensor signal will significantly degrade with radiation. In order to estimate minimal threshold for each front end a measurement of fraction of noisy pixels as a function of mean threshold has been performed. All front ends are tuned individually and number of pixels with a noise occupancy higher than 10^{-6} hits per bunch crossing is measured as a function of a mean threshold. The global threshold is lowered and the measurement is repeated. This procedure is highly dependent on the shape of the threshold distribution. It is assumed that the threshold distributions are Gaussian. The fraction of noisy pixels per analog front end as a function of a mean threshold with bare chip at -20 °C are shown on Figure 8 for the synchronous front end with orange points, linear with green and differential with blue points. The gray horizontal line labels 0.1 % of total pixels per front end.

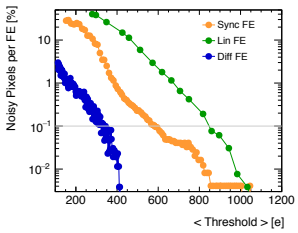

Figure 8: Measurement of fraction of noisy pixels per analog front end as a function of mean threshold for bare chip.

All measurements shown here are with a bare chip. For the full performance of the RD53A chip additional measurement with 50x50 μm^2 or 25x100 μm^2 pixels sensors are planed. This technique will be used to characterize the performance degradation as chips are combined into modules and modules integrated into serial power chains. This measurement is in progress.

RD53A tests and results show that the RD53A chip prototype is a solid baseline for final chip development. The first radiation tests show minimal degradation in analog performance up to 500 Mrad at cold temperature which is in agreement with simulation using post rad transistor models. All analog front ends are fulfilling specifications but all need additional modifications for the final chip. Testing and characterization of the RD53A chip will continue in parallel with the development of the final production chip.

4. Conclusion

The future upgrade of the HL-LHC requires a new generation readout chip for the pixel detectors, which should provide higher granularities and extraordinary performance in term of noise, speed, and readout. The new pixel readout chip has to meet specifications after unprecedented levels of radiation fluence and dose. The RD53 collaboration is a common effort of experts from ATLAS and CMS communities focused to deliver a pixel chip satisfying the main specification of both experiments for the HL-LHC. The RD53A, a readout chip prototype manufactured in a 65 nm CMOS technology, is showing very promising results. The Shunt-LDO regulator and consequently the serial powering scheme has proven to be very stable and reliable in all tests. A new bandgap scheme and some further safety features are being developed for integration in the final production chips, which will be submitted in July (ATLAS) and December (CMS) 2019, to improve reliability and robustness. The measurement results shown in this paper form a basis for performance characterization in a serial power system.

Acknowledgements

This work was supported by the Office of High Energy Physics of the U.S. Department of Energy under contract DE-AC02-05CH11231, and by the Federal Ministry of Education an Research of Germany (project number 05H18PRRD1). A.S. is gratefull for the scholarship of the Promotionskolleg of the University of Applied Sciences and Arts Dortmund.

References

[1] A. G., B. A. I., B. O., F. P., L. M., R. L., T. L., High-Luminosity Large Hadron Collider (HL-LHC): Technical Design Report V. 0.1.
URL https://cds.cern.ch/record/2284929

[2] ATLAS Collaboration, Technical Design Report for the ATLAS Inner Tracker Pixel Detector (CERN-LHCC-2017-021. ATLAS-TDR-030).
URL https://cds.cern.ch/record/2285585

[3] CMS Collaboration, CMS Technical Design Report for the Pixel Detector Upgrade (CERN-LHCC-2012-016. CMS-TDR-11).
URL https://cds.cern.ch/record/1481838

[4] RD53 web site, http://rd53.web.cern.ch/rd53/.

[5] RD53 Collaboration, The RD53A Integrated Circuit,CERN-RD53-PUB-17-001.

[6] P. Placidi, R. Collaboration, Recent progress of rd53 collaboration towards next generation pixel read-out chip for hl-lhc, HL-LHC Journal of Instrumentation 11. doi:10.1088/1748-0221/11/12/C12058.

[7] M. Karagounis et al., An integrated Shunt-LDO regulator for serial powered systems, Proceedings of ESSCIRC (2009) 276–279.