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# Understanding the Enhanced Mobility of Solution-Processed Metal-Oxide Thin-Film Transistors Having High-k Gate Dielectrics

By

Andre Zeumault

A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Engineering – Electrical Engineering and Computer Sciences

in the

Graduate Division

of the

University of California, Berkeley

Committee in charge:

Professor Vivek Subramanian, Chair
Professor Sayeef Salahuddin
Professor Oscar Dubon

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**Understanding the Enhanced Mobility of Solution-Processed Metal-Oxide Thin-Film Transistors Having High-k Gate Dielectrics**

# Abstract

Understanding the Enhanced Mobility of Solution-Processed Metal-Oxide Thin-Film Transistors Having High-k Gate Dielectrics

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Professor Vivek Subramanian, Chair

Primarily used as transparent electrodes in solar-cells, more recently, physical vapor deposited (PVD) transparent conductive oxide (TCO) materials (e.g. ZnO, $In_2O_3$ and $SnO_2$) also serve as the active layer in thin-film transistor (TFT) technology for modern liquid-crystal displays. Relative to a-Si:H and organic TFTs, commercial TCO TFTs have reduced off-state leakage and higher on-state currents. Additionally, since they are transparent, they have the added potential to enable fully transparent TFTs which can potentially improve the power efficiency of existing displays.

In addition to PVD, solution-processing is an alternative route to the production of displays and other large-area electronics. The primary advantage of solution-processing is in the ability to deposit materials at reduced-temperatures on lower-cost substrates (e.g. glass, plastics, paper, metal foils) at high speeds and over large areas. The versatility offered by solution-processing is unlike any conventional deposition process making it a highly attractive emergent technology.

Unfortunately, the benefits of solution-processing are often overshadowed by a dramatic reduction in material quality relative to films produced by conventional PVD methods. Consequently, there is a need to develop methods that improve the electronic performance of solution-processed materials. Ideally, this goal can be met while maintaining relatively low processing temperatures so as to ensure compatibility with low-cost roll-compatible substrates.

Mobility is a commonly used metric for assessing the electronic performance of semiconductors in terms of charge transport. It is commonly observed that TCO materials exhibit significantly higher field-effect mobility when used in conjunction with high-k gate dielectrics (10 to $100\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$) as opposed to conventional thermally-grown $SiO_2$ (0.1 to $20\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$). Despite the large amount of empirical data documenting this bizarre effect, its physical ori-

gin is poorly understood.

In this work, the interaction between semiconductor TCO films and high-k dielectrics is studied with the goal of developing a theory explaining the observed mobility enhancement. Electrical investigation suggests that the mobility enhancement is due to an effective doping of the TCO by the high-k dielectric, facilitated by donor-like defect states inadvertently introduced into the dielectric during processing. The effect these states have on electron transport in the TCO is assessed based on experimental data and electrostatic simulations and is found to correlate with negative aspects of TFT behavior (e.g. frequency dispersion, gate leakage, hysteresis, and poor bias stability).

Based on these findings, we demonstrate the use of an improved device structure, analogous to the concept of modulation doping, which uses the high-k dielectric film as an encapsulate, rather than a gate-dielectric, to achieve a similar doping effect. In doing so, the enhanced mobility of the TCO/high-k interface is retained while simultaneously eliminating the negative drawbacks associated with the presence of charged defects in the gate dielectrics (e.g. frequency dispersion, gate leakage, hysteresis, and poor bias stability). This demonstrates improved understanding of the role of solution-processed high-k dielectrics in field-effect devices as well as provides a practical method to overcome the performance degradation incurred through the use of low-temperature solution-processed TCOs.

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# Chapter 1

# Introduction

## 1.1 Conventional Role of High-k Gate-Dielectrics in Field-Effect Transistors

Transistor design seeks to maximize the response of the gate-induced charge in the semiconductor channel. The ability to modulate semiconductor charge is ultimately limited by the electronic properties of the gate-dielectric. Ideally, it is desirable to have gate-dielectrics with high permittivity, low loss and high breakdown fields. Unfortunately, a truly ideal gate-dielectric possessing all of these properties does not exist due to a combination of physical trade-offs and limitations. For example, materials which are good insulators (i.e. large band gaps) tend to have low dielectric constants (Figure 1.1, page 2). Furthermore, defect formation is unavoidable, leading to additional conduction pathways that enhance losses. Consequently, gate-dielectric optimization is a sensitive component of transistor design.

Historically, aggressive scaling of physical dimensions of transistors has necessitated the use of high-permittivity (i.e. "high-k") dielectrics in high-performance electronics in order to lower operating voltages and increase current density. However, frequency-dependent loss mechanisms lead to loss of electric polarization, ultimately limiting the ability to maintain high dielectric constants at high operating frequencies 1.2. These include [91]:

1. Ionic motion, charge trapping and space charge formation ($10^{-2}$ to $10^2$ Hz; $10^{-17}$ to $10^{-13}$eV)

2. Rotation of molecular dipoles ($10^5$ to $10^7$ Hz; $10^{-10}$ to $10^{-8}$eV)

3. Relaxation of molecular dipoles ($10^{11}$ to $10^{13}$ Hz; $10^{-4}$ to $10^{-2}$eV)

4. Electronic relaxation ($10^{15}$ to $10^{16}$ Hz; 1-10 eV)

Furthermore, high-k dielectrics routinely exhibit non-ideal insulating behavior. Apart from their characteristically high-permittivity, their integration into transistors has been
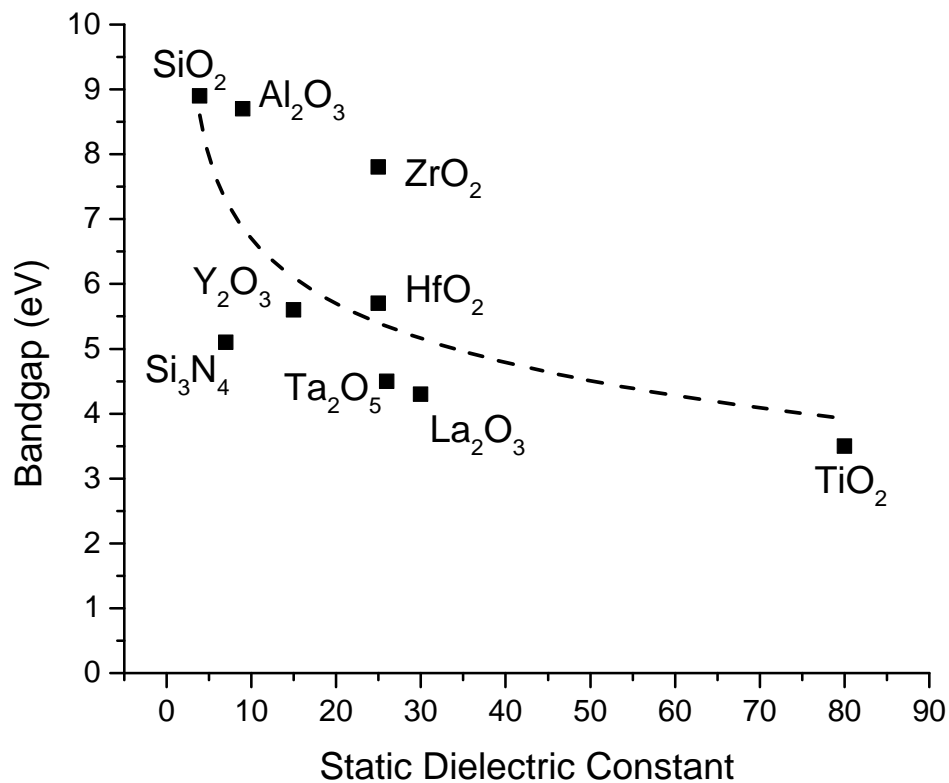
Figure 1.1: Optical band-gap energy versus static dielectric constant for various dielectrics according to [91] with a logarithmic fit indicating the general trend.

complicated by their tendency to contain various charged defects such as fixed charges, interface traps, bulk traps and mobile ions. [54] The effect this has on silicon MOSFETs is well studied and is often characterized by hysteresis in the transfer characteristics, bias/temperature instability and/or a degradation in field-effect mobility due to remote charge scattering [43].

Emergent transistor technologies based on solution-processed semiconductor materials face similar challenges when incorporating high-k gate dielectrics [94]. However, due to fundamental differences in the nature of transport in ordered (i.e. band-like) and disordered semiconductors (i.e. hopping), the interaction between the defect states of the semiconductor and dielectric do not lead to observations consistent with conventional transistor behavior [92].
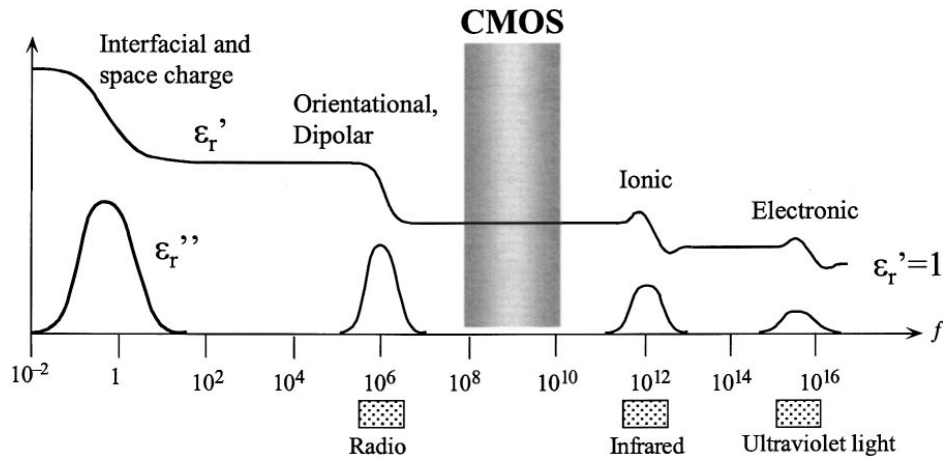
Figure 1.2: Polarization loss mechanisms from [91].

## 1.2 Thin-Film Transistors

### Historical Precedence of TFTs

Thin-film transistors (TFT) offer reduced-cost transistor functionality on unconventional substrates (e.g. glass, plastic and metal foils) for applications where the use of monolithic single-crystalline silicon MOSFETs is either unavailable or unfeasible due to cost or processing restrictions. Unlike conventional MOSFETs, the semiconductor channel in a TFT is deposited, leading towards the formation of amorphous or polycrystalline thin-films [58]. The higher degree of structural disorder present within these films leads to electronic defects that play a decisive role in transistor switching and electronic transport [42]. It is common for TFTs to exhibit low-mobility and threshold voltage instability due to a combination of high concentrations of defects, slow-electronic relaxation and lower energy barriers to defect creation [39]. For these reasons, TFTs have been largely limited to low-performance applications whereby a minimal switching delay is not a critical transistor specification. Although the predominant industrial application of TFTs is in liquid-crystal displays (LCD), they are also used in medical imagers, non-LCD flat panels, imagers/scanners/printers, photo-transistors and chemical sensors [46, 47, 42].

Higher performance (i.e. higher mobility) channel materials for TFTs tend to be polycrystalline (e.g. II-VI materials or polysilicon). A sufficiently high channel mobility, although unnecessary for LCD pixel switching, is desirable since it allows drive-circuitry to be integrated on the TFT backplane using the same transistor technology. Despite a higher mobility, polycrystalline materials have the unfortunate drawback of grain-boundaries distributed somewhat randomly over the backplane that sharply impact electrical behavior and display uniformity over large-areas [47]. Predicting the number and location of grain boundaries is a difficult task for device modeling. Consequently, the electrical properties of polycrystalline materials tend to vary over large areas. Alternatively, amorphous materials do not
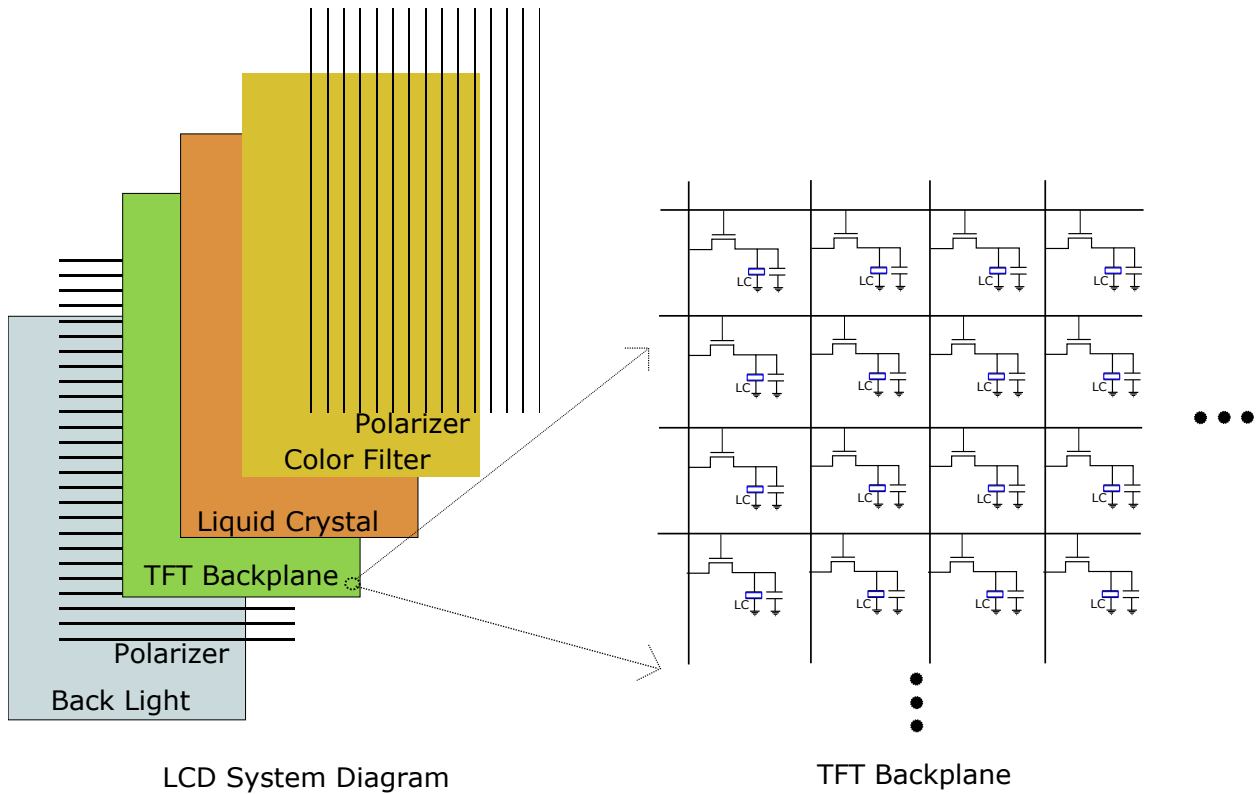
Figure 1.3: Illustration depicting basic AMLCD system layout and TFT backplane

contain grain boundaries and are therefore more desirable for large-area TFT applications (e.g. displays). Historically, active-matrix liquid crystal display (AMLCD) applications have focused almost exclusively on amorphous silicon for the TFT backplane (Figure 1.3, page 4) although, in recent years, amorphous InGaZnO has emerged as a superior alternative [36].

## Transistor Structure and the Gradual Channel Approximation

TFTs come in four possible device configurations depending on the placement of the gate electrode and source/drain contacts relative to each other: staggered, inverted-staggered, coplanar and inverted-coplanar (Figure 1.4, page 5). Coplanar devices have the semiconductor and source/drain contacts adjacent to the same side of the gate dielectric. Alternatively, staggered devices only have the semiconductor in contact to the gate dielectric. The term inverted refers to the placement of the gate electrode (top = normal, bottom = inverted).

TFT operation can be qualitatively described in an analogous way to that of a MOSFET operating only in accumulation and depletion (Figure 1.5, page 6). Inversion is unlikely due to the combination of large band-gaps and the high concentrations of compensating defect states near the band edge of the majority type [87]. Consequently, metal oxide TFTs have
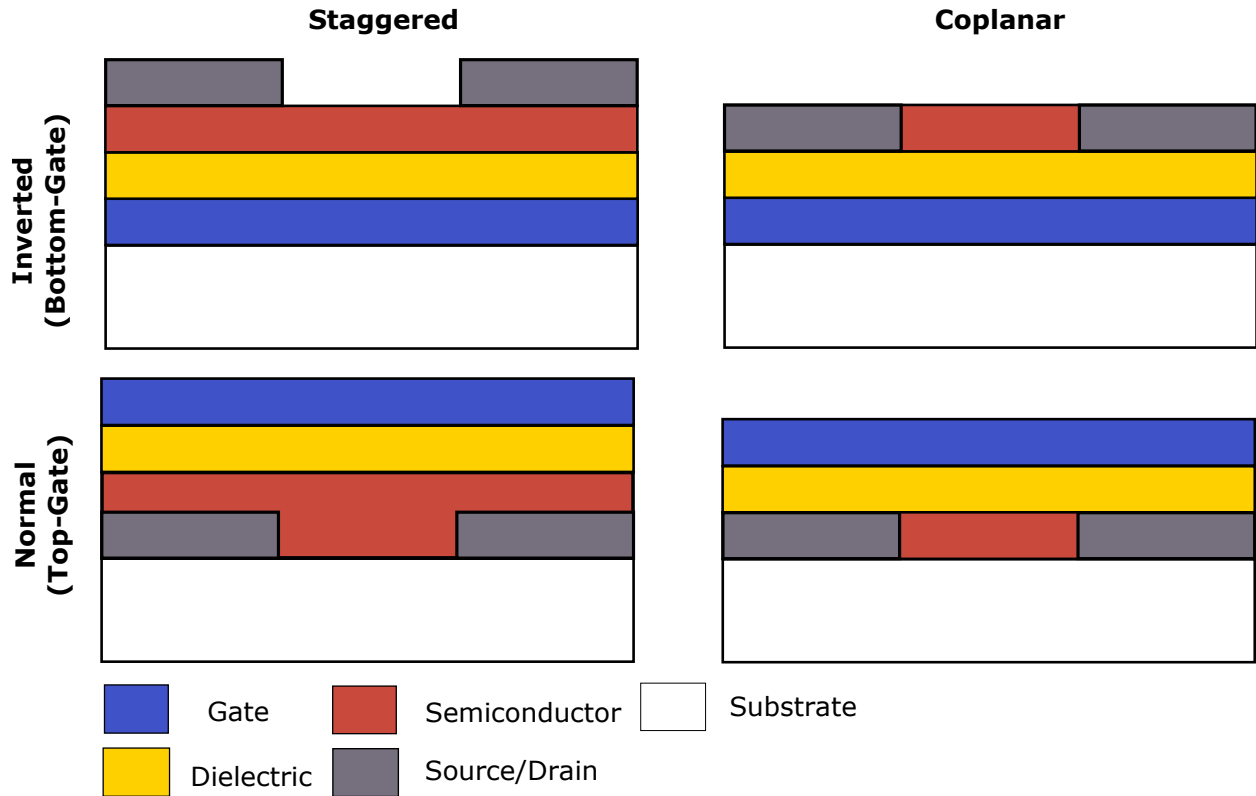
Figure 1.4: Different types of TFT structures.

almost exclusively unipolar transport with electrostatics essentially governed by one carrier type.

In a TFT, the *on* state corresponds to accumulation, when the majority carrier type is more abundant at the surface than the bulk. Conversely, the *off* state corresponds to depletion, when the majority carrier type is less abundant at the surface than the bulk. In practice, the channel material in a TFT is usually made very thin in order to optimize gate-control and charge-modulation. As a result, it is often convenient to approximately describe the channel in the limiting cases as being either fully-accumulated while *on* or fully-depleted while *off*.

A first order theoretical model of transport in a TFT is based on Shockley's analysis of JFETs [78] and is referred to today as the gradual channel approximation (GCA). This model assumes that the electrostatics are one-dimensional, controlled primarily by the application of a gate field. In this sense, the model is identical to simple long-channel MOSFET models where the threshold voltage has been replaced by the flatband voltage to account for accumulation-mode operation. The application of a non-zero drain-to-source voltage causes the local potential in the channel to vary between the source potential at the source and
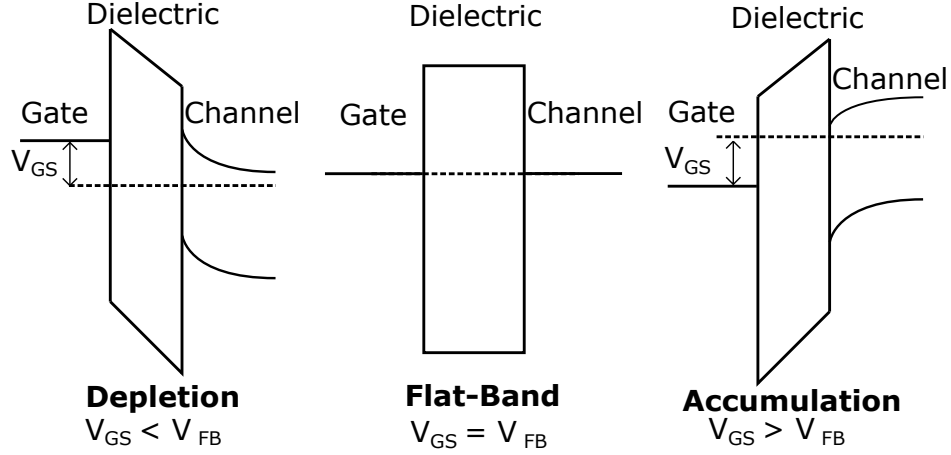
Figure 1.5: TFT modes of operation.

the drain potential at the drain. Assuming that the dielectric is ideal and the mobility is constant, integration of the charge along the channel leads to the well-known square-law model:

$$Q_{ind}(x) = C_{ox}\left(V_{GS} - V_{FB} - \phi(x)\right) \tag{1.1}$$

$$I_D = W\mu_n Q_{ind}\frac{d\phi(x)}{dx} \tag{1.2}$$

$$\int_{x=0}^{x=L} I_D dx = W\mu_n C_{ox}\int_{\phi=0}^{\phi=V_{DS}}\left(V_{GS} - V_{FB} - \phi(x)\right)d\phi \tag{1.3}$$

$$I_D = \frac{W}{L}\mu_n C_{ox}\left(V_{GS} - V_{FB} - \frac{V_{DS}}{2}\right)V_{DS} \tag{1.4}$$

As shown in the next section, the quantitative failures of the overly simplistic square-law model stems primarily from its assumptions related to the channel mobility which is assumed to be a constant material parameter. Improved accuracy can be obtained by accounting for defects in the channel using a more appropriate transport formalisms for highly defective (i.e. disordered) semiconductors.

## 1.3  Transport in Disordered Systems

Unlike well-ordered crystalline materials, electronic transport in disordered semiconductors is not exclusively due delocalized states (i.e. band-like) but also includes contributions from localized states distributed below the conduction band. With regard to field-effect devices, the presence of such states (Figure 1.6, page 7) causes the semiconductor channel to accumulate charge via the gradual filling of trap states. These states are broadly distributed in

energy, and transport can occur within a wide range of energy levels depending on the degree of orbital overlap. This ultimately leads to what is known as **dispersive transport**, as opposed to **gaussian transport** observed in ordered semiconductors 1.8. For these reasons, the device physics of TFTs differs substantially from that of conventional silicon MOSFETs. Square-law models derived from simple theories (e.g. the gradual channel approximation) developed for well-ordered silicon provide a qualitative, but quantitatively inaccurate, description of TFT behavior.
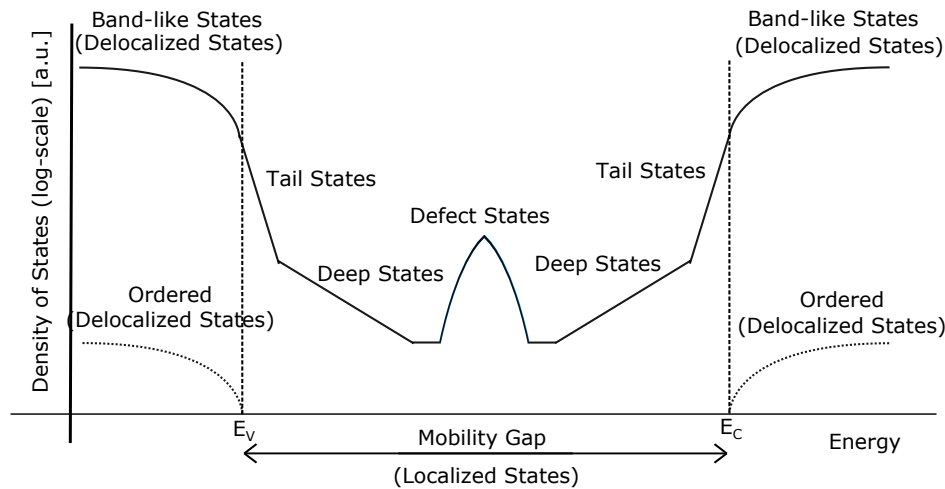


Figure 1.6: Typical density of states for a disordered semiconductor. Band tails and deep states are exponentially decreasing functions of energy, moving away from the conduction band toward mid-gap. For reference, the density of states for an ordered semiconductor are also shown. (dashed line)

Experimentally, dispersive transport is most commonly studied opto-electronically through time-of-flight or transient photoconductivity measurements [30] or electrically through measurements of thermally-activated conduction [12]. Observation of thermally-activated conduction provides a more fundamental distinction between the transport mechanism of ordered systems ($\frac{\partial \mu}{\partial T} < 0$) and disordered systems ($\frac{\partial \mu}{\partial T} > 0$). Models describing thermally-activated conduction in disordered solids include percolation conduction [81], hopping [25], barrier-lowering [77] and multiple-trap-and-release (aka trap-limited conduction) [50].

## Hopping Conduction Between Localized States

Hopping conduction consists of a sequence of incoherent electronic transitions occurring between pairs of localized states separated in energy and/or space (Figure 1.7, page 8) [4]. Since each transition is incoherent, the electron is described as randomly "hopping" between spatially distributed localized states.
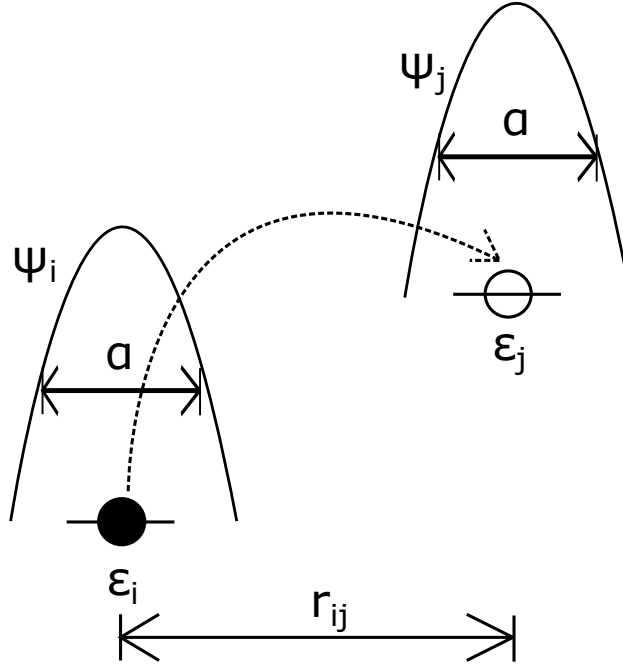
Figure 1.7: Illustration of hopping process.

The transition rate between a state at energy $\epsilon_i$ to a state at energy $\epsilon_j$, separated by a distance $r_{ij}$ is given by the following, which is essentially a Fermi's Golden Rule expression with a Bolztmann factor based on the principle of detailed balance:

$$\nu_{ij}(r_{ij}, \epsilon_i, \epsilon_j) = \nu_0 e^{-\frac{2r_{ij}}{\alpha}} e^{-\frac{\epsilon_i - \epsilon_j + |\epsilon_i - \epsilon_j|}{2k_B T}} \tag{1.5}$$

The parameter $\alpha$ describes the spatial extent of the wave-function corresponding to the localized state and is referred to as the localization length. As localization length increases, the wave-function extends farther radially outward becoming more spatially delocalized. Conversely, as the localization length reduces, the wave-function becomes sharply peaked about its center, overlapping less with neighboring states and therefore becoming more spatially localized.

For semiconductor devices with contacts, it is necessary to include the effect of the Fermi level on the occupation probabilities of states $\epsilon_i$ and $\epsilon_j$. Taking the Fermi level into account, yields the following:

$$\nu_{ij}(r_{ij}, \epsilon_i, \epsilon_j) = \nu_0 e^{-\frac{2r_{ij}}{\alpha}} e^{-\frac{|\epsilon_i - \epsilon_F| + |\epsilon_j - \epsilon_F| + |\epsilon_j - \epsilon_i|}{2k_B T}} \tag{1.6}$$

In order to arrive at an expression for the conductivity, the transition rate is optimized by considering the spatial coordinate as well as energy. However, simplifying assumptions based

on temperature are usually made. At high temperatures, the energy difference between defect states is non-limiting since carriers can easily absorb energy from phonons present in higher concentrations. Instead, spatial separation is limiting. As a consequence, the transition rate is maximized for transitions occurring over very short distances (i.e. $r_{ij} \to 0$). This is referred to as nearest-neighbor hopping (NNH). Due to the larger thermal energy, only information regarding the spatial distribution of defect states is necessary. Typically, defects are assumed to be spatially distributed at random, estimated within a sphere of radius $R_c$ to be some constant value $B_c$ as determined by percolation theory:

$$\frac{4\pi}{3} N_t R_c^3 = B_c \tag{1.7}$$

$$\nu = \nu_0 e^{-2\left(\frac{B_c}{\frac{4}{3}\pi\alpha^3 N_t}\right)^{\frac{1}{3}}} \tag{1.8}$$

Conversely, at lower temperatures, the energy difference between states is a larger fraction of the available average thermal energy $(1.5 k_B T)$. As a result, the transition rate is maximized for transitions requiring energy much less than the thermal energy, which may involve larger spatial separations. This is referred to as variable-range hopping (VRH). Here, knowledge of the density of states in the vicinity of the Fermi energy is needed in order to express the transition rate:

$$g(\epsilon_F)\Delta\epsilon r^3(\Delta\epsilon) = 1 \tag{1.9}$$

$$\nu = \nu_0 e^{-\frac{2}{g(\epsilon_F)\Delta\epsilon\alpha^3} - \frac{\Delta\epsilon}{k_B T}} \tag{1.10}$$

The final expression for the transition rate is obtained by maximizing the above expression as a function of the energy separation $\Delta\epsilon$.

$$\frac{d\nu}{d\Delta\epsilon} = 0 \tag{1.11}$$

$$\Delta\epsilon = \left(\frac{2k_B T}{3g^{\frac{1}{3}}(\epsilon_F)}\right)^{\frac{3}{4}} \tag{1.12}$$

$$\nu = \nu_0 e^{-\left(\frac{T_0}{T}\right)^{\frac{1}{4}}} \tag{1.13}$$

$$T_0 = \frac{\beta}{k_B g(\epsilon_F)\alpha^3} \tag{1.14}$$

## Multiple Trap and Release

Hopping conduction between localized states is expected whenever trap concentrations are high enough that they begin to interact. An example of this is the impurity band that

forms in conventional semiconductors at high doping concentrations [16]. Hopping is also present in disordered materials due to high concentrations of defects [63]. However, hopping tends to be only practically significant at low temperatures [27]. At higher temperatures, phonons are more numerous and the thermal energy is higher, leading to phonon absorption promoting localized electrons into higher-energy extended states. By comparison, hopping events contribute negligibly to the overall conductivity:

$$\sigma_{total} = \sigma_{loc} + \sigma_{ext} \approx \sigma_{ext} \tag{1.15}$$

Particularly useful in high-mobility systems ($> 10 \, \mathrm{cm^2 \, V^{-1} \, s^{-1}}$), MTR theory provides quantitative agreement to empirical current-voltage data (room temperature and above) and is based on a relatively straightforward physical interpretation. Here, electrons associated with defect states (distributed arbitrarily in energy) are assumed immobile. As a result, only trap states in steady-state equilibrium with conductive states make contributions to drain current. Carrier motion is therefore diffusive, in which the energy barrier to motion corresponds to the trap depth below the conduction band edge (aka mobility edge).

These assumptions lead to the use of simple semi-classical drift/diffusion based electrostatic models derived from well-known defect profiles and provides a physically-intuitive definition of the effective mobility as the time-averaged drift mobility [82]:

$$\mu_{eff} = \frac{1}{t_{free} + t_{trapped}} \int_0^{t_{free} + t_{trapped}} \mu(t) dt \tag{1.16}$$

$$= \frac{1}{t_{free} + t_{trapped}} \Big( t_{free} \mu_{free} \Big) \tag{1.17}$$

$$= \Big( \frac{t_{free}}{t_{free} + t_{trapped}} \Big) \mu_{free} \tag{1.18}$$

The effective mobility is therefore interpreted as the band mobility weighted by the fraction of time the charge carrier is spent free. Transport therefore is approximated as a periodic sequence of regular trapping and release intervals corresponding to the lifetime of delocalized and localized states, hence the term, multiple-trap-and-release.

Regarding MTR, a rigorous approach regarding the dynamics of carrier trapping has been given by [74], however the essential properties of multiple-trap-and-release processes can be elucidated by simple models, corresponding to a set of rate equations describing electronic transitions between delocalized and localized states [30]:

$$\frac{\partial n}{\partial t} = g - \nu_0 \Big( \frac{N_t}{N_c} \Big) n + \nu_0 n_t e^{\frac{E_t - E_c}{k_B T}} - \frac{n}{\tau_0} \tag{1.19}$$

$$\frac{\partial n_t}{\partial t} = \nu_0 \Big( \frac{N_t}{N_c} \Big) n - \nu_0 n_t e^{\frac{E_t - E_c}{k_B T}} - \frac{n_t}{\tau_t} \tag{1.20}$$

Here, $\tau_0$ is the lifetime of delocalized states whereas $\tau_t$ is the lifetime of localized states. The latter describes hopping of localized electrons into deeper localized states. $N_c$ and $N_t$ are the effective conduction band density of states for localized states and delocalized states respectively, $\nu_0$ is the attempt-to-escape frequency and $g$ represents carrier generation due to light-absorption (if present). The total carrier concentration is therefore:

$$\frac{\partial(n + n_t)}{\partial t} = g - \frac{n + n_t}{\tau_r} \tag{1.21}$$

Where $\tau_r$ is a time constant describing the decay rate of the total carrier concentration and is defined as:

$$\frac{1}{\tau_r} = \frac{1}{\tau_0}\frac{n}{n + n_t} + \frac{1}{\tau_t}\frac{n_t}{n + n_t} \tag{1.22}$$

MTR assumes that hopping in localized states is negligble. This simplifies $\tau_r$ to the following:

$$\frac{1}{\tau_r} \approx \frac{1}{\tau_0}\frac{n}{n + n_t} \tag{1.23}$$

Taking the inverse and assuming an exponential density of states distribution for $n_t$ leads to the following expression for $\tau_r$:

$$\tau_r = \tau_0\frac{n + n_t}{n} \approx \tau_0\frac{n_t}{n} = \tau_0 e^{\frac{E_c - E_t}{k_B T}} \tag{1.24}$$

Based on the definition of the photoconductivity, the drift mobility will be inversely proportional to the lifetime:

$$\sigma_{ph} = eg\mu\tau_0 = eg\mu_d\tau_r \tag{1.25}$$

$$\mu_d = \frac{\sigma_{ph}}{eg\tau_r} \tag{1.26}$$

This predicts that the mobility will be thermally activated and proportional to the fraction of delocalized states relative to localized states. In steady-state, this provides a defining relation for the mobility as a function of the trapped and free electron concentrations by way of the channel conductance:

$$G_D = \frac{\partial I_D}{\partial V_{DS}} = \frac{W}{L}\mu_{free}Q_{free} = \frac{W}{L}\mu_{eff}\Big(Q_{free} + Q_{trapped}\Big) \tag{1.27}$$

$$\mu_{eff} = \Big(\frac{Q_{free}}{Q_{free} + Q_{trapped}}\Big)\mu_{free} \tag{1.28}$$

Furthermore, this simple framework also provides the theoretical basis needed to describe the characteristically broad photoconductivity decay of disordered semiconductors often referred to as "dispersive transport", as opposed to "gaussian transport" observed in ordered semiconductors. The former is often used to justify the use of a particular defect distribution over another. Observation of excited state lifetime either through capacitance (DLTS) or current (photoconductivity) provides information on the distribution of defect states. For a monoenergetic trap, thermalization occurs over a time scale corresponding to the capture time. However, for a distribution of states, the rate of thermalization is limited by the slow thermally-activated release of carriers from deep localized states whose occupation precludes free-carrier trapping (Figure 1.8, page 12).
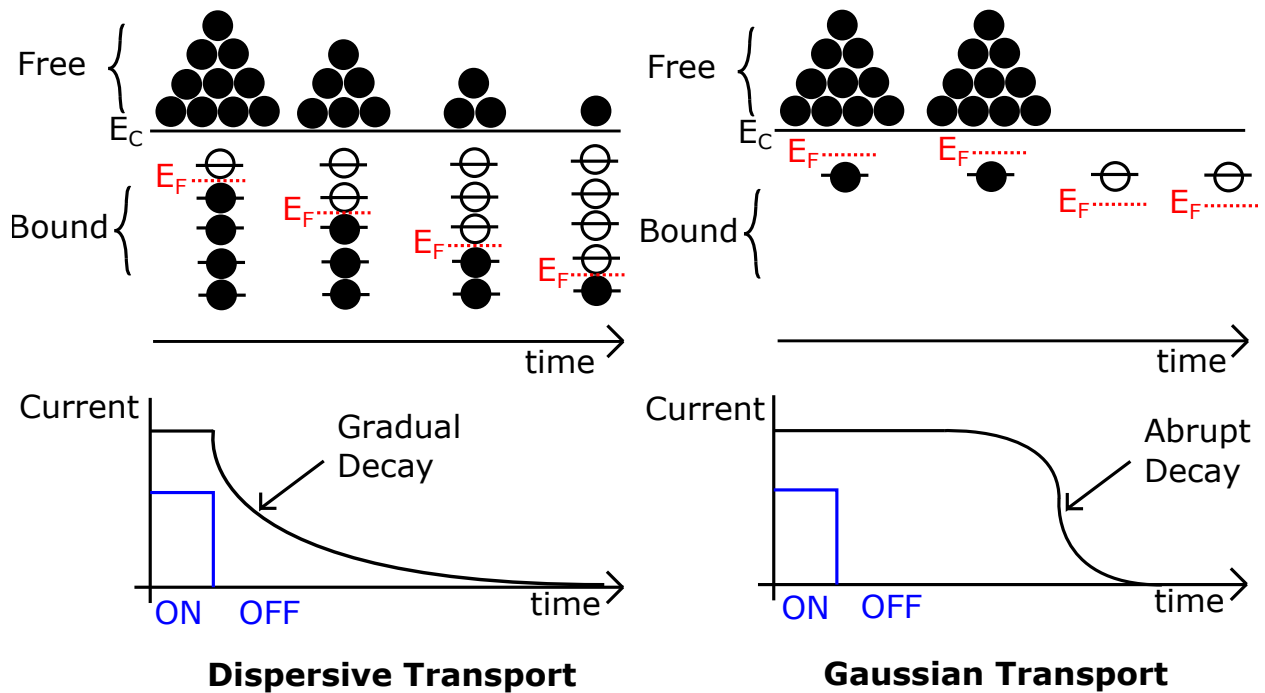


Figure 1.8: Illustration of the difference between gaussian and dispersive transport in ordered and disordered semiconductors respectively.

It is worth noting that clear distinction between hopping and MTR, although convenient, is not straightforward. Naturally, similarities exist between hopping and MTR due to the fact that both exhibit thermally-activated behavior and a strong sensitivity to charge density. Kinetic Monte Carlo simulations have shown strong similarity between the two models. For example, Mehraeen et al argue that the *transport energy* in hopping conduction is effectively replaced by the *mobility edge* in MTR models, both of which have an activation energy that rapidly reduces upon increase in charge density leading to similar trends [60]. However, the

mobility in purely hopping-based systems tends to be low and can be further distinguished based on the magnitude of the mobility.

## 1.4 Printed Electronics for Large-Area Applications

### Introduction to Solution-Processing

Solution-processing, is an alternative, cost-effective manufacturing technique for large-area electronics applications (e.g. displays, smart glass, solar cells, etc...) due to higher module throughput, materials utilization, lower equipment costs, and reduced overall process complexity [72]. Simple routes exist for the formation of electronic thin-films from precursor solutions which can be broadly classified as either sol-gel *solutions* or nanoparticle *suspensions* [72]. These liquids are transferred to substrates using a variety of coating (e.g. spin-coating, dip-coating, blade-coating, slot-casting), printing (e.g. screen, ink-jet, gravure, aerosol) and growth (e.g. spray pyrolysis, chemical bath deposition) techniques available (Figure 1.9, page 14). The chemical decomposition pathways and rheology of solution ultimately determine the precursors available for film formation [72]. Consequently, the electronic properties of solution-processed films tend to be strongly dependent on synthetic conditions. Ultimately, the electronic properties of solution-processed films are poorer in comparison to PVD synthesized films. Thus, there is an apparent trade-off between process complexity and device performance.

### Cost Benefit of Solution-Processing

The primary motivation for printed electronics is a reduction in manufacturing cost due to an increase in throughput (as measured in area per unit time) [85]. As such, increases in process speed and/or processing area are expected to directly result in a reduction in manufacturing cost. Data illustrating specific cost benefits are relatively scarce. Consequently, the cost benefits of solution-processing are usually taken for granted within the academic literature. It is generally assumed that total cost is reduced on a per area basis with an estimated 100 times reduction in cost ($100/ft^2$ as opposed to $10,000/ft^2$) relative to conventional manufacturing methods [61]. More detailed estimates are application specific. A highly detailed example is given by Krebs et al, in which the materials, labor, and processing costs have been itemized for each material in a screen-printed flexible polymer solar cell [44].

## 1.5 Transparent Conductive Oxides

### Role and Applications

Transparent conductive oxides (TCOs) play a vital role in several important electronic device applications including energy harvesting, information display and communication due
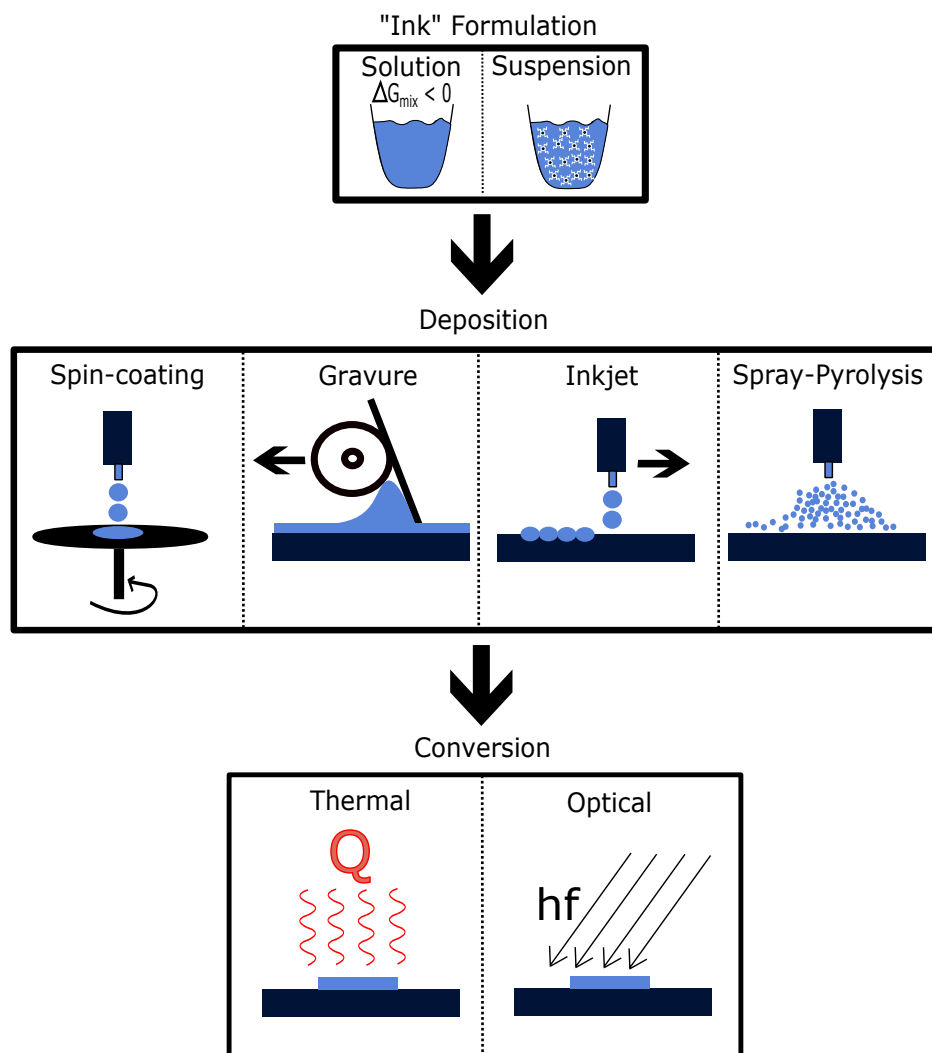
Figure 1.9: Illustration of the solution deposition process.

to their combination of high electronic conductivity and transparency in the visible range along with absorption in the infra-red range (Figure 1.10, page 15). A thorough review of transparent conductive oxides is given by [72]. Most obvious examples of their practical use are in photovoltaic devices, such as solar cells and light emitting diodes (LEDs), which require at least one transparent electrode to allow light to penetrate in or out of the device for proper operation. Additionally, both liquid crystal and LED displays incorporate TCOs into each pixel element which are coupled to thin-film transistors (TFTs) in order to modulate the transmission of light.

The most conductive TCOs may even be able to replace metal grids serving as bus bars for applications where grid transparency affects overall efficiency. For example, silicon solar cells use a grid of opaque silver lines as contacts which reflect light and may reduce overall

efficiency. In terms of simultaneously optimizing transparency and conductivity, ITO is the best option, although there have been growing concerns over the increasing cost of indium. For example, in a detailed cost analysis of screen-printed polymer solar cells, the sputter-deposited ITO coated PET substrates (80 nm ITO, 175 µm PET) accounted for roughly 34% of the total materials cost per module [44]. PET material costs are relatively cheap, therefore, in this case, the majority of the materials cost is due to indium. In contrast, processing costs of the PET-ITO substrates accounted for 19% of the total processing cost per module. Therefore, although materials-related costs may not always be reduced (depending on the choice of precursor), there is certainly room, however, for solution-processing methods to lower the overall manufacturing costs specifically by reducing processing-related costs.

## Deposition Methods

Traditional methods of fabricating TCOs involve expensive physical-vapor deposition (PVD) processes such as sputtering, thermal evaporation, and pulsed laser deposition which are not particularly amenable to large-area, high-throughput processing [85]. Fortunately, TCOs are readily amenable towards solution-processing and can therefore be deposited using any of the afforementioned low-cost methods.
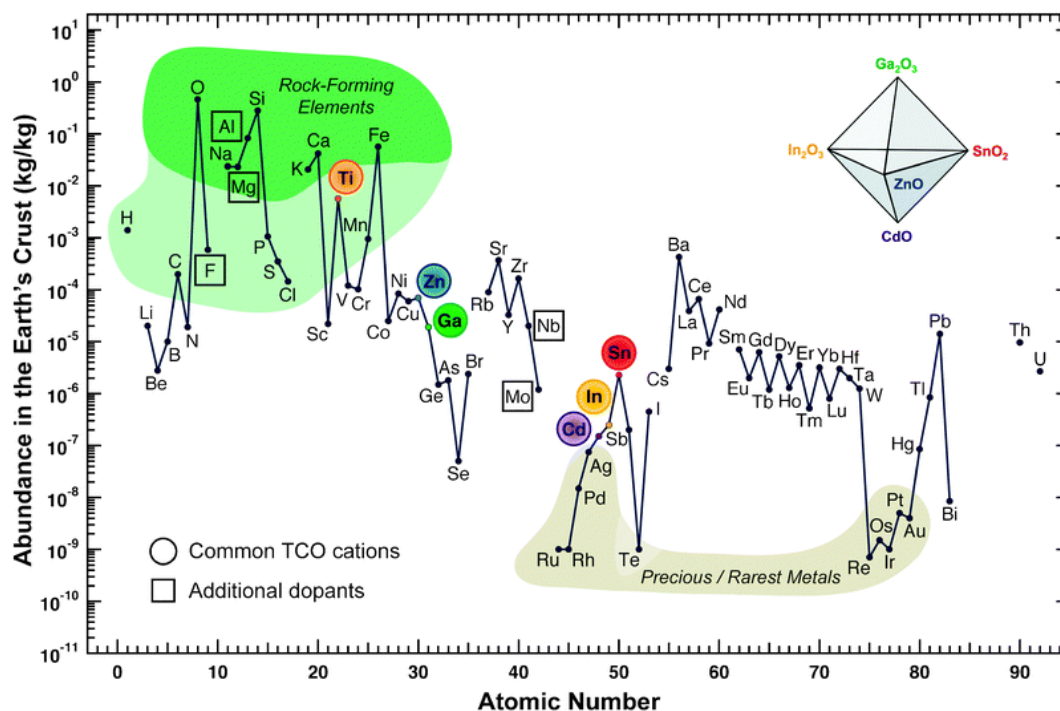


Figure 1.10: Relative abundance of various elements in the Earth's crust according to [72].

## 1.6   Method of Investigation

Field-effect mobility in solution-processed TCOs for semiconductor applications has not yet reached the reliable levels routinely obtained in PVD films (e.g. sputtering, PLD). The most familiar success story regarding solution-processed TCOs that have been able to achieve commercial adoption is $SnO_2$:F, which is deposited commercially for conductor applications via spray-pyrolysis [62]. For semiconductor applications, typical mobility values for solution-processed TCOs fall within the range of 1 to $30\,cm^2\,V^{-1}\,s^{-1}$ whereas PVD films can easily exceed $100\,cm^2\,V^{-1}\,s^{-1}$. The exact cause of lower mobility is unclear but is likely related to the multiple non-equilibrium processes occurring in parallel during annealing of wet films - densification/mass-loss, crystallization, and chemical conversion [9]. These processes typically result in higher defect concentrations and increased porosity relative to films deposited via well-established PVD methods. As a consequence, identifying ways of increasing mobility in these systems either through improved materials synthesis or through exploitation of beneficial material interactions remains an ongoing research effort in the field moving towards the goal of replacing existing PVD process steps with less expensive solution-processes.

An example of a fortuitous material interaction is the astonishing fact that TCO materials exhibit higher field-effect mobility when used in conjunction with high-k gate dielectrics (10 to $100\,cm^2\,V^{-1}\,s^{-1}$) as opposed to conventional thermally-grown $SiO_2$ (0.1 to $20\,cm^2\,V^{-1}\,s^{-1}$). A common observation is that, for TFTs incorporating high-k gate dielectrics, the maximum field-effect mobility values tend to occur at lower transverse electric fields than the general trend observed in literature using ideal thermally grown $SiO_2$ dielectrics (Figure 1.11, page 17). Despite the large amount of empirical data documenting this effect, its physical origin is poorly understood, and, as such, is the primary focus of this work. The aforementioned technological significance of these materials as well as the attractive cost-reduction in solution-processing justifies the need for improving understanding of this oddly beneficial effect as it represents a method for bridging the gap between the mobility of vapor-deposited and solution-processed TCO films.

Recently, the performance of solution-processed ZnO thin-film transistors (TFTs) deposited via spray pyrolysis at $400\,°C$ has become somewhat comparable to sputtering with a competitive mobility of $85\,cm^2\,V^{-1}\,s^{-1}$ obtained on a sol-gel $ZrO_2$ gate dielectric [1]. Based on these results, the $ZnO/ZrO_2$ system was selected as a representative system for further detailed comparison. Furthermore, spray pyrolysis is a mature method for depositing TCOs with reduced process complexity relative to other printing methods allowing the focus to be on device behavior rather than on process complexity.

This study progresses via electrical analysis of thin-film transistor data obtained from TCOs deposited using spray pyrolysis onto various dielectrics. To supplement electrical data, where appropriate, physical characterization (e.g. XPS, XRD, UPS, SEM, AFM) is performed in order to draw additional insight into underlying mechanisms. Additionally, electrostatic simulations were performed to corroborate claims based on experimental data.

Based on the tendency of solution-processed materials to exhibit high defect concentrations, this work is framed around the interactions between defects in the semiconductor
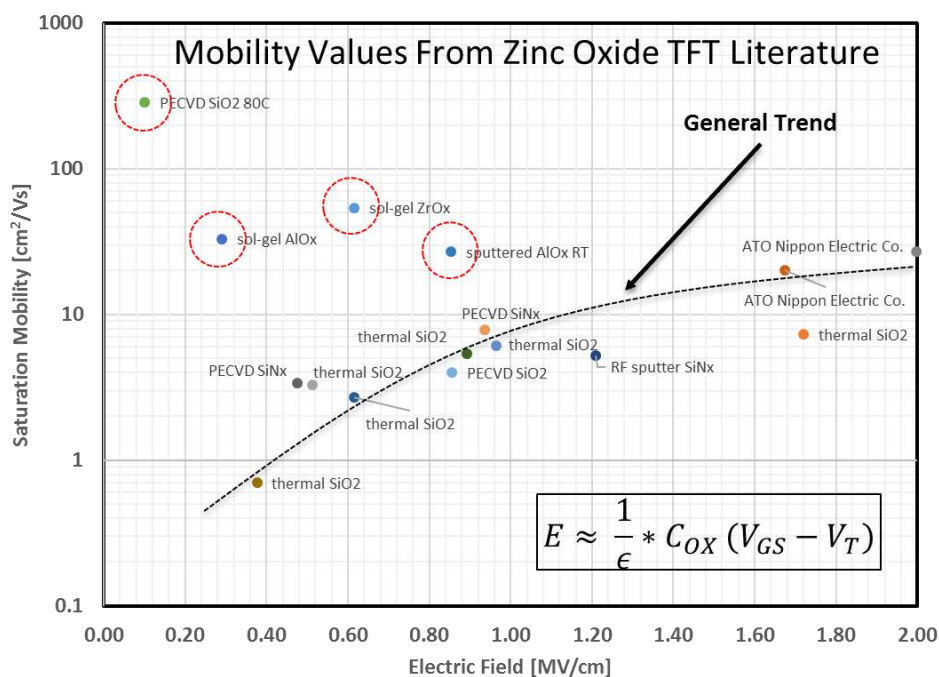
Figure 1.11: Saturation mobility values obtained from ZnO TFT literature plotted as a function of transverse electric field.

and dielectric leading to observable differences in transport behavior. This is reasonable, based on the observation that, in practice, the frequency range of operation in a TFT is typically much lower than in highly scaled CMOS. Consequently, the primary dielectric loss mechanisms relevant for TFT applications include interfacial and space charge polarization. Therefore, slow charging and discharging of dielectric defects are expected to play a larger role in switching characteristics, particularly in solution-processed TFTs due to higher defect concentrations.

## 1.7 Composition

We begin in **chapter 2**, by defining the theoretical framework used for deriving field-effect mobility and density of states from transistor measurements to be used frequently throughout this work. Conventional mobility extraction methods based on inaccurate square-law assumptions originally intended for well-ordered semiconductors (e.g. c-Si) were replaced by a more appropriate framework designed for transistors having disordered channels. Specifically, by separately measuring steady-state induced charge and drain conductance, field-effect mobility is extracted in a more self-consistent way that accounts for the strong gate-voltage

dependence observed in TFTs exhibiting dispersive transport. The utility of this method is extended further in subsequent chapters whereby variable-temperature mobility measurements provide the relevant data needed to extract the density of localized states and draw connections between transport and defect-dominated electrostatics.

The synthetic method used to fabricate TCOs affects electrostatic behavior through formation of intrinsic defects during synthesis. In **chapter 3**, we establish basic relationships between mobility and defect-dominated electrostatics determined by spray-pyrolysis synthetic conditions. Variable-temperature mobility measurements are used to extract density of localized states as a function of synthetic conditions regarding the deposition of ZnO films onto ideal thermally-grown $SiO_2$ dielectrics. The affect of substrate temperature, precursor concentration and volumetric flow rate are identified as statistically-significant factors and their effect on mobility is summarized. The basic relationships formed provide insight into the specific transport mechanism as well as demonstrate how modification of the density of localized states affects mobility in the TCO. In the following chapter, the latter observation is found to be particularly important in this work based on the fact that the density of localized states can be modified either directly, through synthesis, or indirectly, through interactions with other materials like, as will be shown, high-k dielectrics.

The interaction between high-k gate-dielectrics and TCO semiconductors leading to high field-effect mobility is the primary subject matter of this work. In **chapter 4**, we explore this interaction in detail using the established framework for analysis of mobility and density of localized states developed in previous chapters. Initially, we form a baseline comparison to ZnO TFTs having thermally-grown $SiO_2$ gate-dielectrics by using a relatively high-quality and nearly ideal solution-processed $ZrO_2$ gate-dielectric. We then intentionally reduced the quality of the $ZrO_2$ gate-dielectric, introducing more defects by lowering the processing temperature and subsequently evaluated the resulting transport behavior in the ZnO. Surprisingly, mobility was found to increase strongly with reduction in processing temperature which we then correlated to an effective increase in the presence of donor-like defect states in the $ZrO_2$, assumed to be enhanced by the reduction in $ZrO_2$ processing temperature. A theory to explain these and other general observations in literature is deduced based on electron donation from donor-like defects in high-k dielectrics supported by electrical data.

In **chapter 5**, the experimental observations leading to the theory of electron donation from donor-like traps in the gate dielectric are supported with electrostatic simulations whereby donor states are intentionally introduced into the $ZrO_2$ and the effect on electrostatics and field-effect mobility are studied. Simulations show that the presence of donor states in the dielectric lead to mobility enhancement and an increase in electrostatic capacitance alongside a gradual shift in the onset of conduction towards increasingly negative voltages than expected based on the flat-band voltage. These simulations are found to be fully consistent with experimental observations, providing additional confidence in the electron-donation mechanism.

Unfortunately, the negative drawbacks associated with defects in the gate-dielectric of a transistor limit the practical utility of using high-k dielectrics as an additional source of electrons in the TCO. Therefore, in **chapter 6**, an improved method for exploiting this effect

is demonstrated that mitigates some of the negative aspects while retaining the benefits. Specifically, it is shown that encapsulation of ZnO TFTs with $Ga_2O_3$ eliminates frequency dispersion, reduces hysteresis and improves device stability, while enhancing the field-effect mobility relative to unencapsulated ZnO TFTs with $SiO_2$ dielectrics.

Finally, in **chapter 7**, the primary contributions of the present work are summarized and areas of future work and further investigation are suggested.

# Chapter 2

# Quantifying Mobility of Disordered-Channel Thin-Film Transistors

In this chapter, we lay the foundation for the primary methods of experimental analysis used throughout this work. We begin by refining existing techniques to provide a self-consistent, physically-based method particularly well suited for quantifying the mobility of solution-processed transition metal-oxide based thin-film transistors (TFTs). The methodology is presented as a more appropriate alternative to existing square-law techniques whose assumptions are inapplicable to systems exhibiting dispersive transport. To demonstrate its broad utility in solution-processed TFTs, this method was applied to solution-processed $SnO_2$ and ZnO TFTs having various gate dielectrics, but is not limited in its scope to these materials due to its broad applicability in disordered semiconductors. In addition, to account for the different operating voltages set by the differences in effective oxide thickness of the dielectric, mobility was evaluated as a function of the transverse electric field, allowing for the direct comparison of mobility independent of the choice of gate dielectric used later in this work. The utility of the methods developed within this chapter form the foundation of the experimental methods used for the more pressing concerns related to high-k dielectrics, addressed in subsequent chapters.

## 2.1   Background

Existing methods used for quantifying the mobility of amorphous and small-grained poly-crystalline TCO TFTs routinely employ the familiar square-law equation framework [78] originally intended for well-ordered semiconductors, such as crystalline silicon. Unlike crystalline silicon, electronic transport in disordered semiconductors is not limited to transport through the conduction band states, but also can additionally include transport through extended states distributed below the conduction band [64]. The presence of such states

(Figure 2.1, page 21) causes the semiconducting channel to accumulate charge via the gradual filling of trap states, ultimately leading to what is known as dispersive transport.
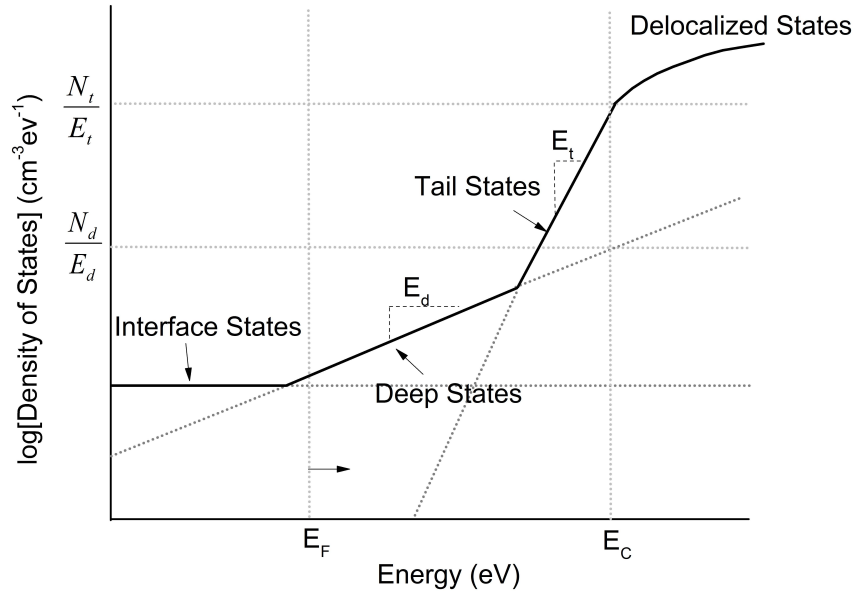


Figure 2.1: Typical density of states for a disordered semiconductor. Band tails and deep states are exponentially decreasing functions of energy, moving away from the conduction band toward midgap.

As a consequence, band-like transport is generally not observed at room temperature and field-effect mobility is found to increase gradually with temperature and gate-voltage as more delocalized states are filled. These effects are generally more pronounced in solution-processed materials, which, typically being deposited at lower temperatures and under non-equilibrium conditions, have a tendency to exhibit greater electronic disorder due to incomplete conversion and poor crystallinity. Nonetheless, accurate static TFT models have been developed based on transport in these and similar disordered systems [50] although the experimental methods used in practice for mobility extraction unfortunately utilize inapplicable square-law assumptions:

1. Mobility is a constant parameter, invariant with respect to the transverse electric field.

2. No accumulation charge exists below threshold.

Hoffman addressed the first point by defining incremental and average mobility based upon the drain conductance ($G_D$) rather than the transconductance ($G_M$), however, at

the time he intentionally did not address the second point, stating that it required direct measurement of the available charge from a capacitance voltage measurement, which he argued was unreliable due to frequency dispersion in the semiconductor [29].

In this chapter, we expand upon the work of Hoffman by experimentally deriving the accumulation charge from quasi-static capacitance voltage (QSCV) measurements, performed under conditions of steady-state equilibrium where electronic dispersion is minimal, allowing accurate charge determination. Furthermore, the slow voltage sweep rates of QSCV make it particularly well suited for electrostatic models of transport whereby slower electronic traps couple to the free electron concentration in steady-state.

QSCV is a technique that measures the static equilibrium capacitance voltage curve by measuring the displacement current of a capacitor in response to a linear voltage ramp of known amplitude and ramp rate [45] (See appendix). Such measurements are highly desirable in comparison with higher frequency small-signal impedance measurements since, due to the near-equilibrium conditions, the otherwise confounding effects of electronic dispersion are negligible. We note that QSCV cannot be applied to systems exhibiting very low frequency dispersion in the gate dielectric, such as that typically exhibited in electrolyte gated transistors, which exhibit ionic and electronic conduction [86] in the sub hertz range because QSCV frequencies are higher than this. Defining mobility in such systems is difficult since electrostatic conditions cannot be reached reasonably quickly. However, under conditions of equilibrium, use of QSCV establishes an appropriate, first-order experimental methodology for quantifying mobility that is more accurate and consistent with theoretical considerations of transport in a dispersive metal oxide semiconductor [83].

Care must be taken to maintain equilibrium conditions, since due to the fact that the semiconductor is defective, containing localized, and extended states (Figure 2.1), the measured capacitance may be affected by these states. The electron concentration derived from capacitance will therefore contain a separate response due to trapped and free electrons and, as a consequence, the free electron concentration can potentially be underestimated when derived through a capacitance-voltage measurement under nonequilibrium conditions. Consequently, mobility derived from such measurements will be overestimated. Nevertheless, trap states at shallow energies corresponding to similar capture and emission rates do not contribute toward this error (Figure 2.2, page 23), since steady-state conditions apply in regards to the free electron concentration.

The energy level to which steady-state approximation breaks down is difficult to predict without precise knowledge of the density of states. Beyond this depth, where capture rates outweigh emission rates, electron concentrations can be underestimated via this method. Fortunately, since the density of states for many disordered systems can be modeled, as shown in Figure 2.1, the shallower states typically outnumber the deep states and this error may be minimal.

A final goal of this chapter, is to enable benchmarking of performance as a function of dielectric and owing to the dielectric and field dependence of mobility, the applied gate-bias is converted into an electric field term that encompasses the electrical properties of the gate dielectric (i.e., dielectric constant, charge, and so on.) and allows mobility to be
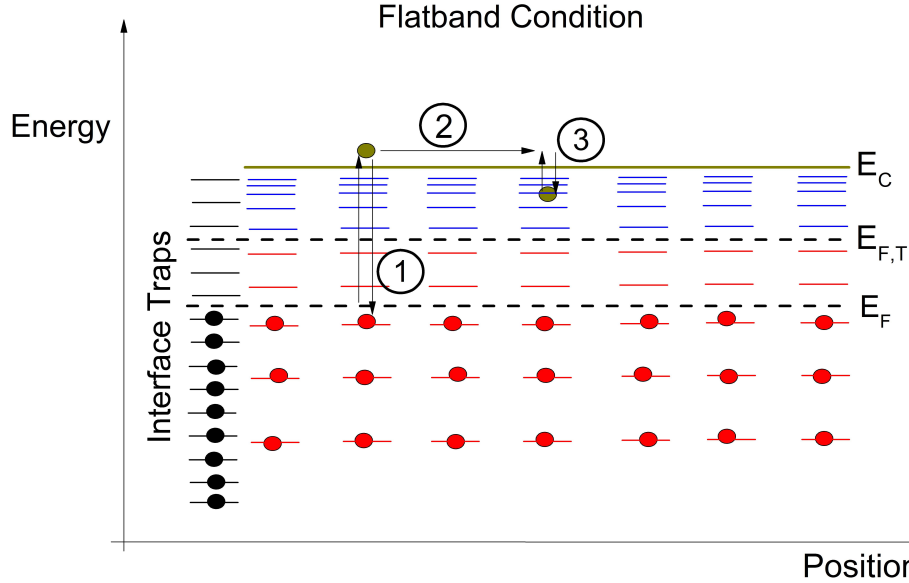
Figure 2.2: Figure showing capture and emission processes. (1) Indicates capture and emission of deep states. (2) Indicates transport above the mobility edge. (3) Indicates capture and emission from shallow states.

evaluated as a function of the effective field seen by accumulation layer electrons. This information is exceedingly more valuable than mobility at a single voltage, which is typically not an absolute maximum for dispersive systems. Not only does this address the empirical observation that mobility is voltage dependent, but it also provides a controlled method for comparing mobility independent of the operating voltage and choice of gate dielectric, thereby standardizing mobility numbers reported elsewhere in the literature.

We note that, while we validate the proposed methodology to solution-processed metal oxide semiconductors, where there is a greater need for more accurate techniques, the methodology is applicable to conventionally deposited materials as well, since none of the approximations made herein are specific to solution processed systems or limited to poor performing materials.

## 2.2 Description of Methodology

In modeling of TFTs, the threshold voltage, $V_T$, is often interchanged with the turn on voltage, $V_{ON}$ [31]. Since $V_{ON}$ is routinely applied despite having any physical origin in an accumulation-mode device, to avoid confusion we have used the flat-band voltage, $V_{FB}$, as it

physically represents the transition point between depletion and accumulation. Furthermore, we specifically focus on linear mobility for evaluating transport, since, in the absence of poor contacts leading to either an injection barrier or contact resistance, saturation mobility has limited physical meaning. This is of course due to the fact that drift mobility is only well defined at low electric fields.

In its most simplest form, the drain current in the linear region is expressed as a drift equation according to Ohm's Law:

$$I_{D,LIN} = \frac{W}{L}\mu_{LIN}(V_{GS})Q_{ACC}(V_{GS})V_{DS,LIN} \tag{2.1}$$

where W and L are the respective device width and length, $Q_{ACC}$ is the gate-bias dependent accumulation charge, $\mu_{LIN}$ is the gate voltage dependent linear mobility, and $V_{DS}$,lin is the drain source voltage in the linear regime. Note that this assumes that the mobility is spatially uniform in the channel thickness direction. Differentiating the drain current with respect to $V_{GS}$ and $V_{DS}$ yields the following expressions for the linear gate transconductance and drain conductance ($G_{M,LIN}$ and $G_{D,LIN}$), respectively:

$$G_{M,LIN} = \frac{\partial I_{D,LIN}}{\partial V_{GS}} = \frac{W}{L}V_{DS,LIN}\Big(Q_{ACC}\frac{\partial \mu_{LIN}}{\partial V_{GS}} + \mu_{LIN}\frac{\partial Q_{ACC}}{\partial V_{GS}}\Big) \tag{2.2}$$

$$G_{D,LIN} = \frac{\partial I_{D,LIN}}{\partial V_{DS}} = \frac{W}{L}Q_{ACC}(V_{GS})\mu_{lin}(V_{GS}) \tag{2.3}$$

Traditional mobility definitions involving $G_{M,LIN}$ assume the mobility to be constant with respect to $V_{GS}$ and further assume that the accumulation charge is linear with respect to $V_{GS}$, assumptions which are inapplicable to oxide based TFTs due to their dispersive transport. Nonetheless, applying these assumptions leads to the conventional definition of the field effect mobility one finds in square law models:

$$\mu_{LIN,SL} = \frac{G_{M,LIN}}{\frac{W}{L}V_{DS}C_{OX}} \tag{2.4}$$

Hoffman was the first to illustrate the error obtained when the bias dependence of the mobility is neglected by comparing incremental and average mobility, with average mobility being the more physically correct measure of the intrinsic mobility.

$$\mu_{AVE} = \frac{G_D}{\frac{W}{L}C_{OX}(V_{GS} - VFB)} \tag{2.5}$$

$$\mu_{INC} = \frac{\frac{\partial G_D}{\partial V_{GS}}}{\frac{W}{L}C_{OX}} \tag{2.6}$$

Therefore, to make self consistent assumptions regarding the dispersive nature of the materials, $G_{D,LIN}$ as opposed to $G_{M,LIN}$ was used in our evaluation of mobility as it does not presume knowledge regarding the mobility or induced charge.

$G_{D,LIN}$ can be obtained by computing the slope of the drain current ($I_D$) versus drain source voltage ($V_{DS}$) curves in the linear region, as $V_{GS}$ was finely stepped from full depletion to strong accumulation. This yields $G_{D,LIN}$ as a function of $V_{GS}$.

The accumulation charge in the channel can be obtained by integrating the quasi static channel capacitance according to the following equation, where $C_{G,S/D}$ is the measured capacitance, $C_{DEP,MIN}$ is the minimum depletion capacitance and, $A_{ACTIVE}$ is the device active area, assumed to be fully accumulated:

$$Q_{ACC}(V_{GS}) = \frac{1}{A_{ACTIVE}} \int_{V_{GS,MIN}}^{V_{GS}} \left( C_{G,S/D} - C_{DEP,MIN} \right) dV_{GS} \tag{2.7}$$

Knowing $G_D$ and $Q_{ACC}$, $\mu_{LIN}$ can now be expressed as a function of gate source voltage. Combining (3) and (4), we arrive at the definition of mobility given in:

$$\mu_{LIN}(V_{GS}) = \frac{G_{D,LIN}(V_{GS})}{\frac{W}{L} Q_{ACC}(V_{GS})} \tag{2.8}$$

This is the primary result of this chapter and is the equation used in foregoing mobility analysis. The utility of this definition of mobility is that it allows the drift mobility to vary arbitrarily with gate voltage and is based on the independent determination of accumulation charge from the channel capacitance, unlike $G_M$ based methods, in which charge and mobility vary simultaneously. When contact resistance is negligible in comparison with the channel resistance, as it was for our long channel devices, this provides an accurate measure of the intrinsic mobility in oxide TFTs. In nonideal cases where contact resistance is no longer negligible, either due to a very high-mobility oxide or very short channel lengths, (4) must be modified to include the effect of contact resistance [5].

As mentioned previously, an additional goal of this work is to enable benchmarking of mobility independent of dielectric choice. Given the strong field dependence of mobility this then necessitates the extraction of the field seen by accumulation layer electrons. Gauss' law provides a relationship between the electric field and charge within the semiconductor according to the following equation, where $k_F$ is the relative dielectric constant of the semiconductor:

$$E_{EFF} = \frac{Q_{ACC}}{k_F \epsilon_0} \tag{2.9}$$

In general, establishing a charge-voltage relationship requires numerical iteration to obtain a solution [70]. By invoking the charge sheet assumptions [8], which assumes that

the surface potential in accumulation is small relative to the other voltage drops and can be neglected essentially placing a delta charge at the dielectric interface, the charge voltage relationships in the MOS capacitor become linear, and the charge voltage relationship known. This assumption is reasonable in accumulation since, unlike amorphous silicon, the carrier concentration in oxide TFTs is much higher and the Debye length smaller. This allows one to express the transverse field as a closed form analytical expression according to the following equation, where $V_{FB}$ is the flat band voltage obtained from the capacitance voltage characteristic:

$$E_{EFF} = \frac{Q_{ACC}}{k_F \epsilon_0} = \frac{C_{OX}\left(V_{GS} - V_{FB}\right)}{k_F \epsilon_0} \tag{2.10}$$

Equation (2.9) is utilized in square law models used to derive the field effect mobility. However, as mentioned, the accuracy of this expression is limited to the accumulation regime, since this is the only regime in which the surface potential is indeed expected to be small enough to ignore and/or the Debye length negligibly small, thus placing a fundamental limit on the utility of the charge sheet model.

Due to the physics describing transport in disordered systems, it is highly desirable to be able to measure, with accuracy, the mobility from depletion to accumulation. For example, within a multiple trap and release framework, mobility throughout the entire operating regime (i.e., depletion to accumulation) is typically used in conjunction with activation energies (derived from thermally stimulated currents) to obtain information regarding the density of states in semiconductors having localized and extended states. Small grained polycrystalline and amorphous oxides fall within this class of materials, and therefore benefit from increased accuracy of mobility over all regimes of operation.

As a consequence, to gain accuracy throughout the entire region of operation (i.e., from depletion to accumulation), the accumulation charge was empirically derived from capacitance according to (2.6), and substituted into (2.8) to evaluate the electric field.

To extract the dielectric constant of the semiconductor film for use in (2.8), the device capacitances were modeled as follows (Figure 2.3). First, it is noted that the source and drain are shorted throughout the QSCV measurement, ensuring a uniform lateral charge distribution in the semiconductor. Based upon the geometry of the inverted-staggered TFT structure, and assuming the semiconductor to be fully accumulated in the on state, the oxide capacitance is given according to the following equation, where $L_S$, $L_{CH}$, and $L_D$ are the physical lengths of the source electrode, semiconductor channel region, and drain electrode, respectively, along the lateral dimension:

$$C_{OX} = \frac{K_{OX}\epsilon_0}{t_{OX}} = \frac{C_{ACC,MAX}}{W\left(L_S + L_{CH} + L_D\right)} \tag{2.11}$$

When the semiconductor film is fully depleted, it behaves like an insulator and its capacitance can be expressed according to the following equation, where $k_F$ is the dielectric
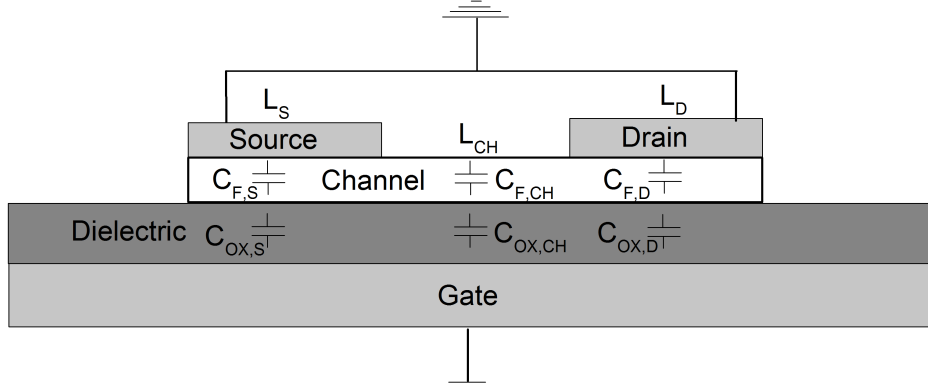
Figure 2.3: Inverted, staggered TFT structure with capacitances inserted for modeling pur-
poses. Film capacitances $C_F$ and oxide capacitances ($C_{OX}$) correspoinding to regions deter-
mined by the source, channel, and drain geometries are indicated

constant of the semiconductor and $t_F$ is the semiconductor thickness:

$$C_F = \frac{K_F \epsilon_0}{t_F} \tag{2.12}$$

Furthermore, in strong depletion, the semiconductor is fully depleted and the capacitance
reaches a minimum, dominated by the overlap capacitance of the source/drain and gate. The
measured capacitance can then be expressed according to:

$$C_{DEP,MIN} = \frac{C_{OX} C_F}{C_{OX} + C_F} W \left( L_S + L_D \right) \tag{2.13}$$

From (8) and (9), it is possible to obtain the dielectric constant of the semiconductor
film according to:

$$k_F = \frac{t_F}{\epsilon_0} \left( \frac{W \left( L_S + L_D \right)}{C_{DEP,MIN}} - \frac{W \left( L_S + L_{CH} + L_D \right)}{C_{ACC,MAX}} \right)^{-1} \tag{2.14}$$

As the proposed methodology is based upon the accuracy and reliability of the QSCV
data, we investigated the dependence of the capacitance derived from QSCV on the ramp
rate by varying the integration time from 16 ms to 128 ms. These times were chosen since
they correspond to integer multiples of the line frequency (60 Hz) and cover the range of times
for the data evaluated in this paper (100 ms). Figure 2.4 indicates that the capacitance is
insensitive to changes in integration time, and therefore ramp rate. Therefore, we conclude
that the capacitance derived via QSCV is nondispersive within this frequency range, unlike

what can be observed through higher frequency impedance measurements. As a result, the charge obtained through integration of this capacitance will be an accurate measure of the electrostatic charge free of otherwise confounding dispersive effects.
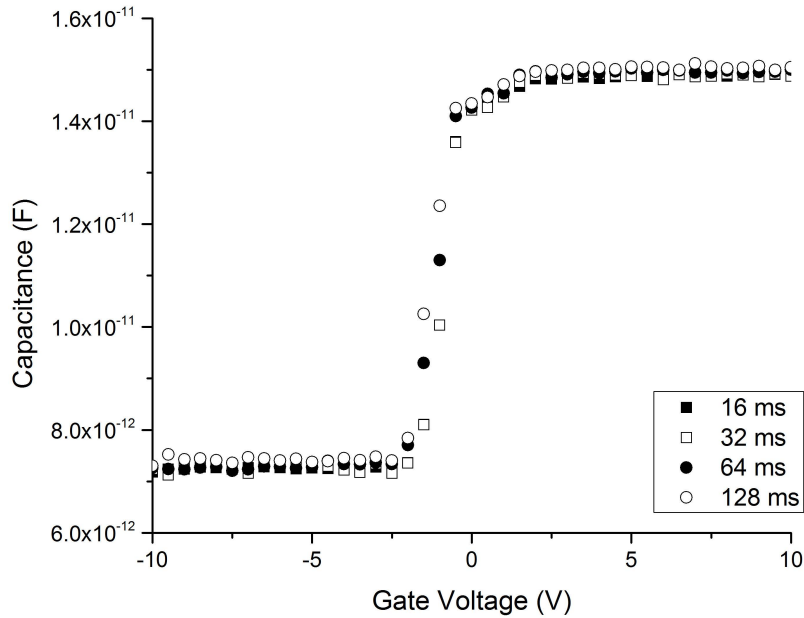


Figure 2.4: Quasistatic capacitance as a function of gate voltage for a ZnO TFT with $100\,\mathrm{nm}$ SiO$_2$ evaluated at different integration times of the charging current (16, 32, 64 and $128\,\mathrm{ms}$). Amplitude applied during integration of charging current was set to $50\,\mathrm{mV}$, leakage integration time used was held constant at $16\,\mathrm{ms}$, corresponding to one period of the line frequency ($60\,\mathrm{Hz}$).

To directly compare our proposed methodology to Hoffman's technique, our method was additionally applied to TFTs consisting of a high quality ZnO channel deposited via spray pyrolysis at $400\,°\mathrm{C}$ onto $100\,\mathrm{nm}$ thermally grown SiO$_2$ according to a procedure outlined by Adamopoulos et al [1]. The results are shown in Figure 2.5. Figure 2.5 shows that the difference between the two methods is such that mobility is slightly overestimated when using the charge sheet approximation to the total induced charge according to Hoffman's technique (black curves). This occurs due to the gradual switching behavior, in which the subthreshold swing cannot be approximated as being zero. The error is minimal for this particular device, since it is of fairly high quality, having a low subthreshold swing (0.6 V/decade) and a high mobility. We therefore conclude that, although Hoffman's technique suffices provided the subthreshold swing is sufficiently low, in general, however, equation (2.7) must be used according to the proposed technique.
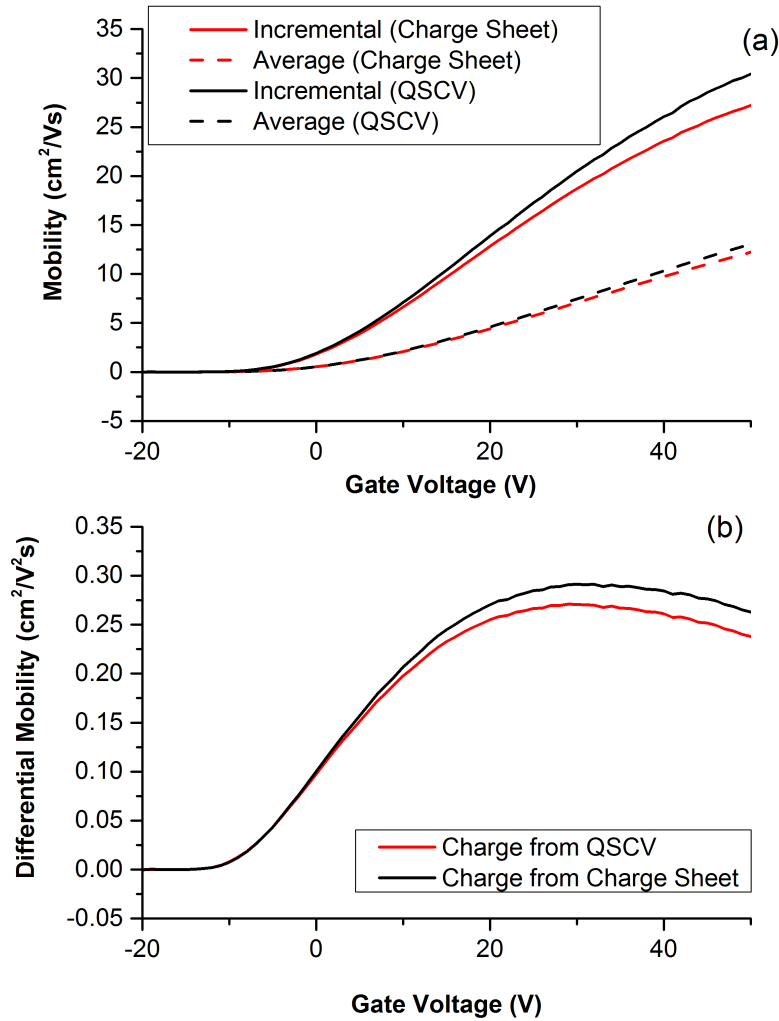
Figure 2.5: Comparison of Hoffman's technique and our proposed method for high-quality ZnO TFT deposited via spray-pyrolysis at $400\,°C$ onto $100\,nm$ $SiO_2$. (a) Incremental and average mobility computed using a charge obtained via the charge sheet approximation and measured quasi static capacitance. (b) Differential mobility comparison for the charge obtained via the charge sheet approximation and measured quasi-static capacitance

## 2.3 Results and Discussion

Having established confidence in the technique by establishing invariance to ramp rate and agreement to Hoffman in the high-quality limit, we have applied the method to low performance metal-oxide TFTs, where due to their higher subthreshold swing, the proposed method has greater utility. The proposed experimental mobility extraction methodology is not region-specific and is able to be applied to devices throughout the entire operating range

from depletion to accumulation because the accumulation charge and drain conductance are both measured from depletion to accumulation. To illustrate the importance of this result, we compare the numerically obtained Pao-Sah [70] solution for a hypothetical $SnO_2$ system consisting solely of mobile electrons and fully ionized donor concentrations of varying magnitudes in Figure 2.6. As expected, it was found that the analytical charge-sheet expression and the Pao-Sah model agree well in accumulation but not in depletion, becoming increasingly inaccurate as the donor concentration decreases.
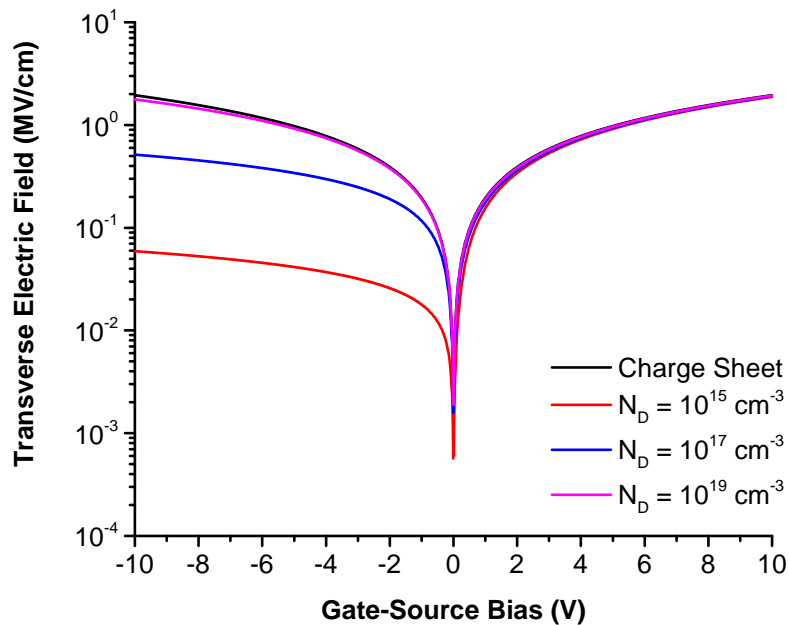


Figure 2.6: Comparison of the numerically computed (Pao-Sah) and analytical (charge sheet) solution of transverse electric field for a hypothetical $SnO_2$ TFT having 20 nm of thermally-grown $SiO_2$ and a flat-band voltage of 0 V with varying donor concentrations.

Moreover, we tested this fact experimentally by comparing the field-dependent mobility for two $SnO_2$ TFTs that were identically processed but differed in terms of $SiO_2$ dielectric thickness. According to the Pao-Sah results in Figure 2.6, (7) should be inaccurate in depletion and the exact dependence upon the dielectric thickness does not follow the simple relationship defined by (7). Experimentally, Figure 2.7 shows that the linear mobility versus field is dielectric thickness invariant (as expected) in accumulation but, because the analytical expression of transverse field is inaccurate near depletion, the linear mobility of the two devices diverges at low fields. This result demonstrates the importance of measuring the accumulation charge by integration of the capacitance-voltage characteristic according to (4).
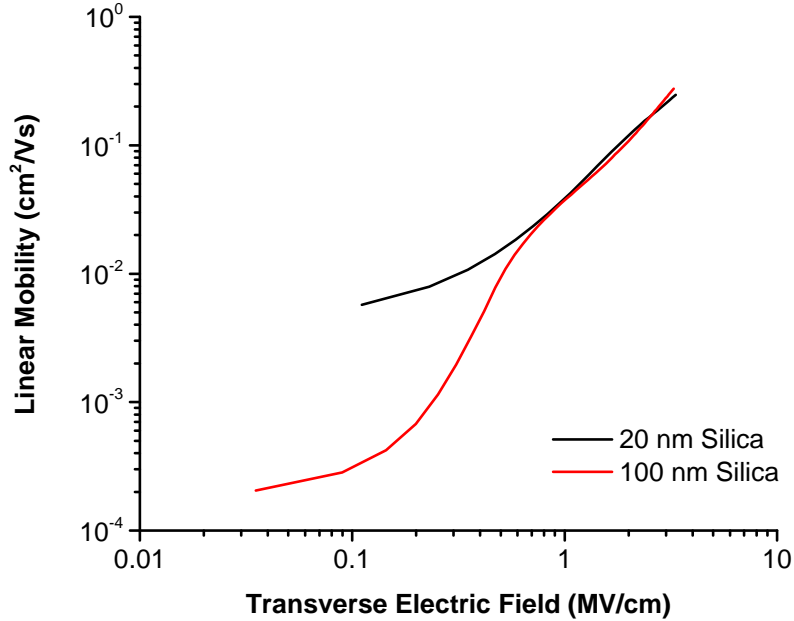
Figure 2.7: Linear mobility versus the transverse electric field for identically processed moderately annealed ($400\,°C$) $SnO_2$ TFTs having different oxide thicknesses.

These results are consistent with the expectation that the charge-sheet solution for the electric field is limited to the accumulation region. For the sake of making accurate comparisons throughout the entire bias range, the empirically derived charge (4) was used henceforth in (6) to compute the transverse field, although the charge-sheet result (7) may have equivalent utility in the strong accumulation region.

Figure 2.8 demonstrates the complete application of the aforementioned method to a ZnO TFT having a thermally grown $SiO_2$ dielectric. $G_D$ was obtained using (3), $Q_{ACC}$ was obtained using (4), $\mu_{LIN}$ was obtained using (5), and $E_{EFF}$ was obtained using (6). All material specific parameters were empirically derived. The flat-band voltage ($V_{FB}$) was obtained from differentiating the capacitance-voltage curve and taking the point of maximum slope and was found to be $47\,V$. The dielectric constant of the semiconductor was obtained through (11) and was found to be 5.45. As expected, this device shows a strong gate-bias dependent mobility due to the gradual filling of defect states throughout the bias range in question.

Figures 2.9 and 2.10 show the model applied to both the $SnO_2$ and ZnO TFTs having different gate dielectrics, respectively. As expected, these devices show a clear dielectric and transverse field dependence. These results can be used to elucidate the commonalities and differences of electronic transport across different dielectrics/interfaces which happens to be

a common interest in the development of metal-oxide and organic TFTs, and is the subject matter of subsequent chapters.

## 2.4 Conclusion

To summarize, we have presented a more accurate, self-consistent, physically based alternative method for quantifying the field effect mobility of metal-oxide-based TFTs, consistent with disordered transport models and the original framework introduced by Hoffman. We have demonstrated the utility of this technique by comparing solution-processed $SnO_2$ and ZnO TFTs fabricated with different gate dielectrics through the use of a normative electric field metric. These results demonstrate the utility of this method in studying electronic transport in disordered metal-oxide TFTs and provide a potentially useful pathway for gaining additional insight into the role that dielectrics have in affecting transport in metal-oxide TFTs. In the following chapters, this methodology will be used to extract the effective density of states in the semiconductor as well as characterize mobility differences related to processing conditions of the semiconductor and dielectric.

## 2.5 Experimental Methods

To compare the effects of different dielectrics, various dielectrics were deposited onto heavily doped (100) n-type silicon substrates (phosphorous doped, $10^{19}$ cm$^{-3}$ , $0.005\,\Omega$ cm) by thermal oxidation or atomic layer deposition (ALD). These included:

1. 100 nm of thermally grown $SiO_2$

2. 55 nm of ALD $ZrO_2$

3. 55 nm of ALD $HfO_2$

4. 45 nm of ALD $Al_2O_3$

All ALD films were deposited at a 250 °C substrate temperature without the use of a plasma source. Two different solution-processed semiconductors were used: zinc oxide (ZnO) and tin oxide ($SnO_2$), both of which were deposited using sol gel routes. The zinc precursor solution was obtained by adding 114 µL of $14.5\,\mathrm{mol\,L^{-1}}$ ammonia to a $0.2\,\mathrm{mol\,L^{-1}}$ solution of zinc acetate dihydrate in methanol. The resulting solution was diluted to $0.05\,\mathrm{mol\,L^{-1}}$ with methanol. The tin precursor solution consisted of $0.1\,\mathrm{mol\,L^{-1}}$ tin (IV) chloride dihydrate dissolved in ethanol. Following dielectric deposition, either the zinc or tin precursor solutions were then spin coated at 3000 rpm for 30 s onto the various dielectric substrates. The tin samples were then subsequently annealed in air at 400 °C for 1 h, whereas the zinc samples were immediately annealed on a hotplate in air at 150 °C for 1 min followed by annealing at 250 °C for 2 h. Film thicknesses were approximately 30 nm. Finally, 100 nm of aluminum was

deposited through a shadow mask via thermal evaporation at 1 microTorr to serve as ohmic source/drain contacts. Long channel devices having aspect ratios of $W/L = 400\,\mu\mathrm{m}/40\,\mu\mathrm{m}$ were used. Figure 2.11 shows an illustration of the completed device structure.

The inverted staggered TFTs were measured in air using an HP4155C semiconductor parameter analyzer. To ensure identical initial conditions, and allow time for full depletion to be reached, each device was biased and held in depletion for 10 s prior to each measurement and then subsequently swept from depletion toward accumulation. Current voltage (IV) characteristics were extracted in the linear region using a long integration time to maintain equilibrium; hysteresis was found to be minimal.

The HP4155C was also used for QSCV measurements in addition to IV measurements. The amplitude of the ramped QSCV voltage applied to all devices was 50 mV, integration time for capacitance determination was 0.1 s and the leakage integration time for compensation was 0.017 s. This corresponds to a voltage ramp rate of $0.5\,\mathrm{V\,s^{-1}}$. Depending on the operating voltage ranges, the voltage step size varied between 0.5 V and 2 V corresponding to an effective frequency range of 0.25 Hz to 1 Hz, which is comparable with the measurement times used to extract the equilibrium IV data obtained using long integration time in a typical DC IV measurement.

Finally, it is worth noting that a practical concern when performing QSCV measurements is leakage current, which when unaccounted for, may cause erroneous interpretation of the displacement current [75]. However, due to the high quality conventionally deposited insulators used in this work, leakage currents were negligible. Nonetheless, leakage compensation was used at a current compliance of 10 nA.
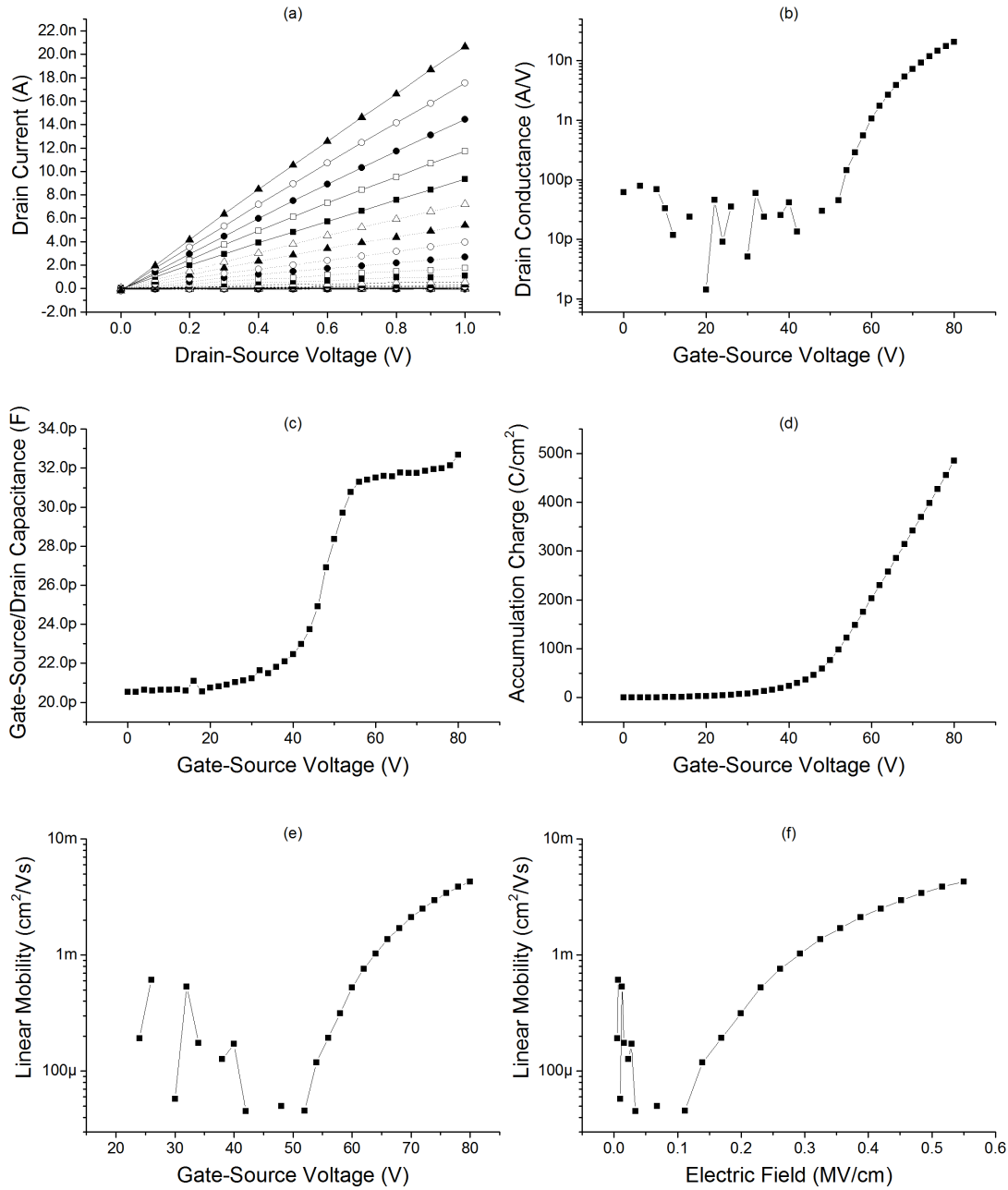
Figure 2.8: Complete mobility extraction process applied to a low-temperature annealed
(250 °C) ZnO TFT having 100 nm of thermally-grown SiO$_2$. $V_{GS}$ was stepped from 0 to
80 V in 2 V increments. (a) Drain current vs. drain voltage at different gate-source voltages.
(b) Drain conductance vs. gate-source voltage extracted from (a). (c) Gate-Source/Drain
capacitance obtained via quasi-static measurements. (d) Accumulation charge extracted
from (c). (e) Mobility vs. gate-source voltage obtained via (b) and (d). (f) Mobility vs.
transverse electric field obtained via (b) and (d) using equation (6).
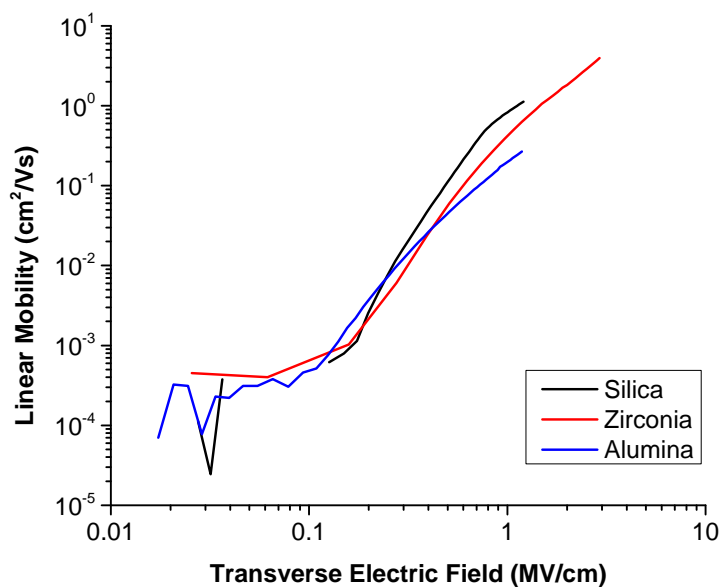
Figure 2.9: Linear mobility versus empirically derived transverese electric field for moderately annealed (400 °C) SnO$_2$ TFTs fabricated on various dielectrics.
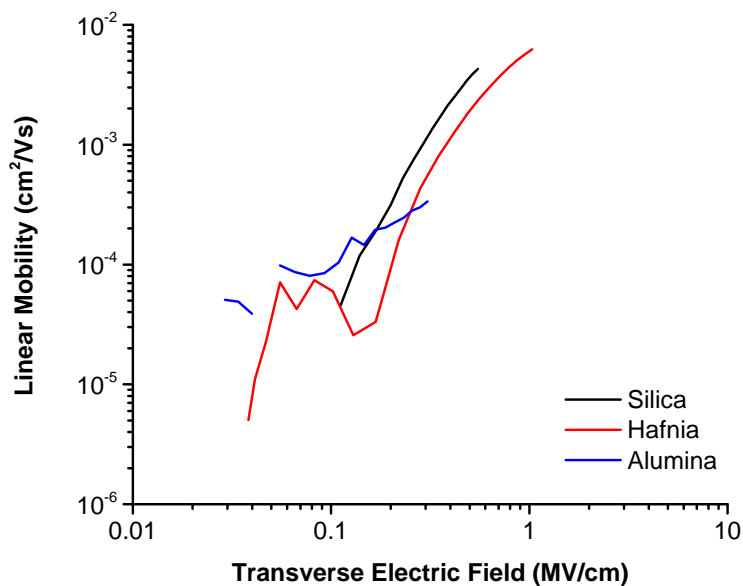


Figure 2.10: Linear mobility versus empirically derived transverese electric field for low-temperature annealed (250 °C) ZnO TFTs fabricated on various dielectrics.
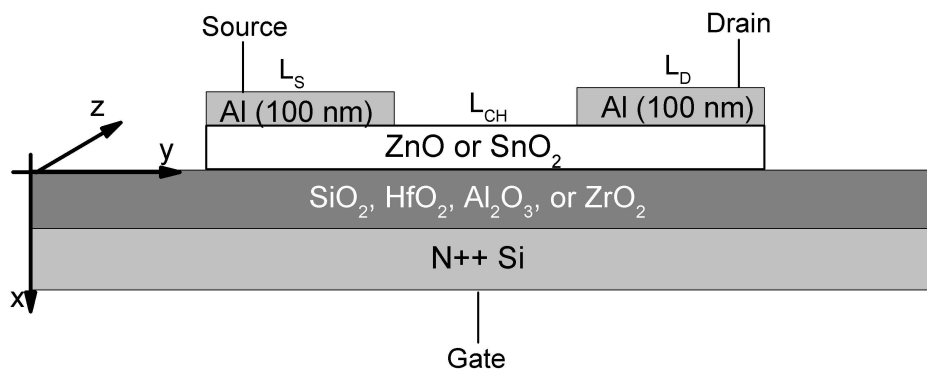
Figure 2.11: Inverted-staggered device structure used in this work. Physical channel length ($L_{CH}$), source electrode length ($L_S$), and drain electrode length ($L_D$) used for capacitance modeling shown in figure. Channel width (not shown) is in the z direction.

# Chapter 3

# Effect of Synthetic Conditions on Density of Localized States in the TCO Channel

The electrostatics and charge transport of disordered semiconductors are largely dominated by defects. Using the mobility extraction methodology of chapter 2, in this chapter we establish a relationship between synthetic conditions and electrostatic behavior of the semiconductor deposited onto thermally-grown $SiO_2$ prior to studying the interaction between the semiconductor and high-k dielectrics. Spray-deposited ZnO films were produced having a diversity of density of localized states profiles determined by defect properties induced via adjustment of synthetic conditions. We demonstrate a controlled mobility enhancement by synthetically modifying the shape of the density of localized states: increasing the band tail slope by increasing Zn precursor concentration and reducing the band edge concentration of shallow states by increasing substrate temperature, thus demonstrating the effect of synthetic conditions on electrostatic behavior as well as providing a means of more precise design of exceptional conductive oxide electronics through defect engineering.

## 3.1 Background and Introduction

Large-area, solution-based, roll-to-roll manufacturing techniques are gaining momentum as highly attractive methods for the manufacturing of next generation materials for displays due to their potential to lower production costs [85]. Additionally, replacing incumbent amorphous silicon technology with transparent conductive oxides (TCOs) mitigates existing design tradeoffs whereby a transparent thin-film transistor (TFT) permits transistor size optimization without sacrificing brightness due to light absorption/reflection [72]. Of the various low-cost deposition techniques available for depositing conductive oxides, spray-pyrolysis is particularly interesting, as it combines the synthetic versatility and low-cost benefits of solution-processing with the favorable growth mechanics afforded by an incre-

mental, vapor-like growth process - typically resulting in films of extraordinary electrical quality. Remarkably, zinc oxide (ZnO) thin-films having mobility as high as $85\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ have been integrated into TFTs using spray-pyrolysis on glass [1], roughly two orders of magnitude higher mobility than existing amorphous silicon technology [50] and comparable to some of the best sputtered oxide films [10].

Historically, spray pyrolysis has had the unfortunate drawback of being a blanket film deposition technique, therefore losing its appeal in comparison to the distinct low-cost benefits of purely additive manufacturing techniques such as inkjet-printing [11]. To address this issue, there have been several successful recent efforts to develop in-situ patterning ability of spray-deposited oxide films by exploiting surface-energy differences on substrates to facilitate film growth in targeted hydrophilic regions [99, 19, 90]. Having shown additive process capability, spray-pyrolysis may become a competitive low-cost manufacturing technology for next generation display materials. However, one additional drawback yet to be addressed is that TCOs are intrinsically conductive as-deposited. That is, regardless of the particular processing technique used, electrostatic behavior can be largely uncontrolled - ultimately determined by the synthetic process [59]. Lacking a method of electrostatic control, this implies the practical technological issue of implementing electronics having adjustable electrical properties.

Intrinsic defects and unintentional doping are presumed to play the dominant role in the observed conductivity of TCOs [59]. The influence of various intrinsic and extrinsic defects have been studied in detail [59, 89]. However, establishing direct links between conductivity and defect chemistry remains an ongoing experimental challenge, typically requiring more advanced characterization techniques [88]. This is particularly challenging in thin-films fabricated via solution-processing methods due to the parallel processes occurring during synthesis - drying, chemical conversion, film densification and crystallization [26, 9]. In ZnO and related TCO materials, the general consensus regarding the electron donation and defect compensation mechanism has shifted from one governed by oxygen vacancies to shallow hydrogen electron donors [89]. For example, recently Sirringhaus et al investigated the electronic structure of InZnO films highlighting the importance of hydrogen donor compensation of deep acceptor states by showing negligible changes in oxygen vacancy concentrations despite large differences in electronic conductivity [80]. However, they note the difficulty in experimentally distinguishing between defects due to variable differences in coordination numbers and bonding character - particularly challenging in disordered thin-films. Alternatively, from an electrostatic perspective, the electronic density of localized states (DOS) can be viewed as a representation of a particular defect spectrum resulting from a given synthetic condition. As a result, the DOS can be engineered through synthetic conditions - providing a degree of electrostatic control and practical advantage in the absence of knowledge regarding specific defect chemistry.

In this work we prepare nanocrystalline ZnO films by spray-pyrolysis in order to establish empirical relationships between synthetic conditions and the density of localized states as a means of achieving electrostatic control. Zinc oxide was selected based on its maturity and established high performance particularly in spray-deposited films [1]. By virtue of the low

carrier densities and small nanometer-sized grains obtained, grain-boundary barrier-heights
are determined to be negligibly small, enabling the use of the MTR model for DOS extraction. By varying the spray-pyrolysis deposition conditions - substrate temperature, precursor
concentration, and flow rate - we obtain a wide range of exponentially-distributed density of
localized states profiles and field-effect mobility values ranging over 3 orders of magnitude
$(0.02\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ - $30\,\mathrm{cm^2\,V^{-1}\,s^{-1}})$ for analysis using a simple, custom-built experimental
setup (Figure 3.1).
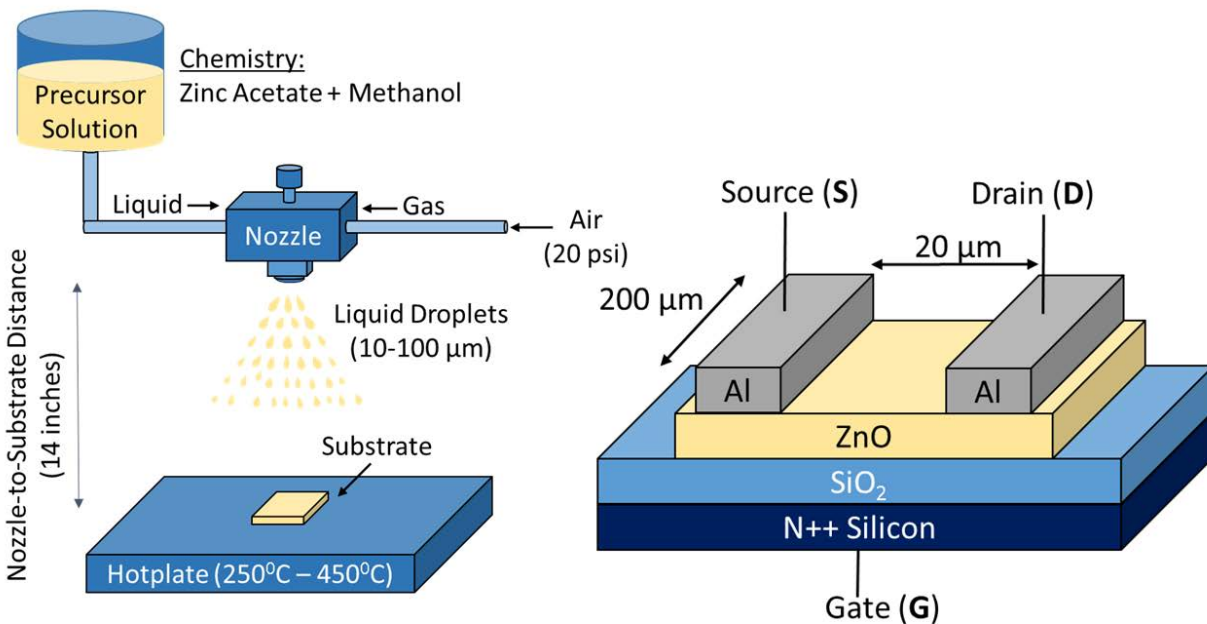


Figure 3.1: Illustration showing components of spray pyrolysis setup (left) and bottom-gate
top-contact thin-film transistor structure (right).

We find that mobility can be controlled by appropriately tuning the shape of the DOS
- increasing the band tail slope and reducing the band edge concentration of shallow states.
In doing so, we provide additional insight into how electron transport is influenced by the
shape of the DOS profiles commonly observed in many TCO materials which may also be
useful for other applications involving these materials such as the electron transport layer in
perovskite solar cells[22]. Most significantly, we show that the shape of the density of localized
states can be modified by adjusting the spray-pyrolysis deposition conditions for electrostatic
control. We find that higher Zn precursor concentration in solution increased the slope of
the band tails, leading to higher mobility. Additionally, the band edge concentration was
reduced with increased substrate temperature also leading to higher mobility. These results
demonstrate that electrostatic control via synthetic modification of the density of localized

states is a potential route to precise design of high-performance conductive oxide electronics and further underscores the utility of spray-pyrolysis as a technologically viable low-cost manufacturing technique for TCO materials.

## 3.2 Results

### Transfer Characteristics, Mobility and Activation Energy

We begin by evaluating the transfer characteristics and mobility in the linear regime (VDS = 0.1V) for each of the synthetic conditions as shown in Figures 3.2a-e. The specific synthetic conditions are labeled as an inset within each figure as an ordered triple - substrate temperature, Zn concentration, flow rate - along with the calculated average growth rate (film thickness/deposition time) and the film thickness. The conditions were simultaneously varied over a wide range to produce a variety of different behavior for analysis. To each synthetic condition we assign an identifier - denoted by the letters A, F, L, N, and O - used throughout this work. For each condition 10 devices were measured and were not found to exhibit significant device-to-device variation in terms of voltage dependence. As indicated, normal transistor behavior is observed in all cases - notwithstanding particular differences with regards to specific synthetic conditions. Linear mobility values, extracted using a technique published elsewhere [97], are observed to fall within a wide range $0.02\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ - $30\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ indicating significant electronic differences, as intended, to be used for further detailed investigation in regards to density of localized states. This measurement procedure was repeated at different temperatures in the range of $0\,°\mathrm{C}$ - $100\,°\mathrm{C}$ in order to obtain activation energy data necessary for density of localized states extraction. Figure 3.3 shows the activation energy as a function of gate-source voltage for each of the samples.
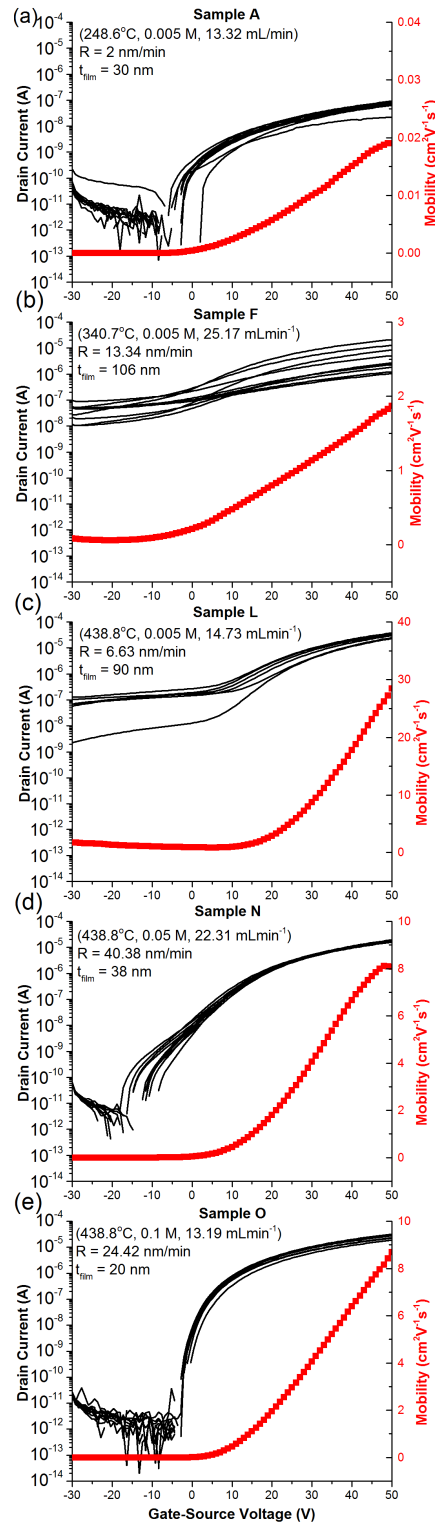
Figure 3.2: (a)-(e) Transfer characteristics and linear mobility ($V_{DS} = 0.1\,\mathrm{V}$) for each sample measured in a $N_2$ environment at room temperature. Data for 10 devices is shown in each case. Deposition parameters, including derived film growth rate and final film thickness are indicated for each condition.
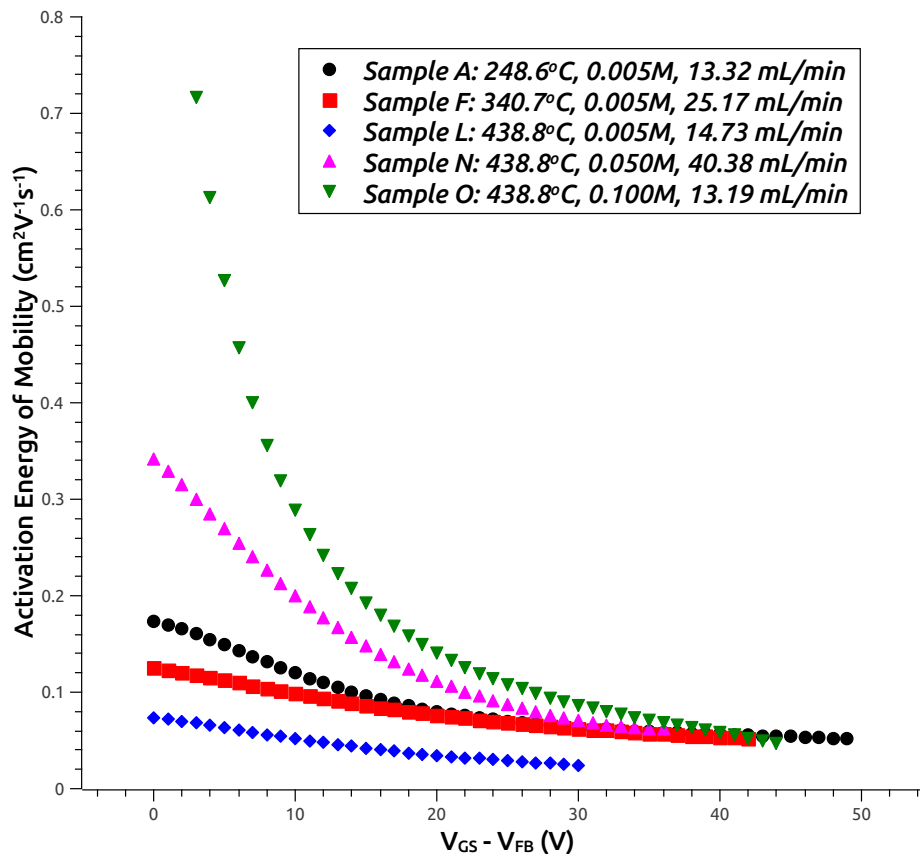
Figure 3.3: Activation energy as a function of gate-source voltage above flatband for each sample condition.

The activation energy decreases monotonically with increasing gate-source voltage, as expected for a trap-limited system. This data was used to extract density of localized states profiles for each condition. However, as previously mentioned, we must first rule out the possibility of barrier-lowering models providing an alternative explanation for the observed activated behavior.

## Grain-Boundary Barrier Heights

To evaluate the effectiveness of barrier lowering models, we estimate the barrier heights by evaluating Seto's model commonly applied to polycrystalline semiconductors [77].

$$E_b = \frac{eNL_g^2}{8\epsilon_r\epsilon_0} \tag{3.1}$$

Binary metal oxides have a tendency to crystallize, unlike their amorphous ternary and quaternary counterparts [22, 23, 17]. As evidenced by Figure 3.4, grazing-incidence x-ray diffraction data indicates that deposited ZnO films are polycrystalline and well matched to the provided powder reference (PDF Card 00-036-1451).
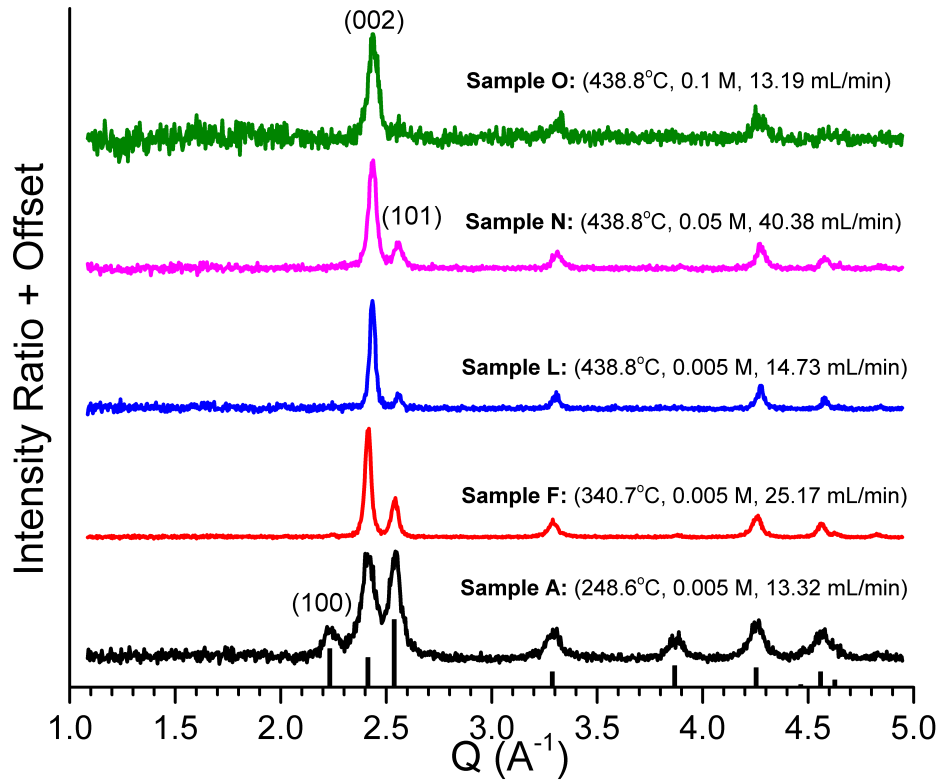


Figure 3.4: Grazing incidence x-ray diffraction data for each sample condition. Reference data shown corresponding to PDF Card 00-036-1451.

As input to the equation for the barrier height corresponding to grain boundaries, we use crystallite sizes obtained via Scherrer-Debye formula [73]

$$L_g = \frac{0.9\lambda}{\beta cos(\theta)} \tag{3.2}$$

and electron concentrations obtained from integration of capacitance-voltage data.

$$N = \frac{1}{t_{film}} \int_{V_{min}}^{V_{fb}} C(V_{gs})dV_{gs} \tag{3.3}$$

An upper bound for the estimation of the grain boundary barrier height is obtained using the FWHM of the narrowest peak, corresponding to the largest crystallites present in the

film. A summary of the data relevant for determining crystallite size estimates and barrier heights is given in Table 3.1, corresponding to the most prominent (002) crystal orientation. To convert areal charge density (obtained from capacitance) to volumetric charge density, we assume the accumulation charge to be uniformly distributed throughout the film thickness. This assumption is justified by the large Debye lengths ($\lambda_D$) and small film thicknesses ($t_{FILM}$) in these materials - such that $\lambda_D >> t_{FILM}$ - resulting in a fully-accumulated film [28]. Additionally, the carrier density is extracted at flat-band such that there is no band bending in the ZnO - further justifying the assumption of a uniform charge density. Using this data as input, in all cases, the grain boundary barrier heights are calculated to be significantly below the thermal energy at room temperature (0.026 eV) and therefore negligibly small. Such small barriers to conduction are inconsistent with relatively large measured activation energies of mobility (0.088 eV - 0.717 eV, Table 3.1) and therefore do not provide a physically-consistent alternative interpretation. This allows us to justifiably neglect barrier-lowering models and percolation and, instead, apply the more appropriate MTR model for interpreting the activation energy of mobility when deriving density of localized states.

| Sample | $N_{FB}$(cm$^{-3}$) | $E_A$(eV) | $Q_{002}$(Å$^{-1}$) | $FWHM$(Å$^{-1}$) | $L_G$(nm) | $E_{B,CALC}$(eV) |
|--------|---------------------|-----------|---------------------|------------------|-----------|------------------|
| A | $1.90 * 10^{16}$ | 0.173 | 2.41588 | 0.08816 | 7 | 0.0002 |
| F | $1.02 * 10^{17}$ | 0.130 | 2.41359 | 0.03827 | 15 | 0.0055 |
| L | $1.47 * 10^{17}$ | 0.088 | 2.43427 | 0.03433 | 17 | 0.0099 |
| N | $8.80 * 10^{16}$ | 0.305 | 2.43469 | 0.04896 | 12 | 0.0029 |
| O | $9.67 * 10^{16}$ | 0.717 | 2.43726 | 0.06123 | 10 | 0.0020 |

Table 3.1: Summary of grain size, flat-band carrier concentration, activation energy and grain boundary barrier heights computed from Seto's model for each sample assuming a dielectric constant of 10 for ZnO corresponding to the (002) orientation. Broadening factor assumed was 0.9. X-ray wavelength was 1.540 56 Å.

## Density of Localized States

The experimental techniques used to extract density of localized states profiles in disordered semiconductors are based on the interpretation of activation energies obtained from mobility measurements - assuming a particular transport mechanism. The models used to describe activated conduction in disordered solids are a combination of percolation conduction, hopping, barrier-lowering models and multiple-trap-and-release (or trap-limited conduction) [56]. A good illustration depicting these various mechanisms is provided in Lee et al [55]. Percolation conduction has been applied to nanocrystalline ZnO films to explain the onset of conduction (i.e. turn-on voltage) for a single midgap defect state [81]. In this model, site occupation probability is equated to the relative fraction of free carriers whereas bond formation

probability is given by a Boltzmann factor due to thermionic emission over grain boundary potential barriers. Physically speaking, the latter assumption is identical to that of barrier lowering models which we have already addressed previously. More commonly, percolation conduction is typically applied to ternary and quaternary compounds such as InGaZnO in the large gate-source voltage limit, in which percolation is expected due to random compositional disorder of cationic species comprising the conduction band [68]. Hopping conduction is present in sufficiently disordered materials, although tends to be only practically significant at low temperatures [65]. At higher temperatures, phonon absorption easily liberates localized electrons into extended states, so that, by comparison, hopping events contribute negligibly to the overall conductivity. Therefore, at sufficient temperatures, hopping conduction can be reasonably neglected, and binary conductive oxides (e.g. $ZnO$, $SnO_2$, $In_2O_3$) are expected to exhibit either a barrier-lowering or multiple-trap-and-release (MTR) mechanism. Barrier lowering was already ruled out due to negligble activation energy barriers at grain boundaries, leaving the MTR framework as a suitable description.

Following the assumptions of the MTR model, as is customarily done in literature regarding TCO TFTs [87], when deriving density of localized states profiles from temperature dependent mobility measurements, we assume that trap states below the Fermi energy make negligible contributions to the measured mobility. In other words, we ignore hopping conduction between them - a reasonable approximation at the sufficiently high temperatures used in this work ($0\,°C$ - $100\,°C$). Since mobility in purely hopping based systems tends to be low ($< 1\,cm^2\,V^{-1}\,s^{-1}$), this assumption is further justified by the relatively high mobility typically observed in TCOs ($10\,cm^2\,V^{-1}\,s^{-1}$ - $100\,cm^2\,V^{-1}\,s^{-1}$) and also in this work. Alternatively, we assume that mobility is limited by thermal excitation of trapped electrons distributed below the Fermi energy to the conduction band. This provides a convenient interpretation of the activation energy as the trap depth below the conduction band edge ($E_A = E_C - E_T$). Since the accumulation charge in the semiconductor is known self-consistently from integration of capacitance-voltage data, this produces a charge versus trap depth curve, which we subsequently fit to an assumed exponential distribution. The exponential distribution is characterized by two parameters - band edge concentration ($N_0$) and band tail slope ($E_0$) - and is a commonly used representation of the density of localized states for these materials [87, 82].

$$g_A(E) = \frac{N_0}{E_0} e^{\left(\frac{E - E_C}{E_0}\right)} \tag{3.4}$$

These assumptions form the basis of the commonly used multiple-trap-and-release model for mobility and are the foundation of the technique used to quantify the density of localized states profiles for each synthetic condition [87].

Density of localized states profiles for each condition were extracted based on the above assumptions. As shown in Figure 3.5a, the different synthetic conditions produce a wide range of DOS profiles for analysis.

These concentrations are reasonable when compared to other reports in literature for ZnO [87]. For reference, we also plot the theoretical free electron concentration for a bulk
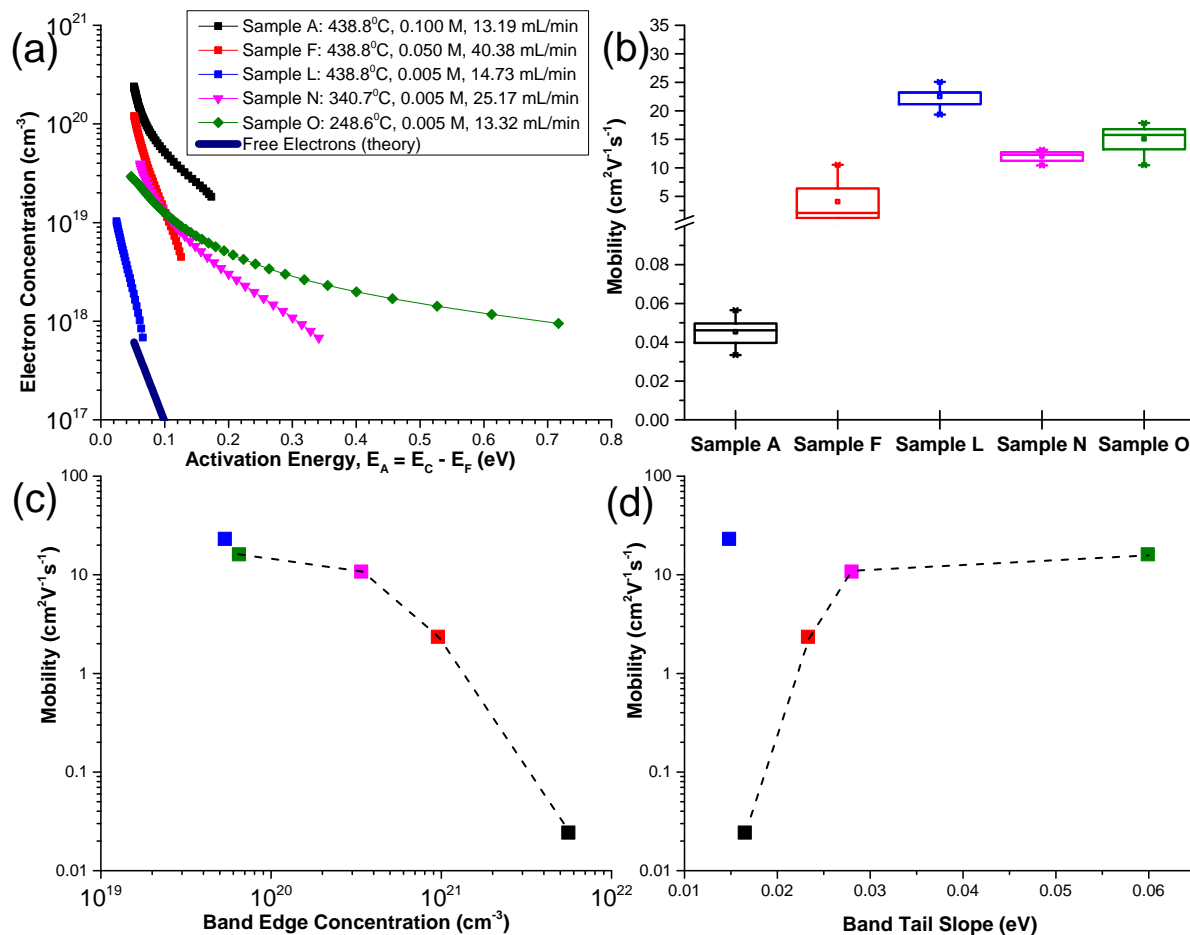
Figure 3.5: (a) Extracted localized carrier concentrations as a function of energy below the conduction band edge. (b) Box-and-whisker plot summary of mobility for the various sample conditions investigated. (c) Mobility as a function of extracted band tail concentration. (d) Mobility as a function of extracted band tail slope.

semiconductor using an effective conduction band density of localized states of $4*10^{18}$ cm$^{-3}$. The shape of the density of localized states profile can be generalized to an exponential distribution - parametrized into an energy slope parameter and concentration at the band edge.

A statistical summary of the mobility values corresponding to these conditions is provided in Figure 3.5b in which differences between samples can be seen to originate from the differences in density of localized states produced by varying synthetic conditions. In order to establish a general understanding as to how the specific shape of the DOS affects electron transport, we evaluate the mobility as a function of the band edge concentration ($N_0$) and band tail slope ($E_0$) as shown in Figures 3.5c-d. We find that the mobility is a strong

function of the shape of the density of localized states profile, exhibiting sensitivity to both
the band tail slope and band edge concentration. Evidently, as the band edge concentration is increased, the mobility reduces, dropping off rapidly at values exceeding $10^{21}$ cm$^{-3}$.
Furthermore, as the band tail slope increases, mobility is found to increase. Interestingly,
the greatest change in mobility occurs as the band tail slope approaches the thermal energy
(0.026 eV), below which, the mobility is greatly reduced. For the applicability of this analysis, it is assumed that free electron concentrations are much smaller than trap states (i.e.
trap-limited conduction). We note that the data point not included in the interpolations
in Figure 3.5c-d corresponds to the highest mobility sample (Sample L) which falls outside
of the scope of the MTR treatment due to its relatively low trap concentration - as can
be seen in Figure 3.5a. For the remaining conditions, however, localized electrons clearly
outnumber free electrons, so that the assumptions of trap-limited conduction are valid. We
illustrate this point more clearly by evaluating the ratio of free charge to total charge against
gate-source voltage (Figure 3.6a) as well as mobility against the ratio of free charge to total
charge (Figure 3.6b).

It can be seen that, for Sample L, the fraction of free carriers varies between 34 and 14
percent as the gate-source voltage is increased. This is a significant fraction of the total charge
such that the assumptions of trap-limited conduction may no longer hold (Figure 3.5d). For
the remaining samples however, the fraction of free carriers is below 3 percent such that the
trap-limited conduction assumptions are appropriate.

Having shown how the shape of the DOS profiles affects mobility, we now show how the
DOS profiles are modified by synthetic conditions - substrate temperature, Zn concentration,
and flow rate. For completeness, scatter plots corresponding to the data is given in Figure 3.7,
though the data is best visualized as a three-dimensional contour plot (Figure 3.8). By
inspection of Figure 3.7, substrate temperature and Zn concentration have the strongest
effects. It is immediately evident that increasing substrate temperature reduces the band
edge concentration (Figure 3.7a) and increasing the Zn concentration increases the band tail
slope (Figure 3.7e) - both actions leading to higher mobility.

Trends with flow rate are much more subtle, due to the overwhelmingly strong effects of
substrate temperature and concentration. To better illustrate the correlated nature of the
effects of the various synthetic conditions, in Figure 3.8 we depict the same data as a series
of contour plots corresponding to all possible parameter pairs. Contour plots corresponding
to band tail slope are shown in Figures 3.8a-c, while those corresponding to band edge concentration are shown in Figures 3.8d-f. Here, the strong effects of substrate temperature and
Zn concentration are clearly indicated. In general, increasing substrate temperature and Zn
concentration is beneficial in increasing band tail slope and reducing band edge concentration - thereby increasing mobility. Therefore, we reiterate that in regards to synthetically
tuning the density of localized states profiles so as to maximize mobility, it is necessary to
increase the band tail slope and reduce the band edge concentration achieved by adjustment
of two deposition parameters - Zn concentration and substrate temperature.
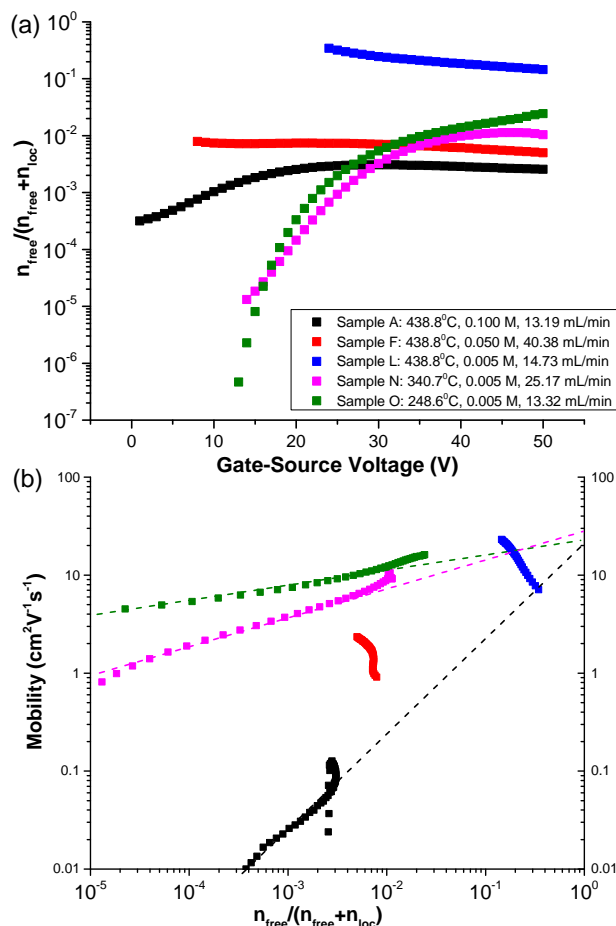
Figure 3.6: (a) Fraction of free carrier concentration to total carrier concentration as a function of gate-source voltage. (b) Mobility as a function of fraction of free carrier concentration to total carrier concentration.

## 3.3 Discussion

### General Transport Behavior

The general dependence of mobility on the density of localized states profile can be explained using Fermi-Dirac statistics, offering additional insight into electronic transport in systems having exponentially-distributed band-tails. As the Fermi energy moves closer towards the conduction band edge, more electrons are promoted both into free states as well as localized states. This follows from the fact that the density of localized states increases towards the conduction band edge (Figure 3.5a). The rate of population of free states is fixed and determined by the thermal energy (i.e. Boltzman statistics), whereas the rate of population of localized states is variable depending on the band tail slope. When the band tail slope be-
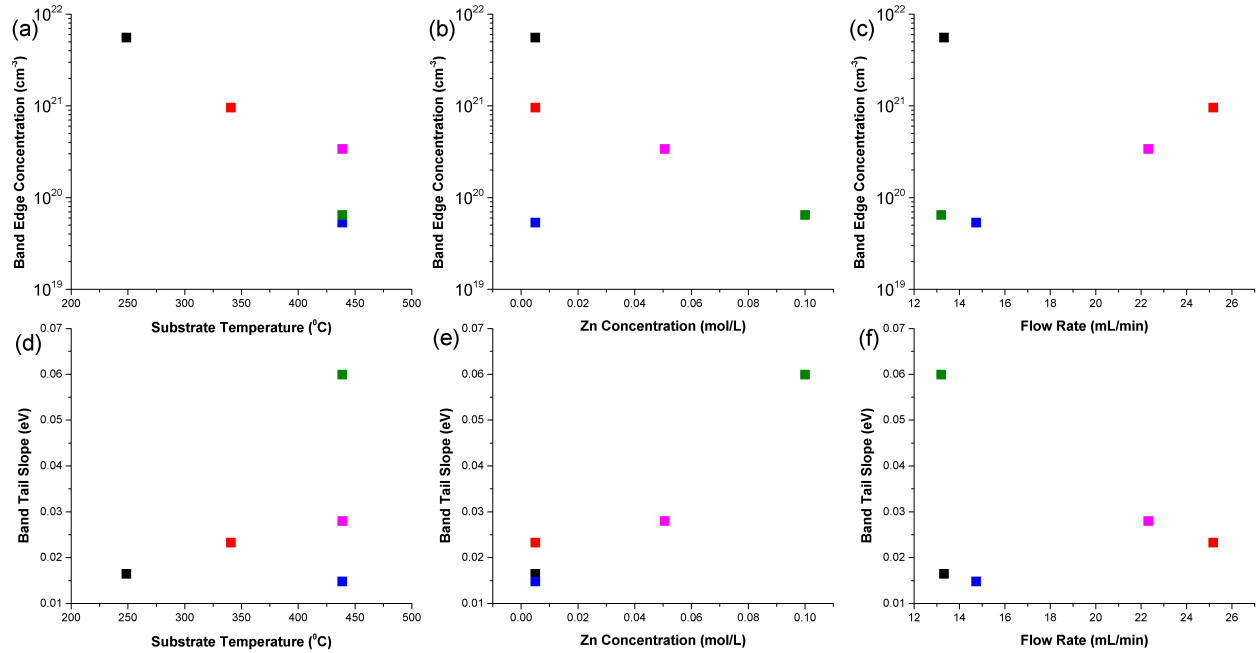
Figure 3.7: (a)-(c) Influence of substrate temperature, zinc concentration and flow rate on band edge concentration and (d)-(f) band tail slope.

comes less than the thermal energy, a greater proportion of induced electrons are expected to occupy localized states than free states upon increasing the Fermi energy towards the conduction band edge. These localized states correspond to ionized acceptors [87] and are therefore expected to scatter free electrons as they become occupied. Therefore, when the Fermi energy enters these shallow states (corresponding to high gate-source voltages) such that activation energies become small and sufficient carriers thermally-excite into the conduction band, transport may become limited by impurity scattering rather than availability of carriers. In other words, in addition to the benefit gained by having more electrons in free states, there is a proportional increase in ionized impurity scattering, potentially limiting systems having band tail slope below the thermal energy.

## Relation of Mobility to Film Orientation and Hydroxide Content

Film orientation and hydroxide content are two of the most important factors known to impact the electron mobility in ZnO thin-films. Evidently, as-deposited ZnO thin films tend to be polycrystalline, having a mobility which is strongly dependent on film orientation - exhibiting the maximum mobility for c-axis (002) oriented films [22]. Consequently, there is a wealth of data showing reduction in mobility due to reduction of texture in ZnO. Likewise, mobility has also been shown to be negatively correlated to hydroxide content [37]. This is
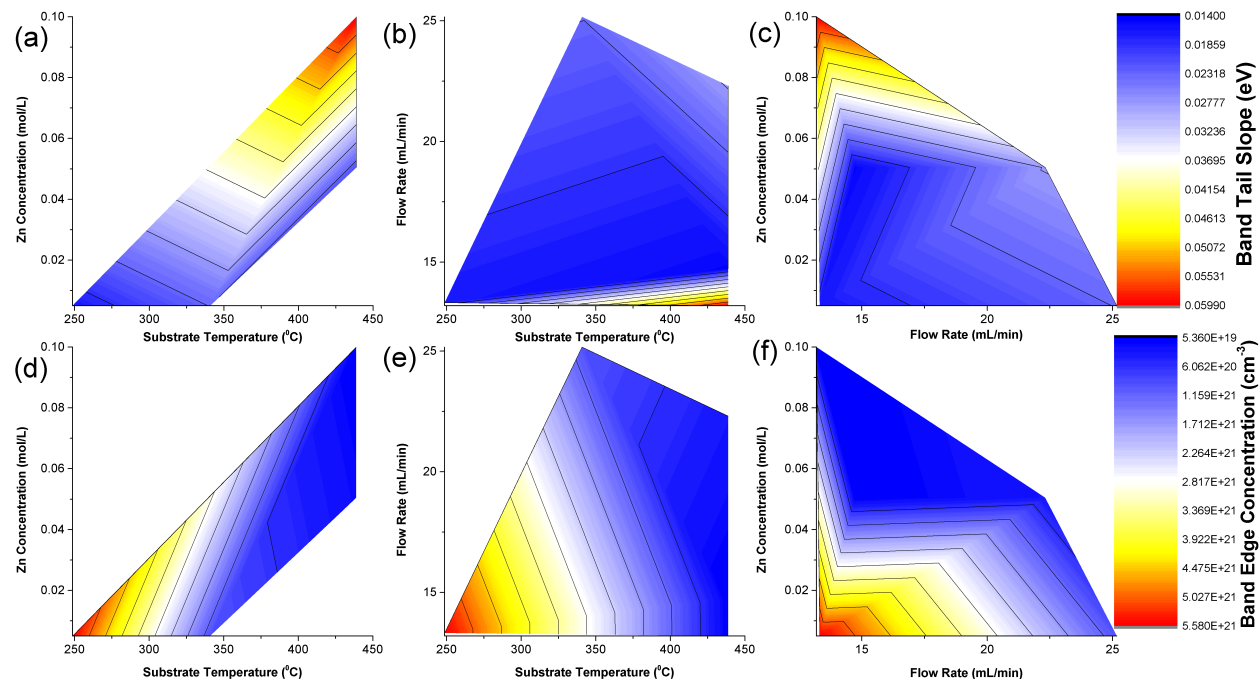
Figure 3.8: Contour plots of band tail slope (a)-(c), and band edge concentration (d)-(f) as a function of spray deposition parameters.

a rather ubiquitous observation across metal oxides in general (e.g. $SnO_2$, $In_2O_3$, and ZnO to name a few), and is particularly problematic when low processing temperatures are used. Zinc acetate dehydrate decomposes to oxide and/or hydroxide species between 190 °C and 310 °C [69]. Marks et al showed that InZnO films annealed below 300 °C were almost exclusively composed of metal-hydroxide species rather than desired metal-oxide species [38]. At higher processing temperatures, conversion to the oxide may be non-limiting, and mobility may show a weaker dependence upon hydroxide content. For example, Cho et al showed a relatively insensitive field-effect mobility to the presence of the high energy peak associated with hydroxide or loosely bound oxygen [7]. Other factors such as porosity, residual carbon and/or counter ions are also important but none have been shown to impact mobility as strongly as do film orientation and hydroxide content. Therefore, we evaluate our observations of mobility within the context of hydroxide content and film orientation, in an attempt to gain further insight regarding the changes in density of localized states.

As shown in Figure 3.9a, ZnO films have noticeably different orientations, depending on the synthetic conditions.
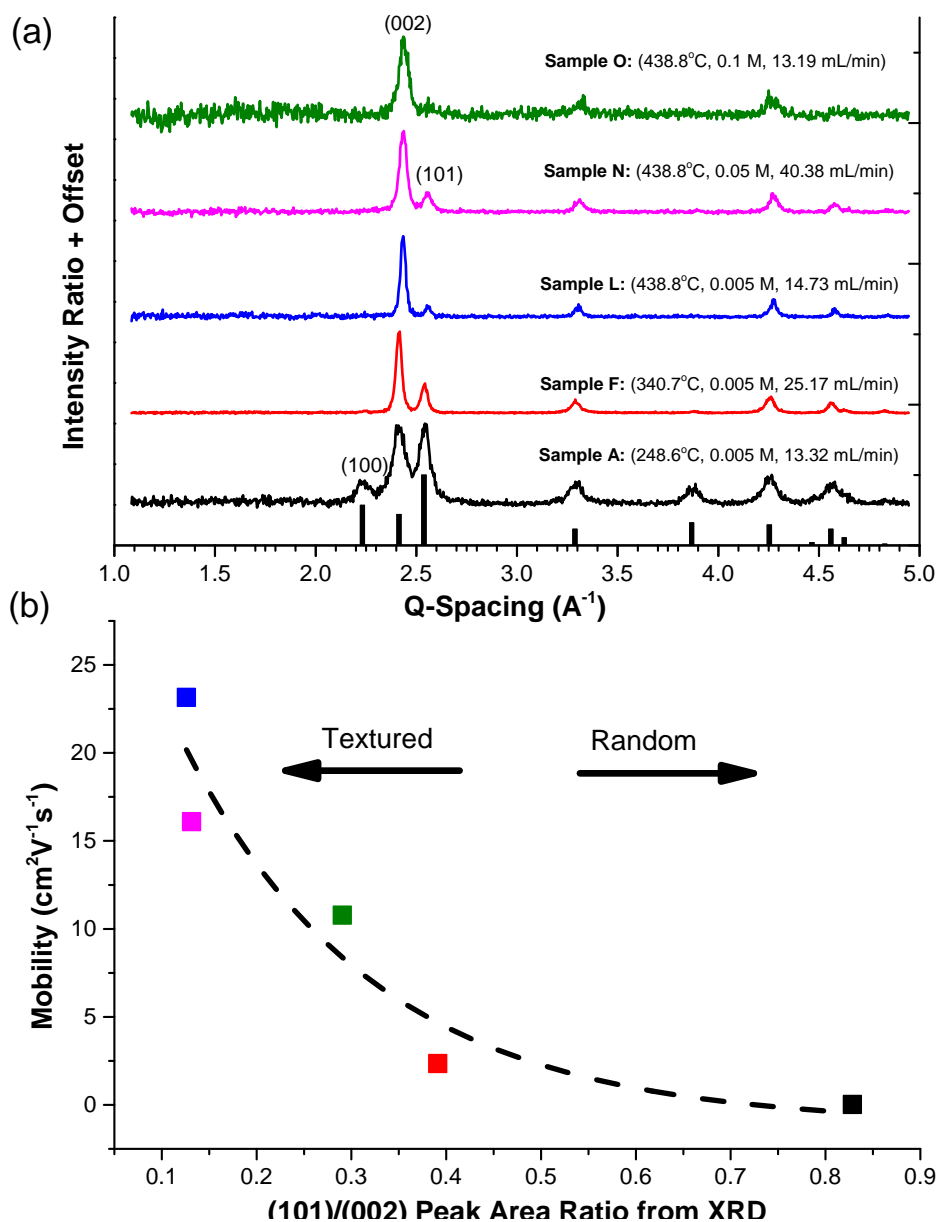
Figure 3.9: (a) Grazing-incidence x-ray diffraction (GIXD) data and (b) linear mobility as a function of (101)/(002) ratio of integrated peak areas.

In Figure 3.9b, we evaluate the effect of this orientation dependence on mobility by plotting mobility versus the ratio of the integrated area of the (101) and (002) peaks. As expected, mobility increases strongly as the films become increasingly oriented along the (002) direction. In Figure 3.10, SEM images indicate a rough surface topology consisting of grains protruding at different angles.

This occurs due to the columnar-like growth of hexagonal ZnO grains [24] and is es-
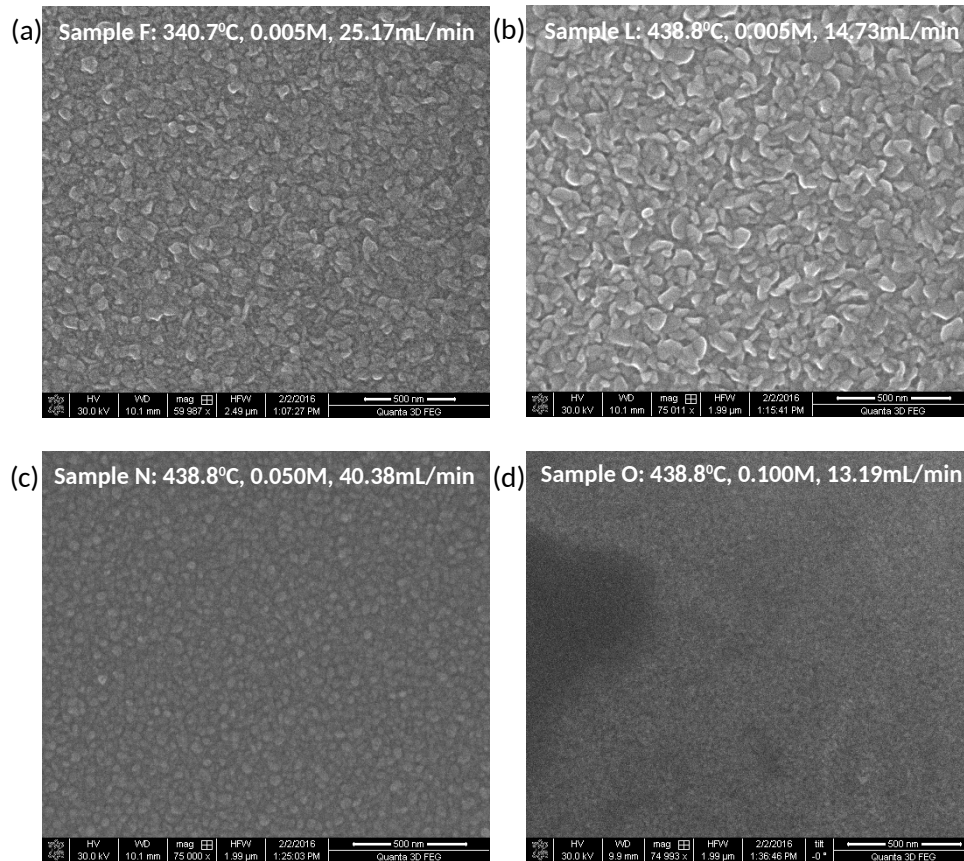
Figure 3.10: SEM images of various films. Images (a)-(d) correspond to Samples F, L, N and O respectively. Sample A was unable to be imaged effectively due to its low carrier density.

sentially a visible representation of the observation of different orientations observed in the diffraction pattern. High resolution TEM studies of grain boundaries in ZnO indicate different atomic structures at grain boundaries depending on the degree of mismatch between lattice planes[34]. Therefore, it is plausible that the DOS modification we achieve by adjusting synthesis conditions originates due to the behavior of grain boundary defects affected by differences in film orientation. This is supported by the observation that metal-organic precursors can be converted into metal-oxide structures leading to functional TFTs at low temperatures. Our observations suggest that an additional knob for tuning electrostatics by adjusting film orientation after conversion into the metal-oxide has taken place. However, in our case, it is necessary to quantify the presence of unconverted species (e.g. hydroxide) in these films in attempts to separate these effects from crystallinity/orientation related effects.

The chemical composition of the films was assessed via XPS by comparing the O(1s) core states as shown in Figure 3.11. As is customarily done in literature, we separate the

total O(1s) peak into two peaks, assigning the higher energy peak to hydroxide and the lower energy peak to metal oxide. It is also common to include a third peak having binding energy between the hydroxide and oxide components, which is believed to be due to oxygen vacancies [41], however, we were able to obtain reasonably good fits to the data by using just the aforementioned two peaks. Mobility was plotted as a function of hydroxide content $(O_{OH}(1s)/O_{TOTAL}(1s))$ to evaluate the impact of conversion on transport. We find that as the hydroxide content increases, mobility reduces, as is commonly observed in literature[36]. However, film orientation tends to obscure a clear trend - as is evidenced by the apparent outlier in Figure 3.12a, corresponding to a randomly oriented film (Sample A). Again, we evaluate these correlated effects on a contour plot to attempt to separate the main effects (Figure 3.12b).
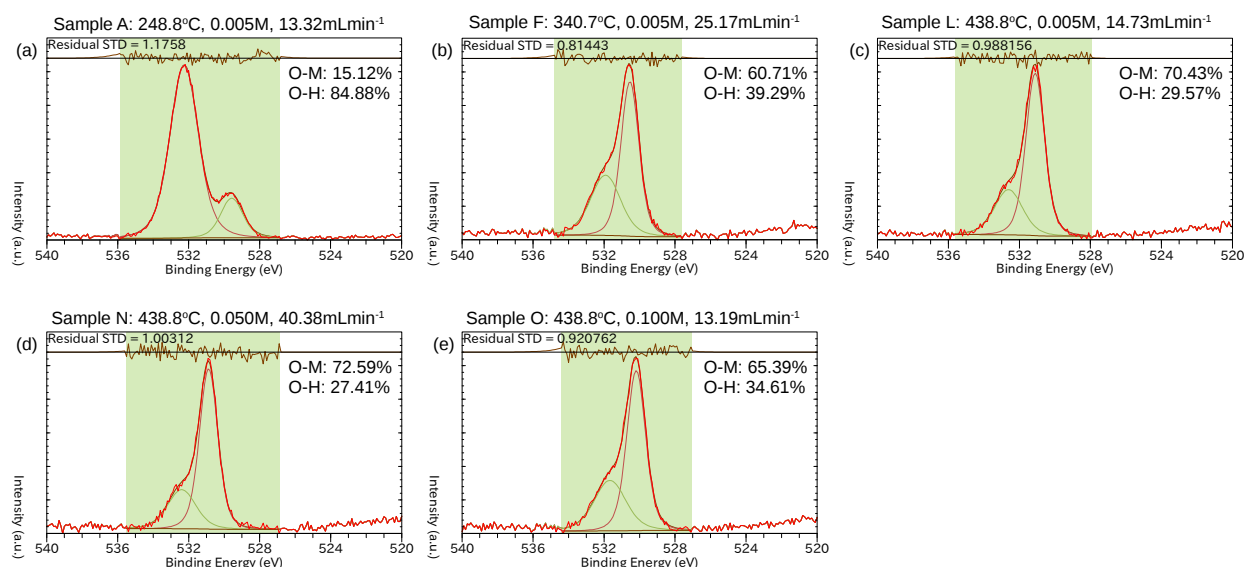


Figure 3.11: X-ray photoelectron spectroscopy results of the oxygen 1s peak for (a) Sample A, (b) Sample F, (c) Sample L, (d) Sample N and (e) Sample O. In each case, the raw data is shown in red. Fits for the metal-oxide (O-M) and hydroxide (O-H) contributions are also shown in green and brown along with the resulting estimated contributions from each species by percentage area.

As shown, both hydroxide content and orientation have strong effects on mobility - showing mobility enhancement with reduced hydroxide content and increased (002) texturing. As a result, we cannot determine which effect dominates in this particular case.
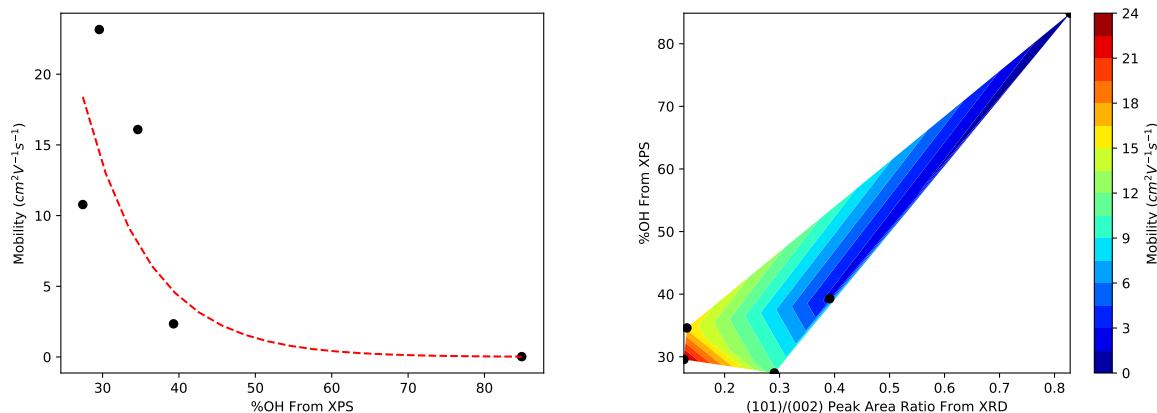
Figure 3.12: (a) Mobility as a function of hydroxide content. (b) Contour plot of mobility versus hydroxide content and extent of texture, as indicated by percent OH obtained from O(1s) peak analysis and integrated peak ratios (101)/(002) from GIXD respectively.

## 3.4   Conclusion

In summary, we have demonstrated a simple means of electrostatic control in zinc oxide thin-film transistors by showing how the synthetic conditions of spray pyrolysis - substrate temperature, precursor concentration and flow rate - can be adjusted to modify the electronic density of localized states profiles, thus providing electrostatic control. By approximating the defect spectrum as an exponential distribution, we parametrize the density of localized states into two components - band edge concentration and band tail slope - and have shown how to modify these independently to adjust film properties for higher mobility. We find that increasing substrate temperature results in significant reduction in band edge concentration while increasing Zn concentration increases the band tail slope - both of which resulted in higher mobility. Investigation of film crystalline orientation and hydroxide content show that both are significant factors in determining mobility, although unfortunately we were unable to clearly isolate the dominant effect. Most importantly however, this work shows that the defect spectrum (i.e. electrostatics) in ZnO is synthetically tunable and can be made to achieve a particular electrostatic behavior for transistor applications. Furthermore, since the analysis is based on widespread observation of exponentially-distributed density of localized states profiles common to several TCO materials, it may be possible to modify the

electrostatics of other semiconducting TCOs (e.g. $In_2O_3$, InGaZnO, InZnO, ZnSnO etc...) using this same strategy as well. Having provided a simple means to address the practical issue regarding the lack of electrostatic control in TCO based TFTs, the utility of spray-pyrolysis as a viable, low-cost manufacturing technique for future displays becomes more readily apparent. In the next chapter, we extend the utility of this methodology to compare differences in the density of localized states between ZnO films deposited identically onto different dielectrics.

# 3.5 Experimental Methods

## Zinc Oxide (ZnO) Precursor Solution

The ZnO precursor solution consisted of zinc acetate (Aldrich 383317) dissolved in methanol at various concentrations (0.005M - 0.1M).

## Zinc Oxide (ZnO) Thin-Film Preparation

Semiconducting ZnO thin-films were prepared using a spray pyrolysis technique. The precursor solution was sprayed onto heavily doped n-type silicon wafers prefixed as having $100\,nm$ of thermally-grown $SiO_2$ which served as the gate dielectric. These substrates were placed on a hotplate ($250\,°C$ - $450\,°C$) at a stationary fixed nozzle-to-substrate distance of $14\,in.$ using compressed air at 20 psi and the precursor solution was directed onto the substrates at various flow rates ($1\,mL\,min^{-1}$ - $20\,mL\,min^{-1}$).

## Metallization and Lithography

Aluminum (100 nm thick) was thermally evaporated (1-2 microTorr) to serve as source/drain electrodes. ZnO was patterned using standard I-line photolithography and etched in aqueous hydrochloric acid (1:500 $HCl:H_2O$).

## Electrical Characterization

Long channel devices (channel length/width = $200\,µm/20\,µm$) were measured using an HP4155C semiconductor parameter analyzer under medium integration time. All mobility measurements were performed in the linear region ($V_{DS} <= 100\,mV$) according to an improved combined capacitance/conductance (C-V/G-V) technique reported in detail elsewhere [97]. density of localized states profiles were extracted using temperature-dependent mobility measurements in the temperature range of $0\,°C$ - $100\,°C$ in a nitrogen environment. Nitrogen was used as an ambient to reduce moisture absorption on the exposed back surfaces of the ZnO films.

## Morphological Characterization

Film thickness was characterized using a Dektak profilometer. The chemical composition of the deposited films was evaluated using x-ray photoelectron spectroscopy (XPS) on a PHI 5000 VersaProbe. The crystallinity of the deposited films was determined using x-ray diffraction on a PANalytical X'PERT system in grazing-incidence mode at 0.14° with a Cu K-a source having a wavelength of 1.540 56 Å. SEM images were obtained using a FEI Quanta 3D FEG system.

# Chapter 4

# Electron Donation from Donor States in High-k Gate Dielectrics

Having developed a suitable experimental methodology for quantifying the field-effect mobility of disordered-channel TFTs in chapter 2 as well as establishing the general relationships between defect-dominated electrostatics and transport in chapter 3, in this chapter we investigate the interactions between high-k dielectrics and the TCO semiconductor. High-mobility ZnO thin-films were deposited onto solution-processed $ZrO_2$ dielectrics as well as thermally-grown $SiO_2$ in order to investigate the large differences between experimental field-effect mobility values obtained when transparent conductive oxide (TCO) materials are deposited onto high-k dielectrics as opposed to thermally-grown $SiO_2$. Through detailed electrical characterization, we correlate the mobility enhancement in ZnO to the presence of donor-like electron traps in $ZrO_2$ serving to provide an additional source of electrons to the ZnO. Furthermore, as a consequence of the general tendency for solution-processed high-k dielectrics, in particular, to exhibit similar behavior, we suggest the broad applicability to other TCO/high-k material combinations in agreement with experimental observations.

## 4.1 Background

It is a remarkable experimental fact that semiconducting transparent conductive oxide (TCO) thin-film transistors (TFTs) consistently exhibit higher electron mobility when used in conjunction with high-k gate dielectrics (10 to $100\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$) as opposed to thermally-grown $SiO_2$ (0.1 to $20\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$). To date, this observation has been regularly reproduced experimentally by several authors using different combinations of semiconducting TCOs and high-k gate dielectrics, underscoring its broad applicability across multiple material systems [48, 18, 96, 32, 13, 84, 21, 66, 52, 100, 14, 93, 6, 1, 53]. In addition, this property has enabled recent advancements in TCO based TFTs at plastic-compatible temperatures for use in flexible and wearable electronics. [76] Despite the large amount of empirical data exploiting this trend for its benefits, to the best of our knowledge, there are no established theories

identifying the origins of the observed mobility increase, which, due to a lack of understanding, greatly limits the engineering of devices to maximally benefit from its utility. [54, 15] Indeed, this mobility enhancement has even been observed in solution-processed TCO-based thin film transistors, which are attractive as candidates for very low-cost printing-based processing [35, 34]. Although expected to meet the demands imposed by emergent technological applications, most demonstrations of high mobility ($> 20\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$) solution-processed TCOs require high annealing temperatures incompatible with plastic substrates. As a result, it is unclear as to whether or not solution-processed TCOs can maintain high performance at plastic compatible temperatures, and modern trends in research seek to achieve this goal. Accomplishing this goal relies on innovations in materials processing as well as identifying physically-based routes exploiting beneficial interactions with other materials so as to maximize performance at lower processing temperatures. We highlight the importance of the latter in this work, by explaining a method of circumventing performance limitations of low-temperature solution-processed TCOs through the interaction with optimally-tuned solution-processed high-k dielectrics.

Recently, Lee et al. (2014) proposed that a higher field-effect mobility can result from an increased gate capacitance (i.e. increased charge) stemming from the higher dielectric constant of the gate insulator relative to $SiO_2$. [51] Their work closely resembles that of Shur et al., who developed a similar mobility model for use in amorphous silicon TFTs based on the multiple-trap-and-release (MTR) model. [79] These models are particularly useful in describing the gate-voltage and capacitance dependent field-effect mobility of TFTs having gate dielectrics that exhibit simple insulating behavior. They predict that, independent of the choice of gate dielectric material, the maximum field-effect mobility observed should be a constant defined by the semiconductor, where higher mobility values can be obtained by simply increasing the transverse electric field (e.g. higher voltage or higher capacitance). However, when mobility data is plotted against the transverse electric field, which normalizes the data against differences in gate voltages and gate capacitance, trends are non-overlapping, and a clear dielectric dependence is revealed. [98] Typically, the maximum obtainable field-effect mobility depends on the choice of dielectric, generally showing considerably higher values on high-k dielectrics than on $SiO_2$. [48, 18, 96, 32, 13, 84, 21, 66, 52, 100, 14, 93, 6, 1, 53]

Explanations that address the difference in maximum mobility typically claim an improvement of the TCO/dielectric interface quality, suggesting a reduction in interface trap states as one might expect intuitively based on an understanding of silicon MOSFETs. [48, 18, 96] However, there are several problems with these arguments. Since solution-processed TCOs are typically amorphous or polycrystalline with nanometer sized grains [3], there are several internal surfaces within the TCO itself leading to high concentrations of localized states. As a consequence, the influence of the interface trap density on transport cannot be easily isolated from that of the many traps within the semiconductor bulk. Additionally, according to the mobility model by Street, [83] which follows from trap-limited conduction, [56] the maximum mobility should coincide with a maximum emission rate from localized states, which is usually obtained for sufficient band bending (i.e. high transverse electric fields)

causing the Fermi level to enter the shallow band tail states. In such a scenario, electrons emitting from deep interface states are expected to contribute negligibly to the conductance at high transverse electric fields (i.e. surface accumulation) and, consequently, are unlikely to explain the difference in maximum mobility. Therefore, it is evident that existing descriptions based on ideal insulating behavior provide an inconsistent account for the observed dielectric dependence of the TCO mobility, and a new theory is needed that accounts either for non-ideal insulating behavior or electronic interaction between the gate dielectric and the TCO.

High-k dielectrics routinely exhibit non-ideal insulating behavior. Characteristically, their integration into transistors has been complicated by their tendency to manifest various charged defects such as fixed charges, electron traps and mobile ions. [53] The effect this has on silicon MOSFETs is well studied and is often characterized by anomalous hysteresis in the transfer characteristics, bias/temperature stress instability and/or a degradation in field-effect mobility due to increased scattering. [57] Related observations have been made in TCO based TFTs, especially those having dielectrics fabricated using solution-processing techniques, [92] although fortunately the field-effect mobility is typically enhanced, not degraded. To date, efforts have been made to reduce hysteresis and improve bias stress stability in TCO based TFT devices, although the mechanisms for the mobility enhancement remain unidentified. [92] Therefore, the goal of this chapter is to address these unexplained observations through a more systematic electrical investigation and offer a comprehensive explanation for the field-effect mobility enhancement in TCO based TFTs incorporating high-k gate dielectrics. As a representative system, we analyze the field-effect mobility enhancement in TCO based TFTs composed of a solution-processed ZnO semiconducting TCO layer deposited onto a solution-processed high-k $ZrO_2$ gate dielectric. This particular interface was selected for study since it has recently been reported to give anomalously high performance comparable to sputtered TCO films using a much simpler solution-based spray pyrolysis deposition technique [1]. Additionally, this particular material system has been extensively characterized in terms of the achievable morphology and physical characteristics by means of transparency, surface topography, X-ray diffraction (XRD) and X-ray photoemission spectroscopy (XPS) [18, 1, 3, 71]. Here, we focus on a systematic evaluation of the TFT electrical characteristics to gain insight into the underpinnings of the observed mobility enhancement. By performing precise mobility measurements based on the improved combined capacitance-conductance (C-V/G-V) extraction technique described in Chapter 2 [97] and studying the influence of the $ZrO_2$ processing temperature on mobility and the exponentially-fitted density of states in the ZnO described in Chapter 3, [87] we correlate the mobility enhancement in the ZnO to the presence of trapped electrons in the $ZrO_2$. We use simple proposed mechanisms deduced purely from electrical data to show that these trapped electrons are responsible for counterclockwise hysteresis as well as the mobility enhancement by increasing the steady-state electron density in the ZnO. Based on our understanding of this system and the general non-ideal behavior exhibited by solution-processed dielectrics, we propose the general application of this phenomenon to other TCO/high-k interfaces.

## 4.2 Establishing a Baseline Comparison to Thermally-Grown SiO$_2$

Earlier reports of anomalously high field-effect mobility in the ZnO/ZrO$_2$ system utilized a chemistry for the ZrO$_2$ layer derived from zirconium acetylacetonate. Zirconium acetylacetonate is known to undergo complete decomposition into zirconium dioxide via calcination at rather high temperatures ($> 750\,°$C), [33] although it is regularly used in TCO based TFT processes at much lower temperatures. [1] However, using this chemistry, we observe unusually large low-frequency dispersion and find that it is necessary to anneal the films at very high temperatures ($> 700\,°$C) in order to completely eliminate the dispersive trend (Figure 4.1, page 61). As shown, ZrO$_2$ films derived from zirconium acetylacetonate tend to have a low-frequency dielectric constant that gradually decreases from a large value, where films are dispersive, towards the bulk ZrO$_2$ value, where films are non-dispersive, as the processing temperature is increased, likely because the film is undergoing conversion into the oxide. Since low-frequency dispersion in dielectrics can confound mobility extraction, we selected ZrO$_2$ films annealed at $700\,°$C to facilitate our initial comparisons with thermally grown SiO$_2$. These films were approximately 25 nm thick, exhibited negligible frequency dispersion and a uniform dielectric strength with no evidence of early breakdown events for more than 20 devices, as indicated by the plot of current density versus electric field (Figure 4.1).

Zinc oxide thin-films derived via spray pyrolysis were deposited onto the aforementioned sol-gel derived ZrO$_2$ dielectrics as well as onto thermally-grown SiO$_2$ in a bottom-gate device configuration and were found to have similar film thickness (20 nm) and a specific contact resistance (4 to $5\,\Omega$ cm, extracted via TLM) using thermally evaporated aluminum source/drain electrodes (Figure 4.2).

However, examination of the field-effect mobility and the density of states reveal significant electrical differences between these films (Figure 4.3).

Using an improved method of quantifying mobility [97], we observe that the maximum field-effect mobility of the ZnO/ZrO$_2$ films ($26\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$) was approximately triple that of the ZnO/SiO$_2$ films ($9\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$). Detailed investigation of the mobility as a function of transverse electric field indicates that, although there is an intermediate region where the mobility of the two overlap ($0.75$-$1.2\,\text{MV}\,\text{cm}^{-1}$), they diverge at low and high electric fields demonstrating a clear dielectric dependence (Figure 4.3a). According to Gauss' law, the transverse electric field is proportional to the induced charge in the ZnO. Therefore, at low electric fields (i.e. lower induced charge), a significantly larger fraction of the induced charge is delocalized in the ZnO/ZrO$_2$ system compared to the ZnO/SiO$_2$ device, as indicated by the higher mobility.

To gain additional insight regarding these mobility differences, we examined the density of states for each device which was extracted using a common multiple-trap-and-release (MTR) framework wherein localized states are treated as traps (i.e. zero average conductivity) and are exponentially distributed in energy [87]. Inspection of the density of states (Figure 4.3b),

Figure 4.1: Electrical data for $ZrO_2$ thin-film capacitors (N++ Si/$ZrO_2$/Al) processed using a chemistry composed of zirconium acetylacetonate dissolved in methanol. (a) Dielectric constant of $ZrO_2$ films as a function of frequency with annealing temperature as a parameter varied from 150 °C to 700 °C. (b) Current density as a function of electric field for 20 different devices in total.

indicates that, unlike the ZnO/$SiO_2$ device, the Fermi level in the ZnO/$ZrO_2$ device resides in a region of high state density, at shallower energies nearer to the ZnO conduction band edge where thermal emission rates from localized states are higher [49]. According to the trap-limited drift mobility model proposed by Street [82], this should result in a higher mobility and is consistent with our observations. Furthermore, the subthreshold swing for each device was evaluated and plotted as a function of temperature (Figure 4.4, page 64). Both devices show a swing reduction with increase in temperature, consistent with thermally-activated conduction. Additionally, the swing was higher in the ZnO/$ZrO_2$ system, consistent with a higher shallow density of localized states.

Again, we emphasize that both films were processed identically, having the same film thickness and contact resistances, although there appears to be a mysterious difference in the density of states, the ZnO/$ZrO_2$ containing additional shallow states. The unknown source of these additional states prompted further investigation into the electrical properties of the $ZrO_2$ itself, since, as previously stated, high-k dielectrics are prone to exhibit electrically charged defects that can influence the perceived state density in the ZnO.
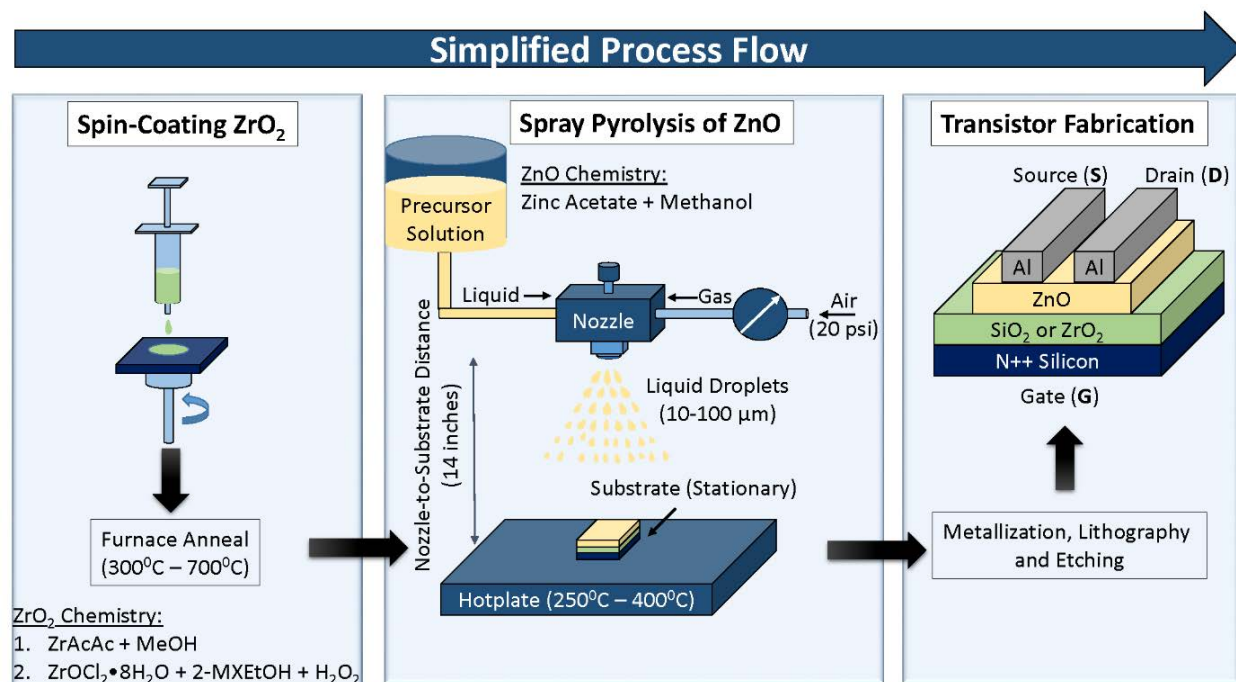
Figure 4.2: Process flow and depiction of spray pyrolysis setup as well as completed bottom-gate, top-contact thin-film transistor (TFT) structure.

## 4.3   Correlating ZrO$_2$ Defects to ZnO Mobility

To investigate the origin of the higher shallow state density in the ZnO/ZrO$_2$ devices, we evaluate the impact of different ZrO$_2$ annealing temperatures, as this should result in different electrical properties in the ZrO$_2$ which should influence the mobility in the ZnO. The previous comparisons were made using a ZrO$_2$ process that required high annealing temperatures ($> 700\,^\circ$C) due to the relatively high decomposition temperature of the zirconium acetylacetonate. Using an improved chemistry composed of zirconyl chloride dissolved in 2-methoxyethanol and hydrogen peroxide, we were able to fabricate relatively non-dispersive ZrO$_2$ films (Figure 4.5) at lower temperatures between $300\,^\circ$C and $500\,^\circ$C according to a process reported elsewhere. [71]

As shown in Figure 4.5, these films exhibit improved dielectric strength and low dispersion at lower temperatures, unlike the zirconium acetylacetonate system. Also, previous ZnO films were deposited at $400\,^\circ$C, therefore for the sake of comparison, in order to maintain a thermal budget limited by the ZrO$_2$, the deposition temperature of the ZnO was reduced to $250\,^\circ$C. All other conditions remained unchanged. These conditions helped to minimize the potentially confounding effect of further annealing the ZrO$_2$ during ZnO deposition due to the back gate device configuration (Figure 4.2).
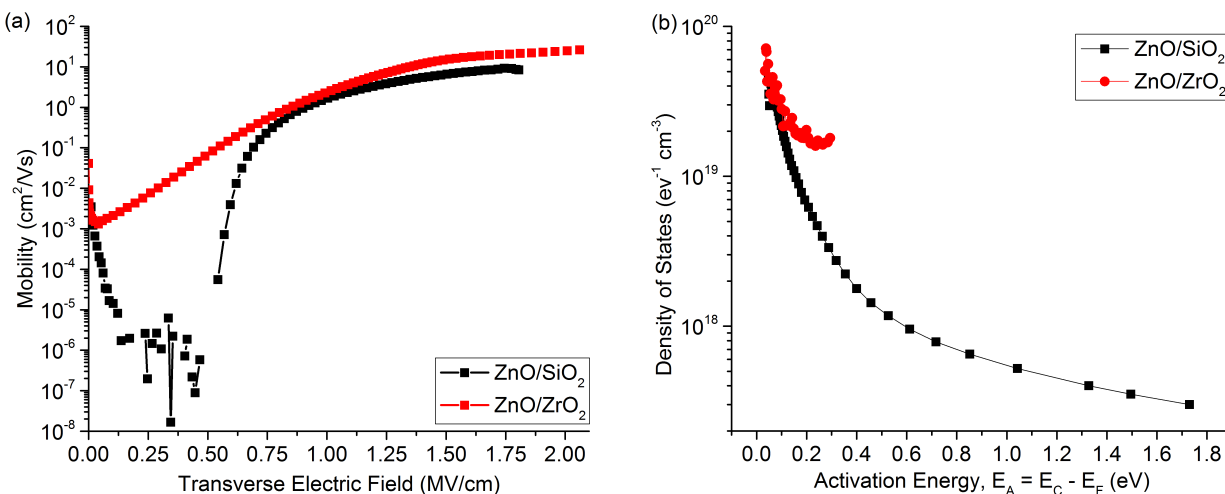
Figure 4.3: Comparison of electrical data for ZnO films deposited via spray pyrolysis onto thermally grown $SiO_2$ and $ZrO_2$ films ($700\,°C$) processed using a chemistry composed of zirconium acetylacetonate dissolved in methanol deposited at $400\,°C$. (a) Mobility as a function of transverse electric field. (b) Density of states as a function of activation energy

Surprisingly, in comparing these new devices we observe a profound improvement in transistor performance as the annealing temperature of the $ZrO_2$ is reduced (Figure 4.6).

Figures 4.6a-c shows the transfer characteristics as a function of the $ZrO_2$ processing temperature. As shown, drive current, subthreshold slope, and on/off ratio improve substantially as the $ZrO_2$ processing temperature is reduced alongside a gradual shift in the onset of conduction towards increasingly negative values. Linear mobility ranges from $1\,cm^2\,V^{-1}\,s^{-1}$ for the $500\,°C$ processed dielectrics to $20\,cm^2\,V^{-1}\,s^{-1}$ for the $300\,°C$ processed dielectrics. This is a remarkable result, given that the ZnO was deposited identically at a low temperature of $250\,°C$, which otherwise resulted in poor performance on $SiO_2$ substrates (mobility $<$ $1\,cm^2\,V^{-1}\,s^{-1}$). Figure 4.6d quantifies the shift in the transfer characteristic in terms of flatband voltage, showing the flatband voltage as a function of the $ZrO_2$ processing temperature. Interestingly, the flatband voltage transitions gradually from a positive value at $500\,°C$, where the device exhibits clockwise hysteresis and poor electrical performance, to a negative value, where the device exhibits counterclockwise hysteresis and greatly improved electrical performance. Evidently, it appears as though the $ZrO_2$ dielectric is compensating for the otherwise poor transistor switching due to the low ZnO processing temperature of $250\,°C$, potentially due to the presence of electrically charged defect(s) in the $ZrO_2$.

Figure 4.6e compares the activation energy of the drain conductance of the ZnO as a function of gate-source voltage obtained through variable temperature I-V measurements for the various $ZrO_2$ processing temperatures. As expected from the transfer characteristic observations, the activation energy is lowered with reducing $ZrO_2$ processing temperature,
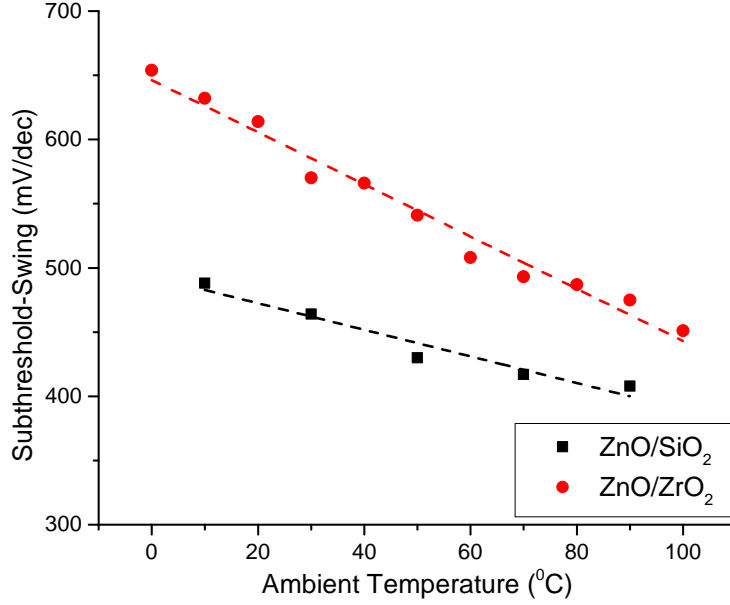
Figure 4.4: Subthreshold swing as a function of temperature for ZnO TFTs having $SiO_2$ and $ZrO_2$ dielectrics.

indicating improved electron transport. Oddly, the 300 °C and 400 °C devices show regions where the activation energy increases with gate-source voltage. This is counterintuitive, since the activation energy within the MTR model is interpreted as a measure of the Fermi energy relative to the conduction band, which, in the absence of Fermi level pinning, is expected to reduce with increasing gate-source voltage in order to accommodate the increase in electron density in the ZnO. In Figure 4.6f, we compare the mobility against the experimentally-derived induced charge obtained from integration of the quasi-static capacitance-voltage, as this provides insight into the nature of the differences in trap-limited conduction between the different devices. As shown, mobility is an increasing function of the induced charge, as is routinely encountered in these systems, and the maximum induced charge increases with reducing $ZrO_2$ processing temperature. Also, for the same induced charge, the mobility is higher for devices fabricated with lower temperature $ZrO_2$, suggesting that the mobility is trap-limited and that the reduction in $ZrO_2$ processing temperature results in a reduction in the ratio of trapped charge to total charge in the ZnO according to Street's mobility model described in the introduction section:

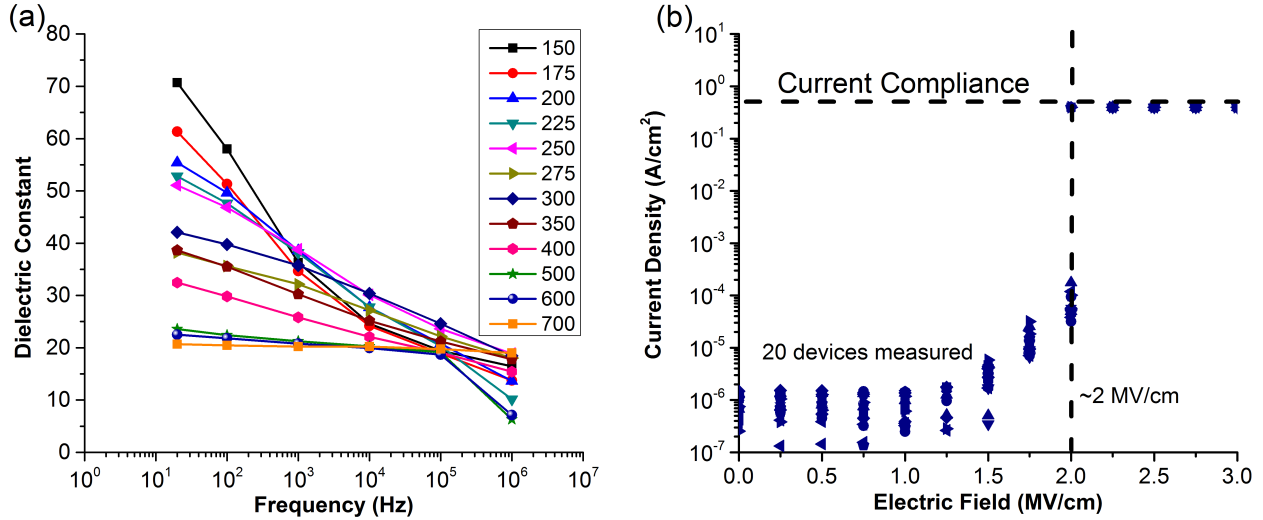$$\mu_{eff} = \left(\frac{Q_{free}}{Q_{free} + Q_{trapped}}\right)\mu_{free} \tag{4.1}$$
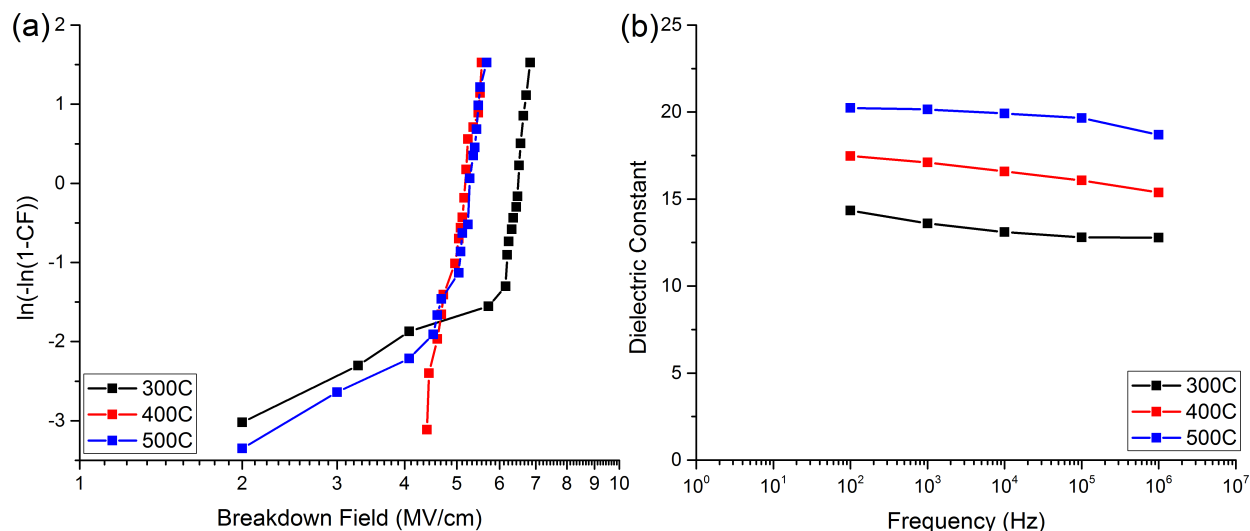
Figure 4.5: Electrical data for $ZrO_2$ thin-film capacitors (N++ Si/$ZrO_2$/Al) processed using a chemistry composed of zirconyl chloride dissolved in 2-methoxyethanol and 4 molar equivalents of $H_2O_2$. (a) Statistical (Weibull) plot of dielectric breakdown field measured for more than 20 devices each. (b) Dielectric constant of $ZrO_2$ films as a function of frequency with annealing temperature as a parameter varied from 300 °C to 500 °C.

Moreover, Figures 4.6g-i compares the drain current as a function of time for different gate-source voltage at a fixed drain voltage of 0.1 V. As shown in Figures 4.6-i, the drain current at 300 °C and 400 °C increases over time whereas at 500 °C it reduces over time. This trend appears to coincide with the observed hysteresis polarity, and can potentially be explained on the basis of electron trapping due to defects in the $ZrO_2$.

To investigate the possibility of electron trapping in the $ZrO_2$, we further investigate the nature of the counterclockwise hysteresis in the 300 °C device by identically fabricating a new device except having an additional thin layer of $SiO_2$ (3 nm confirmed by ellipsometry) inserted between the n++ Si gate and the $ZrO_2$, achieved by briefly oxidizing the silicon wafer prior to $ZrO_2$ deposition. Since the $SiO_2$ layer is very thin, the overall capacitance is largely set by the $ZrO_2$ layer (as confirmed by CV measurements); therefore, if the nature of the hysteresis is ionic (e.g. mobile charge), there should not be a significant change in device behavior. However, if the hysteresis originates from electron capture/emission from bulk traps within the $ZrO_2$, the insertion of 3 nm of $SiO_2$ should prevent electrons from tunneling in/out of the dielectric at the gate/dielectric interface. (Figure 4.7)

Upon evaluating this new device, we observe a substantial reduction of the counterclockwise hysteresis and the flatband voltage was observed to shift in the positive direction towards zero, suggesting the presence of electrons trapped in the $ZrO_2$ (Figure 4.7a). To investigate the effect this has on transport in the ZnO layer, we evaluate the mobility as a function of

transverse field. (Figure 4.7b) As shown, the maximum mobility remains approximately the same ( $20\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$) with and without the $SiO_2$ layer. Lastly, temperature-dependent I-V measurements over a range of 0-100 °C in 10 °C increments were performed on $ZrO_2$ capacitor (n++ Si/$ZrO_2$/Al) structures to further investigate the nature of the defects expected to be present. According to Figure 4.8, different temperature dependent shifts in the I-V curves were obtained as the processing temperature of the $ZrO_2$ was varied.

Evidently, as the processing temperature is reduced from 500 °C to 300 °C, there is an obvious shift in the onset of field-enhanced emission towards lower fields. Similar shifts have been observed and investigated in detail elsewhere, [40] and can be attributed to barrier lowering within the insulator due to the presence of donor-like defect states within the dielectric and is consistent with our observations. The existence of electron traps in the $ZrO_2$ is not too surprising, since these films were processed using non-ideal solution-based techniques, however, the favorable effect their presence seems to have on transport in the ZnO layer is unexpected, but consistent with transport models and previous observations.

## 4.4 Discussion

From these electrical observations, it is evident that this unexpected behavior cannot be explained by simply treating the $ZrO_2$ as an ideal insulator as is typically done in literature. On the contrary, since the mobility of the low-temperature ZnO is trap-limited, it appears that either the $ZrO_2$ improves transport by reducing the trap density in the ZnO or, alternatively, by acting as a source of donor states for the ZnO, contributing electrons to compensate for bulk traps similar to what was observed in the density of states of the ZnO/$ZrO_2$ TFTs. It is worth noting that there is some evidence of correlation between field-effect mobility and crystallinity in the high-k gate dielectric [2]. Nonetheless, we are unaware of experimental evidence in support of a mechanism by which the $ZrO_2$ can reduce the trap density in the ZnO, however, the strong negative shift in the flatband voltage with reducing $ZrO_2$ temperature (Figure 4.6d) is consistent with the $ZrO_2$ behaving as an electron donor.

We explain these observations as follows. As the transverse electric field is increased, electrons in $ZrO_2$ bulk traps begin to emit into the gate electrode in order to minimize their energy (Figure 4.9).

In general, these traps can be acceptor or donor-like, however, our data suggests that they are donor-like, since if they were acceptor-like, the TFT should exhibit enhancement mode switching due to the large positive flatband shift anticipated from a large buildup of negative charge in the $ZrO_2$. Since this is not observed, we conclude that the traps are donor-like. Therefore, as electrons inject into the gate electrode positively charged states remain, resulting in an overall negative flatband voltage shift. This claim is supported by the observation of the counterclockwise hysteresis and the observed increase in drain current over time under constant voltage stress, both of which were eliminated by inserting a thin layer (3 nm) of $SiO_2$ between the gate and the $ZrO_2$, preventing electrons from crossing the barrier imposed by the insulating $SiO_2$ layer (Figure 4.10).

Additionally, it is important to note that the hysteresis in the transfer characteristics (Figure 4.7) is reduced by altering the gate/dielectric interface, even though the semiconductor/dielectric interface is unchanged. This suggests that the observed hysteresis is not caused by carrier trapping at the semiconductor/dielectric interface since this was unchanged by insertion of the $SiO_2$. Therefore, to explain the aforementioned mobility enhancement, either the $ZrO_2$ traps must be concentrated near the gate/dielectric interface or are shallow in energy with respect to the conduction band of the ZnO so as to maintain steady-state capure/emission with respect to the free electron concentration in the ZnO - consistent with the observed reduction in hysteresis. However, the strong correlations observed between mobility, hysteresis and $ZrO_2$ processing temperature suggests a strong interaction between the defects in the $ZrO_2$ and electron transport in the ZnO. For that reason, it is unlikely that the defect concentrations are non-uniformly concentrated near the gate, since their electrostatic contribution falls off with distance.

Therefore, the emission rates of the apparent electron traps within the $ZrO_2$ should be high or comparable to capture rates in the ZnO; this can occur if they are sufficiently shallow traps. These claims are consistent with the higher shallow density of states observed in Figure 4.3, the observed mobility trends vs. accumulation charge seen in Figure 4.6f, and the reduction in activation energy as the $ZrO_2$ processing temperature is lowered as seen in Figure 4.3e. We therefore conclude that the solution processed $ZrO_2$ possesses intrinsic donor-like electron traps which inject electrons into the ZnO via a thermally-activated emissive process at rates comparable to the capture rates in the ZnO. This results in an increase in the steady-state electron concentration in the ZnO and, since transport is trap-limited, an increase in electron mobility.

The generalization of these results to other TCO/high-k dielectric interfaces is straightforward, provided they too exhibit donor-like trap states. Since, the work function of commonly used TCOs exhibiting this trend tends to be large, band diagrams for most TCO/high-k interfaces resemble that shown in Figure 4.10 and charge transfer can occur at their interface with high-k dielectrics having charge neutrality levels above the Fermi energy of the TCO. Since many high-k dielectrics have charge neutrality levels approximately near midgap [95], this should occur for a wide range of material combinations. Therefore, although the extent of which a TCO benefits from having a high-k gate dielectric likely depends on the specific defect polarity and its distribution within the dielectric, a mobility enhancement in the TCO is expected provided that some fraction of electrons trapped in the dielectric participate in the compensation of TCO bulk states during interface formation. Fortunately, in regards to this effect, electron traps are a common property of low-temperature dielectrics processed under non-ideal conditions, such as solution-processed films, which likely contributes towards the general observation across different material systems. However, this should not occur when TCO films are grown on near ideal large bandgap insulators (e.g. $SiO_2$) having relatively few electrons to contribute and deep charge neutrality levels, as is observed experimentally.

# 4.5 Conclusion

In conclusion, through detailed investigation of the electrical properties of $ZnO/ZrO_2$ thin-film transistors as a function of the annealing conditions of the $ZrO_2$, we were able to correlate specific trends in the electron field-effect mobility of the ZnO layer to electron traps in the $ZrO_2$. We posit that donor-like electron traps present in $ZrO_2$ are aligned at shallow energies with respect to the transport band of the ZnO such that, due to the higher density of states near the transport band, emission rates are higher, enabling a higher steady-state carrier concentration in the transport band of the ZnO and a higher electron mobility. Based on observations made in the $ZnO/ZrO_2$ system, we generalize our understanding to other solution-processed TCO/high-k interfaces, which, for the first time, provides clear experimentally-derived evidence in support of a theory by which solution-processed high-k gate dielectrics enhance the mobility of transparent conductive oxide thin-film transistors. Our findings suggest new directions in device fabrication that intentionally incorporate these effects such as the use of layered dielectrics composed of an electron donating layer for TCO bulk trap compensation and an insulating layer for hysteresis and leakage prevention. This new understanding is of potentially widespread utility, since it provides a clear method of circumventing the existing tradeoff between TCO processing temperature and performance of contemporary interest for flexible, solution-processed, TCO based switchable logic technology.

# 4.6 Experimental Methods

## Zirconium Dioxide (ZrO₂) Precursor Solutions

$ZrO_2$ precursor solutions consisted either of zirconium acetylacetonate ($0.1\,\mathrm{mol\,L^{-1}}$) dissolved in methanol ($10\,\mathrm{mL}$) or zirconyl chloride ($0.2\,\mathrm{mol\,L^{-1}}$) dissolved in 2-methoxyethanol ($10\,\mathrm{mL}$) and hydrogen peroxide (4 molar equivalents with respect to Zr). The specific use of either solution is specified in the text where appropriate.

## Zirconium Dioxide (ZrO₂) Thin-Film Preparation

All precursor solutions were spin-coated in air (3000 rpm, 500 rpm/sec for 36 s) onto heavily doped n++ silicon substrates. As-spun films were dried ($150\,^{\circ}\mathrm{C}$, $10\,\mathrm{min}$) on a hotplate in air before annealing in a tube furnace in air at various temperatures ($300\,^{\circ}\mathrm{C}$ âĂŞ $500\,^{\circ}\mathrm{C}$, $2\,\mathrm{h}$ or $700\,^{\circ}\mathrm{C}$, $1\,\mathrm{h}$) where appropriate.

## Zinc Oxide (ZnO) Precursor Solution

The ZnO precursor solution consisted of zinc acetate ($0.01\,\mathrm{mol\,L^{-1}}$) dissolved in methanol ($100\,\mathrm{mL}$).

## Zinc Oxide (ZnO) Thin-Film Preparation

Semiconducting zinc oxide (ZnO) thin-films were prepared using a spray pyrolysis technique. The precursor solution was sprayed ($2\,\mathrm{mL\,min^{-1}}$) onto heated $ZrO_2/n++$ Si or $SiO_2/n++$ Si substrates at a stationary fixed nozzle-to-substrate distance (14 in.) using compressed air (20 psi).

## Metallization and Lithography

Aluminum (100 nm thick) was thermally evaporated (1-2 microTorr) to serve as source/drain electrodes. ZnO was patterned using standard I-line photolithography and etched in aqueous hydrochloric acid (1:500 HCl:$H_2O$).

## Electrical Characterization

Long channel devices (channel length/width $=$ $200\,\mathrm{\mu m}/20\,\mathrm{\mu m}$) were measured using an HP4155C semiconductor parameter analyzer under medium integration time. All mobility measurements were performed in the linear region ($V_{DS} <= 100\,\mathrm{mV}$) according to an improved combined capacitance/conductance (C-V/G-V) technique reported elsewhere. Density of states was extracted using thermally-activated current measurements.
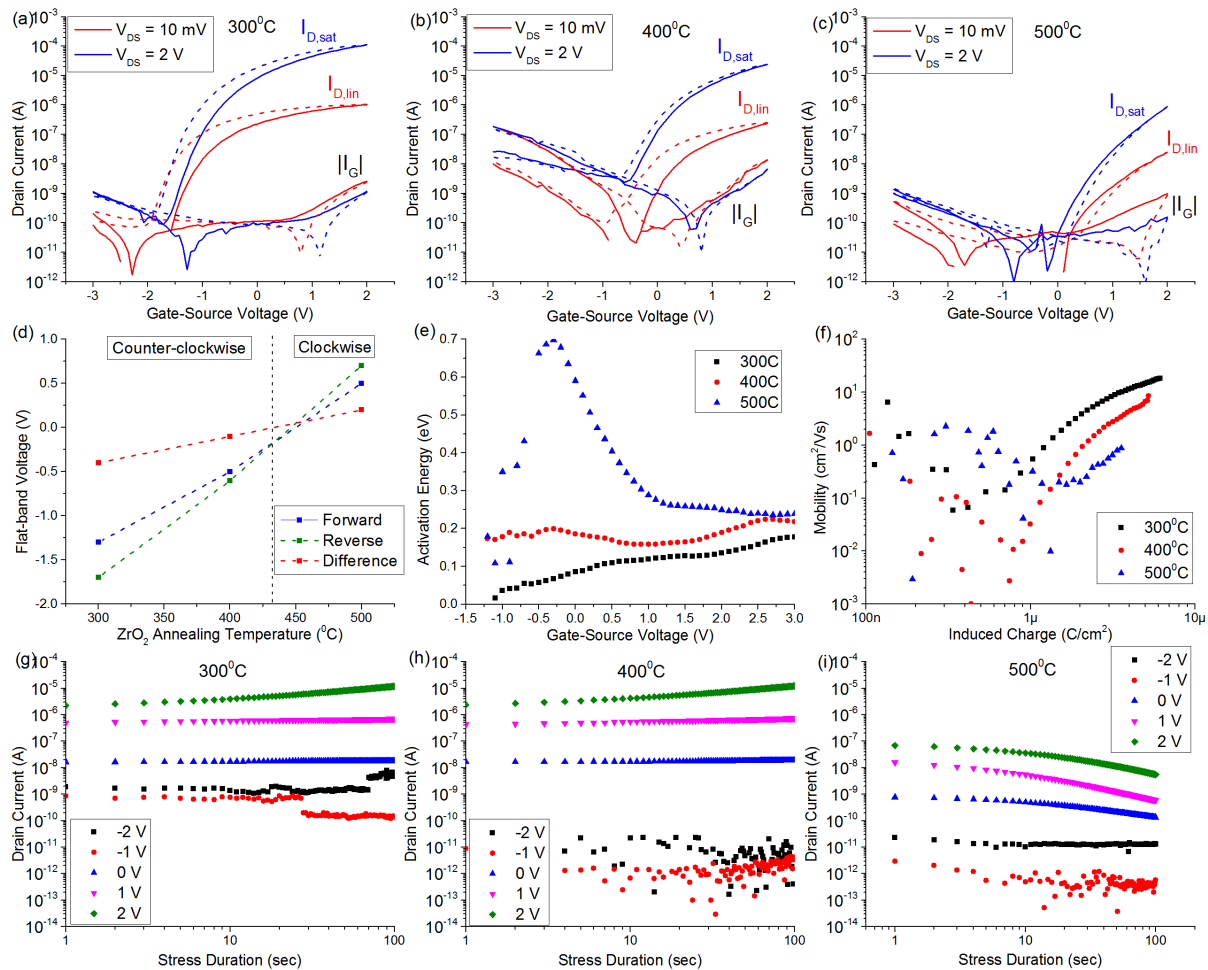
Figure 4.6: Comparison of electrical data for ZnO films deposited via spray pyrolysis at 250 °C onto spin-coated $ZrO_2$ films annealed at various temperatures (300 °C to 500 °C) processed using a chemistry composed of zirconyl chloride dissolved in 2-methoxyethanol and hydrogen peroxide. (a) - (c) Drain current as a function of gate voltage. (d) Flatband voltage versus $ZrO_2$ annealing temperature. (e) Activation energy of drain conductance as a function of gate voltage evaluated between 0-100 °C under flow of $N_2$. (f) Mobility as a function of induced charge density extracted from integration of capacitance data (not shown). (g) - (i) Drain current as a function of stress duration for different gate-source voltages.
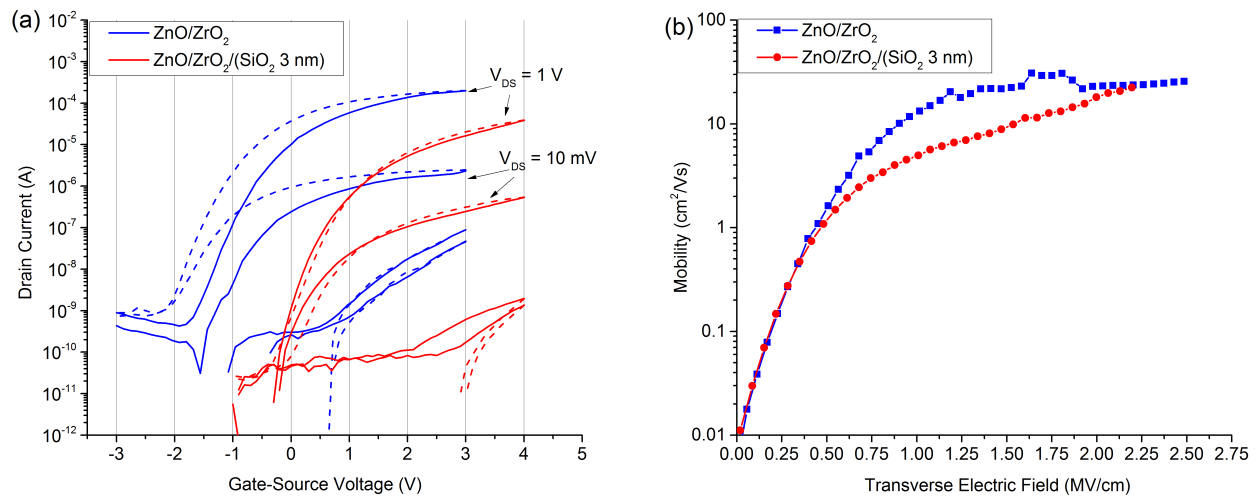
Figure 4.7: Comparison of electrical data for ZnO films deposited via spray pyrolysis at 250 °C onto spin-coated $ZrO_2$ films annealed at 300 °C with and without a thin electron blocking layer of $SiO_2$ (3 nm). (a) Drain current versus gate-source voltage. (b) Mobility versus transverse electric field.
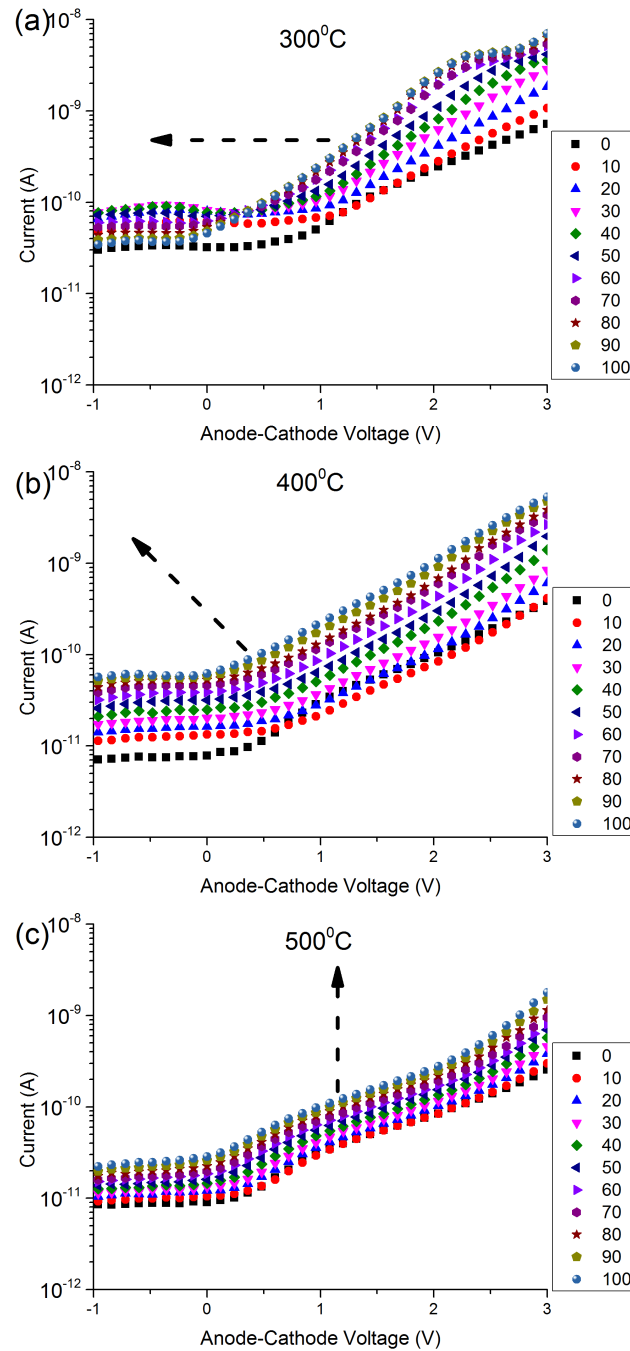
Figure 4.8: Temperature dependent current-voltage (0 - 100 °C) for ZrO$_2$ MIMs processed using low-temperature zirconyl chloride process, annealed at different temperatures as indicated. (a) 300 °C annealing temperature, (b) 400 °C annealing temperature, (c) 500 °C annealing temperature.
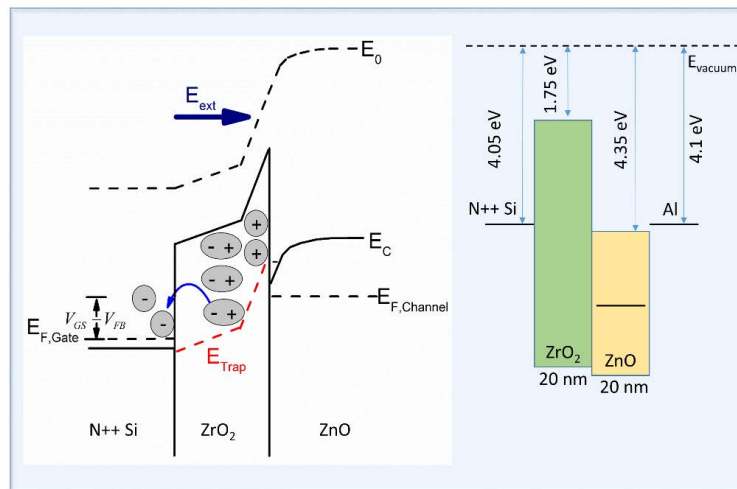
Figure 4.9: Illustration of metal-insulator-semiconductor structure depicting mechanism of electron emission into the gate electrode from donor-like $ZrO_2$ traps ($E_{TRAP}$), causing counterclockwise hysteresis and device instability as the electric field ($E_{EXT}$) is increased (left). Also indicated, the surface within the semiconductor is pinned as a result of electron exchange and dipole creation during interface formation. Band diagram before equilibrium interface formation (right).
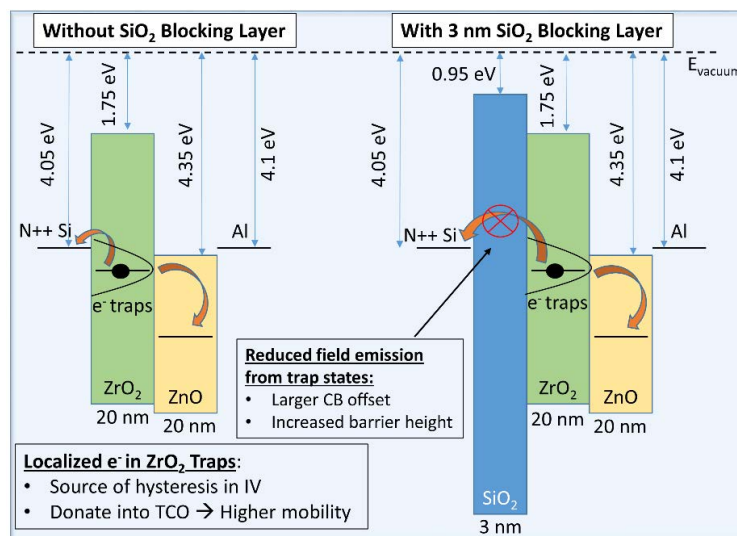


Figure 4.10: Illustration of the effect of the thin blocking layer of $SiO_2$ reducing electron injection into the gate electrode. The $SiO_2$ layer effectively prevents emission from trap states within the $ZrO_2$ which otherwise lend themselves towards counterclockwise hysteresis. The trapped electrons donate to the ZnO during interface formation, resulting in higher mobility.

# Chapter 5

# Electrostatic Simulations of TCO TFTs With Donor States in the Gate Dielectric

In the previous chapter, experimental data was provided that strongly suggested the presence of donor-like defects within the solution-processed $ZrO_2$ gate dielectric interacting with the ZnO. The presence of these states is thought to increase the steady-state electron density in the ZnO, consequently improving field-effect mobility through an increase in carrier mobility due to an increase in charge density as well as an enhancement of thermionic-emission rates from localized states. The main experimental observations are summarized as follows:

1. Higher field-effect mobility in $ZnO/ZrO_2$ (roughly 3x mobility enhancement)

2. Negative shift in flat-band voltage

3. Counter-clockwise hysteresis correlated to mobility enhancement

4. Increase in drain current over time for PBS correlated to mobility enhancement

5. Higher $ZrO_2$ dielectric constant than expected based on bulk phase

6. Higher shallow density of localized states in $ZnO/ZrO_2$

In this chapter, we explain these observations through straightforward electrostatic simulations where donor traps are introduced into $ZrO_2$. It is shown that the inclusion of donors explains the aforementioned observations, therefore providing additional evidence corroborating the claims of chapter 4 related to electron donation from $ZrO_2$.

## 5.1 Numerical Approach

Since the advent of the modern computer, numerical simulation have become increasingly important to simulate and predict the physical behavior of complex systems. Furthermore, simulations are helpful for describing and computing quantities which are not readily observable via experiment (e.g. the electrostatic potential). Numerical simulations of an appropriate physical model therefore yields valuable insight into physical behavior. In this section, the numerical methods used to gain physical insight into semiconductor/dielectric interaction are discussed.

### Finite Difference Method

Finite difference methods (FDM) provide the means of approximating the exact solution to a set of mathematical equations numerically, achieved via successive iteration or direct matrix inversion [67]. Generally speaking, exact derivatives are converted into finite differences using a grid of known spacing to define the computational space. The choice of grid spacing is based on the desired level of accuracy needed to approximate the exact differential and achieve consistency. Consistency is defined as the point when the residual (i.e. error) no longer reduces with additional reduction in grid spacing. Effectively, a smaller grid leads to a better numerical approximation of derivatives. This follows from the definition of the derivative:

$$\frac{\partial f}{\partial x} = \lim_{h \to 0} \frac{f(x+h) - f(x)}{h} \tag{5.1}$$

This is known as a **forward-difference**. For improved accuracy, the **central-difference** is typically used, since the error scales as $O(h^2)$ as opposed to $O(h)$:

$$\frac{\partial f}{\partial x} = \lim_{h \to 0} \frac{f(x+h) - f(x-h)}{2h} \tag{5.2}$$

Formulation of the problem to solve therefore consists of:

1. Describing the relevant physics to model in the form of differential equations.

2. Converting all derivatives into finite differences.

3. Specifying boundary conditions.

4. Solving via iteration or matrix-inversion until convergence is reached.

## Physical Model

The electrostatic behavior of the long-channel field-effect transistor is well approximated using a one-dimensional generalized Poisson equation for a semiconductor having a relative permittivity of $\epsilon_r$ and charge density $\rho$.:

$$\frac{\partial}{\partial x}\left(\epsilon_r \frac{\partial \phi}{\partial x}\right) = -\frac{\rho(x)}{\epsilon_0} \tag{5.3}$$

A simpler version of Poisson's equation can be used if the dielectric permittivity is uniform in each region, provided that the appropriate boundary-conditions are invoked at dielectric interfaces to preserve continuity of electric-flux and potential:

$$\frac{\partial^2 \phi}{\partial x^2} = -\frac{\rho(x)}{\epsilon_r \epsilon_0} \tag{5.4}$$

The charge density, $\rho$ is expressed as usual for a semiconductor having free electrons, holes, ionized donors and acceptors:

$$\rho = e(p + N_D^+ - N_A^- - n) \tag{5.5}$$

The free electron and holes are expressed as:

$$n = \int_{E_C}^{\infty} g_{3D}(E)f(E))dE \tag{5.6}$$

$$p = \int_{-\infty}^{E_V} g_{3D}(E)(1 - f(E))dE \tag{5.7}$$

Here, $g_{3D}$ represent the density of states for a bulk semiconductor in three-dimensions, expressed as a function of the effective conduction band density of states $N_c$:

$$g_{3D}(E) = \frac{N_c}{(k_B T)^{\frac{3}{2}}}\sqrt{E - E_C} \tag{5.8}$$

The ionized donors acceptors are expressed as:

$$N_D^+ = \int_{E_V}^{E_C} g_D(E)(1 - f(E))dE \tag{5.9}$$

$$N_A^- = \int_{E_V}^{E_C} g_A(E)f(E)dE \tag{5.10}$$

In disordered n-type semiconductors, ionized acceptors play the role of trap states:

$$n_{trap} = N_A^-$$ (5.11)

These traps have strong energy dependence and are generally approximated using two exponential functions of energy increasing towards the band edge.

$$g_A(E) = \frac{N_{tt}}{E_{tt}} e^{(\frac{E-E_C}{E_{tt}})} + \frac{N_{td}}{E_{td}} e^{(\frac{E-E_C}{E_{td}})}$$ (5.12)

This definition creates a discontinuity at the band edge. To amend this, the trap density is defined to be constant above the band edge according to [25].

$$g_A(E) = \frac{N_{tt}}{E_{tt}} e^{(\frac{E-E_C}{E_{tt}})} + \frac{N_{td}}{E_{td}} e^{(\frac{E-E_C}{E_{td}})}, E < E_C$$ (5.13)

$$g_A(E) = \frac{N_{tt}}{E_{tt}} + \frac{N_{td}}{E_{td}}, E > E_C$$ (5.14)

Furthermore, ionized donors can be neglected within the semiconductor due to the large concentrations of ionized acceptors near the conduction band edge.

$$g_D(E) \approx 0$$ (5.15)

These assumptions lead to the following expressions for the charge densities:

$$n(\eta_c) = \frac{2}{\sqrt{\pi}} N_c F_{\frac{1}{2}}(\eta_c)$$ (5.16)

$$n_{tt}(\eta_c) = N_{tt}(\frac{k_B T}{E_{tt}}) \int_{-\infty}^{0} \frac{e^{\eta(\frac{k_B T}{E_{tt}})}}{1 + e^{\eta - \eta_c}} d\eta + N_{tt}(\frac{k_B T}{E_{tt}}) F_0(\eta_c)$$ (5.17)

$$n_{td}(\eta_c) = N_{td}(\frac{k_B T}{E_{td}}) \int_{-\infty}^{0} \frac{e^{\eta(\frac{k_B T}{E_{td}})}}{1 + e^{\eta - \eta_c}} d\eta + N_{td}(\frac{k_B T}{E_{td}}) F_0(\eta_c)$$ (5.18)

$$\eta_c(x) \equiv \frac{E_F - E_C(x)}{k_B T} = \frac{q\phi(x) - q\phi(bulk)}{k_B T}$$ (5.19)

$$e\phi(x) \equiv E_C(N) - E_C(x)$$ (5.20)

$$e\phi(bulk) \equiv E_C(N) - E_F(N)$$ (5.21)

From these volumetric charge densities, the sheet charge densities can be calculated, which are relevant for calculating electrostatic capacitances.

$$Q_{free} = -e \int_0^{t_{film}} n(x)dx \tag{5.22}$$

$$Q_{tail} = -e \int_0^{t_{film}} n_{tt}(x)dx \tag{5.23}$$

$$Q_{deep} = -e \int_0^{t_{film}} n_{td}(x)dx \tag{5.24}$$

$$Q_{total} = Q_{free} + Q_{tail} + Q_{deep} \tag{5.25}$$

Within the gradual channel approximation, the channel current is exclusively due to drift. For small $V_{DS}$, assuming only electrons in states above the conduction band contribute to current (i.e. trap-limited conduction; MTR), the current is simply:

$$I_D = \frac{W}{L}eV_{DS} \int_0^{t_{film}} \Big(\mu(n_{tt}(E > E_c) + n_{td}(E > E_c)) + \mu_n n\Big)dx \tag{5.26}$$

Where $W$ and $L$ are the channel width and length respectively, $t_{film}$ is the semiconductor film thickness and $\mu$ is the electron mobility, defined as the band mobility weighted by the fractional concentration of free charge to total charge:

$$\mu(x) = \Big(\frac{n(x)}{n_{total}(x)}\Big)\mu_n \tag{5.27}$$

$$n_{total} \equiv n + n_{tt} + n_{td} \tag{5.28}$$

The relevant electrostatic capacitances are defined, based on the sheet-charge densities, as:

$$C_G = \frac{\partial Q_{total}}{\partial V_{GS}} \tag{5.29}$$

$$C_S = \frac{\partial Q_{total}}{\partial \phi_s} = C_{free} + C_{tail} + C_{deep} \tag{5.30}$$

$$C_{free} = \frac{\partial Q_{free}}{\partial \phi_s} \tag{5.31}$$

$$C_{free} = \frac{\partial Q_{tail}}{\partial \phi_s} \tag{5.32}$$

$$C_{free} = \frac{\partial Q_{deep}}{\partial \phi_s} \tag{5.33}$$

$$\tag{5.34}$$

Field-effect mobility is defined in the usual way from the calculated drain current:

$$\mu_{FET} = \frac{G_M}{\frac{W}{L}V_{DS}C_G} \tag{5.35}$$

## Discretization of Poisson's Equation

The exact form of Poisson's equation in one-dimension is given by:

$$\frac{\partial^2 \phi}{\partial x^2} = -\frac{\rho(x)}{\epsilon_r \epsilon_0} \tag{5.36}$$

Using a grid of uniform spacing, $h$, Poisson's equation is often discretized using the central-difference approximation for the second-derivative:

$$\frac{\phi(i+1) - 2\phi(i) + \phi(i-1)}{h^2} = -\frac{\rho(i)}{\epsilon_r(i)\epsilon_0} \tag{5.37}$$

For a one-dimensional simulation domain consisting of $N$ grid-points, the problem can be re-formulated using matrix algebra:

$$Ax = b \tag{5.38}$$

$A$ is an N by N matrix describing the difference operator, while x and b are N by 1 column vectors describing the electrostatic potential and the charge density respectively. This equation can be solved iteratively using the Newton-Raphson technique.

## Boundary Conditions

The boundary conditions used for solving Poisson's equation are either fixed (Dirichlet) or derivative (Neumann) based. Dirichlet boundaries were used wherever contacts were present (i.e. source, drain, gate). For semiconductor free-surfaces (i.e. no contacts), the derivative of the potential is set to zero at the edge of the semiconductor surface to ensure that the electric field goes to zero.

$$\phi(N) = \phi(N-1) \tag{5.39}$$

The electric flux at the interface between two insulating media is continuous in the absence of fixed charge. Therefore a Neumann boundary was imposed at the dielectric-semiconductor interface:

$$\epsilon_d \frac{\partial \phi(0^-)}{\partial x} = \epsilon_s \frac{\partial \phi(0^+)}{\partial x} \tag{5.40}$$

Additionally, the electrostatic potential must be continuous at interfaces. Therefore, the potential was equated at both sides of the metal-dielectric and dielectric-semiconductor interfaces.

## 5.2 Validation of Model: General MTR Behavior

In Chapter 3, general trends were established regarding how defect-electrostatics affect field-effect mobility. As a result, the shape of the density of localized states was found to have a strong effect on the field-effect mobility. It was found that increasing the concentration of localized states at the band edge resulted in an abrupt decrease in field-effect mobility. Additionally, increasing the band tail slope resulted in a gradual increase in mobility (Figure 3.5, page 46). Notwithstanding, the density of states were extracted from the activation energy of mobility (Figure 3.3, page 42), therefore indicating that transport is thermally-activated, unlike well-ordered semiconductors. These observations are all consistent with the broad classification of trap-limited conduction occuring in disordered systems and consistent with the multiple-trap-and-release description. In this section, we validate the proposed physical model by reproducing these observations essential to the multiple-trap-and-release model of disordered semiconductors.

### Convergence and Consistency

Convergence was obtained for each simulation by defining a minimum residual of $1\,\text{nV}$. Consistency was obtained by reducing grid spacing until the drain current was invariant. Figure 5.1 shows the computed drain current and computation time as a function of grid spacing. As shown, a grid spacing of approximately $0.1\,\text{nm}$ or less provided good consistency. For good measure, a grid spacing of $0.031\,25\,\text{nm}$ was selected as a good balance between accuracy and computation time.

### Variable Band Edge Concentration

The general MTR behavior is validated on a simulation domain consisting of $20\,\text{nm}$ of $\text{SiO}_2$ and $25\,\text{nm}$ of ZnO. We begin by varying the band edge concentration of the shallow tail states from $10^{16}$ to $10^{22}$ cm$^{-3}$ and evaluated the field-effect mobility as a function of gate-source voltage (Figure 5.2(a)) and band edge concentration (Figure 5.2(b)). As shown, the mobility decreases from the band mobility ($200\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$) at negligible trap densities to a small value of $0.03\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$ at a high concentration of $10^{22}$ cm$^{-3}$. This trend is both qualitatively and quantitatively similar to what has been observed experimentally(Figure 3.5, page 46).

### Variable Band Tail Slope

Following the previous results validating trends in band edge concentration, we proceed by simulating the effects of density of states having variable band tail slopes. Based on the definition of the density of tail states,
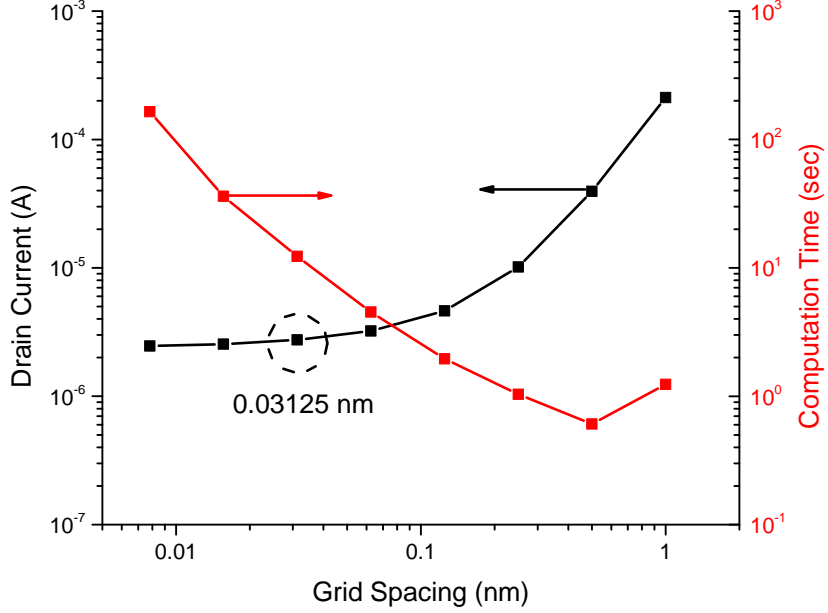
Figure 5.1: Drain current and computation time versus grid spacing. Parameters describing the localized states used in this simulation were: $N_{tt} = 100N_c$, $N_{td} = N_c$, $E_{tt} = 0.05\,\text{eV}$, $E_{td} = 0.5\,\text{eV}$. Data point corresponding to a grid spacing of $0.031\,25\,\text{nm}$ was used throughout this work.

$$g_A(E) = \frac{N_{tt}}{E_{tt}} e^{\left(\frac{E - E_C}{E_{tt}}\right)} \tag{5.41}$$

the density of states at the band edge will be $\frac{N_{tt}}{E_{tt}}$ and is a function of the band tail slope. Therefore, varying the band tail slope can be done in one of two ways by either fixing the density of states at the band edge or allowing it to vary. Simulated results indicate opposite trends with the band tail slope depending on whether or not the density of states at the band edge is fixed (Figure 5.3, page 83). For a variable DOS at the band edge, the field-effect mobility increases with increase in band tail slope. Experimentally, the mobility is found to increase gradually with an increase in band tail slope, suggesting that increasing the band tail slope reduces the band edge concentration as expected from Equation 5.41.

## Variable Temperature

The density of localized states extraction methodology (see appendix) is predicated on the experimental observation of thermally-activated mobility as opposed to band-like transport
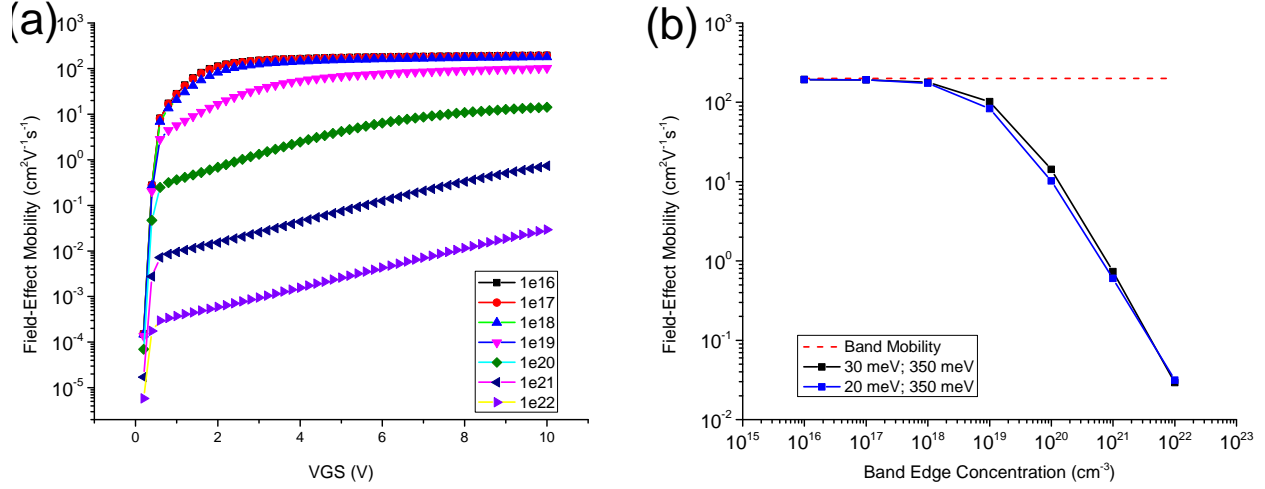
Figure 5.2: (a) Mobility versus gate-source voltage with band edge concentration as a parameter (b) Maximum mobility versus band edge concentration for two different band tail slopes.

observed in well-ordered semiconductors. In this section, we simulate the effect of temperature and evaluate the field-effect mobility for two cases: with and without traps included. The simulated results indicate that, in the absence of traps, mobility is not thermally activated above threshold whereas with traps included the mobility is thermally activated, having activation energy that reduces from a value approximately equal to the position of the Fermi level relative to the conduction band edge in bulk $(E_C - E_F)_{bulk}$ to a smaller value approaching the conduction band edge (Figure 5.4, page 84).

A direct comparison to experimental data from previous chapters is given in Figure 5.5. Figure 5.5(a) shows the experimental mobility plotted along with the simulated mobility described previously as a function of the band edge concentration. Simulated results are in good quantitative agreement to experimental results, further validating the physical model based on the MTR formalism. Furthermore, Figure 5.5(b) shows the experimental mobility plotted along with the simulated mobility as a function of the band tail slope with a variable band-edge concentration according to Equation 5.41. The model shows reasonable quantitative agreement, particularly at higher values of the band tail slope.In Chapter 3 it was argued that the strong reduction in mobility when the band tail slope falls below the thermal energy likely occurs due to an exponential increase in the number of scattering centers, expected to degrade the band mobility of thermally-excited carriers. This potentially explains the worsened quantitative agreement as the band tail slope falls below the thermal energy.
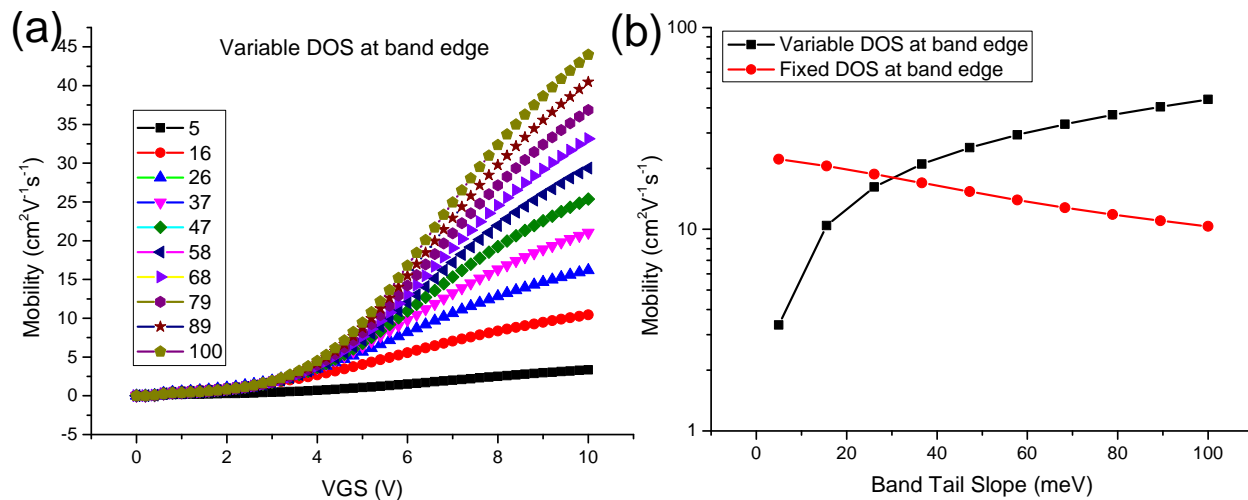
Figure 5.3: (a) Field-effect mobility plotted as a function of gate-source voltage with band tail slope as a parameter. The density of states at the band edge was allowed to vary. (b) Field-effect mobility plotted as a function of band tail slope assuming either that the total density of states at the band edge is fixed (red) or variable as defined (black).

## 5.3 Effect of Donor-Traps in ZrO$_2$ Dielectric

The physical model used in our simulation captures the essential behavior of the MTR model with regard to the trap-limited field-effect mobility. These trends are consistent with experimentally-observed behavior already noted in previous chapters and directly compared again in this chapter. In this section we move on to investigate the effect of donor-traps in the gate-dielectric and corroborate the theory of electron donation suggested in Chapter 4.

We simulate the effects of two types of donor distributions in the ZrO$_2$ dielectric: discrete and continuous. This accounts for general behavior of donor ionization in the dielectric using a simplistic description of donor levels. We evaluate the effect this has on measured current, calculated field-effect mobility and the electrostatic gate capacitance.

### Discrete Donor Level

The addition of a singly-charged discrete donor level is perhaps the most straightforward method to illustrate the general effects of donor-traps in the ZrO$_2$ due to its simplicity. To cover the full range of possibilities, the donor ionization energy was varied from the conduction band to the valence band. Taking the bandgap of ZrO$_2$ to be 6 eV, the donor ionization energy was stepped in 1 eV increments from 0 to 6 eV. The net effect this has on drain current and mobility is shown in Figure 5.6.

As the donor ionization energy is reduced, the turn-on voltage shifts increasingly nega-
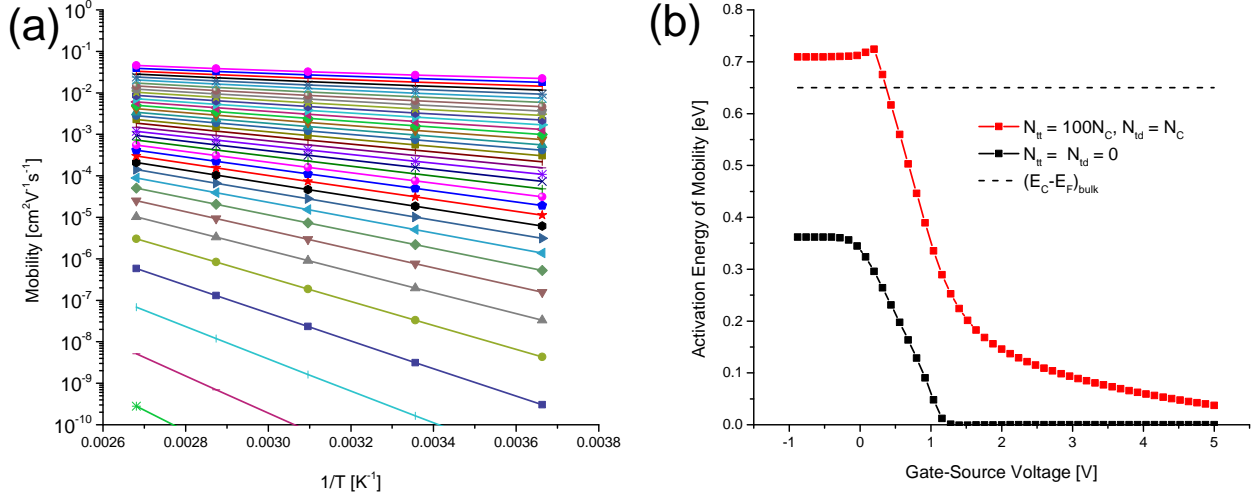
Figure 5.4: (a) Arrhenius plot of mobility as a function of inverse temperature for the case of traps included into the model ($N_{tt} = 100N_c, N_{td} = N_c$). (b) Activation energy of mobility as a function of gate-source voltage for the case of with (red) and without (black) traps ($N_{tt} = 100N_c, N_{td} = N_c$)

tive from its ideal value (i.e. the flatband voltage) indicating that the channel is becoming increasingly conductive due to the additional induced charge appearing in the semiconductor channel. This is also confirmed by a substantial increase in drain current. Additionally, the sub-threshold swing is visibly reduced as well relative to the control, suggesting an increase in gate capacitance within this range. We demonstrate this last point clearly in Figure 5.7 which shows the experimental transfer characteristics and extracted sub-threshold slope for a forward and reverse sweep of a ZnO/ZrO$_2$ TFT that has been stressed to high transverse electric fields not typically used in a normal sweep. The hysteresis window noticeably broadens due to an an increase in donor ionization caused by the high transverse fields. Note that the polarity of the hysteresis is counter clockwise, consistent with an increase in free carrier density in the semiconductor channel as confirmed by electrostatic simulation.

Figure 5.8 shows the gate capacitance for each simulated condition. As shown, the capacitance is increased sharply over a narrow voltage range, exceeding the geometrical capacitance value. Since fixed charge cannot contribute to capacitance, the additional capacitance corresponds to ionization of the donors, expected to lead to an additional change in surface potential unaccounted for by charge-sheet models. The capacitance is expected to be equal to the geometrical value once the donors within the dielectric are fully-ionized. As shown, the capacitance increases sharply as the donor ionization energy is being crossed, then gradually decreases towards the geometrical value as the gate voltage increases as expected.

To further illustrate these effects, the band diagram is shown for a discrete trap having ionization energy of 4 eV computed at different values of the gate voltage in excess of the
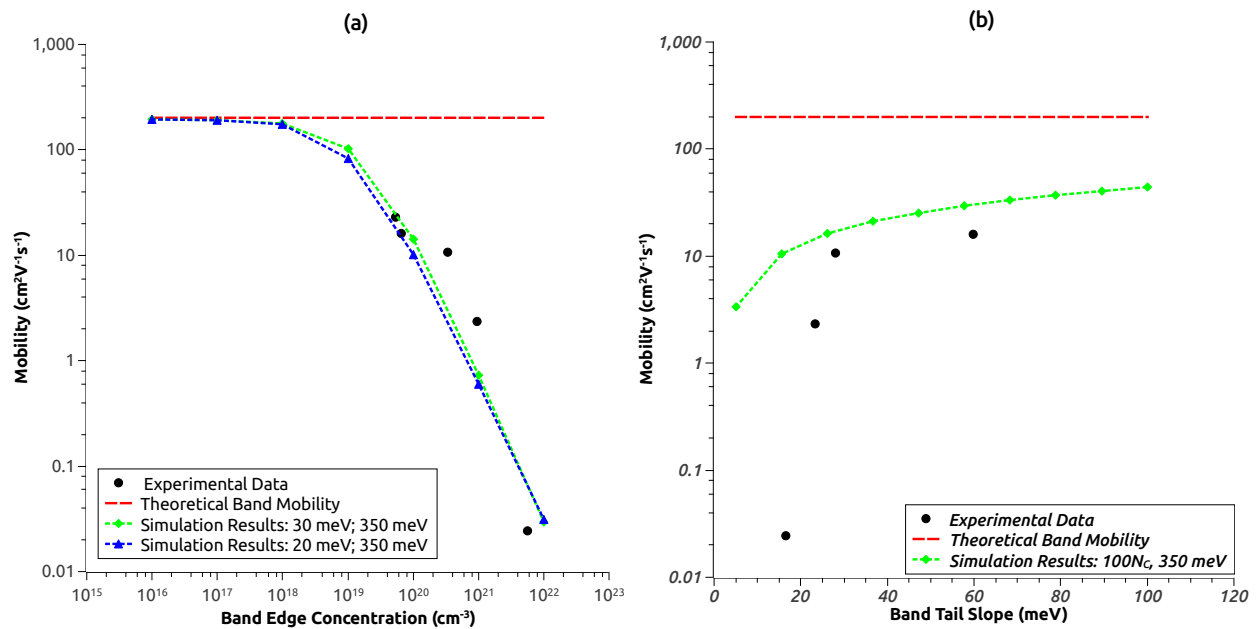
Figure 5.5: Comparison of experimental mobility and simulated mobility. (a) Maximum
mobility versus band edge concentration. (b) Maximum mobility versus band tail slope
$(N_{tt} = 100N_c, N_{td} = N_c)$

flatband voltage (Figure 5.9). As the gate voltage increases, the donor level rises above the
Fermi level leading to donor ionization and increased band bending in the dielectric due to
space charge formation.

The dielectric-semiconductor interface then operates analogously to a reverse-biased pn
junction with the dielectric functioning like the p material and the semiconductor as the n
material. Additional gate voltage creates more space charge in the dielectric, expected to
enhance the electric field at the semiconductor-dielectric interface.

The spatial distribution of the electric field is plotted for different voltages in Figure 5.10.
The electric field increases linearly from its nominal value $\frac{V_{ox}}{t_{ox}}$ from the point where the Fermi
energy crosses the donor level towards the semiconductor-dielectric interface consistent with
a relatively uniform region of ionized donors. Also, it can be seen that the peak field is
higher in the semiconductor than expected based on the ratio of the dielectric constants
$(\epsilon_{ZrO_2} = 20, \epsilon_{ZnO} = 10)$ due to the space charge build up in the dielectric. This explains the
additional charge appearing in the semiconductor leading to increased current and field-effect
mobility as well.

Additionally, the gradual decay in the capacitance can be explained due to donors ionized
increasingly farther away from the interface as the gate voltage increases. These have a
lessened effect on semiconductor capacitance since their electrostatic contribution falls off
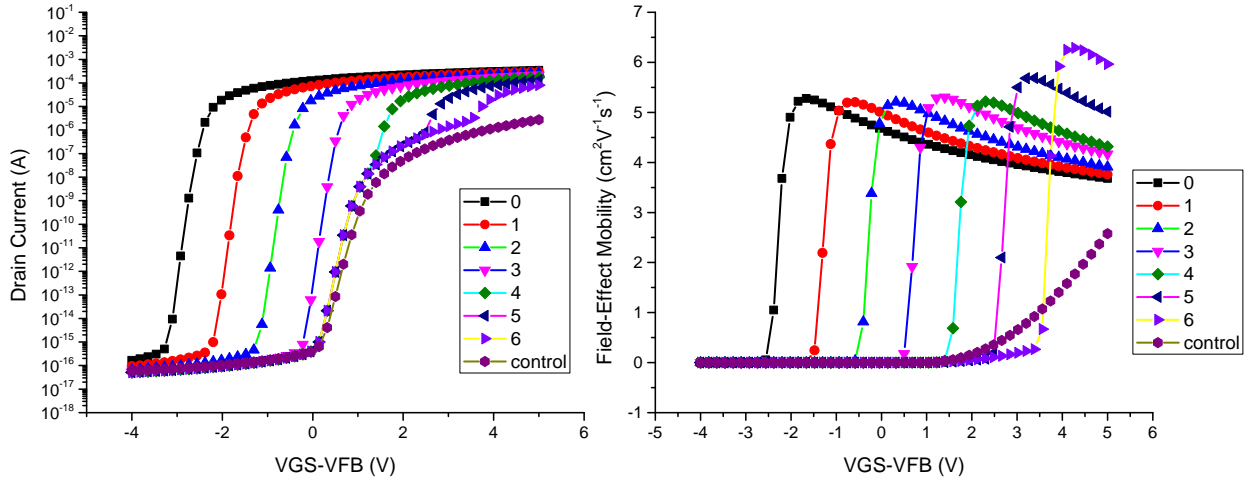
Figure 5.6: (a) Drain current and (b) field-effect mobility computed for different donor ionization energies for a spatially-uniform discrete in energy trap located in the $ZrO_2$. The donor concentration used was $10^{20}$ cm$^{-3}$

with distance. However, the sharp increase and gradual decay in capacitance is not always observed experimentally, suggesting that the actual donor profile must be different. In the next section, we investigate a more realistic continuous distribution of states of varying concentrations.

## Continuous Donor Level

Having demonstrated the general behavior of a discrete donor trap in the $ZrO_2$, we now simulate a continuous distribution of traps. Intuitively, this is expected to more closely resemble the actual defects present within the dielectric, since a monoenergetic trap level is physically inconsistent with the aperiodic electronic environment of a disordered solid. Like solution-processed TCOs, solution-processed dielectrics are also prone to higher defect concentrations that may perturb the energy levels of defects expected based on defect calculations for single crystalline dielectrics leading to broadened defect distributions.

The drain current and field-effect mobility are shown in Figure 5.11 as a function of gate-source voltage for a continuous distribution of donor traps having a variety of concentrations varied from $10^{17}$ cm$^{-3}$ eV$^{-1}$ to $10^{20}$ cm$^{-3}$ eV$^{-1}$. The flat-band voltage shifts negative similarly to what was observed in the case of a discrete donor level. However, the increase in drain current is much more pronounced. The mobility increase is also more pronounced and the gate voltage dependence more gradual due to the gradual ionization of donors with each increase in gate-voltage.

Figure 5.12 shows the gate capacitance for each simulated condition. Unlike the case of a discrete donor, for a continuous donor the gate capacitance exceeds the geometrical value
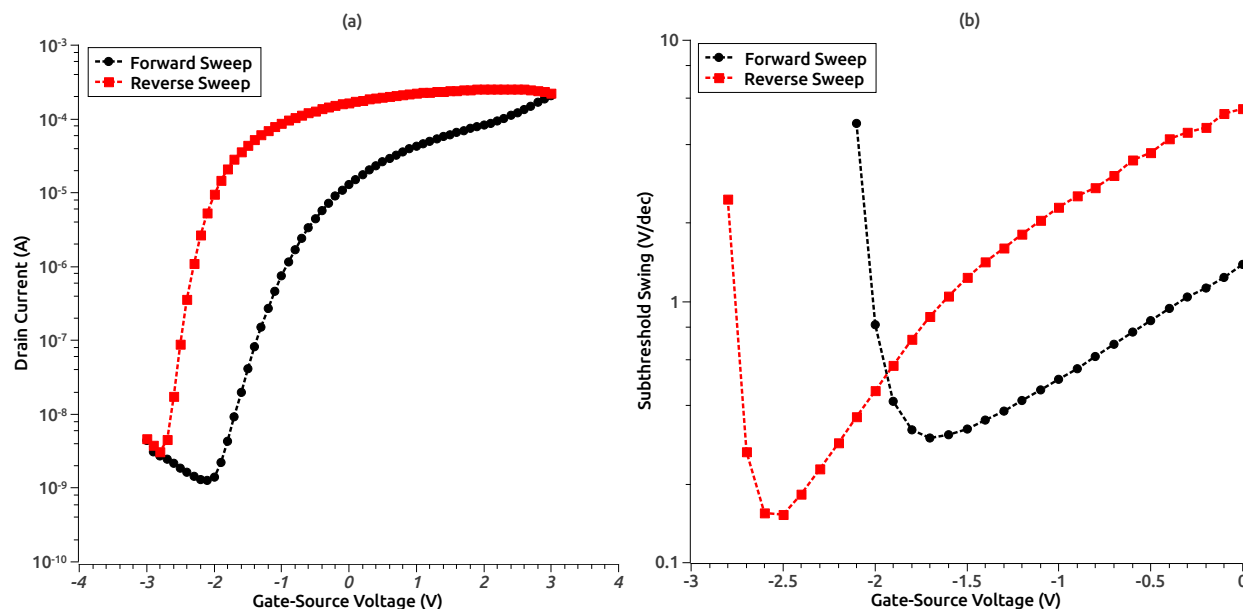
Figure 5.7: (a) Transfer characteristic and (b) sub-threshold swing for a stressed $ZnO/ZrO_2$ TFT in order to illustrate donor-trap behavior. A reduction in the sub-threshold swing on the reverse sweep due to donor ionization is clearly shown.

over a large range. This CV trace resembles experimental data, except with a higher capacitance than expected based on the geometrical value and a more negative flat-band voltage. The higher capacitance explains earlier measurements of dielectric constants exceeding the expected bulk value(Figure 4.1). This occurs also due to the gradual ionization of donors which occurs at every increment of the gate voltage and therefore creates an effective increase in the oxide capacitance similar to that observed for a discrete trap.

We illustrate the effects of donor defects in the $ZrO_2$ more clearly by showing experimental capacitance trends in Figure 5.13. Figure 5.13(a) shows that the forward sweep of a $ZnO/ZrO_2$ TFT connected in a MOSCAP configuration (i.e. source/drain shorted). Additionally, Figure 5.13(b) shows the reverse sweep for the same configuration. In both cases, as the temperature is increased, the capacitance increases and the flat-band voltage shifts towards negative voltages. This can be explained on the basis of an increase in donor ionization within the $ZrO_2$ as confirmed via simulation. Interestingly, the maximum capacitance on the forward sweep does not show a strong gate-voltage dependence except at higher temperatures and is more consistent with a continuous trap distribution. By contrast, the capacitance for the reverse sweep shows a stronger gate-voltage dependence that becomes more pronounced with increasing temperature resembling the behavior of a discrete trap at higher temperatures. Since both increased electric field and temperature can ionize donors
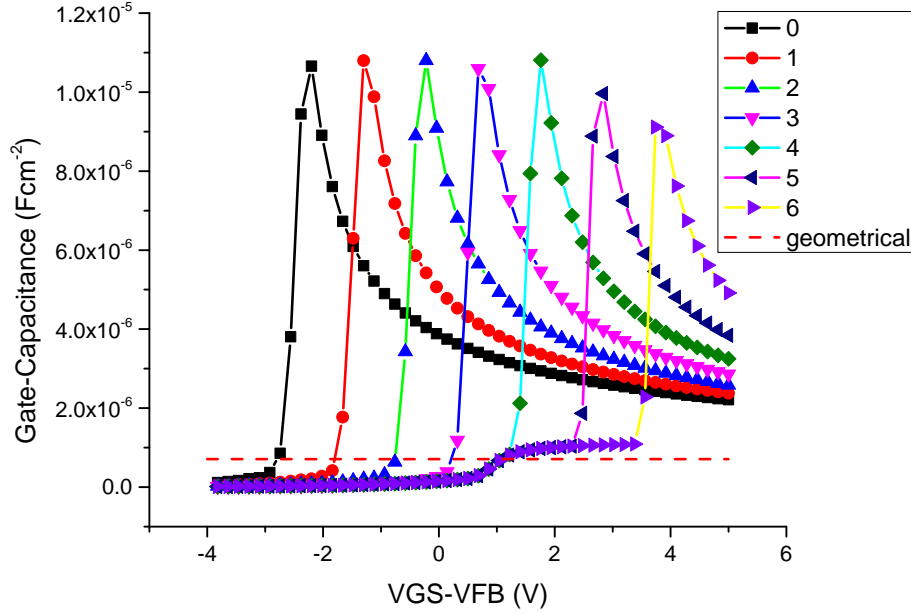
Figure 5.8: Gate capacitance for different donor ionization energies for a spatially-uniform discrete in energy trap located in the $ZrO_2$. The donor concentration used was $10^{20}$ cm$^{-3}$

in the $ZrO_2$, it is likely that a deep state becomes ionized on the forward sweep once the field exceeds a critical value and shows up more pronounced on the reverse sweep. Nonetheless, both cases are fully-consistent with the simple electrostatic simulations.

## 5.4   Summary and Conclusion

From these simple simulations it is clear that the presence of donors in the $ZrO_2$ can lead to a higher field-effect mobility in the ZnO. The comparison of a discrete and continuous energy distributions indicate that although any donor ionization processes can enhance the field-effect mobility in the ZnO, a broader energy distribution leads to a much higher increase in field-effect mobility. Intuitively, this makes sense, since it was shown that in the case of a discrete trap, the crossing of the Fermi energy with the donor level leads to a decreasing electrostatic contribution with distance. By contrast, continuous traps act near the semiconductor-dielectric interface, and have a greater electrostatic contribution. Furthermore, electrons emitting from these states that are not captured by the gate electrode can easily hop into and fill deep states in the semiconductor, effectively modifying the density of states. This last point is consistent with the experimental observation of an apparent modification of the density of states in the ZnO as compared to identically processed ZnO films
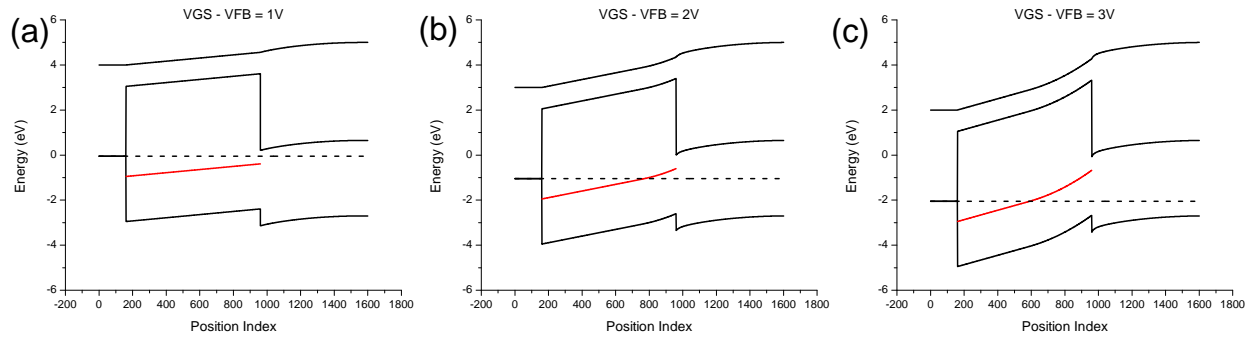
Figure 5.9: Energy band diagram indicating donor level (red) relative to bands (black) at different voltages (a) $V_{GS} - V_{FB} = 1V$, (b) $V_{GS} - V_{FB} = 2V$ and (c) $V_{GS} - V_{FB} = 3V$. The donor ionization energy and concentration was set to $4\,\text{eV}$ and $10^{19}$ cm$^{-3}$ respectively.

deposited onto thermally-grown SiO$_2$. These simulations provide further evidence supporting the theory of electron-donation from high-k dielectrics leading to mobility enhancement in the TCO.
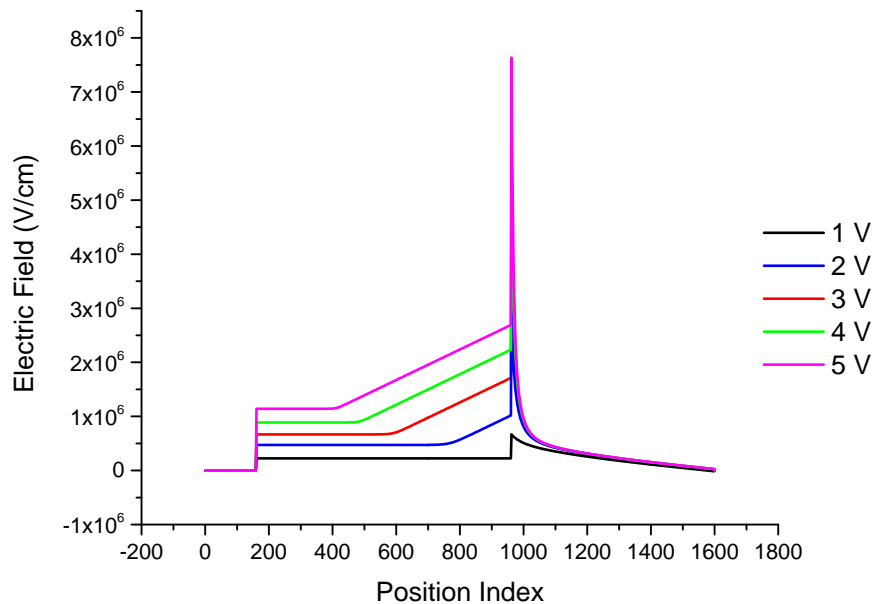
Figure 5.10: Electric field for different voltages. The donor ionization energy and concentration was set to $4\,\text{eV}$ and $10^{19}$ cm$^{-3}$ respectively.
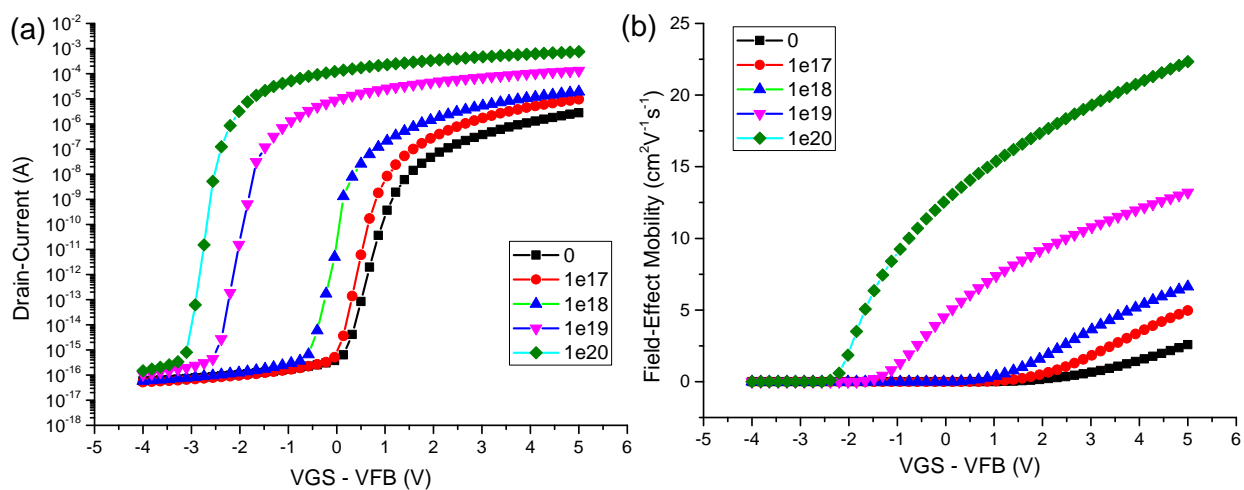


Figure 5.11: (a) Drain current and (b) field-effect mobility computed for different donor concentrations ($10^{17}$ cm$^{-3}$ eV$^{-1}$ to $10^{20}$ cm$^{-3}$ eV$^{-1}$) for a spatially-uniform continuous in energy trap located in the ZrO$_2$.
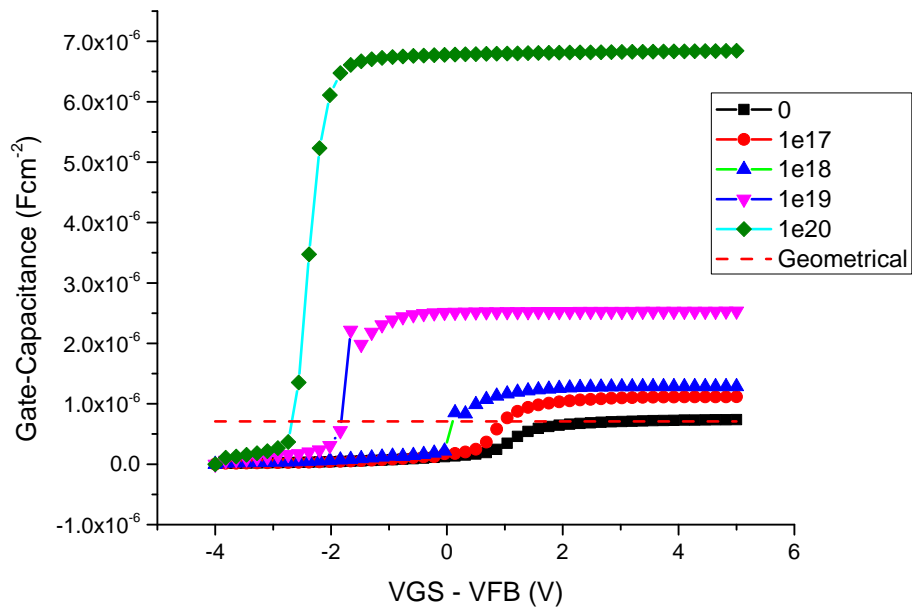
Figure 5.12: Gate capacitance for different donor concentrations ($10^{17}$ cm$^{-3}$ eV$^{-1}$ to $10^{20}$ cm$^{-3}$ eV$^{-1}$) for a spatially-uniform continuous in energy trap located in the ZrO$_2$.
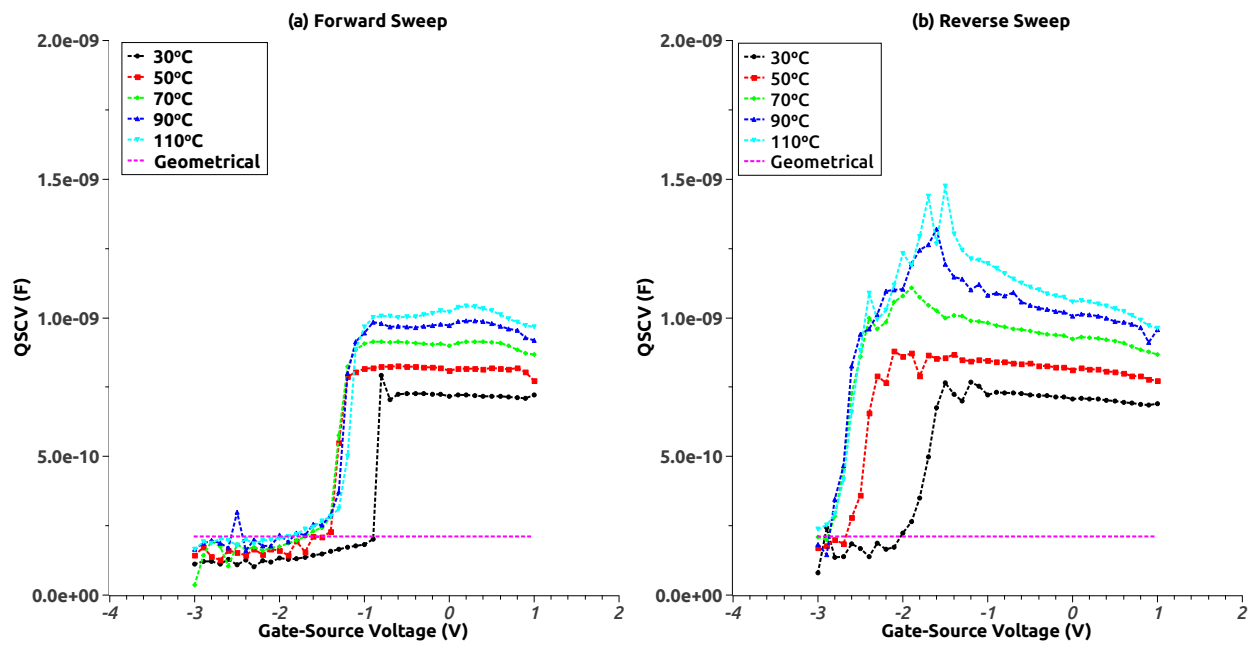
Figure 5.13: Measured quasi-static capacitance in the (a) forward direction and (b) reverse
direction as a function of temperature for a $ZnO/ZrO_2$ TFT.

# Chapter 6

# Modulation Doping of TCO Channel by High-k Dielectric Encapsulation

In chapters 4 and 5, it was shown experimentally and through electrostatic simulations that donor-like traps within the high-k dielectric effectively dope the semiconductor channel leading to higher field-effect mobility. The presence of defects in a gate dielectric is an unintentional and undesirable property due to increased leakage currents, hysteresis and instability under voltage stress. Based on the understanding derived in the previous chapters, in this chapter, we demonstrate an alternative route to maintain high field-effect mobility while mitigating hysteresis, leakage and instability associated with defects in the gate dielectric.

## 6.1 Background and Motivation

Device instabilities associated with defects in gate dielectrics (e.g. hysteresis and gate-leakage) originate because charged defects within the dielectric *feel* the transverse electric field applied to the gate. This results in defect migration, electron capture/emission processes and trap-assisted leakage currents giving rise to hysteresis and gate-leakage.

In this chapter it will be shown that placing the high-k layer on top of the semiconductor (effectively encapsulating the semiconductor) results in the familiar electron donation and mobility enhancement except without the negative drawbacks associated with gate-dielectric defects. This is achieved due to the fact that the transverse electric field *seen* by dielectric defects is screened by electrons in the semiconductor channel, resulting in a reduced electrostatic contribution from defects in the high-k layer. This technique can be compared qualitatively to modulation doping (Figure 6.1) with the key difference that, in this case, injected electrons improve transport by enhancing emission rates from localized states rather than physically separating donors from free electrons.

To illustrate the concept, we use a system consisting of a ZnO semiconductor and $Ga_2O_3$ high-k dielectric encapsulate. $Ga_2O_3$ was selected as opposed to $ZrO_2$ for the encapsulate due to the tendency of the $ZrO_2$ sol-gel solutions used to deposit the $ZrO_2$ to etch the underlying

## (a) Uniform Doping  (b) Modulation Doping
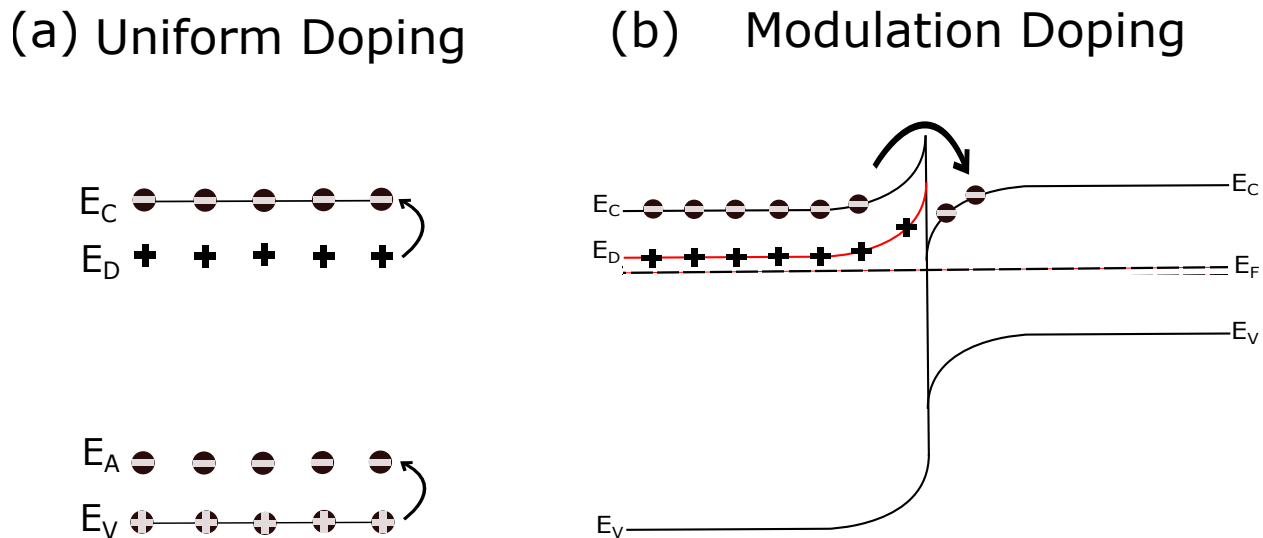


Figure 6.1: Illustration showing the distinction between traditional (uniform doping) and modulation doping

ZnO film. This substitution is justified experimentally by the rather ubiquitous mobility enhancement observed over a wide range of high-k dielectrics owing to strong tendency of solution-processed dielectrics to exhibit defects as well as the similarity in bandgaps between $ZrO_2$ and $Ga_2O_3$.

In practical terms, most importantly, we show that by using this technique, device stability is improved, as indicated by the elimination of leakage current, hysteresis and improved bias stress stability. This attests to the ubiquity of the effective doping theory as well as provides a more robust practical method of obtaining higher mobility.

## 6.2 Thin-Film Characterization of ZnO and $Ga_2O_3$/ZnO Heterostructures

### Hall Mobility of ZnO and $Ga_2O_3$/ZnO Hetereostructures

Since $Ga_2O_3$ is exceedingly more insulating than ZnO due to bandgap differences, the most straightforward indication of modulation doping of ZnO by $Ga_2O_3$ encapsulation is through observation of increased hall mobility of ZnO/$Ga_2O_3$ heterostructure films relative to ZnO alone. Therefore, we begin by comparing hall mobility and electron concentration of a ZnO control film and a ZnO/$Ga_2O_3$ stack deposited onto insulating glass substrates.

Initially, we compared the hall-mobility and electron concentration for heterostructure films where both layers were deposited at the same temperature over a range of 200 °C to

500 °C. Additionally, the ZnO deposition temperature was fixed at a high value of 500 °C while the deposition temperature of the $Ga_2O_3$ was varied from 200 °C to 500 °C. As a control reference, the hall mobility of a ZnO film deposited onto glass at different temperatures is also shown. The hall mobility for the ZnO film on glass is found to increase monotonically with temperature throughout the range of temperatures investigated as is commonly observed in literature. As shown in Figure 6.2, for heterostructure films where both layers were deposited at the same temperature, the hall mobility increases abruptly as the deposition temperature is reduced in the vicinity of 300 °C. In contrast, for heterostructures where the ZnO deposition temperature was fixed at a high value of 500 °C while the deposition temperature of the $Ga_2O_3$ was varied, the hall mobility was found to stay roughly constant at a low value of approximately $5\,cm^2\,V^{-1}\,s^{-1}$.

Since more defects are present in the ZnO as the deposition temperature is lowered, this suggests that the electron donation mechanism is particularly beneficial for enhancing the mobility of poor quality semiconductors. Low temperature ZnO has a higher concentration of traps than high temperature processed ZnO. Therefore, additional electrons help to screen the charge from trapped electrons, increasing the electron mobility (weak screening limit). As the quality of the ZnO is improved, increasing the concentration of free electrons relative to trapped electrons, additional electrons supplied by the $Ga_2O_3$ lead to electron-electron interactions, and a reduction in mobility as is observed (strong screening limit).

Despite fabricating films below 300 °C, not all films yielded a measurable hall mobility, preventing investigation at low-temperatures. To further investigate the behavior of the heterostructure at low temperatures, we deposited films within a narrower and finer temperature range from 200 °C to 300 °C in the vicinity of the sharp increase of Hall mobility and measured the work function of these films.

## Work Function of ZnO and $Ga_2O_3$

The difference in chemical potential between the ZnO and $Ga_2O_3$ films is used to predict the direction of electron transfer across the $ZnO/Ga_2O_3$ interface in terms of energy minimization, providing additional mechanistic evidence. Measurement of the work function of a material provides the position of the chemical potential relative to vacuum. Therefore, the work function of each material was measured to quantify the difference in chemical potential.

The work function of ZnO and $Ga_2O_3$ were measured using a Kelvin Probe technique in lab air. As shown in Figure 6.3, the work function of $Ga_2O_3$ is smaller than the work function of ZnO for a specific temperature range below 300 °C. This means that the chemical potential of $Ga_2O_3$ is higher in energy than that of the ZnO for this temperature range. Therefore, electron transfer is expected from $Ga_2O_3$ to ZnO as the system approaches thermodynamic equilibrium, resulting in an increase in the electron concentration in the ZnO and a corresponding increase in mobility due to improved screening of defects. This data is in good agreement with the previously obtained hall mobility which showed an abrupt increase for ZnO films processed at 300 °C.
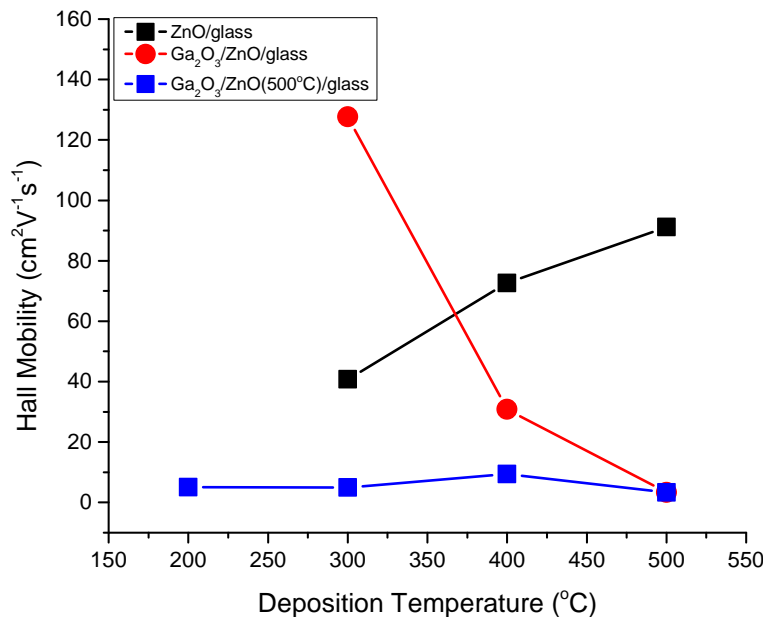
Figure 6.2: Hall mobility of ZnO and ZnO/Ga$_2$O$_3$ films as a function of temperature, obtained using a 1 T permanent magnet.

## 6.3   TFT Characterization of ZnO and ZnO/Ga$_2$O$_3$ Heterostructures

The ultimate test validating the use of high-k encapsulates to circumvent the negative drawbacks associated with defective high-k gate dielectrics is to demonstrate an improvement in field-effect mobility on a structure where the Ga$_2$O$_3$ encapsulate has been integrated. In addition to an improvement in field-effect mobility of the ZnO/Ga$_2$O$_3$ heterostructure TFT relative to the ZnO TFT, a hysteresis reduction is anticipated as well as a reduction in leakage current. These observations decouple the existing undesired tradeoff between TCO transport and instabilities associated with dielectric defects.

Inverted-coplanar TFTs were fabricated consisting of a N++ silicon gate electrode, thermally-grown SiO$_2$ gate dielectric, ZnO semiconductor and FTO (F = 5 percent) source/drain electrodes and corresponding Ga$_2$O$_3$ encapsulate processed at the aforementioned temperatures. The deposition temperature of the ZnO is fixed at 300 °C so that the thermal budget is limited by the ZnO and not the subsequently deposited Ga$_2$O$_3$. Previous transistor studies were based on inverted-staggered structures using Aluminum as the contact material. Inverted-staggered structures are not applicable in this experiment as they add additional series resistance that may confound the interpretation of TFT data and mobility extraction.
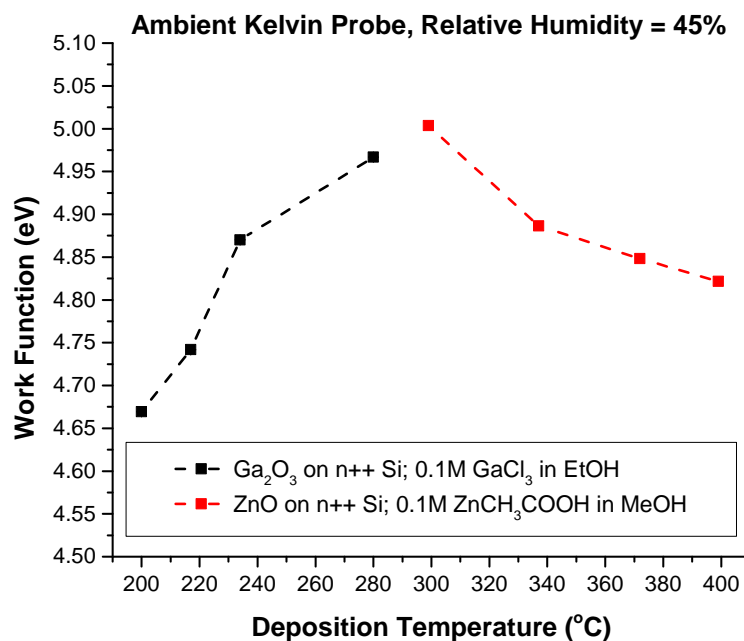
Figure 6.3: Work function of $Ga_2O_3$ and ZnO films obtained via Kelvin Probe in air at a relative humidity of 45 percent.

The drain current for the $ZnO/SiO_2$ and $Ga_2O_3/ZnO/SiO_2$ TFTs are shown in  6.4. The $ZnO/SiO_2$ device exhibits very poor switching characteristics as expected bassed on the low deposition temperatures used to deposit the ZnO thin-film. These devices also exhibit significant clockwise hysteresis in the transfer curve, indicating the presence of trapping within the ZnO or at the interface. By comparison, the $Ga_2O_3/ZnO/SiO_2$ device exhibits far superior transfer characteristics. Additionally, the hysteresis has reduced to an almost negligible value, indicating an improvement in transport as well as device stability.

To further illustrate the improvement in switching characteristics, the quasi-static capacitance is shown in figure  6.5. It can be seen that the flat-band voltage has shifted increasingly negative upon adding the $Ga_2O_3$ encapsulate. Additionally, the change in capacitance from depletion to accumulation is much more abrupt than without the encapsulate indicating an improvement in electrostatic switching.

The field effect mobility was compared in Figure 6.6. As shown, the mobility is several orders of magnitude higher in the heterostructure device than the un-encapsulated device. Additionally, the mobility is much less sensitive to temperature changes, suggesting a reduction in activation energy.

The activation energy of the field-effect mobility is plotted in Figure 6.7 as a function of gate-source voltage. The peak in activation energy occurs at the flat-band voltage and
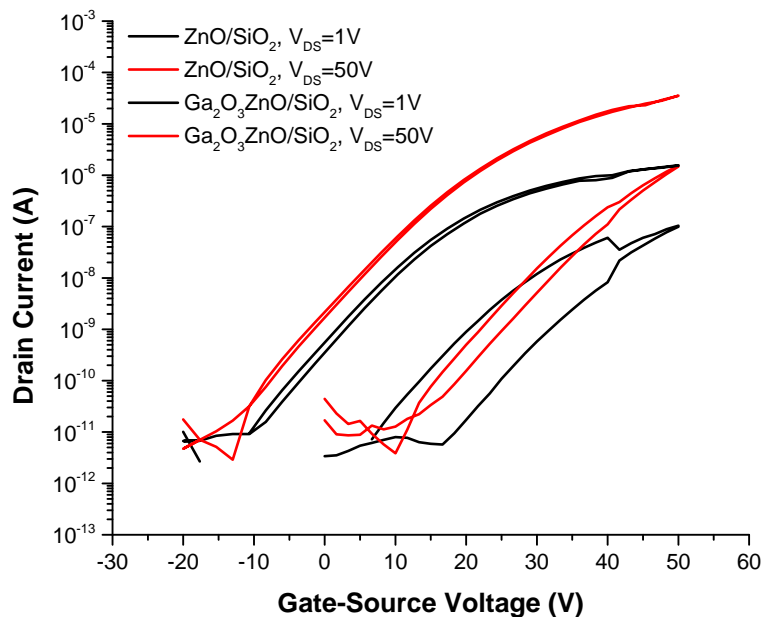
Figure 6.4: Drain current as a function of gate-source voltage for ZnO and ZnO/Ga$_2$O$_3$ TFTs.

physically corresponds to the position of the Fermi energy in the bulk of the semiconductor relative to the conduction band edge. Therefore, a smaller peak activation energy indicates that the Fermi level is closer to the conduction band edge in the heterostructure device than the un-encapsulated device. This alone indicates that there are more available free carriers in the heterostructure device and is consistent with the simple predictions based on the work function differences.

## 6.4 Conclusion

The predictions of the previous chapter regarding electron donation from high-k dielectrics were used to guide experiments of this chapter with the goal of using a high-k encapsulate to achieve modulation doping of the ZnO layer. This was achieved using an inverted-coplanar structure consisting of Ga$_2$O$_3$ encapsulate and ZnO semiconductor using SnO$_2$:F source/drain contacts. Like ZrO$_2$, Ga$_2$O$_3$ has defects. However, by virtue of the placement of the Ga$_2$O$_3$ encapsulate on top of the ZnO, the transverse electric field is screened by electrons in the semiconductor so that hysteresis does not appear in the transfer characteristics. It is because of this fact that this method of high-k encapsulation has particular utility. This was validated initially through hall mobility measurements showing an increase in hall
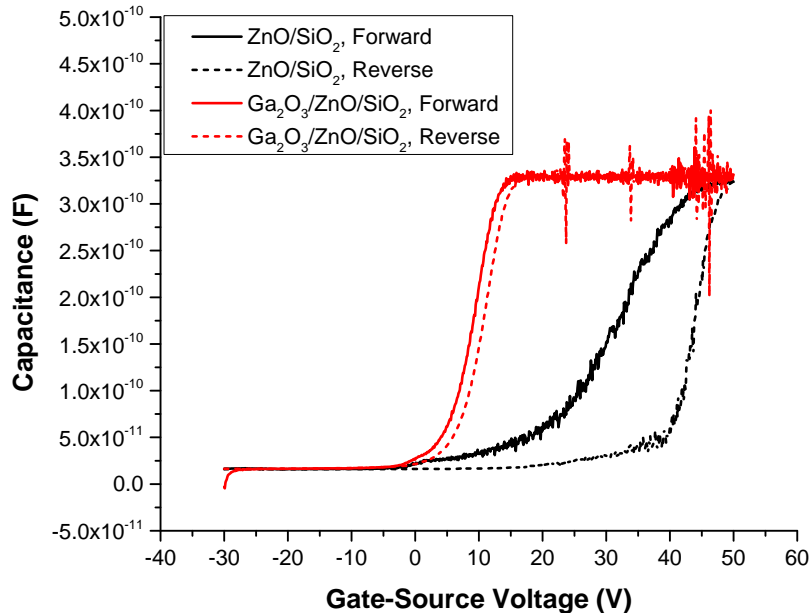
Figure 6.5: Quasi-static capacitance-voltage curves of ZnO and ZnO/Ga$_2$O$_3$ films as a function of gate-source voltage showing reduction in hysteresis and improvement in switching characteristics.

mobility via encapsulation as well as through work function measurements showing that it is energetically favorable for electrons to transfer from the Ga$_2$O$_3$ towards the ZnO. Finally, electrostatic measurements on TFTs with and without the heterostructure show increased field effect mobility, improved abrupt switching and reduced hysteresis in the transfer characteristics. Lastly, measurements of activation energy confirm an increase in carrier density as indicated by the reduction in activation energy of the encapsulated device. These observations are profound in that they provide a more practical method of exploiting the donor-like defects in high-k dielectrics without sacrificing device integrity due to hysteresis, leakage and instability.

## 6.5 Experimental Methods

### Film Preparation

ZnO films were prepared by spray-pyrolysis from solutions of zinc acetate dissolved in methanol to a concentration of 0.1M. The substrate temperature during deposition was maintained at a constant measured temperature of 300 °C or varied where specified depend-
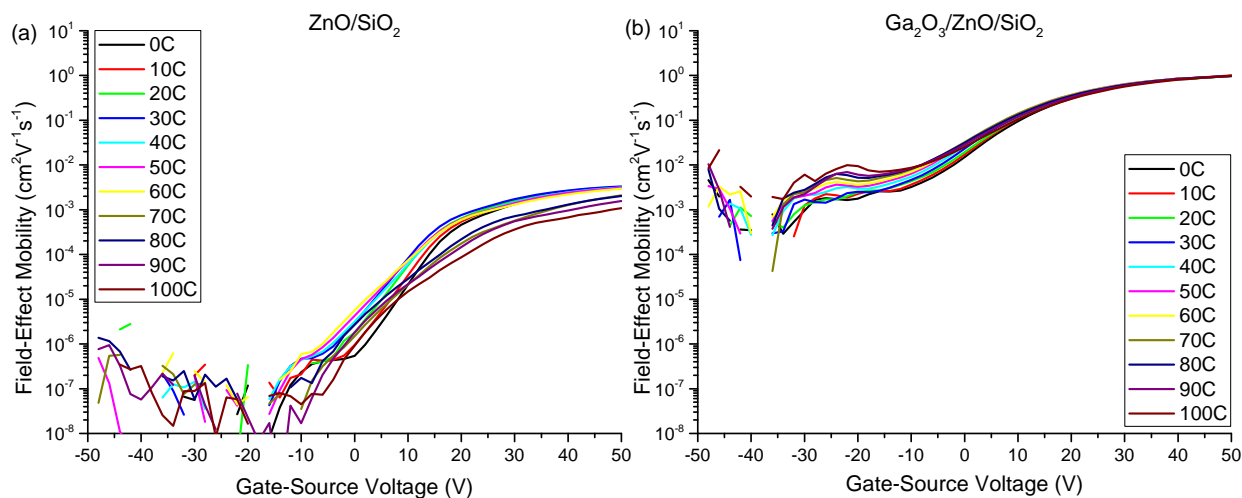
Figure 6.6: Field-effect mobility of ZnO and ZnO/Ga$_2$O$_3$ films as a function of gate-source voltage measured at different temperatures in a N$_2$ environment from $0\,°C$ to $100\,°C$.

ing on the experiment. Compressed air was used as the carrier gas at a pressure of 40 psi. The nozzle-to-substrate distance was fixed at 18 in.. The total precursor volume used was 20 mL. The deposition rate was fixed at $2\,mL\,min^{-1}$ using a syringe pump.

Ga$_2$O$_3$ films were prepared by spray-pyrolysis from solutions of gallium(III) chloride dissolved in ethanol to a concentration of 0.1M. The substrate temperature during deposition was maintained at a constant measured temperature in the range of 200 to $300\,°C$. Compressed air was used as the carrier gas at a pressure of 40 psi. The nozzle-to-substrate distance was fixed at 18 in.. The total precursor volume used was 20 mL. The deposition rate was fixed at $2\,mL\,min^{-1}$ using a syringe pump.

SnO$_2$:F films were prepared by spray-pyrolysis from solutions of tin(IV) chloride dissolved in acetone to a concentration of 0.1M. NH$_4$F was added amounting to 5 molar percent. The substrate temperature during deposition was maintained at a constant measured temperature of $240\,°C$. Compressed air was used as the carrier gas at a pressure of 40 psi. The nozzle-to-substrate distance was fixed at 18 in.. The total precursor volume used was 20 mL. The deposition rate was fixed at $2\,mL\,min^{-1}$ using a syringe pump.

Films were deposited onto different substrates depending on the experiment. For kelvin probe measurements, heavily doped silicon substrates ((100) n-type, phosphorous, $10^{19}cm^{-3}$) were used. For hall measurements, glass was used. For transistor fabrication, 100 nm thick thermally-oxidized heavily doped silicon substrates (n-type, phosphorous, $10(19)\,cm^{-3}$) were used.
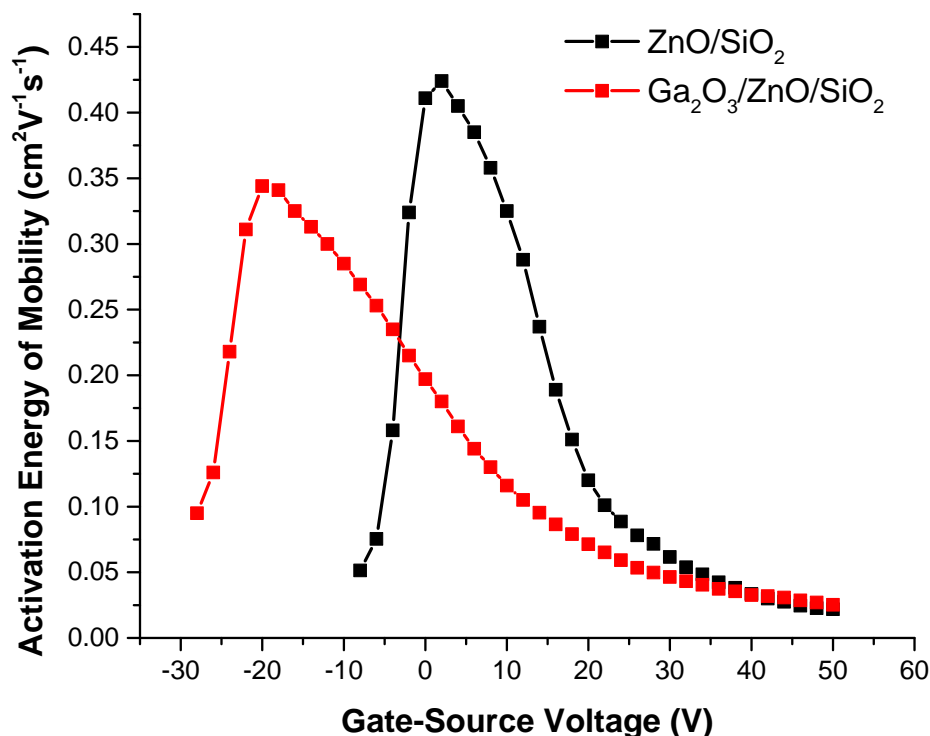
Figure 6.7: Activation energy of field-effect mobility of ZnO and ZnO/Ga$_2$O$_3$ films as a function of gate-source voltage.

## Transistor Fabrication

For transistor fabrication, inverted-coplanar TFTs were prepared consisting of a N++ silicon gate electrode, thermally-grown SiO$_2$ gate dielectric, ZnO semiconductor and SnO$_2$:F (F = 5 percent) source/drain electrodes. The choice to use an inverted-coplanar structure as opposed to the inverted-staggered structure was made to avoid vertical injection through the insulating Ga$_2$O$_3$ layer, expected to add additional series resistance that may confound mobility extraction.

## Hall Mobility Measurements

Hall mobility measurements were performed using a 1 T magnetic flux kit (DC magnet) supplied by Ecopia (Bridgetec).

## Kelvin Probe Measurements

Work function measurements were carried out using an ambient Kelvin probe measurement system from KP Technology.

## Transistor Characterization

Transistor characterization was carried out using a HP4155C semiconductor parameter analyzer. All measurements were performed under flow of $N_2$.

# Chapter 7

# Conclusions

A theory was developed to explain the observation of enhanced field-effect mobility of solution-processed transparent conductive oxide thin-film transistors due to high-k gate dielectrics. Through a comprehensive approach, which included extensive experimental and theoretical investigation, it was concluded that donor-like defects within high-k gate dielectrics donate electrons to adjacent transparent conductive oxide layers. The result of this electron donation is an increase in field-effect mobility resulting from an increase in steady-state electron concentration in the transparent conductive oxide semiconductor layer. This explanation, corroborated both by experiment and simulation, is fully consistent with contemporary physical descriptions of transport in disordered solids wherein electron transport is trap-limited. Additionally, predictions based on this new theory led to the development of an improved transistor structure that utilizes the high-k dielectric as a semiconductor encapsulate rather than a gate-dielectric. This has the previously established benefits of mobility enhancement without the negative drawbacks associated with dielectric defects such as frequency dispersion, hysteresis and gate leakage. As a consequence, not only does this establish a high level of confidence in the proposed theory, the improved understanding has significant practical implications enabling the development of optimally-tuned transparent conductive oxide TFTs that circumvent existing performance degradation incurred through solution-processing.

## 7.1   Summary of Contributions

### Experimental Methodology for Assessing Defects and Mobility

The non-equilibrium deposition conditions characteristic of solution-processing give rise to substantially higher defect concentrations than is typically observed through physical vapor deposition processes. As a consequence, electron transport is not simply limited to extended states but includes contributions from localized states as well. This can be distinguished experimentally based on the temperature dependence of mobility. When localized

states dominate electron transport, mobility is thermally-activated, governed by hopping and thermionic emission. By contrast, conduction exclusively in extended states does not exhibit thermally-activated behavior.

These differences in electron transport necessitate modification of extraction methods required for measuring mobility in a self-consistent way. Specifically, this involves separately measuring induced charge and low-field conductance as a function of gate voltage. This accounts for the fact that changes in electrostatic potential are governed by the filling of defects whereas transport involves thermal excitation into higher energy extended states, both of which are strongly gate-voltage dependent. This is what is meant by trap-limited conduction.

The significance of refining existing methodology for mobility extraction is that if charge and mobility are known accurately, then the measurement of mobility as a function of the induced charge as well as temperature yields information regarding the density of localized states. Knowledge of the density of localized states provides the raw input necessary for electrostatic modeling, defect engineering as well as predicting dynamic behavior.

Furthermore, the chemical nature of localized states is connected to synthetic conditions influenced, for example, by common thin-film properties such as crystallinity, orientation and extent of conversion. Consequently, establishing links between synthetic conditions and the density of localized states potentially drives the synthetic design of optimally-tuned semiconductors.

## Interaction of High-k Defects with Semiconductor Transport States

The presence of donor-like states in high-k dielectrics explains the mobility enhancement, higher effective dielectric constants, frequency dispersion in high-k dielectrics, enhanced leakage currents, counter-clockwise hysteresis and bias stress instability. This can be clearly seen experimentally, through comprehensive assessment of TFT data, as well as through electrostatic simulations based on the assumptions of trap-limited conduction.

The negative drawbacks associated with donor traps in the gate dielectric limit the practical utility of their apparent benefit. To circumvent these issues, the high-k dielectric can be used as a semiconductor encapsulate whereby the transverse electric field *seen* by defects within the high-k are screened by the electrons in the underlying semiconductor channel. This results in improved transport without degraded device integrity in the form of instability, hysteresis or leakage.

## 7.2 Recommendations for Future Work

With regard to electrostatics, it is only necessary to know the charge state (i.e. positive or negative), concentration and energy distribution of defects in order to solve Poisson's equation and predict electrostatic behavior. Chemical identification is unnecessary for this

purpose, but becomes important when attempting to reliably control electrostatic behavior through extrinsic modification (e.g. doping or annealing), notwithstanding gaining additional mechanistic understanding. As a consequence, this work can be continued in the following ways:

1. **Design of heterostructure dielectrics** incorporating electron-donating layers adjacent to the semiconductor and ideal insulating layers adjacent to the gate.

2. **Introduce known dopants** through ion-implantation into ideal insulators and study their impact on device behavior to establish trends with known defects.

3. Develop synthetic methods of **controllably incorporating donors into solution-processed high-k dielectrics**. Ideally, the baseline high-k would be a relatively good insulator (e.g. $Al_2O_3$) and dopants could be introduced that modify donor distributions both energetically and/or spatially.

4. **Chemical identification of dielectric defects** through electron spin resonance (ESR) measurements and positron annihilation spectroscopy (PAS).

5. **Polaron formation and transport.** The ionic character of metal-oxides and large frequency dispersion of solution-processed high-k dielectrics are expected to give rise to strong electron-phonon interactions which may result in an increase in carrier lifetime as it has been suggested in perovskite solar cells.

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# Appendix A

# Quasi-Static Capacitance-Voltage Measurements

Quasi-static capacitance-voltage (QSCV) is a technique that measures the static equilibrium capacitance voltage curve by measuring the displacement current of a capacitor in response to a linear voltage ramp of known amplitude and ramp rate [45]. In this section, an overview is provided of the Agilent specifications regarding how the 4155C/4156C interprets the displacement current for the calculation of the quasi-static capacitance according to chapter 4 of the Agilent 4155C/4156C User's Guide Vol.2, Edition 5.

The quasi-static capacitance is defined from the measured displacement current $I$, leakage current $I_L$ and voltage $V$ according to the following expression:

$$C = \frac{t_{integ,cap}(I - (1 - \alpha)I_L - \alpha I_{L,0})}{V - V_0} \tag{A.1}$$

where $t_{integ,cap}$ is the integration time for the capacitance measurement and $\alpha$ is a parameter that depends on the number of power line cycles required for the capacitance integration ($n$) as well as for stabilizing the current ($k$):

$$\alpha = \frac{2k - 1}{n} \tag{A.2}$$

$n$ is set by the user and is a function of the integration time $t_{integ,c}$ and the line frequency (e.g. 60 Hz). $k$ is not setable, but instead is internally monitored by the 4155C/4156C.

The following figure defines the measurement sequence used as well as the values of $V_0$ and $I_0$ obtained at each voltage step:
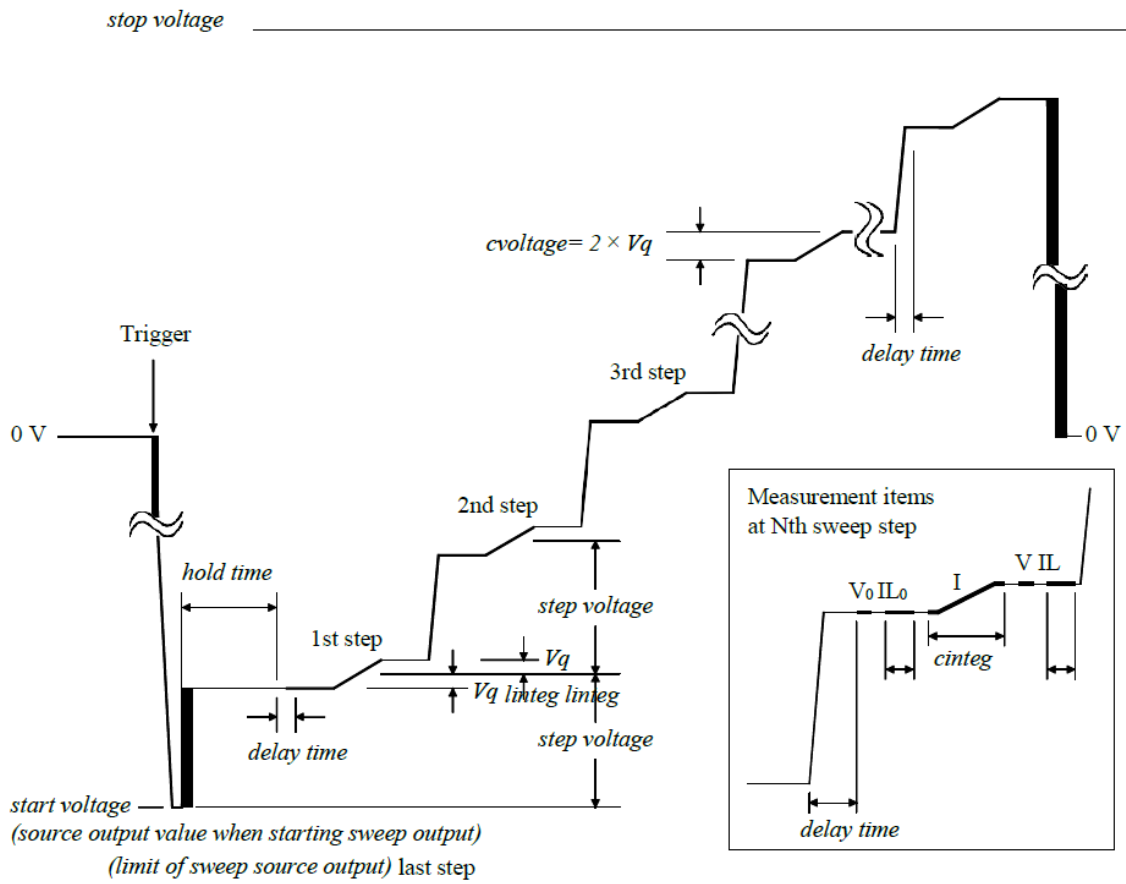
Figure A.1: Figure reprinted from chapter 4 of the Agilent 4155C/4156C User's Guide Vol.2, Edition 5

# Appendix B

# Summary of Mobility Extraction Methodology

The details of the method used to extract field-effect mobility in this work are given in chapter 2. In this section, a brief overview of the extraction method is given to serve as a quick reference.

The drain current is measured in the linear region as a function of gate-source voltage.

$$I_{D,LIN} = \frac{W}{L}\mu_{LIN}(V_{GS})Q_{ACC}(V_{GS})V_{DS,LIN} \tag{B.1}$$

From the drain current, the drain conductance is computed by taking the derivative of the drain current as a function of the drain-source voltage. This is done for each value of the gate-source voltage, producing a drain conductance as a function of the gate-source voltage.

$$G_{D,LIN}(V_{GS}) = \frac{\partial I_{D,LIN}}{\partial V_{DS}} \tag{B.2}$$

The quasi-static capacitance is measured as a function of gate-source voltage. From the capacitance, the accumulation charge is obtained through integration.

$$Q_{ACC}(V_{GS}) = \frac{1}{A_{ACTIVE}} \int_{V_{GS,MIN}}^{V_{GS}} \left(C_{G,S/D} - C_{DEP,MIN}\right)dV_{GS} \tag{B.3}$$

The mobility is calculated based on the drain conductance and the accumulation charge for each value of the gate-source voltage.

$$\mu_{LIN}(V_{GS}) = \frac{G_{D,LIN}(V_{GS})}{\frac{W}{L}Q_{ACC}(V_{GS})} \tag{B.4}$$

# Appendix C

# Density of States Extraction Method

Based on charge neutrality, the gate-induced charge distributes among all available charge states in the semiconductor (assuming no charge in the dielectric).

$$Q_{ind} = C_{ox}(V_{GS} - V_{FB} - \phi_s) = e \int_0^{t_{film}} n_{total}(x)dx \tag{C.1}$$

In general, the integral on the right hand side will be dominated by charge carrier concentrations near the dielectric-semiconductor interface up to a thickness regarded as the accumulation layer thickness $t_{acc}$. The accumulation layer thickness is analogous to the inversion-layer ($t_{inv}$) thickness in silicon MOSFETs which is usually no more than a couple nanometers.

$$Q_{ind} = e \int_0^{t_{acc}} n_{total}(x)dx \tag{C.2}$$

Assuming that the accumulation layer thickness is small, to a good approximation the carrier concentration is uniform over this region.

$$Q_{ind} \approx e t_{acc} n_{total} \tag{C.3}$$

The accumulation layer thickness is calculated by invoking the familiar "triangular barrier approximation" used in silicon MOSFETs which assumes that the surface potential drops linearly over the accumulation layer thickness such that the electric field is uniform in this region.

$$t_{acc} = \frac{\phi_s}{E_s} \tag{C.4}$$

By Gauss' law, the accumulation layer thickness can is expressible in terms of the induced charge density:

$$t_{acc} = \frac{\phi_s \epsilon_s}{Q_{ind}} \tag{C.5}$$

Combining these results allows the expression for the total charge concentration.

$$n_{total} = \frac{Q_{ind}^2}{e\epsilon_s \phi_s} \tag{C.6}$$

The last and final assumption is in regards to the surface potential, which in general will not exceed the difference between the conduction band and the Fermi-energy in the semiconductor bulk. (i.e. the point of degeneracy). This value is readily extracted experimentally from the value of the activation energy of mobility at flat-band conditions.

$$n_{total} = \frac{Q_{ind}^2}{e\epsilon_s(E_C - E_F)_{bulk}} \tag{C.7}$$

The induced charge is obtained by integration of the gate capacitance.

$$Q_{ind} = \int_{V_{min}}^{V_{GS}} C_G(V_{GS})dV_{GS} \tag{C.8}$$

This expression is evaluated at each value of the gate voltage and plotted as a function of the activation energy, interpreted as the Fermi-level depth below the conduction band edge.

The density of localized states can be obtained by differentiating $n_{total}$ with respect to the activation energy:

$$g_{total}(E) = \frac{\partial n_{total}}{\partial E} \tag{C.9}$$

# Appendix D

# Theory of Spray Pyrolysis Deposition

In this section, a summary is given for the basic theory of spray pyrolysis deposition, following the work of Filipovic et al [20].

The deposition of thin-films using spray-pyrolysis can be separated into three main groups:

1. Creation of aerosol (i.e. atomization)

2. Transport of aerosol

3. Decomposition of precursor

## D.1   Atomization

Interestingly, it has been shown that the size of the liquid droplets in an aerosol do not depend on fluid properties of the solution, depending entirely on the fluid charge density level $\rho_e$:

$$r^2 = 10^{-17}[J]\frac{3\epsilon_0}{q\rho_e} \tag{D.1}$$

Assuming a spherical droplet, the droplet radius can be related to its mass and density.

$$m = \frac{4\pi}{3}\rho_q r^3 \tag{D.2}$$

Pressure and ultrasonic atomizers exist for creating aerosols. Pressure-based atomizers use a high speed gas to create the aerosol whereas ultrasonic atomizers work on the basis of cavitation in a liquid. In this work, we use a pressure-fed atomizer due to simplicity. The use of pressure-fed atomizers results in an increase in droplet size with pressure.

It has been shown that droplets fall within a cone of 70 degrees of the nozzle opening, whereas half of the droplets are within a narrower angle of 12 degrees of the nozzle opening (Perednis).

## D.2  Transport

Depending on their initial size, droplets moving through the air experience structural changes. Intuitively they may evaporates to form a vapor or condenses to form a particle, resulting in a change in droplet mass. This, in turn, affects the influence of external forces acting on the droplets. Four external forces direct the path of a droplet as it transports from the nozzle towards the substrate:

1. Gravitational force

2. Electrical force

3. Stokes force

4. Thermophoretic force

Intuitively, gravity is the dominant force for massive droplets. The electrical force applies when nozzles are electrically driven, as is the case of an ultrasonic atomizer. This force can be neglected for pressure-atomizers, since droplets are not charged. The stokes force is a retarding force due to friction the droplet encounters while moving through the air. This force is a function of the droplet velocity and the radius, increasing with both:

$$F_{Stokes} = 6\pi\eta_{air}r(v_d - v_a)(1 + \frac{3}{8}Re) \tag{D.3}$$

where $\eta_{air}$ is the air viscosity, $v_d$ and $v_a$ are the velocities of the droplet and the air respectively and Re is the Reynolds number of the liquid.

The thermophoretic force is a retarding force due to an enhancment of the droplet temperature near the substrate. Because the substrate is heated, droplets encounter a thermal gradient causing them to diffuse away from the substrate to lower their energy in an analogous way to the thermo-electric effect. The strength of the thermophoretic force is given by:

$$F_t = \frac{3\pi\eta_a^2 r}{\rho_a} \frac{3\kappa_a}{2\kappa_a^2 + \kappa_d} \frac{\nabla(T_a)}{T_d} \tag{D.4}$$

where $\eta_a$ is the viscosity of the air, $T_d$ is the droplet temperature, $T_a$ is the air temperature, $\rho_a$ is the density of the air and $\kappa_a$ and $\kappa_d$ are the thermal conductivities of the air and droplet respectively. The thermophoretic force is only significant when droplet size is larger than the mean free path of the air molecules.

## D.3  Decomposition

The transport of droplets towards the heated substrate results in mass loss leading to vapor formation and/or precipitation. If the substrate temperature is sufficiently high, the precipitate may vaporize before impinging upon the substrate. If this happens, film growth is essentially governed by the same processes occurring in chemical vapor deposition:

1. Molecular diffusion of reactant species to the surface.

2. Adsorption of molecular species on the surface.

3. Surface diffusion and chemical reaction (conversion)

4. Desorption and diffusion of reactant byproducts