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High Voltage GaN-on-Si Field-Effect Transistors for Switching Applications

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High Voltage GaN-on-Si Field-Effect Transistors for Switching Applications

A thesis submitted in partial satisfaction of the requirements for the degree Master of Science in Electrical Engineering

by

Xu Chen

2015

ABSTRACT OF THE THESIS

High Voltage GaN-on-Si Field-Effect Transistors for Switching Applications

by

Xu Chen

Master of Science in Electrical Engineering
University of California, Los Angeles, 2015
Professor Mau-Chung Frank Chang, Chair

Because of the special material properties such as wide band gap, high electron mobility and high breakdown field, Gallium nitride (GaN) based semiconductor devices are well suited for power switching applications [1]–[6]. GaN-on-Si technology could significantly reduce the wafer cost of GaN devices. The size of high quality GaN-on-Si wafer is now available up to 6 inch [7]. In order to implement GaN transistors for high-voltage switching applications, there are three core technologies. One is the realization of normally-off operation with low leakage current; the second

is the reduction of the on-resistance; the third is increasing the breakdown voltage of the device. Another advantage of GaN based device is the capability to operate at high temperatures. The wide band gap of GaN leads to very low thermal generation of carriers. In this thesis, a field-effect transistor (FET) employing metal-insulator-semiconductor (MIS) structure is proposed to result normally-off operation, temperature-independent threshold voltage and capability of blocking 600V at 200 °C.

The thesis of Xu Chen is approved.

Kang Lung Wang

Yuanxun Wang

Mau-Chung Frank Chang, Chair

University of California, Los Angeles

2015

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CHAPTER 1

Introduction

1.1 Advantage of GaN over other semiconductor materials

The power device figurer of merit is described as V_{BR}^2/R_{on}. Thus, the most important requirements for power device are high breakdown voltage ($V_{BR)}$ and low on-resistance ($R_{on)}$. Silicon is the most commonly used semiconductor material for almost all devices. However, silicon based power devices rapidly reached the theoretical limit of silicon material. Although there are some novel device structures such as insulated-gate bipolar transistor (IGBT) and Superjunction MOSFET, pushed silicon power device beyond traditional silicon power device performance limit, they suffered from high switching loss and limited switching frequency range.

Material	Si	4H-SiC	GaN	AlN	Diamond
E_g (eV)	1.1	3.26	3.39	6.1	5.45
n_i (cm^{-3})	1.5×10^{10}	8.2×10^{-9}	1.9×10^{-10}	$\sim10^{-31}$	1.6×10^{-27}
ε_r	11.8	10	9.0	8.4	5.5
μ_n (cm^2/Vs)	1350	700	900	1100	1900
E_c (10^6 V/cm)	0.3	3	3.3	11.7	5.6
v_{sat} (10^7 cm/s)	1.0	2.0	2.5	1.8	2.7
Θ_K (W/cmK)	1.5	4.5	1.3	2.5	20

Table I. Physical properties of different semiconductors for high-voltage devices

Wide band gap materials, especially SiC and GaN, attracted researcher's attention for high performance power devices. Table I compares some key electronic properties of GaN with other semiconductors [9]. GaN demonstrated saturated electron velocities as high as 2.5×10^7 cm/s [10] and band gap as large as 3.39 eV. Those superior material properties lead to an ideal material for high performance power device. GaN is also benefited from the high electron density and high mobility in the two-dimensional electron gas (2DEG) formed in the AlGaN/GaN heterojunction interface.

1.2 AlGaN/GaN heterostructure

AlGaN/GaN heterojunction has a highly conductive 2DEG channel at the interface which is created by polarization doping (Figure 1.1). At the AlGaN/GaN interface, the conduction band is lower than the Fermi level with zero bias. Because carriers in the 2DEG channel are almost not affected by impurity scattering because the GaN channel layer is not intentionally doped. The almost impurity free channel layer allows electrons have very high mobility while maintaining high channel charge density. As a result AlGaN/GaN High-electron-mobility transistor (HEMT) could result very low on-resistance with carefully engineer epitaxy layers. Taking advantage of the highly conductive 2DEG channel is the major advantage of GaN over other wide band gap semiconductor material systems such as SiC and diamond.

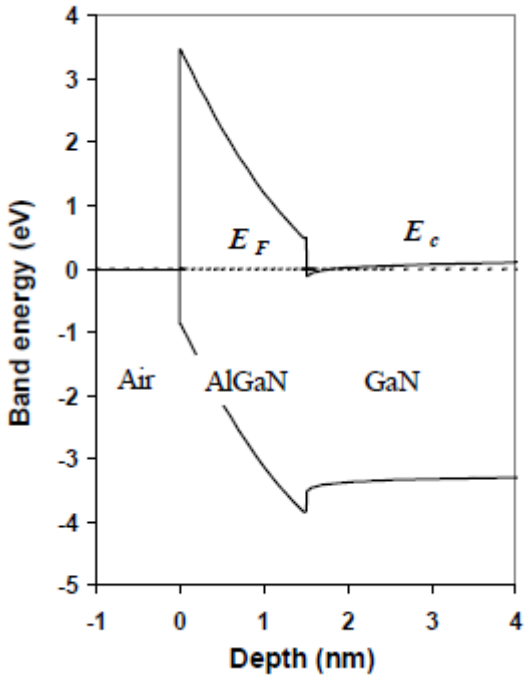


Figure1.1 AlGaN/GaN polarization model

Compared with SiC, GaN has higher mobility due to the 2DEG channel. Similar silicon, SiC based field-effect transistors has a heavily doped channel layer which degrades the channel carrier mobility. This advantage makes GaN become a more suitable solution for fast operation and ultra-low loss switching applications. More importantly, the development of GaN power devices can be benefited from the matured GaN based light emitting diode (LED) industry by sharing same semiconductor material and similar growth equipment. For an example the metalorganic vapour phase epitaxy (MOCVD) system is already available for six inch wafers. The GaN-on-Si technology can be easily adopted by silicon foundry. This is particularly important for high volume production. Although diamond has higher band gap, it still lacking of proper solution to form low resistance contacts and low resistance channel. The extra contact resistance will cause high on-resistance and reduce switch efficiency.

The wide band gap of GaN could also offer very low intrinsic carrier concentration and gives extremely low junction leakage through the buffer layer even at high temperature. In this study our fabricated devices demonstrated low leakage current at 200^{o}C.

1.3 Principle of HEMTs

High electron mobility transistor (HEMT) was initially developed in the 80s. The demonstration of modulated doped AlGaAs/GaAs hetero structure enabled the development of AlGaAs/GaAs based HEMTs. Early HEMTs are based on AlGaAs/GaAs system which is the best understand heterojunction material at that time. The core of HEMT is the highly conductive channel layer in the hetetrojunction structure.

For HEMT device, the drain current is controlled by the gate modulation of 2DEG. At zero gate bias, the channel layer is open. The drain current increase as the gate bias increase until the gate source voltage approaches the threshold voltage. The DC-IV curve is shown in Figure1.2.

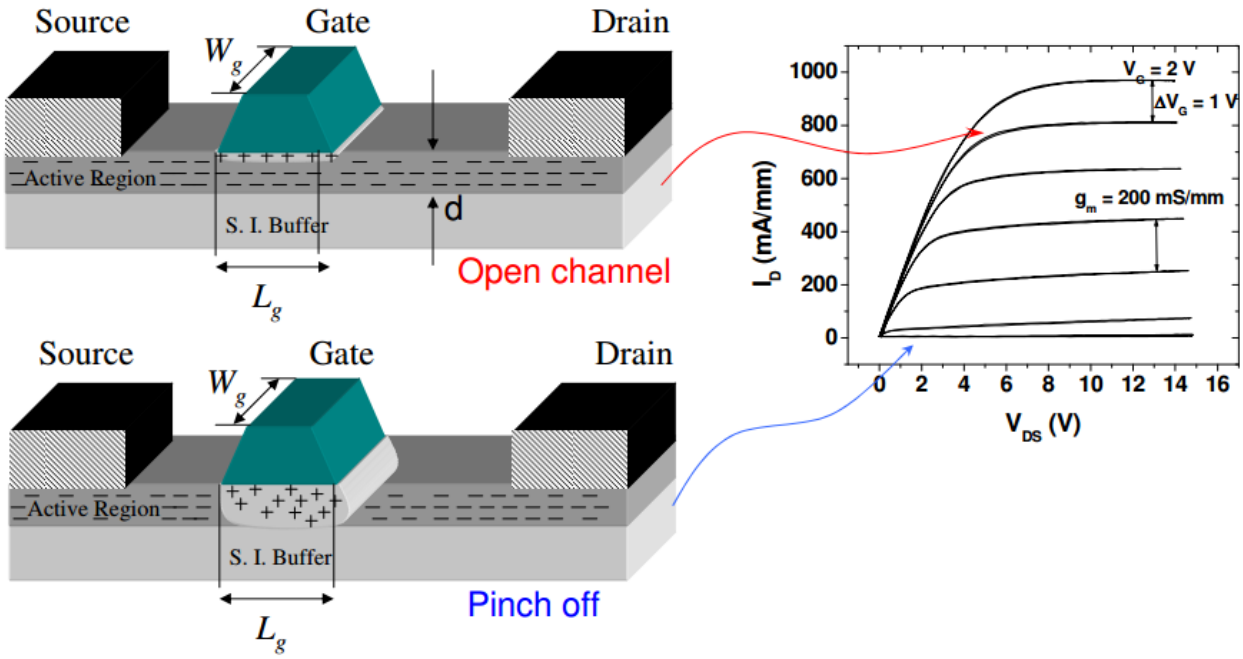


Figure 1.2. Typical HEMT device and IV curves.

The power device figurer of merit is described as V_{BR}^2/R_{on}. As a result, a power switch needs to have high break down voltage and low on-resistance at the same time. However, low resistance are normally associated with high doping level which could significantly reduce the breakdown voltage because the breakdown voltage is twice integration of the doping level in the depletion region.

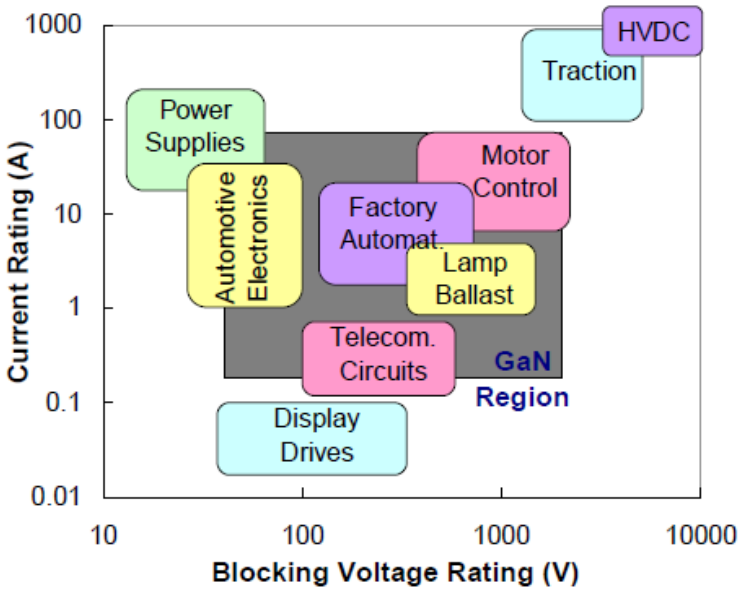


Figure 1.3. Applications for GaN power switching HEMTs.

Among the many potential advantages of power transistors based on wide band gap semiconductors such as GaN, a very important one is the capability of operating at high temperatures, due to the reduced thermal generation of carriers across the large band gap. However, for field-effect transistors employing metal-insulator-semiconductor structures, the high temperature capability can be hindered by the thermal activation of trap states at the insulator-semiconductor interface (Figure 1.4), which gives rise to a negative shift of threshold voltage [11,12] and increase of off-state leakage. In this paper, we report that with properly engineered MIS structures, one can build normally-off GaN-on-Si FETs with temperature-independent threshold voltage and capability of blocking 600 V at 200 °

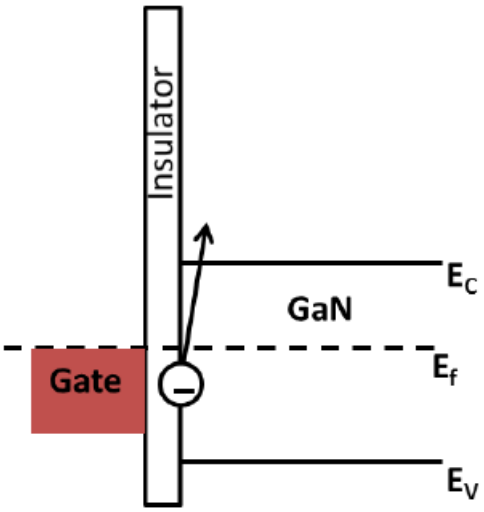


Figure 1.4. Band diagram depicting the generation of electrons from interface trap states to the conduction band in a metal-insulator-semiconductor structure.

1.4 Organization of this Thesis

Over the past decades, GaN based HEMT was fast developed. Recent progress made GaN became a promising candidate for high power and high frequency applications. Although the relatively high cost is still limiting the application of GaN based device, the GaN-on-Si epitaxy wafer could significantly reduce the cost. In chapter2, several key design structure were summarized. In Chapter 3, an analysis of GaN device in high temperature was described. In Chapter 4, the method to improvement the gate module process was discussed.

CHAPTER 2

Structures Design for High Voltage GaN HEMTs

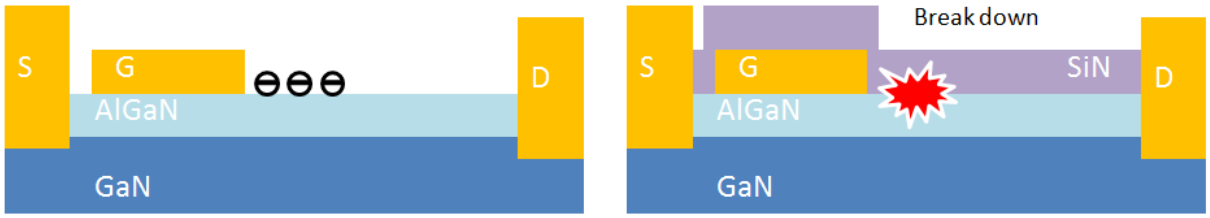
There are two major parameters to evaluate the performance of a power device, the first one is the breakdown voltage and the second one is the switching resistance. The power device figure of merit is described as V_{BR}^2/R_{on} which requires a device to maximize the breakdown voltage and minimize the on-resistance. The break down voltage is directly related to the critical electric field and the on resistance is a result of the electron mobility in the channel. GaN is an ideal material for power device because its critical electric field is 3.3 MV/cm which is more than ten times of slicon.

For a normal switching device, the break down voltage should be at least twice than the operating voltage. The on-resistance of the device should be very low to reduce the power consumption in the switching process. For low frequency operation, Baliga [13] derived the power device a figure of merit, BFOM = $\varepsilon \cdot \mu \cdot E_c^3$, which defined the material parameters of a semiconductor for high performance power device. Here μ is the mobility and E_c is the critical electric field. This equation assumes the conduction loss is only due to the channel resistance. For a real device the contact resistance contributes considerable amount of conduction loss. For wide band gap semiconductor material, it is challenging to form ultra-low resistance contacts. Normally there are two solutions to form low resistance contact, Molecular beam epitaxy (MBE) InGaN regrowth contact and high

temperature metal alloy. In order to reduce the fabrication cost, aluminum based metal alloy is used in this project.

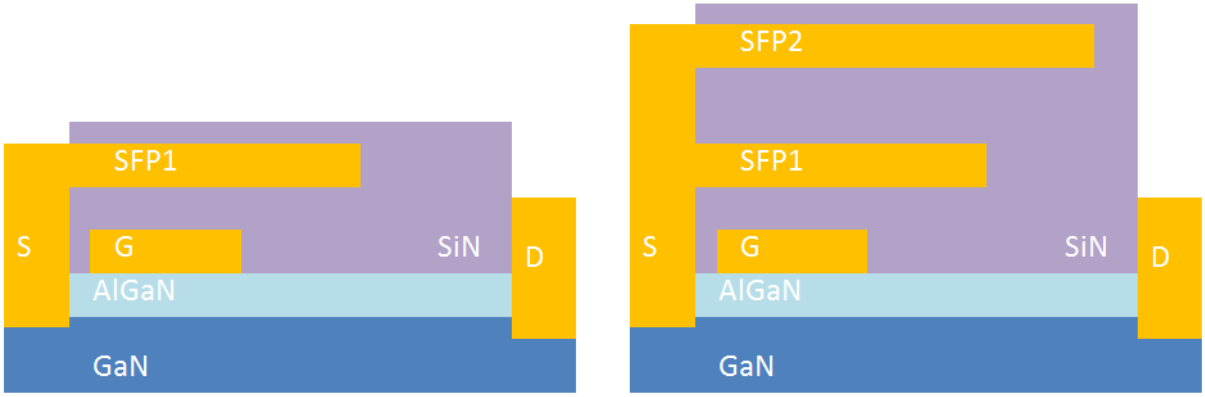
Another advantage of GaN HEMTs is the short rise and fall time. This is especially important for high frequency switching application. The conduction loss can be decreased by increase the change density in the 2DEG or simply increase the gate width. But the switching loss is related to the parasitic capacitance of the device. As the device dimension increases, the parasitic capacitance increases as well. Thus the total loss will be increased for large device. The total loss can be minimized by choosing the optimized device area. For a given device structure and dimension, the switching losses increases as the increasing switching frequency.

2.1 Field plates structure for HEMT device



(a) (b)

Figure 2.1. (a) For device without passivation, Charges are trapped on the surface near the gate. Although it could increase the breakdown voltage by depleting the 2DEG under the gate, such device suffers from current collapse effect); (b) Typical GaN HEMT with SiN passivation.



(a) (b)

Figure2.2. (a) Device with on source field plate; (b) Device with two source field plates.

When the device is at pinch-off point the device has maximum electric field at the gate edge on the drain side [15]. Without passivation, the AlGaN surface is filled with electrons especially close the gate region. This effect may increase the breakdown voltage by extending the extended depletion region but the exposed surface states will significantly decrease the DC and RF performance. After passivation, the electric field reaches a peak at the

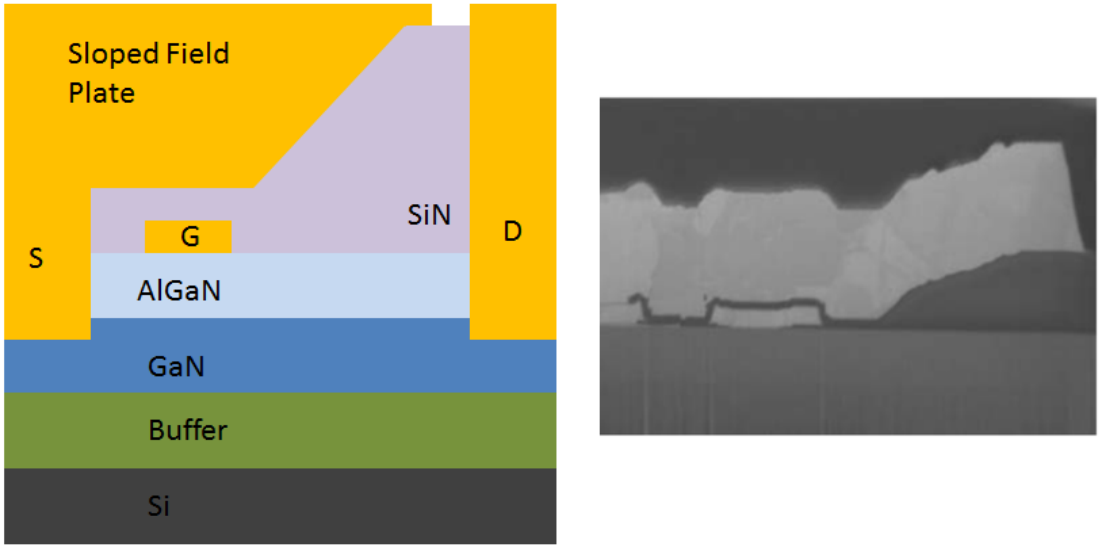
SiN passivation is required for both low frequency and high frequency devices. Before passivation the surface states adjacent to the gate fill up with electrons thereby extending the depletion region width. However there is dc-to-rf dispersion in the IV curves as the surface states do not respond fast to the changes in gate bias.

2.2 Sloped Field-Plate

The performance advantages of the GaN HEMTs rely on the high breakdown field of the GaN material and the high electron mobility of the 2-dimesional electron gas (2DEG) in the AlGaN/GaN heterojunction [16, 17]. In order to take full advantage of the excellent material properties, the shape of the electric-field distribution in the GaN HEMTs must be carefully optimized to operate the device at its highest switching speed while handling a large voltage swing. Without proper field-shaping, a high electric-field can cause electron injection into traps, hence degrading the output current and on-resistance during switching operation. For microwave applications, a V-shaped gate with integrated sloped field-plate was used to control the electric-field with minimal added capacitance associated with the field-plate [18]. For high-voltage applications, a multiple field plates structure was used to scale up the operating voltage [19].

Figure 2.3(a) and (b) respectively show the cross-sectional schematic and SEM of a GaN HEMT with a sloped field plate, which was used in this study. The device consists of an AlGaN/GaN layer grown on a silicon substrate, a dielectric passivation layer, source/drain electrodes, a gate electrode with a gate-connected field-plate, and a source-connected field-plate with sloped sidewall. The gate-connected field-plate was used to prevent trapping at low-voltage. The sloped field-plate shape was created by exposing the photoresist with a gray scale mask. The mask allows modulated intensity of light passing through to create a sloped profile in the photoresist. The profile is then transferred to the underlying dielectric layer by dry etch. Schematics showing the process for making the sloped sidewall are illustrated in Figure 2.4. The cross-section SEM picture of the resulted device structure is shown in Figure2.3 (b). The sloped field-plate process is

simpler and faster than a multiple field-plate process as it eliminates etching and metal deposition steps.



(a) (B)

Figure 2.3. (a) Schematic of a GaN HEMT device with a sloped field-plate; (b) SEM cross sectional view of a sloped field-plate device.

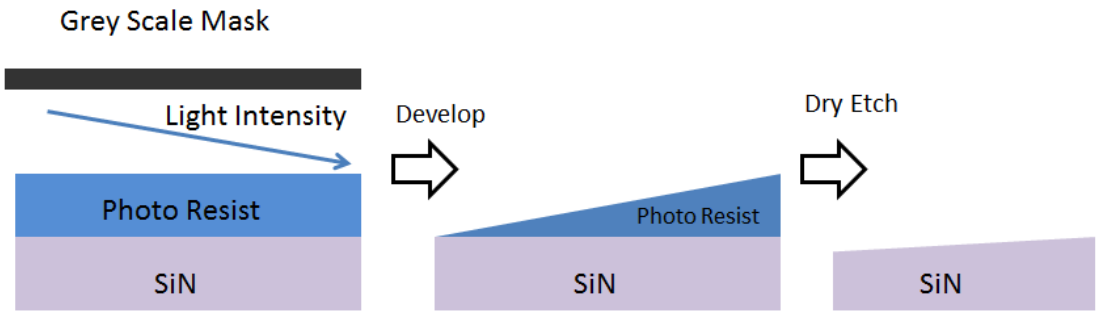


Figure 2.4. Schematic of the fabrication process to create the sloped field-plate profile. A gray scale mask for photo resist pattering and dielectric pattern transferring by dry etch.

The device under this study has a gate length of 1 μm and a gate width of 40 mm. DC-IV characteristics were measured using an Agilent B1505A semiconductor parameter analyzer. The device has a static or DC on-resistance of 12.5 ohm.mm at Vg=2.5V and Id=50mA/mm. The threshold voltage is around 0.25V defined at Vd=0.1V and Id=10μA/mm. Breakdown voltage of more than 600V was achieved with this device. The dynamic on-resistance was evaluated with the circuit depicted in figure 2.5. The circuit applies the high voltage to the drain of the Device Under Test (DUT) by switching Q1 on for 100μs while the DUT is held in the off-state. The DUT is then turned to the on-state at the same time Q1 is switched off. The on-resistance is calculated by measuring the drain current with a sense resistor (Rs) and the drain voltage (Vd) with an oscilloscope during the on-state of the DUT. A comparison of the measured dynamic on-resistance is made between two devices, the first with a 3-fieldplate structure, and the second with a sloped field-plate structure. Both devices were fabricated using the same methods as described in Ref. 2 other than different field-plates. The normalized value of the dynamic on-resistance was calculated relative to the static on-resistance of the device. The increase of dynamic on-resistance at 600V is 47% for the device with multiple field-plates, and only 19% for the device with sloped field-plate. This performance improvement is attributed to a smoother electric-field profile resulted from the sloped field-plate.

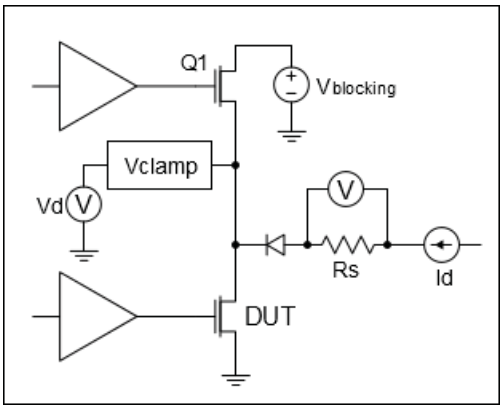


Figure 2.5. Dynamic on-resistance measurement circuit.

Turn-on and turn-off waveform switch GaN ½ bridge at 300V and 16A at 23C and 100C

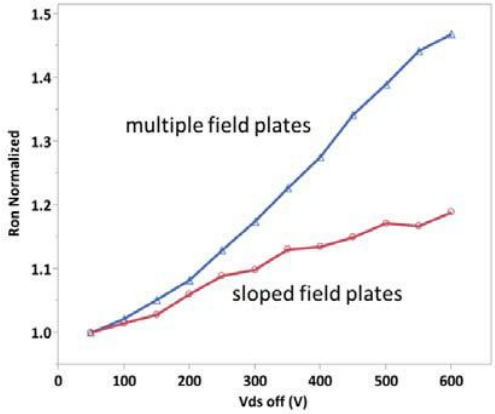


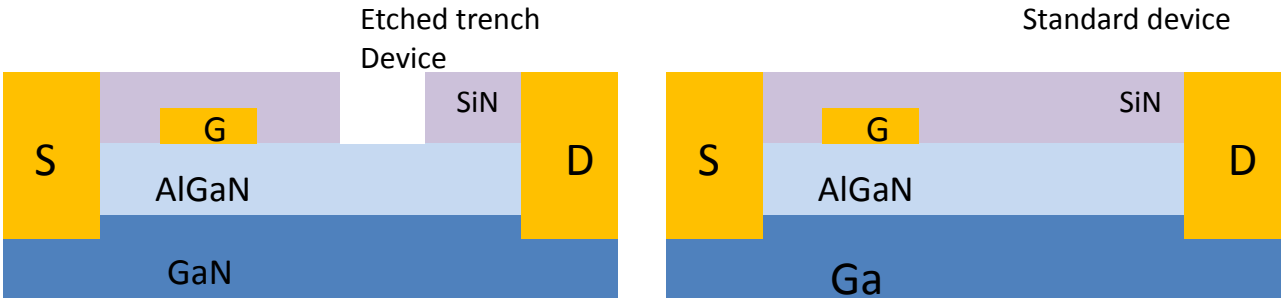
Figure 2.6. Comparison of dynamic Ron of devices with and without sloped field plate.

Results suggest that the sloped field-plate approach is a better approach for reducing the peak electric-field, mitigating field-assisted trapping, and reducing the degradation of dynamic on-resistance. A 60% reduction in dynamic on-resistance at 600V was achieved by switching from a multiple field-plate design to a sloped field-plate design.

2.3 Gate leakage of AlGaN/GaN HEMT

The large band gap and high electron mobility make GaN become an ideal material for high power switch applications. GaN metal semiconductor field-effect transistor

(MESFET) and AlGaN/GaN high electron mobility transistor devices suffer from high gate leakage current. The leakage current not only reduces the switching efficiency but also cause reliability problems due to power dissipated in the switching device. Gate leakage is measured after SiN passivation. The possible source of gate leakage current is from the surface or the passication SiN layer. To identify the gate leakage path, a controlled experiment was performed. In this experiment, a deep trench was etched in the SiN passivation layer which is shown in Figure 2.7(a) and (b). Devices with isolation trench have similar a gate leakage to the device without isolation trench. This experiment showed the leakage is not through the passivation layer.



(a) (b)

Figure 2.7. (a) Etch trenched device; (b) standard device.

The trench location could be shifted from gate to drain. In this experiment, the SiN trench was etched at 1.6um and 1.1 from the gate. In Figure 2.6, the gate leakage showed no strong correlation with the trench location. The leakage is not from the SiN passivation layer and the possible leakage should be from the AlGaN surface.

In figure 2.8, it is indicated gate leakage does not depend on the source drain spacing. Gate leakage current is independent with as the current does not change from 0.7μm to 2μm. In the figure we also can see the gate leakage currently is directly promotional to

gate width which is easy to understand.

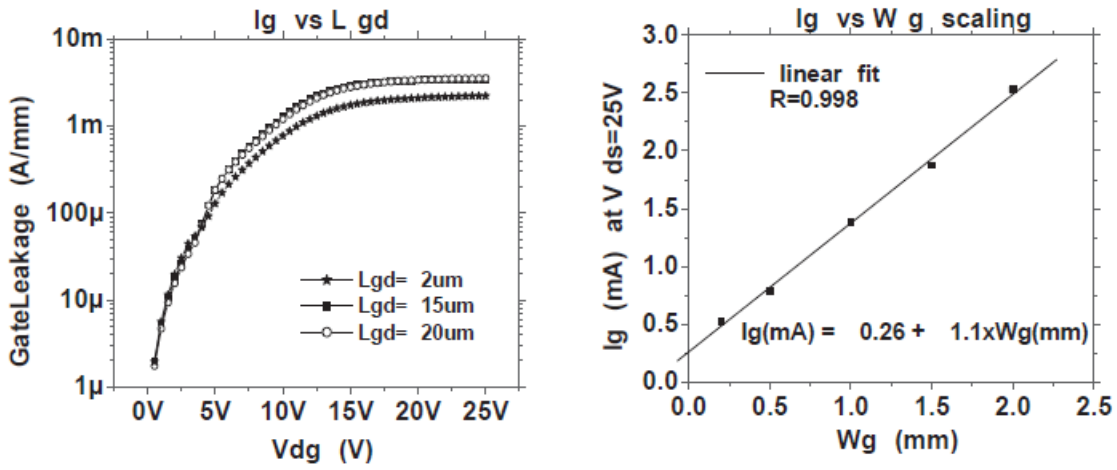


Figure 2.8. (a) Gate Leakage is independent with Lgd; (b) Gate leakage scales with device width W_g.

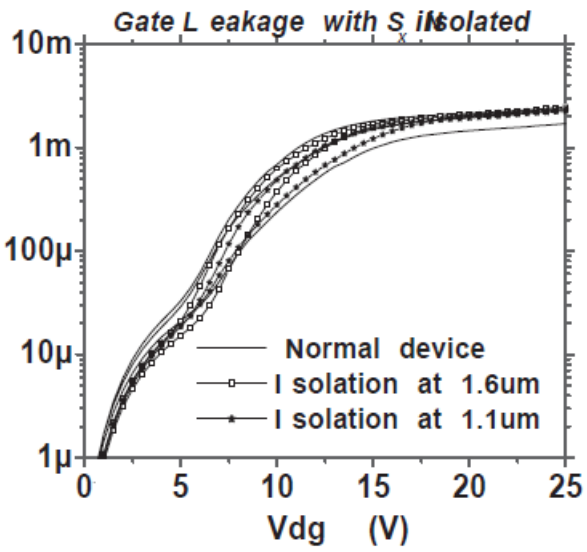


Figure 2.9. Showed the gate leakage current of standard device and device with different etched trench device.

2.4 Reduce gate leakage by using gate dielectrics

This experiment shows the leakage path is through the AlGaN layer at the gate region. In

order to reduce the gate leakage, large barrier between AlGaN and gate is required. Various dielectric materials have been used to insulate the gate leakage in HEMT device. A thin layer of SiO_2 deposited by plasmaenhanced chemical vapor deposition (PECVD) under the gate has been shown to reduce gate leakage by six orders of magnitude in an AlGaN/GaN HEMT device [18].In order to increase the SiO2 dielectric layer quality, atomic layer deposition (ALD) is recently used. In this work, ALD SiO2 growth method was carefully studied for ultra-low gate leakage current. The relatively low dielectric constant of SiO_2, it leaks to large pinch-off voltage and reduce high frequency performance. It is important for high speed GaN HEMT but most of power devices operate at low frequency. This optimization of gate dielectric will be discussed in chapter 4.

2.5 Leakage from field-plates

The leakage through the field plate can be characterized by doing leakage test for a device without gate, and the device structure is shown in figure2.10. In this structure, the possible leakage current path is from the field-plate through the passivation layer and the AlGaN to the 2-DEG channel. The leakage is measured by ground the source and applying a positive voltage on the drain. The testing result showed the leakage from SFP is only about one tenth of the gate leakage current.

The electric field at the field-plate edge increases with the drain bias. At high bias, file plate leakage may play a critical role in the leakage and breakdown process. Thus, the SiN passivation quality is important to reduce total leakage current at drain.

The experiment showed the leakage happens at the AlGaN layer at the drain end of the gate. The leakage current in AlGaN is still not well understood. Different dielectric

materials were tested for gate insulate for GaN HEMTs. Gate dielectric materials have serious degradation problem especially for power devices operating at high voltage and temperature. In-situ dielectrics grown at high temperature is important for power devices.

2.6 Buffer leakage in GaN HEMT

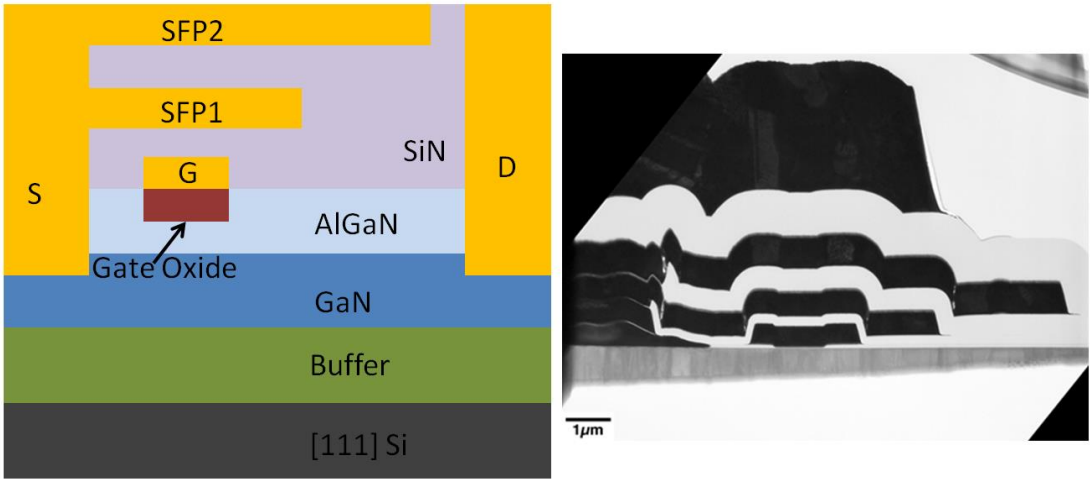
A semi-insulating buffer is the most basic requirement for high power devices. High leakage current will cause large power dissipation and limit the conversion efficiency. Large amount of power dissipated in the device will could rapidly increase the operation temperate. This will decrease the electron mobility and worsen the on-resistance. Conductive substrate also degrades the breakdown voltage by enhancing the impact ionization. The buffer layer could grow on various substrates including sapphire, SiC and Silicon.

CHAPTER 3

GaN HEMT device fabrication and characterization

3.1 Device design and fabrication

The cross-sectional schematic of the device structure is shown in figure 3.1. The AlGaN/GaNepi-structure, with the total epi-layer thickness of around 4 μm, was grown on a Si substrate. The GaN-on-Si platform has the advantage of low material cost, and good scalability to large wafer sizes. Device fabrication steps included device isolation, gate recess, gate dielectric deposition, source/drain ohmic metallization, gate metallization, surface passivation, and formation of field-plates similar to what described in Ref. [19]. The gate recess and gate dielectric deposition are the key steps to achieve normally-off and high-temperature operation. The device presented in this paper has a gate length of 1 μm and a gate width of 600 μm.



(a) (b)

Figure 3.1. Cross-sectional schematic of the GaN-on-Si field-effect transistor (b) TEM image for the device

3.2 Testing result with different temperature

Figure 3.2 shows transfer characteristics of the fabricated device. A maximum current of 280 mA/mm was measured. There is negligible hysteresis between positive and negative sweeps, indicating low density of trap states in the MIS structure. Figure 3.3 shows sub-threshold characteristics in log scale, at varied measurement temperatures. The GaN-on-Si transistor remained normally-off at all different temperatures. From 25 °C to 200 °C, the off-state drain leakage increased by 10 times.

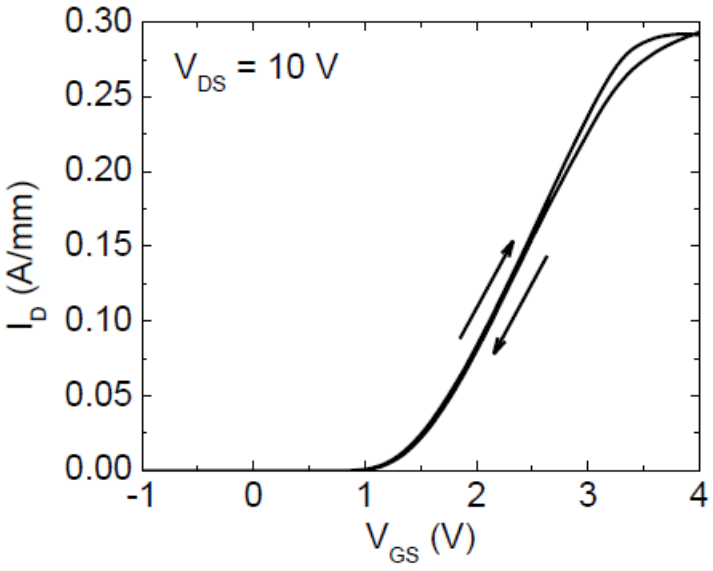


Figure 3.2. ID vs. VGS characteristics at VDS=10V. VGS was swept from -1V to 4V, then from 4V to -1V.

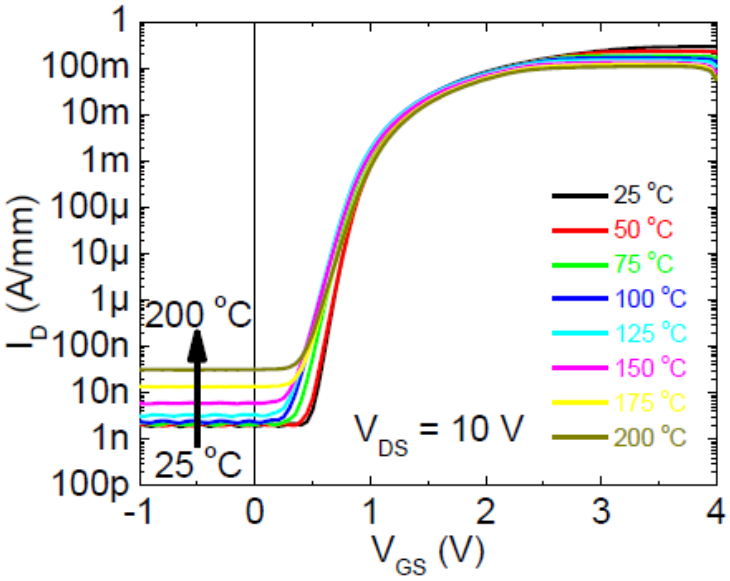


Figure 3.3. ID vs. VGS sub-threshold characteristics at VDS=10V and different temperatures.

Figure 3.4 plots the threshold voltage as a function of temperature. The threshold voltage, which was defined as the gate-to-source voltage where the drain current reaches 10 μA/mm at a drain bias of 10 V, was nearly independent of the temperature while both the Si SJ-MOSFET and the SiC MOSFET showed a clear negative shift of threshold voltage with the increase of the temperature. A temperature independent threshold is a desirable feature to avoid thermal runaway and maintain low level of drain leakage current at high temperatures.

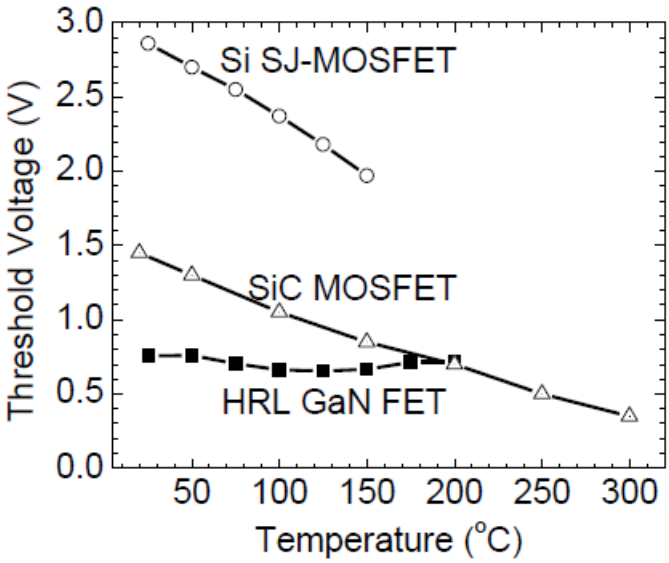


Figure 3.4. Threshold voltage of GaN FET, Si SJ-MOSFET, and HRL GaN FET as a function of temperature.

Figure 3.5 shows that the sub-threshold swing of the GaN FET increased from 72 mV/decade at 25 °C to 123 mV/decade at 200 °C, corresponding to an ideality factor close to 1.3. An ideality factor close to 1.0 suggests good gate control and high-quality MIS interface.

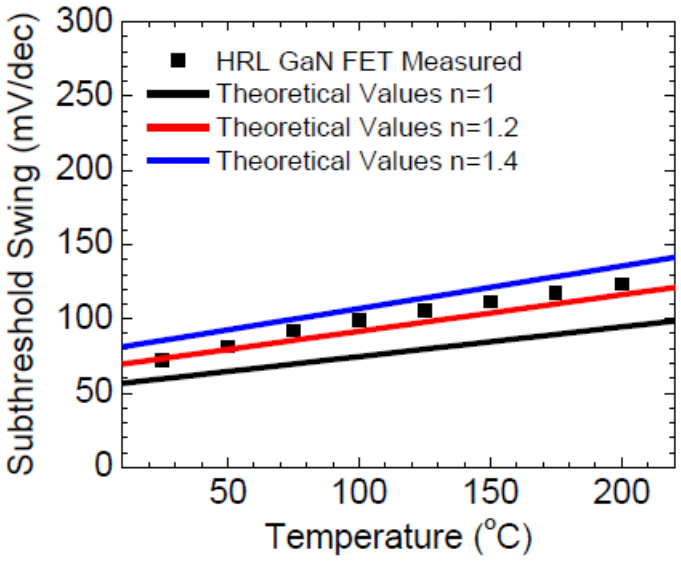


Figure 3.5. Sub-threshold swing of HRL GaN FET as a function of temperature.

Figure 3.6 plots the transistor output characteristics at 25 °C and 200 °C. The on-resistance is 17.3 Ω-mm at 25 °C. Both the output current density and the on-resistance degraded at high temperatures, due to the decrease of electron mobility caused by the increase of phonon scattering. The dependence of on-resistance on temperature is shown in figure 3.7. The increase of on-resistance from 25 °C and 200 °C is similar to the SiC MSOFET, and less than the Si SJ-MOSFET.

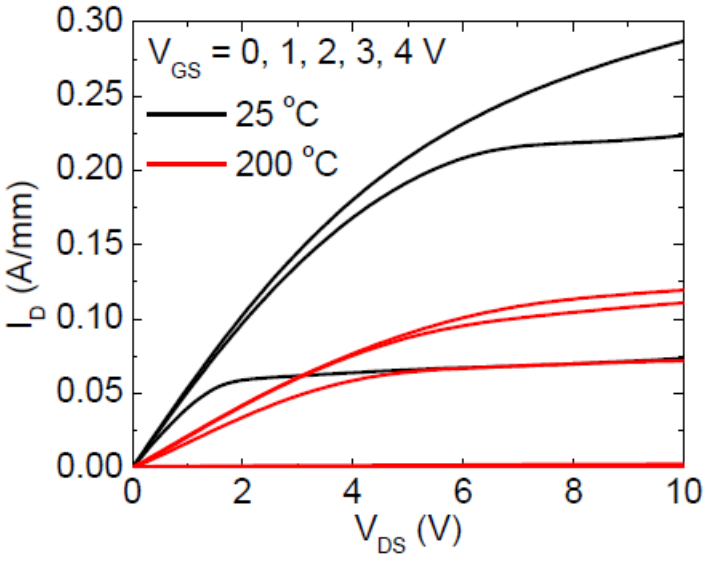


Figure 3.6. ID vs. VDS characteristics at 25 °C and 200 °C.

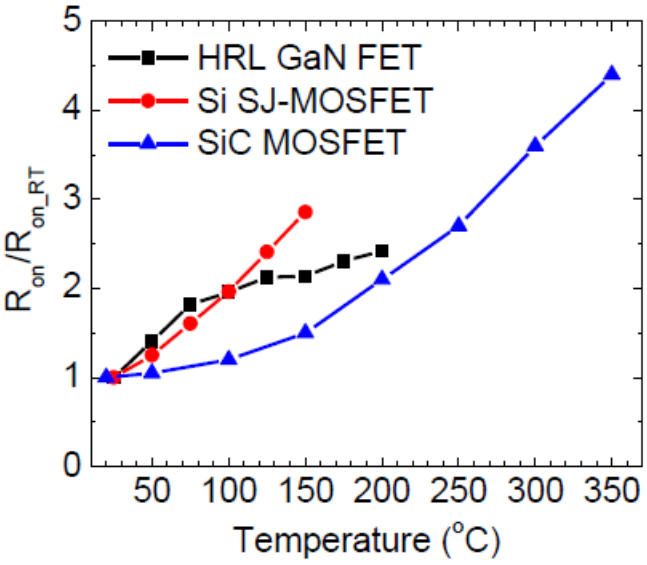


Figure 3.7. Dependence of on-resistance on temperature.

Figure 3.8 and figure 3.9 shows off-state leakage characteristics at 25 °C and 200 °C, with the substrate biased at 0 V. All leakage components were low up to 600 V of drain bias. To our knowledge, this is the first time a normally-off GaN transistor capable of

blocking 600 V at 200 °C is reported. The gate leakage is about 100 times lower than the drain leakage, attesting to the high quality of the gate insulator. The substrate-to-drain current is a major contributor to the total leakage, which can be further reduced by increasing the thickness of the GaN epi-layer.

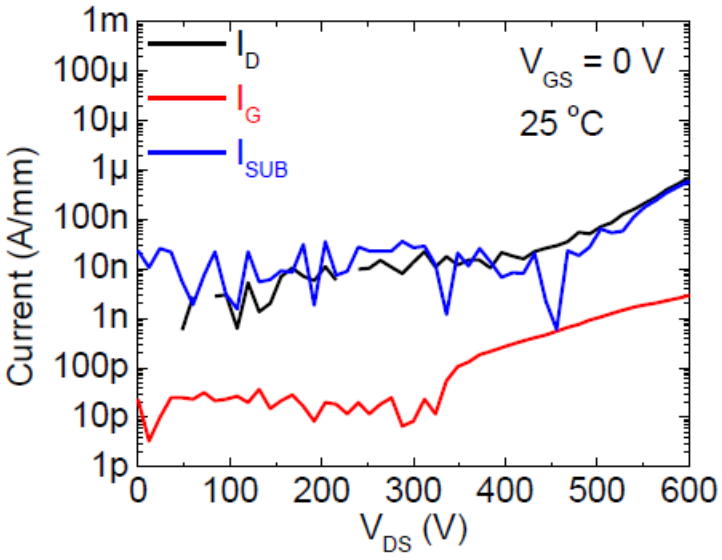


Figure 3.8. Off-state leakage (drain current, gate current, and substrate current) vs. VDSas a function of drain bias measured at 25 °C.

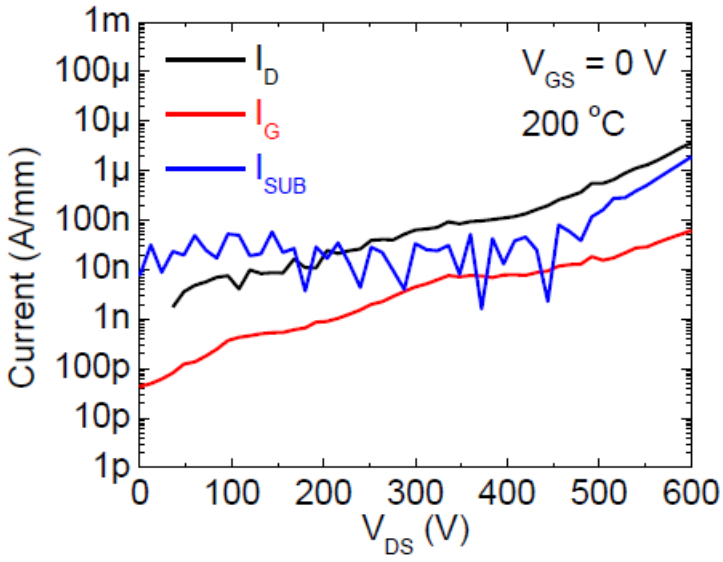


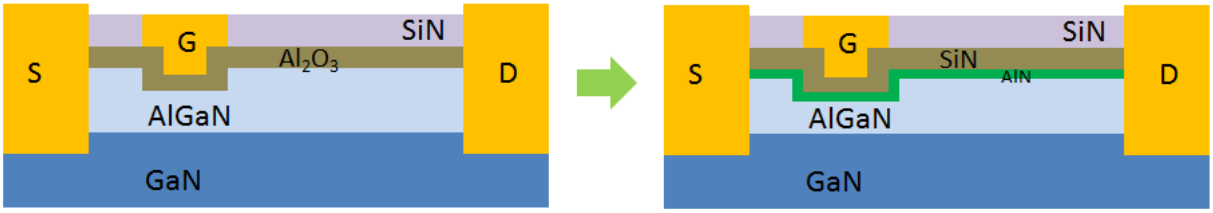
Figure 3.9. Off-state leakage (drain current, gate current, and substrate current) as a function of drain bias measured at 200 °C.

3.3 Second generation device fabrication and testing result

AlGaN/GaN transistors with multiple field-plates were fabricated on Si substrate. The gate length and the gate width are 1 µm and the 40 mm, respectively. Figure3.1(a) shows the cross-sectional schematic of the fabricated device. Different from the previous device structure, this device had no CF4 plasma treatment was used at the gate region. A AlN-based dielectric is used to replace the traditional Al2O3 was used as the gate dielectric. These modifications in gate structure resulted higher threshold voltage (Vth) from 0.6 V to 1.3 V . This new gate process also reduced the oon-resistance (RON) from 500 mohm to 350 mohm. The maximum drain current (ID_MAX) also increased from 5.5 A to 10.5 A which is shown in figure 3.10. The maximum gate bias also increased from +3 to +6V. These performance improvements are attributed to the superior quality of the AlN-based

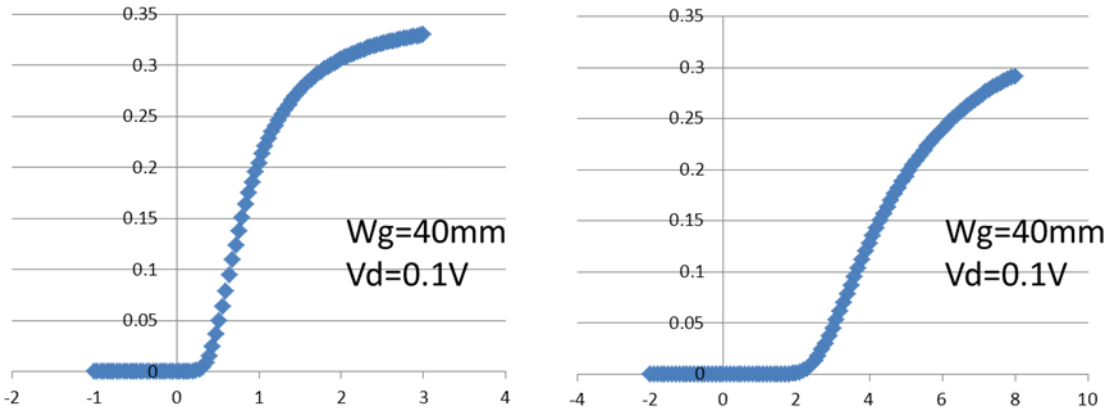
gate dielectric. When the gate to source bias is 0 V, the device can block 600 V with drain and gate leakage currents (IDSS and IGSS) of 40 μA and 10 nA, respectively. These data confirm the device has the desired normally-off feature for safe operation. The quality of the gate dielectric was further characterized by measuring the hysteresis in transfer curves and the stability of device characteristics during a positive gate bias stress. Figure 3.11(a) shows negligible hysteresis in transfer curves between the up and down gate bias sweeps. Figure 3.11(b) plots the R_{ON} and gate leakage current (IG) as a function of the positive gate bias stress time. No noticeable change in RON or IG was observed during the 20-hour gate bias stress at +6 V. Transfer curves before and after the gate bias stress were compared and plotted in figure 3.12. No shift of threshold voltage was observed. The absence of hysteresis as well as the stable device behaviors during the positive gate bias stress suggests the promise of the AlN-based dielectric as the gate insulator for GaN transistors. The switching performance of the GaN-on-Si transistors was evaluated in a half-bridge boost converter circuit shown in figure 2.12. Both the upper and the lower switch consisted of six 40-mm transistors connected in parallel. The GaN-on-Si transistors, gate drivers, and capacitors were assembled with extra care to minimize the parasitic inductance in the power loop. When the converter was operated at a switching frequency of 200 kHz, an input voltage of 200 V, an output voltage of 400 V, and an output power of 1 kW, a conversion efficiency of 97.4% was measured. Figure 3.14(a) plots the measured waveform of the drain-to-source voltage (VDS) across the lower switch. Figure 3.14(b) shows a close-up of the turn-on edge of the VDS waveform. The turn-on time was 1.2 ns; and the peak slew rate was 325 V/ns. This is a more than 2X improvement over the previously reported best value of 140 V/ns (Ref. 2). We attribute this

improvement to the larger VGS_MAX, the lower RON, the higher ID_MAX, as well as the low-inductance circuit assembly.

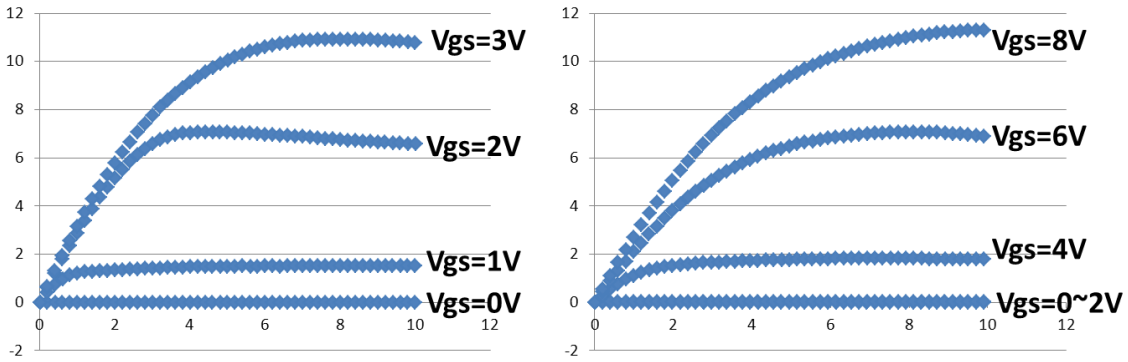


(a) (b)

Figure 3.10. (a) First generation device: 16nm AlGaN barrier with Al_2O_3 gate dielectric (b) Second generation device: 5nm AlGaN Barrier with hybrid gate dielectric

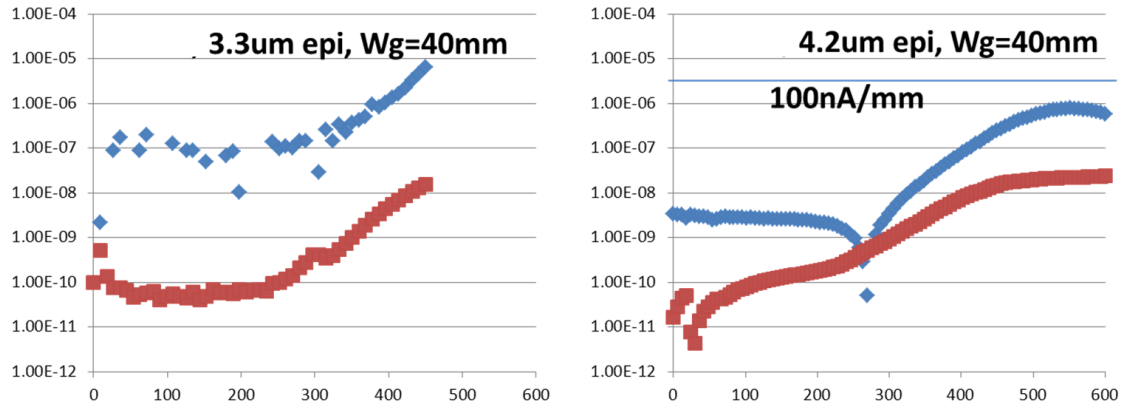


(a) (b)



(c) (a)

Figure 3.11. (a) Transfer IV characteristics for gen 1 device; (b) Transfer IV characteristics for gen 2 device; (c) output IV characteristics for gen 1 device; (d) output IV characteristics for gen 2 device.



(a) (b)

Figure 3.12. (a) Off-state breakdown characteristics of a Gen1 device; (b) Off-state breakdown characteristics of a Gen2 device.

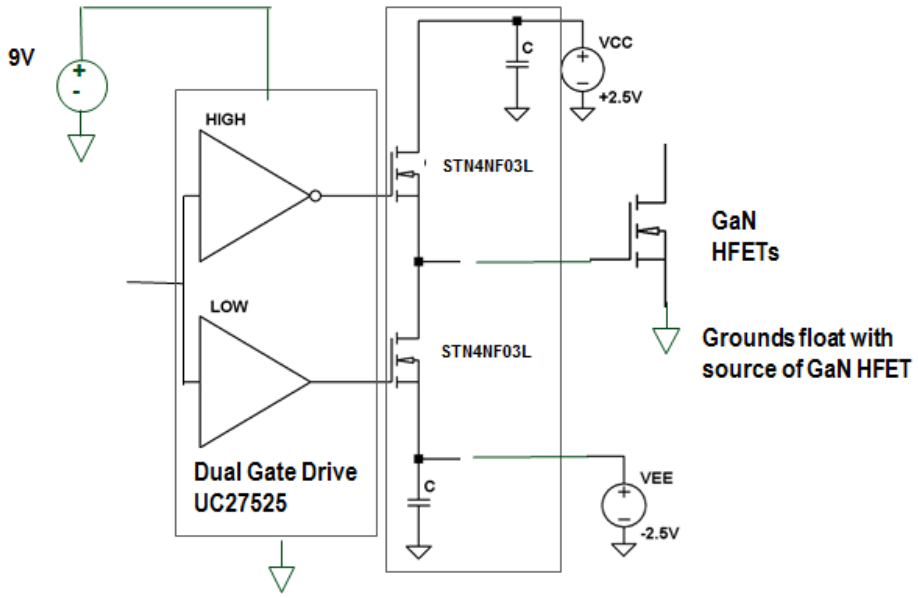


Figure 3.13. Circuit schematic of the half-bridge boost converter used for switching characterization of the fabricated GaN-on-Si transistors

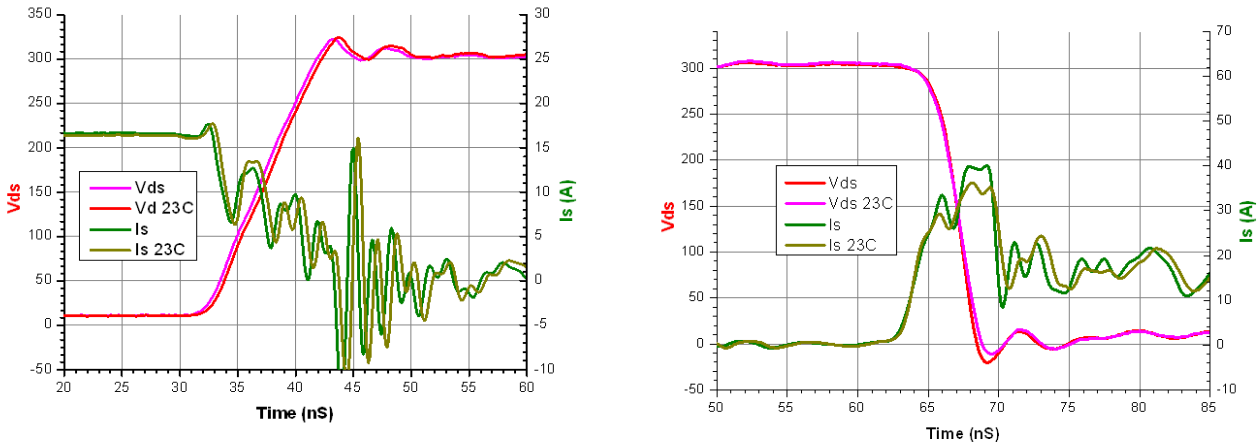


Figure 3.14. (a) Turn-on and turn-off waveform of half-bridge GaN switch at 300V and 16A at room temperature

Chapter 4

Gate Module Process improvement

4.1 ALE etch for normally off operation

A 2D cross-section view of the AlGaN/GaN MOS-HEMT of HRL's GaN-On-Silicon technology is shown in figure 2.1. The device is a hybrid between a HEMT structure and an MOS structure. A positive threshold voltage is achieved by introducing fluorine ions and forming a recess in the AlGaN barrier in the channel region and by the appropriate choices of the gate dielectric thickness, gate metallurgy and process conditions of the gate module.

The starting material is a group III-Nitride epitaxy stack that consists of a nucleation layer, thick III-Nitride buffer layer and AlGaN barrier/GaN Cap layers grown on a 3" Silicon wafer by heteroepitaxy using the MOCVD method. The process starts with patterning the device isolation region followed by high dose ion implantation to remove the 2DEG charge outside the active region.

This is followed by source and drain Ohmic metallization using Ti/Al/Ni/Au stack followed by a brief 860oC anneal. Thereafter, a Si3N4 film is deposited for passivation using the PECVD method. Gate definition step followed by nitride etch, fluorine treatment and gate recess etch using a digital O_2-BCl_3 Atomic Layer Etching (ALE) scheme as described in [20], to implement a normally-off operation. This is immediately followed by Atomic Layer Deposition (ALD) of Al_2O_3 as the gate insulating film followed by gate metal deposition and patterning. A key step is the rapid thermal anneal (RTA) process that is inserted within the gate module process and is performed at 400oC

for 5 minutes to reduce the trap density at the interface between the Al2O3 film and AlGaN surface. Further back-end metallization and intermetallic dielectric evaporation/ deposition steps are performed to realize a low resistance interconnect network and complete the 3-step field plate structure for electric field shaping.

4.2 Experiment design and testing results

A design-of-experiment (DOE) was constructed to study the impact of the following two critical steps on device parameters; 1) the number of ALE cycles used to etch the AlGaN barrier to recess the gate region and 2) the insertion point of the dielectric RTA step in the gate module process flow. A total of 6 identical wafers were split into two main groups to study the impact of the RTA step on device parameters, one group had the RTA step inserted immediately after the Al_2O_3 ALD step while the other group had the RTA step done after gate metal deposition. Each of the two groups had in turn three variations of the ALE number of cycles which were chosen to be 5, 7 and 9 cycles as summarized in Table I below. The device parameters that are used to assess the response to these two steps are gate leakage (Ig_leak) at V_{GS}=2.5V, on-state resistance (Ron) at VGS=2.5V, maximum drain current (Imax) at V_{GS}=3V and V_D=10V and threshold voltage (V_{th}) at Id=10 μA/mm and V_D=0.1V.

Wafer ID	ALE Cycles	RTA after ALD
A	5	Yes
B	5	No
C	7	Yes
D	7	No
E	9	Yes
F	9	No

TABLE II, Summary of the design experiment

Statistical data of measured Process Control Monitors (PCMs) were generated for key device parameters by testing identical devices with gate periphery of 600 μm which have a unit cell design similar to the large gate periphery device (50A device). The testing involved a sample size of 30 reticles across the 3" wafers.

The aforementioned key device parameters were analyzed to study the impact of both the ALE number of cycles and the RTA process sequence on device performance and to arrive at optimized process conditions. Threshold voltage for the 6 wafers, shown in figure 4.2, highlights the dependence on the number of ALE cycles. The data show that a minimum thickness of AlGaN barrier needs to be removed before the channel is switched off. It will require at least 7 ALE cycles (wafer C) to arrive at a positive Vth. The higher the number of cycles the more positive Vth is. However, increasing the number of ALE cycles to move to more positive Vth values is not without constrains as it turns out there is an upper bound on the number of ALE cycles which is imposed by the extent of degradation of Imax, Ron and Ig_leak with the increase of ALE cycles as shown in

Figure 4.4, Figure 4.5 and Figure 4.6, respectively.

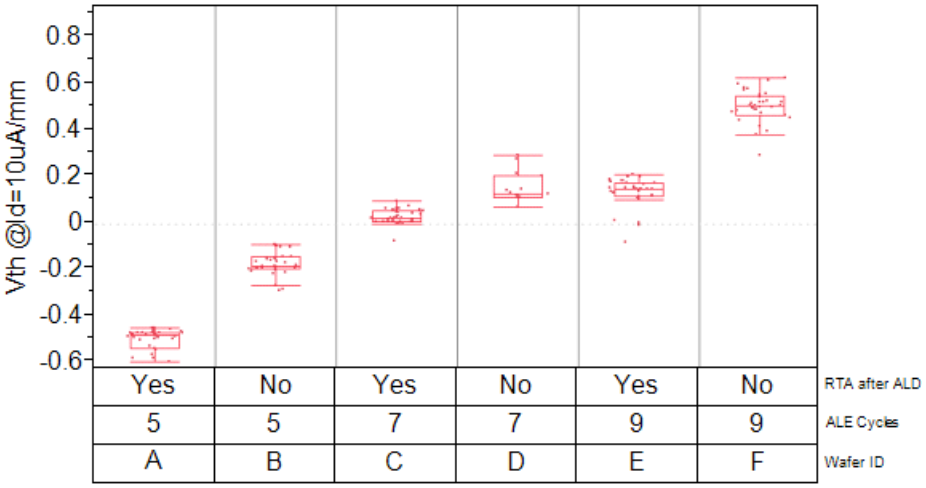


Figure 4.1.Statistical data of Vth of 600 μm MOS-HEMT

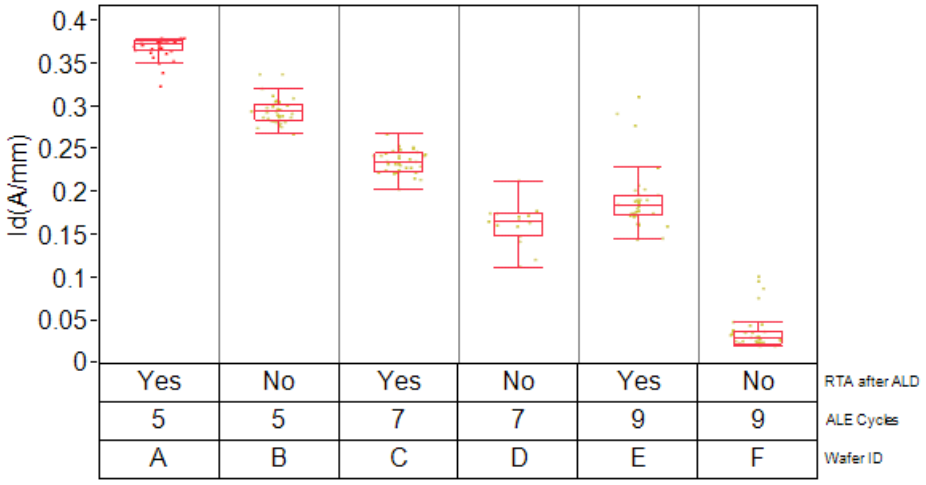


Figure 4.2.Statistical data of Imax of 600 μm MOS-HEMT

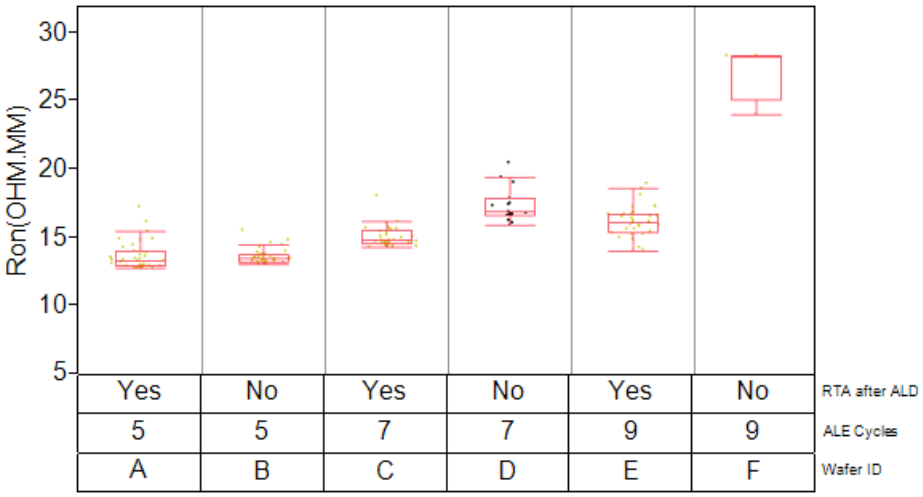


Figure 4.3 Statistical data of Ron of 600 µm MOS-HEMT

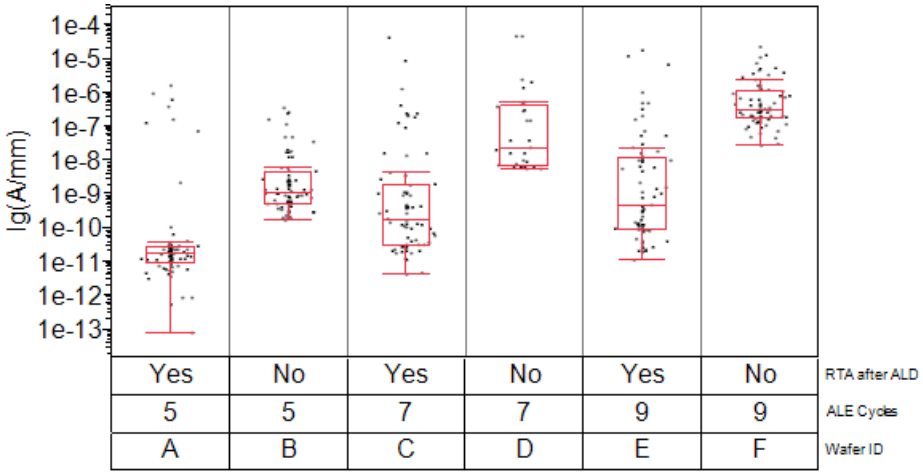


Figure 4.4 Statistical data of Ig_leak of 600 µm MOS-HEMT

The on-state (Imax and Ron) degradation is mainly attributed to the rough interface at the bottom of the gate recess which is moved closer to the gate channel as the ALE number of cycles increases. The scattering of channel carriers at this rough interface is responsible for channel mobility degradation.

A low gate leakage current, which is a critical parameter for device robustness and reliability of GaN- based device and is a prerequisite to implement a large gate periphery

device, is highly dependent on the gate stack composition and the process used to implement it.

The correlation between both the numbers of cycles, the gate dielectric anneals sequence and gate leakage current can be seen in figure 4.6. The gate leakage at positive gate voltage increases if the number of ALE cycles increases and if the RTA step was done after the gate metal deposition.

For a normally-off device, it is important to ensure that gate leakage remains low at a relatively high positive VGS up to at least 3V since a higher gate voltage drive is required for lower Ron and faster switching time. This requirement, which can be met by thickening the gate dielectric, presents a design challenge since it has been shown that increasing Al2O3 thickness to reduce gate

leakage and to improve gate integrity results in shifting the flat-band voltage, and in turn the threshold voltage, to a more negative value [21]. Other gate dielectric such as the high-K HfO2 deposited with ALD has a positive shift in the flat-band voltage with increasing film thickness and is a potential candidate but still suffers at the present time from high interface trap density of the order of 1013 cm-2. Therefore, engineering the gate module to simultaneously achieve a positive Vth and low gate leakage at high positive gate voltage without degrading the on-state performance becomes a challenge.

For HRL's recessed gate structure, the insulating gate dielectric can be thought of as a composite stack made up of the Al2O3 film plus the portion of the AlGaN barrier that remains after the gate recess step, in other words the remaining AlGaN under the gate supports a portion of the voltage drop appearing between the gate electrode and the

2DEG layer, hence reducing the electric field in the Al2O3 film. The reduction of the gate leakage as a result of larger AlGaN thickness under the gate, as seen in Figure 4.4, is attributed to enhanced immunity to Fowler Nordheim tunneling across the composite insulating gate stack.

The TEM images shown in figure 4.5 are taken for samples from an earlier but related experiment where two devices, one with 6 cycles of ALE and the RTA step performed prior to the gate metal deposition, and the second is for a device with 8 cycles and RTA performed after gate metal deposition. Key device parameters Vth, Ron, Imax and Ig-leak followed the same trends as the 6 wafer experiment. The images reveal that the 6 cycle wafer has a remaining layer of AlGaN under the Al2O3 whereas the 8 cycle wafer had almost no AlGaN remaining. The images also show that the gate metal/Al2O3 has a rough interface for the 8 cycles sample where the RTA was done after gate metal deposition whereas no roughness at that interface is observed on the 6 cycles sample where the RTA was done prior to metal deposition. The electrical results and the cross section differences between the two samples confirm the observations and conclusions extracted from the 6 wafer experiment.

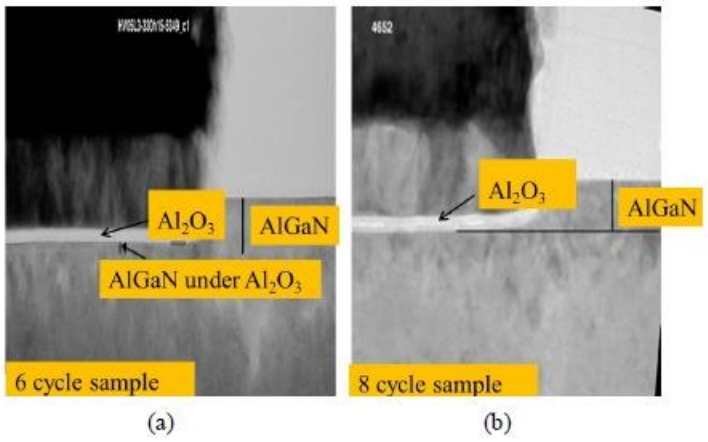


Figure 4.5.TEM images of the gate region: (a) sample with 6 ALE cycles and (b) sample with 8 ALE cycles

Chapter 5

Conclusions

Two processes of the gate module of an AlGaN/GaN MOS-HEMT were identified as critical to device robustness and performance. It was found that the gate recess process should be designed to allow a minimum thickness of the AlGaN barrier to reduce gate leakage current and reduce channel mobility degradation at the rough interface between the Al2O3 gate dielectric and AlGaN in the channel. It was also observed that it is more favorable to perform the dielectric anneal process prior to depositing the gate metal to reduce gate leakage currents and improve on-state performance for a given positive gate voltage. Optimizing the gate module processes has enabled the implementation of a low leakage 50A/600V MOS-HEMT with a positive Vth.

In conclusion, we have demonstrated a normally-off GaN on-Si field-effect transistor capable of high-temperature operation. Our results suggest that the GaN technology is promising for efficient power switching with reduced cooling requirements.

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