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Author

Kirsten, Frederick A.

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Frederick A. Kirsten

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CAMAC SPECIFICATIONS*

Frederick A. Kirsten Lawrence Berkeley Laboratory University of California

Summary

The experience with CAMAC installations resulting from its widespread use has inevitably led to suggestions for changes in the specifications. The NIM and ESONE Dataway Working Groups spent nearly a year discussing these suggestions during the recently completed process of rewriting and revising the CAMAC specifications. Some of the suggestions were included in the revised specification after careful evaluation of any compatibility problems that might arise. Others were felt to lie outside the intended scope of the specification.

In the following, the scope and intent of the CAMAC specification is briefly discussed. Then the significant additions and changes to the Dataway specification are listed, along with some background information. Reference is also made to the information contained in the document "Supplementary Information on CAMAC System."

Introduction

One result of the widespread adoption and use of CAMAC has been an accumulation of experience with the system. Although CAMAC, as originally specified, has worked very successfully, experience showed that certain additions, revisions and clarifications in the CAMAC Specification could be beneficial. The working groups charged with the responsibility for maintaining the specification spent about a year deliberating these changes, always keeping in mind the extreme importance of maintaining compatibility of CAMAC components built before and after any specification change. As a result of this work, two new documents have recently been issued in the United States and in Europe. One is a revised Dataway specification, the other is a revised Branch Highway specification.²

To augment the Dataway and Branch Highway specifications, a third document, "Supplementary Information on CAMAC System" has been prepared and is now being issued. It is intended to present information on the implementation and interpretation of the specifications, as well as preferred practices and current applications. It will be issued in the U.S. as TID-25877 and printed in Europe as part of the CAMAC Bulletin.

This paper is primarily concerned with a discussion of the additions and changes made to the Dataway specification during its revision, and with those portions of the Supplementary Information that concern the Dataway. It gives some background on certain of the changes and discusses the expected uses of some of the new features. The reader is also referred to Appendixes F and G of the Supplementary Information. Appendix F discusses the compatibility aspects of many of the changes. Incidentally, it points out that there are very few cases where any significant compatibility problems will arise, where CAMAC components -- modules, crate controllers, branch drivers-made before and after the changes are used together. Appendix G of Supplementary Information lists the changes that have been made in the Branch Highway and Crate Controller A Specification since the preliminary version was issued in November 1970.

How Far Does the Specification Go?

Before looking at the details of the revision, it may be useful to review briefly what is, and what is not, included in the CAMAC specification. A well-designed specification must effect a compromise between under- and over-specification. It should specify completely all the basic operational details but leave sufficient flexibility that it may be used in diverse applications. The user should have to concern himself mainly with what it does, not with how it works.

At the risk of oversimplification, one may say that the user thinks of CAMAC in terms of its mechanical and electrical, hardware and software aspects. (Here, hardware is used in the computer sense -- i.e., representing the hard-wired electronics that performs individual, predetermined operations, as opposed to programmable operations often performed by software. This usage of "hardware" looks a bit strange when in the same sentence with "mechanical," but it is a common usage.) In each of these aspects, the CAMAC specifications contain some mandatory requirements that must always be followed. There are also descriptions of optional features, which, if used, must satisfy the mandatory requirements. There are recommended features and practices. There are certain areas which are deliberately not covered, and left to the discretion of the designer or the user. One of the problems of the user, therefore is realizing what he must know in order to assemble a working system.

Mechanical and Electrical

It is clearly a fundamental requirement that any plug-in** should be mechanically compatible with any crate. The mechanical aspects of the specification therefore rigidly specify the shapes and dimensions of plug-ins and crates such that mechanical compatibility is guaranteed.

It is also fundamental that it should be possible to use any plug-in in any crate without electrical damage and that all plug-ins should get all necessary signals and supply voltages. These are electrical aspects which, again, are completely specified in CAMAC.

Hardware and Software

In the context of this paper, the term hardware is used to encompass the capability of modules and system controllers (e.g., computers) to interact with each other on a operation-by-operation or cycle-by-cycle basis. Software is used to describe the medium that connects together sequences of individual operations to make a system do a useful task. The division between hardware and software is fuzzy, because in CAMAC, as in other data handling systems, many sequences can be executed by either hardware or software. In essence, however, the term hardware represents the capability

*This work was done under the auspices of the U.S. Atomic Energy Commission.

**In CAMAC parlance, a plug-in is a unit that may be inserted into a crate. Plug-ins that occupy the control station are called "crate controllers";

those that occupy a normal station are "modules."

to transfer "words" between module and controller, and software represents the ability to carry out conversations using these words.

The specification is sufficiently complete that the ability to transfer "words" is assured when a CAMAC system is assembled. However, the conversations to be carried out are necessarily applicationdependent, hence are generally not mentioned in the specification. Therefore, the CAMAC user generally need not concern himself with the mechanics by which words are transferred. But he must concern himself with which words are to be transferred. He must know which commands (function codes and sub-addresses) are used in the modules he uses, and the operation in the module that each command causes to happen. He must know the Look-at-Me (LAM) characteristics, if any, of the module. These include the significance of a LAM, the commands that enable and disable the LAM, and how it is reset. He must know which commands elicit a Q-response, and the significance thereof. He must know whether one of the O-controlled block transfer modes (Address Scan, Repeat and Stop modes) is implemented, and whether the computer interface to CAMAC is equipped to perform these block transfers in hardware.

It is therefore important that the data sheets that describe CAMAC modules, crate controllers, and Branch Drivers clearly inform the user about the conversational properties of these components.

How the Changes and Additions are Discussed

The following sections roughly follow the aforementioned categories--mechanical, electrical, hardware and software. Each section contains the significant additions or changes made in revising the Dataway specification. It also includes any relevant comments contained in the Supplementary Information. References are given to the related paragraphs in the Dataway specification and in the Supplementary Information. The references with letter prefix (e.g., K5.4.1b) refer to Supplementary Information.³ Those without latter prefix (e.g., 5.4.1) To the Dataway Specification TID-25875, EUR-4100e (1972).

Since the largest part of the CAMAC specification is concerned with the hardware aspect, it is convenient to subdivide it into Dataway signals and Dataway codes. Under Dataway signals one considers the qualities or definitions and conventions of signals used in the communication between crate controller and module. In this context, the crate controller is considered a slave or repeater without any power of interpretation. The interpretive and directive power is contained in the system controller, which usually includes a computer. For the purposes of this paper the system controller bridges the hardware-software boundary. It speaks to the modules, through the crate controller, in terms of combinations of signals called codes. Thus, under Dataway codes, one considers the definitions and conventions of the codes used in the communication between system controller and module.

Mechanica1

Most of the mechanical specifications are in Section 4 of TID-25875. It has been rewritten extensively to improve on the clarity of the presentation. The associated figures 1-8 have been redrawn and have minor corrections. No changes have been made that in any way affect mechanical compatibility of old and new crates and plug-ins.

Chamber. The new Fig. 5.3 shows that the allowable chamfer on the printed connector of the plug-in has been reduced to lxl mm from 1.5x2.5 mm. The Supplementary Information recommends that it be no more than 0.1x0.1mm. The reduction helps prevent inadvertent connector misalignment as modules are inserted into crates. This is especially important to prevent damage if modules are inserted with power on.

Coaxial connectors. In the NIM edition of the Dataway specification, the reference to the use of BNC coaxial connectors has been dropped. Reference is made only to the Lemo-type connectors, which have now been designed Type 50-CM. Specification drawings for these connectors are available.

Multi-pin connectors. The Supplementary Information recommends three specific types of multi-pin connectors for front and rear panel use. It also makes recommendations on cable construction of cable assemblies for these connectors.

Panel markings. The Supplementary Information recommends panel markings for coaxial connectors which will enable the user to distinguish whether the signals associated with the connector are TTL levels or NIM levels. It also recommends that the power supply voltage and current markings be listed on the front panel of each plug-in.

Electrical

Pin assignments. Two modifications in the Dataway connector pin assignments have been made. The X line, which was previously Reserved, has now been designated Command Accepted. The use of this signal is discussed later. Pins Pl through P5 of each normal station were previously designated individual patch contacts available for non-standard uses. Now Pl and P2 of all normal stations are designated Free bus-lines (Section 5.6.1), and are now joined by two bus-lines. Pins P3 and P5 at normal stations, and P1-P7 of the control station remain as patch contacts. The Free bus-lines were created to facilitate the busing of non-standard signals to or from modules. Because these signals are non-standard and somewhat unpredictable, it is required that modules using Pl or P2 have a means of disconnecting from these two contacts.

Power supplies. The voltage tolerances (Table X) for the $\pm 12V$ and $\pm 24V$ power supplies have been changed from $\pm 0.5\%$ to $\pm 1.0\%$. This latter figure more accurately represents the tolerance limits that can be expected to be delivered to plug-ins with standard power supplies.

The Supplementary Information recommends that plugin designers should avoid the use of $\pm 12V$, 200 V dc and 117V ac. The $\pm 24V$ voltages should be used instead of $\pm 12V$ whenever possible. Light-emitting diodes are displacing gaseous-discharge indicators, relieving the need for 200 V dc. The 117V ac voltage is very infrequently needed, and presents a shock hazard to the unwary. Discouraging the use of these voltages in modules helps to minimize the number of individual voltage supplies that are needed on the crates. For example, the typical CAMAC power supply CP-1, described in Appendix E of Supplementary Information, delivers only $\pm 6V$ dc and $\pm 24V$ dc.

Signals on Coaxial Connectors. Supplementary Information (Section K4.2.5c) recognizes that CAMAC terminated (NIM fast) signals on coaxial connectors may sometimes be designed to be terminated external to

the module. This is particularly useful where signals are supplied to a number of modules in a "daisy chain." A standard panel marking is recommended to indicate when coaxial inputs are not terminated inside the module.

Dataway signals

A few changes were made in the rules by which crate controllers and modules exchange signals.

Voltage and current levels for Dataway signals (Table VI). The presentation of the table has been rearranged, and there are several changes in the numbers, none of which should affect compatibility.

Critical attention was given to the very important strobes S1 and S2. Since many control and data transfer operations depend on them, it is essential that the timing and integrity of the strobes be preserved.

It has been found that in many crates, the recovery times of the strobe signals are longer than specified in Fig. 9 of the Dataway Specification. This was apparently because the capacity on these lines together with the pull-up resistors resulted in RC time constants that were too large. The stretching of S1 and S2 that results from this condition could lead to abnormal operation. For example, a register addressed by a Read and Clear command—F(2)—could be prematurely cleared if the stretched S2 from a previous command cycle extends into the beginning of Dataway cycle for the F(2) command.

In order to reduce the recovery time of the strobes, the pull-up currents for these two signals have been increased to approximately 40 mA. The lower value of pull-up resistors necessary to supply this current also helps reduce the cross-talk from other signals onto S1 and S2.

The current that a module may draw from its N line has been increased from 1.6 mA to 3.2 mA. This is possible since the controller must supply at least 6.4 mA, and usually only one module is connected to each N line. This change was introduced to facilitate up-dating older modules for the new L-gating requirements, or to make them usable in systems that utilize the X-response.

Timing of Dataway cycles and signals. The original Dataway specification required that all L (Lookat-Me) signals be gated off the Dataway whenever a command cycle was in progress--i.e., whenever B(Busy) was present. The intention of this provision was to prevent cross-coupling from L signals (which could otherwise spontaneously change from '0' to '1' during command cycles) from interfering with the command underway. However, gating by B means a Dataway command addressed to any module causes the L signals from all modules to disappear. This tends to degrade the speed of recognition of demands for attention. Experience shows that it is not difficult to design a Dataway such that the crosscoupling is negligible. It is therefore not necessary to gate the L signals because of the danger of crosscoupling. However, it is still necessary to retain some gating because of certain signal delays on the Branch Highway. The requirement was therefore changed to require L signals to be gated off the Dataway only during those command cycles that result in the L signal being removed.

As an illustration of the new gating requirements, consider a simple module in which the following

commands are implemented:

N-F(0)-A(0)	Read the Register and Reset LAM status
N·F(8)·A(15) N·F(9)·A(0)	Test LAM Clear the Register
N·F(10)·A(0)	Reset LAM status Enable LAM
N·F(26)·A(0) N·F(24)·A(0)	Disable LAM

In this module the LAM status is set (and L generated) whenever the register is ready to be read. Therefore, when the register is read via F(0), the LAM status is reset, since the action requested by the L was executed. According to the changed rule for L gating, the module must be designed so that L is gated off whenever the L signal will be cancelled by the current command. This can be done in various ways. Either of the following satisfies the requirements; the latter is simpler, but the former interferes less with the L signal:

L=LAM status· $N\cdot A(0)\cdot [F(0) + F(10) + F(24)];$

or

 $L= LAM status \cdot \overline{N}$

When it is remembered that the old rule would have required L=LAM status B, it can be seen that many older modules can easily be modified to conform to the revised specification by replacing B with N.

The cycle timing for the unaddressed commands, C(Clear) and Z(Initialize), are now specified in detail (Section 7.1.3.2 and Figure 10).

A minimum rise and fall time of 10ns for all Dataway signals has now been specified (Section 7.1). This figure was chosen to permit the use of "normal" TTL integrated circuits, while excluding faster types such as Schottky TTL. Signal transition times that are too short can result in excessive amounts of cross-coupling and ringing on the Dataway lines. This minimum rise and fall time now applies to all signals, including Inhibit.

 $\frac{\text{Dataway signal definitions.}}{\text{area are the definitions of the Command Accepted signal and the busing of two patch contacts to create two Free bus-lines. Both these changes are discussed in other sections.}$

- 1. Full decoding of F and A (Sections 5.1.2 and 5.1.3). It is now explicitly stated that all five F lines and all four A lines must be used by a module in decoding the Function code and the Sub-address code. This has always been good practice, and has been done in the majority of designs. The intent is to insure that the module will respond only in the manner the user expects. For example, if a data sheet says that a module responds to F(0) in a certain way, then it should respond only to F(0) in that way. However, if the module uses only F1 and F2 to decode F(0)—ignoring F4, F8, F16—then the module responds to all F codes for which F1=F2=0. This includes not only F(0), but also F(4), F(8), etc.
- 2. Initialize. (Section 5.5.1). It is now stated that Initialize is intended to be used during system start up. This puts it in the same category as a Power Clear or Reset I/O command on many computers. It forces the system into an orderly state such that it can accept and obey the further commands necessary to make it do its tasks. It is a much more powerful

signal than Clear, since the registers and bistables that are acted on by Clear are at the discretion of the designer or user. Initialize, on the other hand, is required to set all data and control registers to a defined initial state. This means that the designer must specifically consider every data and control register and decide what initial state it should have during system start-up. This initial state should obviously be one that requires no immediate action by the controller, hence it is required that all LAM requests be disabled by Initialize. It is also now required that the Inhibit signal be put in the I=1 state during the Initialize cycle, and, if Inhibit is controlled by a flip-flop, held there until reset. (There may be cases where Inhibit is controlled by an externallysupplied signal.)

Usage of Dataway Codes and Signals.

The previous section discussed some of the individual signal lines and their significance. During a Dataway operation, groups of these signals can be combined or coded in many different ways. This section discusses some of the changes in the defined usages of various of these codes and signal combinations.

Function code definitions. The set of available function codes has been improved by providing for some very useful operations. It now has four bitmanipulating codes and a code which can be used to trigger any monostable type of operation in a module.

1. Selective set and clear (Sections 6.3.3, 6.3.4, 6.3.5, 6.3.6, and Table IV). One very useful change to the specification is the definition of four Write function codes designed to manipulate individual bits in the addressed registers. The two Selective Set commands, F(18) and F(19), will set the bits in the addressed register that correspond to the 1's in the data word carried with the command. The data word 0's cause no action. F(18) is used with Group 1 registers, and F(19) with Group 2. These two Function codes were previously defined as Selective Overwrite, Group 1 and Group 2, in which a separate mask determined which of the bits in the data word were written into the addressed register. Since the Selective Overwrite commands were very rarely used, very few problems are expected because of the change in definition.

The two Selective Clear command codes, F(21) and F(23), were previously Reserved codes and therefore have not been used. Hence, no downward compatibility problems exist. These commands result in resetting the bits of the addressed register that correspond to 1's in the data word. The data word 0's cause no action.

An example of the use of these commands is given in the paragraphs on the Look-at-Me signal. As another example, consider a 24-bit register, in which each of the 24 bits is used to control the state (e.g., on or off) of a separate external device. By using the Selective Set and Clear commands, the appropriate software routine can send commands to a particular device without needing to know the states of the other devices. In effect, therefore, these commands permit the addressing of up to 24x15=284 one-bit registers in Group 1 and 284 in Group 2.

2. Execute, F(25) (Section 6.4.2). This command code was previously named Increment Preselected Registers, and had a definition that fit its name.

The definition has now been expanded to include a wide variety of operations. It may now be used to initiate or terminate any "one-shot" action in a module. It may not be used to initiate actions which require another command to terminate them, or vice-versa.

Module responses Q, L and X. The scope of the defined actions for Q and L has been expanded. A new X-response signal has been defined.

1. Q-response (Section 5.4.3). The size of Section 5.4.3 has been increased, partly by consolidating Q-related material from other sections, and partly because of the descriptions of the new block transfer modes.

The section now carries the statement that the O response must be clearly defined for each function code and subaddress used by the module. This should help to relieve O of the misplaced desires of some designers to have it be the universal module response signal. (The X signal has been defined to accomplish this task.)

The Address Scan mode (Section 5.4.3.1) is identical to the sequential addressing process described inSections 6.1 and 6.3 of the 1969 specification. It has simply been moved to a new location and given a new name. It is hoped the new language will remove the erroneous impression that all Read and Write registers must have the sequential addressing properties. This was not intended, although the readers of the 1969 version often gained that impression.

There are now three block transfer modes that can use the Q response to control the block transfer algorithm. In addition to Address Scan, there are the newly defined Repeat and Stop modes.

The Repeat mode is useful for block transfers in which the addressed register may not always be ready to transfer. If an attempt is made to access that register when it is not ready, it signals the system controller by returning Q=0. This is an invitation to the controller to try again. It presumably will try again and keep trying until it gets a Q=1 response. It considers that the transfer has been acomplished successfully only on those cycles where a Q=1 is obtained. The Repeat mode is most attractive where the addressed register becomes ready within just a few Dataway cycles. Otherwise, an excessive amount of Dataway time may be spent just in finding out that the register is not ready.

Since Q carries only a single bit of information, it can be used to control only one block transfer mode at a time. The module designer must clearly specify which mode, if any, is used for which operation. It also means that the modes cannot be mixed. For example, it might be useful to allow a register to use both Stop and Repeat modes so that it could transfer a block of undetermined length in which the next word is not always immediately available. However, this is not presently possible.*

*Some installations⁵ are utilizing one of the Free bus-lines to carry a signal called Hold. Together with Q, this can simulate combined Stop and Repeat or Address Scan and Repeat modes. 2. Look-at-Me signal (Section 5.4.1). Section 5.4.1 has been extensively rewritten. The new requirement that L be gated by a logic term that includes N has already been discussed. It is now mandatory to include an F(8) command for testing the state of the L signal. It is now forbidden for a module to spontaneously reset its own L source. This must be done only as a result of a Dataway command.

The most significant addition to Section 5.4.1 is the provision for improving access to the registers used in multi-source LAM logic structures. Although each (single-width) module has only one Look-at-Me connection to the control station, many modules have several sources from which requests for attention may come. When such a module raises its Look-at-Me flag, owing to a request from one or another of these sources, the system controller must usually determine which of the sources within the module originated the request in order to know what action to take. This is done by directing to the module appropriate Dataway commands asking for further information. For this purpose, the 1969 version discussed only commands--such as F(8). Test Look-at-Me--in which a single-bit response is given via the Q line. This necessarily means that only one source can be interrogated for each Dataway cycle. The sources are interrogated in turn by subaddressing; a complete search requires as many Dataway cycles as there are sources.

The 1972 version also describes a second method in which up to 24 sources can be interrogated in a single cycle. The collection of sources is considered to be a register. The state of up to 24 sources can be determined by a Read operation in which each bit of the data word carries the state of one source. The improvement in speed should be obvious.

Both methods of accessing are also used for other purposes in LAM operations, for example, enabling, disabling, resetting, etc. Figure 1 shows an example of multi-source logic in which the access is via sub-addresses. Figure 2 shows an example of accessing via databits. In Fig. 2, note the use of the Selective Set and Clear commands, which were discussed earlier.

Figure 3 is included to show that the LAM logic for a module with single L source can be relatively simple.

Note in all three figures that the Test Lookat-Me command has been assigned sub-address A(15). Although sub-addresses can be chosen arbitrarily, there is an advantage to uniformity, particularly to writers of software. The uniformity that is suggested is to assign the same sub-address to the various function codes associated with a given LAM source. Thus the command for Test LAM Source 0 will be F(8) A(0). Test LAM Source 1 will be F(8)A(1), etc. Interference with this pattern is minimized if the Test LAM command is assigned to the highest subaddress, F(8)A(15).

3. Command Accepted, X (Section 5.4.4). This new module response signal was created because of the needs of system designers and computer programmers for a uniformly defined response from the addressed module. The Q response proved to be inadequate for this purpose because it was defined only for certain commands such as the Test Look-at-Me command, or Read commands intended to be executed in the Address Scan mode. Section 5.4.4, which defines the Command

Accepted signal has a curious characteristic. It has a mandatory definition for the meaning of X=1, but a non-mandatory definition of the meaning of X=0. It says that a module must generate X=1 if it is able to execute the command. Note that it is permissible in certain cases to include the readiness of equipment external to the module in the decision as to whether it is able to execute the command. For example, a command intended to turn on a control motor may not be executable if the motor is not powered. In this example it would be permissible to return X=0.

The non-mandatory definition for X=0 says it should indicate a serious malfunction which needs to be brought to the attention of the operating system. It was decided that making this a mandatory definition would be too restrictive, since the inverse of "able to execute the command" is serious to a greater or lesser degree depending on the particular system. However, the intention is to provide a uniform, automatic means of detecting a malfunction--in hardware or software--at the instant that the command is generated.

It is expected that computer interfaces will provide for various ways of monitoring the X-line which can be chosen according to the application. These ways will include: immediately interrupting the computer; setting a status bit that can be software tested; or disabling the X-line response entirely. The Supplementary Information points out (Section L4.2.3) that non-catastrophic X=0 signals will be "generated" when addressing an old module that has no X-response built in.

A response of X=0 will also be received when performing certain Address Scan operations. (Section K5.4.4b). In executing the Address Scan algorithm, the controller finds it has accessed all the desired registers in a given module when it receives a Q=0 response. However, it receives this response only when it addresses the first register location beyond the Address Scan sequence. If this location is vacant (it need not be vacant; it is only required that it give a Q=0 response), then it must also respond with X=0. Therefore an X=0 in this context does not indicate a malfunction. It is also a normal occurrence in executing an Address Scan algorithm to address an empty station. Here again, X=0 does not indicate a malfunction.

In most other operations however, an alarm upon addressing an empty station is desirable. The station may be empty because the module was mistakenly removed, or there may have been a software error which directs a command to the wrong place. It was for this reason that X=0 was chosen to be the alarm condition. It requires that old modules be updated to avoid giving an alarm, but it has the valuable property of giving a signal when an empty station is addressed.

4. The Group 1/Group 2 controversy. The 1969 version provided for two sets of registers known as Group 1 and Group 2 without making any distinction between them. The 1972 version improves on this slightly by saying (Section 6) "Information concerning status or system organization or requiring restricted access, should be held in Group 2 registers." One intent of this statement is to encourage that ordinary data registers be located in Group 1 and to encourage that registers concerned with the control of the module be in Group 2.

Certain subaddresses in Group 2 have been recommended for designated status registers. These are:

A(15)	Module Characteristic	(Section	6)	
A(14)	LAM Request Register	(Section	5.4.1.2)	į
A(13)	LAM Mask Register	("	")	į
A(12)	LAM Status Register	("	")	

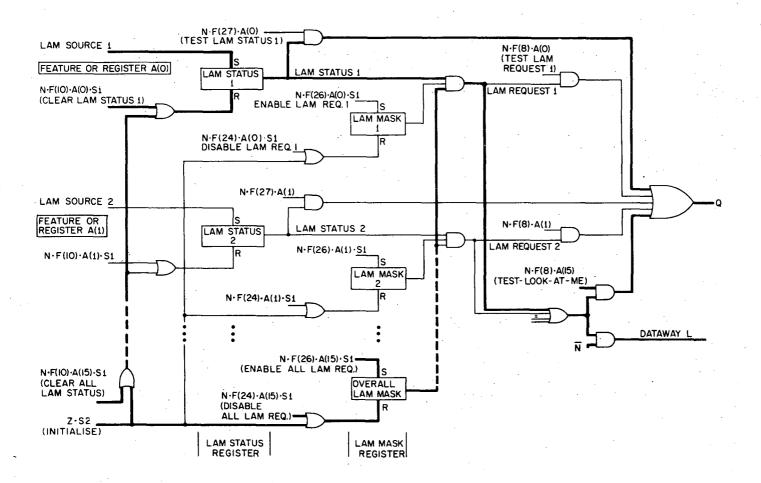
The module characteristic is intended to contain information on the characteristic(s) of the module. This could conceivably include module model number, number of registers, word size, etc., although no standards are given in the specification.

Acknowledgments

One of the unsung heroes of the CAMAC specifications is R.C.M. Barnes of A.E.R.E. Harwell, England. Mr. Barnes has worked tirelessly on the language of the documents, and their clarity and precision is a tribute to his perseverance. Credit should also be given to the members of the ESONE and NIM Working Groups who have spent long hours discussing the various points of the revision.

References

- The revised CAMAC Dataway specification has been issued by the U.S. AEC NIM Committee as TID-25875, and by the European ESONE Committee as EUR 4100e (1972). The content of both documents is identical. The NIM edition is:
 - "CAMAC A Modular Instrumentation System for Data Handling-Revised Description and Specification," TID-25875, United States Atomic Energy Commission, Washington, D.C., (July 1972).
- The CAMAC Branch Highway and Crate Controller Type A specification has been issued by the U.S. AEC NIM Committee as TID-25876, and by the European ESONE Committee as EUR-4600e (1972). The content of both documents is identical. The NIM edition is:
 - "CAMAC Organization of Multi-Crate System, Specification of the Branch Highway and CAMAC Crate Controller Type A," TID-25876, United States Atomic Energy Commission, Washington, D.C., (March 1972).
- 3. The Supplementary Information will be issued by the U.S. AEC NIM Committee as TID-25877, and will also be published by the European ESONE Committee. The NIM edition is:
 - "Supplementary Information on CAMAC Instrumentation System," TID-25877, United States Atomic Energy Commission, Washington, D.C.
- R.C.M. Barnes, "The Revised CAMAC Specification EUR 4100e (1972)," CAMAC Bulletin, Issue No. 4, July 1972, pp6-8.
- F. Iselin, B. Lofstedt, P. Ponting, "CAMAC Dataway-Branch Highway Timing Relationship via the Crate Controller," CAMAC Bulletin, Issue No. 3, March 1972, pp7-8.



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Figure 1. An example of the logic structure in a module for handling Look-at-Me (LAM) signals originating from several sources. The sources of these demands for attention are located in other parts of the module. In this example, the flip-flops and logic gates associated with each source are controlled by commands which are steered by the accompanying sub-address.

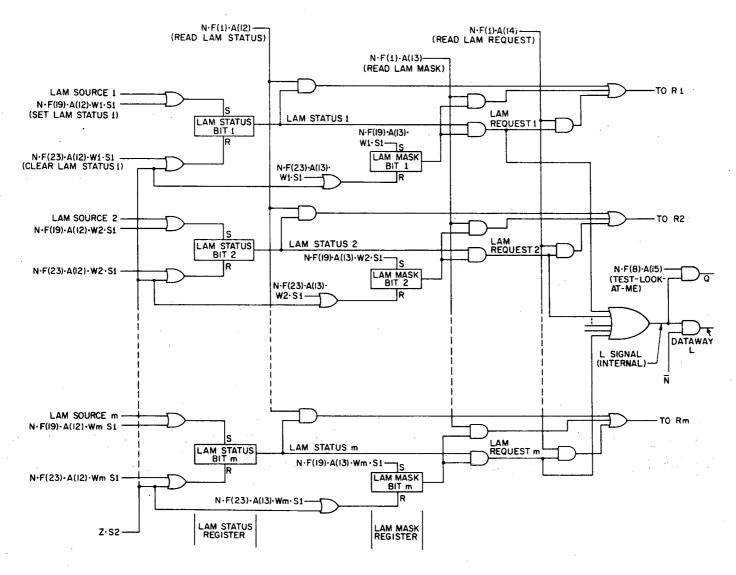


Figure 2. Another example of Look-at-Me logic for a module with several LAM sources. In contrast to Fig. 1, many of the commands in this example are steered by the bits in the accompanying data word. For example, the Selective Set command N.F(19). A(13) will set LAM Mask bit 1 if bit 1 (W1) of the accompanying data word is '1'. The same command also sets LAM Mask bit 2 if W2=1, etc. The setting is done at the time Strobe S1 arrives.

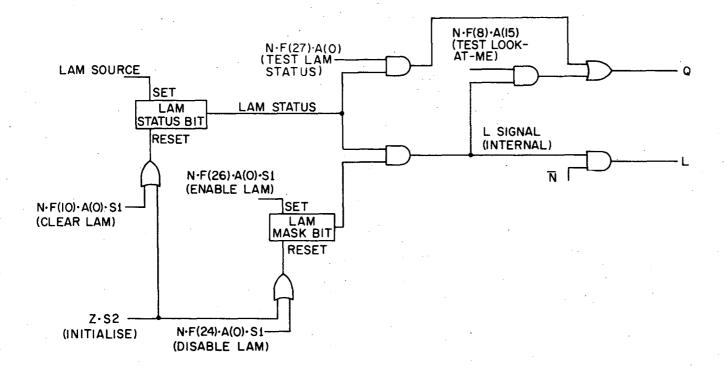


Figure 3. Many modules have only a single source of Look-at-Me demand. In such cases the associated logic can be relatively simple as compared to Figs. 1 and 2. This is an example.

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TECHNICAL INFORMATION DIVISION LAWRENCE BERKELEY LABORATORY UNIVERSITY OF CALIFORNIA BERKELEY, CALIFORNIA 94720