UNIVERSITY OF CALIFORNIA, SAN DIEGO

High Power Millimeter-Wave Signal Generation in Advanced SiGe and CMOS Process

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Hsin-Chang Lin

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Professor Peter Asbeck
Professor James F. Buckwalter
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Professor Brian Keating

2015

The dissertation of Hsin-Chang Lin is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

University of California, San Diego

2015

DEDICATION

To my parents, Bo-Chuan and Shu-Ching.

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Chapter 2 is based on and mostly a reprint of the following paper:

- H.-C. Lin and G. M. Rebeiz, "A 70-80 GHz SiGe Amplifier with Peak Output Power of 27.3 dBm", submitted for publication in *IEEE Transactions on Microwave Theory and Techniques*, Sept. 2015.

Chapter 3 is based on and mostly a reprint of the following paper:

- H.-C. Lin and G. M. Rebeiz, "A 110-134 GHz SiGe Amplifier With Peak Output Power of 100-120 mW", *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 12, pp. 2990-3000, Dec 2014.

Chapter 4 is based on and mostly a reprint of the following paper:

- H.-C. Lin and G. M. Rebeiz, "A 200-230 GHz SiGe Multiplier with Peak Output power of 5-8 dBm", submitted for publication in *IEEE Transactions on Microwave Theory and Techniques*, Oct. 2015.

Chapter 5 is based on and mostly a reprint of the following papers:

- H.-C. Lin and G. M. Rebeiz, "A 135-160 GHz balanced frequency doubler in 45 nm CMOS with 3.5 dBm peak power", *IEEE Int. Microwave Symp. Dig.*, pp. 1-4, June 2014.
- H.-C. Lin and G. M. Rebeiz, "A 200-245 GHz Balanced Frequency Doubler with Peak Output Power of +2 dBm", *IEEE Compound Semiconductor*

Integrated Circuit Symp., pp. 1-4, Oct. 2013.

The dissertation author was the primary author of the work in these chapters.

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Y. Yang, S. Zihir, H. Lin, O. Inac, W. Shin, and G. M. Rebeiz, "A 155 GHz 20 Gbit/s QPSK transceiver in 45nm CMOS", *IEEE Radio Frequency Integrated Circuit Symp.*, pp. 365-368, June 2014.

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H.-C. Lin and G. M. Rebeiz, "A 135-160 GHz balanced frequency doubler in 45 nm CMOS with 3.5 dBm peak power", *IEEE Int. Microwave Symp. Dig.*, pp. 1-4, June 2014.

K.M.-J. Ho, H.-C. Lin, and G. M. Rebeiz, " Improving 3G/4G receiver sensitivity (TIS) using antenna impedance matching networks", *IEEE Int. Microwave Symp. Dig.*, pp. 1-3, June 2014.

H.-C. Lin and G. M. Rebeiz, "A 200-245 GHz Balanced Frequency Doubler with Peak Output Power of +2 dBm", *IEEE Compound Semiconductor Integrated Circuit Symp.*, pp. 1-4, Oct. 2013.

Y. Yang, H. Lin, S. Zihir, O. Inac, W. Shin, and G. M. Rebeiz, "A 155 GHz 20 Gbit/s QPSK transceiver in 45nm CMOS", *IEEE Transactions on Microwave Theory and Techniques*, to be submitted 2015-2016.

ABSTRACT OF THE DISSERTATION

High Power Millimeter-Wave Signal Generation in Advanced SiGe and CMOS Process

by

Hsin-Chang Lin

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California, San Diego, 2015

Professor Gabriel M. Rebeiz, Chair

This thesis presents a fully-integrated 16-way power combining amplifier for 67-92 GHz applications in an advanced 90 nm silicon germanium (SiGe) HBT technology. The 16-way amplifier is implemented using 3-stage common-emitter single-ended power amplifiers (PAs) as building blocks, and reactive λ/4 impedance transformation networks are used for power combining. The 3-stage single PA breakout has a small-signal gain of 22 dB at 74 GHz, and saturated output power (P_{sat}) of 14.3-16.4 dBm at 68-99 GHz. The power-combining PA achieves a small-signal gain of 19.3 dB at 74 GHz, and P_{sat} of 25.3-27.3 dBm at 68-88 GHz with a maximum power added efficiency (PAE) of 12.4%.

The 16-way amplifier occupies 6.48 mm^2 (including pads) and consumes a maximum current of 2.1 A from a 1.8 V supply. To our knowledge, this is the highest power silicon-based E-band amplifier to-date.

Next, a fully-integrated 8-way power combining amplifier for 110-134 GHz applications in an advanced 90 nm silicon germanium (SiGe) HBT technology is presented. The 8-way amplifier is implemented using 4-stage common-emitter single-ended power amplifiers (PAs) as building blocks, and reactive $\lambda/4$ impedance transformation networks are used for power combining. The single-ended PA breakout has a small-signal gain of 20 dB at 116 GHz, and P_{sat} of 12.5-13.8 dBm at 114-130 GHz. The 8-way power combining PA achieves a small-signal gain of 15 dB at 116 GHz, and P_{sat} of 20-20.8 dBm at 114-126 GHz with a power added efficiency (PAE) of 7.6-6.3%. The 8-way amplifier occupies 4.95 mm^2 (including pads) and consumes a maximum current of 980 mA from a 1.6 V supply. To our knowledge, this is the highest power silicon-based D-band amplifier to-date.

Also, a fully-integrated 4-way power combining multiplier for 200-230 GHz applications in an advanced 90 nm silicon germanium (SiGe) HBT technology is presented. The 4-way combined multiplier is implemented using active balanced transistor pairs with device size of $4\times6\times0.1$ μm^2, 4-stage pseudo-differential driver power amplifiers (PAs) as building blocks, and reactive $\lambda/4$ impedance transformation networks for power combining. The 4-stage single-ended PA breakout has a peak small-signal gain of 19.3 dB at 110 GHz, and a P_{sat} of 14.5 dBm at 116 GHz. The multiplier breakout results in a peak output power of 1.8 dBm at 245 GHz with a peak conversion gain of -15.5 dB. The power-combining multiplier achieves a peak output power of 8 dBm at 215 GHz with an associated conversion gain of -4.7 dB. The peak conversion gain is 1.6 dB at 215 GHz for 0 dBm output power. The 4-way combined multiplier occupies 3.63 mm^2 (including pads) and consumes a maximum current of 1.2 A from a 1.8 V supply. To our knowledge,

this work generates the highest power among all silicon-based technology to-date above 200 GHz.

Finally, high-power stand-alone millimeter-wave frequency multipliers in advanced SiGe and CMOS process are presented. First, a 135-160 GHz active doubler has been developed in 45 nm CMOS SOI. Careful optimization is done on the transistor size, layout and transmission-lines in order to result in the best performance. The doubler shows a measured peak power of +3.5 dBm at 150 GHz and $>$ 2 dBm at 140-160 GHz, at a bias voltage of 1 V. These were achieved at an input power of 7-8 dBm at 70-80 GHz, resulting in a conversion gain of -4 to -5 dBm. To our knowledge, these are the best results achieved for a D-band doubler in SiGe or CMOS, and shows that advanced CMOS technology can be used to generate wideband power above 100 GHz. Second, a wideband 90 nm SiGe BiCMOS frequency multiplier at 200-245 GHz is presented. The balanced multiplier results in a low first harmonic component, and uses a reflector at the base nodes to reflect the second harmonics to transistors for improved efficiency. The measured output power is $>$ -2 dBm at 200-245 GHz with a peak value of +2 dBm at 224-228 GHz and a conversion gain of -15 dB. To the author's knowledge, this is the highest power wideband doubler at 200-250 GHz.

Chapter 1

Introduction

1.1 Millimeter-Wave Applications

Millimeter-wave (30-300 GHz) systmes have been an active research topic in the past few years and significant progress has been made to enable complex systems to operate at these frequencies. For instance, millimeter-waves allows wireless communication systems such as 5G cellular at 30-40 GHz, IEEE 802.11ad/WiGig for WLAN at 55-65 GHz, and wireless backhaul at E-band (71-76, 81-86, and 92-95 GHz) to operate at high data rate due to the large achievable bandwidth. Another millimeter-wave application is in radar and image sensing. Due to the the high operating frequency, an antenna with high gain and small size can be achieved. Also, large bandwidth and short wavelength allow such systems to have high spatial resolution for object recognition. For example, automotive radar systems at 79 GHz shows better spatial resolution than radar systems operating at lower frequencies (Fig. 1.1).

Furthermore, with the advance of the semiconductor technology, high data-rate point-to-point communication systems [1, 2, 3, 4, 5], high-resolution radars [6, 7, 8] and imaging systems [9, 10, 11, 12, 13, 7, 14] at 120 GHz and 200-250 GHz (air-attenuation

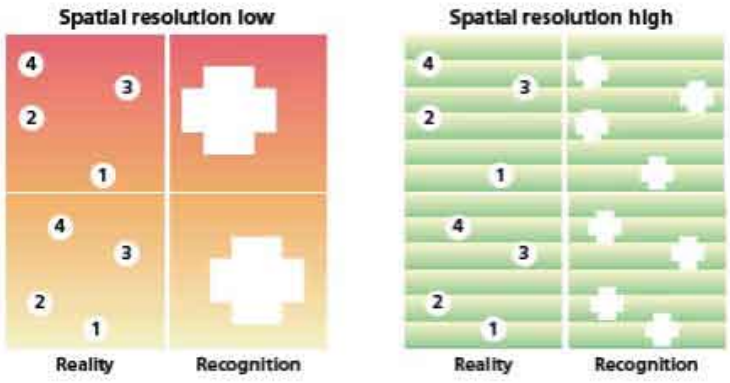


Figure 1.1: Millimeter-wave radar system has higher spatial resolution bandwidth.

gap) or even at THz (0.3-3 THz) have also been demonstrated.

All the systems mentioned above benefit from millimeter-wave applications. However, one key limitation for millimeter-wave systems is the limited transmitted distance. For a given amount of power, the shorter the wavelength, the shorter the transmission distance, and this is due to the high free space path loss at millimeter-wave frequencies. Therefore, this thesis addresses the short propagation-distance issue by increasing output power of the millimeter-wave systems. Power combining techniques using low-loss reactive combiners at 80 GHz and 120 GHz will be first presented. Then, an amplifier-multiplier chain using power-combining technique to generate a signal at 200-230 GHz will be presented.

1.2 Power Combining Techniques

Advanced CMOS and SiGe technologies have pushed their transistor cut-off frequency f_t and f_{max} up to 300-400 GHz and provide low-cost, high-yield and high-integration solutions for systems as mentioned above. However, the output power are still limited due to the scale-down of the transistor size and breakdown voltage. Therefore,

the generation of millimeter-wave signals with adequate power is essential for all high performance millimeter-wave applications.

One solution for the limited output power is on-chip power combining. Power combining techniques such as current combining [15, 16, 17, 18, 19] using Wilkinson combiners (Fig. 1.2(a)) or T-junctions (Fig. 1.2(d)), voltage combining [20, 21, 22, 23, 24] using transformer (Fig. 1.2(b)), spatial power combining [25, 26, 27] using on-chip antennas (Fig. 1.2(c)) are usually used to improve the output power at millimeter-wave frequency. However, as the number of the combining elements (or stages) increase, Wilkinson- and transformer-based techniques usually result in high combining loss. And, free-space combining requires on-chip antennas which typically have a radiation efficiency of 30-50% (3-5 dB loss)[28, 29, 30]. Also, free-space combining does not allow the silicon chip to be used as a driver for a higher-power III-V chip for increased system performance, or a driver for frequency multipliers for high power sources at THz frequencies.

This thesis focuses on reactively power-combining techniques based on $\lambda/4$ transmission-line networks. The $\lambda/4$ combining network is wide-band and low loss, and no extra transmission line is required for connecting the combining networks with the combining elements. The number of the combining elements have been demonstrated up to 16 at 80 GHz with the capability to scale up to 32 elements. This technique has been used at 70-80 GHz in Chapter 2, 110-135 GHz in Chapter 3, and 200-230 GHz at Chapter 4 and results in state-of-art output power at all these frequencies.

1.3 Millimeter-Wave Signal Generation

As mentioned above, there are many benefits for mm-wave wireless system. And, as we eagerly push up the operating frequencies, the generation of a millimeter-wave

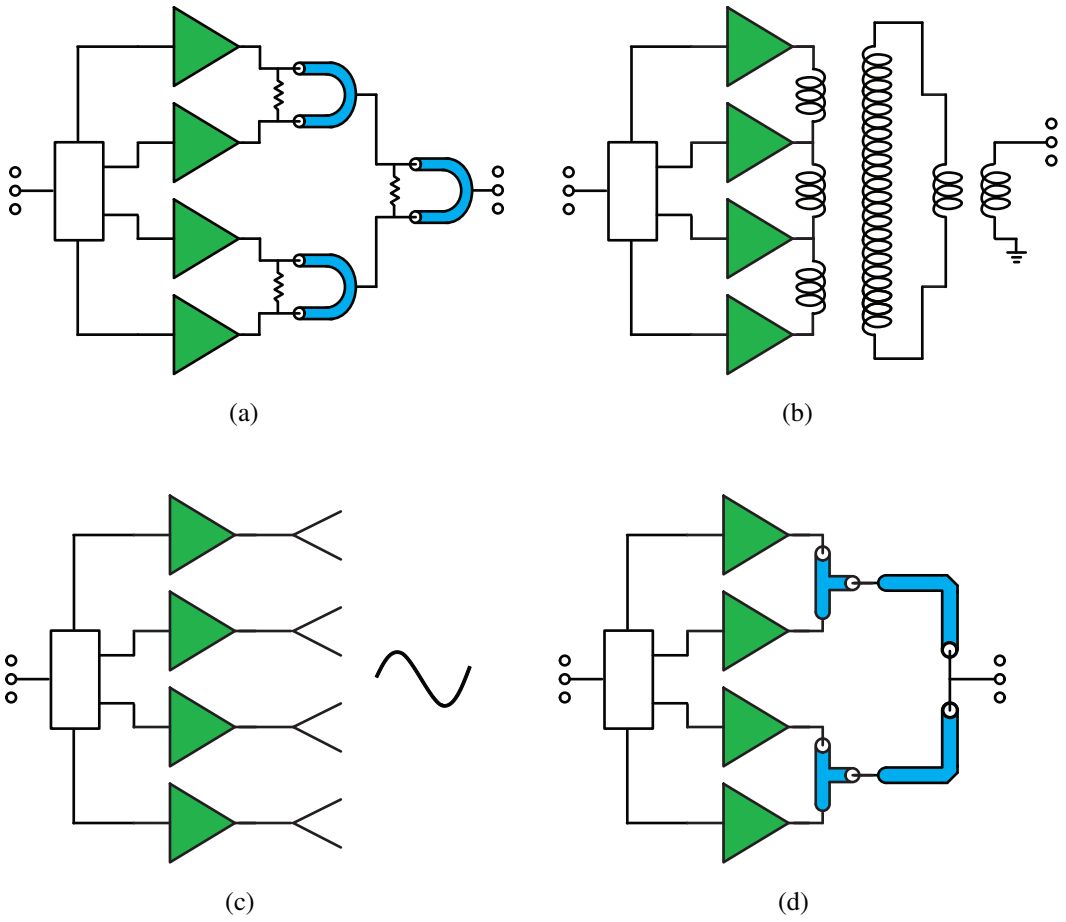
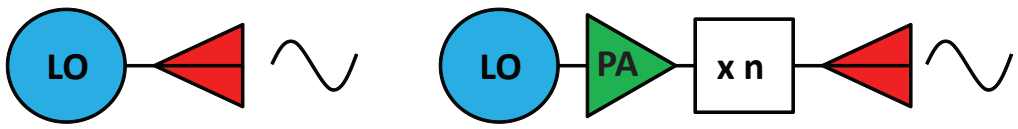


Figure 1.2: (a) Wilkinson, (b) transformer, (c) quasi-optical, and (d) reactive power-combining techniques .

signal plays a crucial role since the transistors are operating close to their f_t and f_{max} limits. There are two ways to generate signals at millimeter-wave frequencies: one directly uses a fundamental oscillator (Fig. 1.3(a)); another uses a fundamental oscillator at lower frequencies, and then power amplifiers and multipliers to generate a signal at the desired frequency (Fig. 1.3(b)). The millimeter-wave source using oscillators have been reported in [31, 32, 33, 34]. However, oscillators operating at high frequency usually suffer from poor phase noise (due to f_0 being close to f_t/f_{max}), limit output power (for f_0 $>$100 GHz), and narrow bandwidths. Furthermore, high frequency dividers are required to lock the free-running oscillator in this approach, which is very hard for f_0 $>$100 GHz.

For the amplifier-doubler approach [35, 36, 37], the oscillator operates at lower frequencies so a better phase noise can be achieved and dividers are also readily available. Besides, power amplifier at lower frequencies have sufficient power to drive frequency multipliers so as to provide wide-band and high-power signals at the desired mm-wave frequencies ($>$100 GHz).

Therefore, this thesis focuses on the amplifier-multiplier approach to generate wideband signals at millimeter-wave frequencies (60-250 GHz). Furthermore, power-combining techniques used to generate a signal with even more power will be introduced in Chapter 4.



(a) (b)

Figure 1.3: LO generation using (a) fundamental oscillator, and (b) oscillator at low frequency with power amplifiers and multipliers.

1.4 Thesis Overview

The thesis first presents high power amplifiers at 70-80 GHz and 110-135 GHz using reactive power-combining techniques. Next, an amplifier-doubler array at 200-230 GHz using reactive power-combining techniques are presented. Finally, stand-alone high-power frequency multipliers at 130-160 GHz and 200-245 GHz in advanced SiGe and CMOS technologies are presented.

Chapter 2 presents a fully-integrated 16-way power combining amplifier for 67-92 GHz applications in an advanced 90 nm silicon germanium (SiGe) HBT technology. The 16-way amplifier is implemented using 3-stage common-emitter single-ended power amplifiers (PAs) as building blocks, and reactive $\lambda/4$ impedance transformation networks are used for power combining. The 3-stage single PA breakout has a small-signal gain of 22 dB at 74 GHz, and P_{sat} of 14.3-16.4 dBm at 68-99 GHz. The power-combining PA achieves a small-signal gain of 19.3 dB at 74 GHz, and P_{sat} of 25.3-27.3 dBm at 68-88 GHz with a maximum power added efficiency (PAE) of 12.4%. The 16-way amplifier occupies 6.48 mm^2 (including pads) and consumes a maximum current of 2.1 A from a 1.8 V supply. To our knowledge, this is the highest power silicon-based E-band amplifier to-date.

Chapter 3 presents a fully-integrated 8-way power combining amplifier for 110-134 GHz applications in an advanced 90 nm silicon germanium (SiGe) HBT technology. The 8-way amplifier is implemented using 4-stage common-emitter single-ended power amplifiers (PAs) as building blocks, and reactive $\lambda/4$ impedance transformation networks are used for power combining. The single-ended PA breakout has a small-signal gain of 20 dB at 116 GHz, and P_{sat} of 12.5-13.8 dBm at 114-130 GHz. The 8-way power combining PA achieves a small-signal gain of 15 dB at 116 GHz, and P_{sat} of 20-20.8 dBm at 114-126 GHz with a power added efficiency (PAE) of 7.6-6.3%. The 8-way amplifier

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Chapter 4 presents a fully-integrated 4-way power combining multiplier for 200-230 GHz applications in an advanced 90 nm silicon germanium (SiGe) HBT technology. The 4-way combined multiplier is implemented using active balanced transistor pairs with device size of $4\times6\times0.1$ μm^2, 4-stage pseudo-differential driver power amplifiers (PAs) as building blocks, and reactive $\lambda/4$ impedance transformation networks for power combining. The 4-stage single-ended PA breakout has a peak small-signal gain of 19.3 dB at 110 GHz, and a P_{sat} of 14.5 dBm at 116 GHz. The multiplier breakout results in a peak output power of 1.8 dBm at 245 GHz with a peak conversion gain of -15.5 dB. The power-combining multiplier achieves a peak output power of 8 dBm at 215 GHz with an associate conversion gain of -4.7 dB and the peak conversion gain is 1.6 dB at 215 GHz. The 4-way combined multiplier occupies 3.63 mm^2 (including pads) and consumes a maximum current of 1.2 A from a 1.8 V supply. To our knowledge, this work generates the highest power among the silicon-based technology to-date at frequency above 200 GHz.

Chapter 5 presents a 135-160 GHz active doubler in 45 nm CMOS SOI. Careful optimization is done on the transistor size, layout and transmission-lines in order to result in the best performance. The doubler shows a measured peak power of +3.5 dBm at 150 GHz and $>$ 2 dBm at 140-160 GHz, at a bias voltage of 1 V. These were achieved at an input power of 7-8 dBm at 70-80 GHz, resulting in a conversion gain of -4 to -5 dBm. To our knowledge, these are the best results achieved for a D-band doubler in SiGe or CMOS, and shows that advanced CMOS technology can be used to generate wideband power above 100 GHz. Second, Chapter 5.2 presents a wideband 90 nm SiGe BiCMOS frequency multiplier at 200-245 GHz. The balanced multiplier results in a low

first harmonic component, and uses a reflector at the base nodes to reflect the second harmonics to transistors for improved efficiency. The measured output power is $>$ -2 dBm at 200-245 GHz with a peak value of +2 dBm at 224-228 GHz and a conversion gain of -15 dB. To the author's knowledge, this is the highest power wideband doubler at 200-250 GHz.

Chapter 2

A 70-80 GHz SiGe Amplifier with Peak Output Power of 27.3 dBm

2.1 Introduction

Silicon-based millimeter-wave (mm-wave) systems at E-band (71-76, 81-86, and 92-95 GHz) have been developed over the past few years for point-to-point multi-Gb/s communication [1, 38, 39, 2, 3] and automotive radar systems [40, 41, 42, 6, 7, 8]. Although advanced CMOS and SiGe technologies provide low-cost, high-yield and high-integration solutions for such systems, the transmit output power is still limited due to the scaling down in transistor sizes and lower breakdown voltages. Therefore, III-V technologies such as GaAs [43, 44, 45], GaN [46, 47, 48, 49] and InP [50, 51, 52] still dominate the power amplifier area at these frequencies despite of their relatively high cost.

Power combining techniques, such as voltage combining where transformers are used [20, 21, 22, 23, 24], current combining where the Wilkison combiners or T-junctions are used [15, 16, 17, 18, 19], and spatial power combing [25, 26, 27], are usually

employed to increase the output power of CMOS and SiGe technologies. Wilkison- and transformer-based power combining techniques result in relatively high loss when the number of combining elements increase, and the free-space power combining technique requires on-chip antennas which occupy large area on the chip and have a 40-55% radiation efficiency[25, 26, 27, 29, 30].

In this work, a 16-way reactively power-combined amplifier with low-loss λ/4 combining networks is presented (Fig. 2.1). The output combining network is based on λ/4 microstrip transmission lines with wide signal lines to achieve low-loss power combining. The simulated 16-way combining loss is 0.5-1.0 dB at 65-92 GHz when all the amplifiers are driven in phase. The amplifier unit cell is implemented using 3-stage common-emitter amplifier with a small-signal gain of 22 dB at 74 GHz. The 16-way power-combining amplifier results in a P_{sat} of 25-27.3 dBm at 68-88 GHz. Also, an 8-way combined PA using the same amplifier unit with λ/4 combining network is demonstrated. The 8-way power combined PA delivers a P_{sat} >21 dBm at 66-95 GHz with a peak value of 24 dBm at 72-80 GHz.

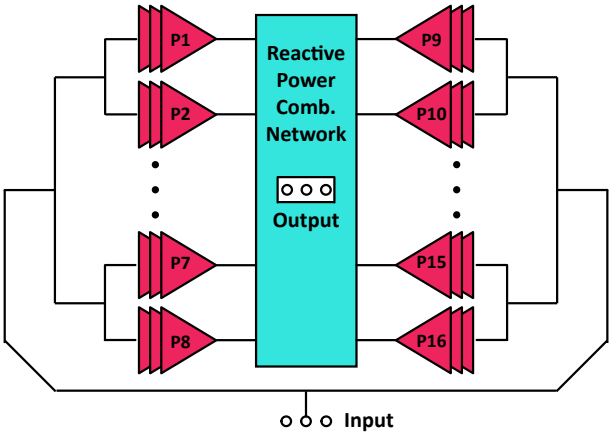
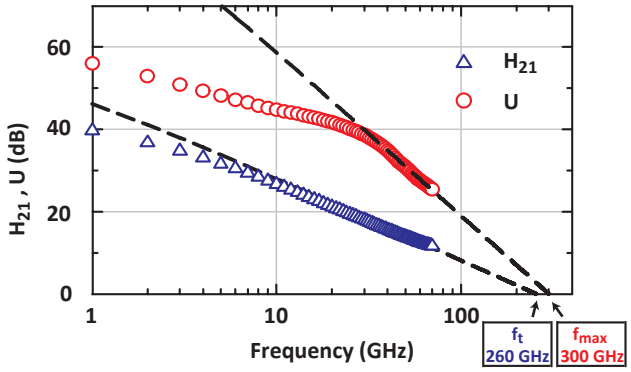


Figure 2.1: A 16-way reactive power-combined amplifier.

2.2 Technology

The 80 GHz PAs are designed using the IBM 9HP BiCMOS process [53]. It is a 90 nm SiGe HBT process built on top of a 90-nm CMOS process, with a 10-layer copper metal backend and high-density metal-insulator-metal (MIM) capacitors (12.2 fF/ μm^2). The 4×0.1 μm^2 transistor model with a single emitter finger, dual collector and base fingers (C-B-E-B-C) from the Cadence library results in a peak f_t/f_{max} of 310/350 GHz at 1.5-2.5 mA/μm bias current when referred to M1 [54]. However, when the interconnect parasitics from M2 to LD are taken into account for the collector and base fingers, and from M2 to M2_4B for the emitter finger, the peak f_t/f_{max} becomes 260/300 GHz (Fig. 2.2(a)). The emitter finger is connected to ground through higher-level metal, M2_4B, instead of lower level metal (M1-3) for reliability consideration and to pass electromigration rules. The interconnects for the 4×0.1 μm^2 transistor (Fig. 2.3(a)) are inserted into a full electromagnetic (EM) simulator (Sonnet EM suite)[55] and the extracted parasitic lumped elements are shown in Fig. 2.3(b). The interconnect parasitics are much better than CMOS transistors which typically reduce the f_t/f_{max} from 460 GHz (referred to M1) to 260 GHz (referred to top metal)[56]. The better performance is due to the all-copper back-end and the thick dielectrics used in the IBM 9HP process.

Fig. 2.4(a) presents the 50 Ω microstrip transmission lines used in this work with two different ground planes. The 10 μm wide transmission line (TL1) is implemented using the top metal LD and M2_4B, and is used in the PA cell for the matching stubs, resulting in a small area and compact layout. The 20 μm wide transmission line (TL2) implemented using LD and M3 is used in the input distribution and output combining networks, and has lower loss than TL1. EM simulations using Sonnet show a loss of 0.45-0.6 dB/mm and 0.28-0.38 dB/mm at 60-100 GHz for TL1 and TL2, respectively (Fig. 2.4(b)). The corresponding transmission-line Q is 24-30 and 39-48, respectively,



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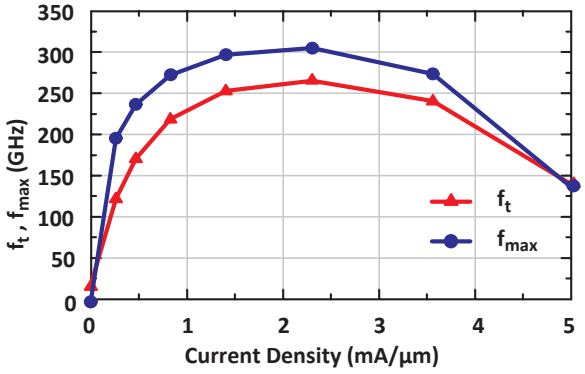
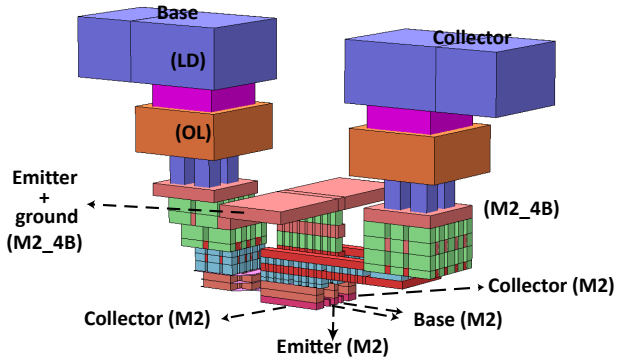


(b)

Figure 2.2: (a) Measured H_{21} and U at 2.2 mA/μm, and (b) f_t and f_{max} of 4×0.1 μm^2 transistor v.s. current density for IBM9HP.



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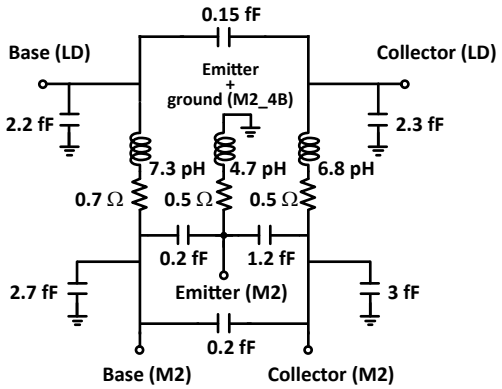
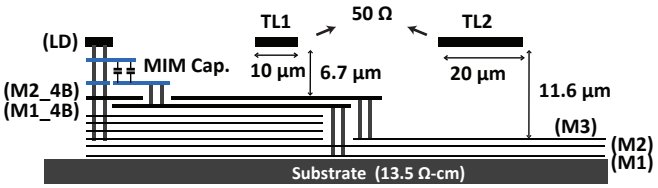


(b)

Figure 2.3: (a) Interconnections from M2 to top metal LD, and (b) lumped-element model for the interconnect parasitics from M2 to LD.



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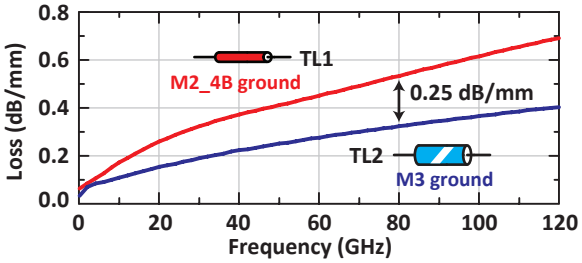


(b)

Figure 2.4: (a) 50 Ω microstrip transmission lines with M2_4B (TL1) or M3 (TL2) as ground plane, and (b) simulated loss.

at 60-100 GHz. In practice, and from different measurements done on IBM 8HP and other processes, the loss is about 20% higher than simulated. Still, a loss of 0.45-0.6 dB/mm and 0.28-0.38 dB/mm is taken for TL1 and TL2 in the Cadence and Sonnet simulations since there are no measurements yet in our group for this process at mm-wave frequencies.

2.3 Design

2.3.1 Single-Ended PA

The PA consists of three common-emitter gain stages biased in the class A region (Fig. 2.5(a)). The transistors are implemented by aggregating smaller, high-f_t npn standard cells. Transistors with dimensions of 4×0.1 or 8×0.1 μm^2 are used as the standard cells with C-B-E-B-C configuration, and each cell is surrounded by a deep-

trench isolation ring. The transistors are biased near their peak f_t current density at a quiescent current of 1.6 mA/μm. The first stage (Q1) consists of two parallel 4×0.1 μm^2 npn cells, while the second stage (Q2) is implemented using two 8×0.1 μm^2 npn cells connected in parallel. The output transistor (Q3) is implemented using four 8×0.1 μm^2 npn cells connected in parallel to form a 32 μm emitter-length device. The first-stage amplifier provides a small-signal gain of 9 dB at 80 GHz while the second- and third-stage provide a gain of 8-9 dB each. All amplifiers are driven by a single Vdd plane (1.7-1.8 V) distributed using M1_4B (0.81 μm) when TL1 is used and M1 and M2 when TL2 is used.

The EM simulation environment of the matching networks for the 80 GHz PA is shown in Fig. 2.5(b). The input matching, inter-stage matching, and output matching networks are implemented using LC-resonant circuits and are all modeled in Sonnet. Compact metal-oxide-metal (MOM) capacitors, implemented using the top metal LD to metal M1_2B, are used as series matching elements where DC-blocks are required. Inductors are implemented using shorted 50 Ω TL1 in different lengths. Customized MOM between LD and M1_2B capacitors are chosen over the process design kit (PDK) MIM and vertical-natural (VN) capacitors for impedance matching because they show a higher Q ($\sim$30) value than VN ($\sim$25) and MIM ($\sim$8) capacitors [16].

The Vdd stubs connected to the collector nodes are followed by dual 710 fF MIM capacitors which are operating close to self resonance and provide a very low impedance ($\sim$1 Ω) at 70-80 GHz. The M2_4B layer is used as a ground plane and the M1_4B layer is used as the Vdd plane for the Vdd stubs. Both ground and Vdd planes are "cheesed" to pass the metal density rule. A quarter-wavelength 50 Ω microstrip line is used at the Q3 collector as a RF chock [57], which presents an open circuit ($>$ 500 Ω) to the low impedance collector node ($\sim$10 Ω), and eases the implementation of the output matching network.

The PA design overcomes the technology's 1.7 V BVceo (breakdown voltage,

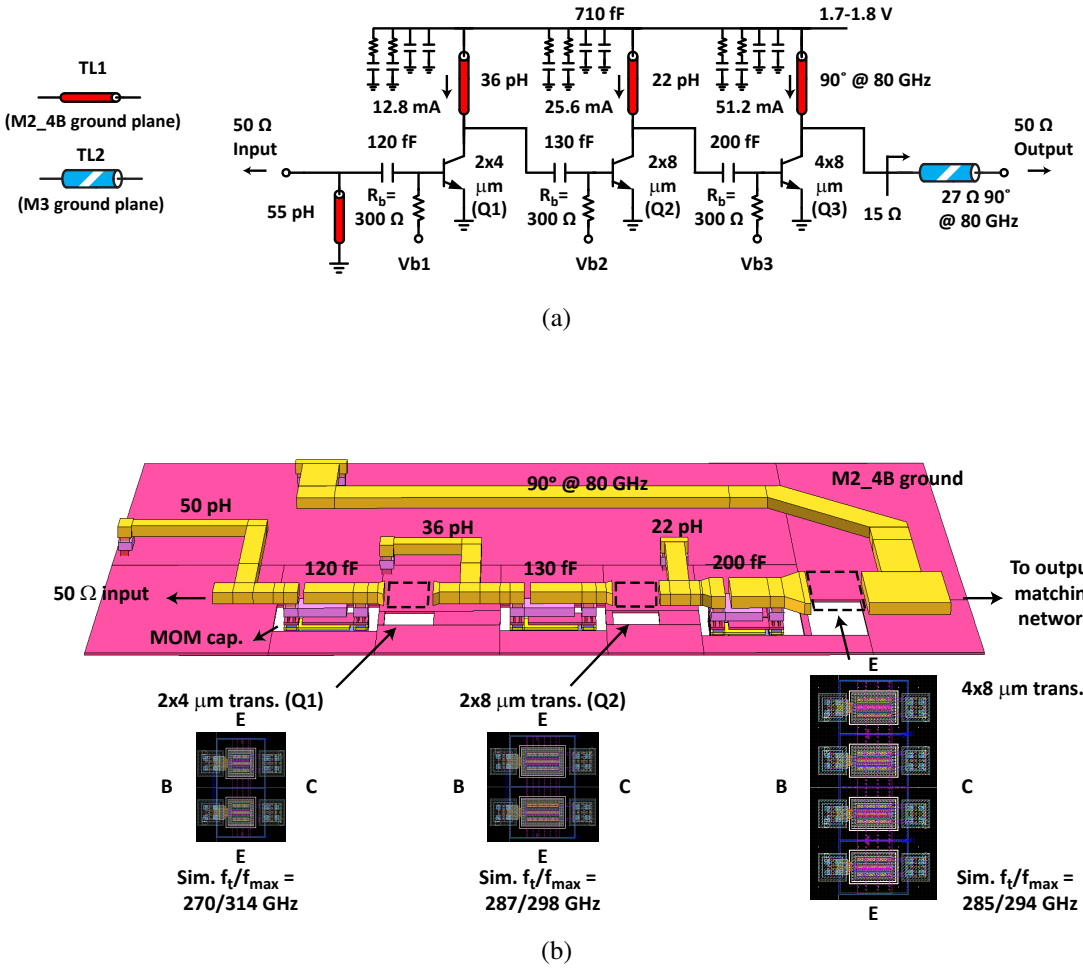


Figure 2.5: (a) Schematic of the 70-80 GHz 3-stage amplifier, and (b) EM modeling of the amplifier done using Sonnet. The f_t/f_{max} simulations including the interconnections to the top-metal layer

collector-emitter, base open) by presenting a low impedance (R_b = 300 Ω) to the transistor base nodes [57, 58]. The resulting effective collector-emitter breakdown voltage allows the voltage at the collector node to peak above 3.1 V, a factor of 1.8 improvement over BVceo.

Fig. 2.6 presents the biasing circuitry for each of the three-stage PA. For each stage, the current ratio in the npn current mirror is 1:2, 1:4, and 1:8 for Q1, Q2, and Q3 respectively. The current ratio of the preceding two-stage MOS current mirror is set to 1:10 for each stage to reduce the power consumption in the biasing network.

Fig. 2.7 presents the simulated P_{sat} versus R_b when only the Q3 stage is considered. A higher P_{sat} is achieved when a lower R_b is used at the base node, and this results in a lower I_bR_b drop which allows for a higher V_{be} at large currents. A R_b=300 Ω is chosen since it is much higher than the base input impedance of Q1 (10.5 - 10.1j Ω), Q2 (7 - 3.3j Ω), and Q3 (4.5 - 1j Ω), and does not load the network. A lower value R_b could have been used with λ/4 transmission line bias circuitry (Fig. 7(b))[57] to isolate the base input impedance and achieve a higher P_{sat}, but is not used due to area considerations.

Since the transistors have sufficient small-signal gain at 70-90 GHz, the interstage-matching between Q1 and Q2, Q2 and Q3, and Q3 to the 50 Ω load are all optimized using load-pull analysis for maximum power transfer at 80 GHz instead of complex-conjugate matching for maximum gain transfer. This explains why the peak small-signal

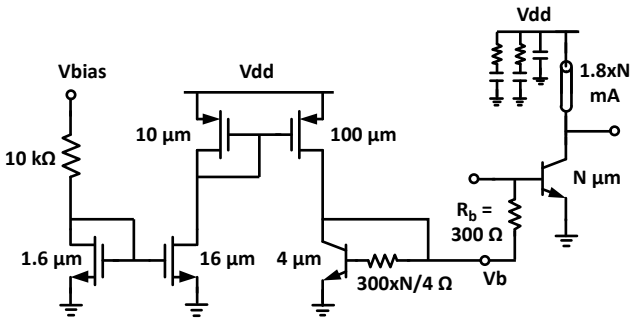


Figure 2.6: Bias circuit for each stage of the 3-stage PA.

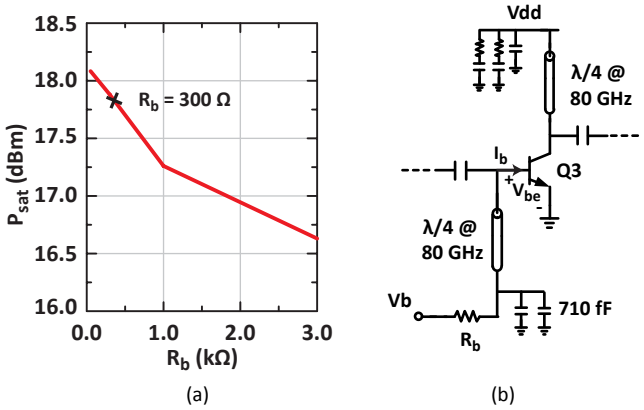


Figure 2.7: (a) Simulated P_{sat} v.s. R_b for Q3 stage alone with optimized load, and (b) bias circuit using λ/4 transmission line.

gain is not centered at 80 GHz, but the maximum output power is at 80 GHz.

Load-pull analysis is first done on Q1, and the optimum load impedance for maximum power delivery is 41 + j22 Ω for an output power of 9.4 dBm. Then, the input impedance of Q2 (base node) is transformed using a series capacitor and shunt inductor to the optimum load impedance for Q1 so as to ensure maximum power delivery. Similarly, load-pull analysis and interstage matching between Q2 and Q3 is done separately, and the optimum load impedance for Q2 is found to be 22 + j8 Ω with a output power of 14.6 dBm. Due to the collector-to-base capacitor (C_{be}) and the relatively large S_{12} for Q2 and Q3 (∼-20 dB at 80 GHz), the stages can not be designed independently, and manual iterations are done in Cadence on the interstage matching networks for optimal power transfer at 80 GHz. The final design is shown in Fig. 2.8.

The optimum load impedance for Q3 is 15 - j2 Ω with a maximum power of 17.2 dBm at 80 GHz (Fig. 2.9(a)), and is obtained using a TL2 with Z_0 = 27 Ω and ℓ = 90°. The 27 Ω TL2 line is 48 μm wide with a simulated loss of 0.3 dB/mm at 80 GHz (Q=48). Fig. 2.9(b) presents the Q3 load lines at small signal, OP1dB, OP1dB+3 dB and P_{sat} (OP1dB + 4.6 dB) respectively. The load lines are all ∼15 Ω due to the TL2 matching network and the DC bias current shifts up for large signals due to the transistor

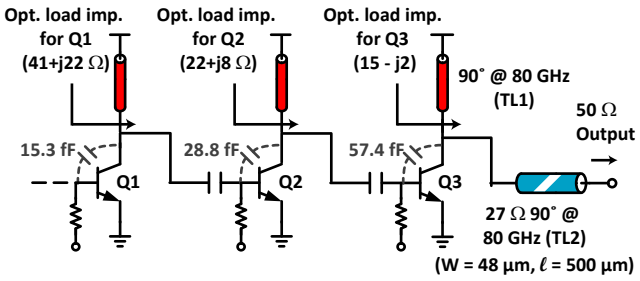
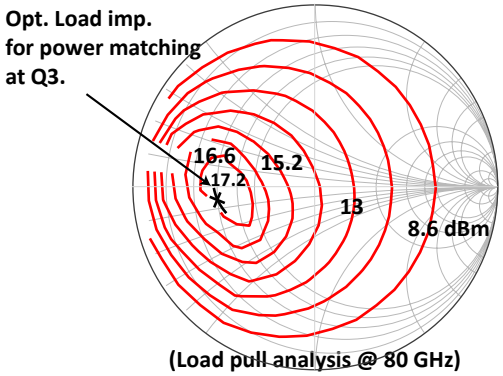
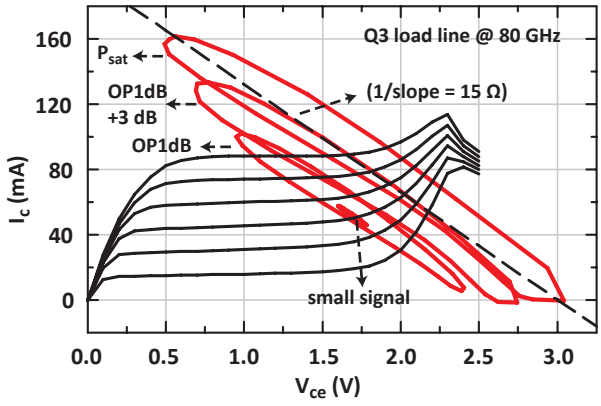


Figure 2.8: Interstage matching between Q1 and Q2, Q2 and Q3, and output matching for Q3.



(a)



(b)

Figure 2.9: (a) Simulated power contours for Q3 and (b) simulated load lines for Q3 with different output power levels. The 3-stage amplifier is simulated and not Q3 alone

self-bias characteristics.

Fig. 2.10 presents the effect of operating temperature on the small-signal gain at 70 GHz and P_{sat} at 80 GHz for the 3-stage amplifier. There is ∼1 dB gain reduction and ∼0.4 dB P_{sat} reduction per 30 °C rise in temperature, and is due to the decrease in f_t and f_{max} versus temperature.

The 3-stage PA has a simulated peak small-signal gain of 27.2 dB at 70 GHz with a 3-dB bandwidth of 65-82 GHz. The simulated P_{sat} is 17.4 dBm at 80 GHz with a linear gain of 25 dB, a peak PAE of 16.4%, and an output power 1-dB compression point (OP_{1dB}) of 12.8 dBm. The 4.6 dB difference between P_{sat} and OP_{1dB} is because the first and second stage, Q1 and Q2, start to saturate earlier than the last stage Q3, and the matching networks are optimized for maximum P_{sat} instead of maximum OP_{1dB} (In hindsight, this was a design error and will be changed in the future work). The quiescent bias current is 110 mA and the bias current at P_{sat} is 180 mA for a Vdd of 1.7 V. The simulated S_{12} is <-55 dB at 60-90 GHz.

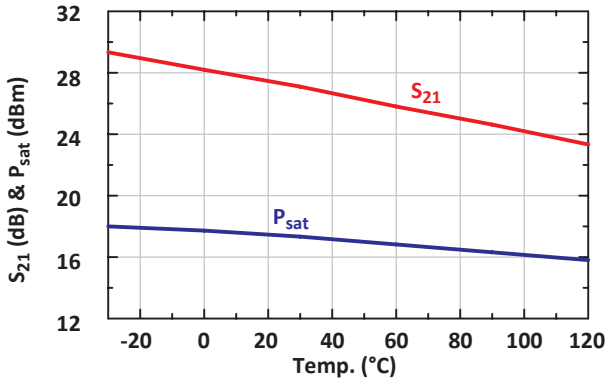


Figure 2.10: Simulated S_{21} at 70 GHz and P_{sat} at 80 GHz of the 3-stage amplifier v.s. temperature.

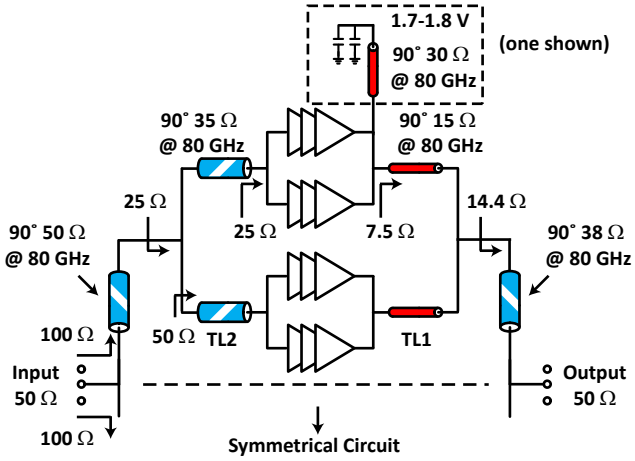
2.3.2 8-way Power Combining

The 8-way power combining PA is implemented using 8 3-stage PAs with λ/4 matching networks connected at the input and output ports (Fig. 2.11(a)). Two adjacent single PAs are first tied together at the input and output nodes to form a PA pair. The Q3 collector nodes in the PA pair share the same λ/4 Vdd stub in order to reduce the chip area. The λ/4 Vdd stub (TL1, W=27 μm, Z_0 = 30 Ω) is designed for the electromigration rule and reliability consideration, and used to bias two 32 μm transistors (∼160 mA in P_{sat}).

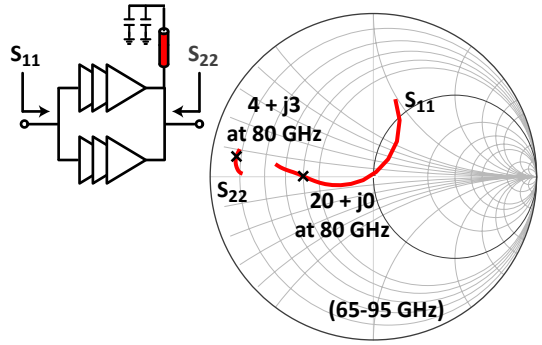
The optimum load impedance at the output of the PA pair is (15 - j2)/2 Ω. In order to connect four PA pairs to a common 50 Ω output port, a 38 Ω quarter-wave TL2 is used to transfer the 50 Ω port impedance (100 Ω in common mode) to 14.4 Ω. Next, the 14.4 Ω (28.8 Ω in common mode) is transferred to 7.5 - j1 Ω using a 15 Ω (TL1, W=66 μm) quarter-wave line. Note that TL1 is used close to the PA pair since a TL2 would have been too wide.

At the input port, the RF signal is distributed to each PA pair using λ/4 T-junction networks. The input impedance of the PA pair is 25 Ω, and is transferred successively to 50 and 100 Ω using λ/4 networks. The final T-junction combines two 100 Ω loads into a 50 Ω impedance. All input networks are done in TL2 for low loss.

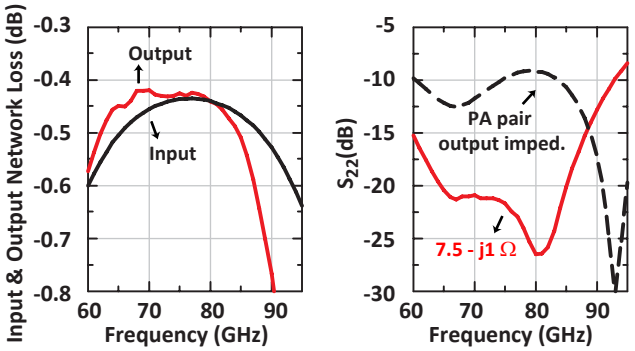
The λ/4 power combining networks are wideband and with low ohmic loss. The combining bandwidth and loss are studied as follows [16]: The output impedance of the PA pair is assumed to be constant vs. frequency (7.5 - j1 Ω), and the combining loss and S_{22} are simulated for the two λ/4 T-junction networks using Sonnet. A loss of 0.42-0.5 dB is found together with an S_{22} <-15 dB at 62-85 GHz. Analysis including the simulated PA pair output impedance, shown in Fig. 2.11(b), results an S_{22} <-9 dB at 60-95 GHz (Fig. 2.11(c)). A similar study is done on the input network, and results in a loss of 0.44-0.5 dB at 65-88 GHz (0.2-0.3 dB for each λ/4 T-junction networks).



(a)



(b)



(c)

Figure 2.11: (a) Schematic of 8-way power combining amplifier, (b) input and output impedance of the PA pair, and (c) simulated output combining and input distribution loss and S_{22} vs. frequency.

The 8-way PA shows a simulated peak small-signal gain of 27.4 dB at 70 GHz with a 3-dB bandwidth of 65-80 GHz. The simulated P_{sat} is 26.3 dBm at 80 GHz with a peak PAE of 18.1% and an OP_{1dB} of 22.1 dBm. The peak small-signal gain is comparable to the single PA because of the low-loss input and output networks (0.8-1.0 dB loss) and due to the fact that its S_{22} (-12 dB) is much better than the single PA (S_{22}= -6 dB) at 70 GHz.

2.3.3 16-way Power Combining

The design consists of 16 single PAs (eight PA pairs) connected again using λ/4 T-junction networks so as to form a compact two-dimensional circuit (Fig. 2.12). Again, the goal is to present 7.5 - j1 Ω at the output node of each PA pair for maximum power transfer. Due to the left/right symmetry, the 16-way PA employs a two-stage output matching network, which is similar to the 8-way PA and with nearly the same low combining loss.

The 50 Ω output port is first transferred to 7.2 Ω using a λ/4 TL2 line (W=52 μm, Z_0 = 27 Ω), and then the 7.2 Ω is transferred to 7.5 Ω to each PA pair by a λ/4 TL1 line (W=66 μm, Z_0 = 15 Ω). The output combining network has a total loss of 0.5-1 dB from 65-92 GHz and S_{22} <-10 dB from 65-92 GHz when the output impedance of each PA pair is constant 7.5 - j1 Ω. When the real single-ended PA output impedance is considered, S_{22} is <-10 dB at 65-97 GHz.

The input distribution network consists three λ/4 T-junction networks with quarter-wave lines and impedance of 35, 35, and 50 Ω at 80 GHz. A 25 Ω 1.6-mm TL2 transmission line is used as the long connecting line from the input port to the two amplifier halves with a loss of 0.48-0.5 dB at 65-90 GHz. The simulated insertion loss of the input distribution network is 1.1-1.5 dB from 70-100 GHz with S_{11} <-15 dB. The input loss has a samll effect on the amplifier's PAE due to the high gain design.

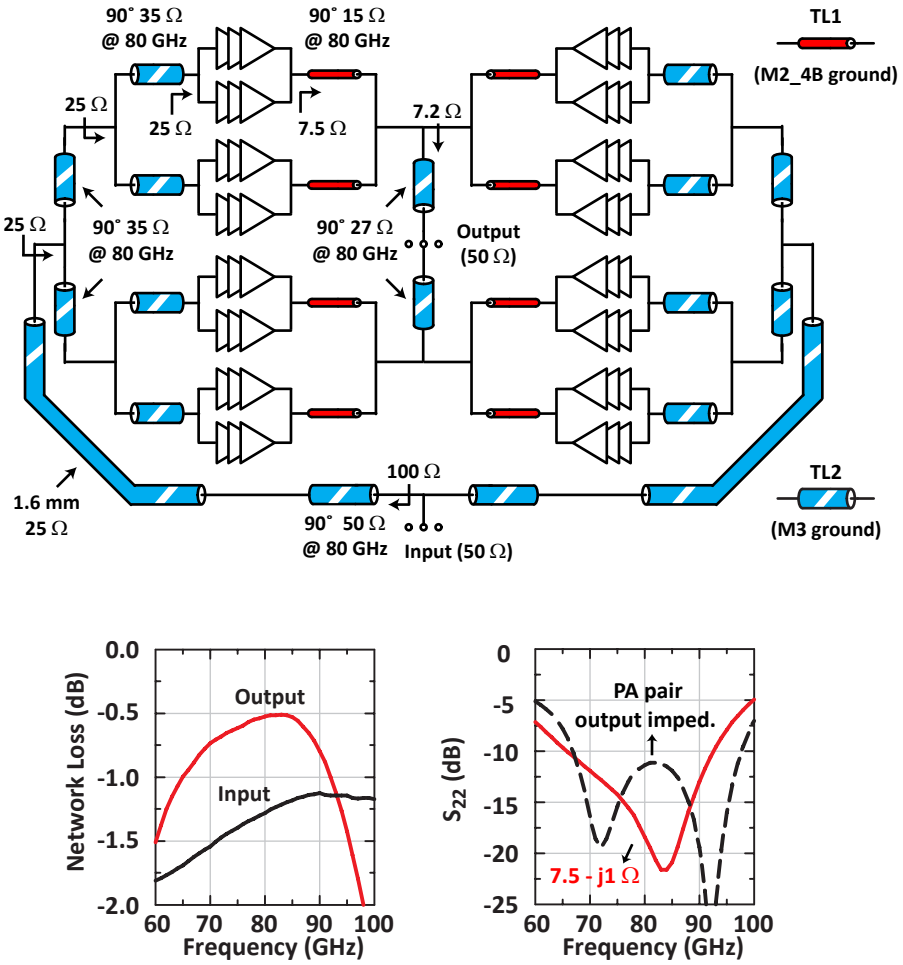


Figure 2.12: Schematic of the 16-way power combining amplifier, simulated input distribution and output combining loss, and S_{22} vs. frequency.

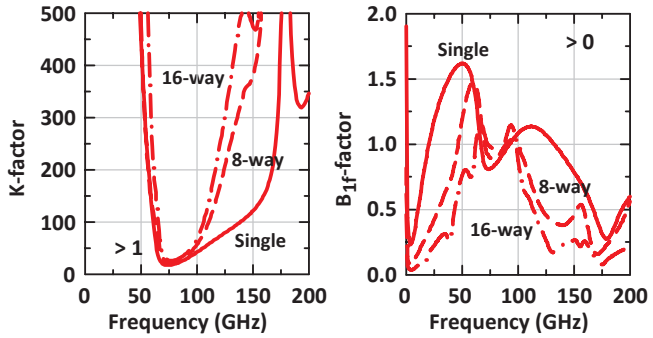
The 16-way combined PA has a simulated peak small-signal gain of 26.6 dB at 71 GHz with a 3-dB bandwidth of 66-80 GHz. The simulated P_{sat} is 29.5 dBm at 80 GHz with a peak PAE of 18.8% and an OP_{1dB} of 25.5 dBm.

Simple electrostatic discharge (ESD) diodes are implemented at the bias control pins for the amplifiers. There is no ESD protection on the RF path to avoid the extra parasitics due to the diode capacitance loading. A large amount of VDD pads are used for the 16-way combined amplifier to distribute the current evenly throughout the chip.

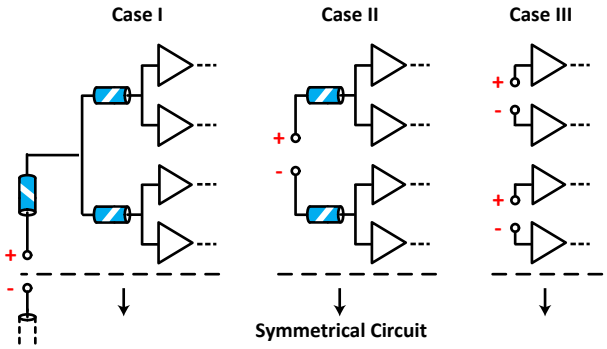
2.3.4 Stability Consideration

The simulated K-factor and B_1-factor for the single, 8-way combined, and 16-way combined PA are shown in Fig. 2.13(a). The K-factor is >1 and B_1-factor is >0 at DC-200 GHz. The 8-way and 16-way combined PA are even-mode unconditionally stable because all the amplifier cells are driven with a signal in the same phase.

The odd-mode stability of the 8-way combined PA is studied as followings: a differential signal is excited at the first input T-junction (case 1), the second input T-junction (case 2), and the last T-junction at the input of PA pairs (case 3) in the 8-way combined PA (Fig. 2.13(b)), and the K-factor and B_1-factor are simulated in Cadence for each case from DC-200 GHz. The odd-mode stability of the 16-way combined PA is studied in the same way as the 8-way combined PA with one more T-junction at the input port. The resulting odd-mode K-factors are >1 and B_1-factors are >0 at DC-200 GHz for all cases (3 cases for 8-way, and 4 cases for 16-way combined PA) due to the very low S_{12} of the 3-stage amplifier. The amplifiers are unconditionally stable at all frequencies.



(a)



(b)

Figure 2.13: (a) Simulated K-factor and B_1-factor for the single, 8-way, and 16-way power combining PA, and (b) odd-mode stability analysis for the 8-way combined amplifier (output combining network is not shown here for brevity).

2.4 Measurements

2.4.1 S-Parameters

The S-parameter are measured using two different setups. An Agilent DC-67 GHz vector network analyzer (VNA) is first used to measure S-parameters from DC-70 GHz, and then an Agilent 50 GHz VNA are used with Agilent mm-wave head controller and VDI WR-10 extenders for measurements at 70-110 GHz (Fig. 4.9). Standard short-open-load-thru (SOLT) calibration on CS-5 calibration substrate is done for both cases. The results include the input and output G-S-G pads loss (measured 0.3-0.5 dB total loss at 60-110 GHz).

The chip microphotographs of the 16-way and 8-way power combining PAs, and the single PA are shown in Fig. 2.15. Fig. 2.16 presents the measured small-signal gain of the single, 8-way combined, and 16-way combined PA. The single PA results a peak gain of 22 dB at 74 GHz with a 3-dB bandwidth of 68-82 GHz. The 4.4 dB difference between simulations and measurements is due to the actual transmission-line loss which is higher than the simulated value in Sonnet, and the inaccuracy in transistor modeling. The IBM9HP process is still in development and the transistor performance can vary a bit from process run to run.

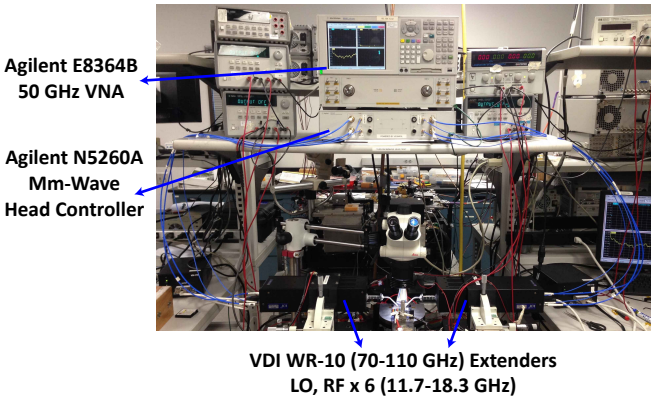


Figure 2.14: 70-110 GHz S-parameter measurement setup.

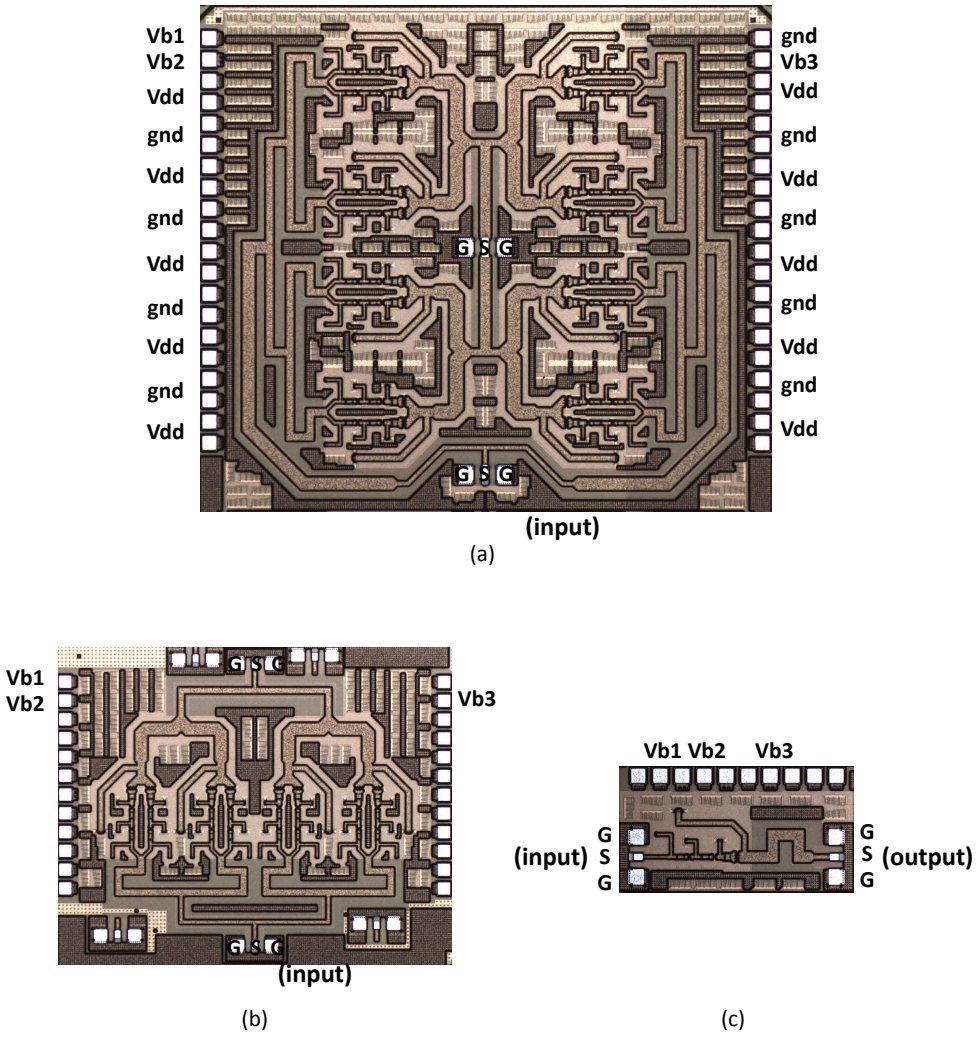


Figure 2.15: Chip microphotograph of (a) 16-way power combining amplifier (2.7×2.4 mm^2 including pads), (b) 8-way power combining amplifier (1.6×2.2 mm^2), and (c) 3-stage amplifier (1×0.6 mm^2). Unlabeled pads are all for ground and Vdd power supply.

The 8-way PA has a peak gain of 21.2 dB at 73 GHz with a 3-dB bandwidth of 68-82 GHz, and a 5.8 dB difference between simulations and measurements. This is an additional 1.4 dB difference than the 3-stage PA. The S_{22} of the 8-way combined PA (-10 dB) is better than the S_{22} of the single PA (-7 dB) at 74 GHz, and taking this into account, the extra transmission-line loss in the 8-way combined PA is 0.9 dB. This is due to additional input and output transmission line loss not taken in simulations.

The 16-way power combining amplifier has a peak gain of 19.3 dB at 74 GHz with a 3-dB bandwidth of 69-81 GHz. There is yet another 1 dB difference between measurements for the 16-way and 8-way PAs. This is due mainly to the long input transmission line.

The measured S_{12} is $<$-50 dB from DC-70 GHz (Agilent DC-67 GHz VNA), and is $<$-35 dB from 70-110 GHz (WR-10 extenders) for all the amplifier cells. We believe that the relatively higher S_{12} at 70-110 GHz is due to the limited dynamic range of WR-10 extenders, and the measured K-factor is $>$1 and B_1-factor is $>$0 at DC-110 GHz for all the amplifiers.

The small-signal power consumption in each case are 257 mW (143 mA), 1.94 W (1.03 A) and 3.65 W (2.03 A) from a 1.8 V supply, respectively. Measurements agree with simulations versus frequency except for the extra transmission line loss and lower transistor gain, and shows the accuracy of the Cadence design and the Sonnet EM models.

2.4.2 Power Measurements

Fig. 2.17 presents the power measurement setup. The input 65-105 GHz signal is generated using VDI-AMC 332-334 multiplier chains and the output power is monitored using PM4 Erickson power sensor [59]. A WR-10 variable attenuator (-6 dB) is used in front of the power sensor due to the 200 mW upper limit of the power sensor. The WR-10 GSG probe loss is measured using a thru on the SiGe wafer, and the measured thru loss

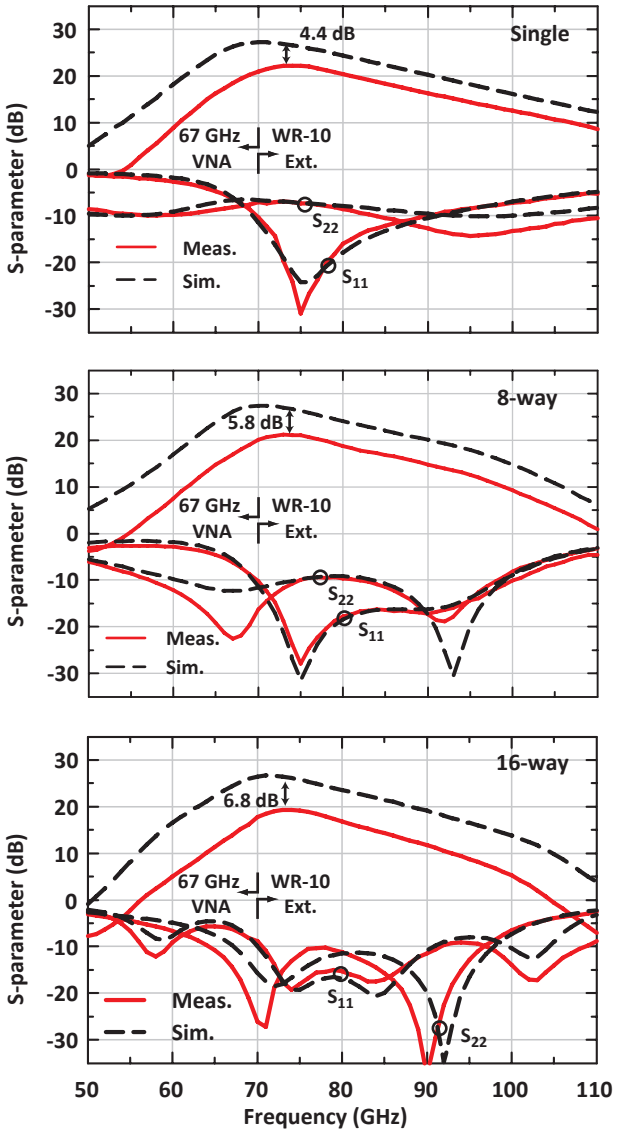


Figure 2.16: Measured S-parameters of single, 8-way combined, and 16-way combined amplifier.

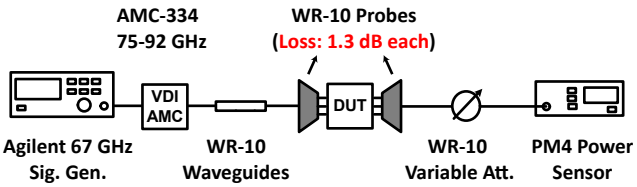


Figure 2.17: Power measurement setup for the 70-80 GHz amplifiers.

is 3.0 dB at 80 GHz with a GSG pad loss of 0.2 dB each. This means that the probe loss is 1.3 dB each, and agrees well to the 1.25 dB loss provided by the manufacturer data sheet [60]. All measurements are referenced to the WR-10 GSG probe tips, and include the 0.2 dB GSG pad loss at the input and output ports.

The single PA results in 15.8 dBm at 80 GHz with a peak PAE of 10.7%. The OP_{1dB} is 11.2 dBm with an associated PAE of 5.1% (not shown for brevity). The 8-way combined PA results in an output power of 24.1 dBm at 76 GHz with a peak PAE of 11.3% and associated gain of 9 dB. The OP_{1dB} is 20.4 dBm with an associated PAE of 5.8%. For the 16-way power-combining PA, an output power of 27.3 dBm is achieved with peak PAE of 12.4% at 76 GHz and with an associated gain of 9 dB (Fig. 2.18). The OP_{1dB} is 21.2 dBm with an associated PAE of 3.8%.

The same measurement setup is used for output power v.s. frequency, and the results are calibrated to the probe tips by carefully de-embedding the input and output losses at 65-105 GHz. The measured P_{sat} for the single PA is >14 dBm at 64-105 GHz with $\geq$ 16 dBm at 80-95 GHz. Measurements on the 8-way combined PA show $\geq$ 21 dBm at 66-95 GHz with 24 dBm at 72-80 GHz (Fig. 2.19). The 16-way power-combining PA achieves a P_{sat} >25 dBm at 68-88 GHz (Fig. 2.20). In particular, the 16-way power combining amplifier results in 26.5-27.3 dBm at 72-84 GHz with PAE > 8%. We have measured 4 different chips with nearly identical results.

Table 2.1 and Fig. 2.21 summarize the measured results and compare this work with recently published amplifiers. The 16-way power-combining PA shows the highest

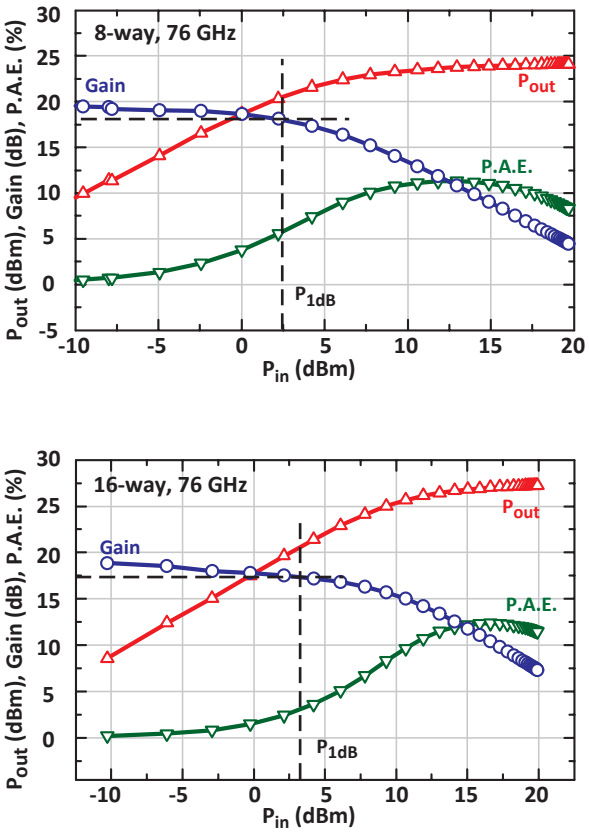


Figure 2.18: Measured output power, gain, and P.A.E. vs input power of the 8-way, and 16-way power combining amplifier at 76 GHz.

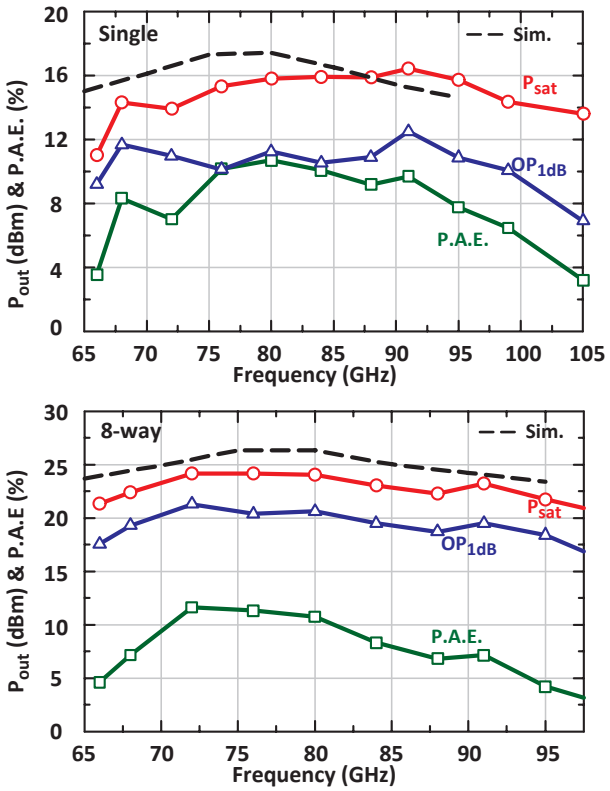


Figure 2.19: Measured P_{sat}, OP_{1dB} and P.A.E. vs frequency of single, and 8-way power combining amplifier.

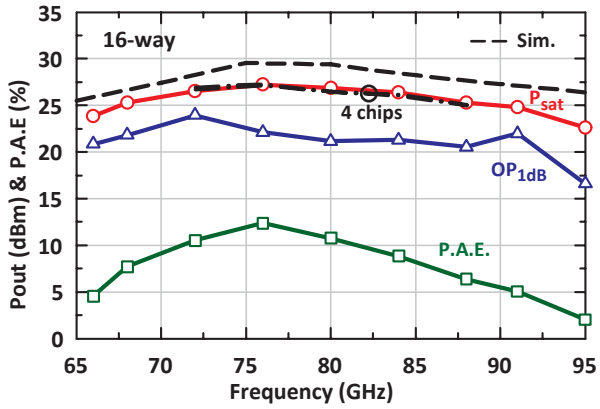


Figure 2.20: Measured P_{sat}, OP_{1dB} and P.A.E. vs frequency of the 16-way combining amplifier.

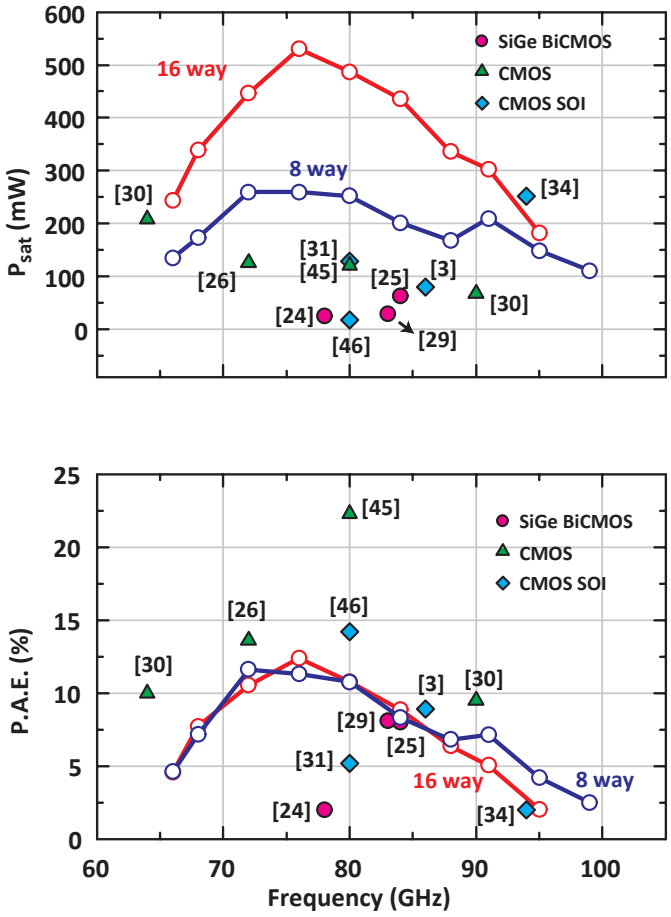


Figure 2.21: P_{sat} and P.A.E. of the 8-way and 16-way amplifiers compared with published work.

Table 2.1: Performance Summary for E-band Amplifiers in SiGe and CMOS Technology

Freq. (GHz)	**Tech.**	**Type**	**P_{sat} (dBm)**	**Gain (dB)**	**OP_{1dB} (dBm)**	**PAE (%)**	**Vdd (V)**	**Area (mm^2)**	**Ref.**
68-105	90-nm SiGe	3-stage single	16.2	22	12.2	10.7	1.8	0.6	This work
68-95	90-nm SiGe	3-stage 8-way comb.	24	21.2	21.3	11.6	1.8	3.52	This work
68-91	90-nm SiGe	3-stage 16-way comb.	27.3	19.3	22.3	12.4	1.8	6.48	This work
78	180-nm SiGe	transformer-based 4-way comb.	14	18.3	12.5	2	3.2	0.85	[22]
83	180-nm SiGe	2-stage cas. 2-way comb.	14.7	25	12.5	8.1	4	0.34	[17]
84	130-nm SiGe	transformer-based 4-way comb.	18	25	16	8	2.5	0.68	[23]
64	65-nm CMOS	3-stage 32-way comb.	23.2	16.3	19.6	10	1.2	2.04	[18]
72	40-nm CMOS	transformer-based 4-way comb.	21	21	19.2	13.6	1.5	0.96	[24]
80	40-nm CMOS	parallel-series 4-way comb.	20.9	18.1	17.8	22.3	0.9	-	[61]
90	65-nm CMOS	3-stage 16-way Comb.	18.3	12.5	17.5	9.5	1.2	0.85	[18]
80	45-nm SOI	2-stage cas. 8-way comb.	21.1	10.1	-	5.2	2	1	[19]
80	45-nm SOI	2-stage cas.	12.4	11	12	14.2	2	0.32	[62]
86	45-nm SOI	stacked amp.	19	36	-	8.9	6.8	-	[39]
94	45-nm SOI	spatial power-comb. stacked amp.	24	-	-	<2	4	26	[27]

output power in this frequency range using silicon technology to-date.

2.5 Conclusions

This paper presented a high-power SiGe amplifier at 70-80 GHz with reactive power division at the input and reactive power combining at the output. The four-stage reactive combiner results in a loss of 0.6-1 dB at 65-95 GHz for the 16-way combined amplifier, and state-of-art output power over a wide frequency. The design technique does not employ $\lambda/4$ chokes in the biasing network and can be used with different silicon processes (advanced CMOS, SiGe with ground vias) for high-power, high-efficiency W-band power amplifiers.

2.6 Acknowledgements

The author would like to thank Analog Devices for technical discussions, Michael Chang at the University of Michigan for process and technical discussions, and IBM (David Harame) for the 9HP wafer space.

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Chapter 3

A 110-134 GHz SiGe Amplifier With Peak Output Power of 100-120 mW

3.1 Introduction

Millimeter-wave systems based on silicon circuits above 90 GHz have been recently developed for short-range high-data rate communication systems [1, 2, 3], focal-plane radiometric imaging [9, 10, 11, 12], radars [6, 7, 8], and other sensing platforms [63]. The use of CMOS and SiGe technology provide high-integration density for these complex systems, and with a low-cost path for a large number of units. Advanced CMOS and SiGe technologies such as 65- or 45-nm CMOS and 0.13-μm and 90-nm SiGe have been shown to result in millimeter-wave low-noise amplifiers and receivers [35] and oscillators with adequate phase noise [31, 33, 34], but the transceivers still suffer from inadequate output power [64, 65]. Although advanced silicon technologies deliver transistors with high f_t/f_{max} and low noise, the breakdown voltage of these devices is also scaled down, which limits the transistor output power.

One solution for limited output power is on-chip power combining. Power

combining using Wilkinson networks [15], transformers [20, 21], free-space [25, 26], and reactive power combining [66, 67] have been reported. Wilkinson- and transformer-based circuits result in high loss for a large number of combining elements (or stages), and free-space combining requires on-chip antennas which typically have a radiation efficiency of 30-50% (3-5 dB loss)[28, 29, 30]. Also, free-space combining does not allow the silicon chip to be used as a driver for a higher-power III-V chip for increased system performance, or for a driver for frequency multipliers for high power sources at THz frequencies [68, 36, 37].

This chapter presents an 8-way reactively combined power amplifier using low-loss $\lambda/4$ combining networks in a 90-nm SiGe BiCMOS process (Fig. 3.1). A single-ended 4-stage common-emitter amplifier with a small-signal gain of 20 dB at 116 GHz is used as the unit cell. The 8-way power-combining amplifier results in a P_{sat} of 20-20.8 dBm at 114-126 GHz. Also, a balanced PA using two single-ended amplifier units driven differentially with a passive balun is demonstrated. The balanced PA delivers a P_{sat} $>$16 dBm at 116-130 GHz with a peak value of 17.5 dBm at 124 GHz (balun loss at output is de-embedded). The differential configuration provides an efficient solution for driving differential antennas, and balanced frequency multipliers.

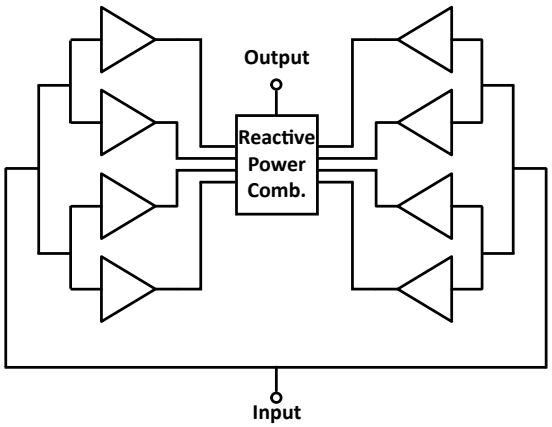
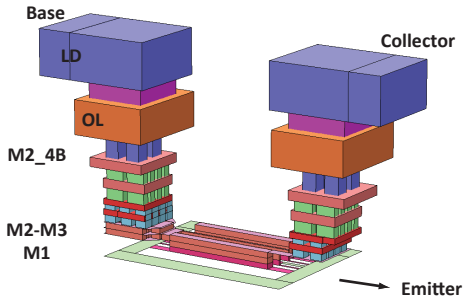


Figure 3.1: An 8-way reactively-combined power amplifier.

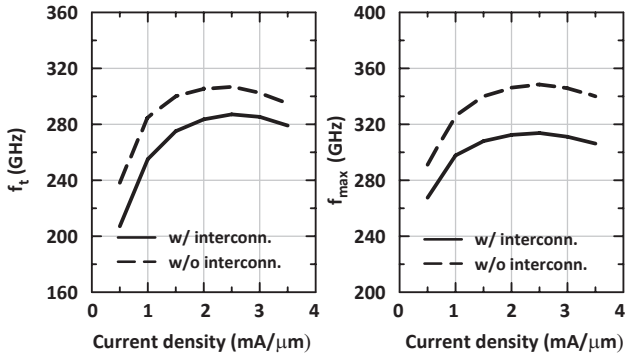
3.2 Technology

The 120 GHz PAs are designed using the IBM 9HP BiCMOS process [53]. It is a 90 nm SiGe HBT process built on top of a 90-nm CMOS process, with a 10-layer copper metal backend and high-density metal-insulator-metal (MIM) capacitors (12.2 fF/ μm^2). The 4$\times$0.1 μm^2 transistor model from the Cadence library results in a peak f_t/f_{max} of 310/350 GHz at 1.5-2.5 mA/μm bias current (Fig. 3.2(a) and 3.2(b)). However, the peak f_t/f_{max} drops to 290/310 GHz when the interconnect parasitic resistance and capacitance from M1 to LD, as modeled in Sonnet EM-suite [55], are taken into account. This is much better than CMOS transistor which typically drop from an f_t/f_{max} of 480 GHz to 260 GHz when the interconnect effects are taken into account [56], and is due to the all-copper back-end and thick dielectrics used in the IBM 9HP process.

Fig. 3.2(c) presents the microstrip 50 Ω transmission line used in the PA design for the matching stubs and the power-combining network, is implemented using the top metal LD with 10 μm width and M2_4B as the ground plane (M1_4B is used as the Vdd plane). Electromagnetic (EM) simulations using Sonnet results in 0.75-0.9 dB/mm loss at 100-150 GHz (0.9-1.1 dB/mm for a G-CPW line), and a transmission-line Q of 24-30 at 100-150 GHz (Fig. 3.2(d)). In practice, and from different measurements done on IBM 8HP and other processes, the loss is a bit higher than simulated and it is expected that a loss of 0.9-1.2 dB/mm is achieved at 100-150 GHz. Still, a loss of 0.75-0.9 dB/mm is taken in the Sonnet simulations since there are no measurements at these frequencies.



(a)



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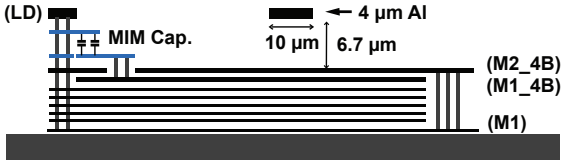
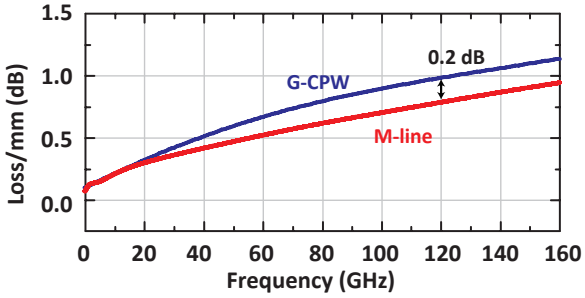


(c)



(d)

Figure 3.2: (a) The interconnection from M1 to top metal LD, (b) simulated f_t and f_{max} of 4×0.1 μm^2 transistor, (c) 50 Ω microstrip transmission, and (d) simulated line loss of microstrip and G-CPW lines.

3.3 Design

3.3.1 Single-Ended PA

The PA consists of four common-emitter gain stages biased in the class AB region (Fig. 3.3(a)). Since no foundry power-transistor layout cells are available in the Cadence library, the power transistors are implemented by aggregating smaller, high-f_t npn standard cells. A 4×0.1 μm^2 transistor is used as the standard aggregating cell with a single emitter finger, dual collectors and base fingers (C-B-E-B-C), and is surrounded by a deep-trench isolation ring. In future work, a custom layout may be used for the power transistor cells and may result in better performance. The power transistors are biased near their peak f_t current density at a quiescent current of 1.2 mA/μm. The first- and second-stage power transistors, Q1 and Q2, consist of two parallel 4 μm npn standard cells while the third stage power transistor Q3 is implemented using four of these standard cells in parallel. The output power transistor Q4 is implemented using four of 2×4 μm npn connected in parallel to form a 32 μm emitter-length device (Fig. 3.4).

The first- and second-stage amplifiers provide a small-signal gain of 6 dB each at 120 GHz while the third- and fourth-stage provide a gain of 4-5 dB each. The third- and fourth-stage power transistors are scaled by twice the area over the previous-stage transistors to ensure that the output transistor Q4 limits the large-signal compression characteristics. All amplifiers are driven by a single Vdd plane (1.5-1.6 V) and a common ground plane (M2_4B). The PA design overcomes the technologys 1.5 V breakdown voltage, collector-emitter, base open (BVceo) by presenting a low external base impedance to the power transistor cells [58][57]. 300 Ω biasing resistors connected at the transistor base nodes are found to have optimal gain and power performance, as shown in Fig. 3.5, and the resistors are implemented using TaN resistors. The resulting effective collector-emitter breakdown voltage allows the output voltage at the collectors

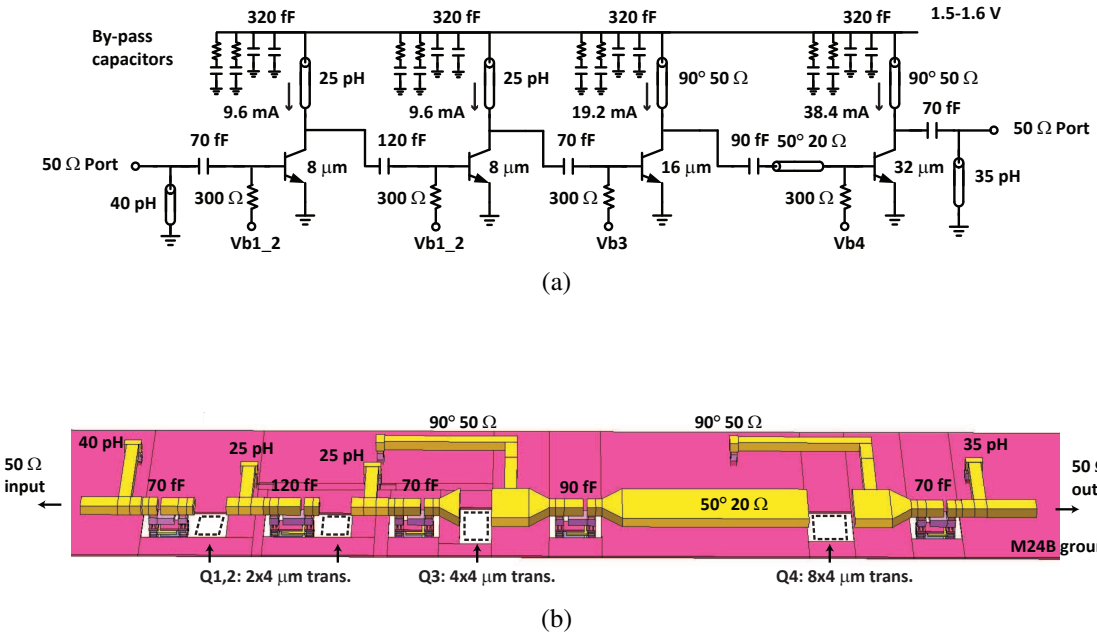


Figure 3.3: (a) Schematic of the 120 GHz amplifier, and (b) EM modeling of the 120 GHz amplifier done using Sonnet.

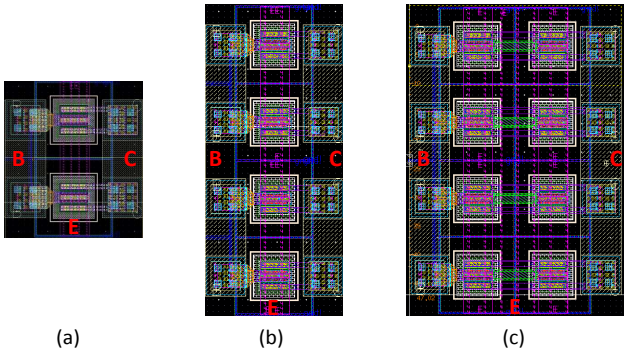


Figure 3.4: Layout of power transistors (a) Q1 and Q2 (2×4 μm), (b) Q3 (4×4 μm), and (c) Q4 (4×2×4 μm).

to peak above 2.2 V, a factor of 1.5 improvement over BVceo.

The EM simulation environment of the matching networks for the 120 GHz PA is shown in Fig. 3.3(b). The input matching, inter-stage matching, and output matching networks are implemented using LC-resonant circuits and are all modeled in Sonnet. Compact metal-oxide-metal (MOM) capacitors, implemented using top metal LD to metal M1_2B, are widely used as series matching elements where DC-blocks are required. Inductors are implemented using shorted 50 Ω microstrip lines with different lengths with associated Q of 14-16 at 120 GHz. Customized MOM between LD and M1_2B capacitors are chosen over the process design kit (PDK) MIM and vertical-natural (VN) capacitors for matching because they show a higher Q value impedance (Fig. 3.6(a)). The models for the MOM, MIM, and VN capacitors are shown in Fig 3.6(b) and (c).

The Vdd stubs connected at the collector nodes are followed by dual 320 fF MIM capacitors which are operating close to self resonance and provide a very low impedance ($\sim$1 Ω) at 120 GHz. M2_4B layer is used as ground plane and M1_4B layer is used as Vdd plane for the Vdd stubs. Both ground and Vdd planes are cheesed to pass the metal density rule. 50 Ω quarter-wavelength microstrip lines at the collector nodes of Q3 and Q4 are used as RF chockes [57], which present an open circuit ($>$ 500 Ω) to the low impedance collector nodes ($\sim$10 Ω) and ease the implementation of the matching network between Q3 and Q4 and the output port.

Fig. 3.7 present the simulated power gain circles and simulated output power contours with respect to different transistor load impedances seen at the Q4 collector node. A transistor load impendence of 11 + j2 Ω is chosen to achieve both optimal power gain (22.7 dB) and output power (13.8 dBm). The 50 Ω output port is transferred to the optimal transistor load impedance using a shunt 35 pH short stub and a series 70 fF MOM capacitors. This results in a wideband output power at 110-130 GHz since the power contours in Fig. 3.7(b) do not change much vs. frequency.

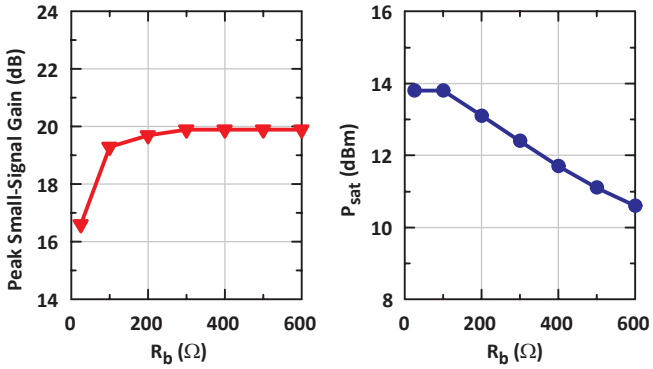


Figure 3.5: Simulated peak small-signal gain and P_{sat} vs. R_b at 116 GHz.

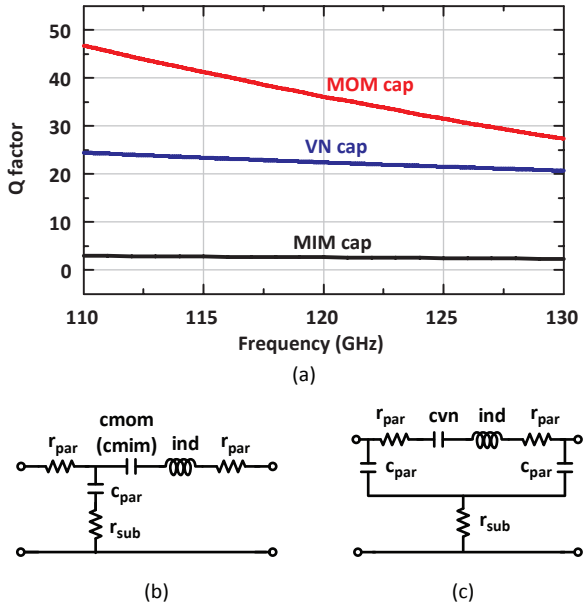


Figure 3.6: (a) Simulated Q value for 90 fF MOM, VN, and MIM capacitors, (b) models for the MOM and MIM capacitors, and (c) model for the VN capacitor.

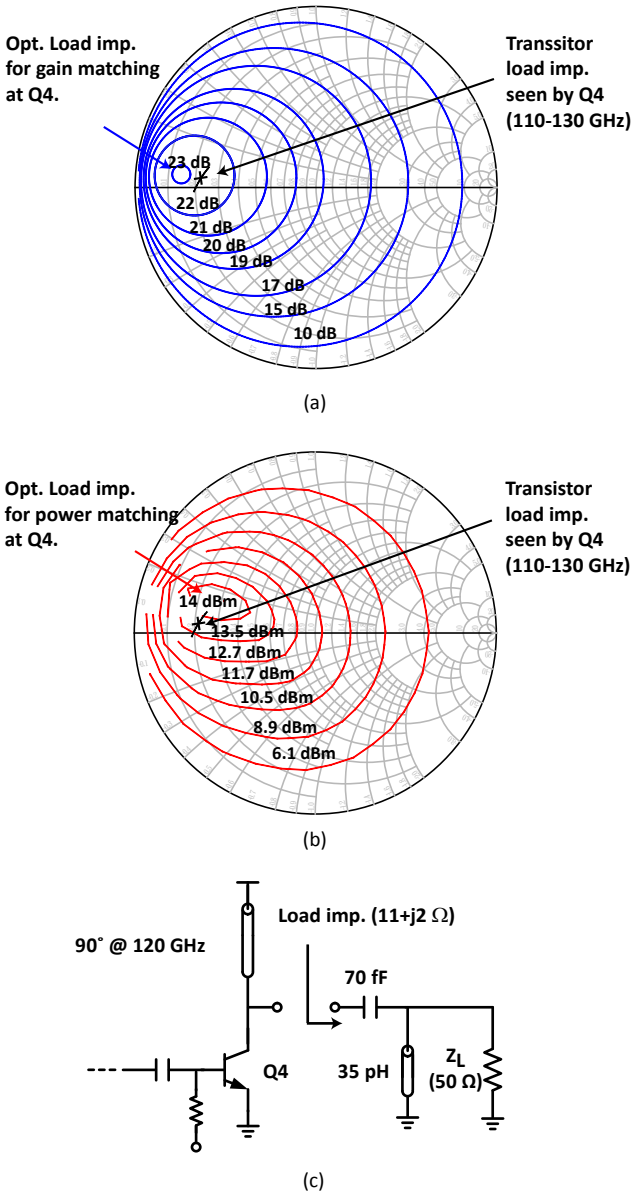


Figure 3.7: (a) Simulated power gain circles and (b) simulated output power contours v.s. load impedance presented at Q4, and (c) load impedance seen by Q4.

The circuit is robust versus port impedance (Z_L) variation. For a 2:1 voltage standing wave ratio (VSWR), the maximum voltage is 2.35 V (instead of 2.2 V for Z_L = 50 Ω) at P_{sat} condition. If an open circuit is placed at the output port, the impedance seen by the transistor Q4 becomes 1.5 Ω-j5 Ω, and the maximum voltage is 2.75 V when driven at P_{sat} condition.

The single-ended PA has a simulated small-signal gain of 22.3 dB at 116 GHz with 3-dB bandwidth of 107-124 GHz. The simulated P_{sat} is 13.4 dBm at 120 GHz with peak PAE of 13% and output power 1-dB compression point (OP_{1dB}) of 10 dBm. The quiescent bias current is 76 mA and the bias current at P_{sat} is 150 mA.

3.3.2 120 GHz Balanced PA

The balanced PA is implemented using two single-ended PAs as half circuits with wideband baluns at the input and output ports (Fig. 3.8). The balun is designed using the top metal (LD) for the first core and the second metal (OL) for the second core and optimized using Sonnet (Fig. 3.9(a)). A shunt 25 fF MOM capacitor is connected to the differential port of the balun to achieve simultaneous matching at the input (50 Ω) and output ports (100 Ω). The simulated insertion loss of the balun is $<$1.5 dB at 100-140 GHz, and the amplitude and phase imbalance are $\sim$0.4 dB and 4^{o}, respectively, up to 140 GHz (Fig. 3.9(b)).

The balanced PA results in twice the power of a single ended PA (16.4 dBm at 120 GHz) assuming that the output balun loss is de-embedded. This circuit is useful for driving a differential antenna or a balanced doubler or quadrupler with output power at 240 GHz or 480 GHz.

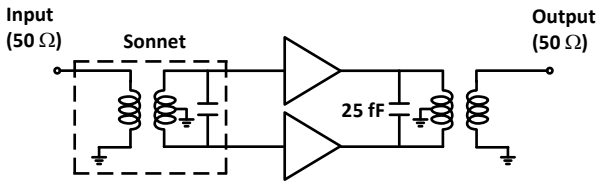
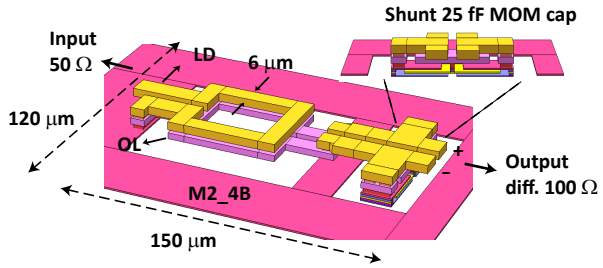
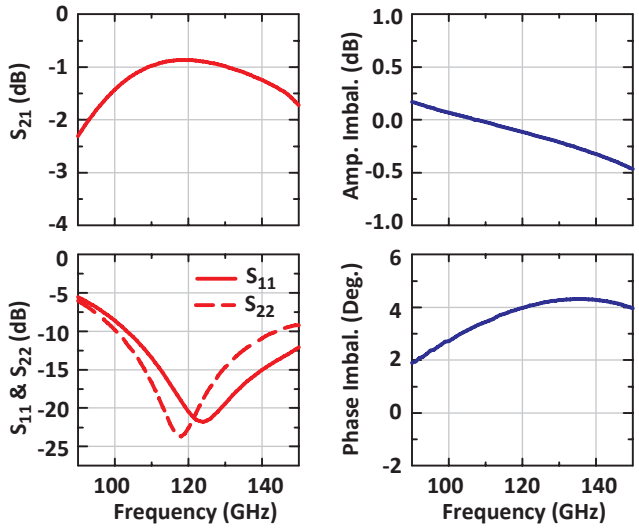


Figure 3.8: Schematic of the 120 GHz balanced amplifier.



(a)



(b)

Figure 3.9: (a) Sonnet EM modeling of the 120 GHz balun and, (b) simulated S-parameters, and amplitude and phase imbalance between the output ports.

3.3.3 8-way Power Combining PA

The design consists of 8 single-ended PAs connected using λ/4 networks so as to form a compact two-dimensional PA circuit (Fig. 3.10). Two adjacent 4-stage single-ended PAs are tied together at the input and output nodes to form a PA pair. The impedance looking into the output node of the PA pair is 25 Ω and is transferred back to 50 Ω using a 35 Ω quarter-wave microstrip line at 120 GHz. When 4 of these pairs are tied together, the impedance at the common node is 50/4 = 12.5 Ω and is transferred to the 50 Ω output port using a 25 Ω quarter-wave line. At the input port, the 110-130 GHz signal is distributed to the left and right PAs using a Wilkinson network, and a T-junction is used with λ/4 35 Ω networks to match the 25 Ω input impedance of the PA pair to 50 Ω.

The λ/4 power combining networks are wideband and with low loss. The bandwidth and loss are studied as follows: The output impedance of the PA pair is assumed to be a constant 50 Ω vs. frequency, and the combining loss and S_{22} are simulated for the output T-junction and the two-stage λ/4 power combining network using Sonnet. A loss of 0.5-0.6 dB is found together with an S_{22} <-20 dB at 102-140 GHz. Analysis including the PA output impedance shows an S_{22} <-10 dB at 117-124 GHz. A similar study is done on the input network, and results in a loss of 2.2 dB at 120 GHz (0.5 dB: Wilkinson, 1.2 dB: 1.6 mm 50 Ω transmission-line, 0.5 dB: input λ/4 matching networks).

The 8-way PA results in a simulated small-signal gain of 18.9 dB and an output saturated power of 21.1 dBm at 120 GHz. Compared to the single-ended PA power of 13.4 dBm, there is a 1.2 dB reduction in the 8-way combined power (13.4 dBm + 9 dB = 22.3 dBm). This indicates that the 8-way reactive combiner has a loss of 1.2 dB (not 0.6 dB) when the actual PA cell output impedance and mismatches are taken into account. The small-signal gain of 18.9 dB is 3.4 dB lower than a single-ended PA cell and is due to 2.2 dB input loss and 1.2 dB output loss.

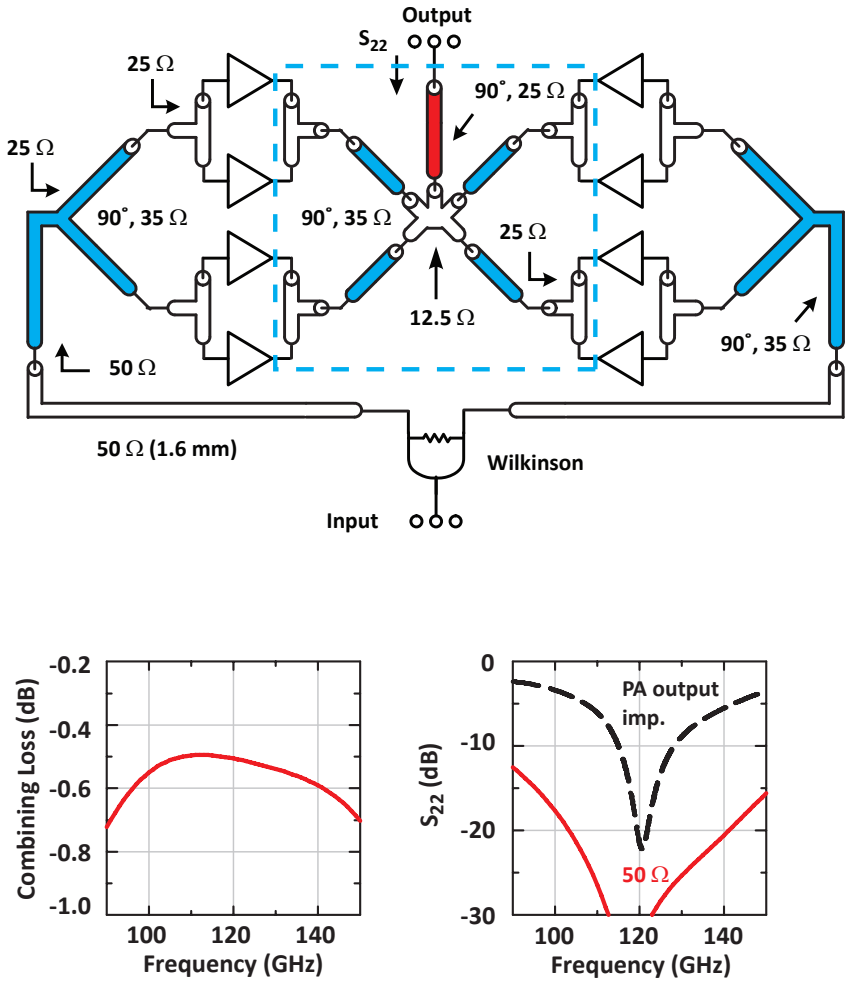


Figure 3.10: Schematic of the 8-way power combining amplifier and simulated output combining loss and S_{22} vs. frequency.

Simple electrostatic discharge (ESD) diodes are implemented with the bias control pins for the amplifiers. There is no ESD protection on the RF pathes to avoid extra parasitics capacitance loading.

3.3.4 Stability Consideration

The simulated K-factor and B_1-factor for the single-ended, differential, and 8-way combined PA are shown in Fig. 3.11. The K-factor is >1 and B_1-factor is >0 for the amplifiers at DC-200 GHz. The even- and odd-mode stability of the differential PA and the 8-way power combining PA are also simulated in Cadence. The resulting K-factor is >1 and B_1-factor is >0 for both cases at frequency of DC-200 GHz. The single-ended, differential, and 8-way power combining PA are shown to be unconditional stable at the operation frequency in simulation.

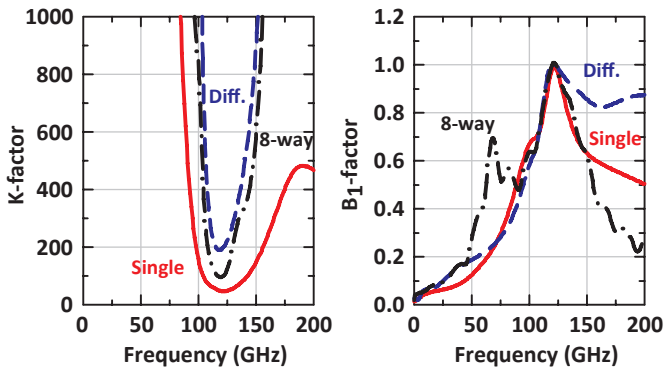


Figure 3.11: Simulated K-factor and B_1-factor for the single-ended, differential, and 8-way power combining PA.

3.4 Measurements

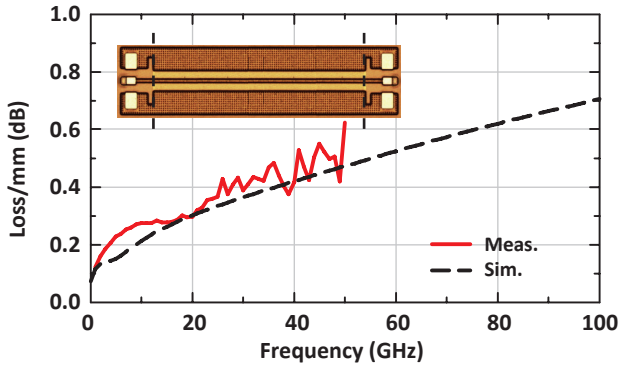
3.4.1 Back-End-of-Line (BEOL)

Several passive and active components were first measured to check the Cadence library models at DC-100 GHz. The measurements are done using standard probe-tip short-open-load-thru (SOLT) calibration. The measurement is then further de-embedded using cascaded open short-thru (C-OST) pad de-embedding to remove the parasitic effects introduced by the G-S-G pads [69].

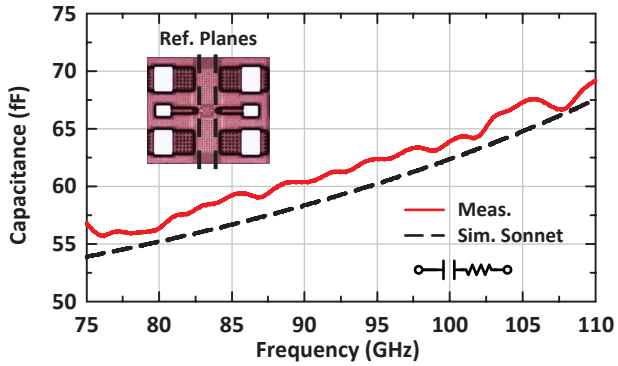
Fig. 3.12(a)-(b) presents measured loss of a 1 mm transmission line and a 70 fF MOM capacitor breakout measurement, and agrees well with simulations. Fig. 3.13 presents the measured S-parameters of a back-to-back balun breakout. In this case, the WR-10 extenders are used at 75-110 GHz, and WR-6 extenders are used for the 110-160 GHz measurements. Calibration is done to the G-S-G probe tips using SOLT standards on a CS-5 calibration substrate for WR-10 measurements, and on a CS-15 calibration substrate for WR-6 measurements. The results include the input and output G-S-G pads loss (measured 1 dB total loss at 120 GHz). The measured insertion loss of the back-to-back balun is $\sim$3 dB at 120 GHz including the pad loss from each side, which results in balun insertion loss of $\sim$1.5 dB including the pad loss. In general, the BEOL measurement results agree well with simulations.

3.4.2 Front-End-of-Line: Transistors

The transistor f_t and f_{max} with emitter lengths of 4, 2$\times$4, 4$\times$4, and 8$\times$4 μm are also measured. The measurement is done using SOLT and on-chip TRL calibration at 0.25-70 GHz. The transistor f_t is acquired using extrapolation of H_{21} from 40-70 GHz, and the f_{max} is acquired using extrapolation of U (Masons unilateral gain) also from 40-70 GHz (Fig. 3.14(a)). The measured f_t and f_{max} are shown in Fig. 3.14(b) for the



(a)



(b)

Figure 3.12: (a) Measured loss of 1 mm microstrip line, and (b) measured capacitance of the series MOM 70 fF capacitor.

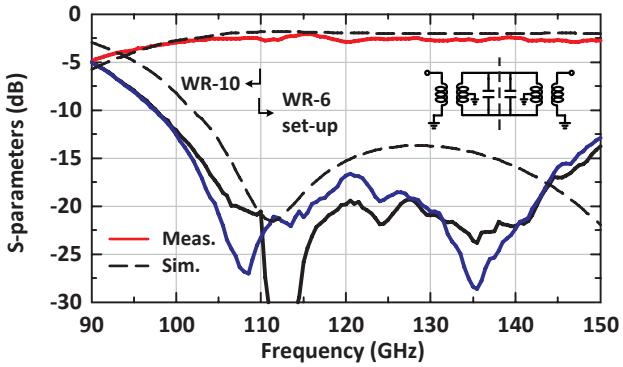
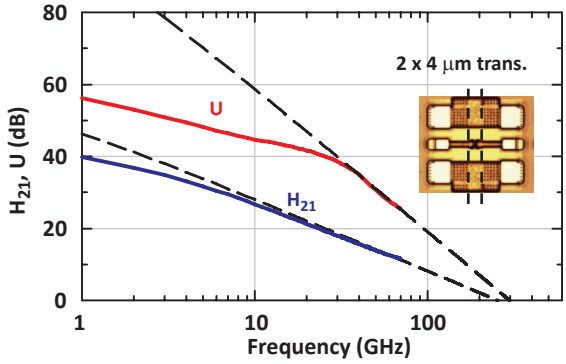
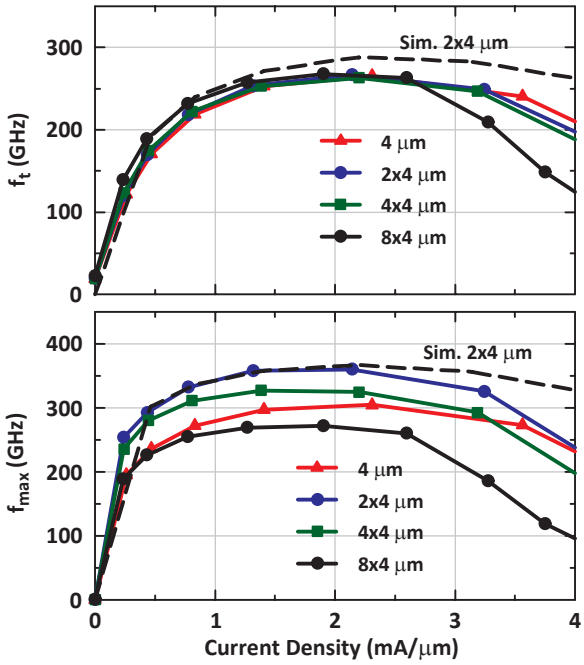


Figure 3.13: Measured S-parameters of the 120 GHz back-to-back balun.



(a)



(b)

Figure 3.14: (a) Measured H_{21} and U of 2×4um transistor and the extrapolation of H_{21} and U from 40-70 GHz, and (b) measured f_t and f_{max} of transistors with emitter length of 4, 2×4, 4×4, and 8×4 μm.

transistors listed above. The measured peak f_t is 270 GHz for all transistors at a current density of 2 mA/μm. The measured peak f_{max} is 360 GHz for the 2×4 μm transistor at current density of 1.5 mA/μm. The 2×4 and 4×4 μm transistors are shown to have a slightly higher f_{max} than the 4 μm cell due to their reduced base resistance. However, the 8×4 μm transistor has a lower f_{max} due to the parasitic capacitance and resistance introduced by the interconnections. Overall, even the 8×4×0.1 μm^2 power transistor maintains an f_{max} >250 GHz and is suitable for power amplifiers at 120 GHz.

3.4.3 Power Amplifiers: S-Parameters

The chip microphotographs of the 8-way power combining PA, single-ended and balanced PAs are shown in Fig. 3.15. The input and output G-S-G pads are designed to be compatible with both 100- and 75-μm-pitch probes for WR-10 and WR-6 measurement setups. The measured small-signal gain of the single-ended PA shows a peak gain of 20 dB at 116 GHz with a 3-dB bandwidth of 110-122 GHz (Fig. 3.16). The balanced PA has a peak gain of 17 dB with a 3-dB bandwidth of 108-126 GHz. The balanced PA gain is ∼3 dB less than the single-ended one due to the input and output balun loss (Fig. 3.16). The 1 dB combined pad loss at input and output ports are included in the measurement. Therefore, there is a 1.3 dB difference between simulations and measurements which is due to the additional transmission-line loss than the value simulated in Sonnet.

The 8-way power combining amplifier has a peak gain of 15 dB at 116 GHz with a 3-dB bandwidth of 108-123 GHz (Fig. 3.17). This is a 2.9 dB difference than the simulated value of 17.9 dB (including pad loss), and is due to the long transmission line used at the input.

The total quiescent power consumption in each case are 143.5 mW (89.7 mA), 288 mW (180 mA) and 1.13 W (710 mA) from an 1.5-1.6 V supply, respectively. Measurements agree well with simulations except for the transmission line loss showing

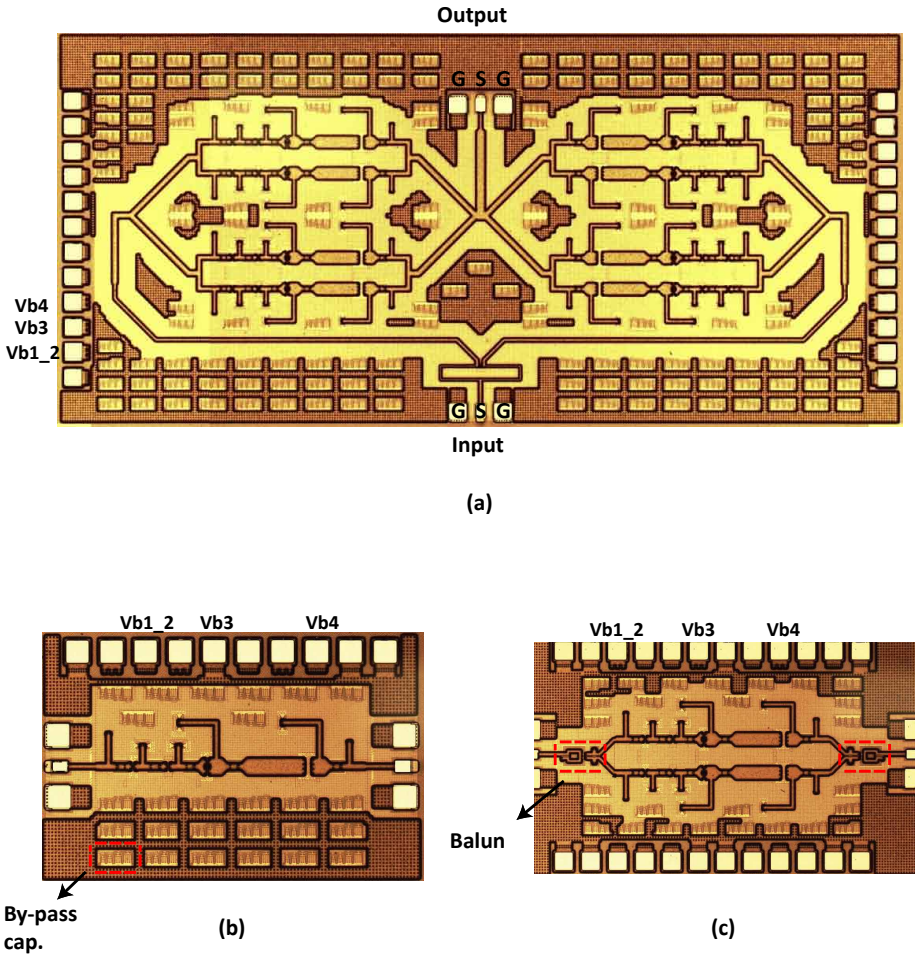


Figure 3.15: Chip microphotograph of (a) 8-way power combining amplifier (3.3×1.5 mm^2 including pads), (b) 120 GHz single-ended amplifier (1.1×0.71 mm^2), and (c) 120 GHz balanced amplifier (1.5×0.86 mm^2). Unlabeled pads are all for ground and Vdd power supply.

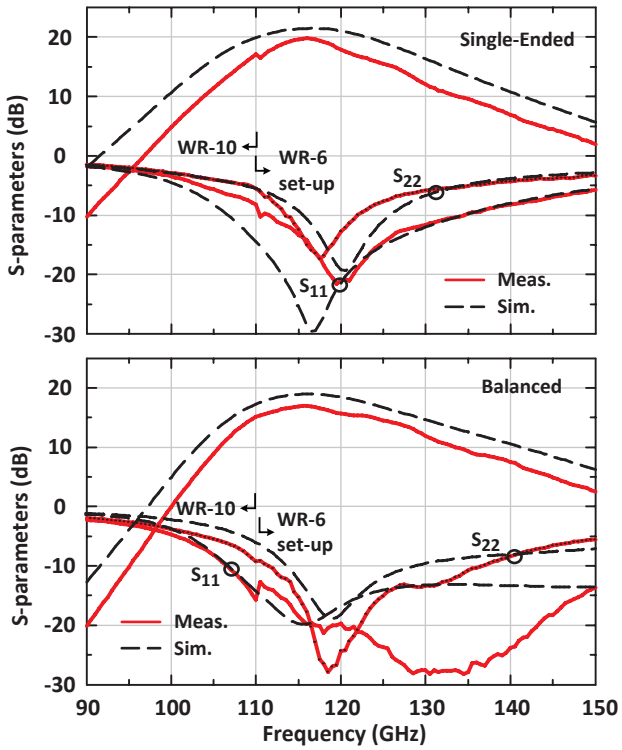


Figure 3.16: Measured S-parameters of the 120 GHz single-ended and balanced amplifier. Input and output pad loss of 1 dB total is taken into account.

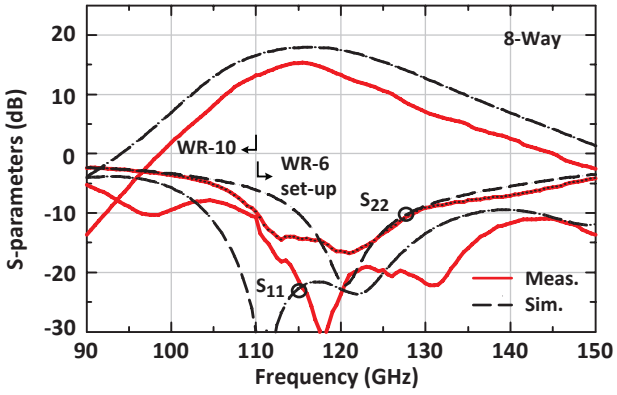


Figure 3.17: Measured S-parameters of the 8-way power combining amplifier. Input and output pad loss of 1 dB total is taken into account.

the accuracy of the Cadence transistor models and the Sonnet EM models.

3.4.4 Power Amplifiers: Power Measurements

Fig. 3.18 presents the large-signal measurement setup. The input 110-130 GHz signal is generated using a multiplier chain and the output power is monitored using PM4 Erickson power sensor [59]. All measurements are referenced to the GSG probe tips, and include the ∼0.5 dB output pad loss.

The output power is first measured at the peak gain frequency of 116 GHz. The single-ended PA results in 13.8 dBm at 116 GHz with a peak PAE of 10%. The OP_{1dB} is 11 dBm with an associated PAE of 8%. The balanced PA results in a power of 16 dBm at 116 GHz with a PAE of 8% when the output balun loss is de-embedded from the measurement (14.5 dBm without de-embedding). The OP_{1dB} is 12.5 dBm with an associated PAE of 5.5% (Fig. 3.19(a)). For the 8-way power-combining PA, a power of 20.8 dBm is achieved with PAE of 7.6% at 116 GHz and with an associated gain of 10 dB (Fig. 3.19(b)). The OP_{1dB} is 17 dBm with an associated PAE of 4%. Fig. 3.20 presents the measured bias current v.s. input power and the amplifiers clearly operate in class AB mode. The currents at OP_{1dB} and P_{sat} are 20% and 50% higher than the quiescent conditions.

The same setup is used for power-frequency measurements, and is calibrated to

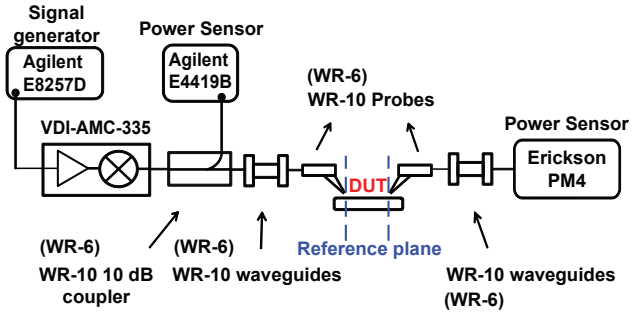


Figure 3.18: Power measurement setup.

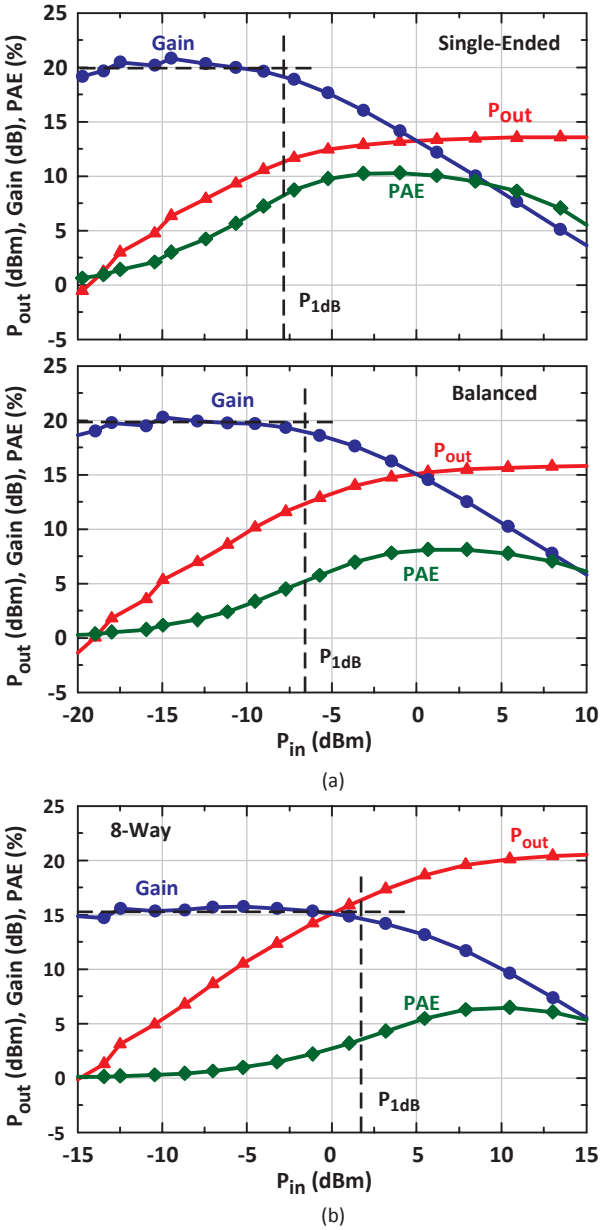


Figure 3.19: (a) Measured output power, gain, and PAE vs input power of the single-ended and balanced amplifier, and (b) the 8-way combined amplifier at 116 GHz.

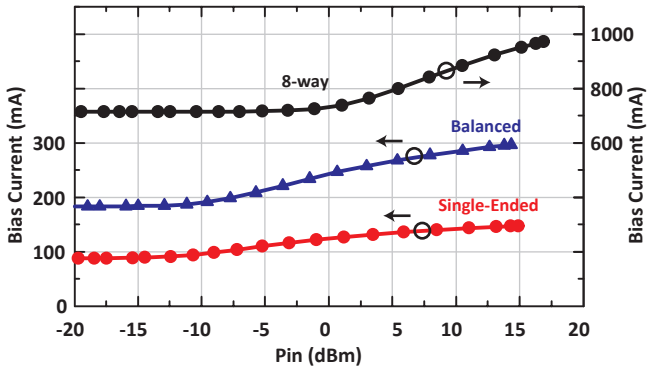


Figure 3.20: Measured bias current vs input power at 116 GHz.

the probe tips by carefully de-embedding the input and output losses at 110-140 GHz. The measured P_{sat} for the single-ended PA is >10 dBm at 114-134 GHz with 13.8 dBm at 125-126 GHz. Measurements on the balanced PA show >12.5 dBm at 110-136 GHz with 17.5 dBm at 124-15 GHz and the output balun loss removed (Fig. 3.21). The 8-way power-combining PA achieves a P_{sat} >17 dBm at 112-130 GHz (Fig. 3.22). In particular, the 8-way power combining amplifier results in 20-20.8 dBm at 114-126 GHz, which is the highest power achieved from any silicon technology. The corresponding large-signal gain at P_{sat} is 10 dB with a peak PAE of 7.6% at 114 GHz, and the PAE remains > 6.3% at 114-126 GHz. The 8-way power combining amplifier delivers a P_{sat} >15 dBm from 110 to 134 GHz.

Table 3.1 summarizes the measured results and compares this work with recently published amplifiers. The 8-way power-combining PA shows the highest output power in this frequency.

3.5 Conclusions

This paper presented a high-power SiGe amplifier at 110-134 GHz with reactive power division at the input and reactive power combining at the output. The three-stage reactive combiner results in a loss of 1-1.2 dB at 120 GHz for 8-amplifiers, and

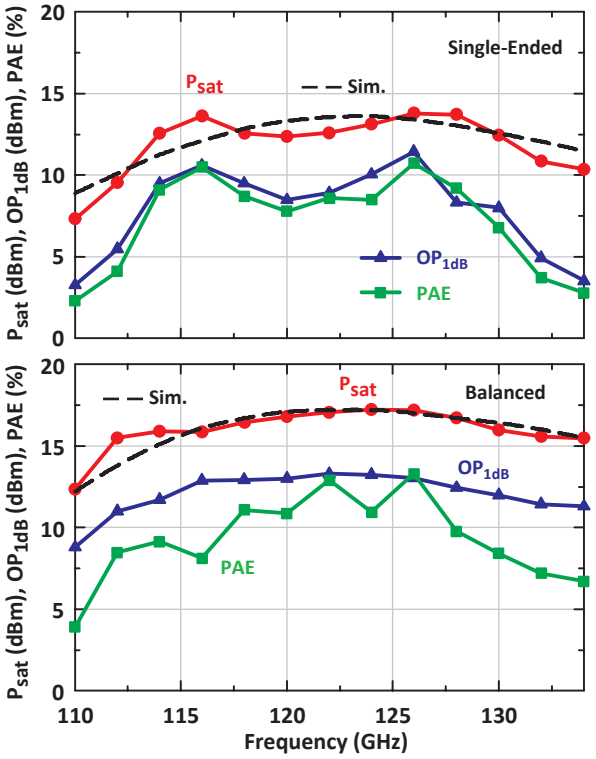


Figure 3.21: Measured P_{sat}, OP_{1dB} and peak PAE vs frequency of the single-ended and balanced PA.

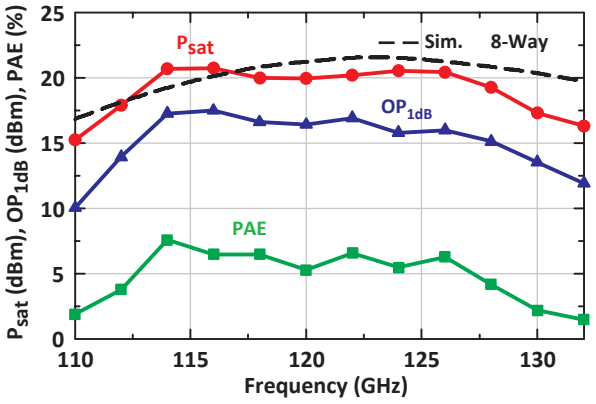


Figure 3.22: Measured P_{sat}, OP_{1dB} and peak PAE vs frequency of the 8-way combined amplifier.

Table 3.1: Performance Summary for Amplifiers Above 100 GHz

Freq. (GHz)	**Tech.**	**Type**	**P_{sat} (dBm)**	**Peak Gain (dB)**	**OP_{1dB} (dBm)**	**Peak PAE (%)**	**P_{dc} (W)**	**Ref.**
114-134	90-nm SiGe	4-stage Single-Ended	13.8	20	11	11.6	0.2[1]	This work
114-134	90-nm SiGe	4-stage Differential	17[2]	20[2]	12.5[2]	12.5[2]	0.48[1]	This work
110-134	90-nm SiGe	4-stage 8-way Comb.	20.8	15	17.0	7.6	1.52[1]	This work
160	130-nm SiGe	3-stage Differential	11.5	32	8.5	-	-	[70]
130	130-nm SiGe	3-stage Single and Diff.[3]	7.7	24.3	6	6.8	0.08	[71]
90-98	130-nm SiGe	Quasi-optical Power Comb. 4-stage	21-23[4]	21.5	-	5.8	3.3	[25]
140	65-nm CMOS	4-stage 8-way Comb.	13.2	15	9.9	14.6	0.12	[67]
110-117	65-nm CMOS	3-stage Differential	13.8	15	10.1	10	0.19	[72]
90-100	65-nm CMOS	3-stage 16-way Comb.	18.3	12.5	17.5	9.5	-	[67]
110	100-nm GaAs	2-stage Common Source	7	10	3	7.8	0.04	[45]
128	100-nm InP	5-stage 2-way Comb.	15	25	13	4.7	-	[**?**]
214	250-nm InP	3-stage 16-way power comb.	22.5	22	9.5	-	12.9	[73]

[1] At P_{sat}.
[2] Balun loss deembedded.
[3] 1^{st} stage is single-ended. 2^{nd} and 3^{rd} are differential.
[4] Output power referred to chip is used.

is much better than Wilkinson power combining. This topology can be extended to 250-300 GHz with advanced SiGe technologies and result in silicon amplifiers capable of delivering an output power of 20-30 mW at near THz frequencies. Future work includes packaging the chips using bond-wires, flip-chip, or embedded wafer-level package (eWLP) technologies.

3.6 Acknowledgements

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Chapter 3 is mostly a reprint of the material as it appears in IEEE Transactions on Microwave Theory and Techniques, 2014. Hsin-Chang Lin and Gabriel M. Rebeiz. The dissertation author was the primary author of this material.

Chapter 4

A 200-230 GHz SiGe Multiplier with Peak Output power of 5-7.8 dBm

4.1 Introduction

Millimeter-wave systems above 120 GHz has been in active development in the past few years and significant progress has been made to enable complex communication and radar systems to operate at this frequencies. For example, high data-rate communication systems with OOK, QPSK and 16 QAM modulation schemes have been demonstrated using SiGe, CMOS, and III-V technologies up to 340 GHz [1, 74, 75, 76, 77]. Other applications are in radar, security, and imaging systems, which have higher spatial resolution due to the shorter wavelengths at 150-500 GHz [78, 9, 6, 79, 80].

Advanced CMOS and SiGe currently result in transistor cut-off frequencies f_t and f_{max} up to 300-400 GHz, and provide low-cost, high-yield and high-integration solutions. However, the transmit power is still in the 0-5 dBm at $>$200 GHz since the power amplifiers operate close to f_t and f_{max} and provide low gain and poor P.A.E. (power added efficiency). Therefore, signal generation at $>$200 GHz is usually implemented using

high frequency oscillators (or harmonic oscillators) and wideband frequency multipliers [81, 34, 82, 83, 84, 4, 85, 35, 36, 37, 68].

However, oscillators operating at >200 GHz usually have poor phase noise and require high frequency dividers to lock to a reference. These dividers are very challenging at >150 GHz and very few publications exist[86]. Another approach is frequency multipliers, which result in better phase noise and wideband power generation.

The output power of oscillators and multipliers is quite low at >200 GHz and power-combining technique are essential. Voltage/current combining using transformers [20, 22, 24, 70], current combining using Wilkinson combiners or T-junctions [15, 16, 17, 18, 19], and spatial combining using on-chip antennas [25, 26, 87, 27, 88], have all been demonstrated to increase the output power from the chip, and with various degrees of combining efficiency.

In this work, a 4-way reactively power-combined multiplier with low-loss current combining networks is presented (Fig. 4.1). The output combining network is based on λ/4 microstrip transmission lines. The multiplier unit cell is implemented using an active balanced transistor pair with double Vcc stubs for better harmonic suppression. A pseudo-differential 4-stage common emitter amplifier with a wide-band balun is used as the driver amplifier for the multiplier cell. The 4-way power combining multiplier results

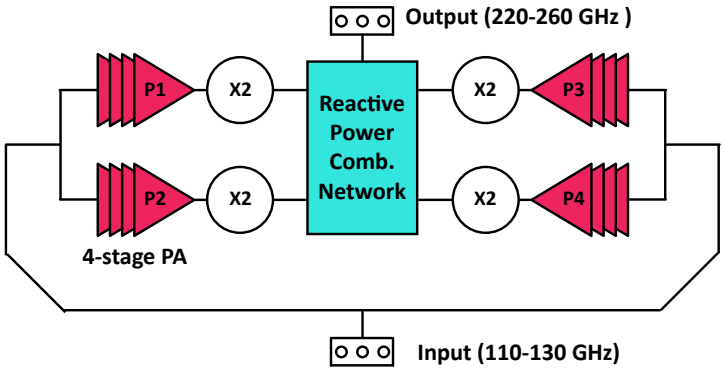


Figure 4.1: Reactive power combining for 220-260 GHz signal generation.

a peak output power of 8 dBm and $>$ 5 dBm at 200-230 GHz.

4.2 Technology

The IBM 9HP BiCMOS process [53] is chosen for this design. It is a 90 nm SiGe HBT process built on top of a 90-nm CMOS process, with a 10-layer copper metal backend and high-density metal-insulator-metal (MIM) capacitors (12.2 fF/ μm^2). The 4$\times$0.1 μm^2 transistor model with a single emitter finger, dual collector and base fingers (C-B-E-B-C) results in a peak f_t/f_{max} of 310/350 GHz at 1.5-2.5 mA/μm bias current when referred to M1 [54], and f_t/f_{max} drops to 260/300 GHz when referred to top metal LD due to the interconnection parasitics [16, 89]. This is much better than CMOS transistors which typically reduce the f_t/f_{max} from 460 GHz (referred to M1) to 260 GHz (referred to top metal)[56]. The better performance is due to the all-copper back-end and the thick dielectrics used in the IBM 9HP process.

Fig. 4.2(a) presents the 50 Ω microstrip transmission line for matching stubs and power combining and distributing networks. It is implemented using the top metal LD with 10 μm width and M2_4B as the ground plane (M1_4B as the Vcc plane). EM (electromagnetic) simulations using Sonnet show a loss of 0.71-1.06 dB/mm at 125-250 GHz (0.86-1.3 dB/mm for a G-CPW line at these frequencies) (Fig. 4.2(b)). The corresponding transmission-line Q is 32-41 at 125-250 GHz (25-35 for a G-CPW at 125-250 GHz). In practice, and from different measurements done on IBM 8HP and other processes, the actual loss is about $\sim$30% higher than simulated. Still, a loss of 0.71-1.06 dB/mm at 125-250 GHz is taken for the 50 Ω microstrip lines in the Cadence and Sonnet[55] simulations since there are no measurements in our group for this process at mm-wave frequencies.

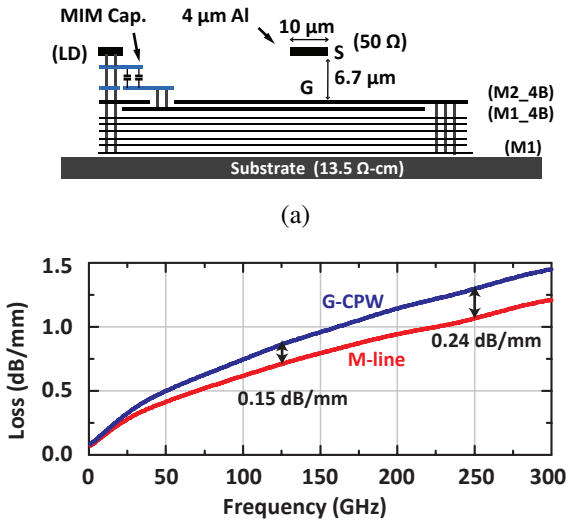


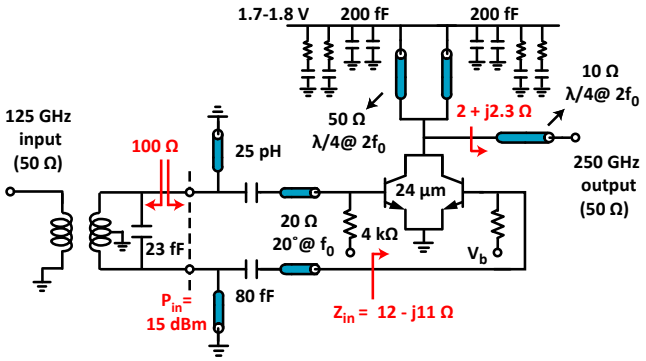
Figure 4.2: (a) 50 Ω microstrip transmission line implemented using top metal LD with M2_4B as ground plane, and (b) simulated loss.

4.3 design

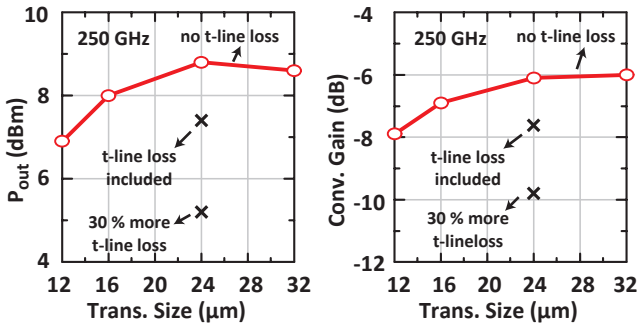
4.3.1 250 GHz Doubler Unit Cell

Fig. 4.3(a) presents the schematic of the active balanced doubler. The doubler is designed to deliver maximum output power at 250 GHz with an input power at 125 GHz. The single-ended input is converted to differential using an passive balun and fed into the balanced transistor pair. The collector nodes are connected together to combine all the even harmonics from the transistor pair, and create a broadband short circuit for the fundamental and the odd harmonics.

The transistor size is optimized using Cadence library models for maximum output power and conversion gain for an input power of 14-15 dBm (Fig. 4.3(b)). Note that this optimization is first done without taking into account the input and output matching networks loss and using an ideal lossless balun. This power is selected because the 115-130 GHz power amplifier (PA) is capable of delivering 14-16 dBm when operating



(a)



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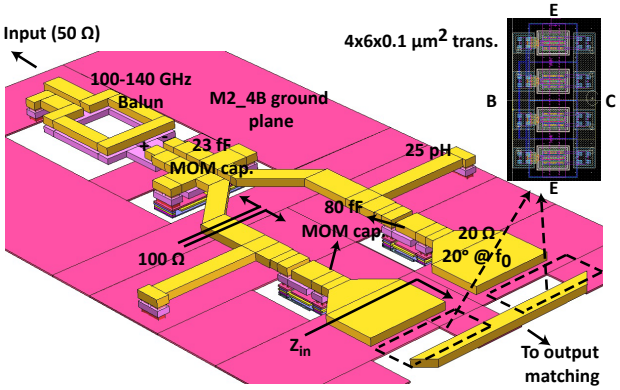


(c)

Figure 4.3: (a) Schematic of 250 GHz doubler, (b) simulated 2^{nd} output power and conversion gain v.s. transistor size with P_{in} = 15 dBm, and (c) Sonnet EM modeling for the input matching network of the doubler unit cell.

in differential mode [16] without the use of a balun. Transistors with total widths of 24 μm result in an output power of 8.8 dBm and conversion gain of -6.2 dB at 250 GHz with an input power of 15 dBm. A 24 μm wide transistor is chosen for the final design since the 32 μm transistor would have resulted in a very small output impedance ($< 1\ \Omega$).

The 24 μm transistors are implemented using four smaller and high-f_t $6\times0.1\ \mu m^2$ transistor with CBEBC configuration and deep-trench isolation ring. The transistor bias condition should be set to result in a conduction angle of 125° to maximize the second harmonic at the output [90]. Therefore, the transistor base is biased at V_b = 0.8 V (just below threshold) for optimum doubler operation.

Fig. 4.3(c) presents the EM model for the doubler input matching network. The 100-140 GHz balun, 23 fF shunt metal-oxide-metal (MOM) capacitor, 25 pH short stubs, and 80 fF series MOM capacitor at the input matching network are all modeled using Sonnet. The input impedance looking into the balanced transistor base nodes (Z_{in} = 12-j11 Ω at 125 GHz) is transferred to 100 Ω differentially using 20 Ω 20^{O} transmission lines, 80 fF series MOM capacitors (LD to M1_2B), and 25 pH stubs (shorted 50 Ω microstrip lines with Q of 18 at 125 GHz). Care is taken to achieve a symmetrical layout.

Double λ/4 Vcc stubs are chosen over a single Vcc stub for collector biasing because they present a symmetrical environment, which suppress the unwanted odd harmonics when the signals are combined at the collector nodes (Fig. 4.4). With this design, the 1^{st} and 3^{rd} harmonic levels are 58 dB lower than the 2^{nd} harmonic level. Note that, in this analysis, an ideal differential signal is used to drive the balanced transistor pair. The stubs are followed by dual 200 fF MIM (metal-insulator-metal) capacitors which are operating close to self resonance and providing a very low impedance ($\sim$1 Ω) at 230-270 GHz. The stubs + MIM capacitors present an open circuit ($>$ 200 Ω) to the low impedance collector node (2-j2.7 Ω), and are used as RF chocks which eases the implementation of the output matching network [57].

Fig. 4.5 presents the output power contours of the balanced multiplier at 250 GHz with an input power of 15 dBm. An optimal load impedance of 2+j2.3 Ω for maximum 2^{nd} harmonic power transfer is shown in the analysis. This is achieved at the collector nodes by transferring the 50 Ω output port using a low-loss 10 Ω ∼λ/4 transmission line at $2f_0$ (w: 96 μm, ℓ: 172 μm, and loss: 0.12 dB at 250 GHz).

At an input power of 15 dBm, the balanced doubler results a simulated output power of 7.4 dBm at 250 GHz with a conversion gain -7.6 dB including the losses from input and output matching networks. Note that the results here are done using an ideal lossless balun since the doubler will be directly driven by a differential amplifier. The simulated peak output power is 7-8 dBm at 247-270 GHz and is >5 dBm at 234-280 GHz. All unwanted harmonics are 50 dB below the 2^{nd} harmonics when double Vcc stubs are used. The output power and conversion gain at 250 GHz drop to 5.2 dBm and -9.8 dB when 30% additional transmission-line loss are added to the matching networks. The doubler consumes 16 mA in small signal condition and 40 mA in large signal from a 1.7 V supply.

4.3.2 250 GHz 4-Way Combined Doubler

The multiplier is implemented using 4 doubler cells and λ/4 impedance transformation networks at output. Four pseudo-differential PAs are implemented using 8 single-ended 4 common-emitter gain stages (see [16] for detailed PA design). The baluns are connected at the PA inputs so as not to result in a 1.5 dB loss between the PAs and the doublers (Fig 4.6).

At the input port, a Wilkinson power divider is first used to divide the RF signal to the left and right circuits with isolation. Then, a 1.5 mm long 50 Ω transmission line is employed together with a 35 Ω λ/4 line and T-junction network to present 50 Ω to the input of each balun. Finally, the balun converts the single-ended signal to a differential

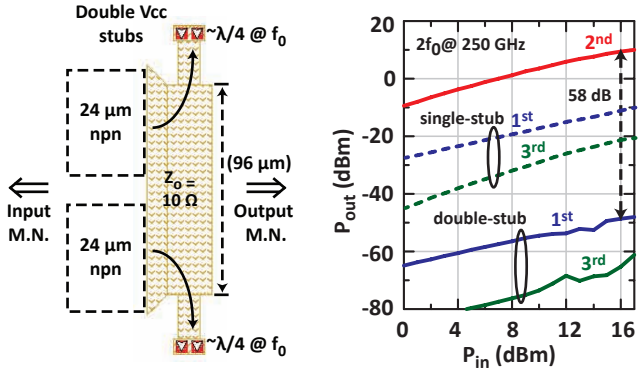


Figure 4.4: Double Vdd stubs are used for better odd-order harmonic suppression.

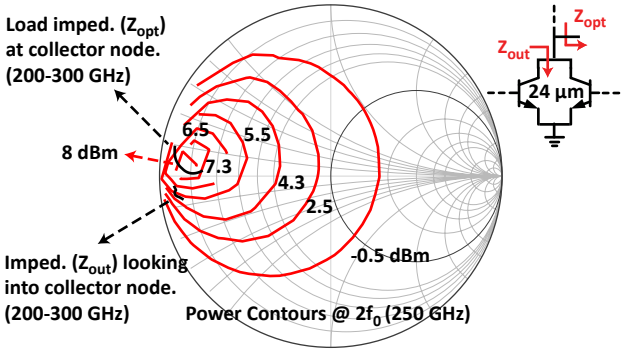


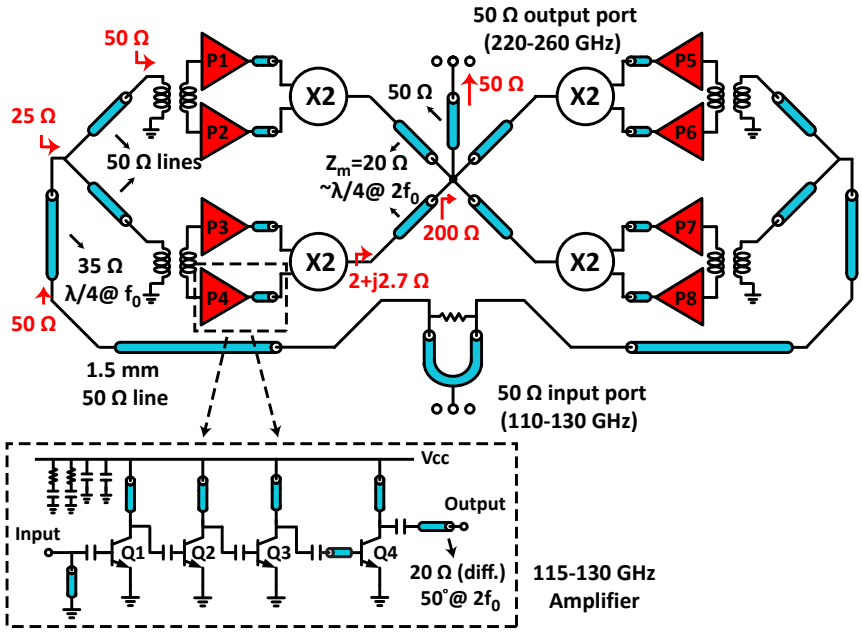
Figure 4.5: Load-pull contours of 24 μm balanced multiplier at 250 GHz with input power of 15 dBm (t-line loss not included).

signal at the input of the PAs. The balun is designed using the top metal (LD) for the first core and the second metal (OL). The shunt 25 fF MOM capacitor implemented using LD to M2_2B, is connected to the differential port of the balun to achieve simultaneous matching at the input (50 Ω) and output ports (100 Ω). The simulated balun insertion loss is <1.5 dB at 100-140 GHz, and the amplitude and phase imbalance are <0.4 dB and 5^{O}, respectively, at 100-140 GHz (see [16] for detail).

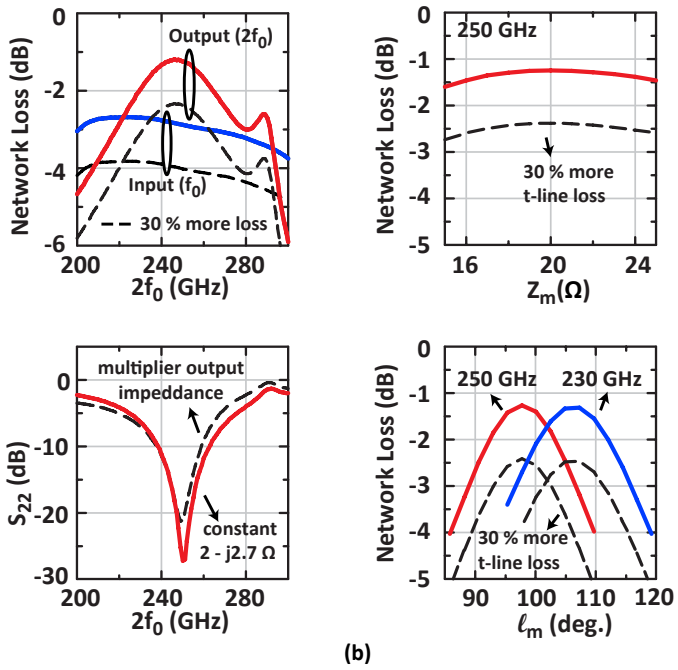
A new matching network is now used between the pseudo-differential PA and the doubler (Fig 4.6(a)). This network matches the doubler input impedance 12-j11 Ω to the PA optimal load impedance (21+j20 Ω) for maximum power delivery (15-16 dBm), and consists of a differential-line with Z_0 (diff) = 20 Ω and $\ell = 50^{\circ}$.

The goal of the output combining network is to present 2+j2.7 Ω to the output of each doubler cell, and is designed as follows: the doubler cell output impedance of 2-j2.7 Ω at 250 GHz is transferred to 200 Ω using a 98° 20 Ω transmission line. Four doubler cells are then connected in a star-junction at the output common node to form a ∼200/4 = 50 Ω impedance. An extra 150 μm-long 50 Ω line (0.16 dB loss at 250 GHz) is connected to this common node in order to use a GSG (ground-signal-ground) pad for measurements.

The output λ/4 power combining networks are relatively wideband and with low ohmic loss. The bandwidth and loss are studied as follows: the output impedance of the doubler is assumed to be constant versus frequency (2-j2.7 Ω), and the combining loss and S_{22} are simulated for the λ/4 star-junction network using Sonnet. A loss of 1.25 dB is found at 250 GHz, and is < 2 dB at 230-265 GHz. The loss increases to 2.35 dB at 250 GHz for a 30% additional line loss. The S_{22} is <-10 dB at 240-260 GHz. The results are similar when the actual doubler output impedance is used versus frequency. The input network loss is 2.7-3.2 dB at 100-140 GHz (0.3-0.4 dB for the Wilkinson divider, 1.1-1.2 dB for the 1.5 mm long transmission line, 0.5-0.6 dB for the λ/4 T-junction



(a)



(b)

Figure 4.6: (a) Schematic of 4-way combined 250 GHz doubler, and (b) input and output network loss and sensitivity to Z_m and ℓ_m.

network, and 0.9-1 dB for the balun), and increases to 3.8-4.3 dB for 30% additional line loss.

The sensitivity of the output combining network is also studied by varying the impedance (Z_m) and electrical length (ℓ_m) of the 20 Ω ~λ/4 (98°) transmission line. The output network loss is not sensitive to the Z_m, and is 1.6-1.25 dB for Z_m = 15-25 Ω (2.75-2.4 dB for 30% additional loss). On the other side, the output loss is sensitive to ℓ_m, and varies from 2.6-1.25 dB for ℓ_m = 90-105°. This sensitivity can also be considered as a frequency shift since the network loss is again 1.25 dB for ℓ_m = 108° but for f_0 = 230 GHz. The sensitivity to ℓ_m is due to the large ~λ/4 line length and impedance ratio between the multiplier output (2-j2.7 Ω) and the 200 Ω at the star-junction.

At an input power of 3 dBm at 125 GHz and an power power of ~15 dBm at the PA output, the 4-way combined doubler results a simulated peak 2^{nd} harmonic power of 12.1 dBm at 250 GHz and is ≥ 10 dBm at 232-260 GHz with peak conversion gain of 0-3.4 dB (Fig. 4.7). All the unwanted harmonics are <-25 dB below the output power at 220-270 GHz including the balun response. The output power at 250 GHz drops to 9.9 dBm and is ≥ 7 dBm at 230-260 GHz when 30 % additional transmission-line loss is used. The 4-way combined doubler consumes 1.3 A (200 mA in doublers and 1100 mA

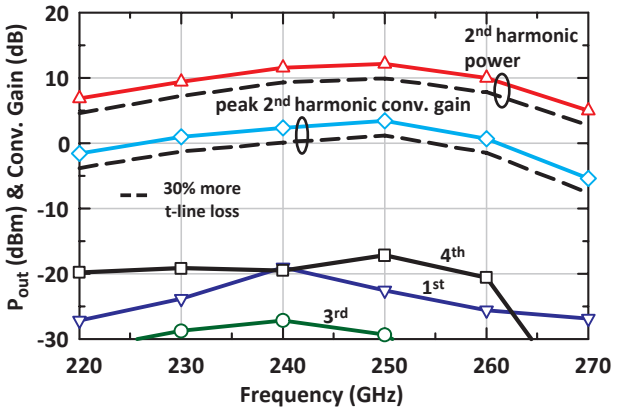


Figure 4.7: Simulated 2^{nd} harmonic power and peak conversion gain versus frequency together with other unwanted harmonics (P_{in} = 3 dBm at 110-135 GHz).

in PAs) at large signal from a 1.7 supply.

Electrostatic discharge (ESD) diodes are implemented at the bias control pins for the amplifiers. There is no ESD protection on the RF path to avoid the extra parasitics due to the diode capacitance loading. A large amount of VDD pads are used for the 4-way combined multiplier to distribute the current evenly throughout the chip.

4.4 Measurements

The microphotographs of the 250 GHz 4-way combined multiplier, 250 GHz doubler breakout, and the 125 GHz single-ended PA breakout are shown in Fig. 4.8. The input and output G-S-G pads are designed to be compatible with both 100- and 75-μm-pitch probes for WR-10, WR-6, and WR-5 measurement setups. The S-parameters are measured using three different setups for three different frequency bands: 1) an Agilent 50 GHz VNA and mm-wave head controller are used with VDI WR-10 extenders at 70-110 GHz (Fig. 4.9). 2) OML WR-6 extenders and 3) VDI WR-5 extenders are used for measurement at 110-170 GHz and 140-225 GHz, respectively. Standard short-open-load-thru (SOLT) calibration is done to the G-S-G probe tips for the WR-10 setup on a CS-5 calibration substrate, and on a CS-15 calibration substrate for the WR-6 and WR-5 setups. The S-parameters are referred to the probe tips, and include the G-S-G pad loss (0.4-0.7 dB each at 110-225 GHz).

Fig. 4.10 presents the power measurement setup for the doubler circuits. The input 100-130 GHz signal is generated using VDI-AMC 332-334 multiplier chains and the output power is monitored using PM4 Erickson power sensor [59]. The WR-6 GSG probe loss is measured using a short thru on the SiGe wafer, and is 9-6.4 dB at 110-125 GHz. This means that the probe loss + GSG pad loss (0.4 dB) is 4.5-3.2 dB each at 110-125 GHz, and agrees well with the 4-2.5 dB loss provided by the manufacturer

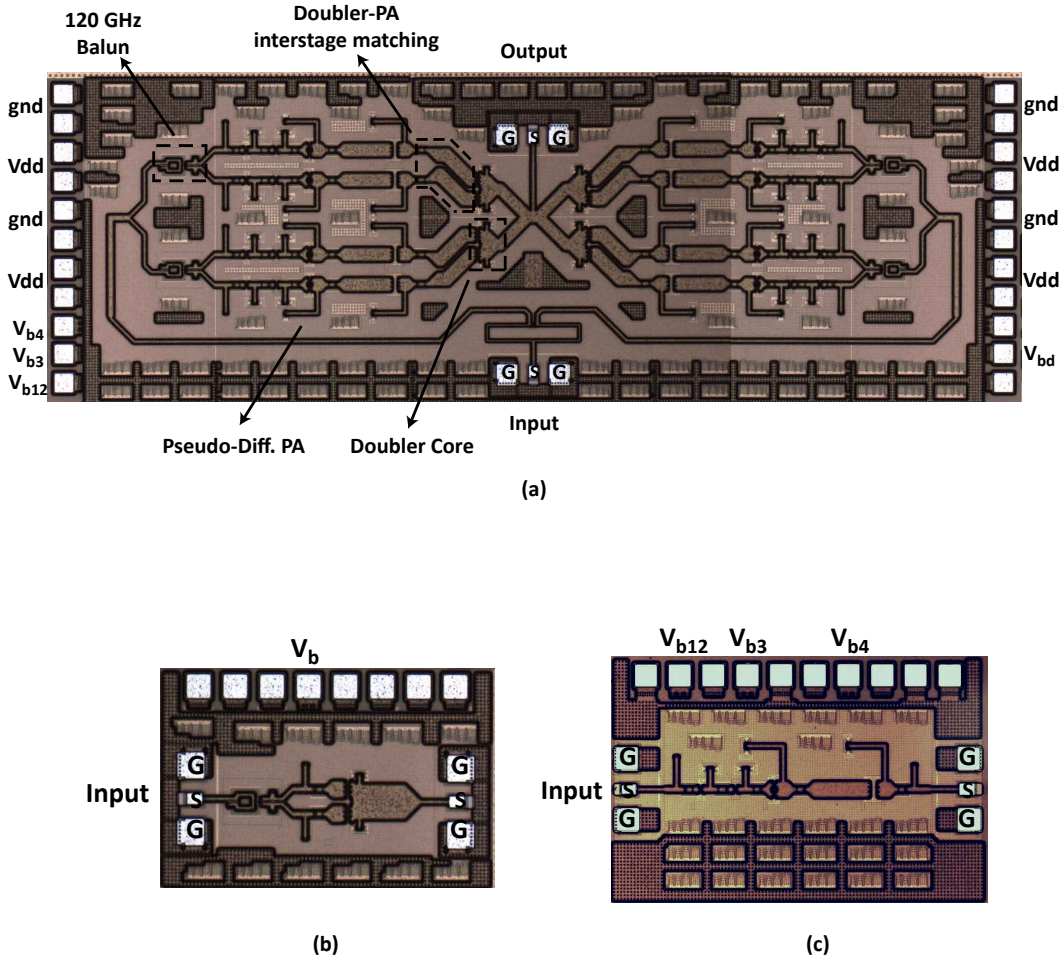


Figure 4.8: Chip photos for (a) 250 GHz 4-way combined multiplier (3.3×1.1 mm^2 including pads), (b) 250 GHz doubler breakout (0.9×0.6 mm^2), and (c) 125 GHz PA breakout (1.1×0.7 mm^2).

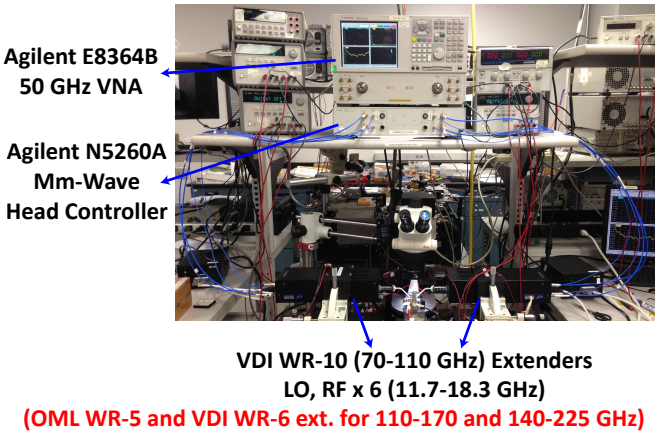


Figure 4.9: 70-110 GHz S-parameter measurement setup.

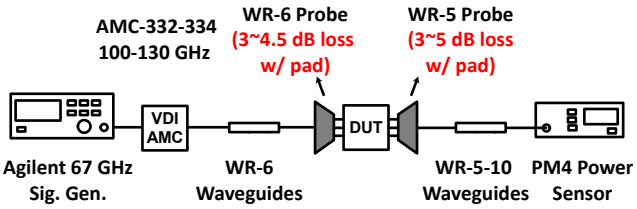


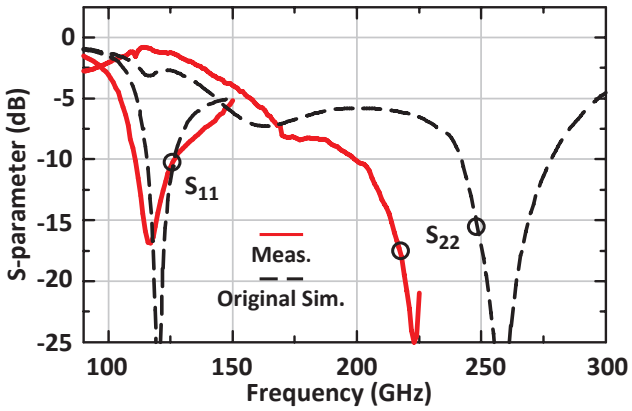
Figure 4.10: Power measurement setup for the 250 GHz multiplier.

data sheet [60]. Similar measurements are done for the WR-5 GSG probe, and the measured probe loss + pad loss (0.6-0.7 dB) is 3.4-4.8 dB at 210-250 GHz. All power measurements are referenced to the G-S-G pad on the SiGe wafer.

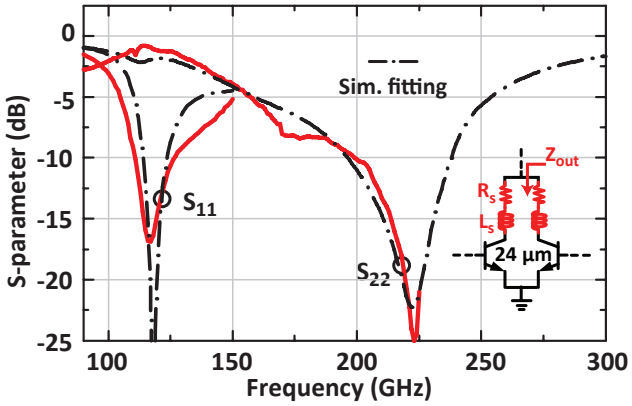
4.4.1 250 GHz Single Doubler

The measured doubler S_{11} and S_{22} are <-10 dB at 108-125 GHz and 200-225+ GHz, respectively (Fig. 4.11(a)). There is a shift in the resonance frequency between the measured and simulated S_{22}, and this is due to transistor modeling inaccuracy. Since the doubler output matching network is using a $\sim\lambda/4$ transmission line and assuming the back-end-of-line (BEOL) does not vary much with process, the shift in S_{22} can be studied by changing the output impedance (Z_{out}) of the doubler. A series L_s is first added to the 24 μm transistor collector node for fitting the frequency difference, and then a series R_s is added to the collector node for fitting the magnitude difference. The simulated S_{22} with L_s = 6 pH and R_s = 3 Ω ($R_s/2$ = 1.5 Ω for the doubler pair) agrees well with measurements (Fig. 4.11(b)), and results in Z_{out} = 3.5 + j2 Ω (instead of simulated Z_{out} = 2 - j2.7 Ω) at 250 GHz. This fit also takes into account any modeling inaccuracies from Sonnet or any shift in the dielectric BEOL.

Fig. 4.12 presents the measured output power and conversion gain of the doubler versus input power at 250 GHz. In this case, the input balun and its 1.5 dB loss are included in the simulations and measurements. Simulations with L_s = 6 pH and R_s 3 Ω are also applied for fitting. The effect of L_s and R_s is a drop in the conversion gain from -10 dB to ∼-15 dB and is partly due to $R_s/2$ = 1.5 Ω and the doubler Z_{out} = 2 - j2.7 Ω. The output power v.s. frequency is ≥ -1 dBm at 222-250 GHz with a peak value of 1.8 dBm at 245 GHz. The measured fundamental leakage is <30 dB from 100-130 GHz. The dip at 220 GHz is due to a low available power at 110 GHz (≤ 12 dBm at the GSG pads), and the resulting output power is -4 dBm. The available input power at other frequencies



(a)



(b)

Figure 4.11: Measured S_{11} and S_{22} of 250 GHz doubler (a) with original simulations, and (b) with simulations after fitting (L_s = 6 pH and R_s = 3 Ω).

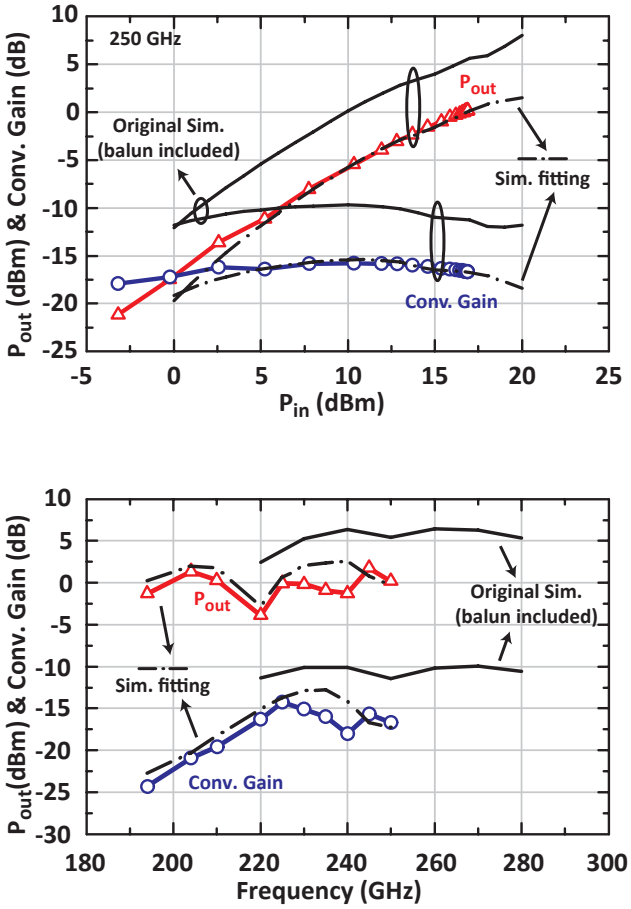


Figure 4.12: Measured output power and conversion gain v.s. input power at 250 GHz, and peak output power and associated conversion gain v.s. frequency of doubler breakout.

is 15-17 dBm at the GSG pads. The doubler breakout consumes 22 mA at small-signal and 50 mA at peak output power from a 1.8 V supply.

4.4.2 110-135 GHz Single-Ended PA

The measured small-signal S-parameters for the 110-135 GHz PA are shown in Fig. 4.13. Again, a shift in frequency is observed between simulations and measurements. Also, note that a shift in frequency is also found between the measured S-parameters in this work and from an identical PA built previously [16]. To fit the simulations with measurements, $L_{s,amp}$ = 7 pH is added to the collector node of the 32 μm transistor (Q4), 2×$L_{s,amp}$ to the 16 μm transistor (Q3), and 4×$L_{s,amp}$ to the 8 μm transistor (Q2 and Q1). The fitted simulations agree with measurements, and especially S_{11} and S_{22}. The measured peak small-signal gain is 19.3 dB at 110 GHz with a 3-dB bandwidth of 105-117 GHz.

Fig. 4.14 presents the amplifier measured P_{sat} (saturated output power) versus frequency, and is ∼12 dBm at 110-115 GHz. This results to 15 dBm of power available at doubler for 220-230 GHz operation. The PA breakout consumes 120 mA at small-signal and 180 mA at P_{sat} from a 1.8 V supply.

4.4.3 250 GHz 4-way Combined Multiplier

Fig. 4.15 presents the measured S_{11} and S_{22} of the 4-way combined multiplier. L_s, R_s, and $L_{s,amp}$ are applied for the fitted simulations. The measured S_{11} is <-10 dB from 96-155 GHz, and S_{22} is <-10 dB at 212-233 GHz. The 4-way combined multiplier results in > 5 dBm at 200-230 GHz with a peak of 8 dBm at 215 GHz. The peak conversion gain is > -5 dB at 200-230 GHz with a peak of 1.6 dB at 215 GHz (Fig. 4.16(b)). The measured fundamental leakage is <-25 dBc.

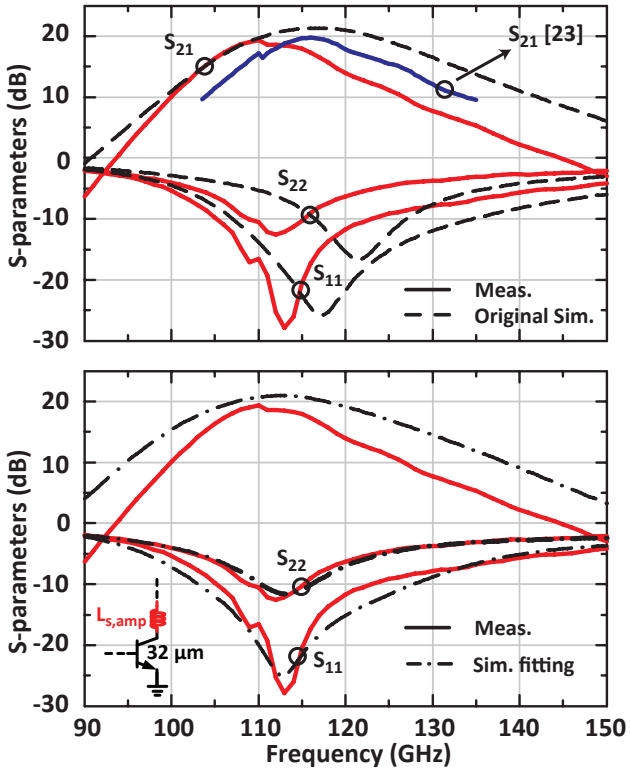


Figure 4.13: Measured S-parameters of 120 GHz PA and comparison with previous work.

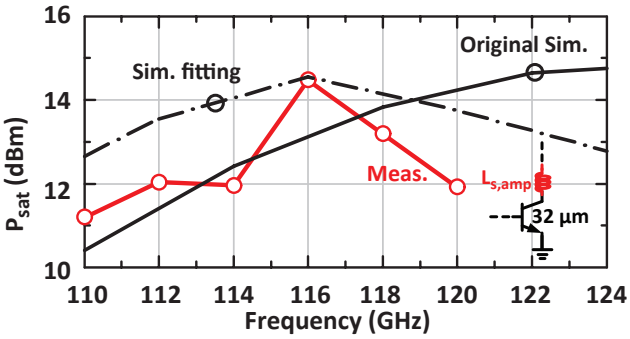


Figure 4.14: Measured P_{sat} v.s. frequency of PA breakout..

A frequency shift occurred from 240-250 GHz to 215-220 GHz due to the transistor modeling with L_s and $L_{s,amp}$, and the $\sim\lambda/4$ (98°) 20 Ω star-junction. Still, a high output power was achieved at 200-230 GHz.

At 215-220 GHz, the multiplier results in a peak output power of 8 dBm with an associated conversion gain of -4.7 dB. Also, a peak conversion gain of 1.6 dB is obtain at P_{in} = -3.6 dBm with an output power of -2 dBm (Fig. 4.16(a)). The 4-way combined doubler consumes 1.5 A from a 1.8 V supply.

Table 4.1 compares different millimeter-wave sources, amplifiers and multipliers at 200-300 GHz. This work results in the highest output power among other SiGe and CMOS chips at >200 GHz.

4.5 Conclusions

The goal of this work was to achieve an output power of 11-13 dBm at 230-260 GHz using an advanced SiGe process, wideband multipliers fed by differential 110-130 GHz power amplifiers, and reactively 4-way power combining at 240 GHz. Measurements showed a frequency shift to 200-230 GHz with an output power of 5-8 dBm, which is still a record, but 4-5 dB lower than predicted. There are several reasons for this: a) transmission-line loss higher than the values provided in the IBM design kit for frequencies above 200 GHz, b) inaccurate transistor models and interconnect EM modeling from M1 to the top metal which can result in added resistance (1-2 Ω) and inductance (6-7 pH), c) inaccurate electromagnetic modeling of the 10-20 Ω transmission lines used for matching and the star junction, and d) variation from run to run in the IBM9HP process since it is not fully qualified for production release. Also, in hindsight, it would have been better to use a smaller transistor for the multiplier cell (16 μm instead of 24 μm) so as to result in a higher output impedance and less sensitivity to matching

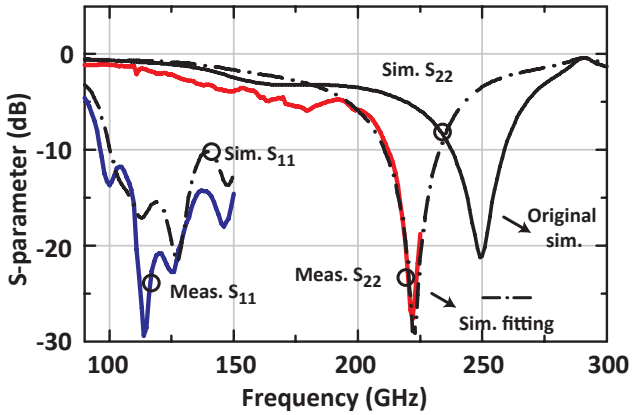


Figure 4.15: Measured S_{11} and S_{22} of 4-way combined doubler.

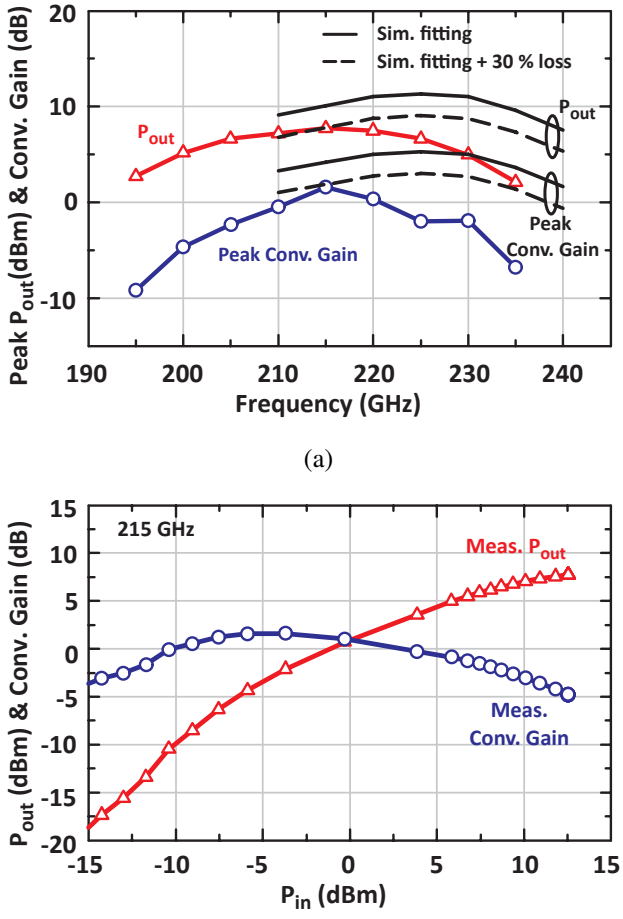


Figure 4.16: 4-way power-combined multiplier: (a) measured peak P_{out} and peak conversion gain versus frequency, and (b) measured output power and conversion gain versus input power at 215 GHz.

Table 4.1: Performance Summary for Doublers and Amplifiers at 180-300 GHz

Frequency (GHz)	**Technology**	**Source Type**	**Peak P_{out} (dBm)**	**Pdc (W)**	**Area (mm^2)**	**Ref.**
222-250	90-nm SiGe	Balanced Mult.	1.8	0.09	0.54	This work
200-230	90-nm SiGe	Amp. + 4-Way Comb. Mult.	7.8	2.16	3.63	This work
229-251	130-nm SiGe	VCO + PA + $\times$2	-2	-	0.32	[82]
235-275	130-nm SiGe	$\times$16 $\times$16 + PA	-6[1] 2.5[1]	0.3 0.7	0.7 0.98	[83]
215-240 308-328 317-328	130-nm SiGe	PA + $\times$2 PA + $\times$2 $\times$18	-3 -1 -3	0.43 0.42 1.62	0.61 0.52 0.95	[84]
210	32-nm SOI	PA VCO + 2$\times$2 PA array	4.6 5.1[2]	0.04 0.24	- 3.5	[4]
163-180	45-nm SOI	2$\times$2 PA-Doubler array	5[2]	0.27	5.8	[91]
202	45-nm SOI	Stack Doubler	5.8	0.065	0.35	[85]
180	40-nm GaN	Single Stage PA	13.7	-	-	[48]
210-220	250-nm InP	Two-Way Comb. PA	20.4	-	1.38	[92]
290-307.5	250-nm InP	Two-Way Comb. PA	10	0.85	0.64	[93]

[1] 2.5 dB balun loss deembedded
[2] EIRP (effective isotropically radiated power)

network and transistor modeling inaccuracies.

This work shows the challenges of achieving high-efficiency designs above 200 GHz, but also, that arraying and power combining can still result in record output power even with frequency shifts and device variation.

4.6 Acknowledgements

The author would like to thank Michael Chang at the University of Michigan for process and technical discussions, and IBM (David Harame) for the 9HP wafer space.

Chapter 4 is mostly a reprint of the material as it is submitted for publishing in IEEE Transactions on Microwave Theory and Techniques, 2015. Hsin-Chang Lin and Gabriel M. Rebeiz. The dissertation author was the primary author of this material.

Chapter 5

High-Power Millimeter-Wave Frequency Multipliers in Advance SiGe and CMOS Process

5.1 A 135-160 GHz Balanced Frequency Doubler in 45 nm CMOS with 3.5 dBm Peak Power

5.1.1 Introduction

There is a lot of recent interest in transceivers and active imaging arrays above 100 GHz [6, 94, 9, 95]. One of the key goal is the generation of adequate power, which is essential for Gbps communication systems (S/N ratio), or to illuminate an scene for active imaging. There are two techniques to generate power at these frequencies: Amplifiers, and multiplier chains. Recently, SiGe and CMOS amplifiers have shown $\sim$10-12 dBm capabilities at 130-160 GHz [70, 96], but at these power levels, they require a large drive signal ($>$ 0 dBm). Therefore, it is essential to develop multipliers with $>$ 0 dBm output

power so as to act either as independent wideband sources, or as drivers for amplifiers, mixers and modulators at D-band frequencies.

The active doubler is the most commonly used transistor multiplier to-date [97, 98, 35]. Due to its differential nature, it cancels the odd harmonic components (first and third), and generates efficient even harmonic levels (second and fourth). At D-band frequencies, the fourth harmonic level is very low ($\sim$20 dB conversion loss), and optimization is done for the second harmonic. This topology has been used in 45nm CMOS and resulted in 0 dBm of power at 180 GHz and with good operation at 170-190 GHz [35]. The goal of this work is to optimize the active doubler and to study the limit of this technology. The goal is also a $\sim$3 dB advance in the state-of-the-art, so that CMOS multipliers can generate 2-4 dBm of wideband power at 130-160 GHz.

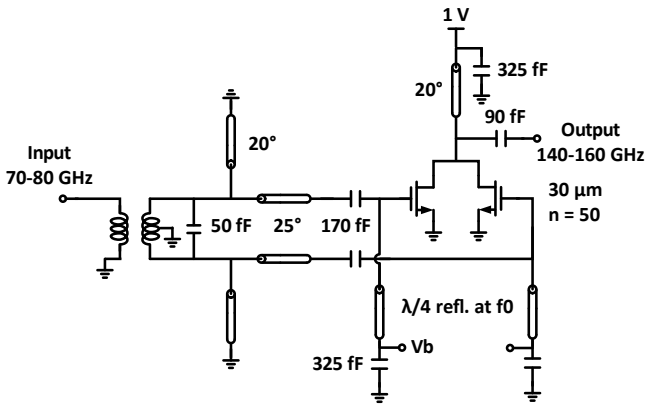
5.1.2 Design

Fig. 5.1(a) presents the active doubler consisting of a differential amplifier biased in a class B mode, a fundamental reflector at the gate, and input and output matching networks. A balun is used at the input to convert the singl-ended GSG signal into a differential signal. The technology is 45nm CMOS SOI with 11 metal layers, and the transistor is connected from the bottom layers (poly-silicon and M1 layer) to the top layer (LB) using a large set of via holes and metal interconnects (Fig. 5.1(b)). These are modeled using RC extraction up to the C1 layer and then using full electromagnetic simulator (Sonnet) from the C1 layer to the LB layer [55]. These additional parasitics are then included in the transistor model for simulations in Cadence.

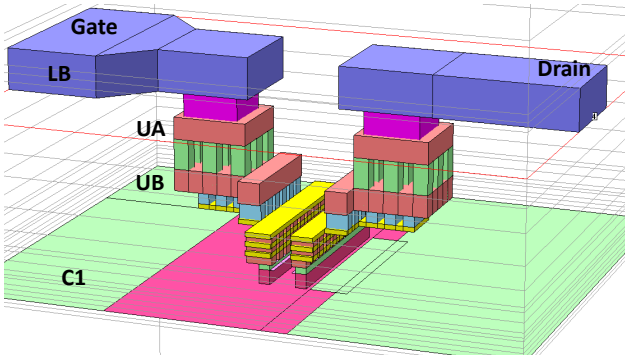
The two important design parameters for optimal performance are: a) transistor size and b) required number of fingers for this specific size. The use of a fundamental reflector at the input and the transistor biasing point were explained before and are not repeated here [35]. The doubler is first simulated vs. varying the transistor size and a

width of 30-40 μm results in an output power of 2.9-3.5 dBm for a finger width of 0.5-1 μm (Vdd=1 V, Vgate= 0.2 V) (Fig. 5.2). Another simulation vs. finger width shows that, for a 30 μm transistor, a 0.4-0.6 μm finger width results in an output power of 3.8-3.5 dBm. The reason for the decrease in the output power and conversion gain above 0.5 μm width is the higher gate resistance for the 1 μm fingers (5 Ω) vs. the 0.5 μm fingers (1.5 Ω), which is in series with the transistor input impedance. Therefore, a 60x0.5 μm transistor layout results in better performance than a 30x1μm layout (including all the connection parasitics to LB). However, stability analysis indicated that a 60x0.5 μm transistor is unstable under high bias condition (S_{11} and $S_{22} > 1$), and therefore, a 50x0.6 μm transistor is chosen since it provides the highest output power and unconditional stability.

The next step is to match the transistor differential input impedance of 35-j180 Ω at 75 GHz to the input 50 Ω port. This is done using a microstrip stub matching network and a balun. Microstrip lines are used since they have a lower loss than CPW lines at W-band (Fig. 5.3). The balun is first optimized for excellent balance using Sonnet (Δ(G) = 0.1 dB and $\Delta(\phi) = 3^{o}$ between output ports at 70-80 GHz), and then its S-parameters are used together with a symmetrical stub network for the input matching network. The 50 fF capacitor is done using C1 to B3 metal layers using the PDK models and its interconnections from B3 to LB are modeled in Sonnet. The output impedance is 5.5-j38 Ω at 140-160 GHz and this is matched to the output 50 Ω port using a single inductive stub and a 90 fF capacitor (again, in microstrip and simulated in Sonnet). The entire Sonnet circuit is shown in Fig. 5.4(a), and the loci of the gate, drain, input and output impedances are shown in Fig. 5.4(b).



(a)



(b)

Figure 5.1: (a) Active doubler schematic, and (b) transistor interconnections.

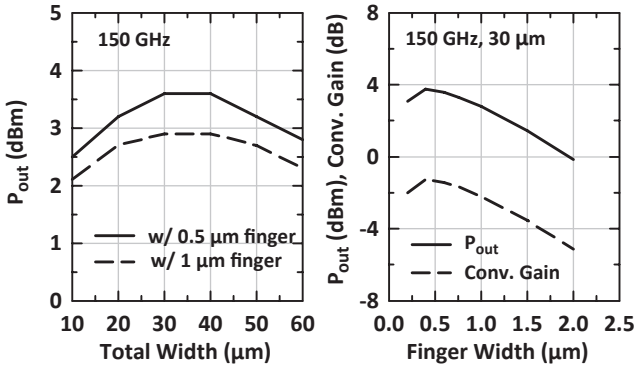


Figure 5.2: Pout vs. total width, and Pout vs. 30 μm transistor with different finger widths.

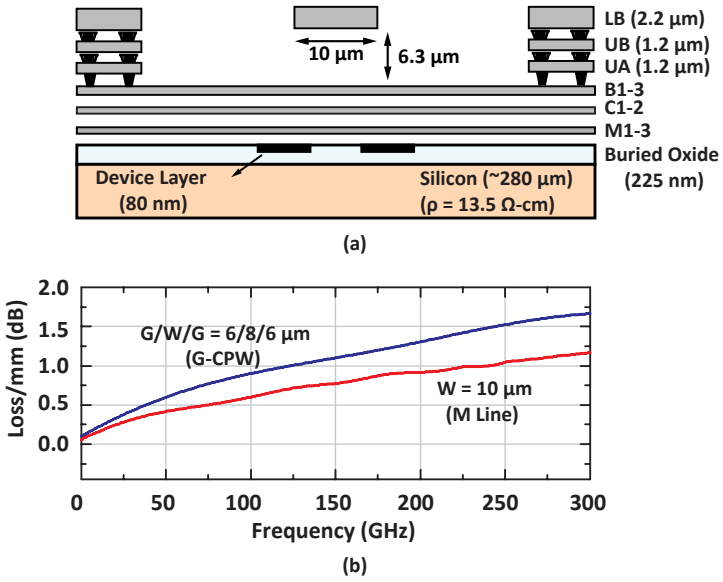
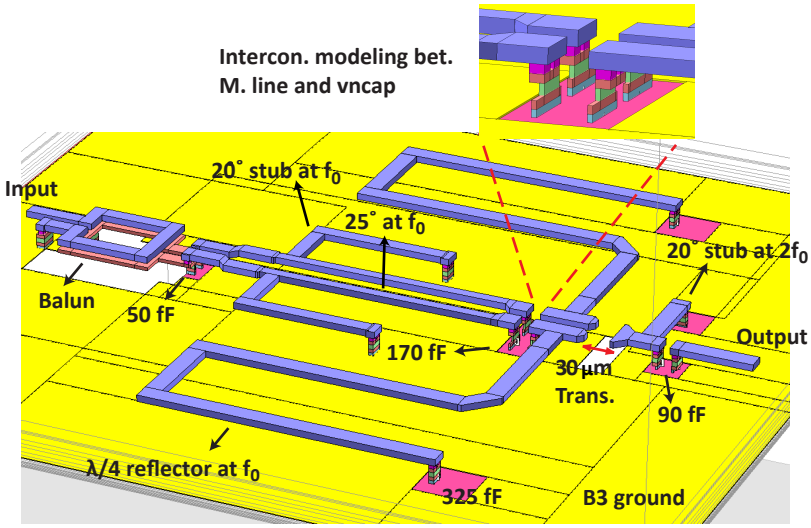


Figure 5.3: (a) Implementation of a 50 Ω microstrip line. (b) Simulated microstrip line loss and a 50 Ω G-CPW line loss.

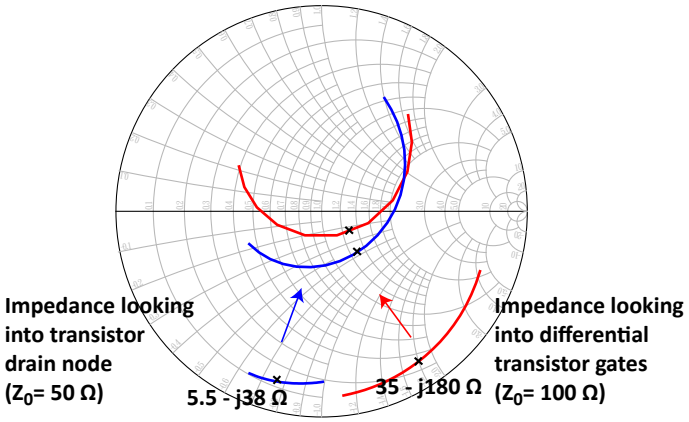
5.1.3 Measurement

Fig. 5.5 presents the D-band doubler with an active area of 0.76×0.58 by mm^2. The measurement set-up is shown in Fig. 5.6 and care was taken to calibrate the power to the GSG pads. This is done by first calibrating the loss the WR-10 and WR-6 waveguide set-ups to the probe inputs, and then measuring the WR-10 and WR-6 probe loss using a back-to-back configuration. Therefore, all power levels are referenced to the probe tips, and include the input and output GSG pad loss (0.15-0.3 dB at 75-150 GHz).

Fig. 5.7(a) presents the measured output power and conversion gain vs. input power at 150 GHz (Vgate = 0.2 V). An output power of +3.5 dBm is achieved with a conversion gain of -4.5 dB at 7 dBm input power, and at a bias current of 25 mA. The output power vs. frequency is $>$ 2 dBm from 140-160 GHz with a peak of +3.5 dBm at 147-150 GHz. The conversion gain is -5 to -7.5 dB at 140-160 GHz for peak output power. Measurements agree well with simulations knowing that such wideband measurements have an inherent error of 0.5-1 dB. The measured fundamental leakage is



(a)



(b)

Figure 5.4: (a) Sonnet em modeling, and (b) input and output impedances of the doubler. Impedances are plotted at 65-85 GHz (input, red) and 130-170 GHz (output, blue). Z_0= 50 Ω except for the differential impedance seen into the transistor gates.

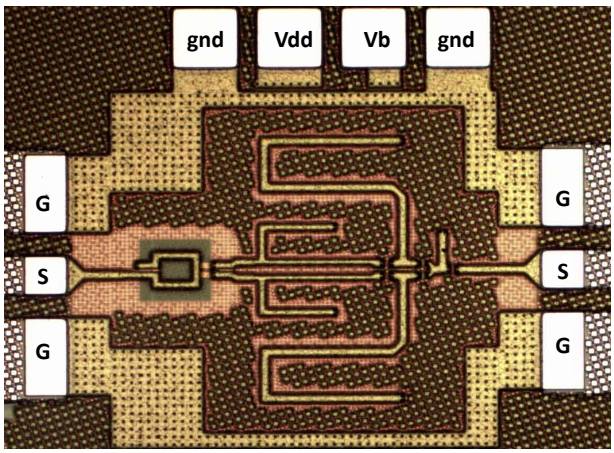


Figure 5.5: D-band doubler photograph (0.76 $\times$ 0.58 mm^2 including all pads).

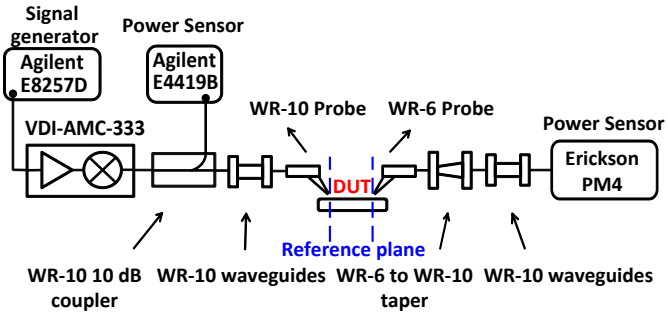
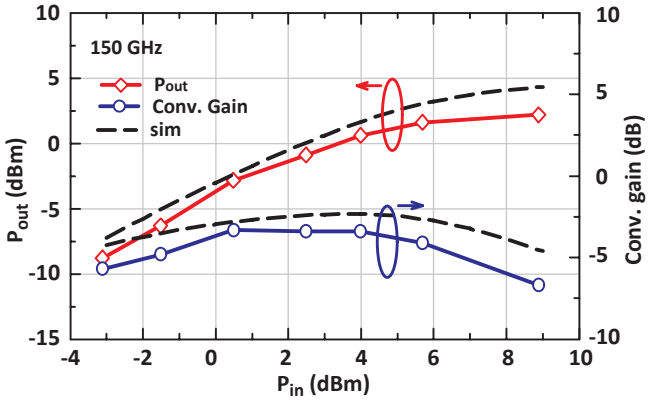
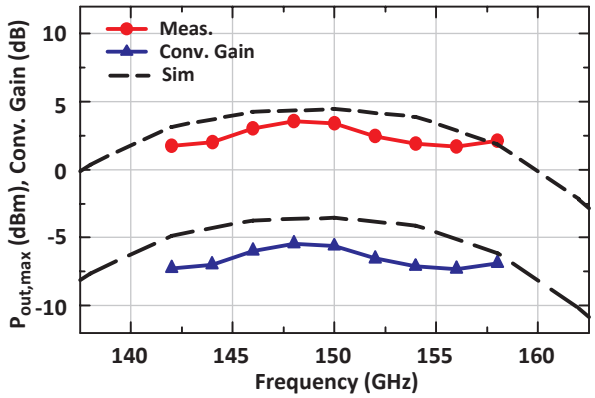


Figure 5.6: WR-10/WR-6 measurement setups for the D-band doubler.



(a)



(b)

Figure 5.7: (a) Measured output power and conversion gain vs. input power at 150 GHz and (b) vs. frequency.

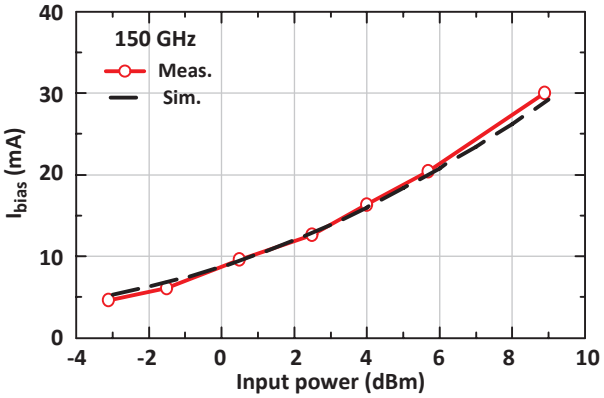


Figure 5.8: Measured bias current vs. input power at 150 GHz.

Table 5.1: Performance Summary for Doublers and Amplifiers

Frequency (GHz)	Technology	Source Type	Peak Pout (dBm)	Peak Gain (dB)	Pdc (mW)	Ref.
135-160	45-nm SOI CMOS	Balanced Doubler	3.5	-3	25	This work
144	350-nm SiGe	VCO + Doubler	3	N/A	410	[98]
170-190	45-nm SOI CMOS	Balanced Doubler	0	-6.4	39	[35]
200-245	90-nm SiGe	Balanced Doubler	2	-15	35	[68]
165	130-nm SiGe	Single-Ended Amplifier	0	15	135	[99]
160	130-nm SiGe	Differential Amplifier	10	32	N/A	[70]
150	65-nm CMOS	Differential Amplifier	12.2	16	115.2	[96]

$<$ -20 dBc. The measured current vs. input power also agrees very well with simulations (Fig. 5.8).

Table 5.1 compares different multipliers and amplifiers at D-band. This work results in a larger output power than most amplifiers (not shown in the table), and the best D-band multiplier to date.

5.1.4 Acknowledgements

Chapter 5.1 is mostly a reprint of the material as it appears in IEEE International Microwave Symposium Digest, 2014. Hsin-Chang Lin and Gabriel M. Rebeiz. The dissertation author was the primary author of this material.

5.2 A 200-245 GHz Balanced Frequency Doubler with Peak Output Power of 2 dBm

5.2.1 Introduction

THz imaging and communication systems based on advanced silicon SiGe and CMOS nodes are an active area of research, and have the potential to greatly lower the cost of such systems. For both imaging and communication applications, it is important to develop a wideband source with > 0 dBm of power so as to act as an illuminator (for active imaging) or as a local oscillator/RF source (for communications). These sources are either built using frequency multipliers or using injection-locked oscillators.

5.2.2 Technology

The 200-245 GHz balanced doubler is designed using IBM 90 nm BiCMOS process. It is a 90 nm SiGe HBT process built on top of a 90 nm CMOS process, with a 10-layer copper metal backend and high-density MIM capacitors (12.2 fF/ μm^2). The transistor model from the Cadence library results in a peak f_T/f_{max} of 300/310 GHz at 1.5-2.5 mA/μm bias current. However, with the effect of interconnection parasitic resistance and capacitance from M1 to LD modeled in Sonnet(Fig. 5.9(a)), the peak f_T/f_{max} drops to 290/250 GHz (Fig. 5.9(b)).

Fig. 5.10(a) shows the microstrip transmission line used in the doubler design for the reflectors and output matching network. The 50 Ω transmission line is implemented using top metal LD with 10 μm width and M2_4B and M1_4B tied together as two ground planes. The electromagnetic (EM) simulations using Sonnet shows an 0.8-1.2 dB/mm loss at 120-240 GHz, and a Q of 20.5-13.6 at 120-240 GHz. In practice, and from many different other measurements, the loss is higher than simulated and it is expected that a

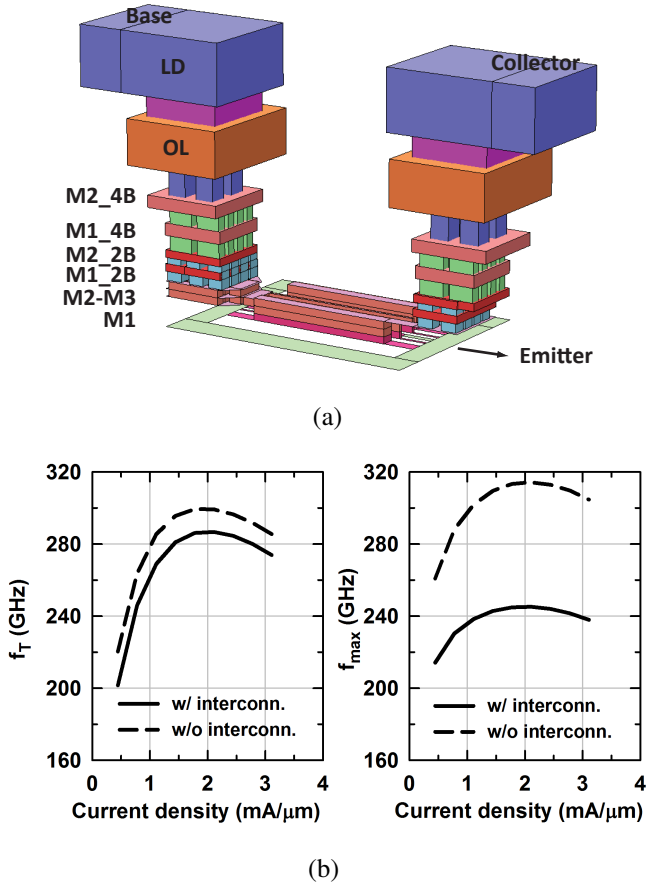


Figure 5.9: (a) The 90 nm SiGe BiCMOS transistor interconnections from M1 to LD modeled in Sonnet, and (b) simulated f_T/f_{max} w/ and w/o transistor interconnections.

loss of 1.2-1.8 dB/mm is achieved at 120-240 GHz with an associated Q of 13.6-9.1.

5.2.3 Design

Fig. 5.11 presents the schematic of the active balanced doubler. The single-ended input is converted to a differential signal using a passive balun and fed into the balanced transistor pair. The drain nodes are connected together to combine all the even harmonics from transistor, and create a broadband short circuit for the fundamental and odd harmonics. Two $\lambda_g/4$ short stubs at f_0 are used at the input base nodes to improve the conversion gain and output power of the doubler[35]. The 320 fF capacitors at the

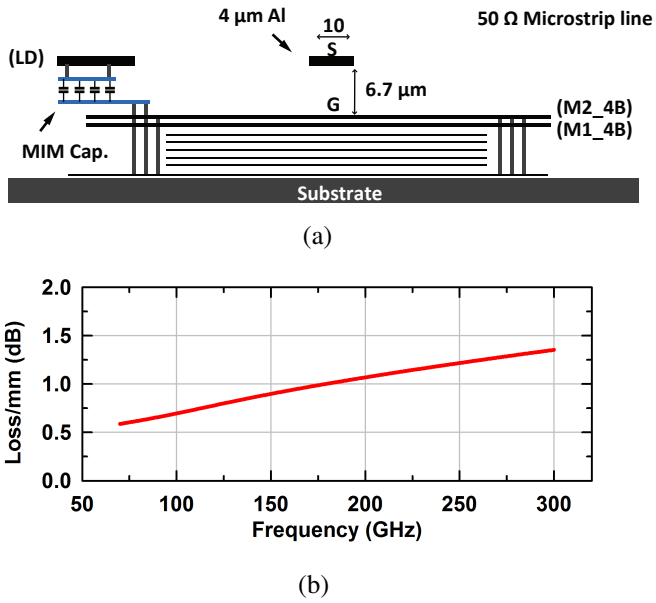


Figure 5.10: (a) 50 Ω microstrip transmission line used in the doubler design, and (b) the simulated line loss of 1 mm length line.

end of the reflector operate close to self-resonance, and provide a very low impedance (1 Ω) for the second harmonic at 240 GHz. Simulations show a 1.5 dB increase in the output power and conversion gain when these reflectors are used.

The 9x0.09 μm^2 transistor cells are standard IBM kit design with a single emitter finger, and dual collector, and base fingers (C-B-E-B-C), and are surrounded by a deep-trench isolation ring. The transistor size is optimized for maximum conversion gain for an input power of 10-15 dBm as shown in Fig. 5.12 using the library Cadence models. This input power is selected because it can be easily achieved from a wideband W-band amplifier in a SiGe process[57], [100]. Note that this optimization is done without taking into account the input and output losses. A transistor size of 6-9 μm results in optimal conversion gain and output power, and a 9 μm size is chosen for the final design. The transistor bias condition should be set to result in a conduction angle of 125° to maximize the second harmonic at the output [90]. Therefore, the transistor base is biased at V_b = 0.6 V (below threshold) for optimum doubler operation.

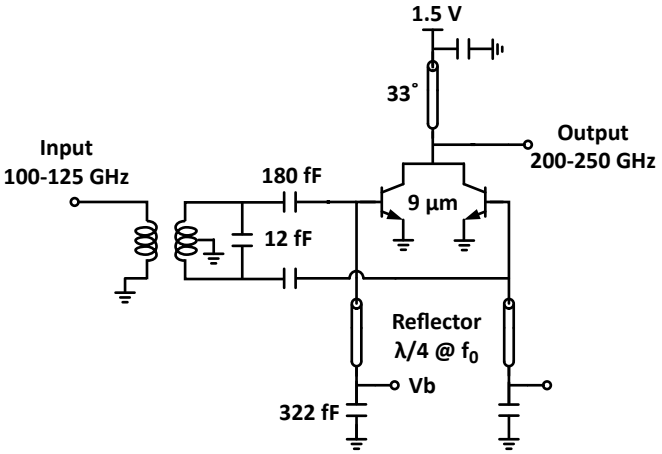


Figure 5.11: the schematic of 200-250 GHz balanced doubler.

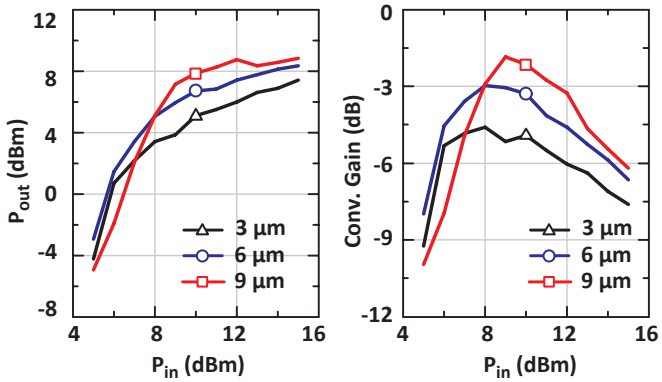


Figure 5.12: Simulated output second harmonic power vs. input power w/o the effect of transistor interconnection parasitics and matching network losses.

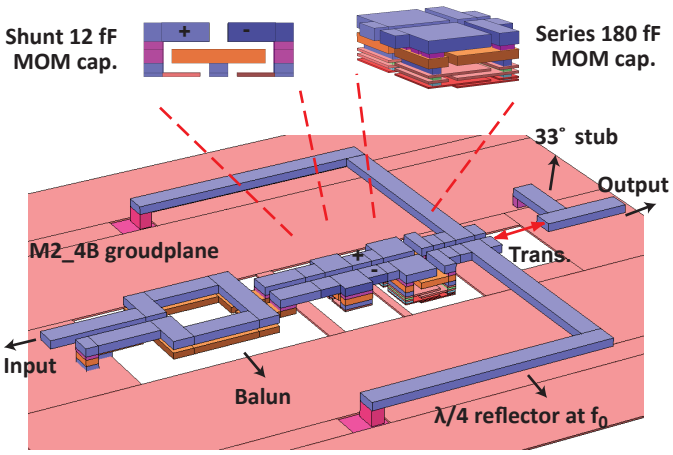


Figure 5.13: Electromagnetic modeling for the input matching network in Sonnet.

Fig. 5.13 presents the EM model for the doubler input matching network. The 100-140 GHz balun, 12 fF shunt metal-oxide-metal (MOM) capacitor, 180 fF series MOM capacitor, and the second harmonic reflectors are all modeled using Sonnet. The 12 fF shunt MOM capacitor is designed with metal layers LD to M2_4B, and the 180 fF series MOM capacitor is design with metal layers LD to M1_2B. The second harmonic reflectors are built using 50 Ω microstrip line and meandered to reduce the chip area. The output matching network is implemented using a short 50 Ω stub and is DC-coupled to the supply voltage. Care is taken to achieve a symmetrical layout and balanced operation.

The simulated loss of the balun using Sonnet is ∼1.5 dB at 100-145 GHz, and the simulated loss of the GSG pad is 0.3 dB at 100-140 GHz and 0.5 dB at 200-250 GHz. Again, measurements on different circuits indicate that these simulated values are optimistic, and typical achieved values are 0.5-0.7 dB at 100-200 GHz.

5.2.4 Measurements

The chip microphotograph is shown in Fig. 5.14, and the DC bias for the base and the collector nodes is supplied using the top pads. The input and output GSG pad are

designed to be compatible with both 100- and 75-μm-pitch GSG probes. The total size is 0.56×0.44 mm^2 including RF and DC pads.

The input return loss is measured using an OML 110-170 GHz extender and a 75-μm-pitch GSG WR-6 waveguide probes (Fig. 5.15). The measured input return loss is $>$ 10 dB at 145 to $>$ 170 GHz and is $>$ 7.5 dB from 110 to $>$ 170 GHz. The output return loss is not measured since the network analyzer extends to 220 GHz.

Fig. 5.16 presents the measurement setup for the output power and conversion gain. All measurements are referenced to the GSG input and output pads. The input power at 100-125 GHz is generated by VDI multiplier chain, and is monitored using a 10-dB coupler and an Agilent power meter. The output is directly connected to an Erickson power meter (PM4) using a WR-5 waveguide probe, a WR-5 to WR-10 taper, and WR-10 sections. The loss of the WR-10 and WR-5 GSG probes were measured using a through line on CS-15 calibration substrate. The measured loss of the WR-10 probe is 1.7-2.2 dB at 100-120 GHz whereas the measured loss of the WR-5 probe is 2.6-3.3 dB at 200-240 GHz. The measured loss of WR-5 to WR-10 taper and WR-10 section is 0.5 dB. Both the probe and waveguide losses are de-embedded from measurements and results are referenced the GSG pads.

A first measurement is done to determine the output fundamental level compared to the second harmonic. A fundamental rejection of 15-25 dB is achieved at an input of 110-140 GHz. The measured output power at 228 GHz versus input power is shown in Fig. 5.17(a). The measured peak output power is $\sim$2 dBm at an input power level of 16-17 dBm with a conversion gain of -15 dB. The self biasing current shown in Fig. 5.17(b) is 12.5-23 mA at an input power level of 11-17 dBm and a base bias voltage of $\sim$0 V. The simulated conversion gain is -10.5 dB at an input power level of 10-12 dBm and is much lower than Fig. 5.12 due to the loss of balun, MOM capacitors, transistor interconnection parasitics, output matching network, and GSG pad. Also, the base bias was decreased

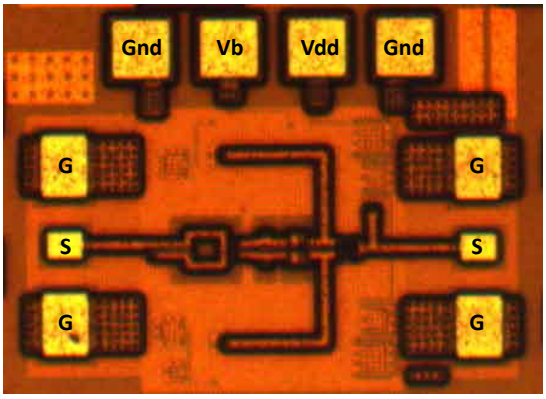


Figure 5.14: The chip microphotograph of 200-250 GHz balanced doubler (0.56 × 0.44 mm^2 including pads) .

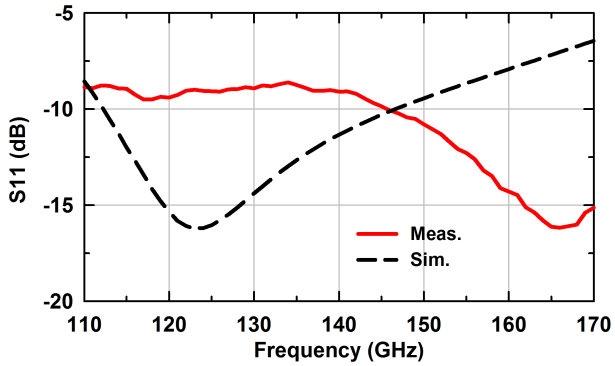


Figure 5.15: Measured and simulated input return loss at 110-170 GHz.

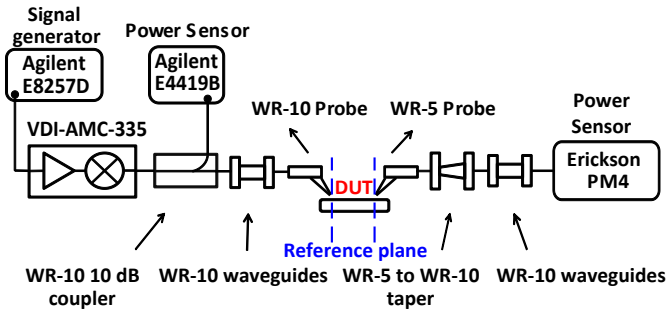


Figure 5.16: Setup for balanced doubler output power and conversion gain measurements.

to $\sim$0 V since the input power increased from 10-12 dBm (Fig. 5.12) to 12-17 dBm (Fig. 5.17(a)).

The measured peak output power shown in Fig. 5.18 is $>$ -2 dBm from 200-245 GHz with a peak value of +2 dBm at 228 GHz. The measured output power is 1-2.5 dB lower than simulation, which is acceptable at these frequencies.

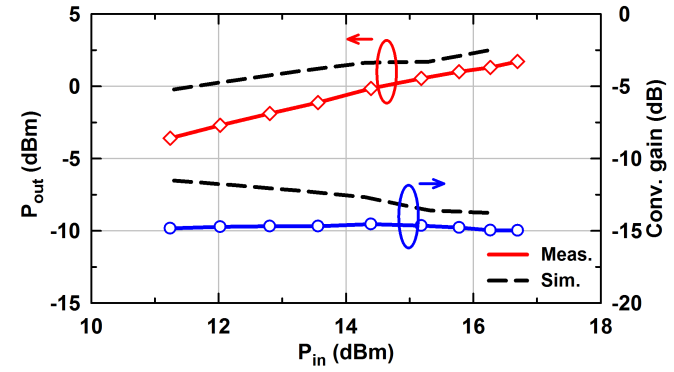
Table 5.2 presents a comparison with recently published SiGe and CMOS multipliers. SiGe HBTs result in higher power than CMOS designs due to higher f_T (referenced to the top metal) and breakdown voltages. It is seen that the 200-245 90 nm SiGe doubler has the widest bandwidth among other SiGe results and the output power level is comparable to the best achieved result. However, it is important to note that this is achieved at an input power level of 15-17 dBm, which may not be possible in implementations which include an integrated buffer.

5.2.5 Conclusions

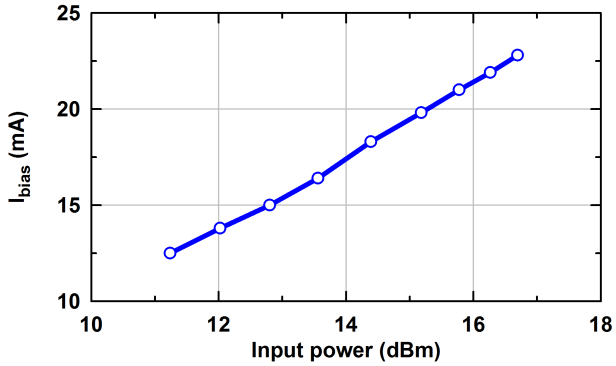
This paper presented a state-of-the-art doubler in 90 nm SiGe technology. The doubler results in wideband performance at 200-245 GHz with a peak output power of +2 dBm. Measurements agree well with simulations.

5.2.6 Acknowledgements

Chapter 5.2 is mostly a reprint of the material as it appears in IEEE Compound Semiconductor Integrated Circuit Symposium, 2013. Hsin-Chang Lin and Gabriel M. Rebeiz. The dissertation author was the primary author of this material.



(a)



(b)

Figure 5.17: (a) Measured output power and conversion vs. input power at 228 GHz, and (b) measured bias current vs. input power.

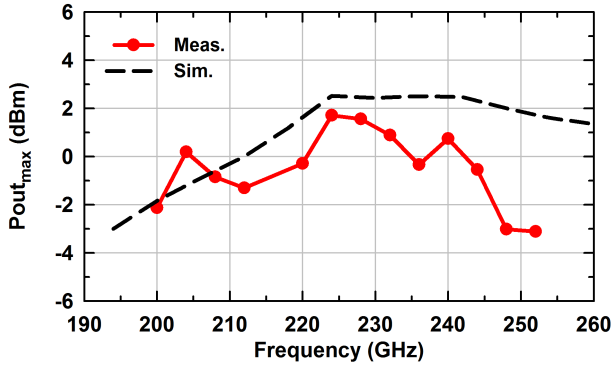


Figure 5.18: Measured maximum output power vs. frequency.

Table 5.2: Performance Summary

Frequency (GHz)	**Technology**	**Source Type**	**Peak Pout (dBm)**	**Peak Conv. Gain (dB)**	**Pdc (mW)**	**Ref.**
200-245	90-nm SiGe	Balanced Doubler	2	-15	35	This work
215-240	130-nm SiGe	Buff. + Balanced Doubler	-1	14	630	[84]
229-251	130-nm SiGe	VCO + Buff.+ Balanced Doubler	2	N/A	290	[82]
288-311	120-nm SiGe	VCO + Buff. + Balanced Doubler	-1.7	N/A	167	[101]
317-328	130-nm SiGe	Buff. + Balanced Doubler	-3	6	420	[84]
170-190	45-nm SOI CMOS	Balanced Doubler	0	-6.4	39	[35]
235-250	65-nm Bulk CMOS	Traveling-Wave Doubler	-6.6	-11.4	40	[102]

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