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Los Angeles

**Signal Processing Techniques Enabling Wideband A/D
Converters**

A dissertation submitted in partial satisfaction
of the requirements for the degree
Doctor of Philosophy in Electrical Engineering

by

Abhishek Ghosh

2013

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ABSTRACT OF THE DISSERTATION

Signal Processing Techniques Enabling Wideband A/D Converters

by

Abhishek Ghosh

Doctor of Philosophy in Electrical Engineering

University of California, Los Angeles, 2013

Professor Sudhakar Pamarti, Chair

With an ever-widening signal spectrum and incorporation of multiple standards that share the available spectrum at the same time, research towards building wideband analog-to-digital converters (ADCs) has gained significant momentum. Furthermore, with an aim to improve spectral efficiency, increasingly complex modulation schemes are being invoked having high peak-to-average ratios, the latter translating to high dynamic ranges for the received signals. Consequently, the ADCs deployed in these receivers need to be of quite high precision as well. With these two primary goals for ADCs (high bandwidth, high resolution) in mind, this thesis presents a few different techniques for achieving them.

In the first part of this thesis, we shall explore the art of dithering to linearize an A/D converter system. In particular, a digital-signal conditioning technique (using subtractive dither) is developed as a stepping-stone for a high resolution system. The effects of filtering the dither signal to shape its spectral content outside the signal band while maintaining its benefits are studied in detail. Design

strategies for finite impulse response (FIR) filters that accomplish spectral shaping as well as allay quantizer non-linearity are derived theoretically.

In the second part of this thesis, the proposed dithering technique is used for linearizing an ADC system that is intrinsically non-linear, namely a VCO-based ADC. Ring voltage-controlled oscillator (VCO)-based ADCs have surfaced as elegant alternatives to the traditional $\Delta - \Sigma$ modulators primarily due to their mostly digital nature. They offer low power, low area and simplicity of design benefits. However, they are known to be notoriously non-linear that can be attributed to the non-linear nature of the frequency-voltage tuning curve of the VCO. In the proposed scheme, the ring VCO-based ADC is preceded by a coarse flash ADC. The former processes the quantization error (residue), a signal with much smaller dynamic range, from the coarse ADC thereby lessening the impact of the non-linearity. The proposed dithering technique further helps in alleviating the non-linearity. It helps condition the signal to the VCO input to appear as white noise thereby eliminating spurious signal content arising out of the VCO nonlinearity. The technique, thus obviates the need for power-hungry digital calibration techniques or expensive front-end loop-filters. A prototype implementation (in 65nm CMOS) based on the technique achieves 10-b ENOB in digitizing signals with 50MHz bandwidth consuming 8.2mW at an FoM of 90fJ/conv.step.

In the third part of this thesis, a very popular technique of bandwidth enhancement through time-interleaving multiple A/D converters is examined. Time-interleaved A/D converters enable high conversion bandwidths with quite high precisions. However, inevitable mismatch errors typical of any integrated circuit fabrication process degrades the achievable dynamic range of such A/D converters. Multiple techniques have been proposed over the past two decades to alleviate the problems of mismatch errors. This chapter takes a detailed look at most of these techniques

bringing out their strengths and weaknesses. The chapter provides a hitherto unavailable common platform to look at analog and digital intensive techniques towards solving this issue motivating the development of a novel solution to this problem in the subsequent section.

In the fourth chapter, a power-efficient technique to combat mismatches for time-interleaved systems is proposed. The proposed technique adaptively selects finite impulse response filters that take advantage of the signal characteristics. The sub-band outputs from the ADC are passed through these filters to correct for errors at a minimal hardware expense. Simulation results substantiating the claims and thorough analyses of the technique are subsequently presented to highlight the efficacy of the technique.

Chapter 1 of this thesis has been published in full in the *International Conference on Acoustics, Speech and Signal Processing(ICASSP)*, 2013. The dissertation author is the primary investigator and author of this paper. Professor Sudhakar Pamarti supervised the research which forms the basis for this paper.

Chapter 2 of this thesis is a reprint of a paper under preparation to be submitted in part or in full to the *IEEE Journal of Solid-States Circuits (JSSC)*. The dissertation author is the primary investigator and Professor Sudhakar Pamarti supervised the research which forms the basis for this paper. By the virtue of being (or to be) independent papers, there is a slight degree of overlap in content between Chapters 1 and 2, but this is essential to maintain the continuity of the chapters.

Chapter 3 of this thesis is a reprint of a paper under preparation to be submitted in part or in full to the *IEEE Transactions of Circuits and Systems-I (TCAS-I)*. The dissertation author is the primary investigator and Professor Sudhakar Pamarti supervised the research which forms the

basis for this paper.

Chapter 4 of this thesis is also a reprint of a paper under preparation to be submitted in part or in full to the *IEEE Transactions of Circuits and Systems-1 (TCAS-1)*. The dissertation author is the primary investigator and Professor Sudhakar Pamarti supervised the research which forms the basis for this paper.

The dissertation of Abhishek Ghosh is approved.

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2013

To Ma and Baba

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PUBLICATIONS

- Abhishek Ghosh and Sudhakar Pamarti, "On the properties of filters for subtractive discrete dither in quantizers", in preparation for publication in *IEEE Trans. on Signal Processing*.
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- Abhishek Ghosh and Sudhakar Pamarti, "Linearization through dithering: A 50MHz bandwidth, 10-b ENOB, 8.2mW VCO-based ADC", in preparation for publication in *IEEE Journal of Solid-States Circuits*

- Abhishek Ghosh and Sudhakar Pamarti, "Phase Mismatches in Time-Interleaved ADCs: Adaptive signal-dependent digital solution to an analog problem", in preparation for publication in *IEEE Trans. on Circuits and Systems-I*.
- Abhishek Ghosh, Sudhakar Pamarti, "Enabling high-speed, high-resolution ADCs using adaptive signal conditioning techniques", *IEEE Mid-West Symposium on Circuits and Systems(MWSCAS)*, 2013
- Abhishek Ghosh, Sudhakar Pamarti, "A 50MHz bandwidth, 10-b ENOB, 8.2mW VCO-based ADC enabled by filtered-dithering based linearization", *IEEE Custom Integrated Circuits Conference(CICC)*, 2013
- Abhishek Ghosh, Sudhakar Pamarti, "Filtering of subtractive discrete dither in quantizers: some new results", *International Conference on Acoustics, Speech and Signal Processing(ICASSP)*, 2013
- Abhishek Ghosh, Sudhakar Pamarti, "Mitigating timing errors in time-interleaved ADCs: a signal conditioning approach", *IEEE International Symposium on Circuits and Systems(ISCAS)*, 2013
- Abhishek Ghosh, Sudhakar Pamarti, "Adaptive signal conditioning algorithms to enable wideband signal digitization", *IEEE International Conference on Communications(ICC)*, 2013
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CHAPTER 1

Filtering of subtractive discrete dither in quantizers: some new results

1.1 Introduction

Quantizers are the portals to digital signal processing of all real-world signals and hence serve as the main interface between natural and machine-based signal processing. An example mid-tread quantizer is shown in Figure 1.1. As can be seen, the input-output characteristic of any example quantizer, is non-linear and hence signals when *quantized* result in errors which have significant dependence on the input signal and hence are spectrally non-white [1–3, 5]. A major understanding from these works is that the input signal to the quantizer needs to be equipped with certain statistical properties in order to ensure that the quantization error is white and its power is the ubiquitous $\Delta^2/12$ (Δ being the quantization step size). In most practical scenarios though, it is highly infeasible to handle signals with the required statistical properties. So, a small signal, random in nature (called *dither*) is added to the input in order to make the composite signal samples *unpredictable* at any given time.

1.1.1 Dithered quantization

Let us define a dithered quantizer more formally. A behavioral schematic is presented in Figure 1.2. A random signal $r[n]$ is added to the signal to be quantized $x[n]$ and the composite signal $z[n] = x[n] + r[n]$ is passed through the quantizer. A dithered quantizer can be implemented in a few different flavors, each unique in the properties it imparts to the quantization error, Figures 1.2(a)-(c).

In Figure 1.2(a), the added dither signal $r[n]$ is subtracted digitally from the quantized value $y[n]$ and hence is called a *subtractively dithered quantizer*. Likewise, Figure 1.2(b) refers to a non-subtractively dithered quantizer (commonly phrased as additive dithered quantizer). The added dither, $r[n]$ is usually constrained to be bounded between one least significant bit (LSB) of the quantizer. Separate conditions [3] have been theoretically derived for either case to ensure that the error-samples ($e[n] = y[n] - z[n]$ for Figure 1.2(a) and $e[n] = y[n] - x[n]$ for Figure 1.2(b)) are independent (among themselves as well as of the input) and uniformly distributed both in terms of first and second order statistics. Henceforth, such error would be called *well-behaved* in this paper. It is found that a well-behaved quantization error can be guaranteed, for a subtractive dithered quantizer, if the dither statistics satisfies certain properties. The simplest class of dither conforming to these statistics is a uniformly distributed dither. However, for an additive dither situation, such conditions are not easily derivable [3].

Unfortunately, a uniformly distributed white dither signal, $r[n]$ would contribute too much noise to the quantizer output. In fact, a uniformly distributed dither signal spanning one quantizer LSB would degrade the overall signal-to-noise ratio (SNR) by 3dB. Furthermore, it may be im-

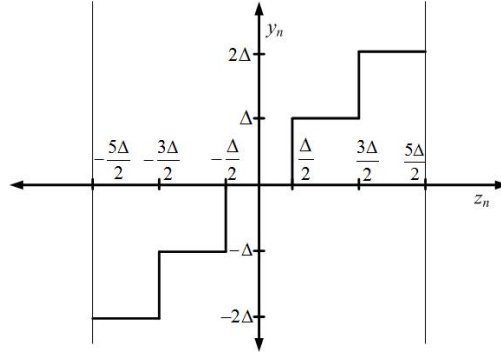


Figure 1.1: Mid-tread quantizer

possible or at least extremely challenging to digitally generate such analog dither [6]. The second problem is solved using hardware-friendly digital dither (that spans only a finite set of values), while the first problem is solved by spectrally shaping such dither out of the band of interest using digital filters [4]. Such an architecture is presented in Figure 1.2(c) as an extension of Figure 1.2(a), where $d[n]$ is a Bernoulli signal with equal probability of a 0 or 1. However, filtering a signal tantamounts to modifying its statistical properties. Consequently, the error signal $e[n]$ in Figure 1.2(c) may not be well-behaved as noted above even if $d[n]$ is sample-wise independent, identically distributed (i.i.d.) and white.

1.1.2 Prior-art

There have been some very interesting works treating filtered dither signals and their efficacies in whitening the quantization error [4, 7, 8]. With reference to Figure 1.2(c), in [4], a detailed analysis is done on the properties of $r[n]$ where $d[n]$'s are i.i.d. random variables. However, the analysis is specific to additive dithered quantizers and imposes very strict conditions on the filter-coefficients (finite (FIR) or infinite (IIR) impulse response). In [8], a simplified condition is derived for FIR filters. However, the quantizer treated in [8], works on integer valued inputs only while the work

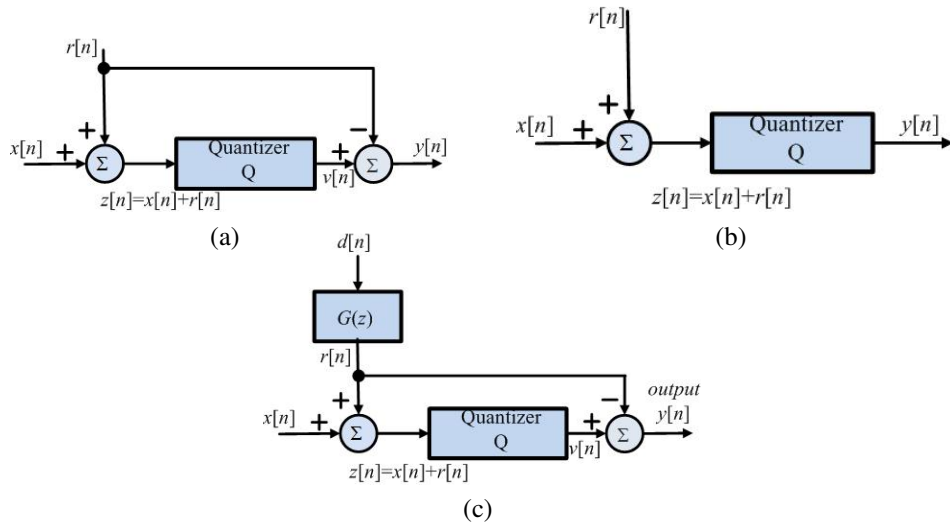


Figure 1.2: Dithered Quantizers: (a) Subtractive (b) Non-subtractive/Additive (c) Filtered-subtractive

in [7] provides conditions for the impulse response of an IIR filter (integrator in feed-forward path of a sigma-delta modulator).

1.1.3 Contribution

The main contribution of this work is the formulation of conditions for integer-valued FIR filters operating on continuous-valued inputs for a subtractively dithered quantizer. We theoretically derive conditions for the error-sequence, subject to such filtering, to be well-behaved. In the next section, we detail the behavioral model to be used in all subsequent derivations. Section 1.3 furnishes the main theoretical results accompanied by some relevant proofs while Section 1.4 provides an insight into the simulation results to validate the theory. We conclude the paper in Section 1.5.

1.2 Behavioral model

The model is as presented in Figure 1.2(c). Let us define an i.i.d. Bernoulli sequence $d[n]$ that follows the statistics: $\mathbb{P}r(d[n] = 0) = \mathbb{P}r(d[n] = 1) = 0.5$. The sequence $d[n]$ is passed through a

digital filter $G(z)$ having a finite impulse response $g[n] \in \mathbb{Z}$ of length K to produce an output $r[n]$. The filter gain is so adjusted that the output $r[n]$ spans Δ , LSB of the quantizer. Consequently, the filtered output $r[n]$ can be expressed as

$$r[n] = \frac{\Delta}{L} (g[0]d[n] + g[1]d[n-1] + \dots + g[K-1]d[n-K+1]) \quad (1.1)$$

where $L = \sum_{i=0}^{K-1} |g[i]|$. The quantity Δ/L can be thought of as the dither LSB (the minimum resolution of the added signal r_n). The input signal $x[n]$ is assumed to be of arbitrary distribution and bounded in $[-(Q-1)\Delta/2, (Q-1)\Delta/2]$ for a Q -level quantizer ($Q \in \mathbb{N} \cap (1, \infty)$). The signal $r[n]$ is added with the input $x[n]$ to result in the composite signal $z[n] = x[n] + r[n]$. $z[n]$ is quantized to generate $v[n]$. The added dither signal $r[n]$ is subtracted from $v[n]$ to result in the actual output $y[n]$. The resultant quantization error is defined as $e[n] = y[n] - x[n] = v[n] - x[n] - r[n]$.

Note-1: Since the dither resolution is finite, namely Δ/L , hence any input of the form $x[n] = [x[n]] + \langle x[n] \rangle$ where $[x[n]] = k\Delta, k \in \mathbb{Z}$ and $\langle x[n] \rangle < \Delta/L$ will not *see* the effect of the added dither, and hence the quantization error will not be guaranteed to be well-behaved. In the remainder of the paper, we shall assume that the input signal $x[n]$ excludes the above special class of signals.

Note-2: In the following arguments, w_j and $w[j]$ would refer to the same quantity and will be used interchangeably.

1.3 Main result: theory

Theorem 1. *For a dithered quantizer, modeled in Section 1.2,*

P.1) The error sequence e_n is an identically distributed uniform random variable independent of the input $x_{n-m}, \forall k_1 \in \mathbb{Z}, \forall m \in \mathbb{Z}$ if and only if ($\langle \rangle_T$ operator denotes modulo- T operation)

C.1) A non-negative integer $i < K$ exists such that $\langle g_i k_1 \rangle_L = L/2$

P.2) The error sequence pair $(e_n, e_{n-p}) \forall p \in \mathbb{Z} \cap (0, K)$ is pairwise independent, each being an identical uniform distribution $\forall (k_1, k_2) \neq (0, 0)$ if and only if either of the following are true

C.2) A non-negative integer $l < p$ exists such that $\langle g_l k_1 \rangle_L = L/2$

C.3) A non-negative integer $1 \leq r \leq p$ exists such that $\langle g_{K-r} k_2 \rangle_L = L/2$

C.4) A non-negative integer $p \leq m < K$ exists such that $\langle g_m k_1 + g_{m-p} k_2 \rangle_L = L/2$

P.3) The error sequence pair $(e_n, e_{n-p}) \forall p \in \mathbb{Z} \cap [K, \infty)$ is pairwise independent, each being an identical uniform distribution $\forall (k_1, k_2) \neq (0, 0)$ if both the following conditions hold

C.5) The FIR filter coefficients $g[k]$ are of the form 2^i where i takes on each value in $[0, s - 1]$ at least once and

C.6) $L = \sum_{i=0}^{K-1} |g[i]| = 2^s$ where $s \in \mathbb{Z} \cap (1, K]$

Remark: For notational convenience, all properties are denoted as P.'s while all conditions are denoted as C.'s. Both P.1 and P.2 are *if and only if* conditions while P.3 is only a sufficiency condition. The strategy of the proof would be to proceed with P.2 first. The proof of P.1 would follow next while P.3 would be proved as a consequence of P.2 and would form the main result of this work, providing easy-to-use closed form solutions for the shaping filter $G(z)$. Let us proceed

with P.2 now.

Proof. The proof would use characteristic functions [9] to derive conditions on the specific properties of the added dither signal. This is a commonly used technique for such applications [8]. In fact, from [3], we know, that the joint characteristic function (jcf) for error-samples (e_n, e_{n-p}) can be written as, $\forall p \in \mathbb{Z} \cap (0, K)$ for $(k_1, k_2) \in \mathbb{Z}^2$

$$\begin{aligned}
\Phi_{e_n, e_{n-p}}(u_1, u_2) &= \sum_{k_1=-\infty}^{\infty} \sum_{k_2=-\infty}^{\infty} \frac{\sin(\pi\Delta(u_1 - k_1/\Delta))}{(\pi\Delta(u_1 - k_1/\Delta))} \\
&\quad \frac{\sin(\pi\Delta(u_2 - k_2/\Delta))}{(\pi\Delta(u_2 - k_2/\Delta))} \\
&\quad \Phi_{x_n, x_{n-p}}\left(\frac{-2\pi k_1}{\Delta}, \frac{-2\pi k_2}{\Delta}\right) \\
&\quad \Phi_{r_n, r_{n-p}}\left(\frac{-2\pi k_1}{\Delta}, \frac{-2\pi k_2}{\Delta}\right)
\end{aligned} \tag{1.2}$$

Hence, for the joint density of (e_n, e_{n-p}) to be uniform and pairwise independent, it suffices to show [3],

$$\begin{aligned}
\Phi_{r_n, r_{n-p}}\left(\frac{-2\pi k_1}{\Delta}, \frac{-2\pi k_2}{\Delta}\right) &= 0 \\
\forall (k_1, k_2) &\in \mathbb{Z}^2 - (0, 0)
\end{aligned} \tag{1.3}$$

The jcf of the dither samples (r_n, r_{n-p}) is defined as

$$\begin{aligned}
\Phi_{r_n, r_{n-p}}(u_1, u_2) &= \mathbb{E}(e^{j(u_1 r_n + u_2 r_{n-p})}) \\
&= \mathbb{E}(e^{j \frac{\Delta}{L} (u_1 \sum_{m=0}^{K-1} g_m d_{n-m} + u_2 \sum_{l=0}^{K-1} g_l d_{n-p-l})}) \\
&= \prod_{l=0}^{p-1} \Phi_d\left(\frac{\Delta}{L} u_1 g_l\right) \\
&\quad \prod_{m=p}^{K-1} \Phi_d\left(\frac{\Delta}{L} (u_1 g_m + u_2 g_{m-p})\right) \\
&\quad \prod_{r=1}^p \Phi_d\left(\frac{\Delta}{L} u_2 g_{K-r}\right)
\end{aligned} \tag{1.4}$$

Now, for a Bernoulli dither d_n , with $\mathbb{P}r(d_n = 0) = \mathbb{P}r(d_n = 1) = 0.5$,

$$\Phi_d(v) = e^{(-jv/2)} \cos(v/2) \tag{1.5}$$

From Eqn. (1.3), we need to evaluate Eqn. (1.4) for $u_{1,2} = 2\pi k_{1,2}/\Delta$. Thus, from Eqns. (1.4) and (1.5), we can write $\forall (k_1, k_2) \in \mathbb{Z}^2 - (0, 0)$

$$\begin{aligned}
|\Phi_{r_n, r_{n-p}}\left(-\frac{2\pi k_1}{\Delta}, \frac{-2\pi k_2}{\Delta}\right)| &= \prod_{l=0}^{p-1} \left| \cos\left(\frac{\pi k_1 g_l}{L}\right) \right| \\
&\quad \prod_{m=p}^{K-1} \left| \cos\left(\frac{\pi (k_1 g_m + k_2 g_{m-p})}{L}\right) \right| \\
&\quad \prod_{r=1}^p \left| \cos\left(\frac{\pi k_2 g_{K-r}}{L}\right) \right|
\end{aligned} \tag{1.6}$$

This proves the *sufficiency* of the theorem, since if any one of the product series terms is zero (C.2-4), P.2 is satisfied.

Necessity: The necessity conditions can be likewise argued, and is omitted here for brevity.

Discussion: It may not be always possible to design FIR filter coefficients satisfying conditions C.2-4 of Theorem 1 since the filter coefficients are not available in a closed-form solution. Furthermore, it's not practically possible to evaluate the characteristic function in Eqn. (1.6). at all integer values of (k_1, k_2) to identify an appropriate filter structure. P.3 addresses this issue in further detail.

For the proof of P.1, we write the probability density function (pdf) of the error sequence e_n conditioned on the input $x_{n-m} \forall m \in \mathbb{Z}$ as

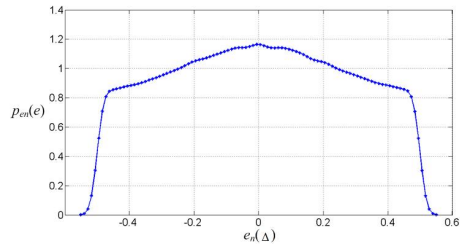
$$p_{e_n|x_{n-m}}(a|b) = \sum_{l=-\infty}^{\infty} p_{z_n|x_{n-m}}(-a + l\Delta|b) \quad (1.7)$$

Now, it is not difficult to see that

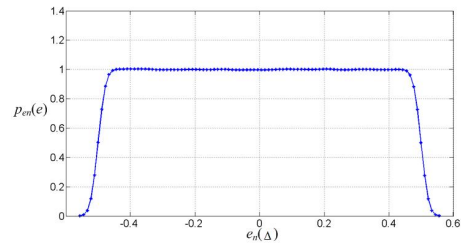
$$\begin{aligned} p_{z_n|x_{n-m}}(c|b) &= p_{x_n+r_n|x_{n-m}}(c|b) \\ &= p_{x_n|x_{n-m}}(c|b) * p_{r_n}(c) \end{aligned} \quad (1.8)$$

since r_n is independent of both x_n and x_{n-m} where a , b and c are in the appropriate domains and $*$ denotes convolution.

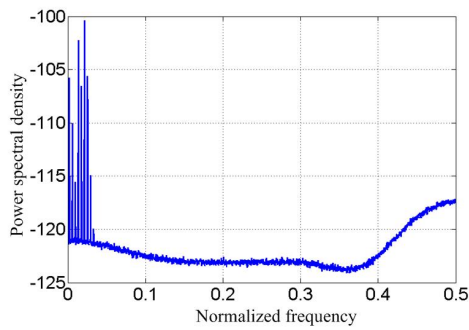
Thus, from Eqns. (1.7) and (1.8), the characteristic function (cf) of e_n conditioned on x_{n-m} ,



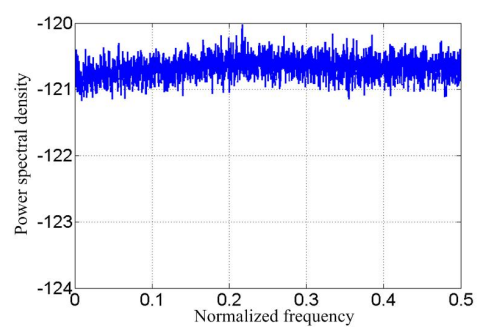
(a) error pdf for G_1



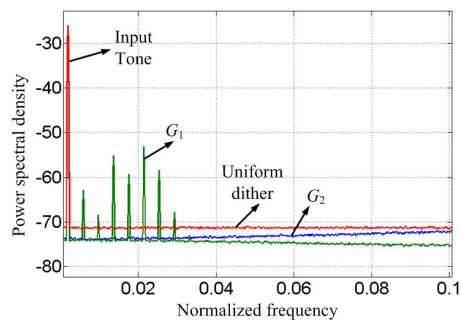
(b) error pdf for G_2



(c) error psd for G_1



(d) error psd for G_2



(e) Output spectrum for three different scenarios

Figure 1.3: Simulation results

can be written as

$$\begin{aligned}\Phi_{e_n|x_{n-m}}(u) &= \frac{1}{\Delta} \sum_{k=-\infty}^{\infty} \Phi_{x_n|x_{n-m}}(-u) \\ &\prod_{i=0}^{K-1} \Phi_{d_n}\left(-ug_i \frac{\Delta}{L}\right) \frac{\sin(\pi\Delta(u_1 - k_1/\Delta))}{(\pi\Delta(u_1 - k_1/\Delta))}\end{aligned}\quad (1.9)$$

For the error-sequence e_n to be independent of x_{n-m} and be uniformly identically distributed, $\Phi_{e_n|x_{n-m}}(-\frac{2\pi k_1}{\Delta})$ must evaluate to 0 for every $k_1 \neq 0$. For this to happen, for any arbitrary input, from the proof of P.2,

$$\begin{aligned}\prod_{i=0}^{K-1} \left| \Phi_{d_n}\left(\frac{-2\pi k_1 g_i \frac{\Delta}{L}}{\Delta}\right) \right| &= \prod_{i=0}^{K-1} \left| \Phi_{d_n}\left(\frac{-2\pi k_1 g_i}{L}\right) \right| \\ &= \prod_{i=0}^{K-1} \left| \cos\left(\frac{\pi k_1 g_i}{L}\right) \right| = 0\end{aligned}\quad (1.10)$$

Eqn. 1.10 holds if and only if C.1 holds (the argument of at least one cosine term is driven to an odd multiple of $\pi/2$) hence proving P.1

The proof of P.3 will lead from that of P.2 through an important observation. Since, $p \geq K$, hence it is not difficult to see that,

$$\begin{aligned}p_{r_n, r_{n-p}}(r_1, r_2) &= p_{r_n}(r_1)p_{r_{n-p}}(r_2) \\ \Phi_{r_n, r_{n-p}}(u_1, u_2) &= \Phi_{r_n}(u_1)\Phi_{r_{n-p}}(u_2)\end{aligned}\quad (1.11)$$

Now, from Eqn. (1.3), we need to prove that $\Phi_{r_n, r_{n-p}}\left(\frac{-2\pi k_1}{\Delta}, \frac{-2\pi k_2}{\Delta}\right)$ goes to zero for all values

of $(k_1, k_2) \in \mathbb{Z}^2 - (0, 0), \forall p \in \mathbb{Z} \cap [K, \infty)$. Based on Eqns. (1.4)-(1.6), this is equivalent to proving

$$\prod_{i=0}^{K-1} \left| \cos\left(\frac{\pi k_1 g_i}{L}\right) \right| \left| \cos\left(\frac{\pi k_2 g_{K-1-i}}{L}\right) \right| = 0 \quad (1.12)$$

for all values of $(k_1, k_2) \in \mathbb{Z}^2 - (0, 0), \forall p \in \mathbb{Z} \cap [K, \infty)$.

It is interesting to note that Eqn. (1.12) leads to an L -periodic sequence (in k_1 or k_2) if condition C.1 is satisfied. Consequently, it suffices to evaluate the cf of Eqn. (1.12) in a finite set of L^2 points. Now it becomes useful to consider the following cases, $\forall (k_1, k_2) \in [-L/2 + 1, L/2]$ assuming the conditions in Theorem 1 hold (sufficiency).

- $k_1 = \text{odd}, k_2 = \text{odd}$ One product term of the right-hand side of Eqn. (1.12) can be written as $\cos(\pi k_j \frac{2^r}{2^s})$, $j = 1, 2$. Hence for $r = s - 1$, we can write the product term as $\cos(\frac{\pi}{2} k_j)$ which goes to 0 since $k_{1,2}$ are odd.
- $k_1 = \text{odd}, k_2 = \text{even}$ Here, k_1 will drive the product term to 0 for $r = s - 1$. The symmetric case of $k_2 = \text{odd}, k_1 = \text{even}$ similarly can be shown to equate to 0.
- $k_1 = \text{even}, k_2 = \text{even}$ Here, let $k_{1,2} = 2^l(2m + 1), l \leq s - 1$ for any integer m . Then the product term containing $r = s - 1 - l$ would yield $\cos(\frac{\pi}{2}(2m + 1))$ which again goes to 0.

□

Discussion: C.5 and C.6 give easy formulae to design the dither-shaping filter. The proposed solution to Eqn. (1.12) may not be unique (under investigation), but the aforementioned conditions are in tune with powers-of-2 FIR filters [10], and hence amenable to facile design. It should further be noted that condition C.5 is a subset of C.1 and hence ensures an uniformly distributed

error sequence independent of the input. It is of interest to observe that though P.5 proves pair-wise independence only for error samples separated by more than K , for all practical purposes the error is white with a uniform distribution.

1.4 Main results: simulation

Let us consider two filters, $G_1(z)$ and $G_2(z)$ (z -transforms of 2 example filters $g_1[n]$ and $g_2[n]$ respectively) such that the former satisfies neither of C.5 and C.6 while the latter satisfies both.

$$\begin{aligned}
 G_1(z) &= 1 - 3z^{-1} + 5z^{-2} - 9z^{-3} + 3z^{-4} - 3z^{-5} \\
 &\quad + 9z^{-6} - 5z^{-7} + 3z^{-8} - z^{-9} \\
 G_2(z) &= -1 - 2z^{-1} - 4z^{-2} - 8z^{-3} + 16z^{-4} - z^{-5}
 \end{aligned}$$

The input $x[n]$ is chosen to be a continuous-valued sinusoid at a normalized frequency of 0.002 with an amplitude of 2Δ . The signal is quantized into $Q = 5$ levels as in Figure 1.1. In Figure 1.3(a),(b), we plot the pdf of the error sequence e_n for both the cases, while Figure 1.3(c)(d) shows the spectra of the error signal. As can be clearly seen, the proposed filter, namely G_2 , whitens the error-sequence and exhibits an almost uniform pdf (Figure 1.3(b)) while G_1 shows an almost triangular pdf (Figure 1.3(a)) for the error samples. The error power spectral density (psd) for G_2 (Figure 1.3(d)) is *white*, while the error psd for G_1 exhibits multiple spurious tones at harmonic frequencies (as is expected from a lookup table type non-linearity) (Figure 1.3(c)). In order to make a fair comparison, a third case where a uniform dither signal $r[n]$ (the case in Figure 1.2(b)) is added to the input signal before quantizing, is also considered. The spectra of $y[n] = x[n] + e[n]$ is plotted

for all the three cases: G_1 , G_2 and uniform dither in Figure 1.3(e). As can be seen, the uniform dithered quantizer contributes the maximal in-band power while whitening the output spectrum completely. G_2 shapes the in-band dither power, as well as gets rid of any spurious components, while G_1 has the least in-band dither power contribution but engenders harmful spurious tones at the quantizer output. This is expected since, from P.1 $e[n]$ being independent of $x[n]$ bequeaths the well-behaved properties of $e[n]$ on $y[n]$.

1.5 Conclusion

A filtered dithering technique in quantizers is proposed. Theoretical conditions on the filter structure are derived to ensure independence, whiteness and uniform distribution of the quantization error signal. Behavioral simulation results are presented to corroborate the proposed results and claims.

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CHAPTER 2

Linearization through dithering: A 50MHz bandwidth, 10-b ENOB, 8.2mW VCO-based ADC

2.1 Introduction

With both wireless communication and imaging applications pushing for higher data rates there is an ever-increasing demand for wideband, high resolution analog-to-digital converters (ADCs). Figure 2.1 projects the wireless and imaging industry requirement in perspective with other popular electronic industries. As can be seen from Figure 2.1, signals in the few tens of MHz range need to be digitized to about 10 – 12 bits accuracy for our target application [1]. Furthermore, such ADCs are often assembled in millions (imaging) or deployed in portable devices imposing strict power consumption limits on a single ADC for enhanced battery-life leading to ease of portability. Several prominent candidates viz. successive approximation register (SAR), oversampling converters lay claim to this application with excellent results [2–4].

SAR ADCs have enjoyed a renewed interest owing to the immense power benefits they offer, particularly in finer technology nodes [2]. However, SAR ADCs are often found to have limited dynamic ranges owing to issues of comparator noise and mismatches between the capacitive

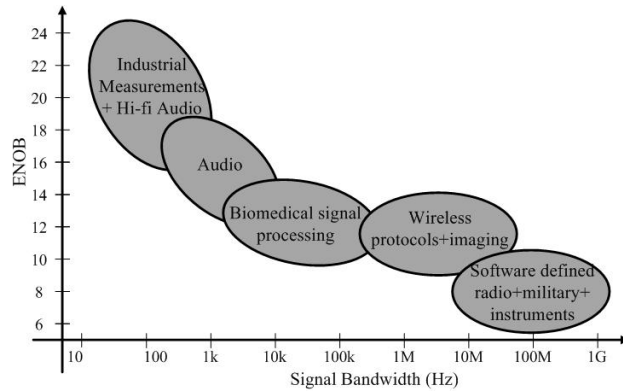


Figure 2.1: ADC performance and applications

digital-to-analog converter (CDAC) elements. Oversampling noise-shaping converters are also being revived in swathes for the power-efficiency they offer for low-moderate bandwidth signals. Furthermore, continuous-time sigma-delta modulators offer an inherent anti-aliasing that relaxes the requirements on the ADC dynamic range by a great amount [3, 4]. However, the problem with noise-shaping ADCs stems from the fact that loop-filters embedded in the loop prove to be a major power sink owing to the high unity gain-bandwidth requirements on them [3]. In addition, the feedback DACs need to be linearized to a high degree for a high-resolution operation which imposes extra power-consumption constraints on the overall design. Furthermore, the largely analog implementation does not admit an easy scaling with process technology that is critical for finer complementary metal-oxide semiconductor (CMOS) nodes.

Voltage-controlled oscillator (VCO)-based ADC has surfaced as a power-efficient, technology-scalable and simple alternative to conventional $\Sigma - \Delta$ modulators [5–14]. The fact that VCO-based architectures are mostly digital makes them amenable to a digital synthesis flow and hence highly attractive from a simplicity-of-design point of view. In spite of all its attractiveness, VCO-based ADCs are plagued by the problem of frequency-voltage non-linearity typical of the VCO core that

limits the overall achievable dynamic range of the entire system. Several approaches have been proposed to allay the non-linearity problem in VCO-ADCs. However, most of these approaches are prohibitively power-hungry, or are not real-time. We shall look into some of these approaches in some detail in the subsequent sections.

In contrast, this work proposes a dithered feed-forward system wherein the input to the VCO is made to look like *white noise* [15]. As a result, the non-linearity in the VCO can only further scramble this noise losing potency to produce spurious signal content. Oversampling in the system suppresses the impact of the scrambled noise within the signal spectrum. The architecture avoids brute-force calibration as well as power-consuming op-amps to suppress the VCO non-linearity.

As a starting basis, however, we shall look into the basic operation of a VCO-ADC first in Section 2.2. Section 2.3 delves into the prior-art that aims to alleviate the non-linearity to develop a high resolution system. Section 2.4 presents the proposed architecture and explains the signal processing details followed by the circuit design nuances in Section 2.5. Section 2.6 shows the test setup and the measurement results for the prototype. Section 2.7 concludes the paper.

2.2 Ring oscillator based VCO-ADC

The basic concept of a VCO-based ADC is shown in Figure 2.2(a). The input signal $V_{in}[n]$ is applied to the control voltage of a ring-VCO. The frequency of oscillation is proportional to $V_{in}[n]$ as shown in Figure 2.2(a). Digital counters following the VCO count the number of rising/falling edges of the VCO output(s), $\Phi_i[n]$, during each sample period T_s . The counter outputs are accumulated to result in the final digital output, $y[n]$. As a result, depending on the frequency of

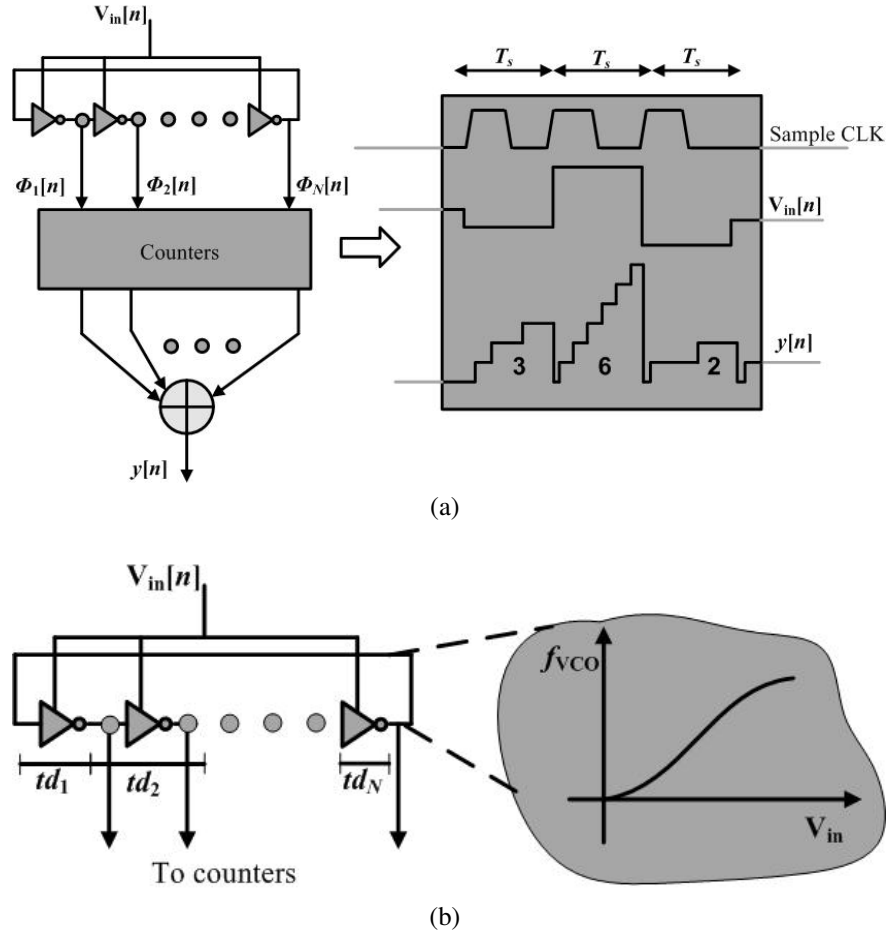


Figure 2.2: VCO-based ADC (a) The Good (b) The Bad and the Ugly

oscillation (that is a direct function of the input voltage), the count $y[n]$ gives a quantized measure of the input, which is the basic principle of any ADC. A VCO-based ADC essentially works upon the principle of phase quantization. Consequently, to maintain continuity in phase between two consecutive sample periods, the present cycle remembers the residual phase of the previous cycle. Based on this argument, it can be shown that the noise introduced due to phase-quantization gets first-order shaped spectrally $(1 - z^{-1})$ [5, 6, 8]. Hence, ring VCO-based ADCs implement, in effect, a first-order $\Delta - \Sigma$ system at a minimal power expense in a low complexity, mostly digital regime [10, 11]. Also note from Figure 2.2(a) that the VCO-based ADC is free of expensive analog

blocks such as amplifiers and is mostly digital. This offers several benefits most of which improve with technology scaling: it can operate at low supply voltages unlike traditional amplifier based ADC designs; it occupies very little die area and consumes very little power. These benefits make the VCO-based ADC particularly suitable for the target application (Figure 2.1).

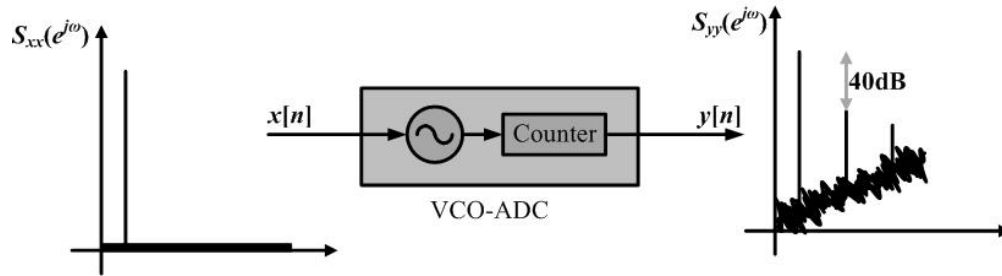


Figure 2.3: Representative signal processing view of VCO-based ADC

However, as hinted in the last section, ring VCOs are quite non-linear. As shown in Figure 2.2(b), the voltage vs. frequency curve of the VCO (often called a tuning curve) is not at all linear. This causes elevated noise floor and spurious tones, thus degrading the spurious free dynamic range (SFDR) and the signal-to-noise-and-distortion-ratio (SNDR) of the ADC.

Besides, there is an additional issue that needs to be dealt with that proves to be a hurdle to building a high-resolution system. The ring-VCO is constituted of multiple delay elements in cascade. Nominally the delays through these elements are matched. However, as illustrated in Figure 2.2(b), inevitable mismatches in the integrated circuit (IC) fabrication process induce mismatch in these delays. Furthermore, voltage-temperature (VT) variations across the die also effect delay mismatches. The mismatches act as look-up table type of non-linearity further degrading the SFDR. However, typically impact of the mismatch is at a much lower level than that of the tuning curve non-linearity and poses as a second-order effect.

Figure 2.3 plots a representative spectrum of the case where a tonal input $x[n]$ is passed through a VCO-based ADC resulting in $y[n]$. Note the first-order shape of the accompanying quantization error in $S_{yy}(e^{j\omega})$. The harmonic content visible in $S_{yy}(e^{j\omega})$ underscores the non-linear behavior of the system, limiting the achievable SNDR to only about 6 – 7 bits.

2.3 Prior-art

Multiple approaches have been proposed to linearize such an ADC to enhance its dynamic range. The major classes of calibration styles for VCO-ADCs can be categorized into four major groups.

2.3.1 Feedback Loop

Like all non-linear systems, feedback is invoked here as well to reduce the effects of non-linearity. Specifically, the VCO-ADC is embedded within a $\Delta - \Sigma$ loop acting as the quantizer illustrated in Figure 2.4(a). The quantizer is preceded by an analog loop-filter of high order (≥ 3). As a result, the VCO sees a small dynamic range signal (the error signal from negative feedback) thereby exercising a small portion of the VCO tuning curve, hence reducing the effects of the non-linearity. However, the analog loop-filter is composed of power-hungry opamps which burn large amounts of static power in order to effect a high filter order [5–7]. Thus, the overall power-efficiency of the system degrades. Furthermore, the opamps in the signal path impose bandwidth constraints and negate several of the aforementioned scaling benefits offered by VCO-based ADCs.

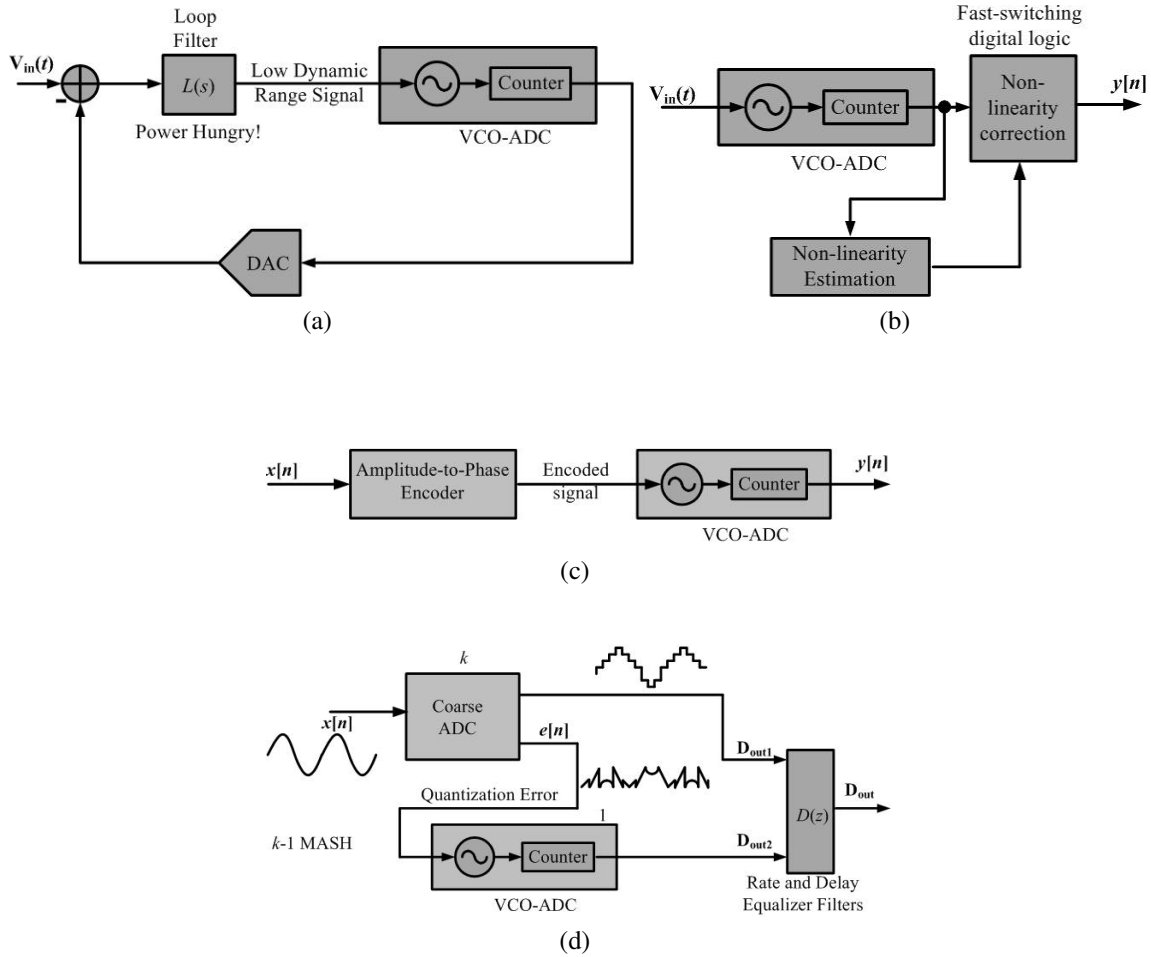


Figure 2.4: VCO-based ADC prior-art (a) Negative feedback through $\Delta - \Sigma$ loop (b) Nonlinearity calibration (c) Input conditioning (d) Pipelining

2.3.2 Foreground Calibration

The VCO-nonlinearity is estimated by applying some known signals in a separate calibration phase. The non-linearity, so estimated is fitted to a polynomial and stored in a look-up table. During actual operation, the ADC output is queried against the look-up table to produce the calibrated result as shown in Figure 2.4(b). However, such techniques are beset with multiple problems. Firstly, looking up a memory for calibration has to happen at the sample-rate of the ADC and can involve a large amount of power consumption. Secondly, the estimated non-linearity is not tracked

real-time and hence overlooks temperature variations, that may prove critical in system-on-chip (SoC) environments [8, 9].

2.3.3 Background calibration

The VCO non-linearity is estimated continuously with the signal without any separate calibration phase (Figure 2.4(b)). Multiple approaches have been proposed to implement the calibration. In [10, 11], the estimation is done using digital dither as a polynomial expansion using multiple digital correlators. The ADC output is subsequently calibrated using the inverse non-linearity, so estimated. This is an attractive approach in the spirit of digital leanings, but can become quite power-hungry since a significant amount of complex digital circuitry switches at the high sampling speed of the ADC [10]. In [12], a replica VCO is used to construct the look-up table in real-time that attempts to track the variations in the actual ADC. The correction is obviously done real time similar to the look-up table queries as described in the foreground mode. This approach is also beset by problems of high power consumption due to high-speed memory access.

2.3.4 Input conditioning

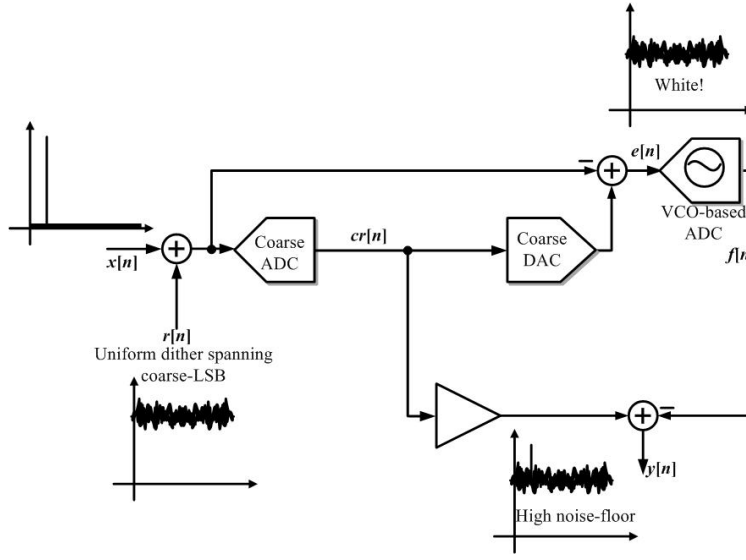
In a few implementations, the input to the VCO-based ADC is suitably conditioned so that it exercises the tuning curve of the VCO in a *linear* manner. An interesting way to effect such conditioning is to encode the amplitude information of the input signal as phase/duty-cycle/pulse-width etc shown in Figure 2.4(c). Such techniques are quite common in transmitter topologies. The work in [13] converts the input signal into a pulse-width modulated (PWM) signal which in an amplitude sense excites only two points of the tuning curve, an operation that is inherently linear.

However, the pulse-width modulator itself consumes significantly large amounts of power and if not designed with caution can spawn undesired non-linear components of its own.

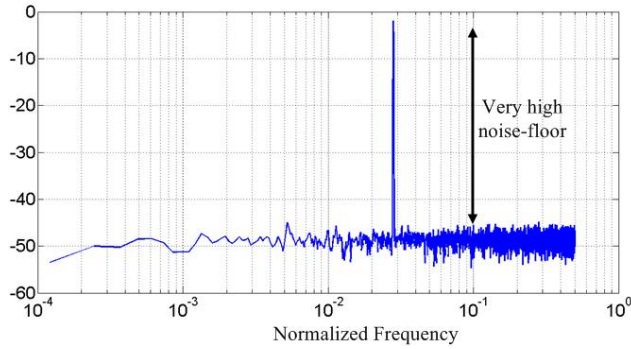
2.3.5 Pipelining

The VCO-ADC is preceded by a coarse-stage ADC such that the former only processes the residue from the coarse stage illustrated in Figure 2.4(d) [7, 14]. The idea is thematically similar to the negative feedback approach for here also the idea is to *show* the VCO a small dynamic range signal to elicit lower non-linearity effects. Depending on the resolution of the coarse-stage the VCO input can have a quite small dynamic range. The outputs of the 2 ADCs are subsequently combined (like in a pipelined ADC) to result in the overall output. However, this approach has to deal with multiple issues. Firstly, to maintain an overall power-budget, the coarse ADC is typically of low resolution (≤ 3 bits). Consequently, the residue fed to the VCO is highly correlated with the input signal [17]. As a result, the non-linearity in the VCO brings out these correlations even further leading to uncorrected input-dependent spurious content in the VCO-ADC output. Representative time-domain waveforms for a sinusoidal input accompany Figure 2.4(d) to emphasize the above-mentioned point. In particular, note the periodicities in the residue signal $e[n]$ that corroborates the demerit of the approach. A second issue is that the gain through the VCO-ADC is an unknown quantity, which needs to be accounted so that the ADC outputs can be combined with minimal coarse-error ($e[n]$)(from Figure 2.4(d)) leaking to the overall output. Typically ad-hoc approaches are resorted to wherein this gain is manually estimated, that makes the system impractical for continuous operations.

With a different approach to tackle the problem in a power-efficient way, this work employs



(a)



(b)

Figure 2.5: Coarse dithering to linearize VCO-based ADC (a) Behavioral model (b) Simulation result

shaped digital dither to essentially randomize the input to the VCO-based ADC in a 0 – 1 MASH architecture, thereby rendering it insensitive to VCO non-linearity [15].

2.4 Proposed Technique: System Level

For notational convenience, in the art of noise-shaping modulators, $i - j$ MASH refers to a cascaded structure where a i -th order noise-shaped modulator is followed by a j -th order one. In

that paradigm, [14] implements a 1 – 1 MASH structure (the second "1" refers to the VCO-ADC) while [16] implements a 0 – 3 structure ("3" is a conventional $\Delta - \Sigma$ modulator). We noted from the pipelining approach (in the last section, Figure 2.4(d)), that for a low-resolution coarse ADC, the residue (quantization error) is deeply correlated with the input signal. As a result, the fine stage (VCO-ADC) further brings out these correlations that remain uncorrected in the overall output. One possible way to further randomize the input to the VCO is to dither the coarse-stage ADC as shown in Figure 2.5(a). An uniformly distributed random signal spanning a coarse-LSB (Δ), dither, is injected to the input signal. Note that Figure 2.4(d) has been redrawn into a 0 – 1 structure in Figure 2.5(a) with the dithering introduced. Such class of dithering is called subtractive, since the dither signal is subtracted from the quantized output to generate the residue ¹. In a behavioral simulation, a sinusoidal input is passed through the structure in Figure 2.5(a) and the power spectral density of the total output $y[n]$ is plotted in Figure 2.5(b). The quantization error from the coarse stage is completely whitened (uncorrelated with the input). However, the coarse ADC output contains this dither and it being at the coarse level (only 2 – 3 bits below the full-scale) degrades the overall SNR severely as shown in Figure 2.5(b). Evolution of an illustrative signal spectrum for a tonal input in Figure 2. 5(a) further clarify the difficulty with a simple coarse-dither.

The way to retrieve the SNR is by pushing the dither energy out of the signal spectrum and concentrating it out-of-band, or in other words by filtering the dither, so that the coarse-stage ADC output is not corrupted by in-band elevated noise floor. The proposition is shown in Figure 2.6. A 2-level, zero-mean Bernoulli random sequence, $d[n]$ (independent and identically distributed with

¹In other words, the quantization error is free of the dither

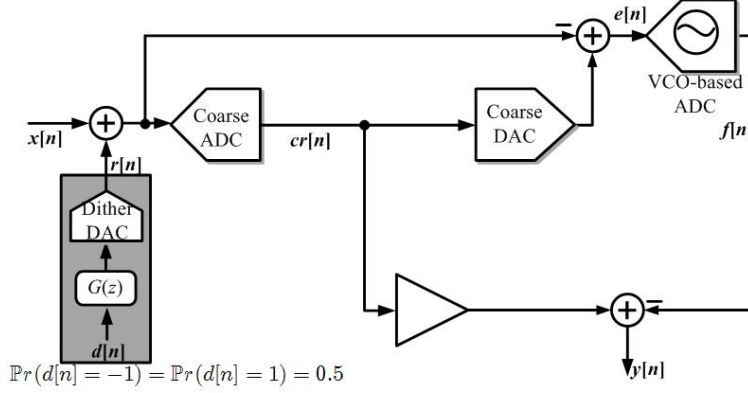


Figure 2.6: Proposed filtering of coarse dither to linearize VCO-based ADC

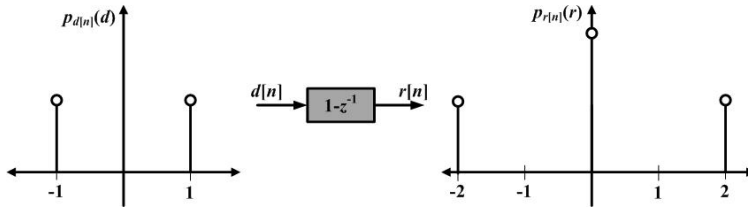


Figure 2.7: Probability mass function (p.m.f) shaping due to filtering

$\mathbb{P}r(d[n] = -1) = \mathbb{P}r(d[n] = 1) = 0.5$), is digitally high-pass filtered ($G(z)$ in Figure 2.6) and added to the input of the coarse-ADC using a digital-to-analog converter (DAC). The gain of the DAC is chosen such that the resultant additive dither is bounded within $[-\Delta/2, \Delta/2]$, where Δ is the quantization step-size of the coarse ADC. However, filtering a signal is equivalent to altering its statistical properties as well. Let's take a simple example.

If we have a simple first-order filter $1 - z^{-1}$, the output of the filter for a Bernoulli input $d[n]$ will be $r[n] = d[n] - d[n - 1]$. The probability mass function (pmf) of the input and the output are shown in Figure 2.7. Clearly, a random signal $d[n]$ has now become correlated and $r[n]$ is not equiprobable to assume any value (unlike $d[n]$). A dither of this type is not guaranteed to ensure a completely white error signal $e[n]$ [17–20] in Figure 2.6. Consequently, the filter $g[n]$ needs to be chosen in such a way that the filtered dither output, $r[n]$ is equipped with the statistical properties

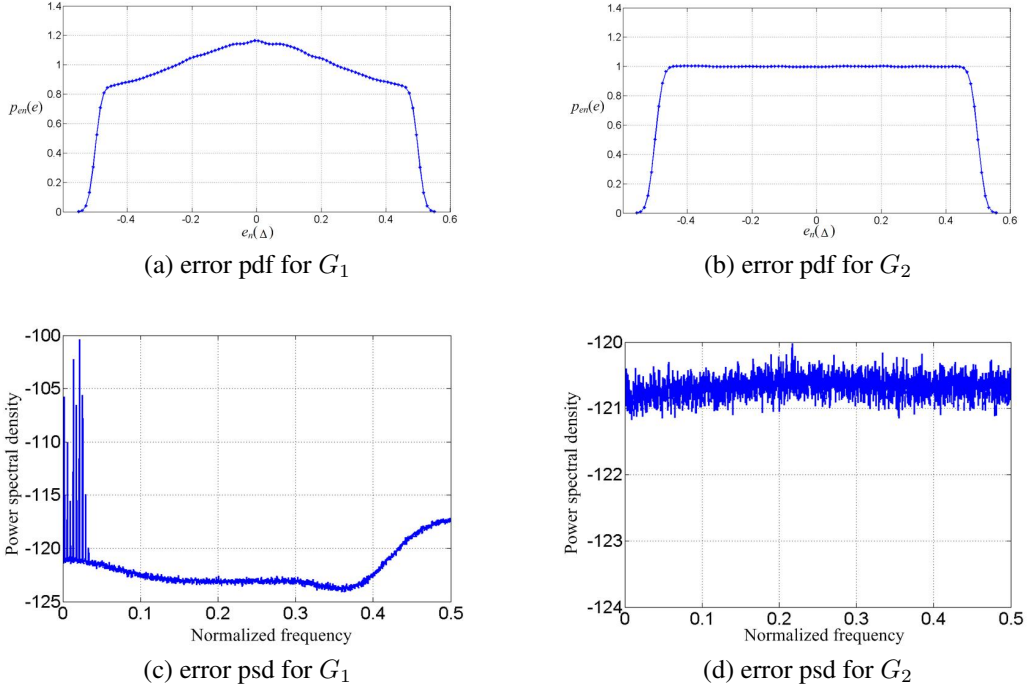


Figure 2.8: Simulation results on the use of an arbitrary filter instead of the prescribed filter

desired [18] as well as being appropriately shaped. To this end, the authors have proposed some specific conditions [21, 23] in which the coefficients of the filter $g[n]$ are specially structured so that the output $r[n]$ is well-behaved. This point is further highlighted in the following brief.

2.4.1 A brief on dithering in ADCs

Consider the coarse-ADC model shown in Figure 2.4(d). We shall define the residue (quantization error) from an ADC to be *well-behaved* if it satisfies the following conditions.

P.1) $e[n]$ is independent of $e[n - m] \forall n \in \mathbb{Z}, m \in \mathbb{Z} - \{0\}$

P.2) $e[n]$ is independent of $x[n - m] \forall n, m \in \mathbb{Z}$

P.3) $e[n]$ is uniformly distributed

The primary condition imposed on any LSB dither signal to ensure these conditions is that the dither signal should be uniformly distributed ². Let us now focus our attention to the filtered dithering scheme shown in Figure 2.6. Remember that for any filtering scheme if the input is uniformly distributed the filtered output is not guaranteed to be uniform anymore (Figure 2.7). Let us assume the dither filter has a finite impulse response (FIR) that vanishes after K samples.

We propose that if

C.1) The FIR filter coefficients $g[k]$ are of the form 2^i where i takes on each value in $[0, s-1]$ at least once

C.2) $L = \sum_{i=0}^{K-1} |g[i]| = 2^s$ where $s \in \mathbb{Z} \cap (1, K]$

then the error sequence pair $(e_n, e_{n-p}) \forall p \in \mathbb{Z} \cap [K, \infty)$ is pairwise independent, each being an identical uniform distribution $\forall (k_1, k_2) \neq (0, 0)$. Furthermore, the aforementioned conditions guarantee that e_n is an identically distributed uniform random variable independent of the input $x_{n-m}, \forall k_1 \in \mathbb{Z}, \forall m \in \mathbb{Z}$. Consequently, these are sufficient conditions to ensure the error signal $e[n]$ is well-behaved. Behavioral simulation results are shown in Figure 2.8. Two different $G(z)$ filters are used for the scheme shown in Figure 2.6.

$$\begin{aligned}
 G_1(z) &= 1 - 3z^{-1} + 5z^{-2} - 9z^{-3} + 3z^{-4} - 3z^{-5} \\
 &\quad + 9z^{-6} - 5z^{-7} + 3z^{-8} - z^{-9} \\
 G_2(z) &= -1 - 2z^{-1} - 4z^{-2} - 8z^{-3} + 16z^{-4} - z^{-5}
 \end{aligned}$$

²This is only a sufficient condition for there can be many other classes of dither distribution viz. triangular [18] that may ensure this, but this is the most obvious and easy-to-meet distribution

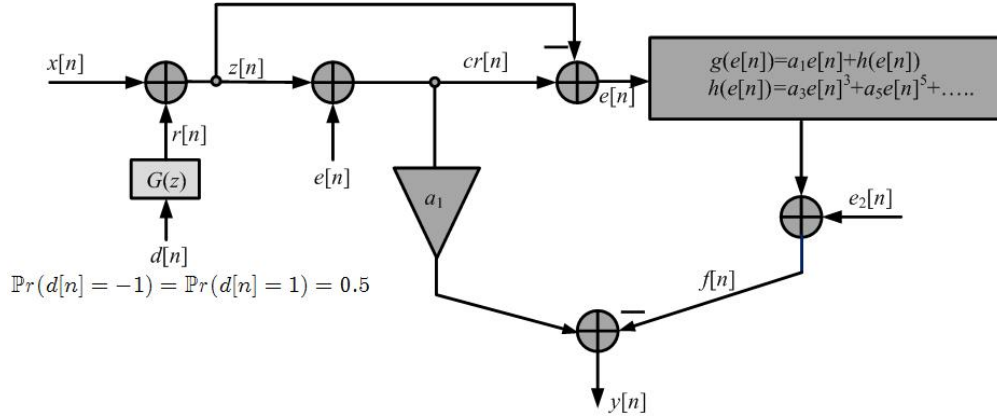


Figure 2.9: Signal processing model of total system

Clearly, $G_1(z)$ does not satisfy any of the conditions above while $G_2(z)$ satisfies both the conditions C.1 and C.2. The probability density function (pdf) of the error signal $e[n]$ is plotted in Figure 2.8(a,b) for the two different filters. G_1 results in a non-uniform pdf while G_2 , as promised, results in a uniform error pdf. Likewise, the power spectral density of the error signal is also plotted for the two different cases in Figure 2.8(c,d). While G_1 renders an input dependent spectrum, G_2 allows a completely white error spectrum.

It should, however be noted that imparting a very aggressive shape to the response of $G(z)$ is difficult satisfying both C.1 and C.2. Hence, we relax the conditions and impose only C.1 on the chosen filter. It is found that the properties enlisted in P.1-3 are met approximately, with the error signal showing a very weak dependence on the input and is almost white with a uniform pdf. It should be understood, that intuitively the effort should be to have a short filter with the smallest possible dither-LSB. The first condition stems from the fact that for longer filters, a large number of dither samples (within the filter length) will be dependent, while the second condition is an attempt to emulate uniform dither as closely as possible.

The advantage of the approach can now be appreciated. Since the VCO non-linearity only acts on white noise from independent sources, hence it loses potency to produce tones. Mathematically, if the VCO characteristics can be written as $f[n] = a_1e[n] + h(e[n])$ where $h(u)$ is a memoryless polynomial nonlinear function, then from Figure 2.6,

$$\begin{aligned}
cr[n](\text{Coarse-ADC output}) &= x[n] + e[n] + r[n] \\
f[n](\text{Fine-ADC output}) &= a_1e[n] + h(e[n]) + e_2[n] \\
y[n](\text{Total output}) &= a_1cr[n] - f[n] \\
&= a_1x[n] + a_1r[n] - h(e[n]) \\
&\quad - e_2[n] \tag{2.1}
\end{aligned}$$

where $r[n]$, $e[n]$ and $e_2[n]$ are the filtered dither, quantization error from the coarse-ADC and quantization error from the fine (VCO-based) ADC respectively.

From Eqn. 2.1, since $r[n]$ has negligible in-band content so it does not corrupt the SNR. Also the dither makes the VCO-input $e[n]$ white, which makes the resultant error ($h(e[n])$ in Eqn. 2.1) devoid of any spurious tones and spreads it in $[0, F_s/2]$. The resultant elevated noise-floor causes negligible error owing to oversampling. A top-level signal-processing model is shown in Figure 2.9. The coarse-stage ADC has been modeled as an input-dependent additive error. The VCO-ADC has been modeled as a polynomial non-linearity in conjunction with an additive fine stage quantization error $e_2[n]$.

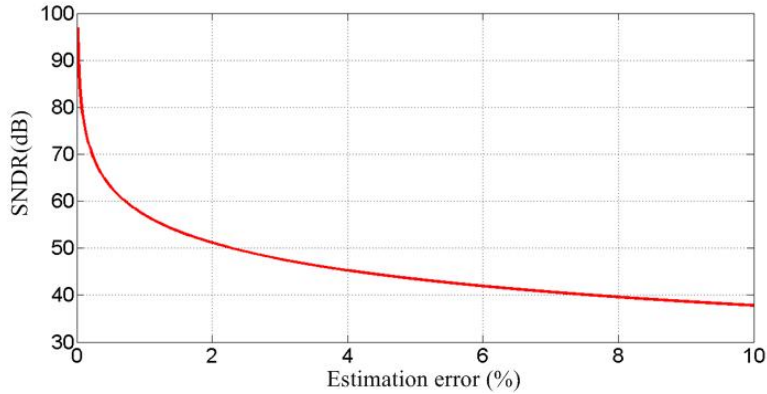


Figure 2.10: Achievable SNDR vs. VCO-gain estimation error based on Eqn. 2.3

The dithering scheme allows another implicit benefit. As explained in Section 2.2, the non-matched delays between the individual elements in a ring-VCO causes additional non-linearity³ in the ADC operation. The whitening of the VCO-input enables this non-linear behavior to be also combatted in a similar fashion since the entries in the look-up table are now chosen randomly! It is perhaps of interest to note that a similar dither filter had been used in a previous work [22] to combat non-linearities in a fractional- N PLL.

2.4.2 Performance Bounds

From Figures 2.4(d), 2.5(a) and 2.6, the total output $y[n]$ is obtained by combining the outputs of the constituent ADCs, namely $cr[n]$ and $f[n]$. For a perfect cancelation of the coarse-stage quantization error $e[n]$, the coarse-stage output $cr[n]$ must be scaled with the accurate gain that $e[n]$ "sees" through the fine path. Inaccuracies in the gain-estimation will limit the performance benefits of the overall system. The magnitude of the limit can be understood using the following relations. For the sake of argument, let us consider that the VCO-ADC is a completely linear

³though of a look-up type, different from a polynomial representation

element having a gain of a_1 . Suppose that a_1 is estimated with an error ϵ . As a result, based on Eqn. 2.1, the total output can be written as

$$y[n] = a_1(1 + \epsilon)x[n] + a_1(1 + \epsilon)r[n] + a_1\epsilon e[n] - e_2[n] \quad (2.2)$$

From Eqn. 2.2, assuming the dither filter pushes out most of the energy of $r[n]$ out of the spectral content of $x[n]$, the only polluting quantity would be the term $\epsilon e[n]$. In fact, assuming a white $e[n]$ ⁴, it is not difficult to show that the SNR will be limited as

$$10 \log_{10} \left[\frac{3}{2} \times \left(1 + \frac{1}{\epsilon}\right)^2 \times \frac{F_s}{B} \times 2^{2m} \right] \quad (2.3)$$

where F_s is the sampling frequency, $B/2$ is the maximum signal bandwidth and m is the resolution of the coarse-ADC. Thus, the ratio F_s/B denotes the oversampling ratio.

Based on Eqn. 2.3, Figure 2.10 plots the achievable theoretical SNDR as a function of the estimation error ϵ . From Figure 2.10, ϵ is required to be in the 1% regime for realizing a > 10 bit system. In the subsequent section, we shall see how we have resorted to a correlation-based gain estimator [10, 25] to estimate the linear gain to a very high accuracy.

As we had seen before, the filtered dithering scheme enables the VCO to process a white noise input that eliminates spurious signal-dependent content from showing in the total output. However, non-linearity acting on the white signal results in an elevated noise floor that folds back in the signal band. Depending on the amount of oversampling the achievable SNR may be curtailed due to this

⁴this may be an over-simplified assumption for low resolution coarse-ADCs but suffices for the argument we want to put forth

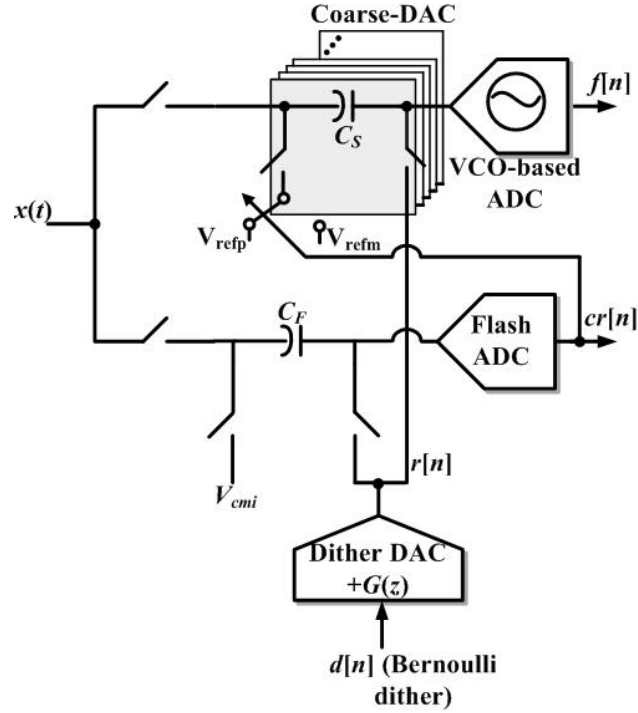


Figure 2.11: Coarse ADC and DAC structure

mechanism. In fact, if the non-linearity of the VCO can be expressed as a third-degree polynomial (admissible for weak-to-moderate non-linearities)

$$y = a_1x - a_3x^3 \quad (2.4)$$

then, the folded-in power due to the non-linearity over the entire band can be calculated as

$$\frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} x^6 dx = \frac{\Delta^6}{448} \quad (2.5)$$

where Δ is the coarse-ADC step size. The aforementioned noise sources should be budgeted to be below the desired resolution from the ADC, depending on the value of the chosen input amplitude, resolution of the coarse stage, the oversampling ratio and the accuracy of the gain-error estimate

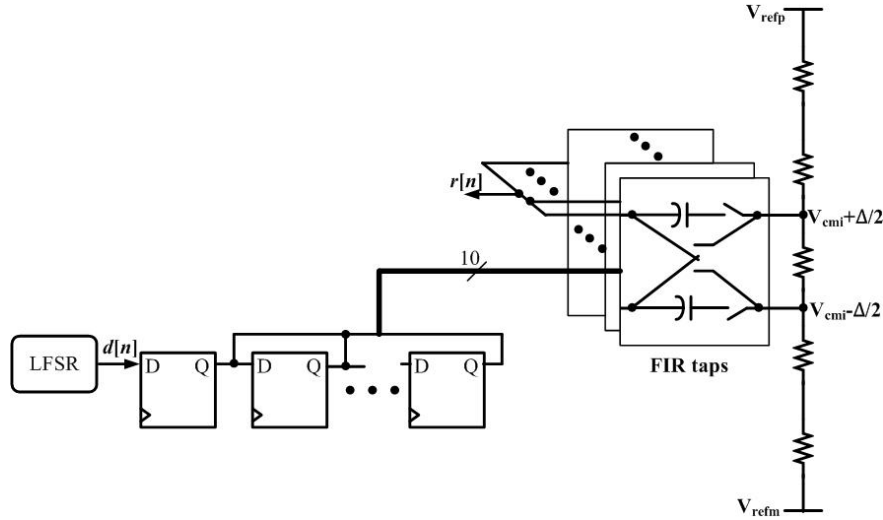


Figure 2.12: Filtered dither generation

etc. We shall cover some of these design choices in the next section.

2.5 Proposed Technique: Circuit Level and other digital signal conditioning

2.5.1 Coarse Stage

A top-level circuit description for the coarse-stage is presented in Figure 2.11. The incoming signal $x(t)$ is sampled on a bank of capacitors ($C_s + C_F$) using bootstrapped switches. C_F is the set of capacitors that is dedicated for the coarse-ADC while C_s is entrusted with sampling the input signal and subtracting the coarse-ADC decision to result in the residue that is fed to the VCO-ADC. The sampling is done in a 3-way time-interleaved mode (with only one high-speed coarse-ADC structure) to relax the settling requirements on the DAC. The three way interleaved structure is nominally matched, with no extra calibration done for residual mismatches since any images so formed do not corrupt the in-band signal content due to the large oversampling involved. The sets of capacitors C_s and C_F are sized appropriately to ensure a low kT/C noise within the

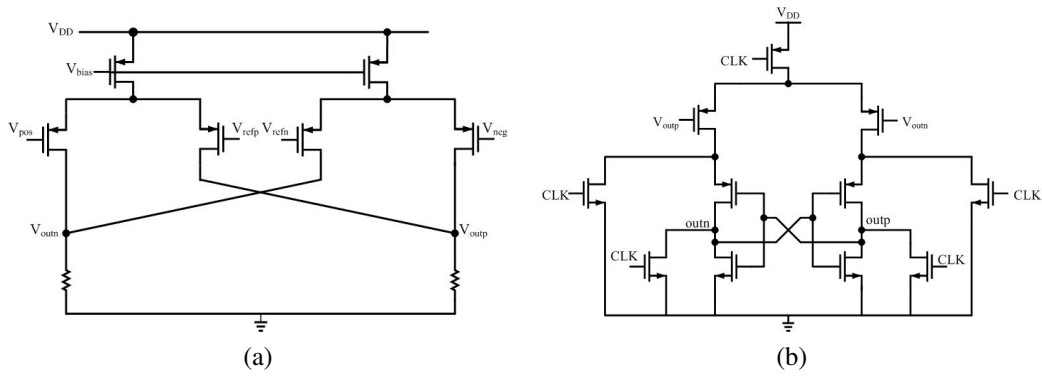


Figure 2.13: Coarse flash ADC components: (a) Preamplifier (b) Dynamic latch

quantization noise budget.

The filtered dither is generated as shown in Figure 2.12. The dither filter used in this work is

$$G(z) = 1 - 4z^{-1} + 4z^{-2} - z^{-3} + 2z^{-4} - 2z^{-5} + z^{-6} - 4z^{-7} + 4z^{-8} - z^{-9}$$

This filter choice is not unique and as discussed in Section 2.2, out of the several filters that effectively whiten the VCO input [23], this filter ensured minimal SNDR degradation from the added dither due to its aggressive high-pass shape. A pseudo-random dither signal $d[n]$ with equal probability of being 0 or 1 is passed through a shift register, with the outputs from the shift register (Figure 2.12), Q_i switching a weighted capacitor array (based on the FIR filter weights). The sign inversions in $G(z)$ are effected through a differential swapping between the positive and the negative nodes as shown in Figure 2.12. It should be borne in mind that errors in the dither-DAC (mismatches in the capacitors) introduce negligible errors, by virtue of the randomness of the dither input. The dither-DAC output is used as the common-mode for the sampling operation of C_s and C_F [24].

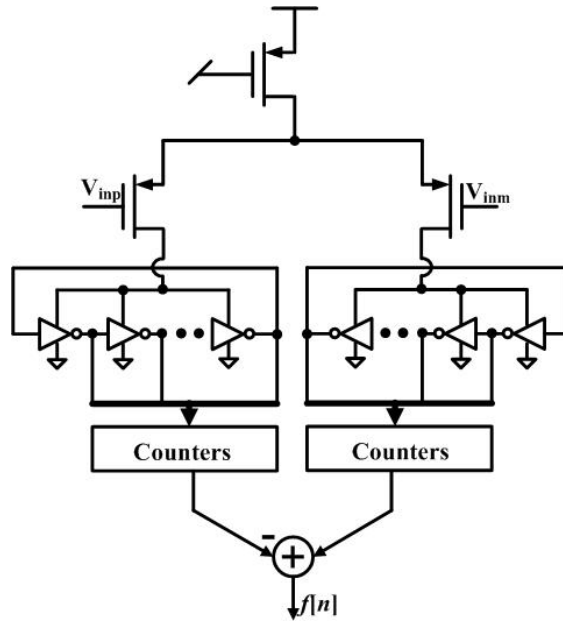


Figure 2.14: Differential ring VCO

The bootstrapped switches used in this design are based on [30]. The coarse-ADC is implemented as a $2 - b$ flash architecture. The implementation is shown in Figure 2.13. The flash architecture consists of 4 identical comparators that are made up of a low-power preamplifier and a dynamic latch [31]. The coarse-DAC is implemented as a passive structure with the residue being generated without any active circuitry to save power [25,26]. The accompanying parasitic-induced errors are accounted for by another signal conditioning technique discussed next.

2.5.2 Fine Stage and Other Digital Conditioning

The VCO-based ADC is implemented as a 33-stage differential architecture as shown in Figure 2.14 [6]. The differential input voltage is passed through a g_m -stage and the resulting signal currents control the oscillation frequency. The passive-DAC structure and the subsequent g_m stage, without any *virtual ground* effect realized through high gain amplifiers, is reminiscent of the open-

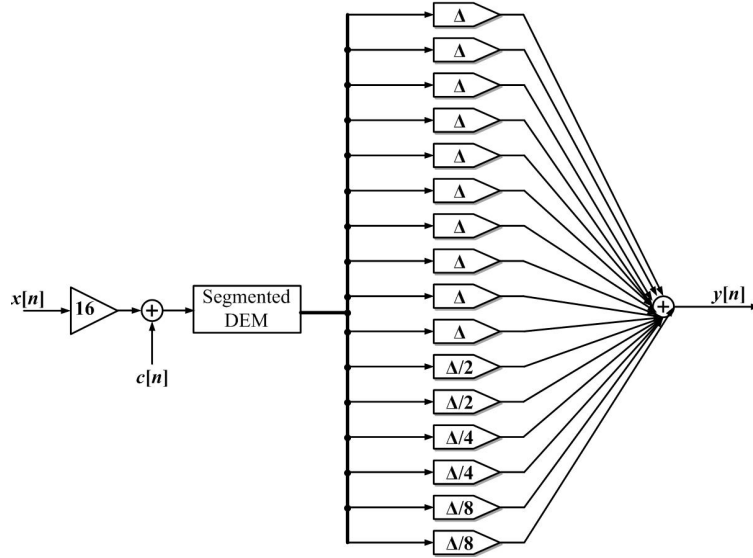


Figure 2.15: Segmented coarse DAC

loop residue amplification techniques treated in [28, 29].

The outputs of the flash-ADC and the VCO-ADC are combined using background gain calibration based on a correlation based gain estimator [25]. A random sequence $c[n]$ which follows the statistics $\mathbb{P}r(c[n] = -\Delta/16) = \mathbb{P}r(c[n] = \Delta/16) = 0.5$ (referred to the coarse-DAC output) is added to the coarse-stage output $cr[n]$ as shown in Figure 2.16. Consequently, $c[n]$ traverses the same path as the error signal $e[n]$ and hence when the fine-stage output $f[n]$ is correlated against $c[n]$, the gain through the coarse-stage DAC and the fine-stage can be estimated. This gain estimation takes care of the parasitic errors arising due to the complete passive operation as well. It should be noted that the non-linear term in the tuning curve (Eqn. 2.4) pollutes the gain-estimate so obtained, hence some additional signal processing needs to be performed to cancel its effect [26].

Any errors in the coarse-stage arising out of mismatches in the coarse-DAC would have shown as degraded SNDR in the overall output. Dynamic element matching (DEM) is employed to counter any static mismatches from the coarse DAC [32] using random sequences $s[n]$, as shown in

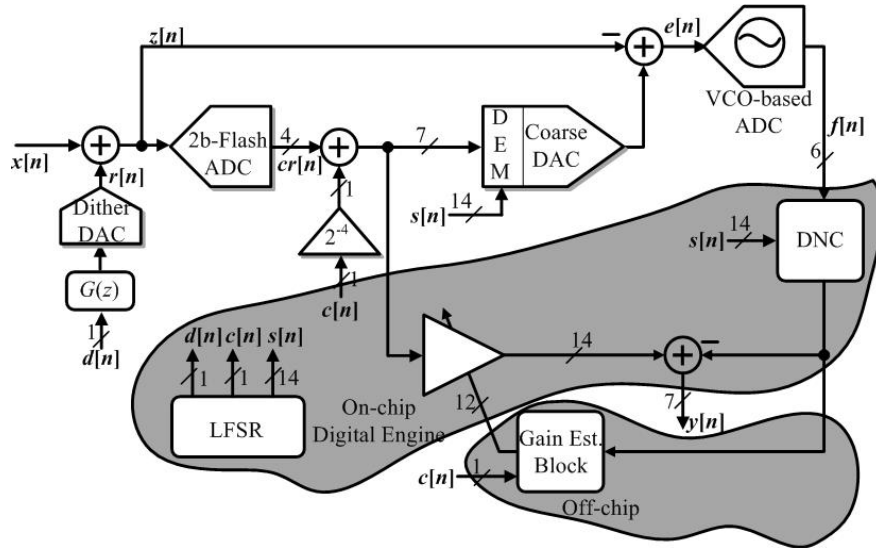


Figure 2.16: Overall structure in IC prototype

Figures 2.15 and 2.16. The addition of the random calibration sequence $c[n]$ to the Flash-ADC output $cr[n]$ at a much lower level enhances its effective dynamic range. Consequently, a segmented DEM architecture [33, 34] is chosen. The DEM block output is a 14-bit sequence that drives the segmented coarse-DAC structure as shown in Figures 2.15 and 2.16. Programmability options to first-order shape the DEM switching sequences $s[n]$ are also provided. It should be noted that since the coarse-DAC scrambles/shapes the error only up to a resolution of the coarse stage, hence an elevated noise floor deteriorates the SNR to a large extent. As a result, the static DAC errors Δ_i are estimated by correlating the fine stage output with the switching sequences $s[n]$ [25, 27] and then the scaled random sequences $\Delta_i s_i[n]$ are subtracted from the overall output. This technique is popular in technical art as DAC noise cancelation for high-resolution systems [25, 27]. It should be understood that the estimations of the static quantities, namely the DAC errors Δ_i or the gain through the coarse-DAC and VCO combination are expected to change ever so slowly and hence they are carried out off-the-chip in a MATLAB environment at a downsampled rate of

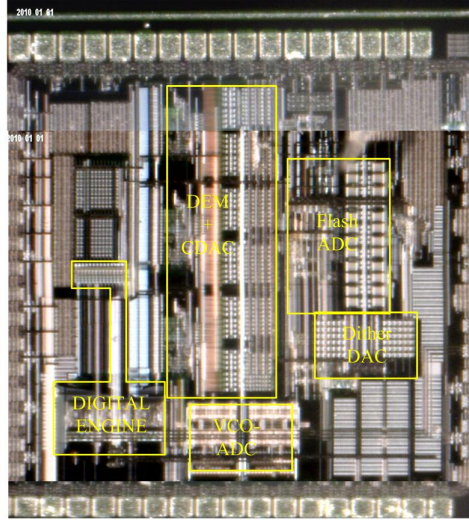


Figure 2.17: Die micrograph

1MHz to save power. However, the corrections are done continuously using low-power on-chip digital engines.

The random quantities essential in the operation of the chip namely the digital dither whitening the VCO input $d[n]$, the calibration sequence $c[n]$ and the DEM sequences $s_k[n], k = 1, 2, \dots, 14$ are generated using a linear-feedback shift register (LFSR) that is architected in an interpolated manner [35] to ensure a large degree of independence between the sequences in a power-efficient way.

Clocking in such systems is crucial to ensure a low-jitter operation so that it does not cause any SNDR degradation. A 2GHz LVDS clock is applied as an input from an off-chip high-precision signal generator. The clock is made full-swing (rail-to-rail) and then further processed to generate the different clock signals required.

Parameter	[6]	[10]	[14]	[7]	This work
Type	$\Delta - \Sigma$ loop	BG calibration	1 – 1 MASH	$\Delta - \Sigma$ loop	Dithering
Technology(nm)	130	65	130	90	65
F_s (MHz)	900	2400	1200	600	1000
Bandwidth(MHz)	20	37.5	4	10	30/50
SNDR(dB)	78.1	70	77	78	64/60
Power(mW)	87	39	13.8	16	8.2
FoM(fJ/conv.step)	330	201	298	125	87/94
Area(mm ²)	0.45	0.075	0.7	0.36	0.62

Table 2.1: Comparison with state-of-the-art

2.6 Measurement Results

The ADC is realized in 65nm CMOS technology at an analog (coarse-stage, VCO, dither-DAC) supply voltage of 1V and a digital (gain calibration, combination) supply voltage of 0.8V with MiM capacitor option. The fabricated IC is wire-bonded on a printed circuit board (PCB) for evaluation. The associated pads for connecting the IC to the external world have human-body model (HBM) ESD protection circuitry embedded in them.

The IC consists of the structure shown in Figure 2.16 with an active area of 0.6 mm². The analog part occupies an area of 70% while the digital part accounts for the remaining 30%. The non-availability of higher density MiM-caps for the process contributed to the chip area growing larger than state-of-the-art. A more advanced process with higher capacitance densities would result in a great reduction in the overall area. The fabricated die micrograph is shown in Figure 2.17 that demarcates different modules in the IC.

The ADC sampling rate F_s is set at 1GHz. The total power consumed is about 8.2mW with a break-up of 5.5mW for the analog domain and 2.7mW for the digital domain. The low-speed

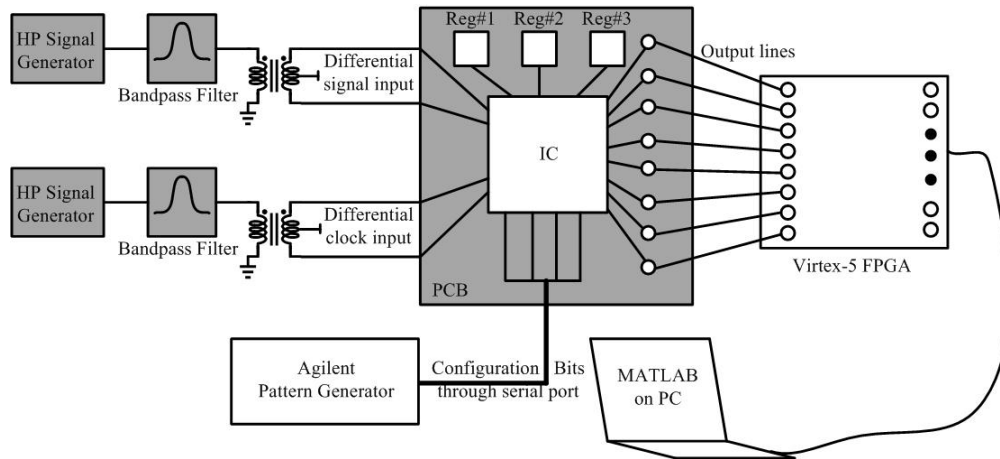


Figure 2.18: Representative test setup

correlation-based gain estimation is done off-the-chip using MATLAB while the on-chip digital engine multiplies $cr[n]$ with this estimate and adds it to $f[n]$ (Figure 2.16)-the latter constitutes bulk of the digital power consumption.

A representative test setup is shown in Figure 2.18. The printed circuit board (PCB) design for evaluating the chip has to cater to a few needs, typical of high-resolution ADC systems. The PCB consists of the wire-bonded chip with multiple regulators to generate the low-noise supplies and the references. Sufficient bypass capacitors with varied frequency responses are provided on the PCB to minimize switching-induced bounce on the supply lines. 50Ω lines are matched and fabricated to minimize reflections on the high-frequency input clock and output clock and data lines. Both the high-frequency clock and data lines are provided by accurate signal generators with sharp band-pass filters to eliminate all out-of-band spurious contents. The PCB also has provisions for communicating the serial port signals for configuring the chip from a pattern generator (Agilent 16720A) as well as multiple SMA ports to capture the high-speed data onto a FPGA (Virtex-5 on a ML-310 board). The data from the FPGA is parallelized and processed in MATLAB in

a PC environment. Two randomly chosen chips were tested using the setup with no significant differences in the results.

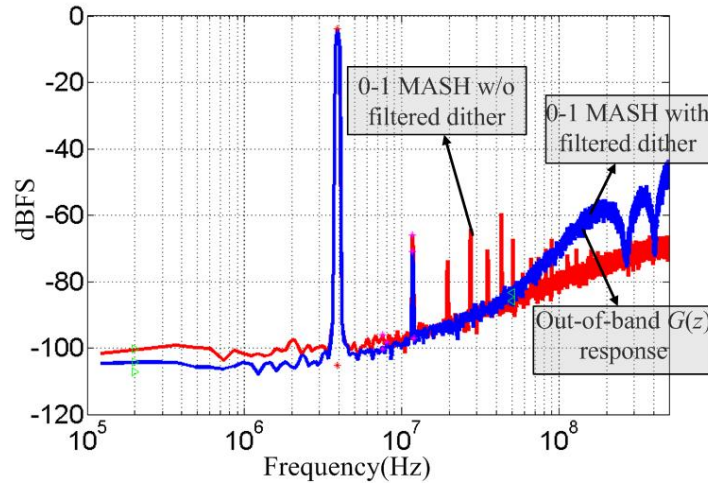


Figure 2.19: Measured performance with and without technique

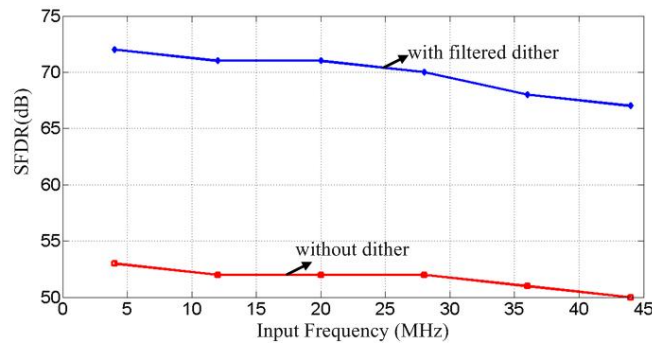


Figure 2.20: Measured SFDR vs. input frequency

The measured power spectral density (PSD) plot for a tonal input at -4dBFS at 3.9MHz is shown with and without the dithering mode in Figure 2.19. As can be seen from Figure 2.19, a simple $0 - 1$ MASH architecture (without dithering) results in a highly adulterated spectrum with uncanceled harmonic content resulting in a SNDR of 50 dB and a SFDR of 60 dB . However, with the filtered dithering mode enabled, most of the spurious content is eliminated. The out-of-band spectral response of the $G(z)$ filter is distinguishable. The residual spurious content (third

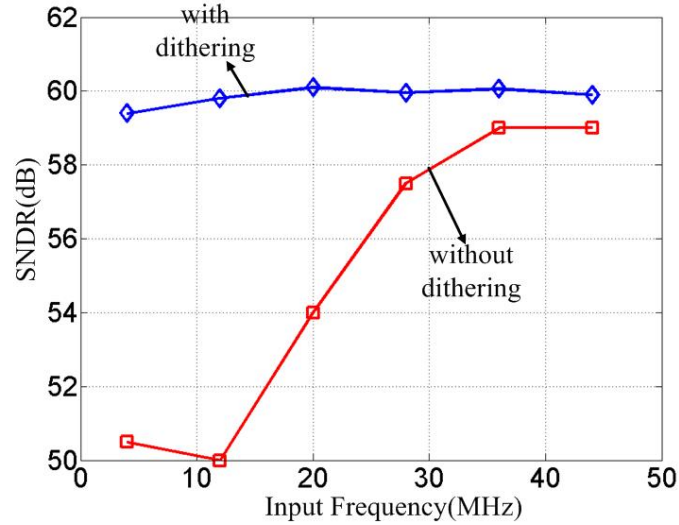


Figure 2.21: Measured SNDR vs. input frequency

harmonic of the input signal) is a result of an unforeseen issue in the dither-DAC buffer design and has nothing to do with the technique per se. The measured SNDR and SFDR with the filtered-dithering mode enabled is 60dB and 74dB respectively, almost 10dB improvement in measured SNDR. The measured FoM is 90fJ/conv.step.

The relationship between the harmonic distortion and the applied input frequency is plotted in Figure 2.20 that shows the SFDR as a function of the input frequency with and without the dithering mode. The dithering particularly helps in mitigating the harmonic distortion artifacts as can be appreciated from Figure 2.20. Figure 2.21 plots the SNDR improvement for different input frequencies without and with the dithering technique (for a -4dBFS input), where the latter shows significant SNDR improvement. The measured dynamic range of the converter is illustrated in Figure 2.22 for a few different applied frequencies. All of them nearly show the same linear trend with a slight degradation near the full-scale. The IC is operated over different noise integration bandwidths and the system performance evaluated. The measured Figure-of-Merit (Schreirer FoM

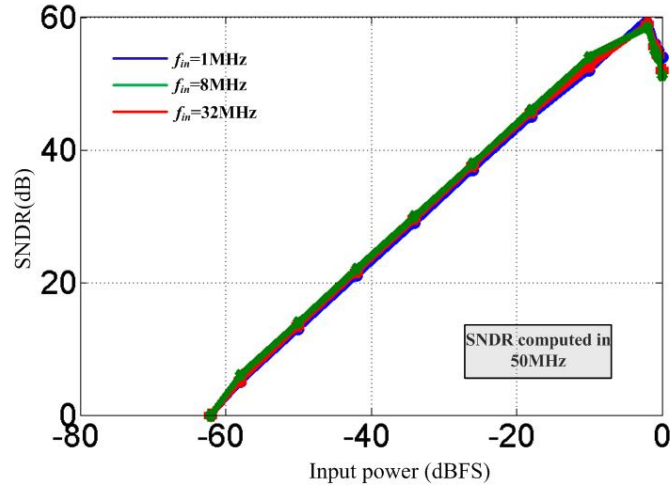


Figure 2.22: Measured dynamic range of the system for different input frequencies

as in [28]) is plotted in Figure 2.23 which shows a roughly uniform trend over a large range of bandwidths promising a wide range of reconfigurability for any system it is employed in. The different operating behaviors of the system vis-a-vis other competing works are projected in Table 1. From the table, it can be seen, that the proposed structure outperforms the state-of-the-art in terms of the reported figure of merit for comparable bandwidths of operation.

2.7 Conclusion

An open-loop signal-conditioning based technique for mitigating the effects of nonlinearity in VCO-based ADCs is presented. The technique relies on using the VCO-based ADC as the second stage in a 0-1 MASH architecture as well as applying a specially filtered dither to the input signal for whitening the VCO input. The prototype built based on the proposed technique is able to achieve the best FoM out of all published VCO-based ADCs.

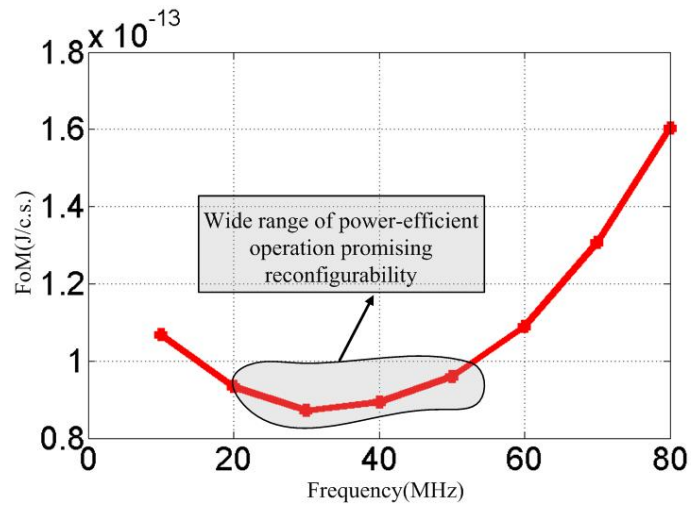


Figure 2.23: Measured FoM of the system for varying noise-integration bandwidths

2.8 Acknowledgement

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CHAPTER 3

Phase Mismatches in Time-Interleaved ADCs: A tutorial

3.1 Introduction

With the usable frequency spectrum becoming more crowded with every passing day, chaffing out the relevant signal of interest with high-fidelity is getting increasingly more difficult. The electronics industry is pushing towards full-spectrum capture receivers for most of these applications wherein the entire spectrum (constituted by the desired signal, the in-band blockers, the out-of-band blockers etc.) is received and conditioned by front-end amplifiers and then digitized by a single Analog-to-Digital converter(ADC). Consequently, for such full-spectrum capture (FSC) scenarios, the ADCs need to be really wideband. At the same time, since the desired channel in the received spectrum needs to be digitally filtered out with high-accuracy, the ADC needs to be of high dynamic range (typically in the range of 8 – 11 bits) [1].

To that end, several ADC architectures have been proposed which can operate on signals having large bandwidths as well as high dynamic ranges. Time-interleaved ADC architectures have proved to be one of the most suitable candidates for this purpose [2–4]. The architecture is essentially similar to a time-division multiplexing scheme (TDM) composed of M channels in a standard communication network, wherein each channel is operated once in every M cycles. Time-interleaving

enables wideband operation with each sub-band ADC operating at a low frequency and thus, in an energy-efficient way. However, time-interleaved architectures are fraught with problems of inevitable mismatches between the nominally identical channels. The mismatches, in different forms, induce errors in the ADC output that curtail the achievable dynamic range of the receiver and hence limit the use of time-interleaved architectures in high-resolution systems. Several calibration strategies have been proposed both by the circuits and signal-processing communities to mitigate the effects of the mismatch induced errors. However, there seems to be a distinct gulf between the two communities in the approaches they take for calibrations. This work will attempt to survey most of the published techniques, in no way claiming to be exhaustive, and marry the notions from both the communities.

In that spirit, we shall take a closer look at the operation of a time-interleaved ADC in the next section. Section 3.3 will take a brief look at the calibration methods for gain and offset mismatches. We shall take a detailed look at the calibration methods proposed for timing mismatches both of analog and digital flavors in Section 3.4 while the proposed methods for bandwidth mismatch calibration are looked into in Section 3.5. Section 3.6 concludes the chapter.

3.2 Time-Interleaved ADCs: modeling and effects

The basic architecture is illustrated in Figure 3.1. The incoming signal $x(t)$ is processed by M parallel branches, such that each branch operates on the signal with a time-period MT_s where T_s is the overall sampling time for the ADC, satisfying $F_s = 1/T_s$ (F_s is the sampling frequency). It is assumed that $x(t)$ is a band-limited signal with a bandwidth B such that $F_s > 2B$ (the

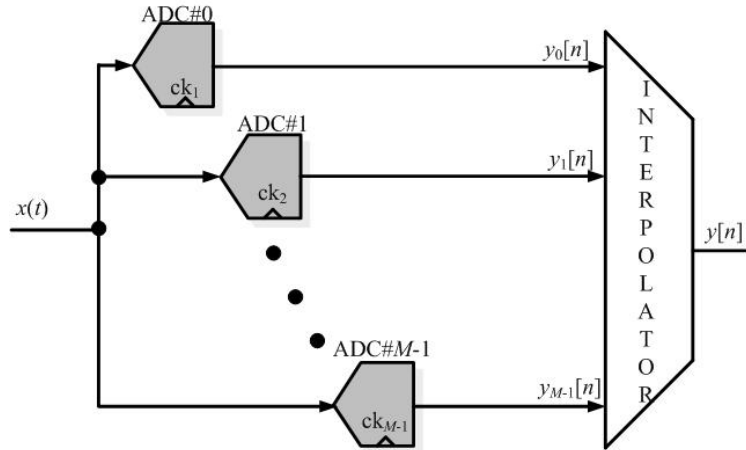


Figure 3.1: Time-interleaved ADC: model

familiar Nyquist relation). Since each individual branch operates only at a speed F_s/M , hence realization of a single ADC becomes quite feasible and economical at a nominal power expense. The digital outputs of each individual ADC $y_i[n]$ where $i \in [0, M - 1]$ are combined to result in the final digital output $y[n]$. A large volume of literature is available that reports successful implementations of high-speed time-interleaved ADCs [5 – 10, 12, 14 – 16] with varying dynamic ranges, depending on the application. In the discussions and treatises to follow, we shall use these notations extensively assuming familiarity from the reader.

Time-interleaved architectures, though apparently very elegant, are plagued with issues attributed to inevitable mismatches between the individual branches typical of any practical implementation. The parallel branches can be mismatched in several different ways, primarily which can be grouped into four major classes: [3,4](as shown in Figure 3.2 for the i -th channel), namely

- DC offset mismatches
- Gain mismatches

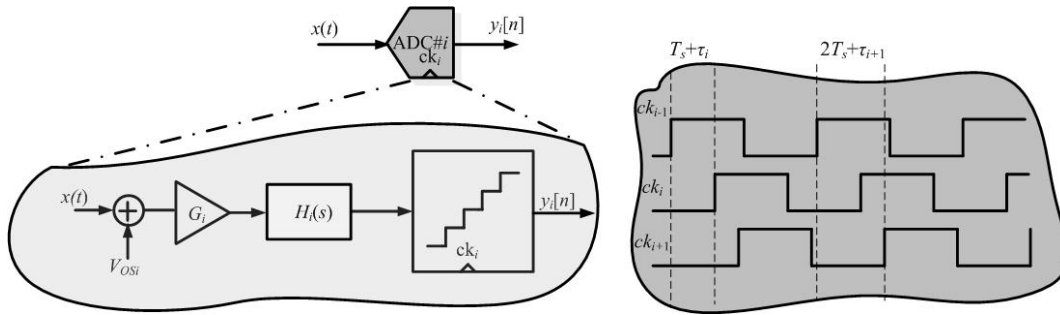


Figure 3.2: Time-interleaved ADC: error sources

- Timing mismatches
- Bandwidth mismatches

Let's try to get a clearer understanding of each of these effects.

3.2.0.1 DC offset mismatches

Each channel has an unknown constant inadvertently added to the incoming signal and these constants vary across channels. Typically, such effects arise from random offsets in the comparator (the arbitrator inside any ADC) that are unique to each interleaved channel [3, 16, 17]. Mathematically, such an effect can be described as, for the i -th channel output y_i ,

$$y_i[n] = x(t) + o_i|_{t=(n-1)MT_s+(i+1)T_s} \quad (3.1)$$

Once the outputs of the individual ADCs are combined, it is not difficult to see that DC offset mismatches will lead to tones resulting at multiples of F_s/M , independent of the signal content.

3.2.0.2 Gain mismatches

Each channel multiplies the incoming signal by a different amount (G_i for the i -th channel), that varies across the channels with the variation being attributed to both systematic (layout mismatches etc.) and random components [4, 18, 19]. In the presence of gain mismatches, the output of the i -th channel can be expressed as,

$$y_i[n] = G_i x(t)|_{t=(n-1)MT_s+(i+1)T_s} \quad (3.2)$$

Unlike DC-offset mismatches, this is a *multiplicative* error, and hence it causes signal dependent images at $F_s/M \pm f_{in}$ where f_{in} is the input signal frequency. The magnitude of the image is evidently scaled by the gain mismatch quantities.

3.2.0.3 Timing mismatches

In a time-interleaved ADC, each channel is supposed to sample the incoming signal T_s seconds after its preceding channel. However, readers familiar with analog integrated circuit (IC) design would appreciate that such precise control on the timing instants is impossible due to inevitable clock-line routing mismatches etc. Consequently, the signal $x(t)$ is sampled non-uniformly at instants defined by the set $\mathbb{T} = \{nMT_s + \tau_0, nMT_s + T_s + \tau_1, nMT_s + 2T_s + \tau_2 \dots, nMT_s + (M-1)T_s + \tau_{M-1}\}$, $n \in \mathbb{N} \cup \{0\}$ (Figure 3.2). As before, the i -th channel output in the face of timing mismatches can be expressed as,

$$y_i[n] = x(t + \tau_i)|_{t=(n-1)MT_s+(i+1)T_s} \quad (3.3)$$

The discerning reader should be able to distinguish such an error from a simple additive or multiplicative error discussed before. For instance, for a static(dc) signal, timing mismatches between the channels won't give rise to any error because wherever one samples, one always gets to digitize the same value. Extending the argument, for a very slowly varying signal (let's say a 50Hz signal), the amount of error incurred due to small timing mismatches would be negligible [6, 10]. However, for a very rapidly changing signal, even small timing mismatches can result in errors that may degrade the signal-to-noise and distortion ratio (SNDR) appreciably. Hence, it's not difficult to see that timing mismatch errors cause signal-slope dependent images around multiples of F_s/M , with the image strength again being a function of the timing mismatch amount.

3.2.0.4 Bandwidth mismatch

Each channel effectively presents some form of low-pass filtering (may not be explicit always) on the incoming signal before it is sampled. Nominally, the filters on each channel are identical.

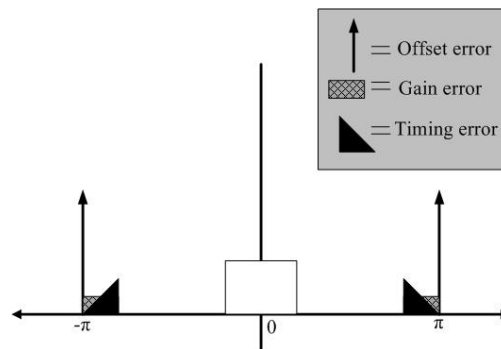


Figure 3.3: Mismatch effects on output spectrum for a 2-channel ADC

However, as before, mismatches between the filter responses (typically in the sample-and-hold stage or SHA) across the channels gives rise to errors in the reconstructed signal. Let's take an example with a sinusoidal input $x(t) = A \sin(\omega_0 t)$. Now, let us assume that the i -th channel filter

has a transfer function $H_i(j\omega)$ [20, 22, 23]. Hence, it is easy to see that in the presence of only bandwidth mismatches, the i -th channel output can be expressed as

$$y_i[n] = |H_i(j\omega_0)|A \sin(\omega_0 t + \angle H_i(j\omega_0)) \Big|_{t=(n-1)MT_s+(i+1)T_s} \quad (3.4)$$

Thematically, this is similar to gain and timing mismatches described above. However, the gain and timing mismatch amounts are input signal spectral content dependent. Consequently, these can cause complex images around multiples of F_s/M . Bandwidth mismatches are gaining notoriety with the operable bandwidths of the ADCs increasing. This stems from the fact that since each channel is now operating at higher frequencies, nearing the pole of the SHA filter, mismatch effects are becoming all the more pronounced. For a given output rate, increasing the number of channels would lower the operating frequency of each channel, and hence reduce the effects of bandwidth mismatch.

Figure 3.3 presents the overall impact of all these mismatches in a representative spectrum for a generic input signal $x(t)$ corresponding to a 2-channel ADC. In the presence of all these imperfections, time-interleaved ADCs can severely curtail the overall dynamic range even if each sub-ADC is perfect in all respects. Consequently, to mitigate their effects several calibration techniques have been proposed.

3.3 Offset and gain calibration methods

As discussed before, DC-offset and gain mismatch errors are additive and multiplicative errors respectively. Hence, with a prior knowledge of these mismatch quantities, it is easy to eliminate these errors simply by inverse scaling the signal and subtracting the estimated offset. It's easy to estimate the offset o_i in channel i by long-term averaging/chopping [9, 17, 18]. Likewise, the offset can also be estimated in foreground by applying known dc-inputs and then observing the analog input for which the digital output is driven to zero. This noted analog value is an estimate of the dc-offset. With an estimate of the dc-offset, it can be gotten rid of in a few ways. In one method, the digital estimate of the offset is simply subtracted out from the digital output $y_i[n]$ [16, 17]. Otherwise, with the analog estimate available, an equal offset with opposite sign is applied at the channel- i input to nullify its effect.

As for offset, several techniques have been proposed to counter the problem of gain-mismatch between channels. The main ideas stem from estimating the gain(s) of each channel and then digitally normalizing the output of each channel to a uniform gain, either through a negative feedback loop or in a feed-forward manner (for a foreground calibration mode) [18, 19].

Calibrating for phase mismatches (through timing or bandwidth mismatches) proves to be a much more tedious task, primarily because a simple scaling/subtraction operation does not suffice. Hence, not surprisingly, the bulk of the calibration literature addresses this issue. Calibration for phase mismatches (timing/bandwidth) is composed of two different techniques: estimation of the error and correction of the error. Typically, the former is done in the digital domain from the ADC output while the latter can be effected in both analog/digital domains.

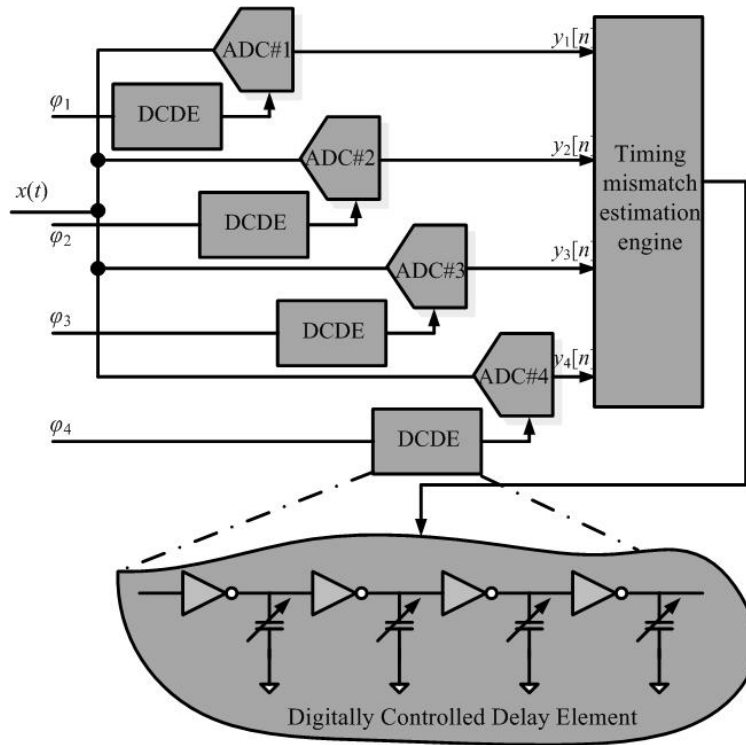


Figure 3.4: Analog correction of phase errors

3.4 Timing mismatch calibration in time-interleaved ADCs

3.4.1 Analog

The essence of analog correction techniques is shown in Figure 3.4. The timing-skews between the channels are estimated either through foreground means or background methods and then the sampling-clock edge for each channel is *shifted* to match with the correct edge. The physical shifting is implemented using any form of digitally controlled delay elements [5–7, 10, 14, 15, 25]. In fact, most of the published literature from the circuits community leverages this technique.

The correction by shifting the sampling clock is essentially the same in all the works of this kind, so we shall not delve into the individual details of each, but will instead look at a representative architecture for adjusting the sampling clock through a digitally-controlled delay buffer for

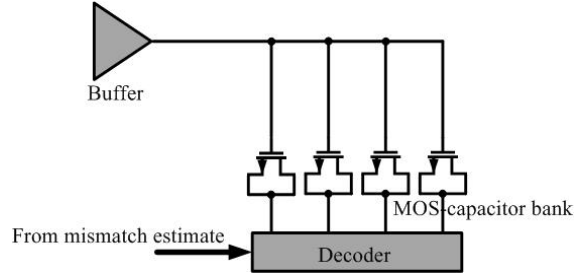


Figure 3.5: Representative digitally controlled delay element

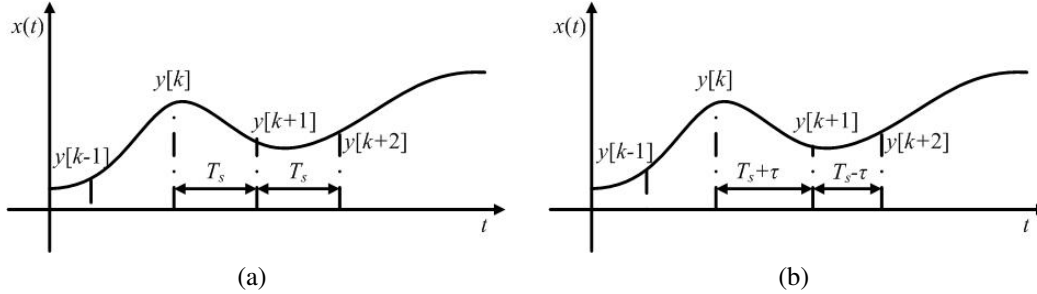


Figure 3.6: Correction principle in [10, 11, 15] (a) A two-channel output waveform without mismatch (b) A two-channel output waveform with mismatch

coarse/fine adjustment of the clock-phases, as shown in Figure 3.5. The digital codes for the clock adjustment are obtained through a timing mismatch estimation engine that may operate in the foreground/background. These codes typically tune a bank of capacitors which load the clock-driving buffer and hence vary the sampling edge of clock. However, there are considerable variations between the estimation techniques employed in these works and hence it is worth reviewing them.

Using time-averaged cross-correlation between signals from separate channels is a commonly used way to estimate the timing mismatch [6, 10, 14, 15, 25]. In [10, 15], cross-correlation between the consecutive channel outputs is exploited to estimate the timing-error. Let us take a look at Figure 3.6 for a two-channel system to understand this approach. Adjacent samples in a perfectly matched TIADC should be separated by T_s . However, for timing mismatches present, $y[k]$ and

$y[k + 1]$ will be separated in time by $T_s + \tau$ while $y[k + 1]$ and $y[k + 2]$ will be separated by $T_s - \tau$. Computing the long term cross-correlation between $y[k], y[k + 1]$ and between $y[k + 1], y[k + 2]$ and taking their difference gives a function that is directly proportional to τ . Based on this estimate of τ , the delay-line is programmed. However, this approach is beset with quite a few issues. The approach is not guaranteed to work for signals that are near dc or near F_s or for very wideband, almost white signals (since the auto-correlation of the signal vanishes at all points other than at 0). In [6], a different kind of cross-correlation is utilized to generate the mismatch estimate. An auxiliary channel also processes the input signal in parallel with the main ADC. The calibration proceeds in a per-channel manner. For a M -channel system, M different cross-correlations (with the auxiliary channel) are calculated. The cross-correlations should reach their maxima when there is absolutely no timing difference between the channels. The cross-correlator is embedded in a loop involving the sampling edge adjustment that equalizes the sampling instants between the main ADC channel and the auxiliary channel. It is of value to note that the auxiliary channel can be of much lower resolution than the main ADC. This technique is attractive, however it has been proven to work successfully to work for only a 5-bit system [6] and may be problematic for high-resolution systems.

In [5], for a two-channel system, a zero-crossing detector is used to count the average number of zero-crossings between the even and the odd samples. Nominally these two averages should be equal for a perfectly matched scenario. However, for a mismatched case when the input frequency is completely unrelated to the sampling frequency, the even and the odd zero crossings will show different averages as can be seen from Figure 3.7(a). The difference between these averages can be shown to be proportional to the timing mismatch. Thematically, this is similar to the work

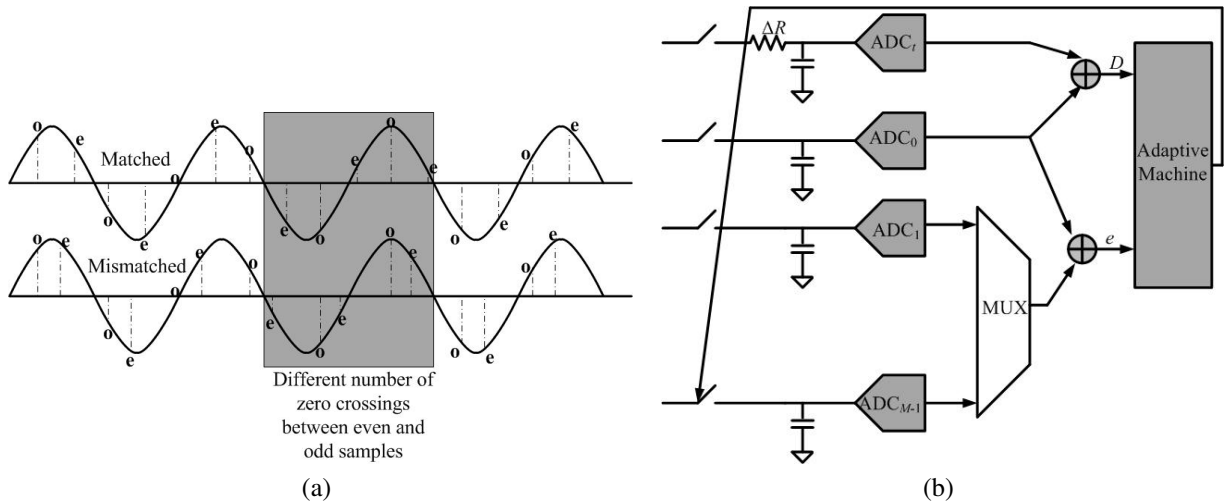


Figure 3.7: Correction principle (a) Zero crossing variation without and with mismatch [5] (b) Structure in [7]

in [10, 15]. However, this technique is also limited by the same drawbacks that plague [10, 15]. For input frequencies near dc or near Nyquist the technique would give erroneous mismatch estimates. Extending the argument, even for input frequencies that are rational sub-multiples of the clock frequency, this technique will not show any mismatch estimate. The authors in [7] estimate the timing mismatch in an adaptive loop as shown in Figure 3.7(b).

$$t_{i+1} = t_i + \mu D e \quad (3.5)$$

The timing updates in each iteration (i) are performed by an analog delay line as shown in Figure 3.5. D denotes the signal derivative since a timing mismatch between two nominally matched channels produces an error that is proportional to the derivative. The technique attempts to compute the derivative (D) in an analog fashion by taking the difference of two nominally matched channels where one channel has been intentionally tuned to have a lower bandwidth by incrementing the sampling resistance as shown in Figure 3.7(b). The update error (e) is obtained by computing the

difference between adjacent channel outputs (duly delayed by appropriate sample times).

Analog correction methods are however, plagued with problems of precise edge-matching that is based on the quantum of the digital-to-time converter step-size t_{step} in the delay-buffer of Figure 3.5 (which may be poorly controlled over process, voltage, temperature variations in a practical implementation) in the digitally controlled delay element and hence can limit the overall signal-to-noise ratio(SNR) for high performance systems. Furthermore, the preciseness of the sampling clock adjustment will be a direct function of the CMOS technology node and hence can limit the attainable dynamic range for a particular node unfavorably.

3.4.2 Digital

Digital techniques, on the other hand are mathematically more involved from a signal-processing standpoint. However, they are more robust, but seldom used by the circuits community. To appreciate the digital correction methods, an interesting interpretation of phase-mismatches is useful. Instead of assuming that the sampling clocks to the sub-ADCs are skewed, equivalently the incoming signals to the sub-ADCs can be thought to have similar delays in each channel. Consequently, the entire error can be expressed as a filter in the signal path, of the form

$$H_i(z) = z^{r_i} H_{BW,i}(z) \quad (3.6)$$

where $r_i T_s$ is the timing-skew of the i -th channel and $H_{BW,i}$ is the transfer-function of the i -th channel sample-and-hold filter. With this interpretation in mind, one can present a time-interleaved ADC architecture as a maximally decimated filter-bank [37] in Figure 3.8. Based on this model, let

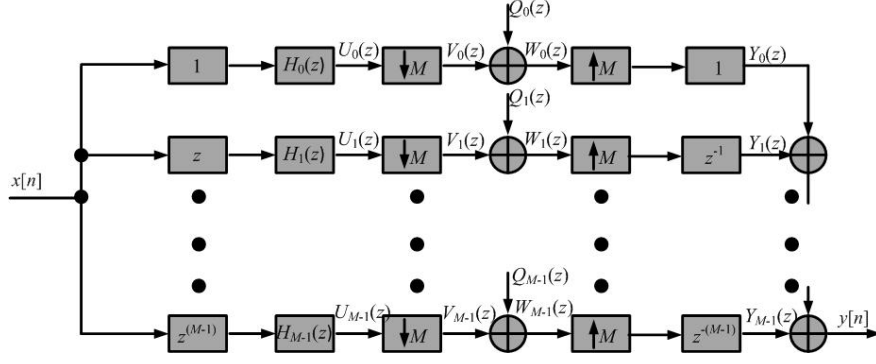


Figure 3.8: Filterbank model of time-interleaved ADC

us try to find the errors caused by phase-errors in time-interleaved ADCs. The evolution of signals across the filterbank structure can be expressed as below.

$$\begin{aligned}
 U_i(e^{j\omega}) &= \frac{1}{M} \sum_{k=0}^{M-1} X(e^{j(\omega - \frac{2k\pi}{M})}) e^{j(\omega - \frac{2k\pi}{M})i} H_i(e^{j(\omega - \frac{2k\pi}{M})}) \\
 V_i(e^{j\omega}) &= \frac{1}{M} \sum_{k=0}^{M-1} X(e^{j(\omega - \frac{2k\pi}{M})}) e^{j(\omega - \frac{2k\pi}{M})i} H_i(e^{j(\omega - \frac{2k\pi}{M})}) \\
 Y_i(e^{j\omega}) &= \frac{1}{M} \sum_{k=0}^{M-1} X(e^{j(\omega - \frac{2k\pi}{M})}) e^{-j\frac{2k\pi}{M}i} H_i(e^{j(\omega - \frac{2k\pi}{M})})
 \end{aligned} \tag{3.7}$$

Please note that (from Figure 3.8), $W_i(e^{j\omega})$ and hence $Y_i(e^{j\omega})$ will also consist of the quantization error $Q_i(e^{j\omega})$, but we have suppressed the term in Eqn. 3.7 and all subsequent analyses for simplicity without any compromise in the technical merit of the arguments.

Hence, the overall output $Y(e^{j\omega})$ can be expressed as

$$Y(e^{j\omega}) = \sum_{i=0}^{M-1} Y_i(e^{j\omega}) \tag{3.8}$$

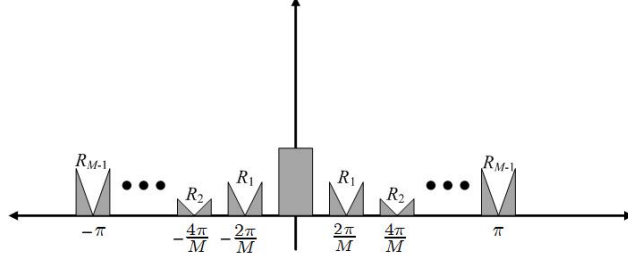


Figure 3.9: Representative output spectrum due to timing mismatch errors in a M -channel ADC

For simplicity of analysis, let us assume that the bandwidth on each channel is well-matched, hence Eqn. 3.6 reduces to

$$H_i(e^{j\omega}) = e^{j\omega r_i} \quad (3.9)$$

which can simplify Eqn. 3.7. Figure 3.9 plots a representative spectrum for a generic time-interleaved ADC with timing mismatch errors corresponding to Eqn. 3.7. Note the derivative-shaped errors at the sub-multiples of the sampling frequency. For alias-free reconstruction [37], these images must be eliminated. To that end, we can now introduce the two major classes of error calibrations.

3.4.2.1 Fractional delay filtering (FDF)

The structure in Figure 3.8 is modified to result in the structure in Figure 3.10, wherein an additional class of filters (synthesis filters in filter-bank parlance) are inserted to operate on $y_i[n]$. Let us also state (without a necessity proof) that for

$$F_i(e^{j\omega}) = a_i e^{-j\omega r_i} \quad (3.10)$$

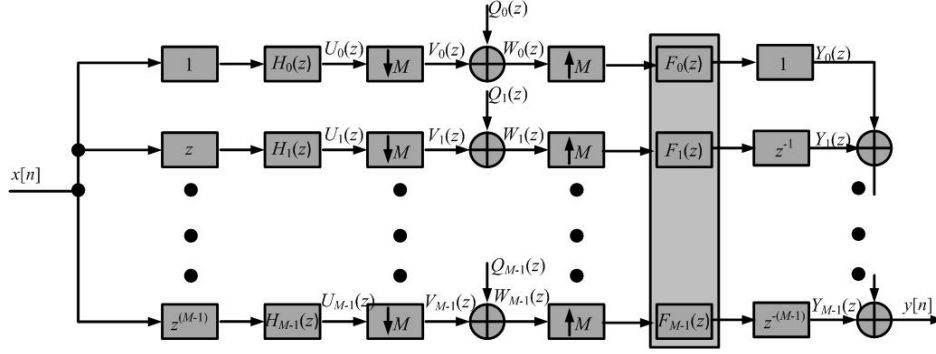


Figure 3.10: Fractional Delay Filter correction applied to filter-bank model of time-interleaved ADC

the overall output can be written as

$$Y(e^{j\omega}) = \frac{1}{M} \sum_{k=0}^{M-1} X(e^{j(\omega - \frac{2k\pi}{M})}) \sum_{i=0}^{M-1} a_i e^{-j\frac{2k\pi}{M}(i+r_i)} \quad (3.11)$$

Now, clearly, if one can ensure that,

$$\sum_{i=0}^{M-1} a_i e^{-j\frac{2k\pi}{M}(i+r_i)} = 0 \forall k \neq 0 \quad (3.12)$$

one can ensure perfect reconstruction of the ADC input. Such class of filters that satisfy the frequency response as in Eqn. 3.10 are called fractional-delay filters where the terminology is self-explanatory. Now if we write Eqn. 3.12 in a matrix form as in Eqn. 3.13, then it is not difficult to see that the coefficients a_i can be computed simply by solving Eqn. 3.13 once the mismatch quantities $r_i, i \in [0, M - 1]$ are known by some estimation technique.

However, such class of filters are non-trivial to build since the impulse response of a filter of

$$\begin{pmatrix} e^{-j\frac{2.0.\pi}{M}(0+r_0)} & e^{-j\frac{2.0.\pi}{M}(1+r_1)} & \dots & e^{-j\frac{2.0.\pi}{M}(M-1+r_{M-1})} \\ e^{-j\frac{2.1.\pi}{M}(0+r_0)} & e^{-j\frac{2.1.\pi}{M}(1+r_1)} & \dots & e^{-j\frac{2.1.\pi}{M}(M-1+r_{M-1})} \\ \vdots & \vdots & \ddots & \vdots \\ e^{-j\frac{2.M-1.\pi}{M}(0+r_0)} & e^{-j\frac{2.M-1.\pi}{M}(1+r_1)} & \dots & e^{-j\frac{2.M-1.\pi}{M}(M-1+r_{M-1})} \end{pmatrix} \times \begin{pmatrix} a_0 \\ a_1 \\ \vdots \\ a_{M-1} \end{pmatrix} = \begin{pmatrix} M \\ 0 \\ \vdots \\ 0 \end{pmatrix} \quad (3.13)$$

the form in Eqn. 3.10 can be written as

$$f_i[n] = -a_i \frac{\sin(\pi r_i)n}{(\pi r_i)n} \quad (3.14)$$

This is an infinite impulse response (IIR) filter and hence not feasible to build with constrained hardware. The problem becomes more complicated if the desired fractional delay (and a constant magnitude) is to be ensured over a very wide frequency range. It is of interest to note that a large amount of research effort has been expended on the design of fractional delay filters, out of which the most popular structure is the Farrow structure [29] shown in Figure 3.11. The input is passed through multiple FIR filters, the outputs of each being scaled by the desired delay and added with each other to result in the overall output as shown in Fig. 3.11.

To simplify the design of the filters in the context of time-interleaved ADCs, researchers take the liberty of oversampling the signal to some extent to ensure that there is a *don't care* band where the correction need not be applied. Applying a similar argument here, the synthesis filter structure in Figure 3.10 can be modified to result in Figure 3.12. Each fractional delay filter $F_i(z)$ has been decomposed into $F_i(z) = E_i(z)P(z)$ where $P(z)$ is a low-pass filter depending on the amount of oversampling. $E_i(z)$ is expected to provide the required fractional delay response until the passband ω_p , after which its response is not quite important since it will be filtered out

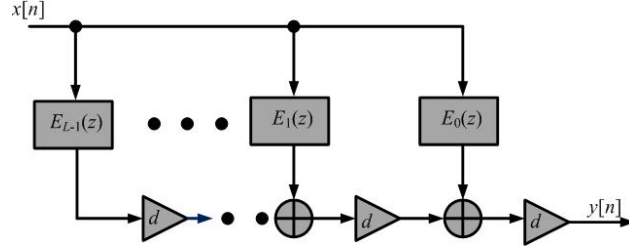


Figure 3.11: Farrow structure to realize fractional delay

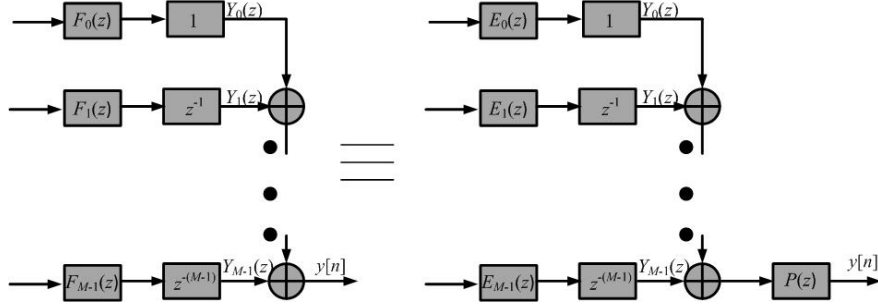


Figure 3.12: Modification of synthesis filters for easy realization in [26]

by $P(z)$. This assumption simplifies the design of the FDF to a great extent and is resorted to in several works. As mentioned before, such kind of an approach may not always be admissible for blind calibrations where the mismatch quantities are unknown.

Researchers in [27] propose modifying the structure of the fractional delay filter that admits an adaptive estimation of the mismatch quantity for a two-channel system and extends the argument for a four-channel one in [28]. Intuitively, the approach can be explained as follows. For a two-channel system, the sub-band output of each sub-ADC consists of the desired signal and the image component, based on the model in Figure 3.8 as shown in Eqn. 3.15.

$$\begin{aligned}
 Y_0(e^{j\omega}) &= \frac{1}{2}[X(e^{j\omega/2}) + X(e^{j(\omega/2-\pi)})] \\
 Y_1(e^{j\omega}) &= \frac{1}{2}[X(e^{j\omega/2})e^{j\omega/2(1+r_1)} + X(e^{j(\omega/2-\pi)})e^{j(\omega/2-\pi)(1+r_1)}]
 \end{aligned} \tag{3.15}$$

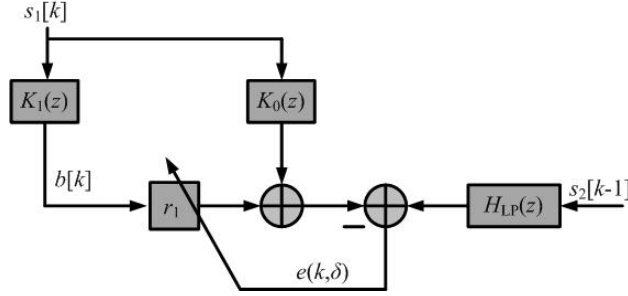


Figure 3.13: Estimation structure in [27]

Ignoring quantization error, the outputs of the sub-ADCs can be low-pass filtered to result only in the signal component (no alias component). The signal components so obtained can now be compared with each other by delaying one channel output by the quantity $\frac{1+r_1}{2}$ through an adaptive algorithm. The comparison is deemed perfect when the delay r_1 is accurately estimated. The estimation structure is shown in Figure 3.13 that implements the fractional-delay filter (of delay $\frac{1+r_1}{2}$) in the popular Farrow structure [29]. The Farrow structure allows an elegant adaptation of the mismatch delay r_1 as shown in Figure 3.13. The low-pass filter $H_{LP}(e^{j\omega})$ is subsumed in the delay filter. In other words, the filter $K(e^{j\omega})$ implements the transfer function,

$$\begin{aligned}
 K(e^{j\omega}) &= K_0(e^{j\omega}) + r_1 K_1(e^{j\omega}) \\
 &= e^{-j\omega/2(1+r_1)} |_{|\omega| \leq \omega_0}
 \end{aligned} \tag{3.16}$$

where ω_0 is the corner of $H_{LP}(e^{j\omega})$. The low-pass criterion on the filter $K(e^{j\omega})$ serves two purposes. Firstly, it enables an easy comparison of the signal outputs, without the alias components, for facile adaptation. Secondly, over a smaller bandwidth ($\leq \omega_0$) the design of the fractional delay filter now becomes easier as argued before. However, even though the blind estimation of the mismatch delay is attractive in them, [27] and [28] resort to expensive full-band fractional delay filters

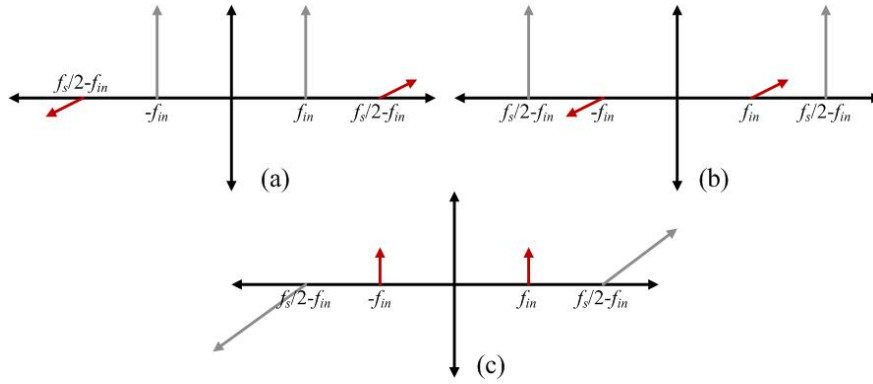


Figure 3.14: Principle of mismatch estimation in [13] (a) Output spectrum (b) Output spectrum chopped by $(-1)^n$ (c) Output spectrum chopped by $(-1)^n$ and Hilbert transformed

to effect the correction based on [26] and some simplifications.

In [9], [12] and [13], the authors implement fractional delay filters for correcting time-interleaving errors for two-channel and four-channel cases. They resort to a foreground estimation of the mismatch quantities and then feed the obtained estimate to a fractional-delay filter to effect the correction. The basic principle of the mismatch estimation can be understood upon inspection of Figure 3.14. For an input frequency of f_{in} , the image due to the mismatch forms at $\pm(F_s/2 - f_{in})$. The image strength is dependent on the mismatch amount. The ADC output is multiplied with a sequence $(-1)^n$ that results in the spectrum shown in Fig. 3.14(b) (brings the image in the signal location and vice-versa). Now, upon passing this chopped signal through a Hilbert transformer, the image comes in the real plane while the signal goes to the orthogonal plane as shown in Fig. 3.14(c). Now, clearly upon multiplying the signals shown in Figs. 3.14(a) and (c), the dc term will bear information about the timing mismatch amount. This is a simple approach to estimate the delay with high accuracies and then apply the same to the fractional-delay filter through a look-up table or direct on-chip computation of the filter coefficients. However, this approach is beset with problems with certain pathological frequencies where this scheme will fail. For instance, for a

$f_{in} = F_s/4$, the image and signal are at the same location flagging an erroneous timing mismatch value. In such cases, the authors in [9, 13] have resorted to notching out such frequencies with custom filters viz. $(1 + z^{-2})$. Furthermore, the technique will need significantly large amount of hardware with increasing number of channels.

3.4.2.2 Direct Alias Cancelation (DAC)

This technique is an approximation on the fractional delay filter and often allows a much lower complexity than FDFs without a large penalty in accuracy [31–34]. In an intuitive way, the technique can be understood as shown in Figure 3.15. A reference path separates out a part of the alias-error component using a filter $F(z)$ (the top path in Figure 3.15) while the bottom path attempts to emulate this out-of-band error using some signal processing that involves estimating the timing-mismatch parameters correctly. The estimation is done in an adaptive manner. Mathematically, the technique can be understood by invoking Eqns. 3.6, 3.7 and expanding $e^{j\omega r_i}$ in a Taylor-series (after some simplification)

$$Y(e^{j\omega}) \simeq X(e^{j\omega}) + \frac{1}{M} \sum_{k=1}^{M-1} X(e^{j(\omega - \frac{2k\pi}{M})}) j(\omega - \frac{2k\pi}{M}) R_k \quad (3.17)$$

where

$$R_k = \sum_{l=0}^{M-1} r_l e^{-j \frac{2k\pi}{M} l}$$

Inspecting Eqn. 3.17, it is clear, that the first term denotes the perfectly reconstructed output while the second term denotes the error $E(e^{j\omega})$. Now, one can re-write Eqn. 3.17 in the sample domain as

$$\begin{aligned} y[n] &= x[n] + e[n] \\ &= x[n] + \frac{1}{M} \sum_{k=1}^{M-1} R_k x[n] * h_d[n] e^{j\frac{2k\pi}{M}n} \end{aligned} \quad (3.18)$$

where $h_d[n]$ is an ideal differentiator operation having frequency response

$$H_d(e^{j\omega}) = j\omega, \quad -\pi < \omega < \pi \quad (3.19)$$

The calibration can now be explained as follows. From Eqns. 3.17 and 3.18, the error-term has some spectral content out of the input signal band. Consequently, an error-separation filter $F(z)$ gets rid of the signal to generate a part of the error term $e[n]$ (the signal band also contains folded error terms). An auxiliary path attempts to emulate this error by adaptively finding the coefficients R_k in Eqn. 3.17. as shown in Figure 3.16. $m[n]$ represents the modulation vector $e^{j\frac{2k\pi}{M}n}$. Hence, if one can build a good approximation to $h_d[n]$, this is an elegant way to estimate and hence cancel the timing mismatch components. A simple example for a two-channel scenario can be explored further for greater insight and potential reduction of hardware for a more power-efficient structure. Upon inserting $M = 2$ in Eqn. 3.18, we find that the overall output can be written as

$$y[n] = x[n] + \frac{1}{2}x[n] * h_d[n] \times (-1)^n \times (r_0 - r_1) \quad (3.20)$$

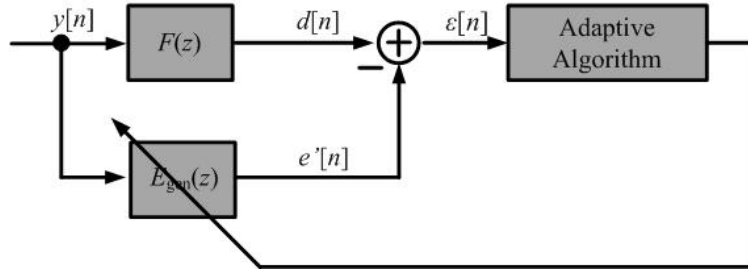


Figure 3.15: Direct alias cancellation structure: general

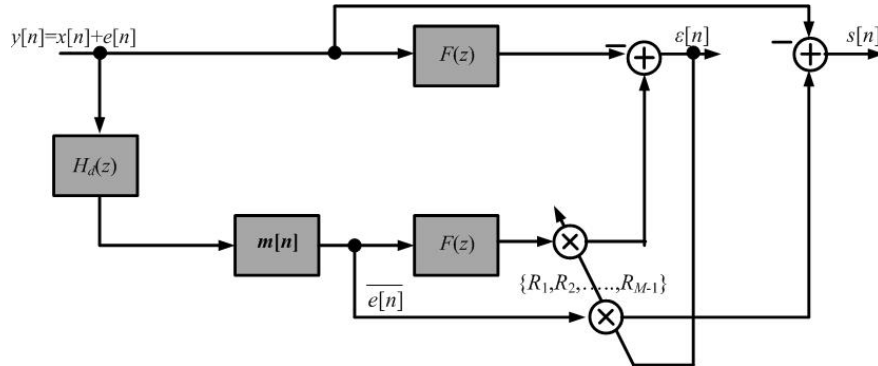


Figure 3.16: Direct alias cancellation structure: in [32]

The corresponding correction structure is shown in Figure 3.17 which is simply a 2-channel version of Figure 3.16. However, note that the term $(-1)^n$ representing the modulation vector $m[n]$ in Figure 3.16 is simply the second row of 2×2 Hadamard matrix [34] or for that matter a DFT matrix [37]. This idea is extended for higher number of channels as well where the modulation vector translates to non-unity rows of the $M \times M$ Hadamard matrix for a M -channel ADC with suitable weights for R_k from Eqn. 3.18. This observation was made in [34] that considerably relaxes the hardware requirement since a multiplication by ± 1 is a lot less hardware intensive than a full-blown floating point multiplication.

In a slight variant, instead of approximating Eqn. 3.9 as a first-order Taylor series expansion, [31] allows a higher-order expansion. This is a closer approximation to the fractional-delay and is reminiscent of the Farrow-structure as shown in Figure 3.11.

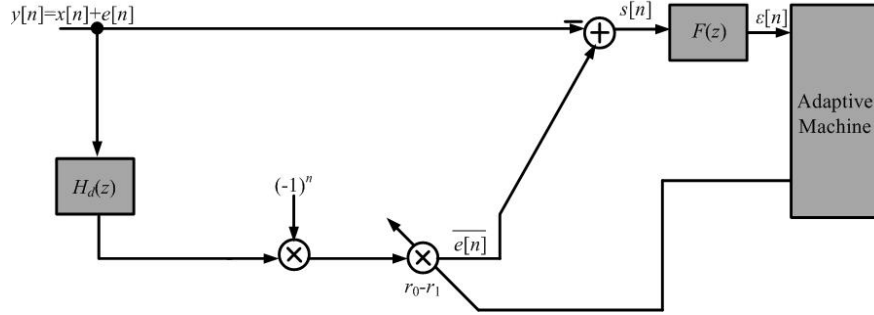


Figure 3.17: Direct alias cancellation applied to a 2-channel case to show modulation being realized through Hadamard transform [34]

3.5 Bandwidth Mismatch Calibration

As mentioned in Section 3.2, bandwidth mismatch effects are gaining prominence with higher bandwidth operations. However the techniques employed to tackle its effects are not as evolved as the timing mismatch case. In fact, the published literature resorts to techniques that are slight modifications of the structures used for timing mismatch calibration.

The circuits community typically resorts to "*careful*" layout techniques to alleviate the mismatch effect and also modulates the supply of the sampling switch to equalize the bandwidths across the channels [35, 36]. While this may be effective for the reported art, but at the end of the day, it remains an ad-hoc approach and defeats the virtues gained from digital corrections. The signal-processing community, on the other hand, expresses the first-order pole filter as a polynomial in frequency as

$$H(e^{j\omega}) = \sum_{p=0}^{p=P-1} c_p(j\omega)^p \quad (3.21)$$

Such an expression allows the invocation of direct alias cancellation since by obtaining the esti-

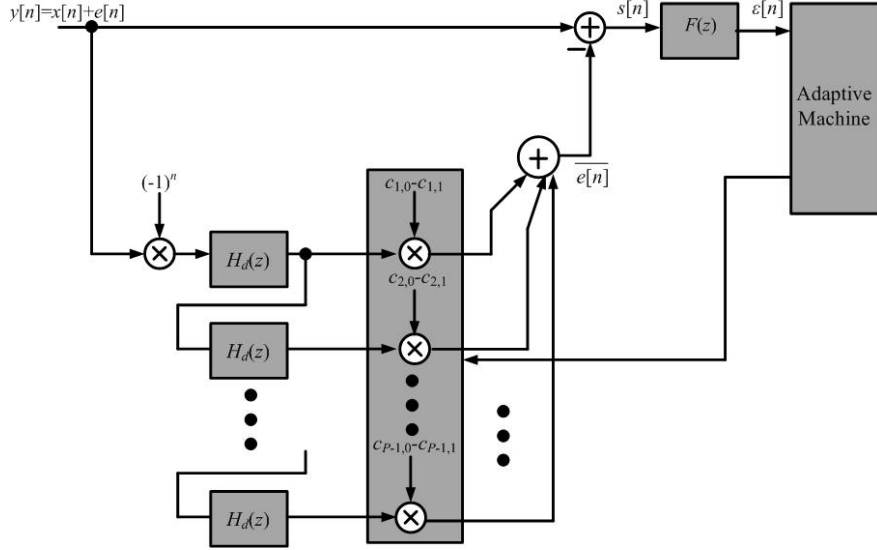


Figure 3.18: Bandwidth mismatch calibration in [23] and [24] using polynomial expansion

mates c_p for each channel, the bandwidth mismatch error can be estimated and hence subtracted from the original output. In [21], the polynomial coefficients c_p are assumed to be known which allows the authors to build multiple differentiator filters (up to order $P - 1$) and multiply with the c_p to estimate the error value that is eventually subtracted from the overall output. In [24], the coefficients c_p are approximated blindly as can be seen below. To further see it, Eqn. 3.17 can be re-written as

$$E(e^{j\omega}) = \frac{1}{M} \sum_{k=1}^{M-1} X(e^{j(\omega - \frac{2k\pi}{M})}) e^{-j\frac{2k\pi}{M}i} H_i(e^{j(\omega - \frac{2k\pi}{M})}) \quad (3.22)$$

Substituting Eqn. 3.21 in Eqn. 3.22, the error $E(e^{j\omega})$ can be written as,

$$\begin{aligned}
E(e^{j\omega}) &= \frac{1}{M} \sum_{k=1}^{M-1} X(e^{j(\omega - \frac{2k\pi}{M})}) \sum_{i=0}^{M-1} e^{-j\frac{2k\pi}{M}i} \sum_{p=0}^{P-1} c_{p,i} (j(\omega - \frac{2k\pi}{M}))^p \\
&= \frac{1}{M} \sum_{k=1}^{M-1} X(e^{j(\omega - \frac{2k\pi}{M})}) \sum_{p=0}^{P-1} (j(\omega - \frac{2k\pi}{M}))^p \sum_{i=0}^{M-1} c_{p,i} e^{-j\frac{2k\pi}{M}i} \\
&= \frac{1}{M} \sum_{k=1}^{M-1} X(e^{j(\omega - \frac{2k\pi}{M})}) \sum_{p=0}^{P-1} C_{p,k} (j(\omega - \frac{2k\pi}{M}))^p
\end{aligned} \tag{3.23}$$

where

$$C_{p,k} = \sum_{i=0}^{M-1} c_{p,i} e^{-j\frac{2k\pi}{M}i}$$

In the sample-domain, the error-term can hence be written as in Eqn. 3.24.

The mismatch coefficients are estimated by comparing the error in a mismatch band using a filter $f[n]$ admitting a structure as shown in Figure 3.18. As can be seen, this is a very similar structure as Figure 3.16. In [23] and [24], this structure has been simulated for a 2-channel scenario with good results. However, this can become computationally expensive for a larger number of channels. In [20], a test signal is injected near the Nyquist band-edge and a structure similar to Figure 3.13 is used to estimate the relative time-constant mismatch between 2 channels. The obtained estimate is subsequently used in an IIR-FIR cascade to correct for the mismatch errors. This is a highly computationally intensive procedure as well with significant amount of hardware required for the two-channels only.

$$e[n] = \frac{1}{M} \sum_{k=1}^{M-1} x[n] * (C_{0,k} + C_{1,k}h_d[n] + C_{2,k}h_d[n] * h_d[n] + \dots + C_{P-1,k}h_d[n] * \dots (P - 1\text{times})h_d[n])e^{j\frac{2k\pi}{M}n} \quad (3.24)$$

3.6 Conclusion

This chapter reviewed multiple analog and digital intensive techniques to correct for timing and bandwidth mismatches in time-interleaved ADCs. It attempted to bring out the pros and cons in most of these techniques and provided a detailed platform for prior-art in this field that will help develop a signal-dependent adaptive algorithm to treat mismatch errors in the following chapter. The proposed structure will enable the building of a system with a much lower complexity compared to prior-art as shown in the following chapter.

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CHAPTER 4

Phase Mismatches in Time-Interleaved ADCs: Adaptive signal-dependent digital solution to an analog problem

4.1 Introduction

We have conducted a detailed study of the prior-art to mitigate the effects of phase mismatch errors in time-interleaved ADCs in the previous chapter. We identified their respective merits and demerits. With these in light, we propose a technique to calibrate phase-mismatch errors (both from timing and bandwidth mismatch) that develops an *inherent intelligence* to choose a calibration structure which is efficient. We shall not re-introduce the model and notations that we had uniformly used in Chapter-3, but will assume familiarity from the reader.

4.2 Proposed technique

4.2.1 Architecture

The technique has been introduced in [1] and slightly modified in [2]. The work in [1] will be elaborated further here and thoroughly analyzed. The technique can be best understood with an

inspection of Figure 4.1. Along with the M usual ADCs, there is an additional identical ADC which has been termed the calibration ADC or ADCc. The purpose of ADCc is to correct for errors from individual channels in a round-robin manner based on the correction algorithm i.e. the ADCc cycles through each channel calibrating it before moving to the next channel and continues in a circular manner in the background operating throughout the ADC operation. Nominally, when ADCc is calibrating ADC- i , $y_c[n] = y_i[n]$. Disagreements between $y_c[n]$ and $y_i[n]$ are equalized through the correction algorithm in an adaptive manner. Hence, all mismatches are referenced to ADCc, or in other words, ADCc is assumed to be the error-less ADC. Once all the ADC's are matched to ADCc, the system is calibrated to all mismatch errors. The calibrated channel outputs $y_{ic}[n], i = 1, 2, \dots, M$ are subsequently combined.

4.2.2 Signal processing

The signal processing aspect of the technique is highlighted in Figure 4.2. Based on the calibration of ADC- i , the filter $F_i(e^{j\omega})$ generates the error-signal across the ADC sub-band $[-\pi/M, \pi/M]$ in an adaptive manner (in the case of perfect adaptation, the entire error is captured). From Figure 4.1 and 4.2, since we are trying to minimize the discrepancy between Y_i and Y_c , consequently in steady-state, the *synthesis* filter for the i -th channel can be written as,

$$\begin{aligned}
 F_i(e^{j\omega}) &= \frac{Y_i(e^{j\omega}) - Y_c(e^{j\omega})}{Y_i(e^{j\omega})} \\
 &= \frac{\sum_{k=0}^{M-1} X(e^{j\frac{\omega-2\pi k}{M}}) [e^{j(\frac{\omega-2\pi k}{M})n_i} - 1] e^{j\frac{\omega-2\pi k}{M}i}}{\sum_{k=0}^{M-1} X(e^{j\frac{\omega-2\pi k}{M}}) e^{j\frac{\omega-2\pi k}{M}i}}
 \end{aligned} \tag{4.1}$$

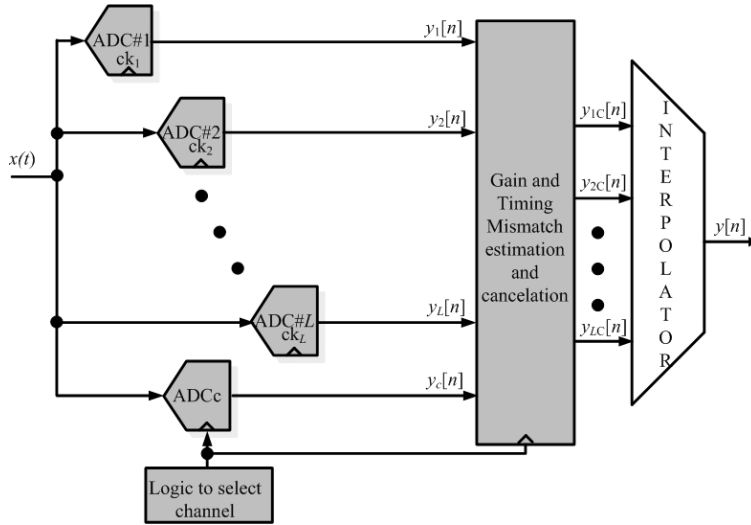


Figure 4.1: Proposed architecture: top

From Eqn 4.1, it is clear that this is a signal dependent filter, and this is what we shall see in the latter sections enable us to build a much lower complexity filter compared to prior-art [3–8]. Figure 4.3 illustrates the operation of the algorithm from a signal perspective in a sub-band. The alias component can be completely out-of-band or in-band depending on the signal occupancy of the available spectrum. It is interesting to note that in the proposed architecture, the calibration channel is being utilized to separate out the error generated in its entirety and then the filter $f_i[n]$ helps emulate this error as much as possible. This is analogous to the direct alias cancellation error estimation where $f[n]$ (Figs. 8 and 9) separates out the error only at out-of-band locations and hence imposes restrictions on having prior knowledge about the signal spectral content. Furthermore, in this work, since the error is being estimated at the sub-band level, consequently no modulation etc. need to be invoked [6] (Figure 3.16). It may be noted that even with bandwidth mismatches, where $H_i(e^{j\omega}) = e^{j\omega r_i} H_{BW,i}(e^{j\omega})$, the proposed technique would operate perfectly fine for it does not attempt to estimate the mismatch parameters [3, 4] but estimates the error (alias) component as a

whole. For completeness, for a generic $H_i(e^{j\omega})$, the synthesis filter for the i -th channel is

$$F_i(e^{j\omega}) = \frac{\sum_{k=0}^{M-1} X(e^{j\frac{\omega-2\pi k}{M}}) [H_i(e^{j\frac{\omega-2\pi k}{M}}) - 1] e^{j\frac{\omega-2\pi k}{M} i}}{\sum_{k=0}^{M-1} X(e^{j\frac{\omega-2\pi k}{M}}) e^{j\frac{\omega-2\pi k}{M} i}} \quad (4.2)$$

An interesting point to note is that in traditional approaches [3–5, 9], the calibration hardware complexity is invariant of the applied signal and hence is the same for a dc signal or a 15-dB peak-to-average ratio (PAR) orthogonal frequency division multiplexing (OFDM) signal. The only adaptation that these techniques [3–5, 9] employ is to estimate the timing-skew based on a fixed FIR filter (for the differentiator). In contrast, the proposed technique can be adapted to the desired complexity based on the signal.

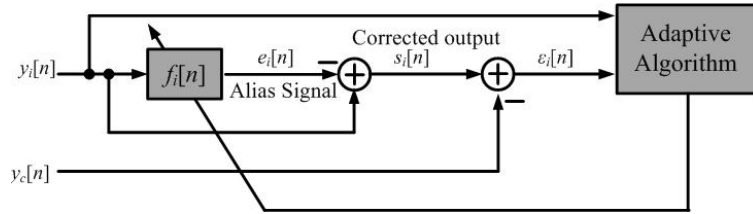


Figure 4.2: Proposed architecture: sub-band

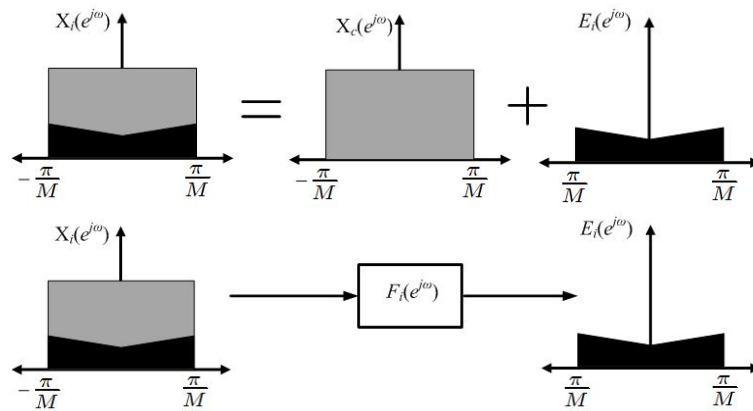


Figure 4.3: Proposed architecture: signal processing

For further intuition, we can see that for narrow-band signals, the error terms have minimal

in-band signal content [6]. Thus, the adapted filter response need not provide a differentiator-like transfer function at all frequencies, but only at frequencies, which are out-of-the-signal-band-of-interest. This is where the main theme of the technique lies. In steady-state, on convergence of the adaptation loop, the filter *de-emphasizes* the input signal or in other words, the correction is not applied at frequencies where there is significant signal content. This enables the filter to be designed with a much lower number of taps than compared to standard perfect reconstruction techniques [10, 12]. However, as noted earlier, for a richer sub-band signal content, the technique will need higher number of taps.

4.2.3 Calibration algorithm details

The algorithm is described in the following flow-chart:

Algorithm 1 Calibrate Time-interleaved ADC

$$\hat{o}_c = \frac{1}{M} \sum_{j=0}^{M-1} y_c[j], M \text{ is the averaging-length}$$

$$z_c[n] = y_c[n] - \hat{o}_c$$

while ADC ON **do**

for $i = 1; i < L + 1; i = i + 1$ **do**

$$\hat{o}_i = \frac{1}{M} \sum_{j=0}^{M-1} y_i[j]$$

$$z_i[n] = y_i[n] - \hat{o}_i$$

$$\mathbb{C}_i(z_i, z_c)$$

if $i = L$ **then**

$$i = 1$$

end if

end for

end while

(\mathbb{C}_i is the correction algorithm for the i -th channel). The calibration algorithm rids the channel outputs of the respective offsets (by averaging the outputs and subtracting the estimated offset)¹

¹It is assumed that the incoming signal $x(t)$ is zero-mean. A finite dc offset in the signal will also follow a similar algorithm with some minor modifications, which do not distract from the description of \mathbb{C}_i

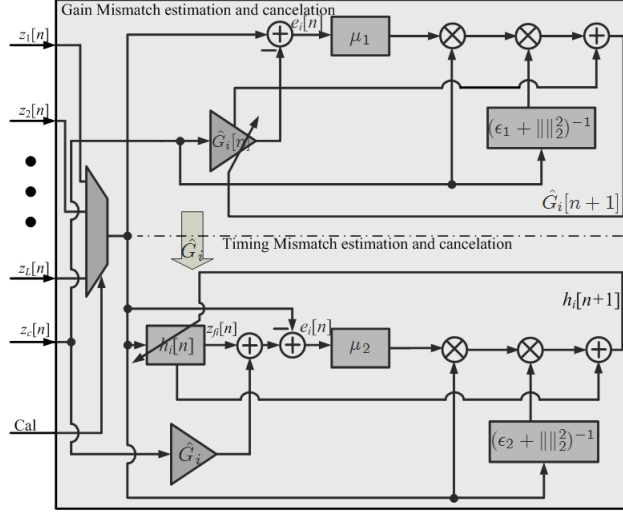


Figure 4.4: Proposed architecture: Correction Algorithm

and applies the correction algorithm between the new channel outputs z_i and z_c . Henceforth, in all discussions, the output of ADC_i will be assumed to be $y_i[n]$ that is indistinguishable from $z_i[n]$ (in other words, the system is assumed to be free of all offset errors). Let us now explain the actual algorithm ($\mathbb{C}_i(y_i, y_c)$) in detail.

In the presence of sampling mismatches τ_i and gain mismatches between channels G_i , the output of the i -th channel can be expressed as:

$$y_i[n] = G_i x(t + \tau_i)|_{t=(n-1)MT_s+(i+1)T_s} \quad (4.3)$$

Now, Eqn. 4.3 can be recast as (after Taylor series expansion)

$$z_i[n] = G_i(x(t) + \tau_i x'(t) + \frac{\tau_i^2}{2} x''(t) + \dots)|_{t=(n-1)MT_s+(i+1)T_s} \quad (4.4)$$

It hence suffices to cancel the error terms viz. $\tau_i x'(t), \frac{\tau_i^2}{2} x''(t), \dots$ etc. sampled at the appro-

appropriate times to effect an appropriate calibration. The correction algorithm is illustrated in Figure 4.4 (the gain and timing mismatch estimation and cancelation block of Figure 4.4). The following operations are performed on the available outputs

$$e_{1i}[n] = y_i[n] - \hat{G}_i[n]y_c[n] \quad (4.5)$$

$$\hat{G}_i[n+1] = \hat{G}_i[n] + \frac{\mu_1}{\epsilon_1 + y_c^2[n]} e_{1i}[n]y_c[n] \quad (4.6)$$

Eqns. 4.5, 4.6 represent a normalized least-mean square (NLMS) algorithm [13] for calibrating the inter-channel gain error. Once the NLMS (the upper half of the correction algorithm in Figure 4.4) converges, the gain estimate \hat{G}_i (of G_i) is used for the next step

$$e_{2i}[n] = y_i[n] - \hat{G}_i y_c[n] - h_i^T[n]\bar{y}_i[n] \quad (4.7)$$

$$h_i[n+1] = h_i[n] + \frac{\mu_2}{\epsilon_2 + \|\bar{y}_i[n]\|_2^2} e_{2i}[n]\bar{y}_i[n] \quad (4.8)$$

where $h_i[n] = [h_{i,(K-1)}[n], h_{i,(K-2)}[n], \dots, h_{i,0}[n]]^T$ (the correction filter coefficients) and $\bar{y}_i[n] = [y_i[n], y_i[n-1], \dots, y_i[n-K+1]]^T$, K being the correction filter-length (the lower half of the correction algorithm in Figure 4.4). $\mu_{1,2}, \epsilon_{1,2}$ are standard parameters for NLMS [13].

On convergence of the above algorithm, the filtered output $y_{fi}[n] = h_i^T[n]\bar{y}_i[n]$ denotes all pertinent error terms for the i -th channel with respect to the calibration channel. It should be noted that this is the error of the sub-band(i) system. Mathematically, in steady-state convergence,

$$y_{fi}[n] = G_i(\tau_i x'(t) + \frac{\tau_i^2}{2} x''(t) + \dots)|_{t=(n-1)MT_s+(i+1)T_s} \quad (4.9)$$

A point of caveat should however be noted here. Since the adaptation filter is signal-characteristic dependent, so for a sudden change in the signal (within the bandwidth of interest), the tracking time of the filter should be within the signal bandwidth. The simulation results presented in the next section confirm that an effective design of the filter ensures that.

4.3 Simulation Results, Implementation Details and Practical Considerations

Behavioral simulations with the proposed technique have been performed using four interleaved channels and one calibration channel. The ADC's in each channel are chosen to be of 10-bit dynamic range. A sinusoidal input at a normalized frequency of 0.0078 is applied. A 10% random timing, gain and bandwidth mismatch between the channels has been assumed (based on the discussion in the previous section, presence/absence of offset mismatches does not interfere with the core of the technique). A filter-length of 6 has been chosen for the simulations shown in Figs. 14(a),(b). This marks a great reduction in the overall hardware complexity [3, 6, 9]. Figure 4.5(a) shows the improvement the technique enables (to the tune of about 55dB in the achievable SFDR). Figure 4.5(b) shows the adapted filter magnitude response. As can be seen from the figure, the adapted filter magnitude response shows no correction at the desired frequency (spectral null)

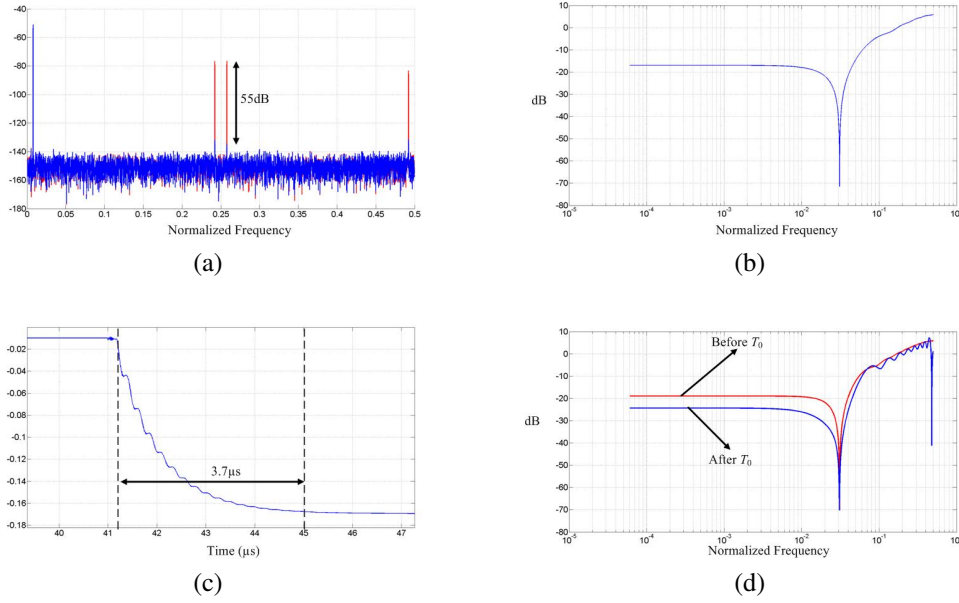


Figure 4.5: Simulation results for the proposed technique (a) Performance of the system with mismatches with and without the calibration (b) Filter magnitude response for the second channel (c) Adaptation time for $h_{4,20}$ for an input as in Eqn. 4.10 (d) Filter magnitude response(s) for inputs as in Eqn. 4.10

while the out-of-band frequencies have the required corrective response.

Figure 4.5(c) illustrates the adaptive tracking for a changing signal scenario. As discussed in Section 4.2, since the correction filter is signal dependent there may be a concern towards the tracking time of the system for a fast transition of the input signal. For this simulation an FIR filter of order 21 is chosen². Figure 4.5(c) illustrates the tracking time of the last tap of the filter in the fourth channel for a step-transition of the input as:

$$x(t) = A \sin(\omega_0 t) + A \sin(\omega_1 t)u(t - T_0) \quad (4.10)$$

²a lower filter-order ≈ 6 would also have converged, but would have taken a longer time for the same convergence parameters. A different set of adaptation parameters or a more sophisticated LMS algorithm(RLS, CMA2-2 etc. [13]) would be required for a faster convergence with a lower filter-order(not shown here for brevity)

for $\omega_0 = 2\pi 0.0078F_s$, $\omega_1 = 2\pi 0.4F_s$. T_0 has been chosen to be $18.2\mu s$. The tracking time is found to be about $3.5\mu s$, which is comparable to standard ADC calibration times [3]. The magnitude responses of the two filters before and after the signal transition step is applied is shown in Figure 4.5(d). Note the adaptive change in the filter before and after T_0 (the additional null at 0.4). We now study the various aspects of the technique's performance with respect to different design parameters.

4.3.1 Signals

The proposed technique is not limited to narrow-band signals but can handle signals of different types. The technique does not impose any particular condition on the operable signal class, since it does not rely on any sort of parameter estimation ([3, 4, 9]) that may be a function of the applied signal. However, it should be borne in mind that for very rich signals in the ADC sub-band $((k-1)\pi/M, k\pi/M)$, the complexity of the filter approaches that of a conventional fractional delay filter in the limit and the benefits obtained from the dependency on the signal characteristics will be less obvious. Figure 4.6(a-d) present some simulation results for different classes of signals that are passed through a 4-way interleaved ADC before and after the technique is applied. The inputs are chosen to be concentrated richly in a single Nyquist zone. Clearly, all of them are able to reclaim most of the lost SNDR that is sufficient for most applications. Furthermore, Figure 4.6(e) demonstrates the efficacy of the technique for inputs spanning different Nyquist zones, wherein also the output spectrum is reclaimed in its most entirety. The filters chosen for this simulation are all of 16 taps.

Parameter	[11]	[6]	[8]	This work
Type of correction	FDF	DAC	DAC	Adaptive DAC
LUT	3	0	0	0
No. multipliers	61x4x4+21x3	33x4 + 6x4+16x4x2	31x4 + 6x4	16x4
No. adders	60x4x4+20x3	32x4+32x4x2	30x4 + 2x4	15x4
Extra channel	0	0	0	P_{AmW}
Total	$1039P + 1020S$	$284P + 384S$	$148P + 128S$	$64P + 63S + P_A$

Table 4.1: Comparison with state-of-the-art

4.3.2 Channels

As can be seen from Figure 4.7(a), the technique ensures an almost constant SFDR irrespective of the number of channels (there is a slight degradation), hence promising a really wideband system (for higher number of channels) with the applied input being the same as in Figure 4.5(a-b). Also, the power-efficiency of the system actually improves with increasing number of channels. This can be explained since for a single ADC of bandwidth B , having a nominal power consumption of P_0 with a resolution of m bits, the figure-of-merit of the M -way time-interleaved system is [14]

$$\begin{aligned}
\text{FoM} &= \frac{(M+1)P_0}{2MB2^m} \\
&= \left(1 + \frac{1}{M}\right) \frac{P_0}{2^{m+1}B}
\end{aligned} \tag{4.11}$$

Hence, with increasing M , the FoM improves.

4.3.3 Taps

We apply the same input as before (Figure 4.5(a)) and observe the effect of the number of taps in the FIR filter both on the achievable SNDR and the adaptation time of the filter. Figure 4.7(b)

plots the overall ADC SFDR as a function of the number of the filter taps. For increasingly rich signals, having more number of taps helps to distinguish their features more accurately and hence for the example chosen in Figure 4.7(b), an improving trend is observed with the filter length. However, the trend levels off after a certain value. For the presented example, the optimal number of filter taps appears to be 14. In an actual implementation the number of filter taps will be made programmable depending on the desired accuracy of the filter and the class of signals expected to be processed.

The number of taps however has a more profound effect on the adaptation time of the filter. We apply a signal input of the form as in Eqn. 4.10 where $\omega_0 = 2\pi 0.0078F_s$, $\omega_1 = 2\pi 0.4F_s$. We observe the adaptation time of the filter as a function of the number of filter-taps, as shown in Figure 4.7(c). The adaptation time [13] is a direct function of the filter taps and hence can be chosen depending on the settling time dictated by the standard.

4.3.4 Bits

An input signal similar to Figure 4.5(a) is applied and the achievable SFDR is observed as a function of the resolution of the filter coefficients. The same 6-tap filter is used for adaptation, however with different bit-lengths. As expected, the SFDR degrades quite sharply for bit lengths lower than 10 (the dynamic range of the ADC). However, for bit lengths exceeding 10 bits, the ADC system is more than adequate to accommodate the signal dynamic range. Based on Figure 4.7(d), an optimal number for the coefficient bit-width is 11 – 12.

4.3.5 Comparing with state-of-the-art

For a similar output rate, the proposed technique is compared in terms of hardware expense with a few techniques proposed recently in the lines of prior-art discussed in Chapter 3 in Table-1 for a 4-way interleaved system with each channel operating at 250MS/s. Here P denotes the power consumption of a 10 bit by 12 bit multiplier and S denotes the sum of two 12-bit numbers operating at 250MS/s. The ADC power P_A quoted in the last column of Table 1 is about 5.12mW based on recently published data [14] for Nyquist data-converters in the 250MS/s, 10-bit operating regime. As can be appreciated from Table-1, the proposed technique, due to its signal dependence property, has the minimum hardware requirement of all that augurs well for many communication scenarios.

4.4 Conclusion

This work presents an adaptive digital signal conditioning based technique for mitigating timing mismatch errors in time-interleaved ADCs. Sub-band filters based on a round-robin calibration for each channel are designed to minimize the aliasing error in the sub-band. Consequently, the technique exploits the signal characteristics enabling a reduction in hardware complexity compared to prior-art for most classes of signals. The technique performs well over a large class of input signal types and performs favorably with respect to recently published digital calibration methods.

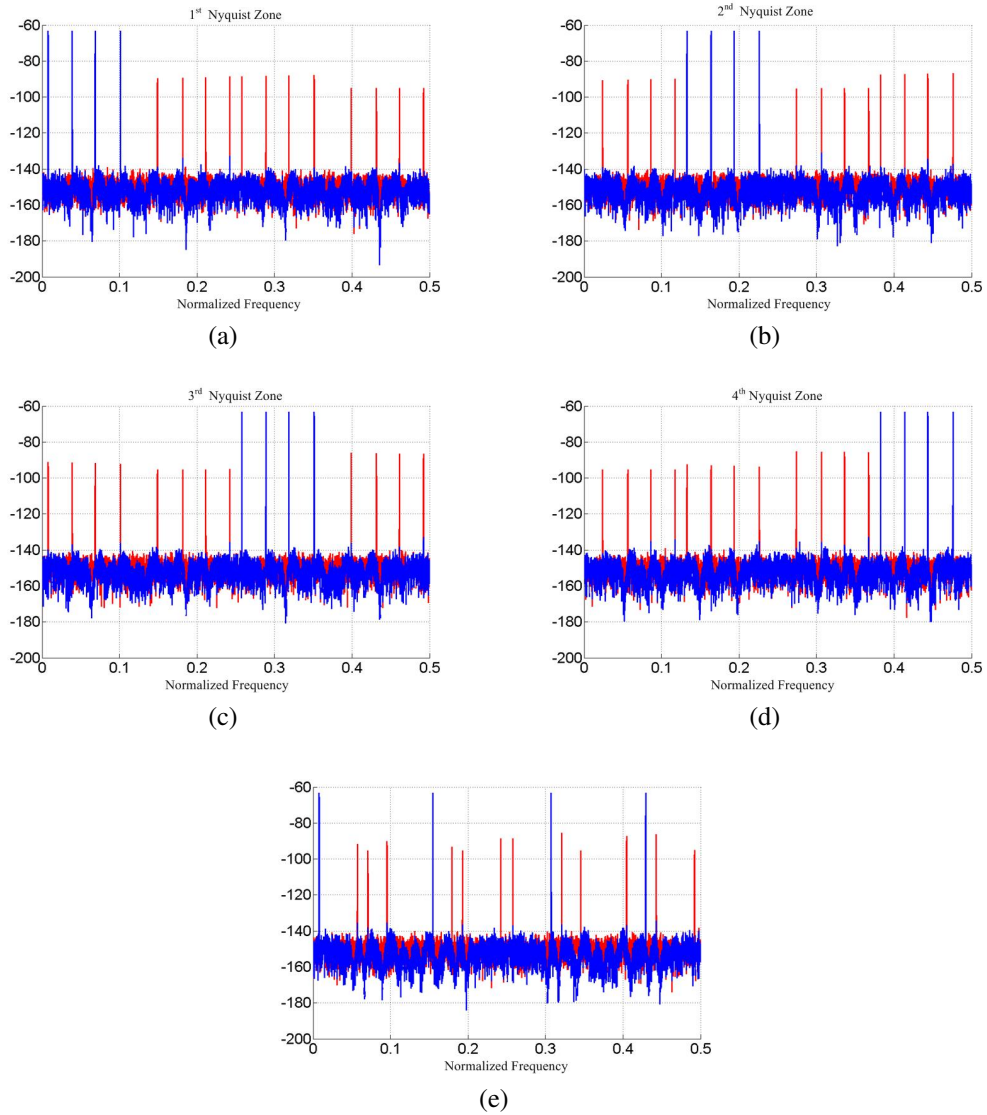


Figure 4.6: Simulation results for the proposed technique with rich inputs in (a) Nyquist zone 1 (b) Nyquist zone 2 (c) Nyquist zone 3 (d) Nyquist zone 4 (e) All Nyquist zones

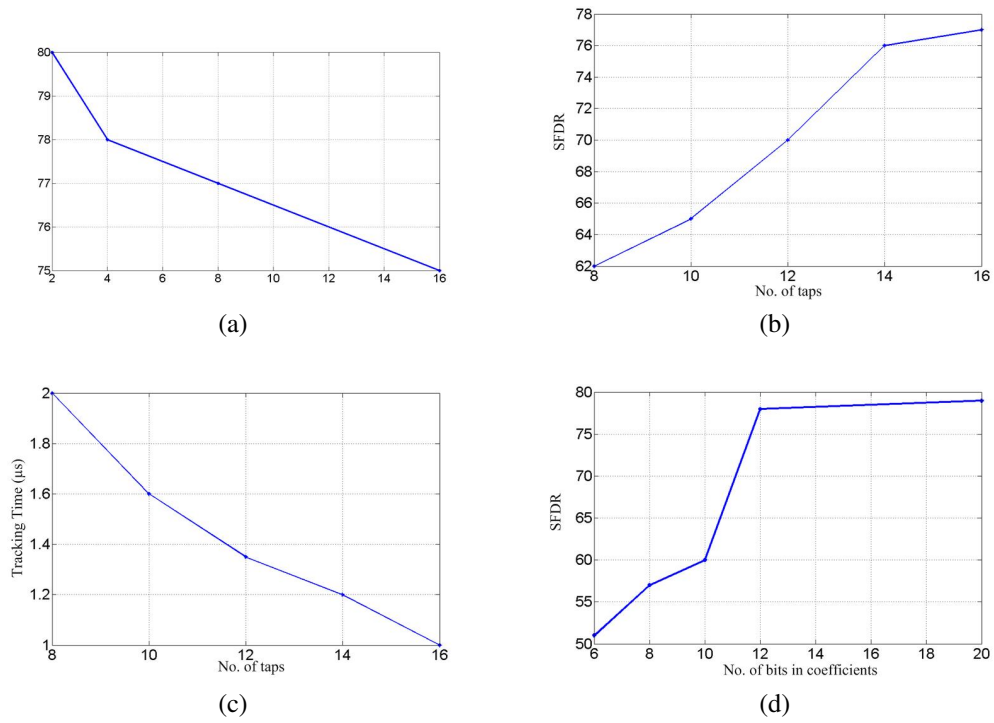


Figure 4.7: Trends (a) SFDR vs. number of channels (b) SFDR vs. number of filter taps (c) Adaptation time vs. number of taps (d) SFDR vs. coefficient bit-width

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