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# Multiplexed Oversampling Digitizer in 65 nm CMOS for Column-Parallel CCD Readout

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*Abstract*–A digitizer designed to read out column-parallel charge-coupled devices (CCDs) used for high-speed X-ray imaging is presented. The digitizer is included as part of the High-Speed Image Preprocessor with Oversampling (HIPPO) integrated circuit. The digitizer module comprises a multiplexed, oversampling, 12-bit, 80 MS/s pipelined Analog-to-Digital Converter (ADC) and a bank of four fast-settling sample-and-hold amplifiers to instrument four analog channels. The ADC multiplexes and oversamples to reduce its area to allow integration that is pitch-matched to the columns of the CCD. Novel design techniques are used to enable oversampling and multiplexing with a reduced power penalty. The ADC exhibits 188 V-rms noise which is less than 1 LSB at a 12-bit level. The prototype is implemented in a commercially available 65 nm CMOS process. The digitizer will lead to a proof-of-principle 2D 10 Gigapixel/s X-ray detector.

## I. INTRODUCTION

Emerging particle detection and scientific imaging applications require greatly increased readout rates to enable the capture of dynamic processes. Future X-ray light sources, for example, will require instrumentation that digitizes at pixel rates in excess of 100 Gpixel/s [1]. A significant research and development effort is underway to develop application appropriate solid-state imagers and their associated readout electronics. The circuit described leverages 65 nm technology and novel design techniques to enable a column rate of 10 MHz, corresponding to a system pixel rate of 10 Gpixel/second (10,000 fps for a 1 Mpixel square sensor). The circuit is envisioned for use as a platform for the accelerated development of detector readout ICs. Its first application is in the High-Speed Image Preprocessor with Oversampling (HIPPO), a highly integrated column-parallel CCD readout Application Specific Integrated Circuit (ASIC) whose system aspects have been described [2]. This paper is organized as follows: Section II presents the digitizer requirements, Section III describes the circuit architecture and circuit testing is discussed in Section IV.

## II. CCD DIGITIZER REQUIREMENTS

In order to reduce system cost and complexity, the readout channels are required to match the 50 μm column pitch of a prototype column-parallel thick, fully depleted X-ray CCD.

To provide sufficient dynamic range, the digitizer is required to combine 12-bit resolution and noise with 10-bit accuracy. Traditionally, pipelined ADCs are specified for enhanced linearity relative to their noise performance because of the significant linearity requirements for digitizers used in digital communications. In scientific imaging, however, noise is often more important than linearity when the imager is deployed in situations where it is not expected to simultaneously image bright and low-light areas. The 80 MS/s sampling rate requirement is due to multiplexing and oversampling, as discussed below. The requirements are summarized in Table I. The full-scale range is chosen for compatibility with 65 nm CMOS technology and the serial output is specified by a desire to reduce output pin count.

TABLE I. HIPPO DIGITIZER REQUIREMENTS

| Requirement | Value | Units | Comment |
|---|---|---|---|
| Resolution | 12 | Bits | |
| Sampling Rate | 80 | MS/s | |
| Full Scale | 1 | Volts | Vpp-differential |
| Noise | 200 | V-rms | LSB is 250 uV |
| Linearity | 10 | Bits | Differential |
| Circuit Pitch | 50 | m | match CCD |
| Serial Output | 480 | Mb/s | dual data rate |

A block diagram of a possible application system for HIPPO is shown in Fig. 1. The CCD control FPGA generates multi-phase digital clocks for the clock driver chip. These digital clocks are converted in the clock driver chip to high-voltage clocks suitable for driving the CCD. The CCD control FPGA also generates a master clock and convert signal for the HIPPO ASIC in order to synchronize the data transfer across the system. The readout FPGA consumes the data from the HIPPO ASIC. An analog timing monitor output from the HIPPO ASIC is used provide a fine control to the CCD clocks to improve their synchronization with the HIPPO clocks and improve the quality of image transfer. Both the CCD control FPGA and the readout FPGA share a common crystal-derived time base.
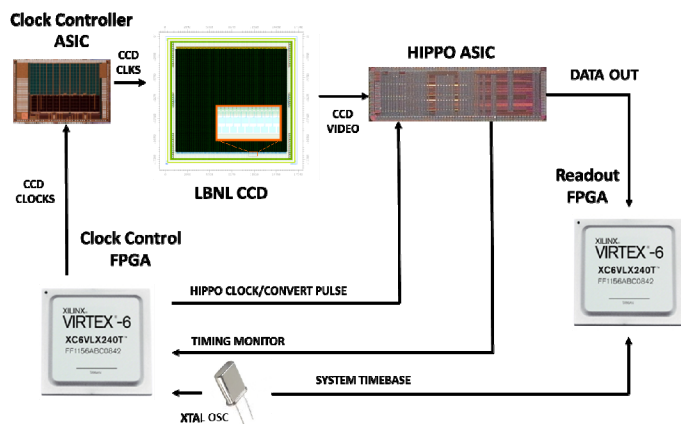
Fig. 1. Block diagram of HIPPO ASIC application system for Column-Parallel CCD readout.



Fig. 3. Block diagram of HIPPO ADC. The ADC uses the Redundant Signed Digit algorithm to relax requirements on the analog components.

## III. CIRCUIT ARCHITECTURE

A block diagram of a HIPPO IC module is shown in Fig. 2. The implemented ASIC comprises 16 channels, which are organized as four distinct 4-channel modules. Each readout module consists of four analog front-end circuits, a bank of four sample-and-hold amplifiers (SHAs), and a multiplexed pipelined ADC. The ADC is multiplexed between the four channels to enable channel pitch matching with the 50 μm CCD columns. The ADC data are serialized to save pin count and are sent off chip at 480 Mb/s.
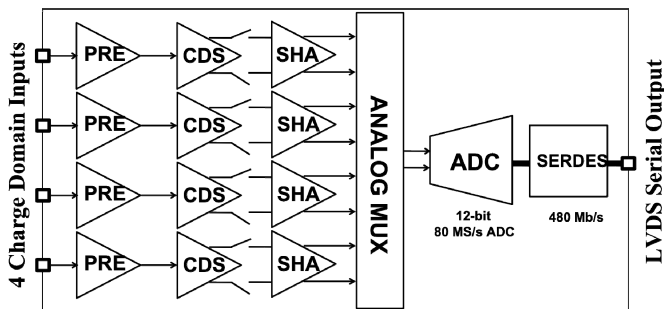


Fig. 2. Simplified block diagram of HIPPO ASIC module. The ASIC comprises four such modules of four channels each, for a total of input 16 channels.

A block diagram of the ADC is shown in Fig. 3. The ADC consists of 11 identical stages each containing a coarse ADC, a coarse DAC, and an interstage amplifier. Each stage processes the quantization error of the previous stage, and each stage provides one effective bit (two for stage 11) after redundancy elimination. The redundancy provided by the 1.5 bits/stage algorithm allows the accuracy of the ADC to be determined almost entirely by the accuracy of the interstage amplifier because a three-level coarse DAC is inherently linear in a differential sense and large offsets can be tolerated in the coarse ADC [3]. In the prototype the stages are not scaled in order to reduce design time. In future versions the downstream stages can be scaled to reduce power consumption and area without compromising performance.
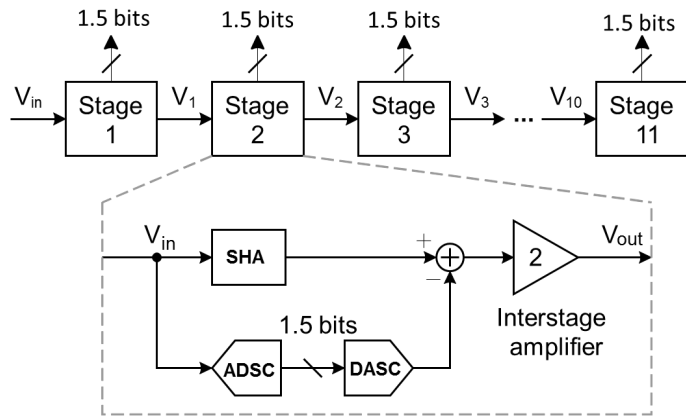
In a pipelined ADC, the gain of the first stage interstage amplifier must be at least as accurate as the resolution remaining after the first stage [4]. In the ADC presented, the first stage resolves one effective bit and the linearity specification for the total ADC is 10 bits. Therefore, the interstage amplifier in the first stage of the ADC must be at least 9-bit accurate. Given the feedback factor of the closed-loop amplifier, this translates to an open-loop gain requirement of about 60 dB for the Operational Transconductance Amplifier (OTA) used to implement the interstage amplifier. In the prototype, all OTAs use the fully differential folded-cascode structure shown in Fig. 4. In 65 nm CMOS, achieving high open-loop gain in one stage is challenging because the self-gain of the devices is less than 10 when small devices biased in moderate inversion are used [5]. The open-loop gain cannot be easily increased by using multiple levels of cascoding because of the headroom constraints imposed by the low power supply voltage required by the 65 nm process. To overcome this gain limitation, gain boosting is used in the OTA to regulate the voltage across the cascode devices in order to increase the OTA output resistance [6]. Gain boosting increases the open-loop gain of the OTA by a factor of about the gain of the gain-boosting amplifier. The expense of gain boosting is increased power dissipation and more challenging frequency compensation due to the presence of a pole-zero couplet in the transfer function [7].
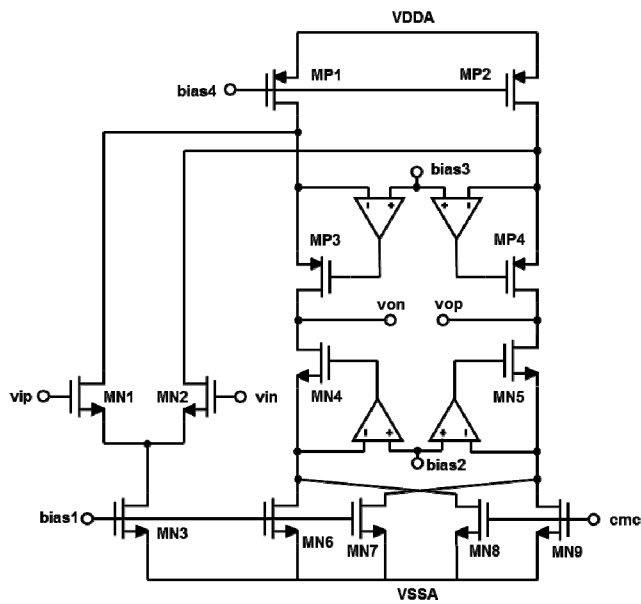
Fig. 4. Schematic of OTA used in the HIPPO ADC and SHA. Circuit uses gain boosting to enable closed-loop settling to better than 0.025% of full scale in a single stage.

To meet the required noise performance in a reduced silicon area, oversampling is employed. Oversampling entails averaging multiple samples of a signal. Because the signal components of the samples are strongly correlated and the white noise components uncorrelated, oversampling increases the signal-to-noise ratio of the signal by a factor equal to the square root of the number of samples used in the average. A plot of the efficacy of oversampling in reducing the input referred noise of a Nyquist-rate ADC is shown in Fig. 5. The same performance could be achieved without oversampling by increasing the sizes of the capacitors in the interstage amplifier but at the expense of increased die area.
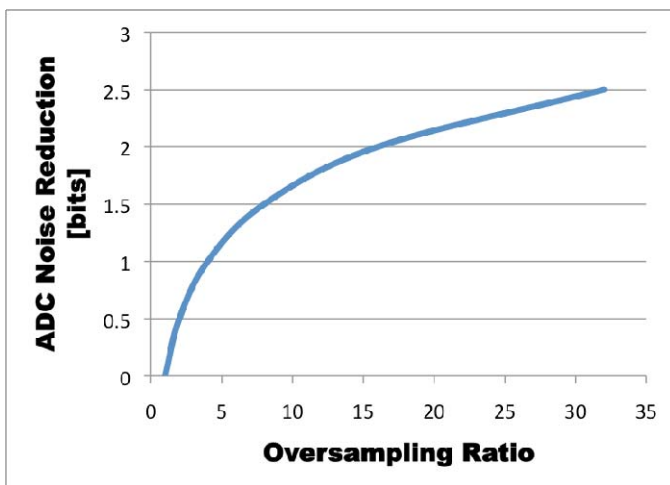


Fig. 5. ADC noise reduction as a function of the ADC oversampling ratio.

Significant improvements in noise performance are possible with oversampling. Oversampling is only feasible when the input bandwidth is significantly below the achievable sampling rate of the technology. To generate the required

timing to implement oversampling, the HIPPO digitizer is flexibly clocked using the circuit in Fig. 6. A master clock is sent down independent delay lines that are then used to select different frequencies for the ADC clock and the channel clock under digital control.
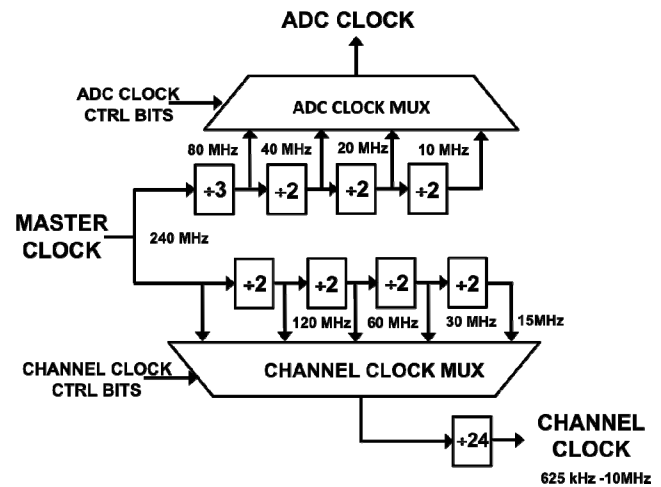


Fig. 6. HIPPO clock generation block that features flexible choice of channel and ADC clock rates to choose oversampling ratio.

The channel clock is the digital clock that controls the front-end circuits of the system [2] such as the preamp and the correlated double-sampler. The ADC clock drives the analog-to-digital converter. The channel clock and the ADC clock can be adjusted separately to give an oversampling ratio of between 1 (no oversampling) to 32 (maximum oversampling). The key penalties in oversampling using a Nyquist-rate ADC are the reduction in the system input bandwidth and the increased power dissipation for a given speed.

There are at least two reasons why oversampling a multiplexed input signal that is not valid throughout the ADC sampling period is challenging. First, it requires a number of SHAs equal to the number of channels, increasing die area and power dissipation. Second, it requires a SHA fast enough to provide multiple samples of the valid period. In Fig. 2, for example, the SHA input is valid for about 10 ns when the channel is operated at 5 MHz. Oversampling this SHA by a factor of four would require it to settle to the desired accuracy in less than 2.5 ns. To relax the SHA requirements while still allowing low-noise oversampling we have developed a sampling method that adds less noise to the signal than would an analog delay line at a given power dissipation. Oversampling the front-end output directly would require an extremely fast ADC that would dissipate a large amount of power. Instead, a bank of fast-settling SHAs is used to allow for uniform ADC sampling without additional noise, since the bank of SHAs would replace the ADC input SHAs required to implement multiplexing. The sampling is uniform in the sense the ADC is sampling periodically. To reduce power, the SHAs can taper their bias currents based on the order in which they are sampled. This increases the settling time of each tapered SHA but has no effect on accuracy as long as the SHA is settled before sampling, as shown in Fig. 7. The power is

reduced because the SHAs no longer consume power to settle quickly when they are not scheduled for sampling for some time.
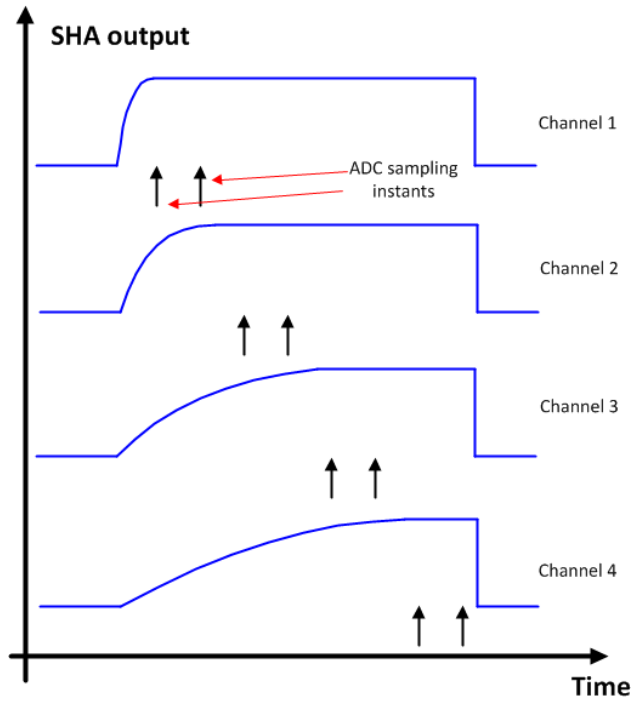


Fig. 7. Bias tapered SHA sampling. The settling time of each parallel SHA is tuned to settle to its desired accuracy right before sampling to reduce power consumption.

The potential for system-level power reduction that can be achieved through the use of bias tapering can be seen in Fig. 8.
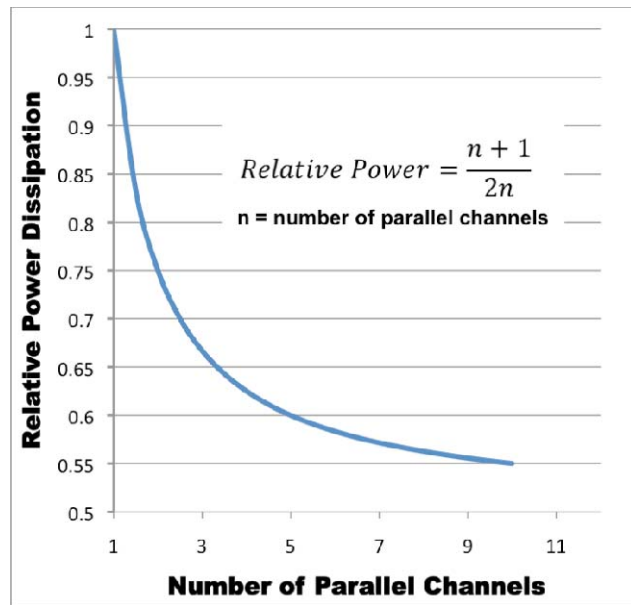


$$Relative\ Power = \frac{n+1}{2n}$$

n = number of parallel channels

Fig. 8. Power savings in SHA arrary using tapered biasing and untapered , standard biasing.

The number of parallel channels is the number of channels receiving bias tapering. In the prototype, each 4-channel

module is bias tapered, which reduces the power dissipated in the SHA bank by 37.5% relative to the case when all SHAs settle with the same time constant.

Even with the introduction of the bias tapering technique, the SHAs still require fast settling and consume a significant amount of power. To enable the fast settling of the SHAs at acceptable power dissipation, the flip-around architecture shown in Fig. 9 is used to maximize the SHA feedback factor [4]. The flip-around SHA uses the same capacitor for acquisition and regeneration of the input signal, and therefore has a feedback factor that is substantially higher than a traditional switched-capacitor amplifier. To eliminate signal-dependent offsets, the SHA uses the bottom-plate sampling technique [8]. The input common-mode shorting switchs clocked by $\phi_{1p}$ are turned off slightly before the input switches. Therefore, charge injection from the shorting switch is a common-mode signal to first order. In a differential configuration this charge injection is canceled and does not affect the linearity of the circuit. The SHA is clocked such that it tracks the analog front-end output during settling and can sample without spending additional time to acquire the signal. The output common-mode level of the SHA is stabilized by a switched-capacitor based common-mode feedback circuit [8].
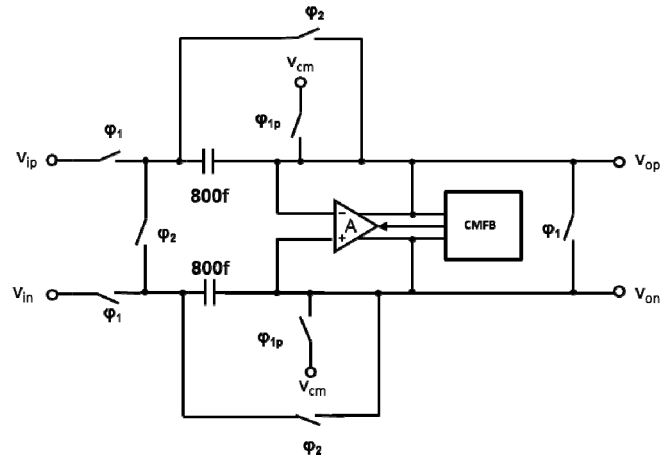


Fig. 9. HIPPO Sample-and-Hold amplifier. The circuit uses the flip-around architecture to maximize the feedback factor for fast settling.

To minimize design time, the OTA that was designed to meet the requirements for the first stage of the ADC was reused to implement the SHA.

A block diagram of the serializer used in the HIPPO ASIC is shown in Fig. 10. Because the data rate is limited to 480 Mb/s/port, two serializers are used to output data when the ADC is converting at 80 MHz. The serializer operates as follows. First, the word to be serialized is latched by a 40 MHz word clock and then introduced into two parallel shift registers. Next, these shift registers are clocked using a 240 MHz bit clock. Finally, the outputs of these shift registers are then multiplexed into an LVDS driver. The bit clock is used to drive the multiplexer so the output bit changes on both the rising edge and the falling edge of the bit clock, giving a data rate of twice the bit clock frequency, or 480 Mb/s. The datapath consists of manually routed standard cells, while the

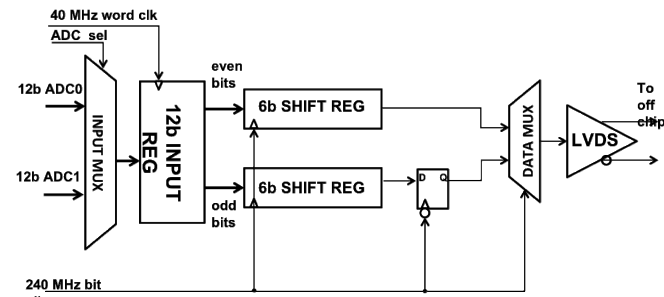serializer control state machine is constructed with synthesized logic.



Fig. 10.  Block diagram of HIPPO dual data rate serializer.

A die photomicrograph of the HIPPO ASIC is shown in Fig. 11.  To maintain a 50 m channel pitch, the inputs are bonded to staggered pads.  Including a test channel and bond pads, the IC is 4.2 mm by 1 mm in size.
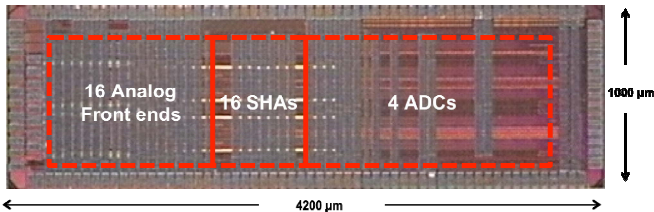


Fig. 11.  Annotated photomicrograph of HIPPO ASIC.

## IV.  CIRCUIT TESTING

A photograph of the custom HIPPO testboard and a control board based on a commercial FPGA evaluation board is shown in Fig. 12.  The FPGA evaluation board generates the master system clock and receives and decodes the LVDS outputs of the HIPPO IC.  The FPGA also programs the HIPPO configuration register for settings such as channel rate, ADC rate, test-mode status and fine tuning for the timing generator.
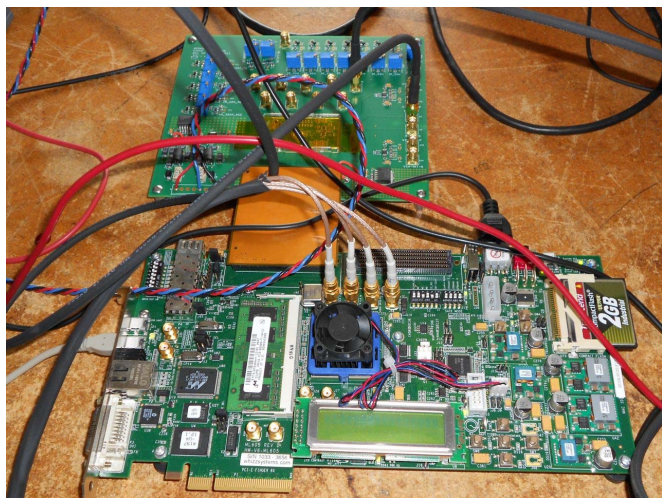


Fig. 12.  Photograph of custom HIPPO testboard and control board based on commercial FPGA evaluation board.

A close-up photograph of the HIPPO test board is shown in Fig. 13.  The die is direct-to-board bonded.
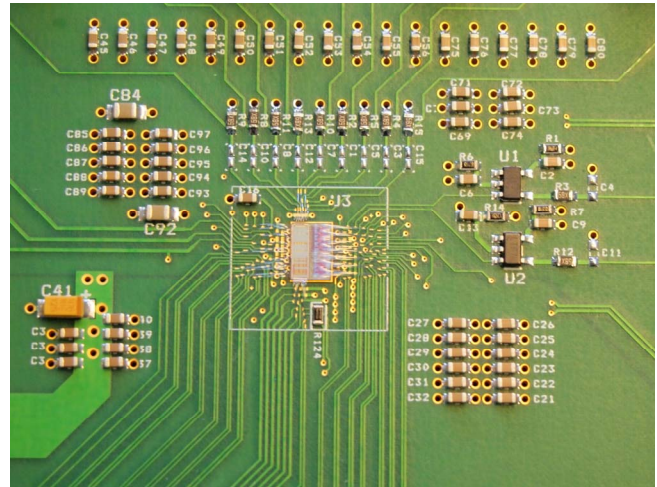


Fig. 13.  Close-up photograph of HIPPO custom test board showing direct wirebonding to board assembly.

A screenshot of the test software showing ADC functionality is shown in Fig. 14.  In this test, the input is a low frequency sinusoid and the plot shows digital data recovered by the FPGA.
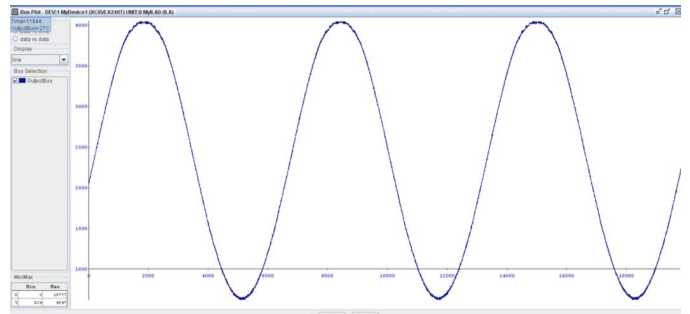


Fig. 14.  Example digital output of HIPPO ADC.  Test input was analog sinusoid.

The primary design challenge for the HIPPO ADC is its specification for low-noise operation.  To test the noise performance of the ADC, the input was set at a dc level and continuously converted.  The data are plotted in Fig. 15.  A Gaussian distribution that is fitted to the data is also plotted. The spread of the output codes then can be interpreted as an indication of the input-referred noise of the ADC.  HIPPO was specified for noise less than 200 V-rms.  With a full-scale voltage range of 1 V pp-diff, this equates to less than an LSB at a 12-bit level.  The rms noise is 188 V-rms, or about 0.77 LSB.
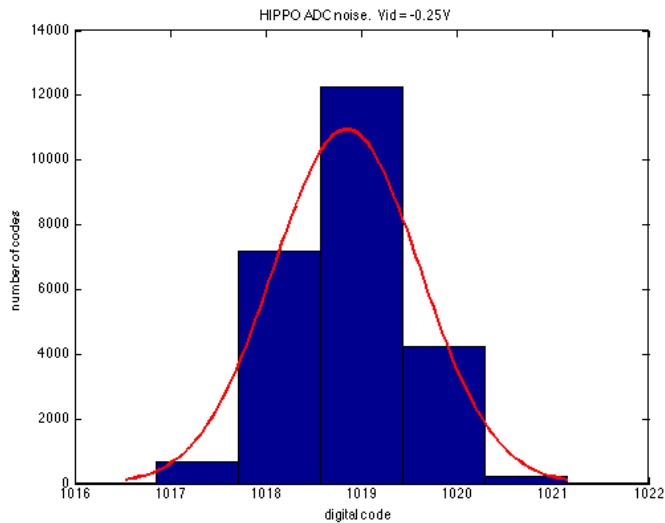
Fig. 15. Noise performance of HIPPO ADC. Noise level is 188 V-rms, or about 0.77 LSB at a 12-bit level.

## V. CONCLUSION

An integrated digitizer suitable for the instrumentation of column-parallel CCDs is presented. The digitizer provides true 12-bit noise performance and operates up to 80 MS/s. Combined with a charge-sensitive analog front end in the HIPPO ASIC, the digitizer will lead to a proof-of-principle 2D 10 Gigapixel/s X-ray detector.

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