UCLA
UCLA Electronic Theses and Dissertations

Title
Flexible and Transparent Memory

Permalink
https://escholarship.org/uc/item/42c6w65s

Author
KIM, SUNG MIN

Publication Date
2012

Peer reviewed|Thesis/dissertation

eScholarship.org Powered by the California Digital Library
University of California

UNIVERSITY OF CALIFORNIA

Los Angeles

Flexible and Transparent Memory

A dissertation submitted in partial satisfaction

of the requirements for the degree Doctor of Philosophy

in Electrical Engineering

by

Sung Min Kim

2012

© Copyright by

Sung Min Kim

2012

ABSTRACT OF THE DISSERTATION

Flexible and Transparent Memory

by

Sung Min Kim
Doctor of Philosophy in Electrical Engineering
University of California, Los Angeles, 2012
Professor Kang L. Wang, Chair

Electronic devices have been going through intensive renovations in order to reply to the high demands of consumers. In the near future, electronic devices are projected to be incorporated into flexible and wearable modules to meet the everlasting needs. With the intention of turning this somewhat fantasy into reality, flexible and wearable electronic devices would require multiple core modules, such as display, logic, and memory to be integrated on a single substrate.

In this thesis, we present a graphene channel transistor based flexible and transparent memory (FTM) fabricated on Poly-ethylene-naphtalate (PEN) substrate. FTM samples were successfully fabricated through low temperature processes preventing substrate deformation. The injection of electrons into the trap sites of a triple high-k dielectric stack resulted in a memory window of more than 9.0V. The experimental results show great potential for FTM to be used as a memory cell for fully flexible and transparent electronics. Furthermore, FTM might enable making a breakthrough in innovative design for electronics that has been impossible when using stiff and opaque substrates.

The dissertation of Sung Min Kim is approved.

Oscar Stafsudd

Yong Chen

Rob Candler

Kang Wang, Committee Chair

University of California, Los Angeles

2012

TO MY PARENTS FOR THEIR UNBOUNDED LOVE AND SUPPORT,
TO MY BROTHER AND SISTER-IN-LAW FOR THEIR SINCERE ENCOURAGEMENT,

TABLE OF CONTENTS

Chapter 1 **Introduction**

1.1 Overview: Non-Volatile Memory (NVM) technology 1

1.2 The basic operation principle and history of NVM device 1

1.3 Scaling of Flash memory 4

1.4 Charge Trap Memory (CTF) 6

1.5 Carbon based materials for flexible electronics 9

1.6 Graphene fabrication 11

1.7 Electrical properties of graphene 14

1.8 Mechanical properties of graphene 17

1.9 Flexible electronics 19

1.10 References 21

Chapter 2 **Non-Volatile Graphene channel Memory (NVGM)**

2.1 Introduction: Graphene channel FET based NVM 27

2.2 Fabrication: NVGM structure and process flow 29

2.3 Electrical characteristics 32

2.3.1 Performances of graphene channel FETs 32

2.3.2 NVGM memory functions 34

2.4 Impact of gate work-function on memory characteristics 37

2.5 Summary 46

2.5 References 47

Chapter 3 **Flexible and Transparent Memory (FTM)**

3.1 Introduction: Memory module for flexible and transparent electronics 49

3.2 FTM structure and fabrication process flow 50

3.3 Optical transparency of FTM 54

3.4 Electrical characteristics of FTM

3.4.1 Performance of flexible and transparent FET 55

3.4.2 FTM memory functions 59

3.5 Functional sustainability under geometrical deformation 63

3.6 Summary 68

3.7 References 69

Chapter 4 **Embedded Oxide Trap memory (EOTM) using graphene as channel**

4.1 Motivation: Electron back injection issue of FTM 73

4.2 EOTM structure and fabrication process flow 73

4.3 Electrical characteristics of EOTM 76

4.4 Summary 81

4.5 References 82

Chapter 5 **Suspended few-layer Graphene beam electromechanical Switch (SGS)**

5.1 Introduction: Abrupt On/Off switching with zero leakage current 84

5.2 SGS structure and fabrication process flow 86

5.3 Switching characteristics of SGS 90

5.4 Summary 95

5.8 References 95

Chapter 6 **Conclusion and Future works** 99

LIST OF FIGURES

Figure 1.1 Basic operating principle of nonvolatile semiconductor memory: the storage of charges in the gate insulator of a MOSFET. 2

Figure 1.2 Influence of charges in the charge storage layer on the threshold characteristics of an n-channel MOSFET. 2

Figure 1.3 Schematic energy band diagram of a charge trap non-volatile memory. (a) A Programming Operation. Positive bias is applied on a gate and induces FN tunneling current injecting electrons from a channel to a nitride film, (b) An Erasing Operation. Positive bias is applied on a body electrode (or negative bias on a gate) and allows electrons to go back to a channel. 3

Figure 1.4 (a) NAND flash memory cell (Intel–Micron technology 2010) (b) scaling trend of microprocessor and flash memory. 5

Figure 1.5 3D NAND flash cell structures. 6

Figure 1.6 Structures of the charge-trapping based nonvolatile memory transistors. 8

Figure 1.7 Carbon nano-tubes (CNT), which hold similar electrical and mechanical properties compared to graphene, have also been considered as a channel material for flexible electronics. 10

Figure 1.8 Optical images of graphene films depending on different wavelengths of light. 11

Figure 1.9 Atomic force microscopy (a,c,d) and Raman spectroscopy (b,d,e) of SiC substrates graphitized at (a,b) 1225 °C, (c,d) 1325 °C. (ref.34). 12

Figure 1.10 Schematic of the roll-based production of graphene films grown on a copper foil. The process includes adhesion of polymer supports, copper foil. The processes are divided into three steps: (a) the adhesion of polymer supports, (b) copper etching and (c) transfer to the target substrate. 14

Figure 1.11 Graphene band structure showing the nonequivalent K and K valleys. In the figure the Fermi energy (transparent plane) is located at the Dirac neutrality points, which separate the hole states below them

from the electron states above them. Inset shows the energy dispersion relations along the high symmetry axes near the Dirac point. 15

Figure 1.12 (a) Scanning Electron Micrograph image of back gated graphene channel transistor. (b) Typical Drain current I_D to gate voltage V_G characteristic of graphene channel transistor, Conical low-energy spectrum E(k), indicating changes in the position of the Fermi energy E_F with changing V_G. 17

Figure 1.13 (a) Honeycomb lattice of graphene and (b) its Brillouin zone. Left: lattice structure of graphene, (**a**1 and **a**2 are the lattice unit vectors, and i, i=1,2,3 are the nearest-neighbor vectors). 18

Figure 1.14 (a) Evolution of personal computer responding to customer's demands. Flexible electronic devices demonstrate by (b) Samsung Mobile Display and (c) LG electronics. 20

Figure 2.1 Schematic diagram of NVGM structure. 28

Figure 2.2 RAMAN spectra of transferred SLG and MLG. 29

Figure 2.3 Process flow for the test structure of Non-Volatile Graphene channel Memory (NVGM). 30

Figure 2.4 Cross-sectional TEM image of NVGM cut along A-A' direction in Figure 2.1 and $Al_2O_3/HfO_2/Al_2O_3$ (AHA) stack. 30

Figure 2.5 Band structure of NVGM before and after contact. 31

Figure 2.6 NVGM is designed to have similar and structure and operation mechanism to SONOS. But the channel is replaced by graphene and ONO dielectric stack is replaced by triple Al_2O_3 HfO_2 Al_2O_3 triple high-k stack to enhance performance and to lower the process temperature. 31

Figure 2.7 (a) Dual sweep I_{DS}-V_{GS} and (b) I_{DS}-V_{GS} characteristic of NVGM with SLG channel as functions of V_{TG} and V_{BG}. 33

Figure 2.8 I_{DS}-V_{GS} characteristic of NVGM depends on $V_{BG.}$ NVGM with L_G/W=3/4.3um shows high current drivability approaching 1mA at V_{TG}=10V, V_{BG}=35V, and V_D=1.2V. 34

Figure 2.9 Program and erase characteristics of NVGM. Samples with SLG and MLG channels display memory windows of 11.5V and 7.3V.

respectively. Samples are programmed by voltage stress with V_P=30V for 10ms and erased by V_E=-25mV for 30ms.. 35

Figure 2.10 Samples with SLG channel shows (a) higher initial V_{DIRAC} position and (b) wider memory window than that with MLG. 36

Figure 2.11 V_{DIRAC} shift depends on the program and erase voltage (V_P and V_E). Back electron injection from gate electrode is observed when V_E<-28V. 37

Figure 2.12 (a) I_{DS}-V_{GS} characteristic curves of gFET(AHA) after programming and erasing at various V_P (+12 – +24 V; 10 ms; step: +2 V) and V_E (-12 to - 24 V; 30 ms, step: - 2 V). (b) Variation of ΔV_{Dirac} as a function of V_P and V_E for Ti-gate gFET(AHA). 39

Figure 2.13 (a) I_{DS}-V_{GS} characteristic curves of Ni-gate gFET(AHA) after programming and erasing at various V_P (=+16 to +32 V; 10 ms; step: +2V) and V_E (=-16 to - 32 V, 30 ms; step: - 2 V). (b) Variation of ΔV_{Dirac} as a function of V_P and V_E for Ni-gate gFET(AHA) 40

Figure 2.14 Energy band diagrams of Ti- and Ni-gate gFETs(AHA) at various bias conditions. Ti-gate gFET(AHA): (a) V_G = 0 V, (b) V_G = +V_1, (c) V_G = -V_2, (d) V_G = -V_3 (<<-V_2). Ni-gate gFET(AHA): (e) V_G = 0 V, (f) V_G = +V_1, (g) V_G = -V_2, (h) V_G = -V_3 (<< -V_2).. 41

Figure 2.15 Gate leakage current density of AHA high-k gate dielectric. 43

Figure 2.16 Data retention characteristics of NVGM. 44

Figure 2.17 SEM image of NVGM cell array. 44

Figure 2.18 Possible application of NVGM ultra-high-density data storage. NVGM cell could be fabricated using flat panel display production lines and 3D multi-stack memory could be fabricated stacking NVGM cell on peripheral circuit fabricated using Si CMOS processing. 45

Figure 3.1 Fabrication process steps of transparent-flexible FTM. 51

Figure 3.2 FTM is fabricated on flexible and transparent polyethylene naphtalate (PEN) substrate. 52

Figure 3.3 Schematic illustration of FTM device structure. 52

Figure 3.4 (a) Cross-sectional SEM and TEM image of $Al_2O_3/HfO_x/Al_2O_3$ (AHA) gate stack in FTM. (b) Bird's eye view SEM image of high-density FTM array. 53

Figure 3.5 Optical transmittance spectra of FTM and PEN substrate. The addition of FTM on the PEN results in an 8% reduction of transparency in the visible wavelengths. 55

Figure 3.6 Photograph of the large scale transparent-flexible FTM array fabricated on PEN substrate. 56

Figure 3.7 I_D-V_G characteristics of FTM. 57

Figure 3.8 I_D-V_D characteristics of FTM. 57

Figure 3.9 Program and erase operation mechanism of FTM. 58

Figure 3.10 Electrical characteristics of FTM. (a) Memory window as a function of program/erase voltage. A maximum window of ~8.6 V is achieved. Electron back injection starts to occur at erase voltage of ~-22 V. 60

Figure 3.11 Gate tunneling current density. The tunneling mechanism for the standard program/erase operation corresponds to trap-assisted (TA) tunneling and the electron-back injection arises through Fowler-Nordheim (FN) tunneling. 61

Figure 3.12 Retention characteristics of FTM. 62

Figure 3.13 Endurance of electrical characteristics under flex. (a) Normalized resistance vs. gate voltage under tensile and compressive stress at V_D = 1 V. The FTM reveals minimal Dirac point shift and channel transconductance change under bending. 63

Figure 3.14 On-state current under bending stress measured at V_D = 1 V and V_G = 7 V. 64

Figure 3.15 Position of Dirac point under bending stress at program/erase states (V_P = 23 V, V_E = -21V). 65

Figure 3.16 FTM can be utilized for transparent and flexible electronics that require integration of logic, memory and display on a single substrate with high transparency and endurance under flex. 66

Figure 4.1 For the fully flexible and transparent electronics application, adoption of graphene gate electrode is desirable, but graphene gate electrode might cause serious electron back injection problem as well when it integrated with AHA triple high-k dielectric. 74

Figure 4.2 Schematic of EOTM test structure with AAA triple high-k stack. 75

Figure 4.3 Fabrication procedure of transparent-flexible EOTM (AAA). 75

Figure 4.4 SEM image of FTM active region formed on PEN flexible and transparent substrate. 75

Figure 4.5 (a) Transistor characteristics controlled by back gate electrode before and after OIB process. (b) No significant reduction drain current was observed. This result reflects that the depth of OIB is shallower than 15nm and graphene channel remained intact after OIB process. 76

Figure 4.6 (a) I_{DS}-V_{GS} and (b) I_{DS}-V_{DS} characteristics of EOTM with SLG channels. EOTM transistor with L_G/W=15 m/7 m shows current drivability approaching 85 A. 77

Figure 4.7 I_{DS}-V_{DS} curve of EOTM with SLG channel and AAA dielectric stack. EOTM shows high on-state current due to the high carrier mobility of graphene channel. 77

Figure 4.8 Comparison of memory characteristics depends on OIB power, EOTM fabricated with higher OIB process showed wider memory window. The MW of 11.3V for 200W and 9.5V for 100W are achieved by using a P/E conditions of V_P=24V, 10ms and V_E=-22V, 30ms. 78

Figure 4.9 V_{DIRAC} shifts depend on the program and erase voltage (V_P and V_E). 78

Figure 4.10 V_{DIRAC} shifts depending on the program and erase voltage (V_P and V_E). Adoption of AAA effectively suppresses electron back injection from the gate electrode. 79

Figure 4.11 A low dielectric constant of AlO_x results in a larger potential drop across the charge storage layer and reduces the slope of the conduction band in the control oxide. Hence, the thickness of the F-N tunneling barrier increases making it difficult for the electron back injection to occur. 80

Figure 4.12 Data retention characteristics of FTMs with different charge storage layers. FTMs can maintain memory window of 1V up to 10 years. 81

Figure 5.1 Moving parts of MEMS switch have been made of poly-crystalline or amorphous material such as metal or poly-Si or metal. For this reason, pull-in voltages of conventional MEMS switches are still too high to be integrated with CMOS circuits. 85

Figure 5.2 The size of the moving part become comparable to the size of poly-crystalline grain when it scaled down bellow hundred nanometer regime. Durability of moving part is degraded mainly due to the cracks originates from grain boundaries. 85

Figure 5.3 Scanning electron microscope (SEM) images of suspended graphene beam switches. (a) Bird's eye view of graphene beam length/width of 15 m/2 m and air gap of 0.15 m, (b) Tilted view of grapehen beam length/width of 15 m/5 m and gap of 2 m. 87

Figure 5.4 Schematic of fabrication process flow for SGS. 1: A 6-inches wafer scale CVD grown multi layer graphene film is transferred onto a SiO_2 layer thermally grown on highly doped n-type Si substrate. 2: Graphene beam is patterned using photolithography and O_2 plasma etching process. 3: Au/Cr top electrode is formed by e-beam evaporation and following metal lift-off and 4: graphene beam is released by selective removal of SiO_2 layer using diluted HF and the height is controlled by successive etching of Si substrate using diluted KOH solution. Then sample is dried by super critical point drying. 88

Figure 5.5 (a) RAMAN spectrum of transferred multi-layer graphene. (b) Optical microscope image of patterned graphene, transferred graphene is measured to be around 3nm in thickness. 89

Figure 5.6 Current-Voltage characteristics between the top and bottom electrodes. The average pull-in voltage of SGS with 20 m graphene beam and 0.15 m gap was lower than 1.85. 91

Figure 5.7 Pull-in voltage dependence on graphene beam length. 92

Figure 5.8 Degradation of switching characteristic resulting from initial stiction and contamination. 93

Figure 5.9 Conceptual combination of graphene based memory with MEMS switch. 94

LIST OF TABLES

Table 1.1 Materials properties of graphene and bulk silicon. 19

Table 2.1 Comparison of SONOS memory and FTM. 67

ACKNOWLEDGEMENTS

In fact, I could not write this page without expressing my deepest thanks to my academic advisor, Prof Kang Wang. I appreciate his encouragement and invaluable opportunity he provided me with. I have learnt a lot from his vast knowledge, experience and profession. I am grateful for all the support, invaluable advices, and helpful insights of my committee members: Prof. Oscar Stafsudd, Prof. Rob. Chandler and Prof. Yong Chen.

As a member of DRL Group, I am also privileged to be able to work with talented and hard-working members. I would grateful to Emil B. Song and Sejoon Lee for their invaluable collaboration and discussion on my research topic. I also would like to thank Siguang Ma, Minsheng Wang, Carlos Manuel Torres, Boris Vulovic, Caifu Zeng and Hsin-Chieh Yu for their friendship. I would like to thank my friends, Kyungsik Shin, Yongha Hwang, Kyungwon Park, Hyungsuk Yu and Pilbum Kim for sharing both joyful and hard times in graduate school together.

I would like to acknowledge Samsung Electronics for trust and financial support. Especially, I would really thank Vice President Donggun Park for his precious advices and encouragement for me to enter the academic education program.

I should thank all my friends, colleagues and former members who worked with me at Device Research Team, Semiconductor R&D center.

I would like to thank master course's advisors in Kyunghee University, Prof. Hosun Lee and Prof. Suk-ho Choi for opening my career as a researcher in this field.

Finally, there are no words in the world to express my deepest gratitude to my parents, my brother and my sister in law. Their continuous love, sacrifice, support, blessings and encouragement guided my life even when I got lost in darkness and despair. I also thank especially to my grandparents, uncles and aunts for the wonderful memories and teachings in my childhood.

VITA

1992-1998	B.S., Physics Kyunghee University, Yong-in, Korea
1998-2000	M.S., Physics Kyunghee University, Yong-in, Korea

PUBLICATIONS AND PRESENTATIONS

S. M. Kim, E. B. Song, S. Lee, J. Zhu, D. H. Seo, M. Mecklenburg, S. Seo, and K. L. Wang
"Transparent and Flexible Graphene Charge-Trap Memory"
ACS Nano, (published online) August 13, 2012
http://pubs.acs.org/doi/abs/10.1021/nn302193q

S. M. Kim, E. B. Song, S. Seo, D. H. Seo, Y. Hwang, R. Candler and K. L.Wang
"Suspended multi-layer graphene beam electromechanical switch with abrupt on-off characteristics and minimal leakage current,"
Applied Physics Letters, 99:023103, 2011

S. M. Kim, E. B. Song, S. Lee, J. Zhou, S. Seo, D. H. Seo and K. L. Wang.,
"Flexible and Transparent Memory"
IEEE International Memory Workshop 2012, Milan, Italy

S. M. Kim, S. Seo, E. B. Song, D. H. Seo, H. Seok, and K. L. Wang.,
Graphene-Based Embedded-Oxide-Trap Memory (gEOTM) for Flexible Electronics Application
IEEE Ultimate Integration on Silicon 2012, Grenoble, France

S. M. Kim, S. Seo, E. B. Song, D. H. Seo, H. Seok, and K. L. Wang.,
"Non-Volatile Graphene channel Memory (NVGM) for flexible electronics and 3D multi-stack ultra-high-density data storages"
IEEE VLSI Technology Symposium 2011, Kyoto, Japan

S. M. Kim, E. B. Song, S. Seo, D. H. Seo, H. Seok, and K. L. Wang.,
(Invited) "Non-Volatile Graphene channel Memory (NVGM) for flexible electronics and 3D multi-stack ultra-high-density data storages "
SID International Display Workshop 2011, Nagoya, Japan

S. M. Kim, K. H. Cho, E. B. Song, D-W. Kim, D. Park, K. L. Wang and K. Kim.,

“Vertical Si Nano-Wire Channel 2-Bit Non-Volatile Memory (V2M) for High Density Flash Cell Application”
IEEE Silicon Nanoelectronics Workshop 2009, Kyoto, Japan

Y. Hwang, **S. Kim** and R. N. Candler,
“Receptor-Coated Porous Silicon Resonator for Enhanced Sensitivity of Vapor Detection”
Joint Conference of the International Frequency Control Symposium & European Frequency and Time Forum, 2011

S. Lee, E. B. Song, **S. M. Kim**, D. H. Seo, S. Seo, T. W. Kang, and K. L. Wang.,
“Impact of gate work-function on memory characteristics in $Al_2O_3/HfO_x/Al_2O_3$/graphene charge-trap memory devices,”
Applied Physics Letters.100: 023109, 2012

E. B. Song, B. Lian, **S. M. Kim**, S. Lee, T-K. Chung, M. Wang, C. Zeng, G. Xu, K. Wong, Y. Zhou, H. I. Rasool, D. H. Seo, H-J.Chung, J. Heo, S.Seo and K. L. Wang.,
“Robust Bi-Stable Memory Operation in Single-Layer Graphene Ferroelectric Memory,”
Applied Physics Letters, 99: 0421091, 2011

J. Kim, A. J. Hong, **S. M. Kim**, K. Shin, E. B. Song, Y. Hwang, F. Xiu, K. Galatsis, C. O. Chui, R. N. Candler, S. Choi, J –T. Moon, and K. L. Wang.,
"Stacked Memory Device on Logic 3D Technology for Ultra High Density Data Storage,"
IOP Nanotechnology, 22: 254006, 2011

E. B. Song, B. Lian, G. Xu, B. Yuan, C. Zeng, A. Chen, M. Wang, **S. M. Kim**, M. Lang, Y. Zhou and K. L. Wang
“Visibility and Raman spectroscopy of mono and bilayer grapheme on crystalline silicon”
Applied Physics Letters, 96:081911, 2010

J. Kim, A. J. Hong, **S. M. Kim**, E. B. Song, J. H. Park, J. Han, S. Choi, D. Jang, J. T. Moon, and K. L .Wang
“Novel Vertical-Stacked-Array-Transistor for ultra-high-density and cost-effective NAND Flash memory devices and SSD ”
VLSI Technology Symposium 2009, Kyoto, Japan.

Chapter 1

Introduction

1.1. Overview: Non-Volatile Memory (NVM) technology

Memory device has become ubiquitous in our daily lives, inside of computers, mobile phones, USB drives, Solid State Drives, etc. These memories have two main categories, volatile and non-volatile. Volatile memory needs constant power input to maintain the stored data, in other words, the data is lost as soon as the input power is turned off. On the other hand, non-volatile memory retains the data even if the power is turned off. Flash memory is the most suitable structure for non-volatile memory because one cell consists of only one transistor. Although, flash memory has been first developed in the 1980s, the use of it has grown rapidly in recent years as it forms the basis of many memory products. It is now widely used and is one of the most important memory technology for medium term storage.[1,2] Flash memory devices have been aggressively scaled down, increasing memory capacity for the last several decades. In this chapter, a brief overview of flash memory and challenges in scaling will be provided.

1.2. The basic operation principle and history of NVM device

Flash memory cell transistor has a similar structure to a standard MOSFET, except the charge storage layer. Every memory cell contains a control gate (CG), a control oxide (CO), and a charge storage layer that stores data. The charge storage layer is sandwiched

between the CG and the MOSFET channel. Because the charge storage layer is electrically isolated by adjacent insulating layers, the trapped and stored charges are retained when the input power is removed. The stored charge screens the electric field from the CG, which shifts the threshold voltage (V_{TH}) of the MOSFET.

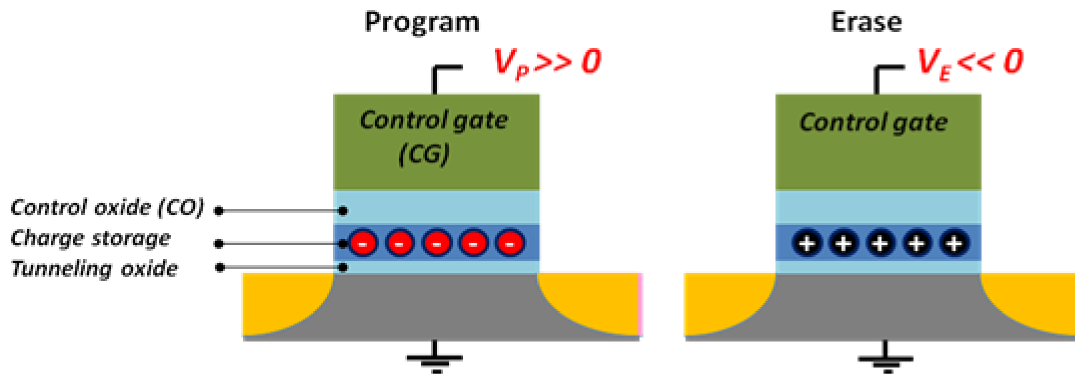


Figure 1.1. Basic operating principle of nonvolatile semiconductor memory: the storage of charges in the gate insulator of a MOSFET.

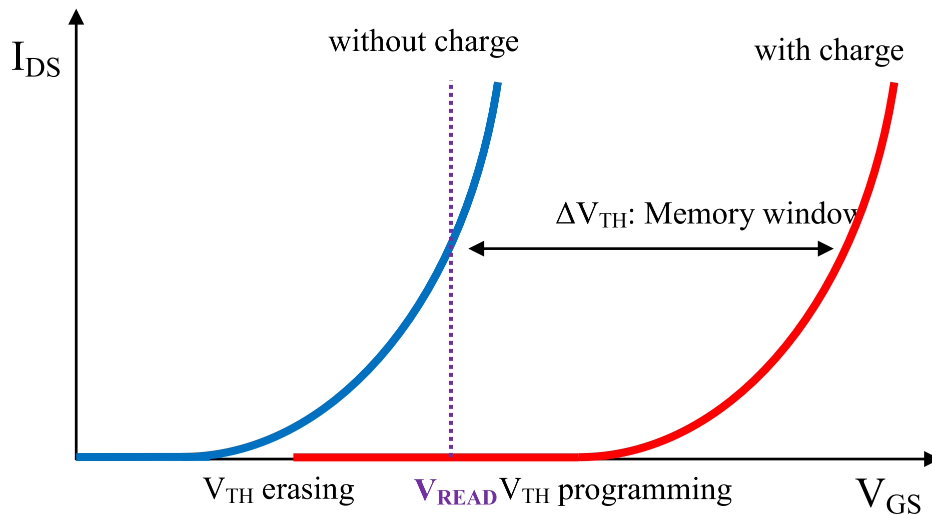


Figure 1.2 Influence of charges in the charge storage layer on the threshold characteristics of an n-channel MOSFET.[5] The stored charge screens the electric field from the CG, which shifts the threshold voltage (V_{TH}) of the MOSFET. The data stored in the charge storage layer is detected by applying a gate voltage V_{READ}, which has a value in between the two possible V_{TH}s.

The threshold voltage of a MOSFET transistor is given by

$$V_{TH} = 2\Phi_F + \Phi_{ms} - \frac{Q_I}{C_I} - \frac{Q_D}{C_I} - \frac{Q_T}{\epsilon_I} d_I \qquad \text{(Eq. 1.1)}$$

where Φ_{ms}= the work function difference between the gate electrode and the channel material [4,5]

Φ_F= the Fermi-level of the semiconductor

Q_I= the fixed charge at the silicon/insulator interface

Q_D = the charge in the silicon depletion layer

Q_T = the charge stored in the gate insulator at a distance d_I from the gate

C_I = the capacitance of the insulator layer

ϵ_I = the dielectric constant of the insulator

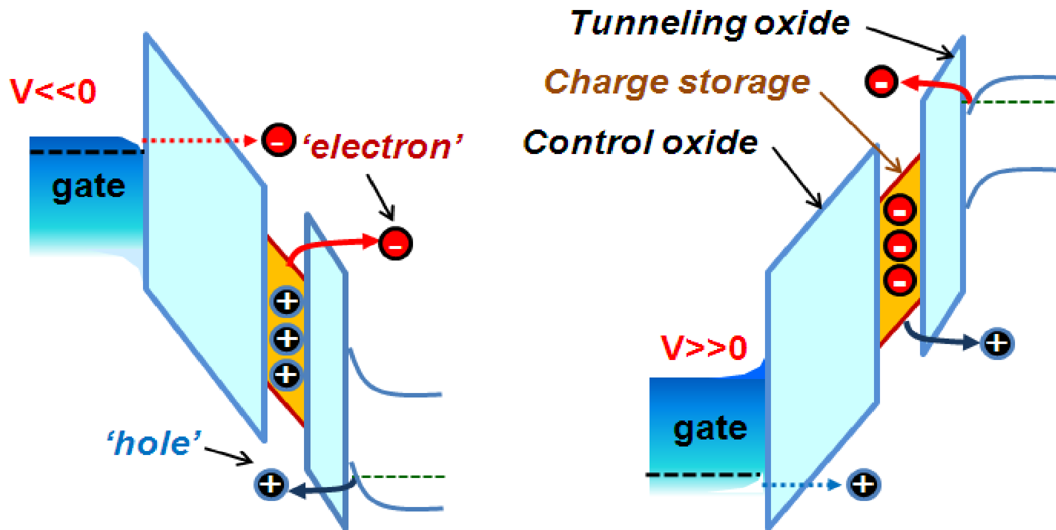


Figure 1.3 Schematic energy band diagram of a charge trap non-volatile memory. (a) A Programming Operation. Positive bias is applied on a gate and induces FN tunneling current by injecting electrons from the channel to the nitride film, (b) An Erasing Operation. Positive bias is applied on a body electrode (or negative bias on a gate) and allows electrons to go back to the channel.

Thus, the threshold voltage shift, created from the stored charge Q_T is given by

$$\Delta V_{TH} = -\frac{Q_T}{\epsilon_I} d_I \qquad \text{(Eq. 1.2)}$$

The data stored in the charge storage layer is detected by applying a gate voltage V_{READ}, which has a value in between the two possible V_{TH}s. In one state, the transistor is in the on state, while, in the other, the transistor is in the off state. Figure 1.3 shows the band-diagrams to illustrate the programming/erase operations. For the programming operation, when a high programming voltage (or V_P) is applied on the gate, the energy band slope of the tunnel oxide layer increases, and the edge of the barrier becomes very thin. As a result, Fowler- Nordheim (FN) tunneling of electrons from the substrate to the storage layer takes place. [1,5] Electron stored inside the charge storage layer by this programming operation makes the Fermi level of the storage layer higher than those of the gate and the substrate. For erase operation, a negative voltage bias (or V_E) is applied on the CG, and allows back tunneling of stored electrons as well as injection of holes from the channel.

1.3. Scaling of flash memory

Silicon based FETs revolutionized the modern integrated circuit technology. The size of the transistors has consistently been miniaturized to enhance operation speed and to maximize packing density. Classical scaling of transistor follows the Moore's law that states the number of transistors on a chip doubles every 2 years. The state-of-art micro processor technology, Intel 'Ivy Bridge' microprocessor, presented at 2011 has a transistor with a channel length of 22 nm. Furthermore, MOSFET scaling is heading towards to 10nm technology node.[6]

Since the 256Mb-NAND flash memory chips were announced in the beginning of 21st century, the capacity of flash memory has been doubling every year.[3] From 2006, NAND flash memory has been the most scaled device. Currently, NAND flash memory is in the 20nm technology node. If this trend continues, the classical scaling of NAND flash cell is expected to be faced with physical limits in 2015. In order to keep scaling memory devices beyond this physical scaling limit, memory industries have proposed 3-dimensionally stacked (3D) memory structures.[7,8] Most of 3D multi stack flash memory cells have a poly-Si thin film channel. To resolve the low mobility of poly-Si channel, Si re-crystallization processes, such as laser annealing or solid phase epitaxy (SPE) processes are being introduced. But unfortunately, those methods have not been matured enough to turn poly-Si film into perfect single crystalline silicon.

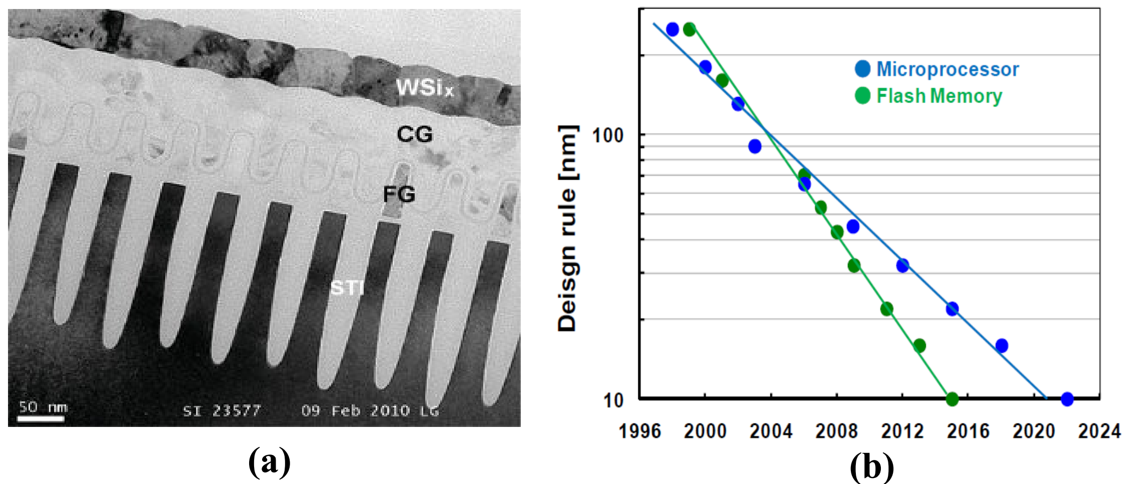
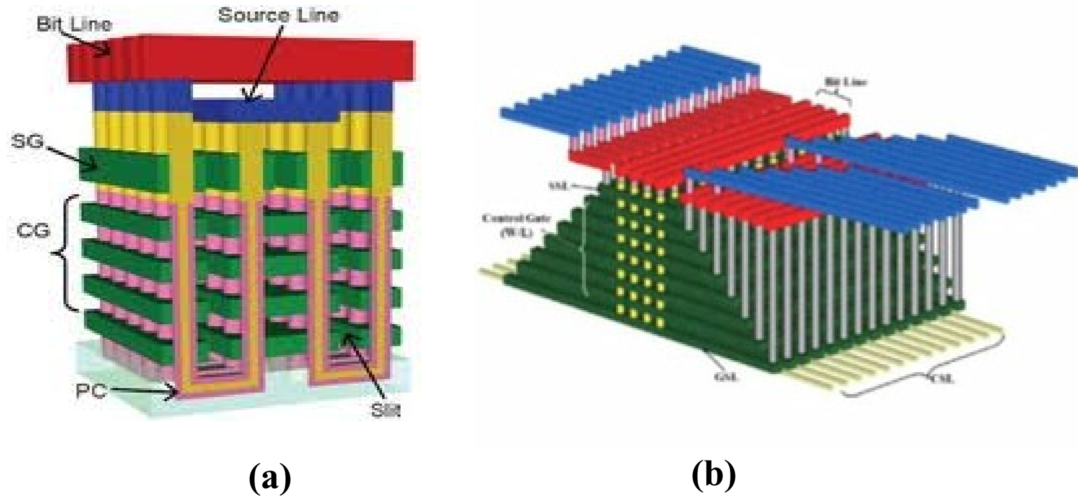


Figure 1.4 (a) NAND flash memory cell (Intel–Micron technology 2010), (b) recent scaling trend of microprocessor and flash memory. Currently, NAND flash memory is in the 20nm technology node. If this trend continues, the classical scaling of NAND flash cell is expected to be faced with physical limits in 2015



(a) **(b)**

Figure 1.5 3D NAND flash cell structures proposed by Toshiba and Samsung. [7.8]

Meanwhile, Memory companies have made wafer size transitions because of the overall cost benefits (i.e. increase in the number of dice per wafer). But this wafer size transition also has physical limits and needs huge investments to build production facilities. The second motivation of this research is to replace Si substrates with non-Si substrates, such as glass or plastic film, which has much larger size than silicon wafers. This will reduce the production cost and maximize the memory capacity.

1.4. Charge trap memory (CTF)

Charge trap memory is considered as a promising alternative to the conventional floating gate non-volatile memory because the adoption of a charge-trap layer can be a solution to relieve all capacitive coupling effects between the neighboring cell transistors and to reduce the height of gate stacks. Since several different types of charge-trap memories have been proposed, they are reviewed in this section.

MNOS

The metal-nitride-oxide-silicon (MNOS) devices were invented in 1967 by Wenger et al., which is the first type of charge trapping NVM.[9] In case of NVM with conductive floating gate, if there were a leakage path in the SiO_2 that allowed charges to escape, all of the charge on the floating gate would be lost along with the memory state.[12,13]. To alleviate this problem, for MNOS, the floating gate is replaced by a nonconductive Si_3N_4 film with discrete and deep traps. The charges injected by tunneling from the channel are stored in the defects sites of the Si_3N_4 data storage layer, which is sandwiched between a SiO_2 tunneling oxide and a control metal gate. The MNOS structure has a couple of challenges; charge loss through leakage from the Si_3N_4 to the metal gate electrode, and high program/erase voltages due to the thick nitride films. [10]

SONOS

To overcome the problems of MNOS structure, the SONOS (Poly-Si gate-$Si0_2$-SiN-$Si0_2$-Si substrate) structure has been proposed.[11] This structure is different from the MNOS structure by an insertion of an additional SiO_2 control oxide layer between the Si_3N_4 charge storage layer and the gate electrode. The control oxide blocks the stored charge in the Si_3N_4 and prevents data loss resulting from charge leakage into the gate electrode. Adoption of the control oxide effectively inhibits not only charge loss from the SiN charge storage layer, but also blocks charge-injection from the metal gate. This results in a higher trapping efficiency and relieves the problem caused by the thin SiN charge storage layer.[14] Even though retention characteristic and performance of SONOS memory is not sufficient to be used as a commercial product; it is a significant

improvement towards the mass production of CTF memory. Today, SONOS memory has been considered as a promising alternative to conventional floating gate NVM. Because, as NAND flash scales down, the space between cell transistors are narrowed, and therefore, capacitive coupling between the drain and floating-gate layer begins to affect the floating-gate nonvolatile memory device characteristics. The SONOS with a very thin Si_3N_4 data storage is inherently immune to this capacitive coupling issue, and enables the adoption of a thin gate stack.

TANOS

As devices are scaled down, SONOS is free from the critical issues describe above. However, the usage of a thin tunnel oxide is a road-block for the SONOS device to become a high-density NAND flash memory. The SANOS (Poly Si-Ai_20_3-SiN-$Si0_2$-Si substrate) structure appeared to enhance the programming and erase efficiency by maximizing the capacitance of the blocking layer. [15] However, the electron tunneling from the gate to the trapping layer becomes severe with the Al_2O_3 blocking layer because the barrier height of AI_2O_3 is not significantly higher than that of Si_3N_4 charge storage layer.

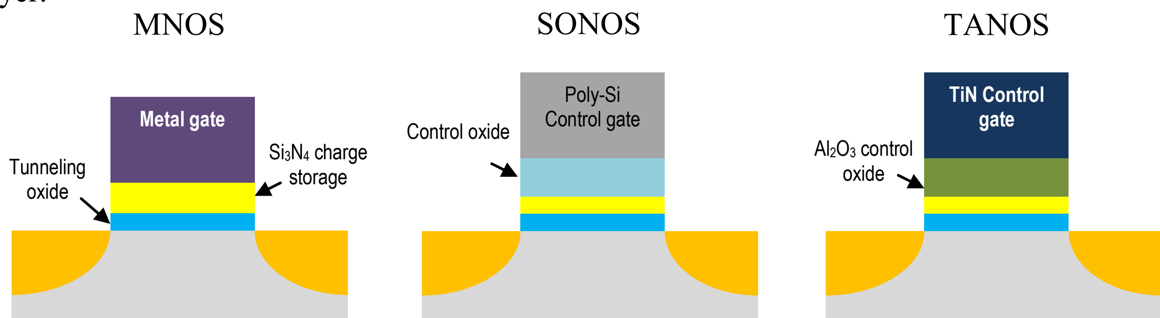


Figure 1.6 Structures of the charge-trapping based nonvolatile memory transistors. Today, TANOS memory cell is considered the most practical evolution of the floating-gate Flash cell for NAND architectures.

Therefore, a metal gate with high work function (Φ_M) is required to improve the performance.[16-18] Today, the TANOS memory cell is considered the most practical evolution of the floating-gate Flash cell for NAND architectures.

1.5. Carbon based materials for flexible and transparent electronics.

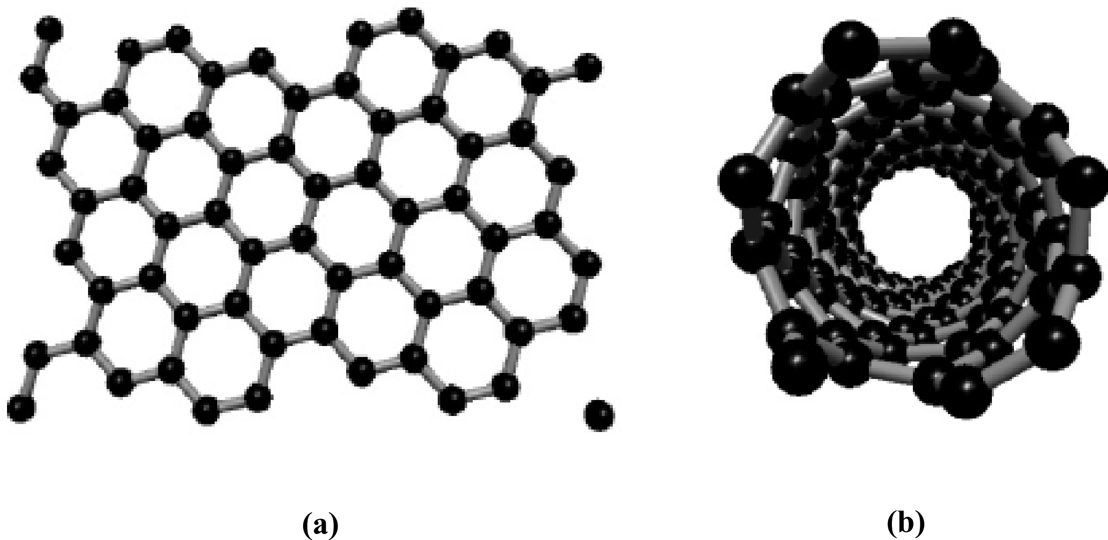
Si technology has been the main stream of integrated circuit technology for several decades. But for flexible and transparent electronic circuits, Si is not suitable as a channel material because it is very rigid and opaque, and furthermore a small force can cause it to crack. Carbon is one of the most abundant materials on earth, and has been used in most industrial products. Carbon nanotubes (CNTs) and Graphene, due to their extremely desirable electrical, mechanical and optical properties have been considered for their applicability in flexible and transparent electronics.

CNTs

Due to their excellent electrical and thermal properties, carbon nanotubes (CNTs) have been considered for a promising channel material for VLSI circuit [19-23]. CNTs are defined as sheets of graphene rolled up as hollow cylinders. CNTs can be classified into two groups: single-walled (SWNTs) and multi-walled (MWNTs). The electrical properties of the SWNTs can be either metallic or semiconducting depending on the direction in which they get rolled up.[24,25] However, MWNTs are always metallic materials. Although, SWNTs have good semiconducting properties with extremely high electron mobility, VLSI circuits with CNT channels are still far from mass production due to the difficulties in controlling the shape and the position of each CNTs.

Graphene

Since graphene was experimentally discovered in 2004, this two dimensional sheet of carbon has been heavily researched by many scientists.[26] Similar to carbon nanotubes, graphene has excellent electrical, mechanical and thermal properties. Unique properties of graphene have been studied for the application of transparent electrodes, field-effect transistors, energy-storage materials, digital and analog integrated circuits, integrated circuit interconnects, solar cells, ultra-capacitors, and electro-mechanical sensors such as single molecule detectors and biosensors. [27-29] The electrical properties of graphene, such as the very high electron mobility at room temperature and the symmetry of carrier mobility between electrons and holes are highly attractive to be applied in high-performance electronic devices. [30-31]



(a) **(b)**

Figure 1.7 (a) Graphene, which holds similar electrical and mechanical properties compared to (b)Carbon nano-tubes (CNT), have also been considered as a channel material for flexible electronics. [56]

1.6. Graphene Fabrication

Exfoliation

The most common method of graphene fabrication is exfoliation. This well-known method of making graphene sheets is also called the "Scotch Tape" method, which is simply peeling off the graphene sheets from a graphite flake with the use of scotch tape, and sticking that tape on top of the substrate.[26] While this exfoliation technique produces high-quality graphene, this method is limited to small scale devices and unsuitable for mass production for graphene based electronics due to the difficulties in controlling the position and thickness of graphene sheets. Fig 1.7 illustrates the optical image of an exfoliated graphene depending on different wavelengths of light.[32]

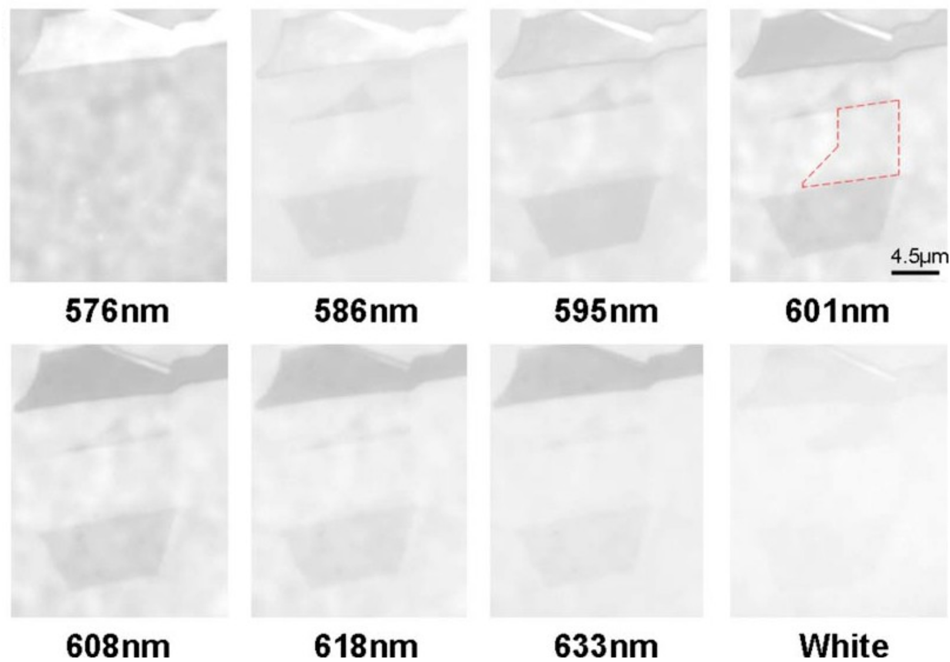


Figure 1.8 Optical images of exfoliated graphene flakes on SiO_2 thin films depending on different wavelengths of light. [32]

Epitaxial Growth

Another attractive method is to heat SiC in vacuum at temperatures around 1300°C. When SiC is heated, sublimation of Si takes place, leaving behind carbon atoms, which assemble into graphene layers. This technology seems to have the greatest potential for mass production of graphene. But epitaxial growth of graphene has difficulties in controlling the number of layers, and graphitization of the SiC induces surface roughening that limits lateral extension of graphene crystallites and degrades carrier mobility.[33,34] Furthermore, isolating single sheets from SiC substrate needs sophisticated processes and requires additional lithography steps to pattern electrostatic gates on top of the graphene.

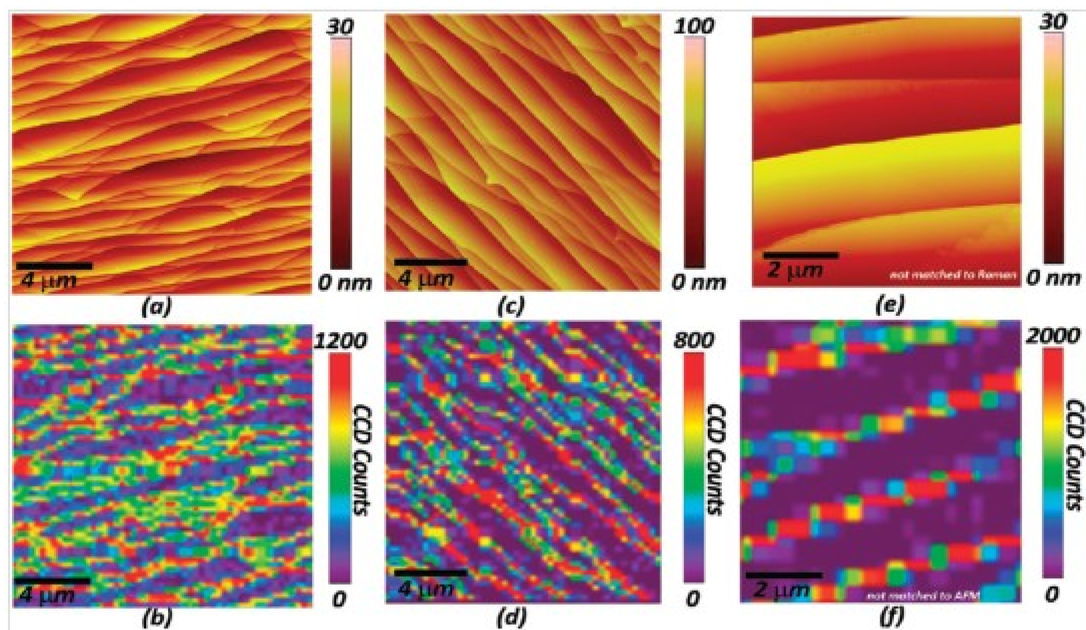


Figure 1.9 Atomic force microscopy (a,c,d) and Raman topography map of the 2D Raman peak intensity as a function of x/y position (b,d,e) of SiC substrates graphitized at (a,b) 1225 °C, (c,d) 1325 °C and (e,f) 1425 °C.[34] Two-dimensional Raman peak near the wavelength of 2730cm^{-1} is used to rapidly identify the presence of graphene. Epitaxial growth of graphene has difficulties in controlling the number of layers and surface roughness.

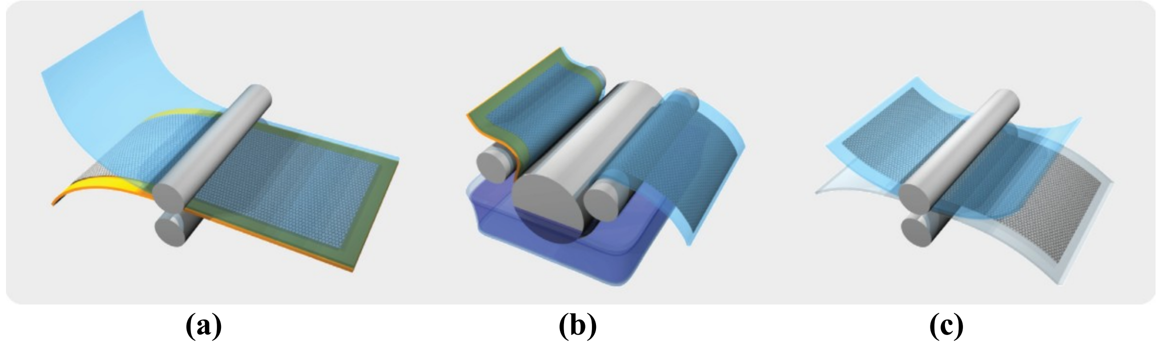
CVD growth

A more productive way to grow graphene is chemical vapor deposition (CVD). In CVD graphene growth, a metal substrate, such as copper (Cu) and nickel (Ni) are loaded into a vacuum chamber of a furnace and heated under temperatures around 1000°C.[35,37] Methane (CH_4) and hydrogen (H_2) gases are then flowed into the furnace. Carbon atoms from the methane are deposited onto the surface of the metal through chemical adsorption. Nickel absorbs carbon more than copper, and leads to an overabundance of carbon, which forms into multi-layer graphene sheets instead of a single graphene sheet.[36,37] Copper attracts less carbon and the carbon atoms can only be formed with open bonding sites at the Cu surface. Therefore different from other metals, Cu foils can be used in CVD graphene for larger scale growth than wafer size.[35]

Large-scale graphene synthesis and transfer

An advantage to CVD graphene growth is the ability to transfer the graphene to an arbitrary substrate. Recently, large scale graphene growth and transfer technology has been introduced opening up possibilities for large scale production of graphene devices.[35] A CVD grown wafer-scale graphene film can be transferred to target substrates utilizing poly-di-methyl-siloxane (PDMS), spin-coated poly-methyl-methacrylate (PMMA) polymer films as support materials.[38-40] However, the scale is also limited below the size of wafers because the PDMS and PMMA layers have to be spin-coated on flat and rigid substrates. In order to overcome the limitation of previous methods,[35] Samsung developed a roll-to-roll transfer method utilizing thermal release tapes as shown in figure

1.10.



(a) **(b)** **(c)**

Figure 1.10 Schematic of the roll-based production of graphene films grown on a copper foil. The process includes adhesion of polymer supports, copper foil. The processes are divided into three steps: (a) the adhesion of polymer supports, (b) copper etching and (c) transfer to the target substrate.[35]

1.7. Electrical Properties of Graphene

The electronic properties of graphene are determined by the bonding π- and antibonding π*-orbitals, which form electronic valence and conduction bands. The tight-binding approach, which considers only the first nearest neighbor interaction, provides the dispersion relation of the electrons near the K / K ′ points: [41, 42]

$$E_{\pm}(\vec{k}) = \pm t\sqrt{1 + 4\cos\frac{\sqrt{3}k_x a}{2}\cos\frac{k_y a}{2} + 4\cos^2\frac{k_y a}{2}} \qquad \text{(Eq. 1.3)}$$

where $a = \sqrt{3}a_{cc}$, a_{cc}: carbon-carbon bonding length (0.142nm), and t: transfer integral.

The positive part of the energy dispersion describes the π* anti-bonding energy band and the negative part is the π bonding energy band. Interestingly, the π* anti-bonding and

π bonding bands are degenerate at the K points where the Fermi energy passes. By expanding Equation (1) near the K /K ′ points, the dispersion relation can be obtained as

$$E = \hbar v_F k \qquad \text{(Eq. 1.4)}$$

where ħ is the reduced Planck's constant and v_F (≈106 m/s) is the electron Fermi velocity in graphene.

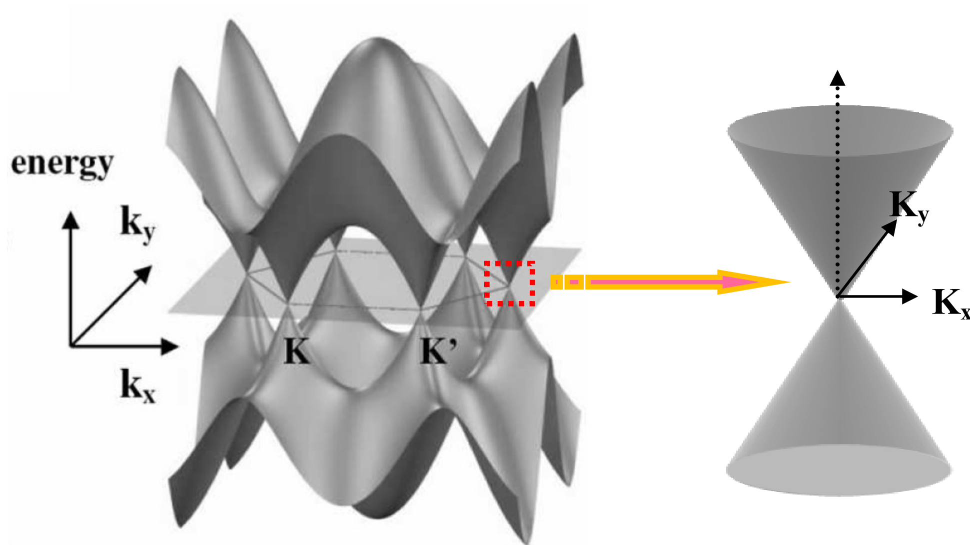


Figure 1.11 Graphene band structure showing the nonequivalent K and K valleys. In the figure the Fermi energy (transparent plane) is located at the Dirac neutrality points, which separate the hole states below them from the electron states above them. Inset shows the energy dispersion relations along the high symmetry axes near the Dirac point. [27,28,42]

Figure 1.11 shows graphene valence (π) and conduction (π*) bands and the energy of the π (π*) and σ (σ*) band in the first Brillouin zone.[27,28] The unique electronic band dispersion leads to the description of carriers in graphene as "massless Dirac fermions".

The six points where the cones touch are referred to as the “Dirac” points. The unusual feature in electronic properties of graphene arises from the linear dispersion relation near the Dirac point. This leads to new fascinating effects, such as electron-hole symmetric conductance, high carrier mobilities, ballistic transport, and anomalous quantum Hall effects.[43-45]

Graphene channel FET

The outstanding electrical conductivity of graphene has attracted interest from scientists and engineers to replace silicon in the next generation of semiconductors devices. Since the energy band of graphene is symmetric at the Dirac point, (i.e. the point $E = E_{2p} = 0$) the density of states at the Fermi level is exactly zero and graphene exhibits semimetallic property from the half filling of the band. By applying a suitable “gate” voltage to the graphene relative to the substrate, we induce a nonzero charge, which is equivalent to injecting electrons in the upper half or holes in the lower half of the Dirac cones. This effect is known as the electric-field effect (Figure 1.12).

For commercial device applications, a strong gate dependence of the graphene channel is required for transistor applications. Unfortunately, graphene is a zero band gap material. Therefore, a graphene channel transistor has a small on/off ratio and a small conductivity change under the gate voltage control. Several methods can be proposed to improve the On/Off ratio. For example, the low On/Off ratio can be increased by creating an energy band-gap (E_g) in this otherwise gapless material through quantum confinement effects (E_g

=50 meV) in graphene nanoribbons[46] and field-induced effects ($E_g \leq 250$meV) in bi or trilayer graphene.[47,48]

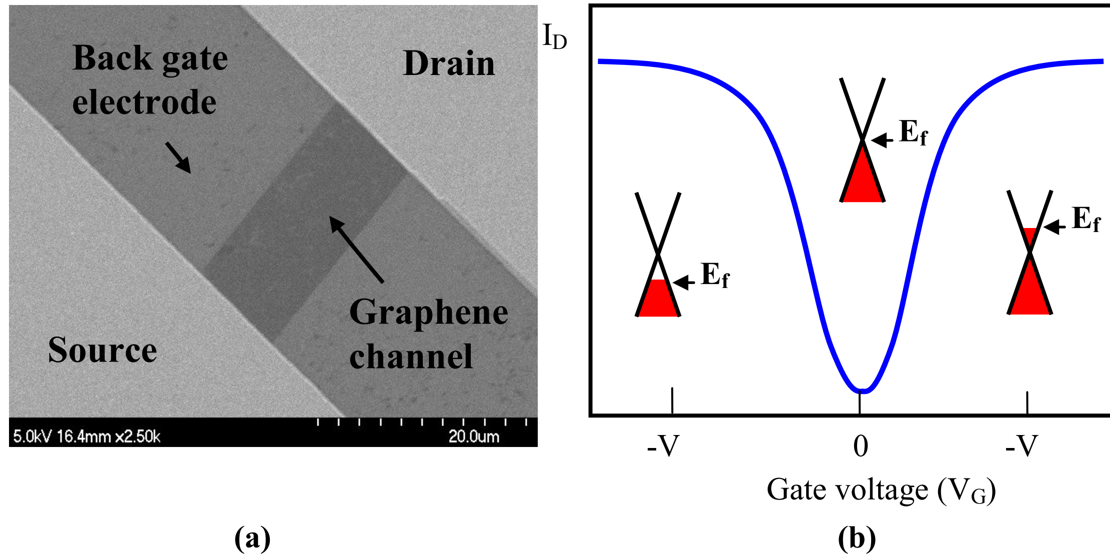


Figure 1.12 (a) Scanning Electron Micrograph image of back gated graphene channel transistor. (b) Typical Drain current I_D to gate voltage V_G characteristic of graphene channel transistor, Conical low-energy spectrum E(k), indicating changes in the position of the Fermi energy E_F with changing V_G

1.8. Mechanical property of Graphene

Graphene is a 2-dimensional carbon sheet, which has strong mechanical stiffness and high electron mobility even with a single atomic thickness. A single layer graphene sheet has a honeycomb structure with 3-covalent bonds with neighboring atoms (Figure 1. 13). The mechanical strength and thermal properties of the covalent bonds between the carbon atoms are nearly equivalent to that of diamond. From the mechanical point of view, graphene is one of the strongest materials ever discovered with a breaking strength

of over 200 times that of steel.[49] Furthermore, it is thermally stable to temperatures up to 500 °C in air, being inert to most gases.

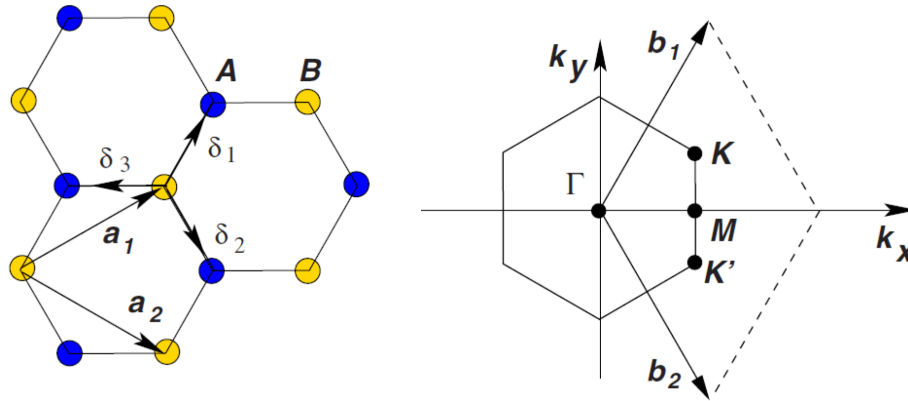


Figure 1.13 (a) Honeycomb lattice of graphene and (b) its Brillouin zone. Left: lattice structure of graphene (**a**1 and **a**2 are the lattice unit vectors, and i, i=1, 2, 3 are the nearest-neighbor vectors). [42]

Due to the unique chemical bonding and physical structure, graphene has much higher value of the Young modulus and Poisson ratio compared to that of silicon even with its atomic thickness. (Table.1) This higher value allows graphene application for high speed MEMS with several times larger resonant frequency and operation speed than silicon MEMS under the same dimensions. Since Bunch et al. have demonstrated graphene electromechanical resonators exhibiting extremely high frequency and its sensor application with extremely high sensitivities,[53] interest in graphene based MEMS/NEMS has been growing fast. Electronic and mechanical properties of graphene might enable mechanical systems to be merged into electronic circuits with superior functionality.

Material	Young's Modulus (TPa)	Mobility $cm^2V^{-1}S(300^\circ K)$	Thermal conductivity $Wm^{-1}K^{-1}$	Poisson ratio
Silicon	~0.13 [54]	≤1400 [55]	~1500 [56]	~0.28 [56]
Graphene (SLG)	~1 [3]	>15000 [43]	~5000 [52]	0.165 [49]

Table 1: Materials properties of graphene and bulk silicon.

1.9. Flexible electronics

Electronic devices have been changing its appearance responding to customer's demands. In the near future, electronic devices are projected to be flexible and wearable because people have dreamed of using electronic circuits that would bend and stretch, rather than being confined to rigid chips and boards. Flexible circuits are also promising for use in wearable electronics devices, low cost sensors, and other disposable electronic devices. Furthermore, flexible electronics circuits would be able to deliver innovative designs of electronic devices that rigid circuits cannot. The market for flexible electronics is expected to be growing exponentially in the next decade. Smaller, lighter, and faster flexible electronic devices require multiple modules, such as logic, analog, and memory to be built in the same flexible substrate. Many electronic companies have demonstrated flexible electronic devices, but most of them are not fully flexible because the other modules such as memory and logic are not flexible yet.

In this thesis, we concentrate on how to achieve high density memory cell on flexible and transparent substrate. To prevent the thermal deformation of the flexible substrate, samples were fabricated with non-Si materials using newly developed low temperature processes. We will present the first non-volatile memory device based on graphene channel thin-film transistors and circuits on a Polyethylene naphtalate (PEN) substrate. We will also discuss the relationship between the device electronic characteristics and mechanical strain in flexible memory devices.

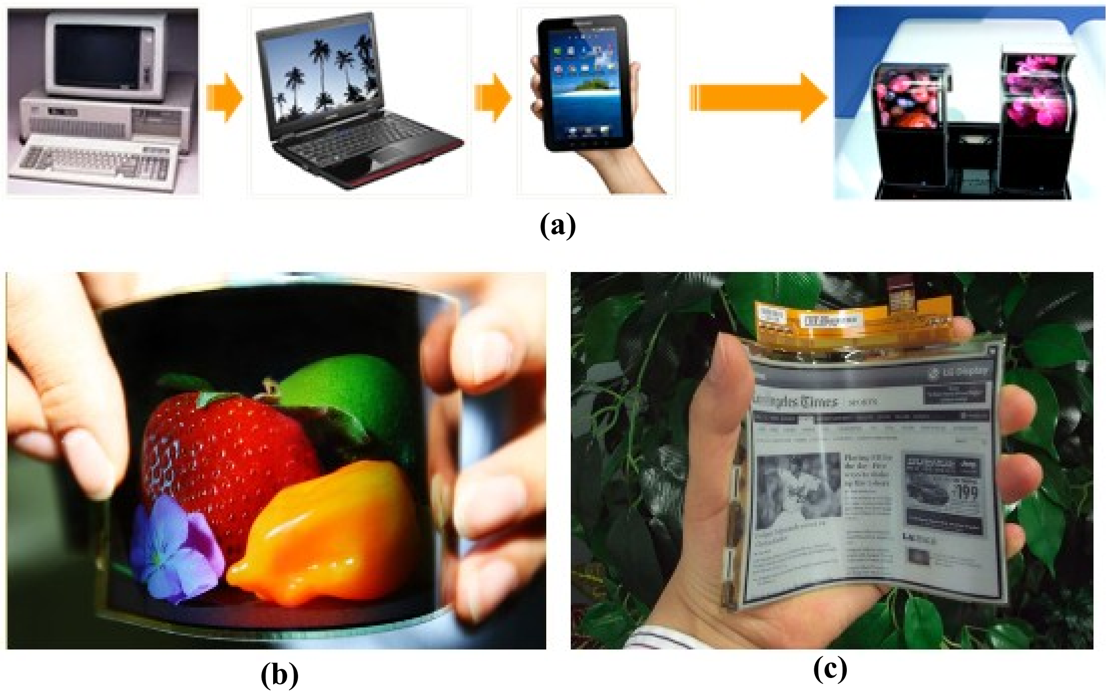


Figure 1.14 (a) Evolution of personal computers responding to customer's demands. Flexible electronic devices demonstrate by (b) Samsung Mobile Display and (c) LG electronics. Electronic devices have been changing its appearance responding to customer's demands. In the near future, electronic devices are projected to be flexible and wearable.

1.10 Reference

1. R. Bez, E. Camerlenghi, A. Modelli, and A. Visconti, "Introduction to flash memory," Proceedings of the IEEE, vol. 91, pp. 489-502,(2003)
2. D. C. Guterman, I. H. Rimawi, C. Te-Long, R. D. Halvorson, and D. J. McElroy, "An electrically alterable nonvolatile memory cell using a floating-gate structure," Electron Devices, IEEE Transactions on, vol. 26, pp. 576-586, (1979)
3. Kim, K. S.; Zhao, Y.; Jang, H.; Lee, S. Y.; Kim, J. M.; Kim, K. S.; Ahn, J.-H.; Kim, P.; Choi, J.-Y.; Hong, B. H., Large-Scale Pattern Growth of Graphene Films for Stretchable Transparent Electrodes. Nature **2009**, 457, 706-710.J. R. Yeargain and C. Kuo, "A high density floating-gate EEPROM cell," International Electron Devices Meeting, 1981, pp. 24-27, (1981)
4. J. R. Yeargain and C. Kuo, "A high density floating-gate EEPROM cell," in International Electron Devices Meeting, 1981, pp. 24-27, (1981)
5. G. Groeseneken, H. E. Maes, J. VanHoudt, and J. S. Witters, NVSM Technology, IEEE Press, Chap. 1998. [2] S. Kim and J. Lee “Flexible Organic Transistor Memory Devices” Nano Lett., 10 8), pp. 2884–2890, (2010)
6. “Intel 22nm Technology” http://www.intel.com/content/www/us/en/silicon-innovations/intel-22nm-technology
7. J. Jang, H.-S. Kim, W. Cho, H. Cho, J. Kim, S. I. Shim, Y. Jang, J.-H. Jeong, B.-K. Son, D. W. Kim, K. Kim, J.-J. Shim, J. S. Lim, K.-H. Kim, S. Y. Yi, J.-Y. Lim, D. Chung, H.-C. Moon, S. Hwang, J.-W. Lee, Y.-H. Son, U. I. Chung, and W.-S. Lee, "Vertical cell array using TCAT(Terabit Cell Array Transistor) technology for ultra high density NAND flash memory," Tech. Digest of Symposium on VLSI Technology, pp. 192-193.(2009)
8. H. Tanaka, M. Kido, K. Yahashi, M. Oomura, R. Katsumata, M. Kito, Y Fukuzumi, M. Sato, Y Nagata, Y Matsuoka, Y Iwata, H. Aochi, and A. Nitayama,"Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory," Tech. Digest Symposium on VLSI Technology, pp. 14-15, (2007)

9. Y.Yatsuda, T.Hagiwara, S.Minami, R.Kondo, K.Uchida, and K. Uchiumi., “Scaling down MNOS nonvolatile memory devices,” Jap. J.Appl.Phys. vol.21,S21-1, p.85, (1982)
10. T.Hagiwara,Y.Yatsuda,S.Minami,S.Naketani,K.Ushida, and T.Yasui, “A 5V only 64k MNOS memory device for highly integrated byte erasable 5V only EEPROMs,” Tech. Digest of International Electron Devices Meeting., pp.733-7337, (1982)
11. J. Bu and M. H. White, "Design considerations in scaled SONOS nonvolatile memory devices," Solid State Electronics, vol. 45, pp. 113-120,(2001)
12. D.Adams, J.Murray, and M.H.White, “SONOS Nonvolatile Semiconductor Memories for Space and Military Applications”, Proc. of NVMTS, San Diego, CA, pp.92-95 (2001)
13. J.D.Lee, et al,, “Effects of floating-gate interference on NAND flash memory cell operations,” IEEE Electron Device Letters, vlo. 23, pp., 264- 266, (2002)
14. S. Wrazien, Y. Zhao, J. Krayer, and M. White, "Characterization of SONOS oxynitride nonvolatile semiconductor memory devices," Solid State Electronics, vol. 47, pp. 885-891, (2003)
15. C.-H. Lee, S.-H. Hur, Y.-C. Shin, J.-H. Choi, D.-G. Park, and K. Kim, "Charge trapping device structure of Si02/SiN/high-k dielectric AI_2O_3 for high-density flash memory," Appl. Phys. Lett, vol.86, p.152908, (2005)
16. S. Jeon, J.H. Han, J. Lee, S. Choi, H. Hwang, and C. Kim, "Impact of Metal Work Function on Memory Properties of Charge-Trap Flash Memory Devices Using Fowler-Nordheim P/E Mode," IEEE Elect. Devi. Lett., vol.27, pp.486-488, (2006)
17. S. Jeon, J.H. Han, J. Lee, S. Choi, H. Hwang, and C. Kim, "High work-function metal gate and high-k dielectrics for charge trap flash memory device applications," IEEE Trans. Elect. Devi., vol.52, pp.2654-2659, (2005)
18. D.C. Gilmer, N. Goel, S. Verma, H. Park, C. Park, G. Bersuker, P.D. Kirsch, K.C. Saraswat, R. Jammy, "Band engineered tunnel oxides for improved TANOS-type

flash program/erase with good retention and 100K cycle endurance," Tech. Dig. of VLSI-TSA, pp. 156-157, (2009)

19. A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. Dai. Ballistic car- bon nanotube Field-effect transistors. Nature, 424(6949):654,(2003)
20. S. J. Tans, R. M Verschueren, and C. Dekker. Room temperature transistor based on a single carbon nanotube. Nature, 393(6680):4952,(1998)
21. A. Bachtold, P. Hadley, T. Nakanishi, and C. Dekker. “Logic circuits based on carbon nanotubes,” Physica E, 16(1):pp. 42-46, (2003)
22. K. Ishibashi, M. Suzuki, T. Ida, and Y. Aoyagi. Formation of coupled quantum dots in single-wall carbon nanotubes. Appl. Phys. Lett., 79(12):1864 (2001)
23. S. Rosenblatt, Y. Yaish, J. Park, J. Gore, V. Sazonova, and P. L. McEuen. High performance electrolyte gated carbon nanotube tran-sistors. Nano Lett., 2(8):PP.869-872,(2002)
24. S. J. Wind, J. Appenzeller, R. Martel, V. Derycke, and P. Avouris. Fabrication and electrical characterization of top gate single-wall carbon nanotube field effect transistors. J. Vac. Sci. Technol. B, 20(6): PP. 2798-2801, (2002)
25. R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and Ph. Avouris. Single-and multi-wall carbon nanotube field effect transistors. Appl. Phys. Lett., 73(17):2447(1998)
26. K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva and A. A. Firsov., "Electric Field Effect in Atomically Thin Carbon Films" Science 22, Vol. 306 no. 5696 pp. 666-669, (2004)
27. A. K. Geim, and A. H. MacDonald. “Graphene: Exploring carbon flatland.” Physics Today, 60 : pp.35-41. (2007)
28. A. K. Geim, and K. S. Novoselov. “The Rise of Graphene.” Nature Material,s 6 pp. 183-191, (007).
29. L.Hu, G. Gruner, J. Gong2, C-J "CJ”Kim, and B. Hornbostel "Electrowetting devices with transparent single-walled carbon nanotube electrodes" Appl. Phys. Lett. 90, p. 093124 (2007)

30. K.I. Bolotin, K.J. Sikes, Z. Jiang, M. Klima, G. Fudenberg, J. Hone, P. Kima and H.L. Stormer, "Ultra-high electron mobility in suspended graphene." Solid State Communications, 146(9-10), pp. 351-355, (2008).
31. Xu Du, Ivan Skachko, Anthony Barker and Eva Y. Andrei. "Approaching ballistic transport in suspended graphene." Nature Nanotechnology 3(8), pp. 491-495, (2008)
32. E. B. Song, B. Lian, S. M. Kim, S. Lee, T-K. Chung, M. Wang, C. Zeng, G. Xu, K. Wong, Y. Zhou, H. I. Rasool, D. H. Seo, H-J.Chung, J. Heo, S.Seo and K. L. Wang., "Robust Bi-Stable Memory Operation in Single-Layer Graphene Ferroelectric Memory," Appl. Phy. Lett., 99 (4), pp. 0421091-0421093. (2011)
33. C. Berger, Z. Song1, X. Li, X. Wu, N. Brown, C. Naud, D. Mayou, T. Li, J. Hass, A. N. Marchenkov, E. H. Conrad, P. N. First and W. A. de Heer "Electronic Confinement and Coherence in Patterned Epitaxial Graphene" Science, Vol. 312, no. 5777, pp. 1191-1196, (2006)
34. J. Robinson, X. Weng, K. Trumbull, R. Cavalero, M. Wetherington, E. Frantz, M. LaBella, Z. Hughes, M. Fanton and D. Snyder., "Nucleation of Epitaxial Graphene on SiC(001)" ACS Nano., Vol. 4, No.1, pp 153–158.(2010)
35. S. Bae, H. Kim, Y. Lee, X. Xu, J-S. Park, Y. Zheng, J. Balakrishnan, T. Lei, H. R. Kim, Y. I. Song, Y-J. Kim, K. S. Kim, B. Özyilmaz, J-H. Ahn, B. H. Hong and S. Iijima "Roll-to-roll production of 30-inch graphene films for transparent electrodes." Nature nanotechnology, 5(8):pp.574-578, (2010)
36. S. Bhaviripudi, X. Jia, M. S. Dresselhaus, and J. Kong. " Role of kinetic factors in chemical vapor deposition synthesis of uniform large area Graphene using copper catalyst." Nano Letters, 10(10):4128-413, (2009)
37. K. S. Kim, Y. Zhao, H. Jang, S. Y. Lee, J. M. Kim, K. S. Kim, J-H. Ahn, P. Kim, J-Y. Choi, and B. H. Hong. "Large-scale pattern growth of graphene films for stretchable transparent electrodes." Nature, 457: pp.706-710, (2009)

38. Y. Lee, S. Bae, H. Jang, S. Jang, S-E. Zhu, S. H. Sim, Y. I. Song, B. H. Hong and J-H. Ahn., "Wafer-Scale Synthesis and Transfer of Graphene Films" Nano Lett., 10 (2), pp. 490–493,(2010)
39. A. Reina, X. Jia, J. Ho, D. Nezich, H. Son, V. Bulovic, M. S. Dresselhaus and J. Kong "Large Area, Few-Layer Graphene Films on Arbitrary Substrates by Chemical Vapor Deposition" Nano Letters., , 9 (1), pp.30–35,(2009)
40. X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo and R. S. Ruoff, "Large-area synthesis of high-quality and uniform graphene films on copper foils" Science, Vol. 324 no. 5932 pp. 1312-1314, (2009)
41. P. R. Wallace, "The Band Theory of Graphite" Phys. Rev. 71,pp. 622–634, 1947
42. A. H. C. Neto, F. Guinea, N. M. R. Peres, K. S. Novoselov and A. K. Geim, "The electronic properties of graphene" Review of Modern Physics. Vol.81, pp.109-162,(2009)
43. K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, M. I. Katsnelson, I. V. Grigorieva, S. V. Dubonos, & A. A. Firsov., Two-dimensional gas of massless Dirac fermions in graphene, Nature Vol. 438, pp. 197– 200. (2005)
44. Y. Zhang, Y.-W. Tan, H. L. Stormer, & P. Kim. Experimental observation of thequantum hall effect and Berry's phase in graphene, Nature Vol. 438, pp. 201–204. (2005)
45. K. S. Novoselov, Z. Jiang, Y. Zhang, S. V. Morozov, H. L. Stormer, U. Zeitler, J. C. Maan, G. S. Boebinger, P. Kim, and & A. K. Geim, "Room-Temperature Quantum Hall Effect in Graphene." Science Vol. 315, pp.1379-1282, (2007).
46. T. Shimizu, J. Haruyama, D. C. Marcano, D. V. Kosinkin, J. M. Tour, K. Hirose, and K. Suenaga, "Large intrinsic energy bandgaps in annealed nanotube-derived graphene nanoribbons," Nat. Nanotechnol. 6, pp.45-50 (2011).
47. Y. Zhang, T.-T. Tang, C. Girit, Z. Hao, M. C. Martin, A. Zettl, M. F. Crommie, Y. R Shen, and F. Wang, "Direct observation of a widely tunable bandgap in bilayer graphene," Nature 459, pp.820-825, (2009).

48. C. H. Lui, Z. Li, K. F. Mak, E. Cappelluti, and T. F. Heinz, "Observation of an electrically tunable band gap in trilayer graphene," Nat. Phys. 7, 944-950, (2011).
49. C. Lee, X. Wei, J. W. Kysar and J. Hone. "Measurement of the Elastic Properties and Intrinsic Strength of Monolayer Graphene" Science, Vol. 321, no. 5887, pp. 385-388, (2008)
50. T. Sekitani, T. Yokota, U. Zschieschang, H. Klauk, S. Bauer, K. Takeuchi, M. Takamiya, T. Sakurai and T. Someya., "Organic Nonvolatile Memory Transistors for Flexible Sensor Arrays" Science, Vol. 326, pp. 516-1519, 2009
51. L. Li, Q.D. Ling, S.L. Lim, Y.P. Tan, C. Zhu, D.S.H. Chan, E.T. Kang and K.G. Kang "A flexible polymer memory device" Organic Electronics, Vol 8, pp. 401–406, (2007)
52. A. A. Balandin, S. Ghosh, W. Bao, I. Calizo, D. Teweldebrhan, F. Miao, and C. N. Lau, "Superior thermal conductivity of single-layer graphene," Nano Letters 8 (3): pp. 902–907, (2008)
53. J. S. Bunch, A. M. van der Zande, S. S. Verbridge, I. W. Frank, D. M. Tanenbaum, J. M. Parpia, H. G. Craighead, and P. L. McEuen, "Electromechanical Resonators from Graphene Sheets," Science 315, pp.490-493, (2007).
54. K. E. Petersen, "Fabrication of an integrated, planar silicon inkjet structure," IEEE Trans. Electron Devices, vol. ED-26, pp.1918-1923, (1979)
55. http://www.ioffe.rssi.ru/SVA/NSM/Semicond/Si/el ectric.html
56. M. Gad-el-Hak edit., MEMS Handbook, CRC press (2002).
57. R. Vargas-Bernal and G Herrera-Perez, "Carbon Nanotube-and Graphene Based Devices, Circuits and Sensors," VLSI Design, (2012)

Chapter 2

Non-Volatile Graphene channel Memory (NVGM) for ultra-high density memory applications.

2.1. Introduction

Recently, flexible electronics have attracted great attention due to the high-demands of mobile electronics. Graphene has been considered as one of the potential candidates for channel material for FET because of its outstanding electrical properties. Meanwhile, Solid-State Drive (SSD) is becoming the mainstream module for data storage, particularity for mobile platform.[1] The majority of SSDs, however, utilize the conventional silicon channel CMOS transistor-based floating gate non-volatile memory cell, which requires high temperature processes, which flexible substrates cannot withstand. From 2005, NAND flash memory has been the most scaled device. Classical scaling of NAND flash memory is being expected to be faced with the physical limits within 2015. To keep memory scaling beyond this physical limit, memory industries have proposed 3-D NAND flash memory cell structures. But most of 3D NAND flash cell has poly-Si crystalline channel. To resolve the low mobility of poly Si channel, re-

crystallization processes such as solid phase epitaxial growth or laser annealing process have been used. But those methods have not been matured enough to turn poly-Si perfectly into c-Si. The high mobility of graphene and low temperature processes of NVGM can surpass these limitations. Recently, large scale pattern growth of graphene has been demonstrated [2] and could provide an effective solution to satisfy integrability with flexible electronics. Graphene channel transistor based memory cell fabrication technology could reduce production cost and maximize memory capacity replacing Si substrate with non-Si substrate such as glass or plastic film which has much larger than size than silicon wafer. In this chapter, non-volatile memory based on graphene channel transistor is fabricated and characterized and 3-dimensionally stacked NAND flash cell structure is proposed; it is shown as a solution of high speed, ultra high density flash memory.

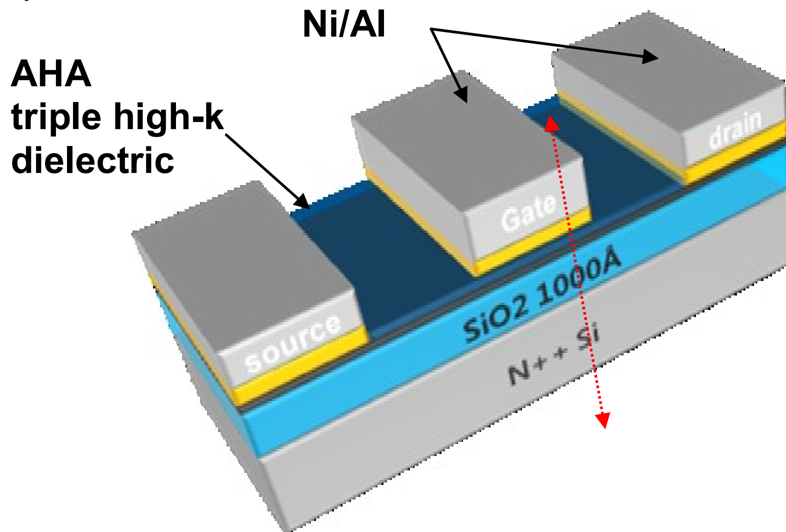


Figure.2.1 Schematic diagram of NVGM; a non-volatile memory (NVM) exploiting single-layer graphene (SLG) and multi-layer graphene (MLG) as channel materials and $Al_2O_3/HfO_2/Al_2O_3$ (AHA) triple high-k stack as a gate dielectric fabricated on SiO_2 film.

2.2. Fabrication

The schematic structure of NVGM memory is shown in Figure 2.1. Figure.2.4 shows the cross-sectional TEM image of gate stacks cut along the A-A' direction in Figure 2.1. The SLG and MLG are grown on copper (Cu) and Nickel (Ni) films, respectively, by chemical vapor deposition (CVD) and then transferred onto a 1000Å - SiO_2 film thermally grown on a highly doped n-type wafer.[3] The thickness of graphene layers (SLG and MLG) are confirmed by Raman spectroscopy (Figure 2.2). The major fabrication steps of NVGM are shown in Figure 2.3, where the active regions were patterned by conventional photolithography and oxygen plasma etching. An advantage in using graphene as an active layer is to eliminate the source and drain junction formation step that requires high temperature for dopant activation. This allows memory cell formation on non-Si flexible substrates. In NVGM, the metal source and drain (S/D) contacts are formed by e-beam evaporation followed by a lift-off procedure. Due to the hydro-phobic surface of graphene, a thin Al layer of 10Å is deposited and oxidized in air to provide nucleation sites for subsequent atomic-layer deposition (ALD) of the oxide stack. [4]

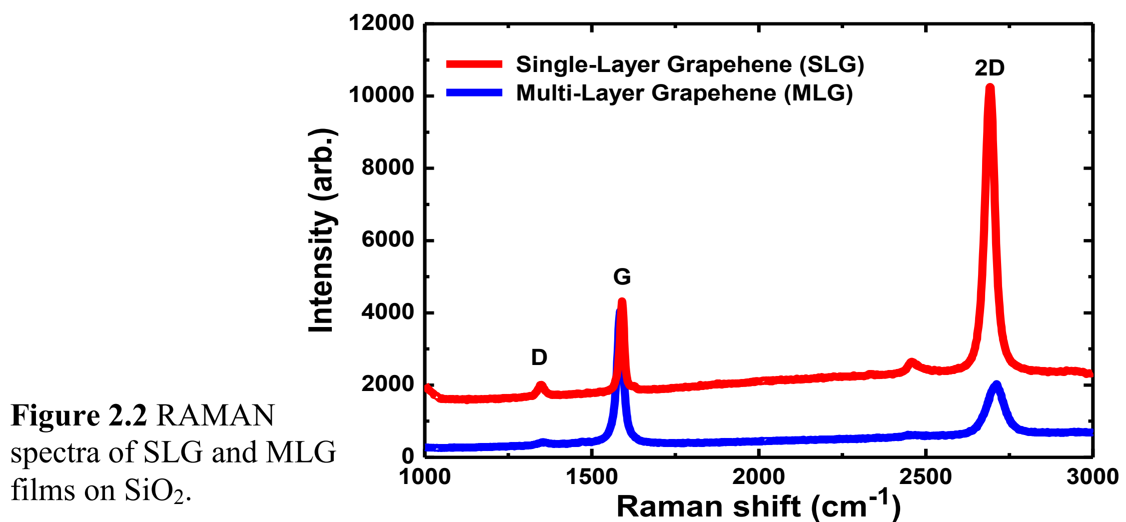


Figure 2.2 RAMAN spectra of SLG and MLG films on SiO_2.

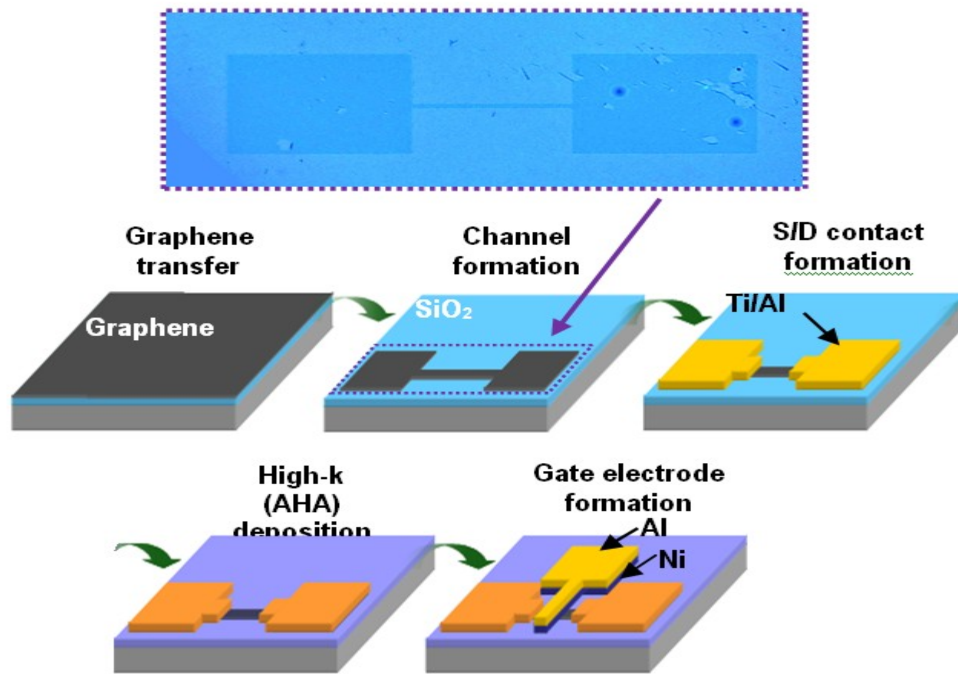


Figure 2.3 Process flow for the test structure of Non-Volatile Graphene channel Memory (NVGM).

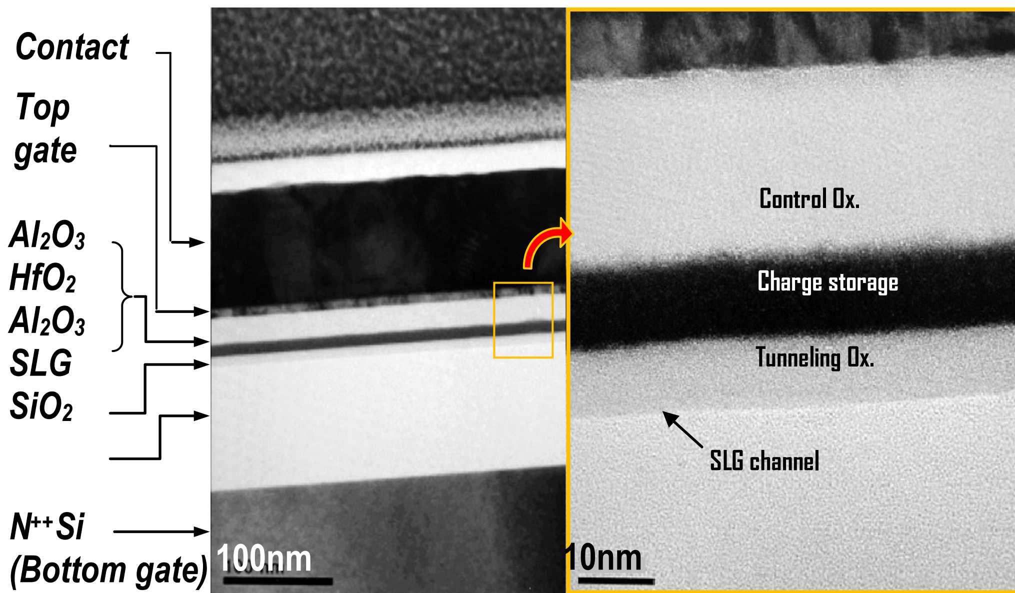


Figure 2.4 Cross-sectional TEM image of NVGM cut along A-A' direction in Figure 2.1 and $Al_2O_3/HfO_2/Al_2O_3$ (AHA) stack.

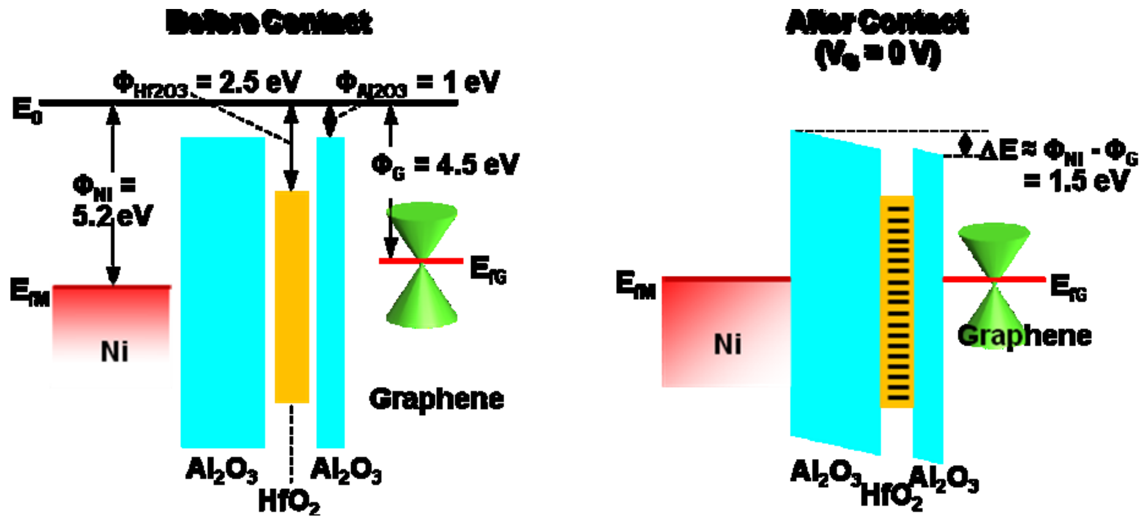
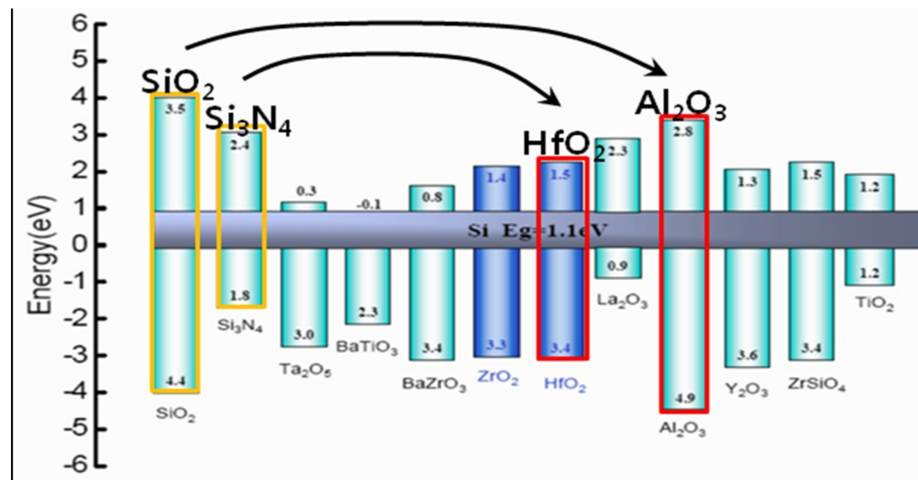


Figure 2.5 Band structure of NVGM before and after contact. NVGM is a charge trap memory designed to have similar structure and operation mechanism to S ONOS memory.



SONOS		NVGM
Silicon (Si)	Gate	Metal
Oxide (SiO_2)	Control oxide	Alumina (Al_2O_3)
Nitride (Si_3N_4)	Charge trap layer	Hafnia (HfO_2)
Oxide (SiO_2)	Tunneling oxide	Alumina (Al_2O_3)
Silicon (Si)	Channel	Graphene

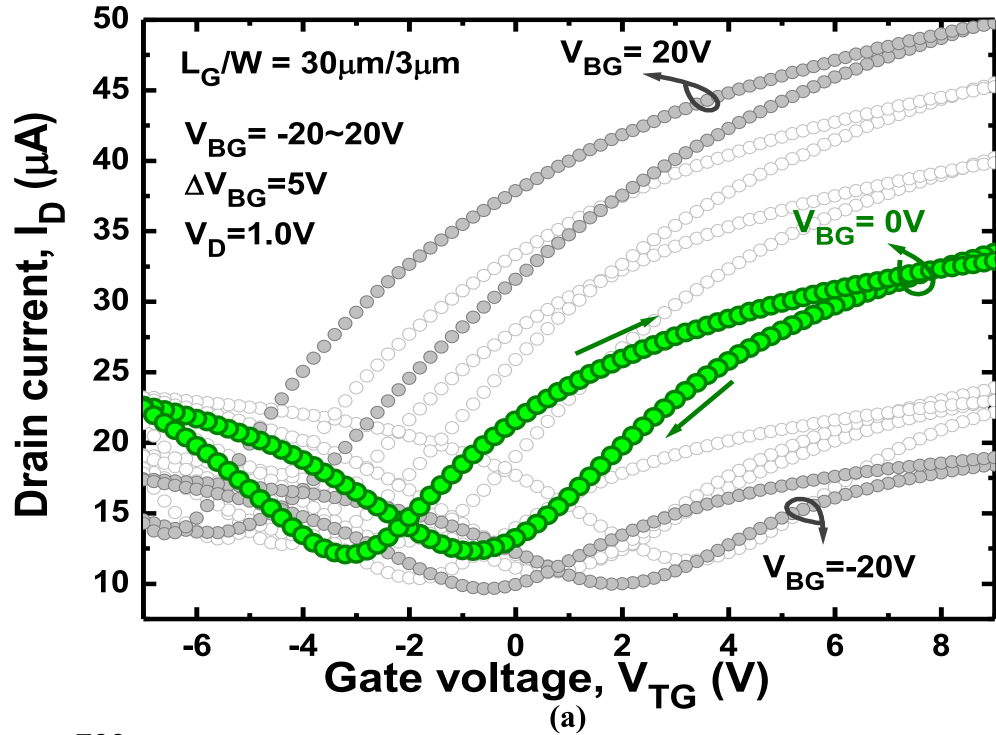
Figure 2.6 NVGM is designed to have similar structure and operation mechanism to SONOS. But the channel is replaced by graphene and ONO dielectric stack is replaced by triple $Al_2O_3/HfO_2/Al_2O_3$ triple high-k stack to enhance performance and to lower the fabrication process temperature.

The $Al_2O_3^{tunneling\ oxide}/HfO_2^{charge\ storage}/Al_2O_3^{control\ oxide}$ (AHA) high-k layers shown in Figure 2.4 were subsequently deposited by ALD.[5] Finally, metal gate electrodes are formed using the identical processes of the S/D formation. Ni has been chosen for the gate material because of its high work function (Φ_B), which promotes stable erase operation. Silicon–Oxide–Nitride–Oxide-Silicon (SONOS) structure has been considered to be a promising alternative to conventional floating-gate non-volatile memory (NVM) cells as it is immune to the adjacent capacitive-coupling issues and it enables the adoption of thin gate stacks. NVGM is also a charge trap memory structure, which has a similar operation mechanism to SONOS. The differences are that the channel material is replaced by grapheme and the $SiO_2/Si_3N_4/SiO_2$ triple dielectric stack is replaced by the triple high-k stack of $Al_2O_3/HfO_2/Al_2O_3$ (AHA) in order to lower the process temperature and enhance device performance. AHA triple high-k stack is chosen after considering the band-gap and electron affinity of dielectric materials to have similar structure to ONO.

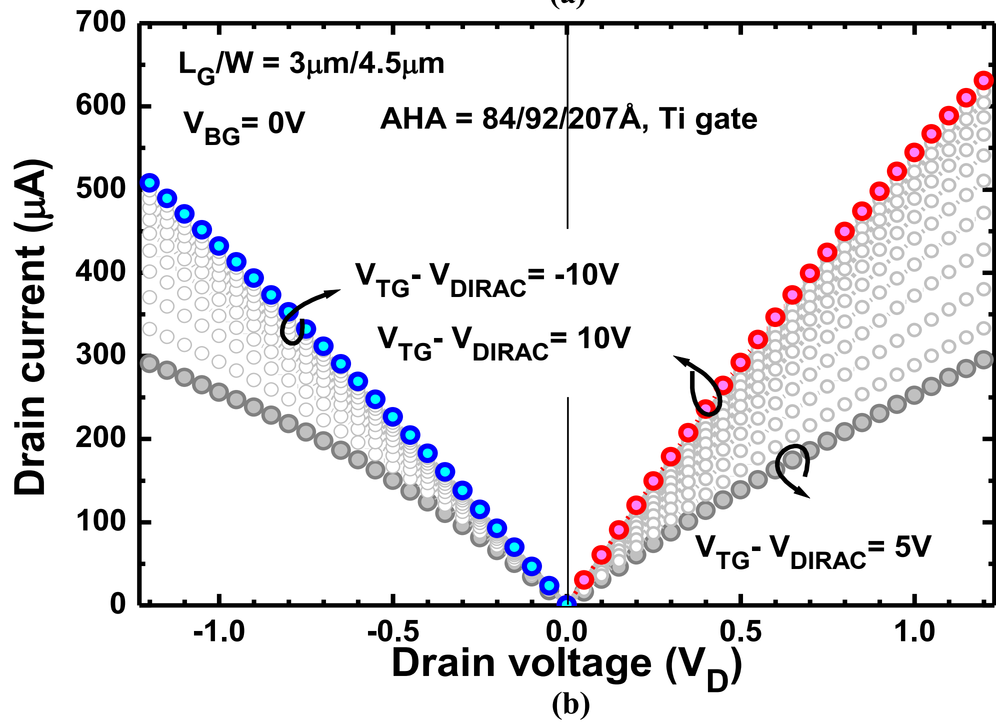
2.3. Electrical Characteristics

2.3.1. Performances of graphene channel FETs

The I_{DS}-V_{TG} characteristics of NVGM as functions of the top gate voltage (V_{TG}) for several different bottom gate voltage biases (V_{BG}) are shown in Figure 2.7. The hysteresis of I_{DS}-V_{TG} curve mainly originates from the trapping of charge into the interface between the graphene and gate dielectric. Therefore, a circular sweep of V_{TG} switches the type of carriers in the graphene channel from one to the other. Due to the zero bandgap semiconducting property of SLG, the I_{ON}-I_{OFF} ratio of NVGM transistor is less than 4.5



(a)



(b)

Figure 2.7 (a) Dual sweep I_{DS}-V_{GS} and (b) I_{DS}-V_{GS} characteristic of NVGM with SLG channel as functions of V_{TG} and V_{BG}. The hysteresis of I_{DS}-V_{TG} curve mainly originates from the trapping of charge into the interface between the graphene and gate dielectric

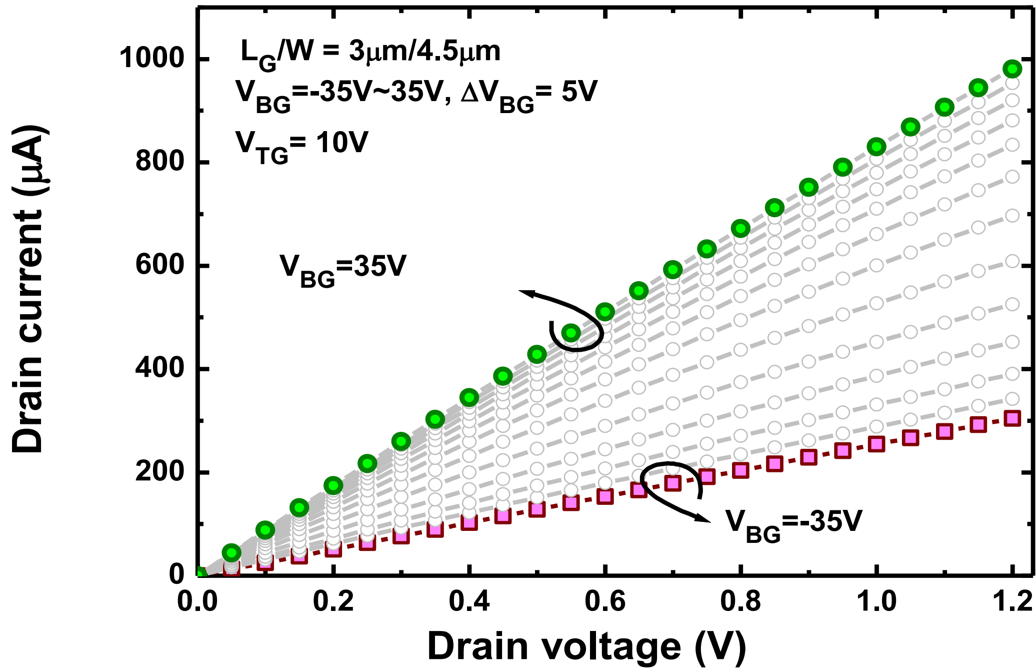


Figure 2.8 I_{DS}-V_{GS} characteristic of NVGM depends on $V_{BG.}$ NVGM with L_G/W=3/4.3um shows high current drivability approaching 1mA at V_{TG}=10V, V_{BG}=35V, and V_D=1.2V.

Figure 2.7 and 2.8 show the I_{DS}-V_{DS} curves of NVGM with the SLG channels. Due to the high mobility of the graphene channel, the drain current of NVGM transistor with the SLG channel and a gate length/channel width (L_G/W) of 3m/4.5 m approaches 1mA in spite of the fact that there is no source and drain deep junction formation.

2.3.2. NVGM memory functions

In conventional CMOS memory devices, the memory window (MW) corresponds to the threshold voltage shift of the FET (i.e., MW=$\Delta V_{TH} \approx \Delta V_{FB}$, where the ΔV_{FB} is the flat-band voltage shift due to the electron injection into the charge storage layer).[6,7] Because of the unipolar transport characteristics in CMOS, the ΔV_{TH} can only be

observable in either the positive or negative direction, which depends on the charge polarity of majority carriers. Thus, the MW is only determined by the positive ΔV_{TH} in n-MOS or the negative ΔV_{TH} in p-MOS.

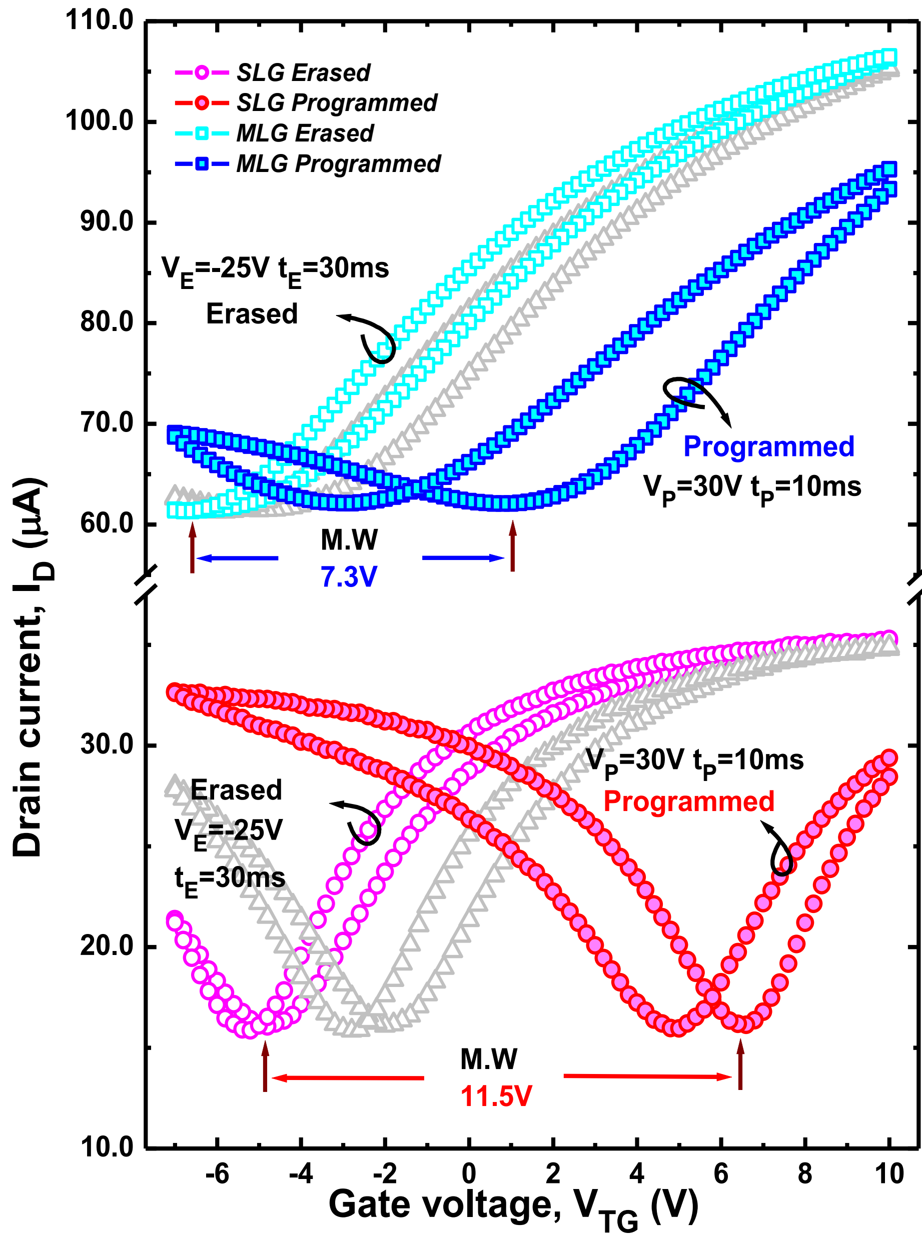


Figure 2.9 Program and erase characteristics of NVGM. Samples with SLG and MLG channels display memory windows of 11.5V and 7.3V respectively. Samples are programmed by voltage stress with V_P=30V for 10ms and erased by V_E=-25mV for 30ms.

In the graphene based FET memories, however, the MW can be larger because of the ambipolar conduction property. In other words, the MW in gFET memories can be defined as a summation of both the positive maximum ΔV_{Dirac} after a program operation and the negative maximum ΔV_{Dirac} after an erase operation [i.e., MW=$|+\Delta V_{Dirac(max)|}V_P|_+|-\Delta V_{Dirac(max)|}V_E|$].

In Figure 2.10, the memory functions of the NVGM samples with SLG and MLG channels are compared. The memory windows (MW) of 11.3V for SLG and 7.5V for MLG are achieved by using a programming condition of V_P=30V for 10ms and erasing condition of V_E=-25V for 30ms. Figure.2.11 shows V_{DIRAC} from the initial point depending on the program and the erase voltages. The initial V_{DIRAC} and memory window distributions of NVGM with SLG and MLG channels are compared in Figure 2.10 (b). The NVGM of SLG shows wider memory window than that of MLG.

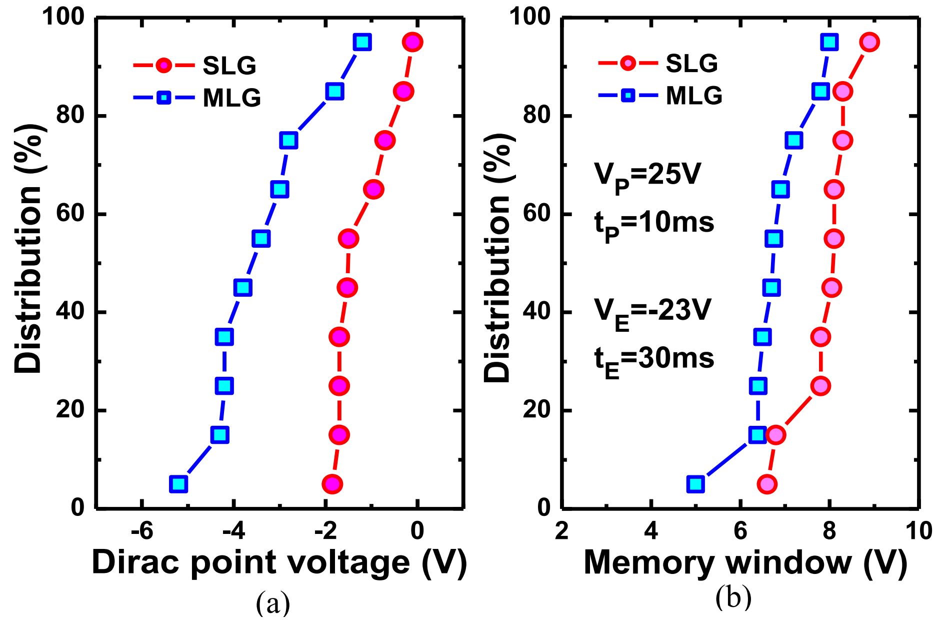


Figure 2.10 Samples with SLG channel shows (a) higher initial V_{DIRAC} position and (b) wider memory window than that with MLG.

These results suggest that SLG channel NVGM is more desirable for a high-fidelity memory device, although MLG has lower resistivity and is more robust under harsh process conditions.

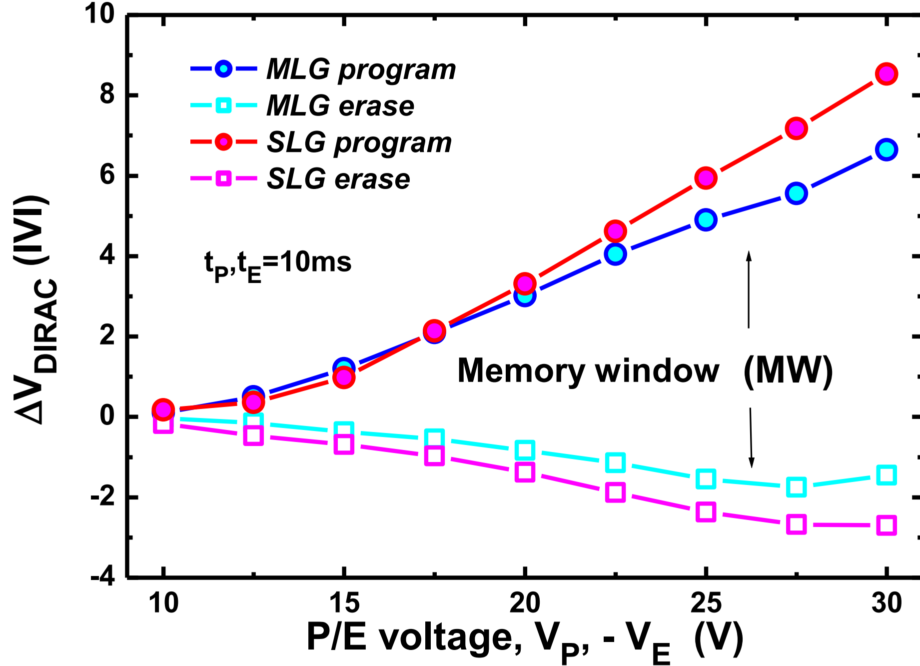
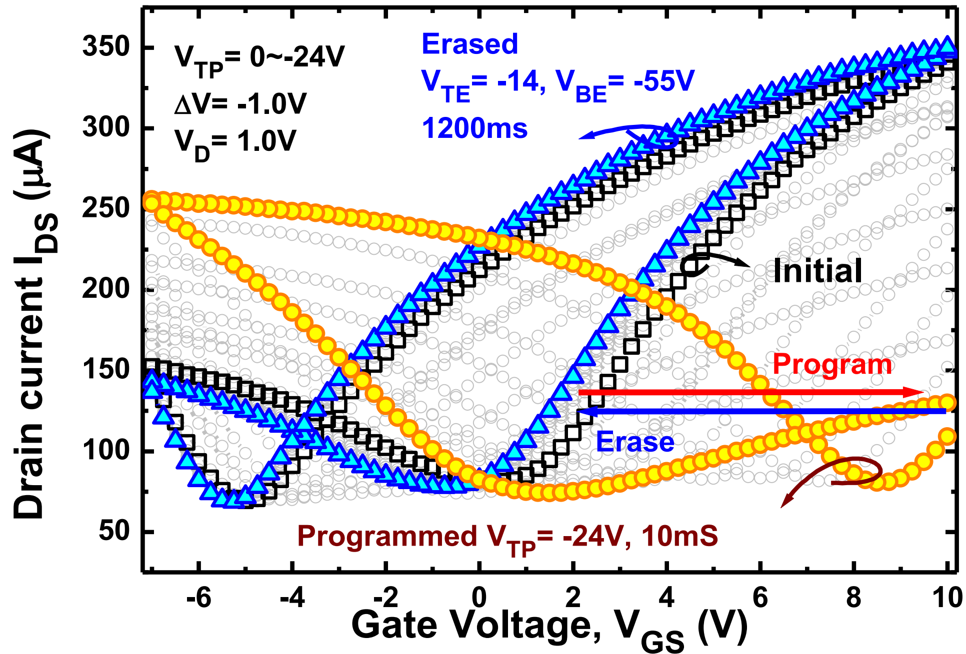


Figure 2.11 V_{DIRAC} shift depends on the program and erase voltage (V_P and V_E). Memory window (MW) of NVGM increased with the increase of V_P and V_E. Electron back injection from gate electrode is observed when V_E<-28V.

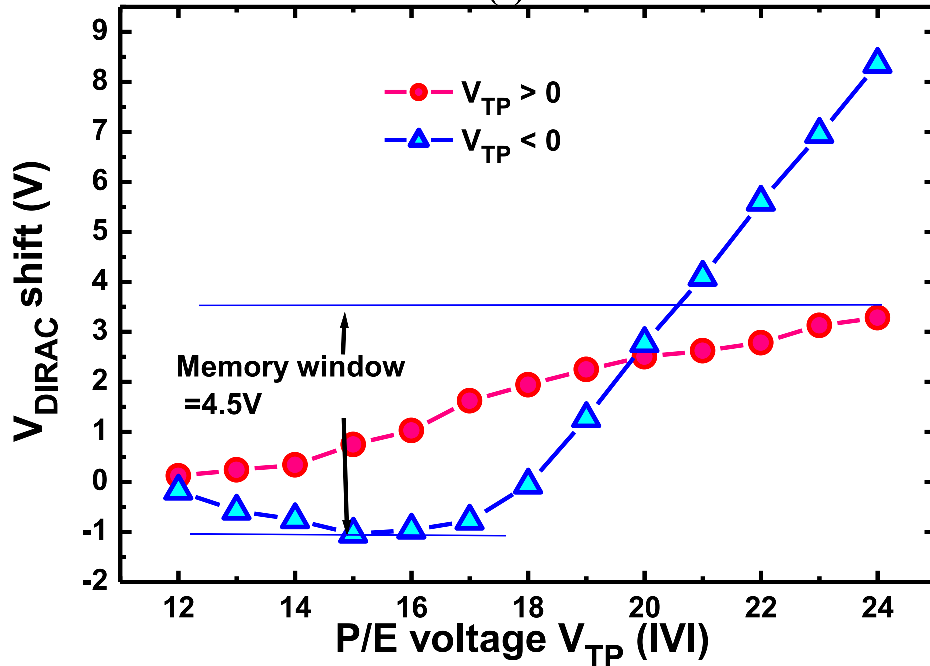
2.4. Impact of gate work-function on memory characteristics

We used two different kinds of gate metals (Ti and Ni) to examine the effects of the work-function (Φ_B) on the memory characteristics of the graphene channel field effect transistor with AHA triple high-k stack (gFET(AHA)). Figure 2.12 (a) shows the drain current vs. gate voltage (I_{DS}-V_{GS}) characteristics depending on the program voltage (V_P) erase voltage (V_E) of the gFET(AHA). In stand-by mode (V_P=0V), the device exhibits a typical V-shaped curve where the charge neutrality point (V_{Dirac}) is observed at ~0V.

After applying V_P (≥12V), the V_{Dirac} positively shifts, and the amount of shift (ΔV_{Dirac}) increases with V_P. The positive ΔV_{Dirac} is attributed to the reduction of electrochemical potential (μ) in the AHA gate stack due to the electron injection [6-8] from SLG to AHA. The V_{Dirac} slightly shifts toward the negative direction when a negative V_E (-12 to -14V) is applied and is ascribed by the increase of μ in the AHA due to the hole injection from SLG to AHA. However, when V_E exceeds -16 V, the V_{Dirac} suddenly turns and moves back toward the positive direction. This is caused by the electron back-injection from the Ti-gate to the AHA, which will be explained later in detail. As indicated in Figure 2.12(b), the maximum MW of the gFET with Ti gate electrode is ~4.5V. Here, it should be noted that the effect of the ultra-thin Al nucleation layer gives minimal effect on the memory characteristics, since the final Al_2O_3 layer shows a low interface state density (<9.41010cm^{-2}), which corresponds to a hysteresis of ~16mV when a ~45nm thickness of Al_2O_3 gate oxide is assumed. According to the above description, the electron back injection at larger V_E (<<-15 V) impedes the expansion of MW. This is closely related to the Φ_B of the gate electrode because Φ_B is a key factor in determining both the barrier height (φ_b) and the initial flat-band conditions for the device [see also Figures 2.14(a) and 2.14(e)]. Thus, in order to suppress the electron back-injection, we changed the gate electrode from Ti (Φ_{Ti}=4.3 eV) to Ni (Φ_{Ni}=5.1 eV). Similar to the Ti-gate device, the V_{Dirac} is positively shifted when V_P is increased [Figure 2.13(a)]. But, a clearly different behavior is observed when the erase operation is performed. The device exhibits a systematic ΔV_{Dirac} towards the negative direction up to V_E=-30V where the electron back-injection occurs [Figures 2.13 (b)].

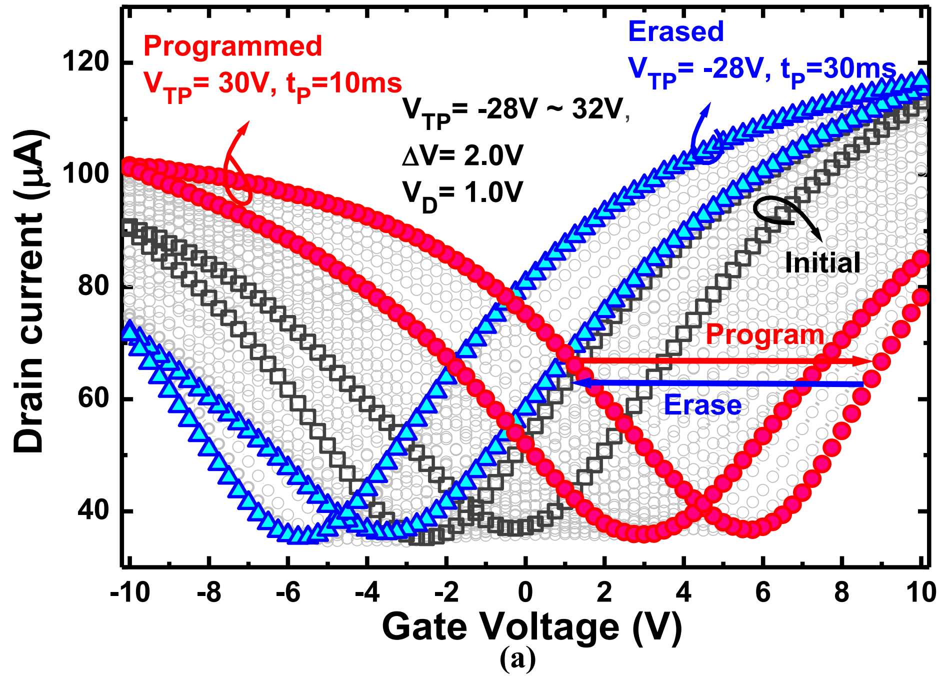


(a)

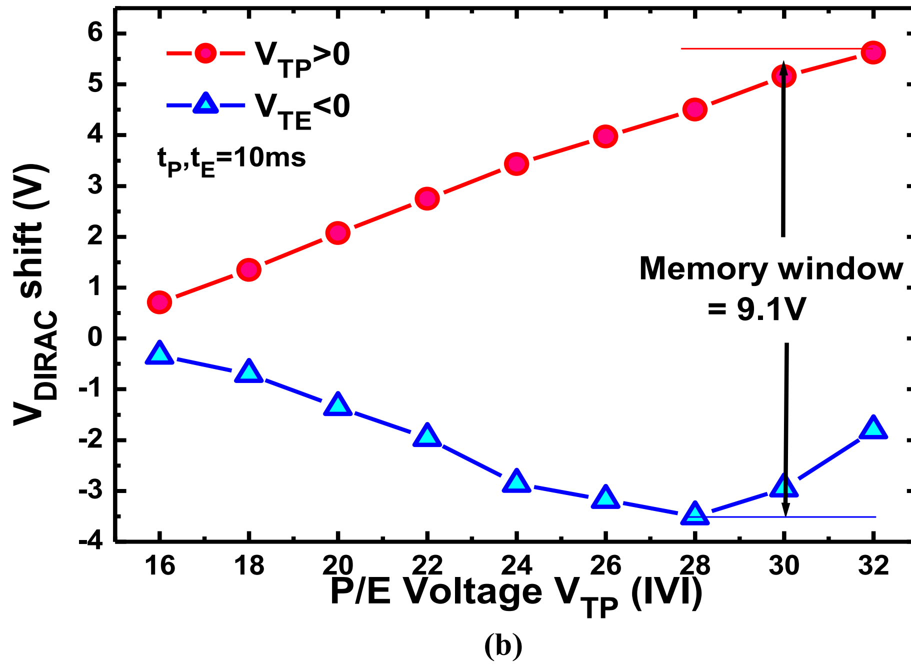


(b)

Figure 2.12 (a) I_{DS}-V_{GS} characteristic curves of gFET(AHA) after programming and erasing at various V_P (+12 – +24 V; 10 ms; step: +2 V) and V_E (-12 to -24 V; 30 ms, step: - 2 V). (b) Variation of ΔV_{Dirac} as a function of VP and V_E for Ti-gate gFET(AHA). NVGM with low workfunction Ti (Φ_{Ti}=4.3 eV) metal gate electrode shows serious electron back injection when the V_E >16V



(a)



(b)

Figure 2.13 (a) I_{DS}-V_{GS} characteristic curves of Ni-gate gFET(AHA) after programming and erasing at various V_P (=+16 to +32 V; 10 ms; step: +2V) and V_E (=-16 to - 32 V, 30 ms; step: - 2 V). (b) Variation of ΔV_{Dirac} as a function of V_P and V_E for Ni-gate gFET(AHA). Electron back injection is effectively suppressed by the adoption of high workfunction gate metal Ni (Φ_{Ni}=5.1 eV) electrode.

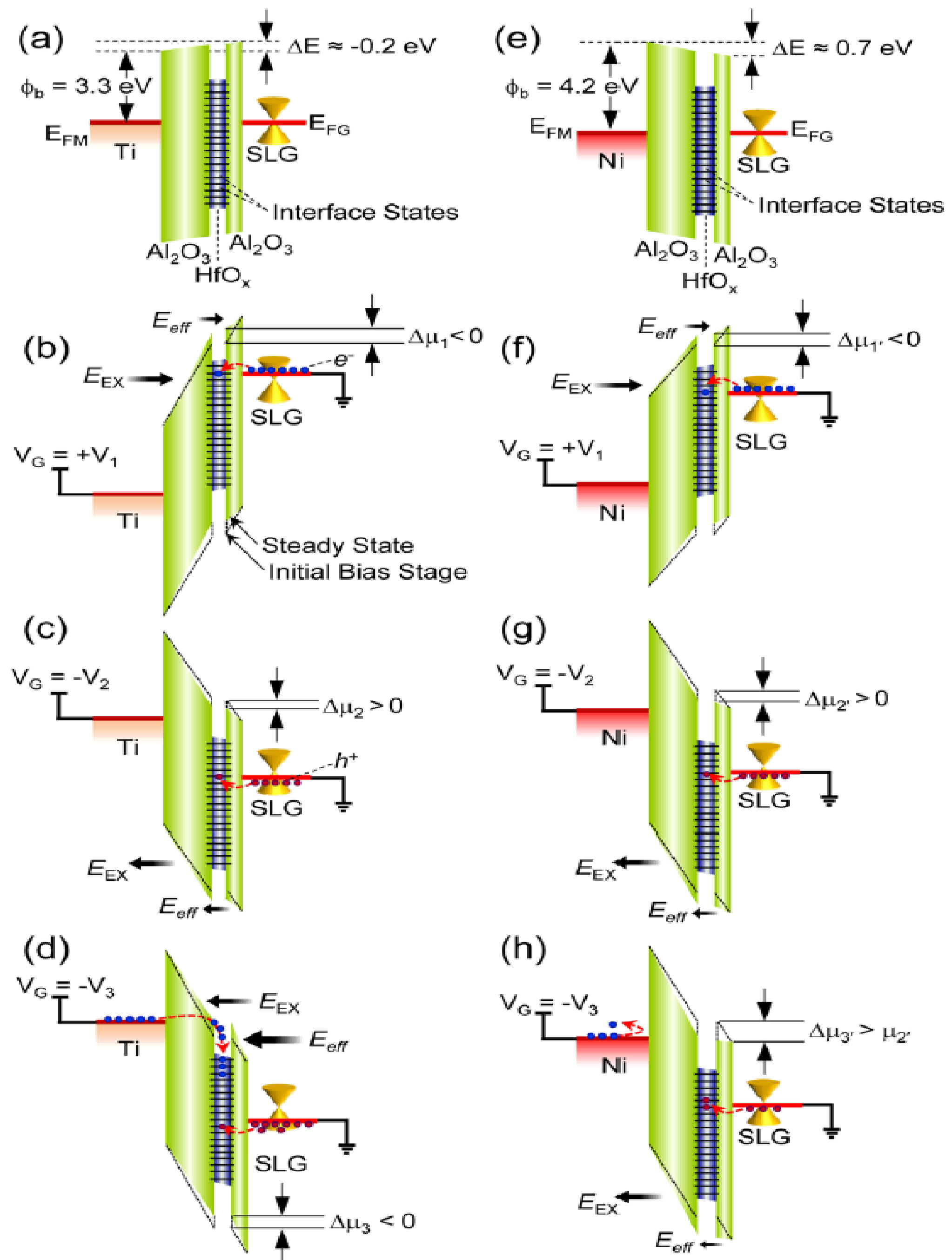


Figure 2.14 Energy band diagrams of Ti- and Ni-gate gFETs(AHA) at various bias conditions. Ti-gate gFET(AHA): (a) $V_G = 0$ V, (b) $V_G = +V_1$, (c) $V_G = -V_2$, (d) $V_G = -V_3$ ($<<-V_2$). Ni-gate gFET(AHA): (e) $V_G = 0$ V, (f) $V_G = +V_1$, (g) $V_G = -V_2$, (h) $V_G = -V_3$ ($<< -V_2$).

As a result, the Ni-gate device exhibits a larger MW=9.1V through an increase in both MW compared to the Ti-gate device. On the basis of our device performance, we believe that the Φ of gate electrodes plays a crucial role in the memory characteristics of NVGMs.

To understand the impact of Φ on the device operation, we compare and explain the carrier transport mechanisms in the gFET(AHA)s. Figure 2.14 represents the energy band diagrams of the Ti-gate and the Ni gate gFET(AHA) memory devices at various bias conditions. At zero bias, the φ_b (Φ_{Gate} - Φ_{Al2O3} = 4.3–1.0 eV) [8] is 3.3 eV and the ΔE (Φ_{Gate} - Φ_{SLG} = 4.3–4.5 eV) [8,9] is - 0.2 eV for the Ti-gate device [Figure 2.14(a)]. For the Ni-gate device, since the Φ_{Ni} (5.2 eV)[8] is larger than the Φ_{Ti}, the φ_b is increased to 4.2 eV and the ΔE is reversed to 0.7eV [Figure 2.14 (e)]. As we apply V_P beyond the V_{Dirac} (e.g., V_G=+V_1 >> V_{Dirac}), the electrons are induced in SLG and some of the electrons are injected into the AHA due to the high external electric-field (E_{EX}). At steady state [Figures 2.14(b) and 2.14(f)], the electrons stored in HfO_x reduce the μ in the AHA and causes the effective electric-field (E_{eff}) to decrease near the interface region between Al_2O_3 and SLG. This creates the positive ΔV_{Dirac} when V_P is applied. Here, the difference in flat-band conditions (i.e., ΔE=-0.2 eV for the Ti-gate device and ΔE=+0.7 eV for the Ni-gate device) produces a larger $\Delta V_{Dirac(max)|}V_P$ in the Ni-gate device compared to the Ti-gate device. In the case of the erase operation [Figures. 2.14(c) and 2.14(g)], the applied V_E (e.g., V_G=-V_2 << V_{Dirac}) induces hole carriers in SLG and the E_{EX} gives rise to the hole injection into the AHA. Similar to the program operation, the holes stored in HfO_x increases the μ_1 in the AHA and the increased μ_l leads to the negative ΔV_{Dirac}.

When V_E reaches the critical turning point (e.g., V_G=-V_3<<-V_2), the electron back injection takes place in the Ti-gate device through Fowler-Nordheim tunneling [Figure 2.14(d)], which is caused by the high E_{EX} and the relatively low φ_b. The back-injected electrons reduce the μ_l and a sudden change in ΔV_{Dirac} to the positive direction occurs. However, in the case of the Ni-gate device [Figure 2.14(d)], the probability of electron back-injection is low because of the relatively high φ_b. This allows a further increase in negative $|\Delta V_{Dirac}|$. As a consequence, the increase in both $|\Delta V_{Dirac(max)|}V_P|$ and $|-\Delta V_{Dirac(max)|}V_E|$ results in the enlargement of MW. With regard to the overall memory performance, the operating speed of our graphene charge trap memory would be limited by the capacitive charging speed of the gate stack, since the high graphene mobility[10,11] of 5000–100,000 cm^2/Vs renders an extremely short transit-time.

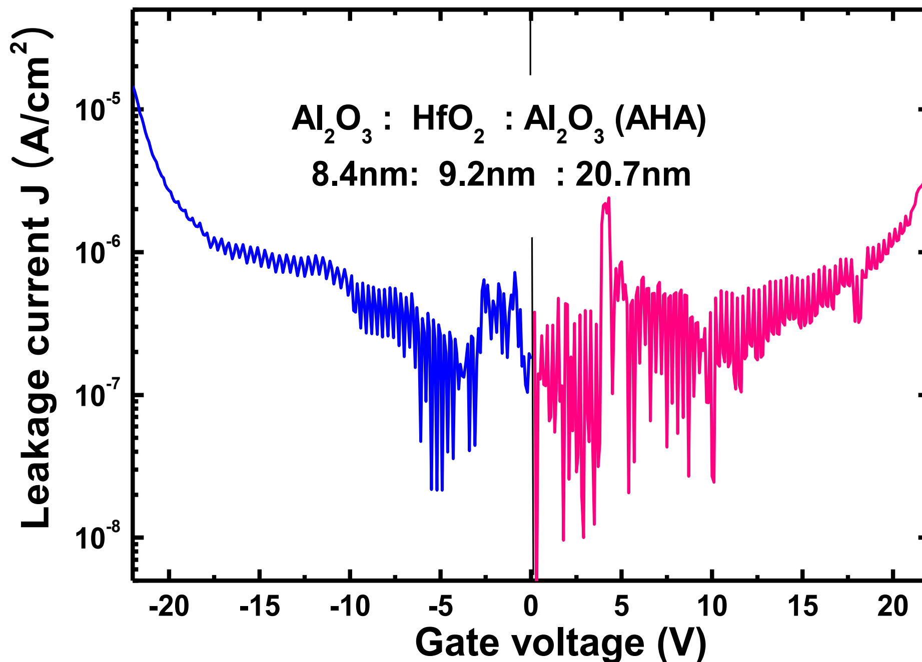


Figure 2.15 Gate leakage current density of AHA high-k gate dielectric.

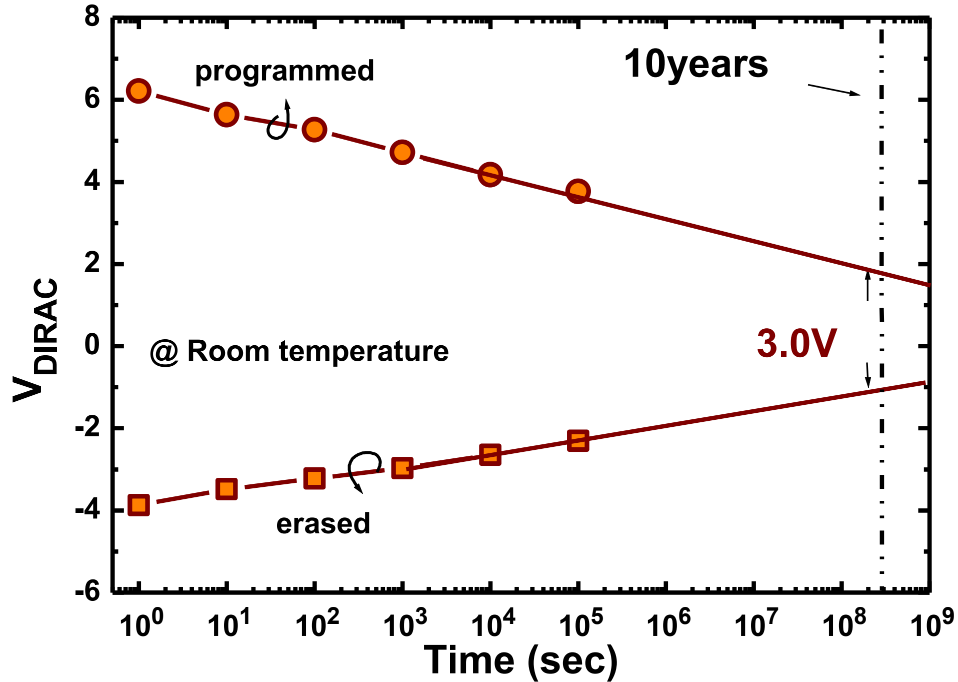


Figure 2.16 Data retention characteristics of NVGM. The NVGM can maintain programmed states larger than 3.0V for 10 years but charge loss is about 70%. The degraded retention characteristics in NVGMmight be attributed to the quality of Al_2O_3 tunneling oxide.

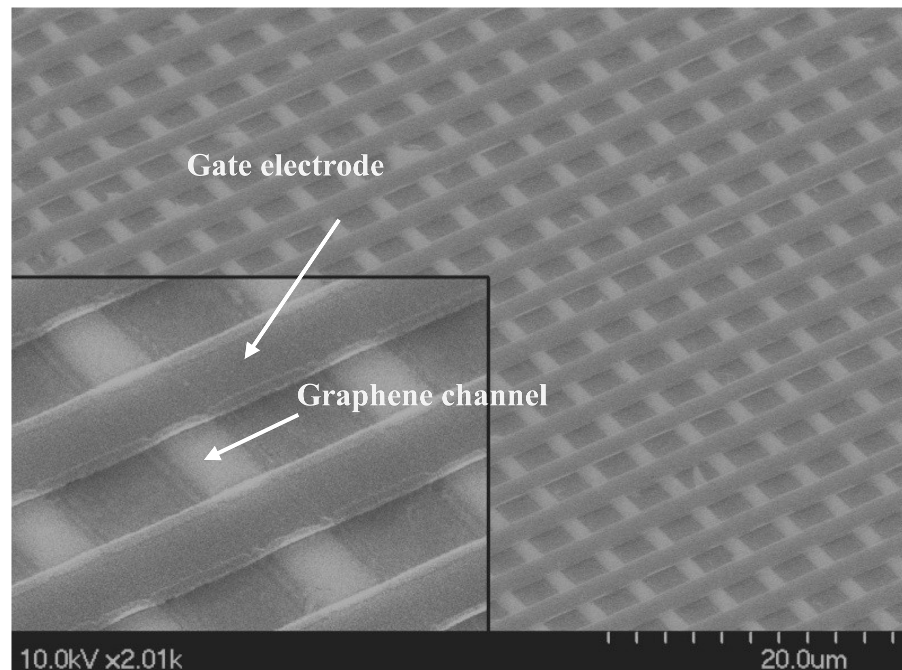


Figure 2.17 SEM image of NVGM cell array. Large scale graphene growth and transfer technology enables fabrication of high density NVGM cell.

Figure 2.16 shows data retention time measured at room temperature. The NVGM can maintain programmed states larger than 3.0V for 10 years. Degraded data retention characteristics might be attributed to the poor quality of Al_2O_3 tunneling oxide which is deposited at low temperature. So further process optimization such as finding out new material for tunneling oxide or changing band structure of gate stacks are required to improve the data retention characteristics of NVGM. Figure 2.17 displays the SEM image of a NVGM cell array.

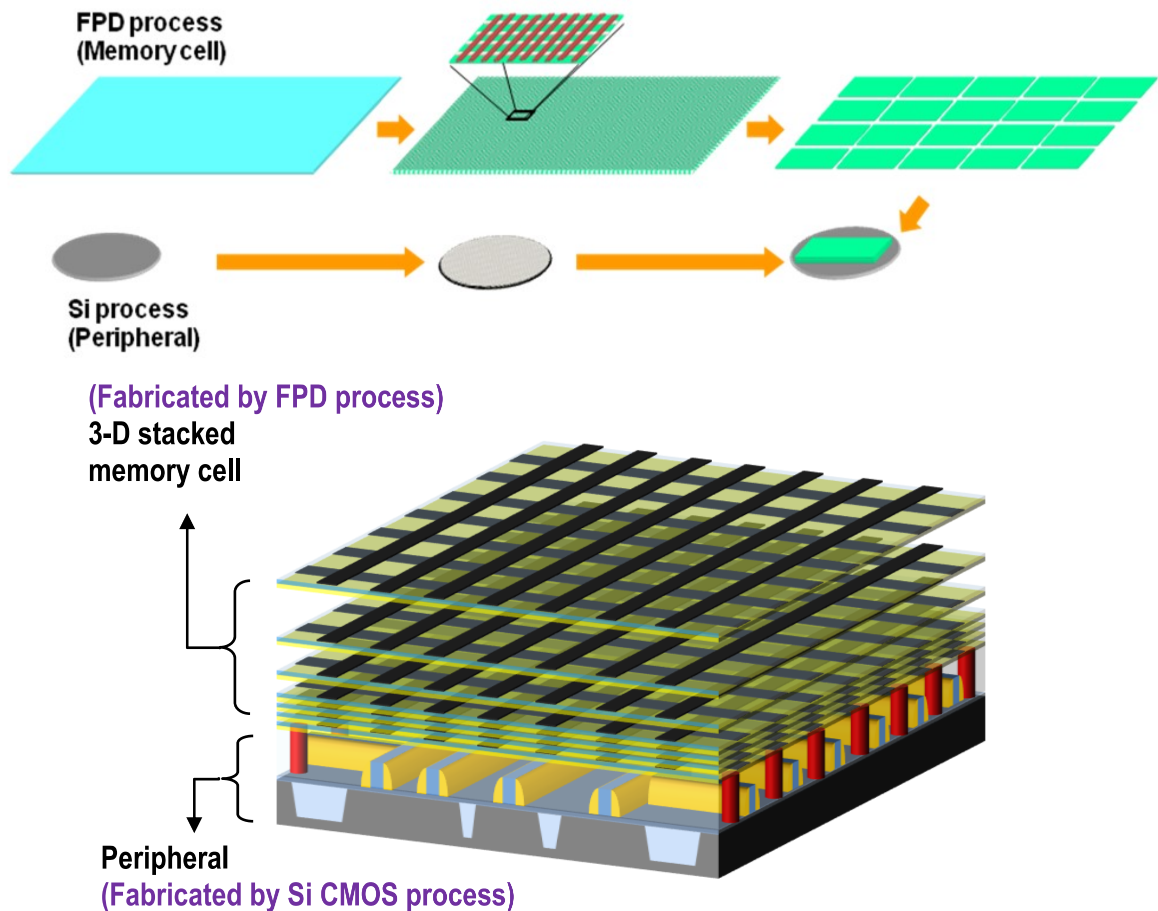


Figure 2.18 Most possible application of NVGM ultra-high-density data storage. NVGM cell could be fabricated using flat panel display production lines and 3D multi-stack memory could fabricated stacking NVGM cell on peripheral circuit fabricated using Si CMOS processing.

The NVGM cell can be formed on any substrate larger than a 12” Si wafer, which can withstand 250°C. Therefore, the NVGM cell structure could be fabricated using flat panel display production lines and could eventually lower the memory production costs. Furthermore, the top and bottom gate electrodes of the NVGM cell could be replaced with graphene electrodes to further enhance the elasticity of flexible electronics as illustrated in Figure 2.18.

2.5. Summary

The graphene channel non-volatile-memory devices with SLG and MLG have been successfully fabricated. Large scale graphene growth and transfer enabled NVGM cell array fabrication and greatly reduced the thermal budget of fabrication processes. The AHA-gFETs fabricated with two different gate electrodes (Ti and Ni) show a strong dependence of their memory characteristics on the Φ of gate materials. In comparison with the Ti-gate device (MW~4.5V), the Ni gate device reveals a larger MW~9.1V arising from a greater value in both $|\Delta V_{Dirac(max)|}V_P|$ and $|-\Delta V_{Dirac(max)|}V_E|$. The increased $|\Delta V_{Dirac(max)|}V_P|$ is directly attributed to the positive ΔE from the flat-band condition, and the increased $|-\Delta V_{Dirac(max)|}V_E|$ is a result of the high φ_b. The NVGM shows excellent electrical characteristics and great potential to be used for flexible electronics with ultra-high-capacity data storage.

2.5. REFERENCES

1. J. Jang, H-S. Kim, W. Cho, H Cho, J. Kim, S. I. Shim, Y. Jang, J-H. Jeong, B-K. Son, D. W. Kim, J-J. Shim, J. S. Lim, K-H. Kim, S. Y. Yi, J-Y Lim, D. Chung, H-C Moon, S Hwang, J-W Lee, Y-H Son, U-I. Chung and W-S Lee., “Vertical cell array using Terabit Cell Array Transistor technologies for ultra high density NAND flash memory” Tech. Digest. VLSI Tech. symposium, pp.192-193 (2009).
2. S. Bae, H. Kim, Y. Lee, X. Xu, J-S. Park, Y. Zheng, J. Balakrishnan, T. Lei, H. R. Kim, Y. I. Song, Y-J. Kim, K. S. Kim, B. Özyilmaz, J-H Ahn, B. H. Hong and S. Iijima “Roll-to-roll production of 30-inch graphene films for transparent electrodes”, Nature Nanotechnology 5, pp.574–578 (2010)
3. K. S. Kim, Y. Zhao, H. Jang, S. Y. Lee, J. M. Kim, K. S. Kim.6, J-H. Ahn, P. Kim, J-Y. Choi and B. H. Hong., “Large-scale pattern growth of graphene films for stretchable transparent electrodes”, Nature 457, pp. 706-710 (2009)
4. S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tutuc and S. K. Banerjee., ” Realization of a high mobility dual-gated graphene field-effect transistor with Al2O3 dielectric”, APL 94, pp.062107-062111, (2009)
5. S. Jeon, S. Choi, H. Park, H. Hwang, J. H. Han, H. Chae, S. D. Chae, J. H. Kim, M. K. Kim, Y. S. Jeong, Y. Park, S. Seo, J. W. Lee and C. W. Ki, “Triple high-K stacks ($A1_20_3/Hf0_2/Al_20_3$) with high pressure H_2 and D_2 annealing for SONOS type flash memory device applications”, Tech. digest of IEEE Conf. on Nanotech. pp. 53-55 (2004)
6. D. K. Schroder, Semiconductor Material and Device Characterization, 3rd ed. (Wiley, New York, 2006).
7. S. M. Sze, Physics of Semiconductor Devices, 3rd ed. (Wiley, New York, 2006).
8. S. Oda and D. Ferry, Silicon Nanoelectronics (Taylor & Francis, New York, 2006).
9. Y.-J. Yu, Y. Zhao, S. Ryu, L. E. Brus, K. S. Kim, and P. Kim, “Tuning the graphene workfunction by electric field effect,” Nano Lett. 9, 3430 (2009).

10. A. K. Geim, "Graphene: Status and Prospects," Science 324, 1530 (2009).
11. A. H. Castro Neto, F. Guinea, N. M. R. Peres, K. S. Novoselov, and A. K. Geim, "The electronic properties of graphene," Rev. Mod. Phys. 81, 109 (2009).

Chapter 3

Transparent and Flexible Memory (FTM)

3.1. Introduction

Electronic modules have been going through extensive renovations in order to incorporate multiple functionalities, such as portability, transparency, flexibility, and wearability. This would require multiple core electronic devices, such as logic, memory, and display to be integrated on a single transparent-flexible substrate without degrading the transparency from the addition of active layers and device performance under flex. In the past decade, difficulties in achieving transparent high-quality crystalline inorganic materials on transparent-flexible substrates have made organic materials[1,2] and semiconducting nanowires[3,4]/nanotubes[5,6] favorable for transparent-flexible electronic devices.[7,8]

Alternatively, the two dimensional graphene can offer enhanced performance to transparent-flexible electronic modules because it inherently possesses high carrier mobility[9] with minimal light absorbance.[10] Furthermore, due to the strong hexagonal covalent bonds, graphene maintains its extraordinary mechanical properties even at the nano-scale regime.[11] In recent years, the success of artificially growing large scale

graphene[12,13] has led to graphene based transparent electrodes,[10] which transcended to the emergence of graphene based touch screen, liquid crystal display, organic solar cells, and organic light emitting diodes. In addition to graphene being exploited as a passive element, flexible and stretchable graphene transistors have also been demonstrated using an ion-gel gate dielectric.[14,15] Transparent-flexible memory modules, on the other hand, have been limited to memristive systems such as graphene-organic hybrid devices[16,17] and chemically derived graphene oxide devices.[18]

In this chapter, we show memory operation in a flexible and transparent memory (FTM) composed of a single-layer graphene channel and a triple high-k dielectric ($Al_2O_3/HfO_x/Al_2O_3$) gate stack on a transparent-flexible polyethylene naphthalate (PEN) substrate. [Figure 3.2] Although the memory performance can be characterized through many means, we focus on the degradation of transparency due to the active graphene/triple-gate stack, the operating mechanism and retention properties of the memory function, and the influence of bending stress on the device performance.

3.2. FTM structure and fabrication process flow

Most transparent-flexible substrates cannot withstand high temperatures associated with processing steps necessary for device fabrication due to the low glass transition and/or thermal decomposition temperatures of the substrate. An advantage in using graphene as an active layer is to eliminate high temperature processes that are generally required for obtaining high quality channel materials and Ohmic source/drain junctions. Here, we fabricate the transparent-flexible FTM through a multi-step procedure

at temperatures below 110°C as shown in Figure 3.1. First, single-layer graphene was grown on a copper film by chemical vapor deposition (CVD),[19,20] transferred onto a PEN substrate, and characterized through Raman spectroscopy.[20-22] Active channel regions were then patterned by photolithography and etched through oxygen plasma. Next, a photoresist mask was formed by photolithography and a thin Al layer of 12 Å was deposited and oxidized in air to promote nucleation of Al_2O_3.[20,23] Finally, a triple-gate stack of $Al_2O_3/HfO_x/Al_2O_3$ (8nm /8nm /25nm) was subsequently deposited through atomic layer deposition and transparent indium tin oxide (ITO) gate electrodes were formed by sputtering and lift-off. The schematic diagram, cross-sectional transmission electron microscope (TEM) image of the as fabricated FTM, and scanning electron microscope (SEM) image of the high-density FTM array are shown in Figure 3.4(a).

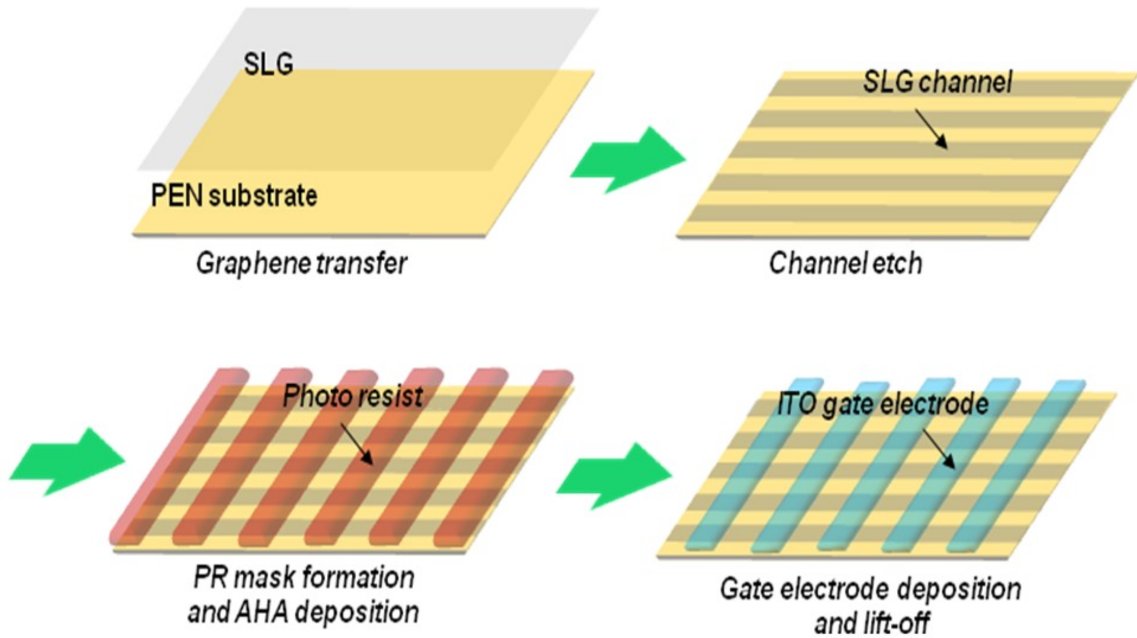


Figure 3.1 Fabrication process steps of transparent-flexible FTM.

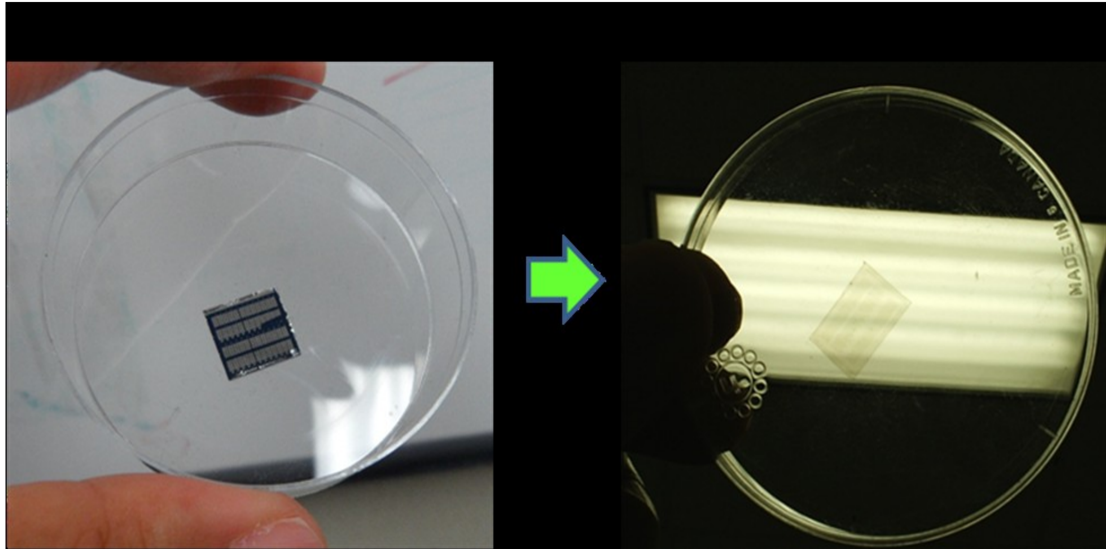


Figure 3.2 FTM is fabricated on flexible and transparent polyethylene naphtalate (PEN) substrate.

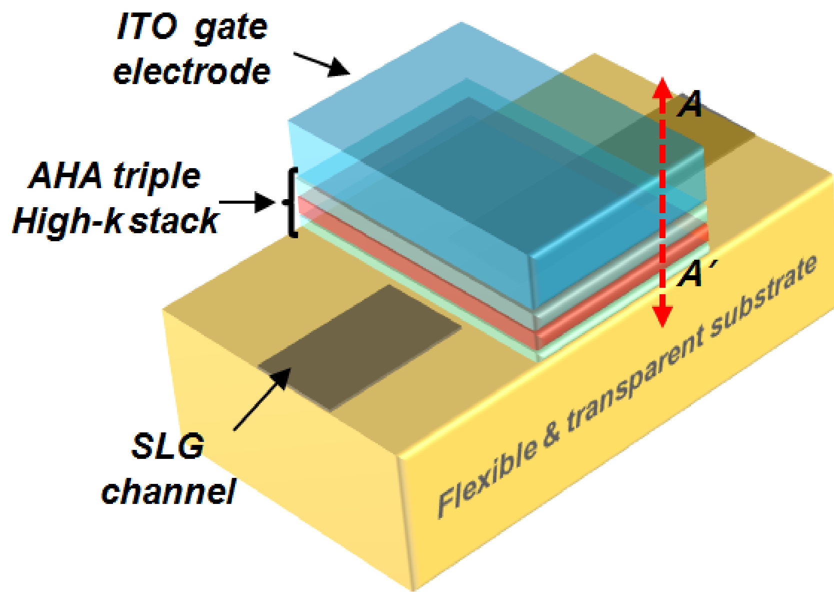
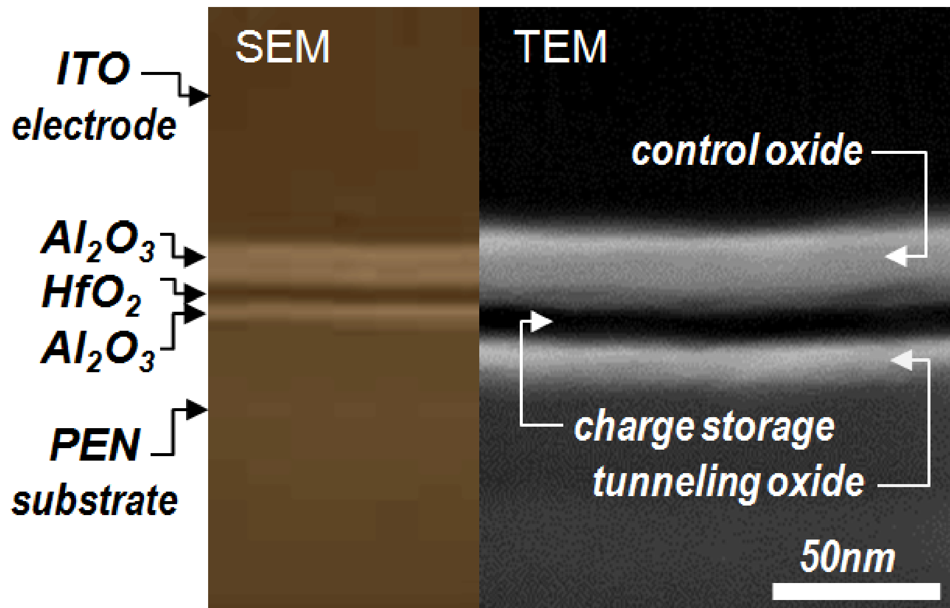
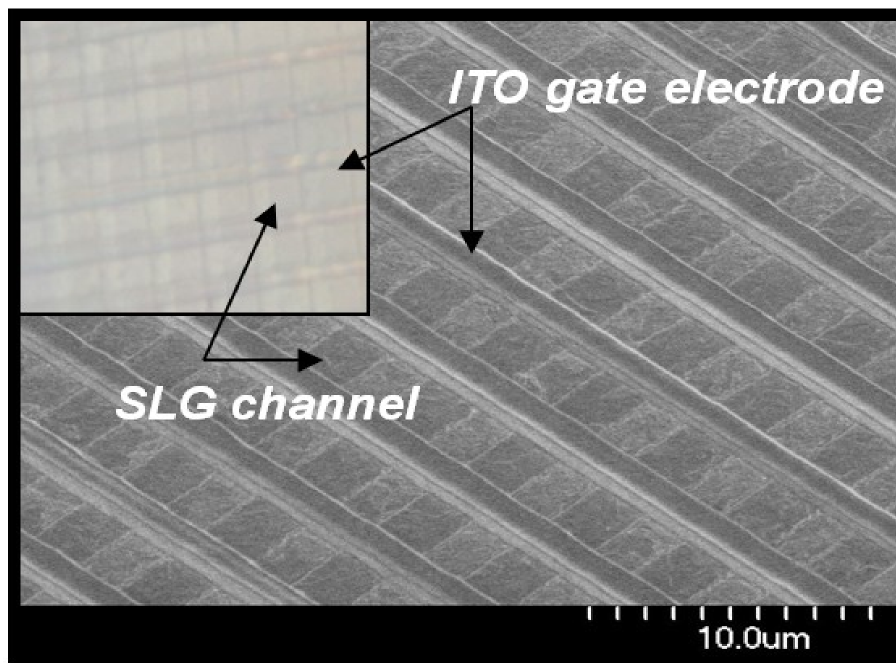


Figure 3.3 Schematic illustration of FTM device structure. FTM is fabricated exploiting graphene (SLG) channel, $Al_2O_3/HfO_2/Al_2O_3$ (AHA) triple high-k dielectric stack and ITO transparent gate electrode.



(a)



(b)

Figure 3.4 (a) Cross-sectional SEM and TEM image of $Al_2O_3/HfO_x/Al_2O_3$ (AHA) gate stack in FTM. (b) Bird's eye view SEM image of high-density FTM array. Single layer graphene was not resolved with TEM because of single atomic thickness. Large scale graphene growth and transfer technology enables high density memory cell fabrication on flexible substrate.

The triple gate stack comprised of an Al_2O_3 - tunnel oxide, a HfO_x - charge trap layer, and an Al_2O_3 - control oxide is clearly noticeable. The SEM image of the array [Figure 3.4(b)] is to demonstrate a possible cell circuitry composed of FTMs without metal electrodes. The semi-metallic property of graphene allows the graphene to be used as either the channel material or the interconnections. In other words, the region of graphene underneath the gate stack serves as the channel material, while the rest of graphene may function as both the source/drain contacts and interconnections.

3.3. Optical transparency of FTM

We first examine the transparency degradation arising from the addition of FTM on the PEN substrate. Figure 3.5 compares the optical transmittance spectra of the PEN substrate with and without the FTM array. The active layers reduce the transparency only by 8% in the visible-infrared wavelength range (400-900 nm) and sustain its transparency without distorting an image behind the FTM array [Figure 3.6]. Minimum requirement for transparency for an active electronic element should be greater than 80% considering the transparency of a transparent electrode is nowadays above 90%.[24] Up to date, transparency ranging in 60-80% has been demonstrated in various transparent electronic modules; for example, semiconducting nanowires/nanotube transistors and logic gates (>80%),[4,5,25,26] wide bandgap transparent conducting oxide memory structures (~80%),[27] organic light emitting diodes (~70%),[28] and grid structured lithium-ion batteries (~60%).[29] Our FTM array shows transmittance over 80% in the visible-infrared regions, which is comparable to the most transparent active components.

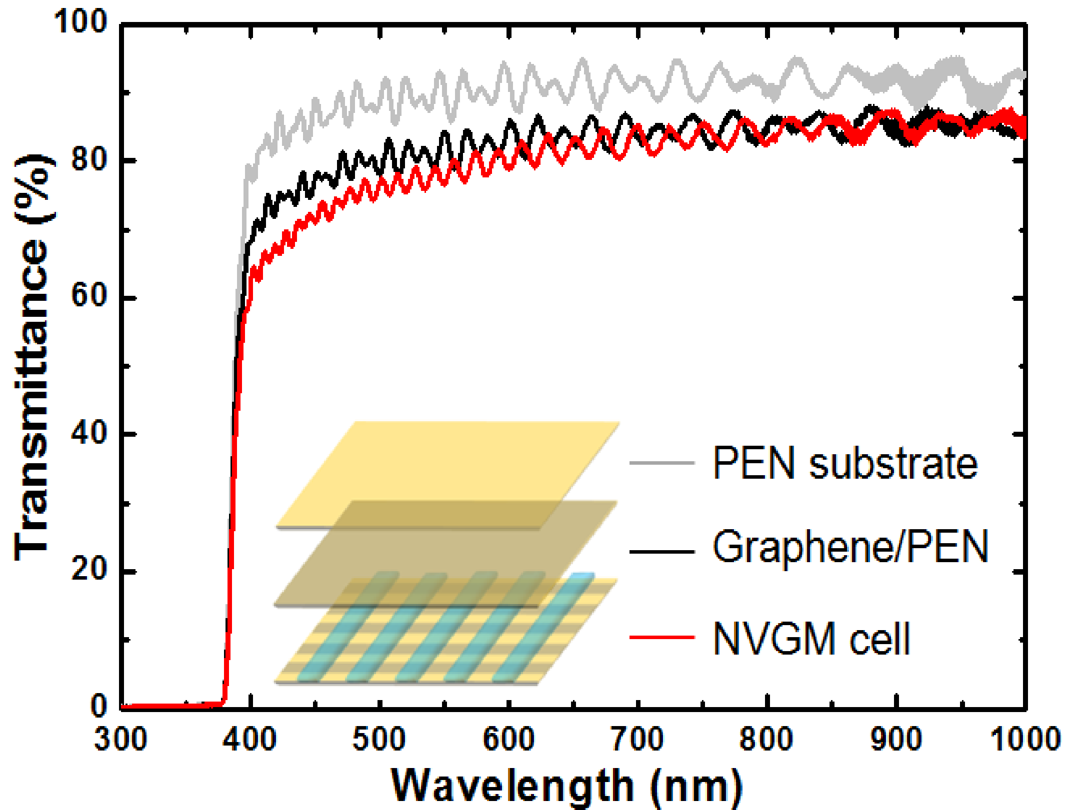


Figure 3.5 Optical transmittance spectra of FTM and PEN substrate before and after graphene transfer. The addition of FTM on the PEN results in an 8% reduction of transparency in the visible wavelengths.

3.4. Electrical characteristics of FTM

3.4.1. Performance of flexible and transparent FET

Next, we study the electrical performance of the FTM where all electrical measurements were taken on individual FTM devices with channel dimensions (W/L ~ 4.5 μm/30 μm) and Ti/Al (10nm/100nm) source/drain contacts due to the difficulties in probing the monolayer graphene electrodes.

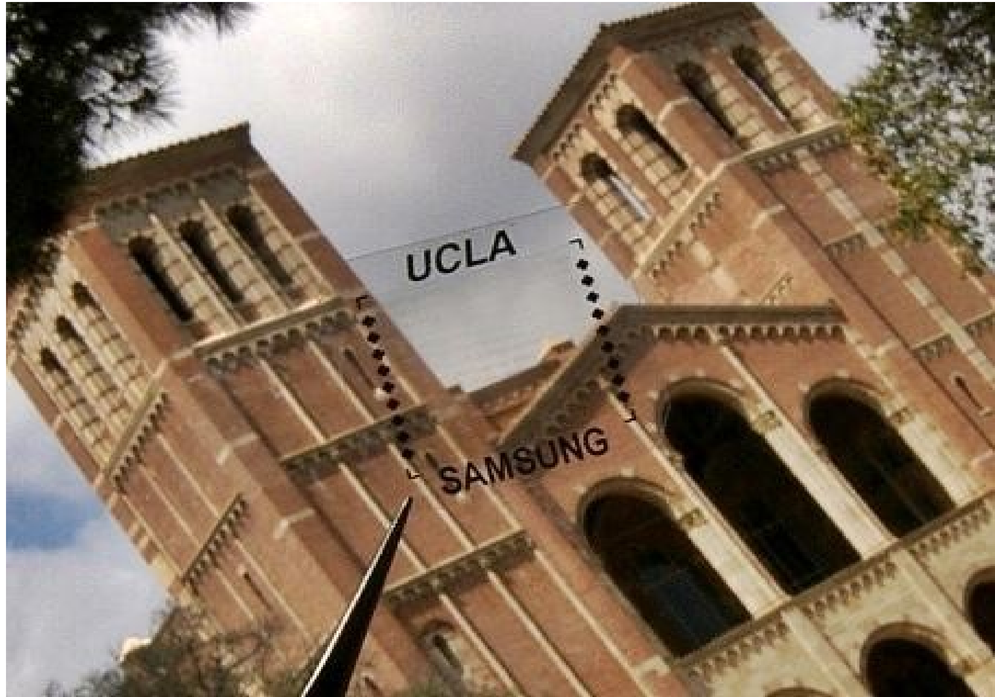


Figure 3.6 Photographs of the large scale transparent-flexible FTM array fabricated on PEN substrate. FTM cell is transparent enough to see objects through it without image distortion.

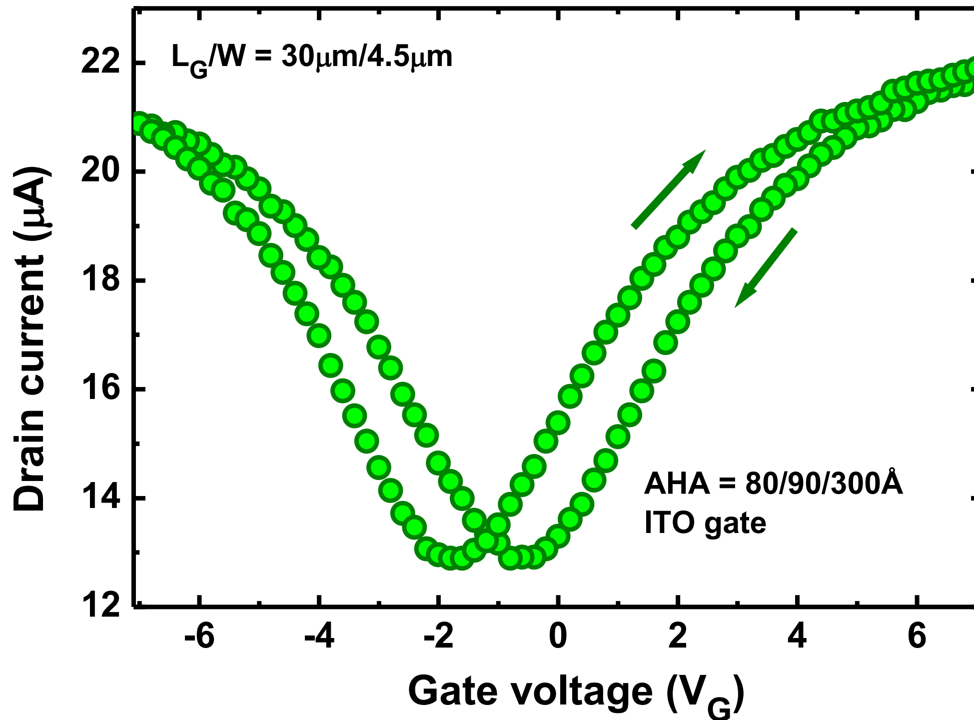


Figure 3.7 I_D-V_G characteristics of FTM. due to the zero-bandgap semiconducting property of graphene Ion/Ioff ratio is less than 3.

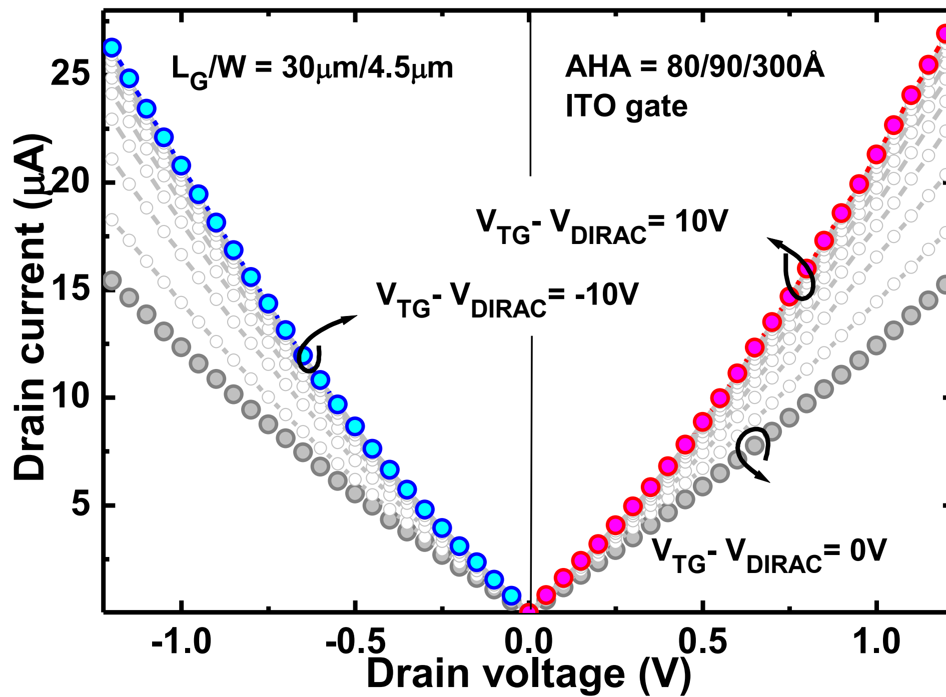


Figure 3.8 I_D-V_D characteristics of FTM. Graphene channel FET with L_G/W=30μm/4.5μm shows high current drivability approaching 28mA.

First, electrical characteristics of the FTM transistors are evaluated. Figure 3.7 and Figure 3.8 show the I_{DS}-V_{GS} and I_{DS}-V_{DS} characteristics of FTM transistor with SLG channel and AHA triple high-k dielectric stack. Due to the zero bandgap semiconducting property of SLG channel, FTM transistor also shows ambipolar characteristics with I_{ON}/I_{OFF} ratio less than 2. The drain current (I_{DS}) of the FTM transistor (gate length/channel width = L_G/W ~ 30 m/9 m) approaches 33 A due to the high carrier mobility of SLG.

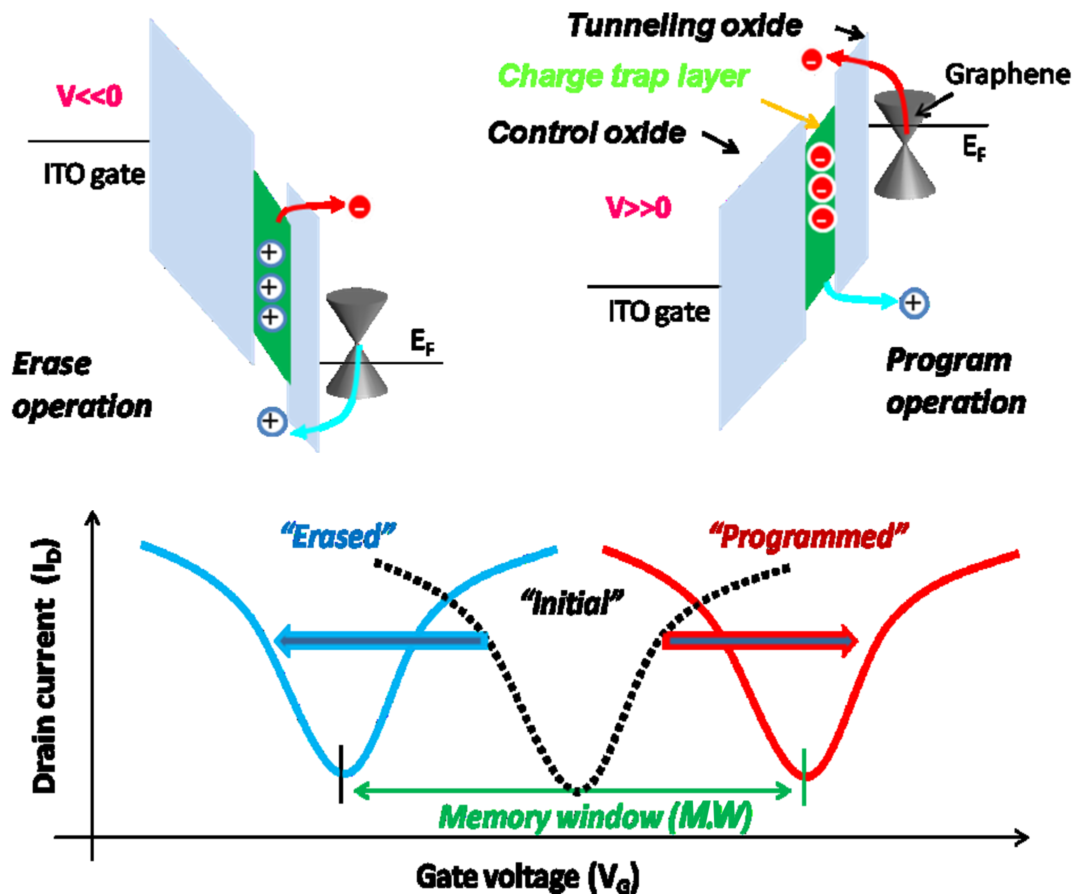
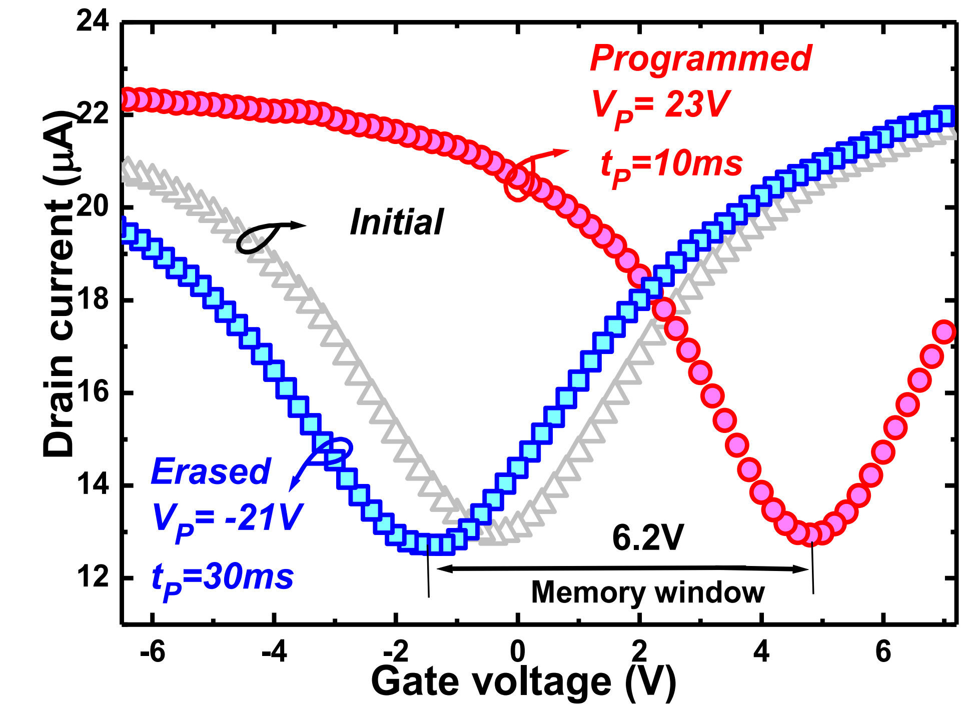


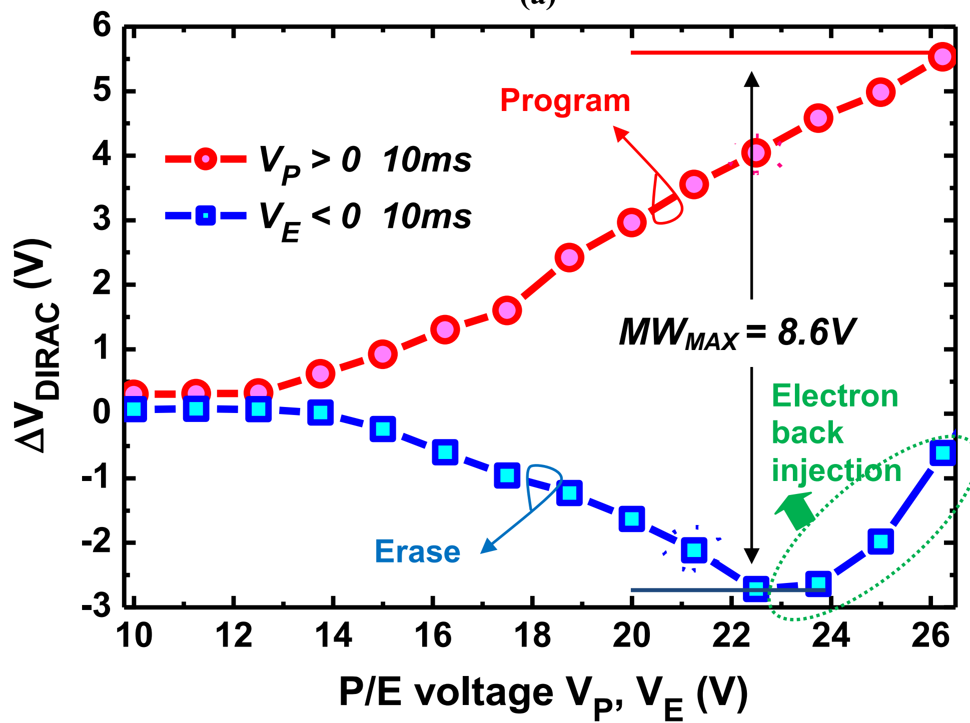
Figure 3.9 Program and erase operation mechanism of FTM. For the programming operation, under the positive V_P, Electrons injected into HfO_2 charge trap layer increases the V_{DIRAC}. During the erasing phase, the applied negative V_E allows the back tunneling of the stored electrons and reduces the V_{DIRAC}. Memory window (MW) is defined by the amount of V_{DIRAC} shift.

3.4.2 FTM memory functions

The operational mechanism of the program/erase mode in our FTM is illustrated in Figure 3.9. In the program (erase) mode, where the gate is under a positive (negative) voltage, the internal electric-field within the gate stack and the thin Al_2O_3 tunneling oxide permits electrons (holes) from the graphene to be injected into the HfO_x charge trap layer. The trapped electrons (holes) effectively dope the graphene to p-type (n-type) and results in a positive (negative) shift of V_{Dirac}. This is shown in Figure 3.10(b), where a positive (negative) shift of V_{Dirac} occurs upon applying a program (erase) voltage pulse of V_P = 23 V (V_E = -21 V). The trapped charges in the charge trap layer modify the energy band alignment of the gate stack and lead to a memory effect in the device characteristics. The change of the electrochemical potential within the gate stack leads to the shift of the Dirac point (ΔV_{Dirac}), from which the memory window (MW) of the FTM can be defined. The memory window of charge-trap memories is determined by the number of trapped charges in the charge storage layer, which rely on the magnitude of program/erase voltages. Thus, we examine the ΔV_{Dirac} at various magnitudes of $|V_{P/E}|$. As shown in Figure 3.10, the memory effect starts at a voltage pulse of $|V_{P/E}|$ ~ 14V and increases monotonically as $|V_{P/E}|$ increases, resulting in a maximum memory window of $MW_{(max)}$ ~8.6 V. However, the ΔV_{Dirac} suddenly reduces after V_E ~ - 24 V. As we discussed in Chapter 2, this is attributed to the electron back-injection from the ITO gate to the charge trap layer via Fowler-Nordheim tunneling [Figure 3.11(inset)]. When a negative erase voltage is applied, the charge trap layer is filled with holes and the back injected electrons compensate the overall positively stored charges, resulting in a reduction of ΔV_{Dirac}.



(a)



(b)

Figure 3.10 (a) Memory characteristics of FTM. (b) Memory window as a function of program/erase voltage. A maximum window (MW) of ~8.6 V is achieved. Electron back injection starts to occur at erase voltage of ~-22 V.

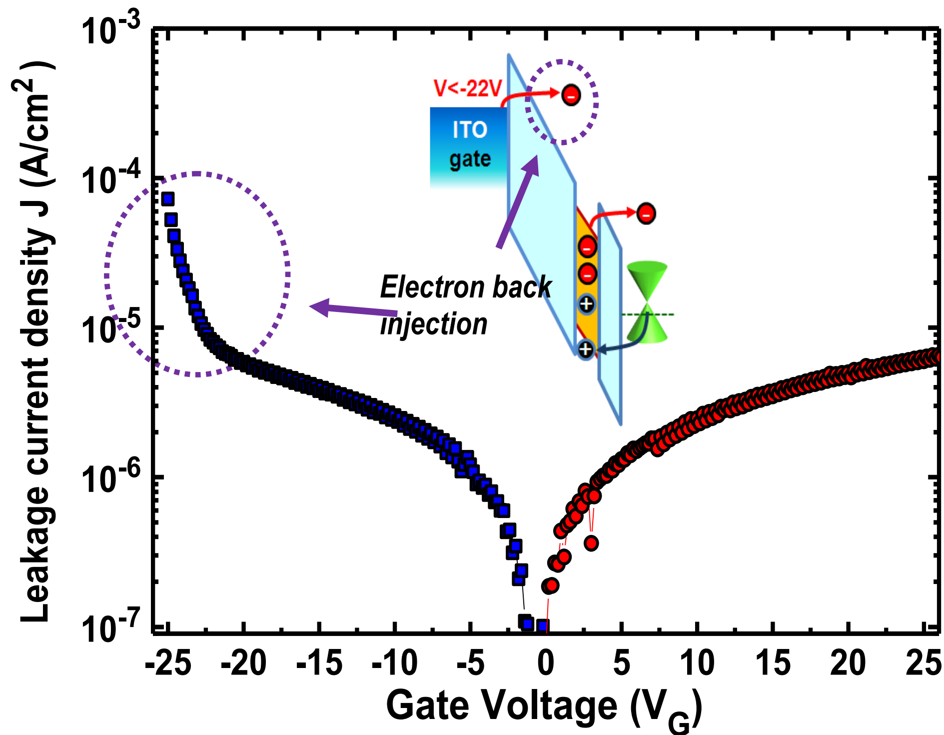


Figure 3.11 Gate tunneling current density. The tunneling mechanism for the standard program/erase operation corresponds to trap-assisted (TA) tunneling and the electron-back injection arises through Fowler-Nordheim (FN) tunneling.

To further investigate the transport mechanism of the device, we measure the gate tunneling current of the FTM. As shown in Figure 3.11, the parabolic dependence shows trap-assisted (TA) tunneling[30] as the normal write/erase mechanism, whereas the linear relation below V_E ~ -24V indicates Fowler-Nordheim (FN) tunneling[30,31] to be responsible for the electron back-injection. To suppress or eliminate such effects, a high work-function gate material would be favorable because it will modify the flat band condition and increase the tunneling barrier of the control oxide layer making it difficult for the back-

injection to occur.[22] Gate stack modification to resolve electron back injection problem will be discussed in next chapter.

In addition to the large memory window, the FTM shows 15% data retention per 10 years at room temperature [Figure 3.12]. At elevated temperatures, the retention characteristics degrade. We noticed that the PEN substrate thermally expands at 85°C. One possibility of such meager retention is the quality of the tunnel oxide formed at low temperatures. Since the glass transition temperature of the PEN substrate is ~ 200°C, we carried out all of the fabrication steps below 110°C. This might cause the formation of point defects in the tunnel oxide layer and diminish the retention characteristics. Thus, optimizing the process to achieve high quality tunnel oxides at low temperature would be vital to improve the retention characteristics.

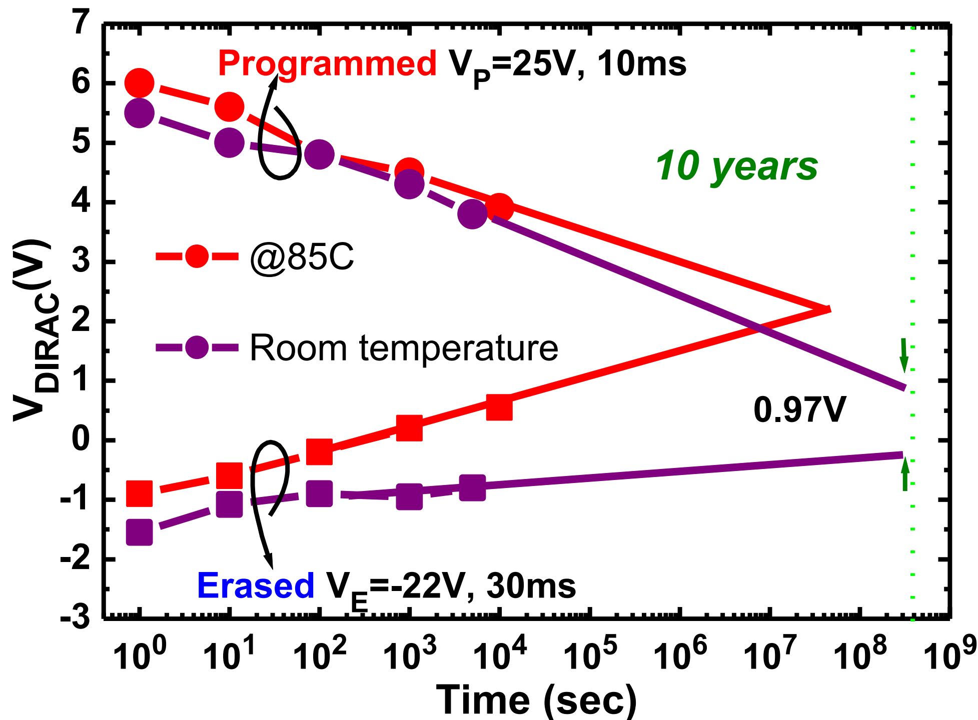


Figure 3.12 Retention characteristics of FTM. The degraded retention characteristics in FTM, compared to the commercial one, might be attributed to the tunneling leakage induced by traps in Al_2O_3 tunneling oxide

3.5. Functional sustainability under geometrical deformation

Flexible electronics require its functions to sustain under geometric deformation. They will need to be rolled or folded to maximize portability and wearability. The extremely large intrinsic breaking strength of 130GPa makes graphene resilient to fracture upon stress.[32]

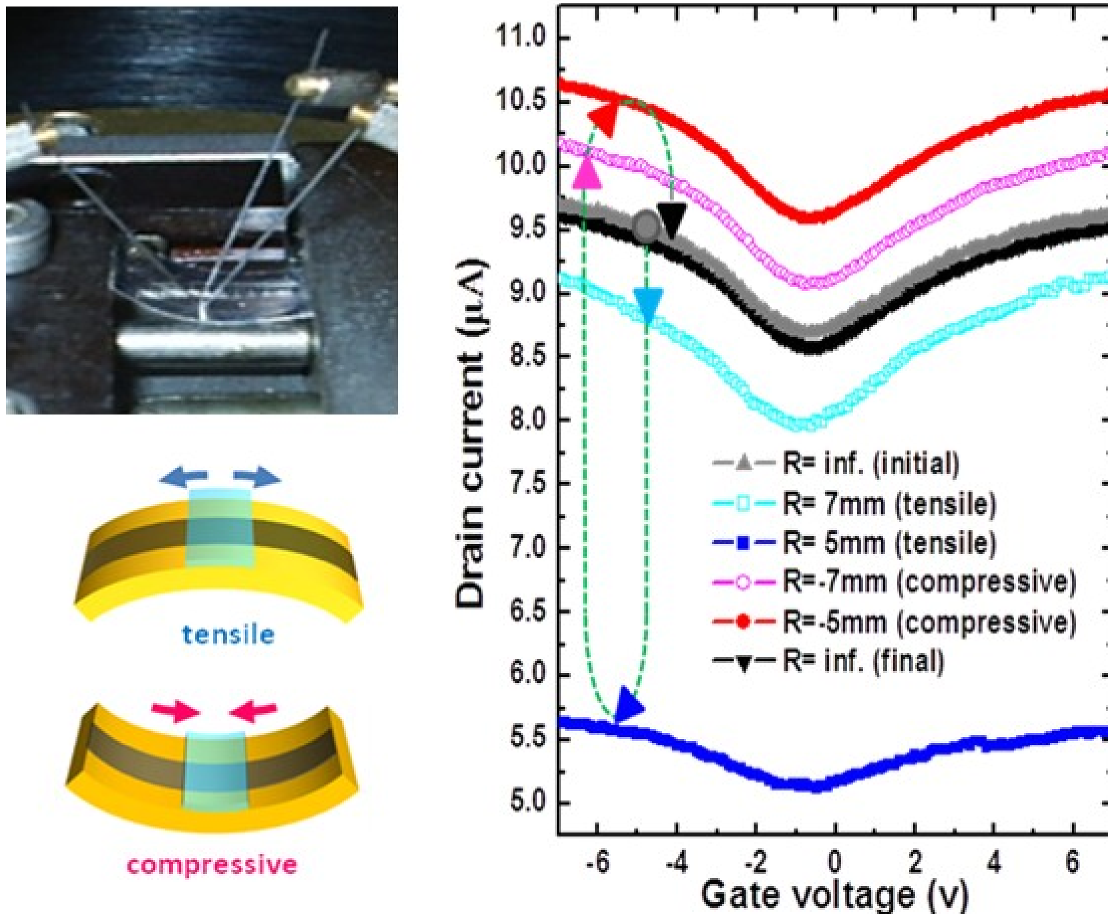


Figure 3.13 Endurance of electrical characteristics under flex. (a) Normalized resistance vs. gate voltage under tensile and compressive stress at $V_D = 1$ V. The FTM reveals minimal Dirac point shift and channel transconductance change under bending.

On the other hand, the high Young's modulus of graphene (~1TPa) is sought to be undesirable for deformation, but the extra degree of freedom perpendicular to its 2D honeycomb lattice makes graphene an exception. In some sense, the flexibility of graphene stems from similar reasons to why graphene exhibits a negative thermal expansion coefficient.[33-35] Since the channel dimension (i.e. overlap region between gate oxide and graphene) is W/L ~ 4.5μm/30μm, the stress effect would be pronounced along the L direction. Thus, we performed the effect of bending stress along the channel direction.

The asymmetric device structure along its vertical direction makes it worthwhile to investigate the impact of both tensile and compressive stress (R_σ: bending radius).

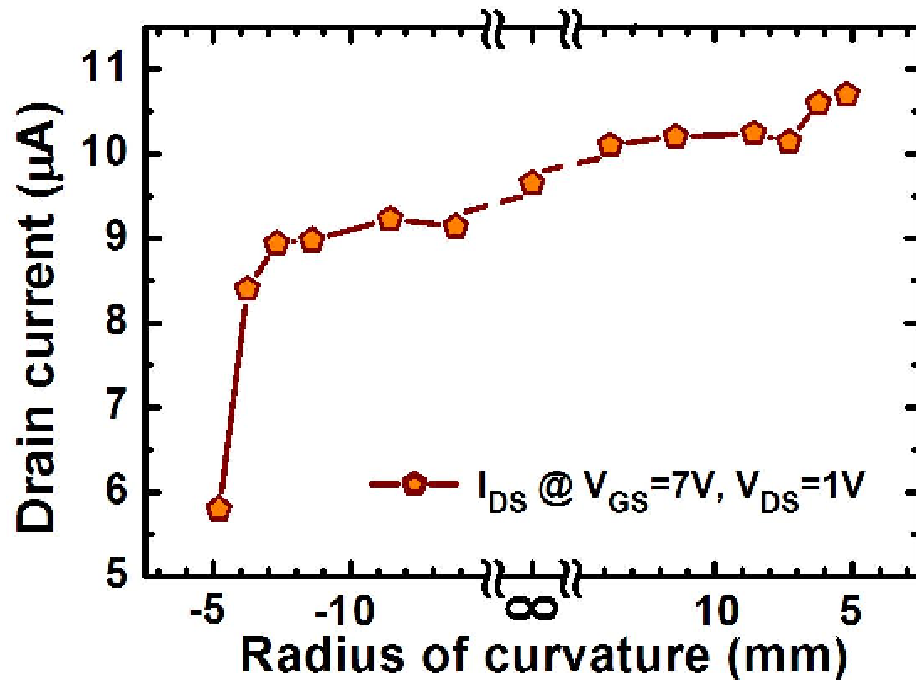


Figure 3.14 On-state current under bending stress measured at V_{DS} = 1V and V_{GS} = 7V. On state current shows little fluctuations within the range of 10% until rolled up with the radius of 7mm. And it restored immediately after stresses are removed

The FTM shows no change in the position of the Dirac point, which suggests the potential profile of the energy bands along the gate electrode and dielectric are stable under bending. Furthermore, no significant change in the slope at the linear regime indicates that the graphene channel is robust under stress. From the channel transconductance ($g_m \propto \mu$), the average electron/hole mobility (μ) of multiple devices is estimated to be ~67cm^2/V·s and varied up to 10% under flex. The slight change in resistance might be due to the contact regions, which requires further investigation. As a consequence, as shown in Figures 3.13 and 3.14, the on-state current measured at V_D = 1 V and V_G = 7V remains steady, while the Dirac point at program (V_P = 23V) and erase (V_E = -21V) states stays unaffected.

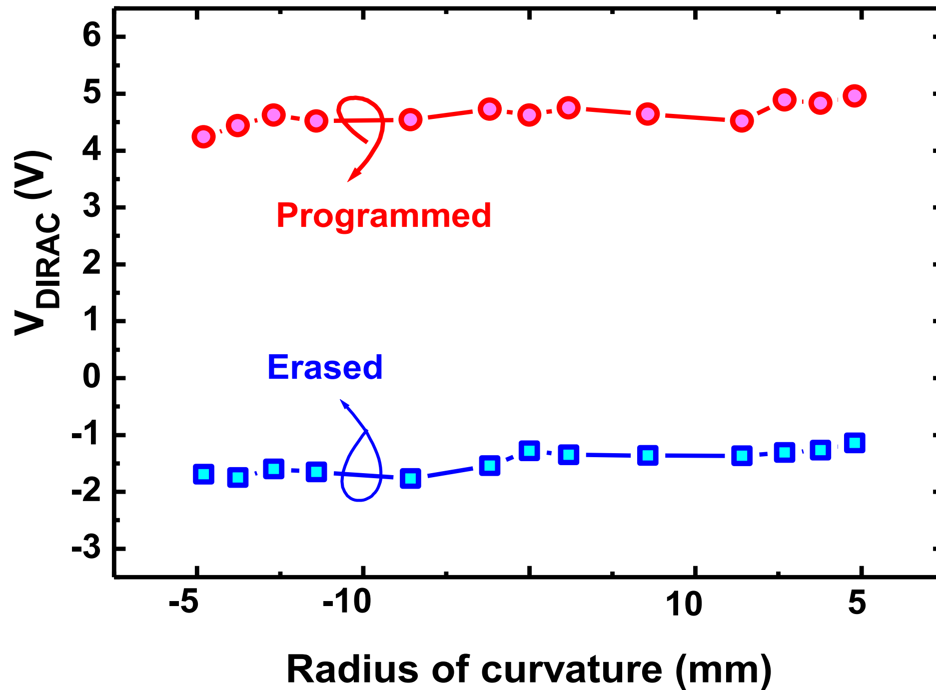


Figure 3.15 Position of Dirac point under bending stress at program/erase states (V_P = 23V, V_E = -21V). No significant dependences of memory characteristics on geometrical deformation were observed.

Here we note that ITO is not a flexible material that inappropriate for fully flexible electronics. Thus, replacing ITO with graphene as the gate material would be beneficial to further improve the flexibility of FTM. The ON/OFF ratio of graphene-based devices is still an ongoing challenge in the graphene community. Several methods have been proposed to create an energy bandgap in this otherwise gapless material. For example, graphene nanoribbons show that a bandgap of ≤50meV can be achieved through quantum confinement effects,[3]6 and bi or trilayer graphene exhibits a bandgap of ≤250meV under high electric fields.[37,38] Implementing such behaviors in our device structure should be the next step to improve the memory performance of graphene based charge trap flash memory structures.

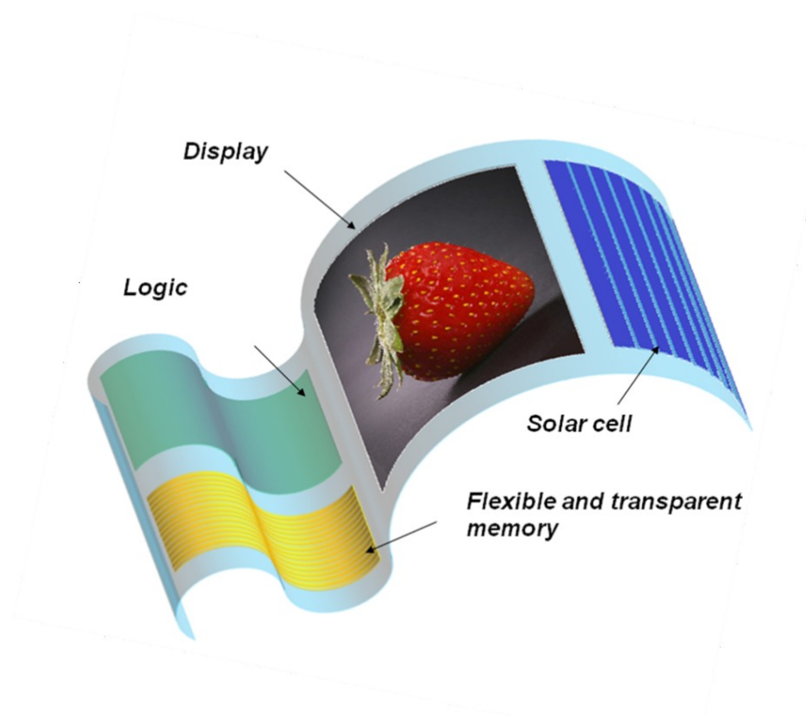


Figure 3.16 FTM can be utilized for transparent and flexible electronics that require integration of logic, memory and display on a single substrate with high transparency and endurance under flex.

Device	**SONOS memory cell (Si-oxide-nitride-oxide-Si)**	**FTM memory cell**
Channel	**Si or Poly-Si**	**graphene**
Charge storage	**Si_3N_4**	**HfO_2, Trap-rich Al_2O_3**
Max. process temperature	**Over than 850C°** (Source drain dopant activation)	**Less than 110C°** (ALD Al_2O_3 growth)
Substrate	**Si wafer (8",12"….)**	**Flexible or transparent substrate.** (plastic, glass) **Much larger than 12"**
Fabrication	**Complicate** (Si process) • Requires many photo-lithography and sophisticated processes • Burdens to etch, gap filling.	**Simple** • No source drain formation step. • Low cost
Memory window	Less than **6V**	Wider than **9V**
Data retention	**Normal**	**Poor (Need to be improved)**

Table 2.1 Comparison of SONOS memory and FTM.

3.6. Summary

In summary, a transparent and flexible graphene charge trap memory composed of a single-layer graphene channel and a 3-dimensional gate stack was fabricated on a poly-ethylene naphtalate substrate the covalently bonded graphene greatly reduces the heat budget and enables fabrication of ultra-high density flexible and transparent FTM cell. The FTM exhibits memory functionality of ~8.6 V memory window and 15% data retention per 10 years, while maintaining ~80% of transparency in the visible wavelength. Under both tensile and compressive stress, the FTM shows minimal effect on the program/erase states and the on-state current. This can be utilized for transparent and flexible electronics that require integration of logic, memory and display on a single substrate with high transparency and endurance under flex.

3.7. Reference

1. B. Cho,S. Song, Y. Ji, T-W. Kim and T. Lee., "Organic Resistive Memory Devices: Performance Enhancement, Integration, and Advanced Architectures," Adv. Funct. Mater., 21, pp. 2806-2829. (2011)
2. S. R. Forrest., The Path to Ubiquitous and Low-Cost Organic Electronic Appliances on Plastic. Nature, 428, pp. 911-918. (2004)
3. D-H. Kim, J-H. Ahn, W. M. Choi, H-S. Kim, T-H. Kim, J. Song, Y. Y. Huang, Z. Liu, C Lu and J. A. Rogers., "Stretchable and Foldable Silicon Integrated Circuits," Science, 320, pp.507-511,(2008)
4.S. Ju, A. Facchetti, Y. Xuan, J. Liu, F. Ishikawa, P. Ye, C. Zhou, T. J. Marks, D. B. Janes., "Fabrication of Fully Transparent Nanowire Transistors for Transparent and Flexible Electronics," Nat. Nanotechnol. , 2, pp.378-384, (2007)
5. W. J. Yu, S. Y. Lee, S. H. Chae, D. Perello, G. H. Han, M. Yun and Y. H. Lee., "Small Hysteresis Nanocarbon-Based Integrated Circuits on Flexible and Transparent Plastic Substrate," Nano Lett., 11, pp.1344-1350, (2011)
6. Q. Cao, H.-s. Kim, N. Pimparkar, J. P. Kulkarni, C. Wang, M. Shim, K. Roy, M. A. Alam and J. A. Rogers., "Medium-Scale Carbon Nanotube Thin-Film Integrated Circuits on Flexible Plastic Substrates," Nature, 454,pp. 495-500, (2008)
7. J. F. Wager, D. A. Keszler and R. E. Presley., "Transparent Electronics," Springer Science: New York, (2010)
8. W. S. Wong and A. Salleo., "Flexible Electronics: Materials and Applications," Springer Science: New York, (2009)
9. F. Schwierz., "Graphene Transistors," Nat. Nanotechnol., 5, pp.487-496, (2010)
10. S. Pang, Y. Hernandez, X. Feng and K. Müllen., "Graphene as Transparent Electrode Material for Organic Electronics," Adv. Mater., 23, pp.2779-2795, (2011)
11. R. A. Barton, J. Parpia and H. G. Craighead., "Fabrication and Performance of Graphene Nanoelectromechanical Systems," J. Vac. Sci. Technol. B, 29, pp.050801-05808, (2011)

12. X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L.Colombo and R. S. Ruoff., "Large-Area Synthesis of High-Quality and Uniform Graphene Films on Copper Foils," Science, 324, pp. 1312-1314, (2009)
13. K. S. Kim, Y. Zhao, H. Jang, S. Y. Lee, J. M. Kim, K. S. Kim, J.-H. Ahn, P. Kim, J.-Y. Choi and B. H. Hong., "Large-Scale Pattern Growth of Graphene Films for Stretchable Transparent Electrodes," Nature, 457, pp. 706-710, (2009)
14. B. J. Kim, H. Jang, S.-K. Lee, B. H. Hong, J.-H. Ahn and J. H. Cho., "High-Performance Flexible Graphene Field Effect Transistors with Ion Gel Gate Dielectrics," Nano Lett., pp. 3464-3466, (2010)
15. S.-K. Lee, B. J. Kim, H. Jang, S. C. Yoon, C. Lee, B. H. Hong, J. A. Rogers, J. H. Cho and J.-H. Ahn., "Stretchable Graphene Transistors with Printed Dielectrics and Gate Electrodes," Nano Lett., 11,pp. 4642-4646, (2011)
16. D. I. Son, T. W. Kim, J. H. Shim, J. H. Jung, D. U. Lee, J. M. Lee, W. I. Park and W. K. Choi., Flexible Organic Bistable Devices Based on Graphene Embedded in an Insulating Poly(methyl methacrylate) Polymer Layer. Nano Lett., 10, pp. 2441-2447, (2010)
17. Y. Ji, S. Lee, B. Cho, S. Song and T. Lee., "Flexible Organic Memory Devices with Multilayer Graphene Electrodes," ACS Nano, 5, pp. 5995-6000, (2011)
18. H. Y. Jeong, J. Y. Kim, J. W. Kim, J. O. Hwang, J.-E. Kim, J. Y. Lee, T. H. Yoon, B. J. Cho, S. O. Kim, R. S. Ruoff and S. Y. Choi., "Graphene Oxide Thin Films for Flexible Nonvolatile Memory Applications," Nano Lett., 10, pp. 4381-4386, (2010)
19. I. Jeon, H. Yang, S.-H. Lee, J. Heo, D. H. Seo, J. Shin, U. I. Chung, Z. G. Kim, H.-J. Chung and S. Seo., "Passivation of Metal Surface States: Microscopic Origin for Uniform Monolayer Graphene by Low Temperature Chemical Vapor Deposition," ACS Nano., 5, pp. 1915-1920, (2011)
20. B. J. Kim, H. Jang, S-K Lee, B. H. Hong, J-H Ahn and J. H. Cho, "High-Performance Flexible Graphene Field Effect Transistors with Ion Gel Gate Dielectric." Nano Lett., pp. 3464–3466, (2010)

21. E. B. Song, B. Lian, S. M. Kim, S. Lee, T.-K. Chung, M. Wang, C. Zeng, G. Xu, K. Wong, Y. Zhou et al., "Robust Bi-Stable Memory Operation in Single-Layer Graphene Ferroelectric Memory," Appl. Phys. Lett., 99, pp. 042109-04212, (2011)
22. S. Lee, E. B. Song, S. Kim, D. H. Seo, S. Seo, T. W. Kang and K. L. Wang., "Impact of Gate Work-Function on Memory Characteristics in $Al_2O_3/HfO_x/Al_2O_3$/Graphene Charge Trap Memory," Appl. Phys. Lett., 100, pp. 023109-023112, (2012).
23. S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tutuc and S. K. Banerjee., "Realization of a High Mobility Dual-gated Graphene Field-effect Transistor with Al_2O_3 Dielectric," Appl. Phys. Lett., 94, 062107-062111, (2009)
24. K. Ellmer, A. Klein and B. Rech, "Transparent Conductive Zinc Oxide: Basics and Applications in Thin Film Solar Cells," Springer: Berlin, Heidelberg, (2010)
25. D. Lee, J. Yi, W. Lee, U. Paik, J. Rogers and W. Park., "Optical Properties of Laterally Aligned Si Nanowires for Transparent Electronics Applications," Nano Research, 4, pp.817-823, (2012)
26. F. N. Ishikawa, H.-k. Chang, K. Ryu, P.-c. Chen, A. Badmaev, L. Gomez De Arco, G. Shen, C. Zhou., "Transparent Electronics Based on Transfer Printed Aligned Carbon Nanotubes on Rigid and Flexible Substrates," ACS Nano, 3, pp.73-79, (2009)
27. H. Yin, S. Kim, C. J. Kim, I. Song, J. Park, S. Kim and Y. Park., "Fully Transparent Nonvolatile Memory Employing Amorphous Oxides as Charge Trap and Transistor's Channel Layer," Appl. Phys. Lett., 93, pp.172109-1721012, (2008)
28. T. Uchida, S. Kaneta, M. Ichihara, M. Ohtsuka, T. Otomo and D. R. Marx., "Flexible Transparent Organic Light Emitting Devices on Plastic Films with Alkali Metal Doping as Electron Injection Layer," Jpn. J. Appl. Phys., 44, pp.L282-L284, (2005)
29. Y. Yang, S. Jeong, L. Hu, H. Wu, S. W. Lee and Y. Cui., "Transparent Lithium-Ion Batteries," Proc. Natl. Acad. Sci., 108, pp.13013-13018, (2011)
30. M. Porti, M. Avidano, M. Nafria, X. Aymerich, J. Carreras and B. Garrido., "Conduction Mechanisms and Charge Storage in Si-Nanocrystals Metal-Oxide-Semiconductor Memory Devices Studied with Conducting Atomic Force Microscopy," J. Appl. Phys., 98, pp.056101-056104, (2005)

31. G. Chakraborty, S. Chattopadhyay, C. K. Sarkar and C. Pramanik., "Tunneling Current at the Interface of Silicon and Silicon Dioxide Partly Embedded with Silicon Nanocrystals in Metal Oxide Semiconductor Structures," J. Appl. Phys., 101, 024315, (2007)
32. C. Lee, X. Wei, J. W. Kysar and J. Hone., "Measurement of the Elastic Properties and Intrinsic Strength of Monolayer Graphene," Science, 321, pp.385-388, (2008)
33. W. Bao, F. Miao, Z. Chen, H. Zhang, W. Jang, C. Dames and C. N. Lau., "Controlled Ripple Texturing of Suspended Graphene and Ultrathin Graphite Membranes," Nat. Nanotechnol., 4, pp.562-566, (2009)
34. Yoon, D.; Son, Y.-W.; Cheong, H., Negative Thermal Expansion Coefficient of Graphene Measured by Raman Spectroscopy. Nano Lett., 11, pp.3227-3231, (2011)
35. N. Mounet and N. Marzari., "First-Principles Determination of the Structural, Vibrational and Thermodynamic Properties of Diamond, Graphite, and Derivatives," Phys. Rev. B, 71, pp.205214-205148, (2005)
36. T. Shimizu, J. Haruyama, D. C. Marcano, D. V. Kosinkin, J. M. Tour, K. Hirose, and K, Suenaga., "Large intrinsic energy bandgaps in annealed nanotube-derived graphene nanoribbons," Nat. Nanotechnol., 6, 45-50, (2011)
37. Y. Zhang, T.-T. Tang, C. Girit, Z. Hao, M. C. Martin, A. Zettl, M. F. Crommie, Y. R. Shen and F. Wang., "Direct observation of a widely tunable bandgap in bilayer graphene," Nature, 459, pp.820-823, (2009)
38. C. H. Lui, Z. Li, K. F. Mak, E. Cappelluti and T. F. Heinz., "Observation of an electrically tunable band gap in trilayer graphene," Nat. Phys., 7, pp.944-947, (2011)

Chapter 4

Embedded Oxide Trap memory (EOTM) using graphene as channel

4.1. Motivation

FTM with AHA triple high-k stack has showed excellent characteristics with large memory window. But it has had electron back injection issue that limits erase voltage. As we demonstrated in Chapter 2, back electron injection from gate electrode can be alleviated by the adoption of high work function (Φ_M) metal gate electrode. But for the application to fully flexible and transparent electronics, adoption of graphene might be required not only for channel but also for gate electrode. [Figure 4.1] Graphene has low Φ_M around 4.5eV, graphene gate electrode might cause serious electron back injection problem as well when it integrated with AHA triple high-k dielectric. So, it has been needed to find other way which can effectively suppress the electron back injection without changing gate material. In this chapter, we show memory operation in a flexible-transparent graphene charge-trap memory composed of a single-layer graphene channel and trap rich Al_2O_3 data storage layer effectively suppress the electron back injection.

4.2. EOTM structure and fabrication process flow

The schematic structure of EOTM memory is shown in Figure 4.2. FTM is fabricated through a multi-step procedure as shown in Figure 4.3 at temperatures below

110°C to prevent the thermal deformation of PEN substrate. SLG was grown on a copper film by chemical vapor deposition (CVD)[4] and transferred onto a PEN substrate. Active channel regions were then patterned by photolithography and etched through oxygen plasma. After the deposition of 15-nm-thick Al_2O_3 by atomic-layer-deposition, oxygen ion-bombardment (OIB) is carried out using reactive ion etching (RIE) to form a trap-rich Al_2O_3 (AlO_x) charge storage layer. This OIB process generates trap sites such as vacancies and interstitials in the Al_2O_3 layer.[5] It was little difficult to measure the depth of oxygen ion bombardment damage directly. So, we measured transistor characteristics controlled by back gate electrode before and after OIB process. As we can see in this Figure 4.5, there was no significant reduction I-V current. This result reflects that graphene channel remained intact after OIB process.

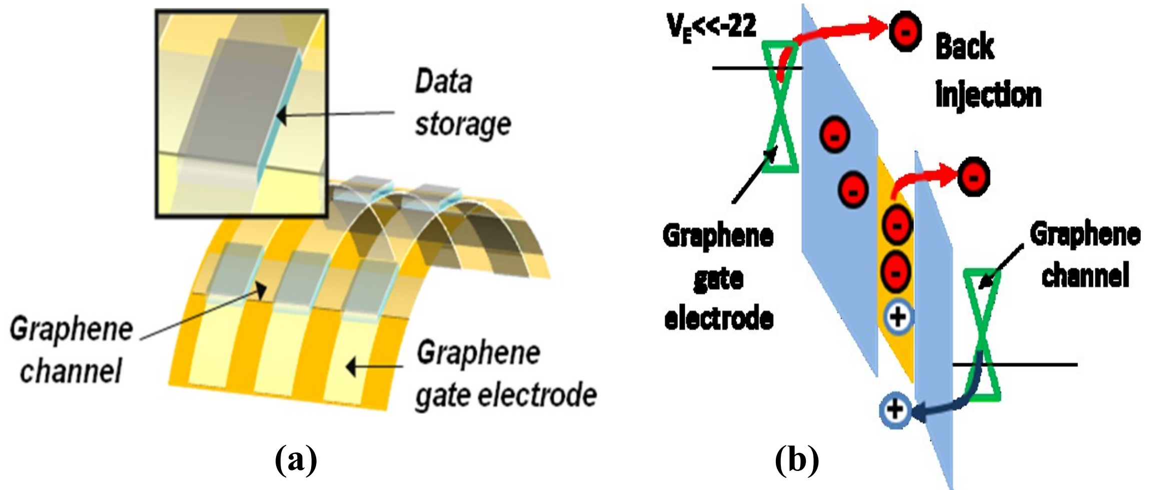


Figure 4.1 (a) Schematic diagram of fully flexible memory cell structure using graphene as channels and gate electrodes. (b) Illustration of electron back injection caused from the low work-function of graphene gate electrode. For the fully flexible and transparent electronics application, adoption of graphene gate electrode is desirable, but graphene gate electrode might cause serious electron back injection problem as well when it integrated with AHA triple high-k dielectric.

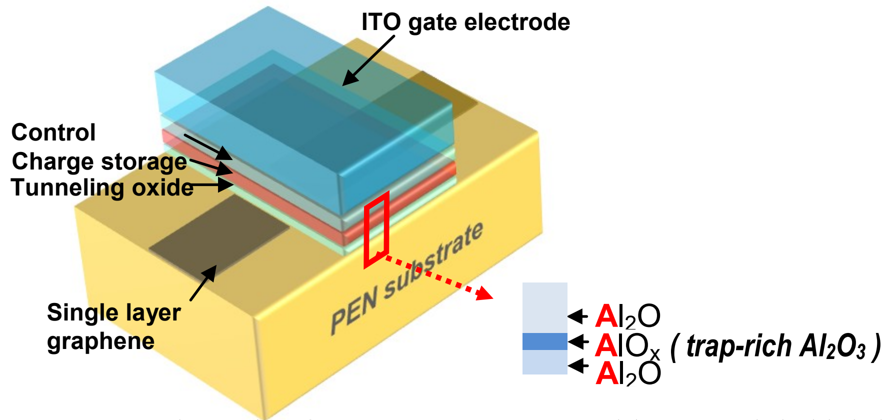


Figure 4.2. Schematic of EOTM test structure with AAA triple high-k stack. To achieve more stable erase condition, and wider MW, For EOTM, HfO_2 charge trap layer of FTM is replaced by trap-rich Al_2O_3 layer.

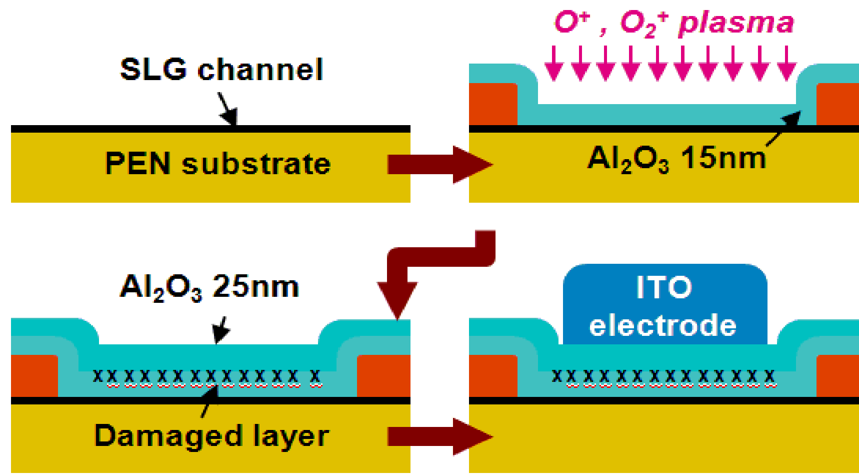


Figure 4.3 Fabrication procedure of transparent-flexible EOTM (AAA). For EOTM charge storage is formed by ion bombardment (OIB) process. The OIB process turns deposited Al_2O_3 layer into trap-rich Al2O3 generating vacancies and interstitials

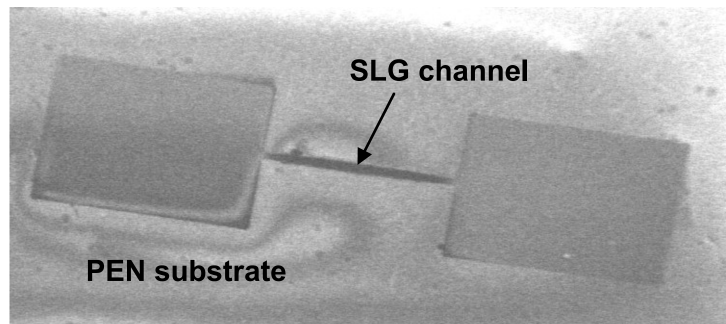
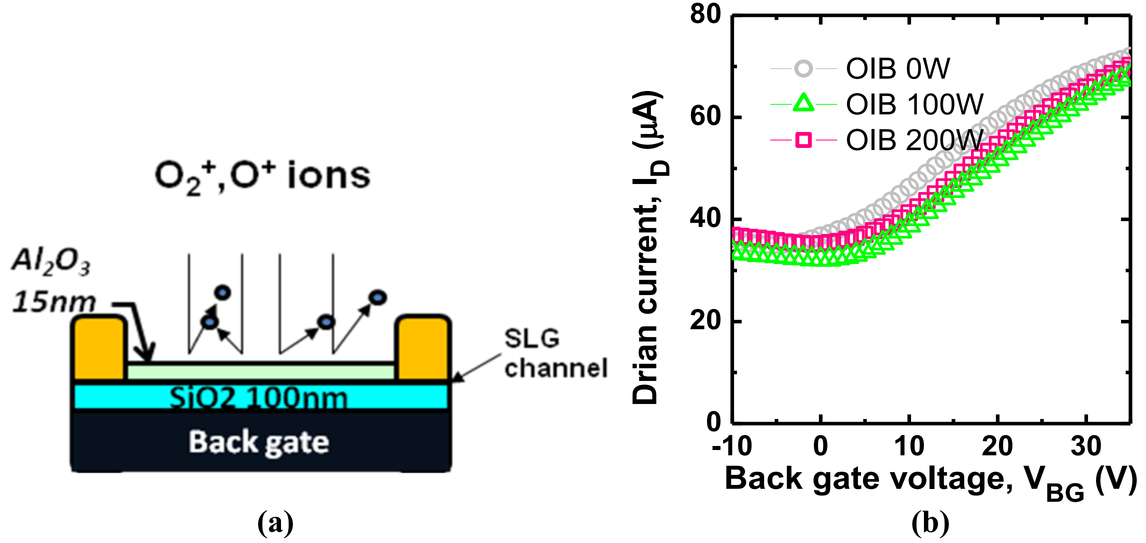


Figure 4.4 SEM image of FTM active region formed on PEN flexible and transparent substrate.

Then, a control oxide of 25-nm-thick Al_2O_3 is deposited. Finally, the ITO gate electrodes are formed using a sputtering process.



(a) (b)

Figure 4.5 (a) Transistor characteristics controlled by back gate electrode before and after OIB process. (b) No significant reduction drain current was observed. This result reflects that the depth of OIB is shallower than 15nm and graphene channel remained intact after OIB process.

4.3. Electrical characteristics of EOTM

First, electrical characteristics of the EOTM transistors are evaluated. Figure 4.6 show the I_{DS}-V_{GS} and I_{DS}-V_{DS} characteristics of EOTM transistor with SLG channel and AAA dielectric. The drain current (I_D) of the EOTM transistor (gate length/channel width = $L_G/W \sim 30$ m/9 m) approaches 33 A due to the high carrier mobility of SLG. In principle, EOTM is a charge trap memory that has a similar operation mechanism to Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) memory. Figure 4.7 shows the memory function of EOTM with AAA. The EOTM was programmed and erased by a positive voltage stress (V_P) of 28V and by a negative voltage stress (V_E) of -28V for 10ms on the

ITO gate electrode. The memory window (MW) of the two states is approximately 7.2V, which is wider than conventional SONOS memory.[6]

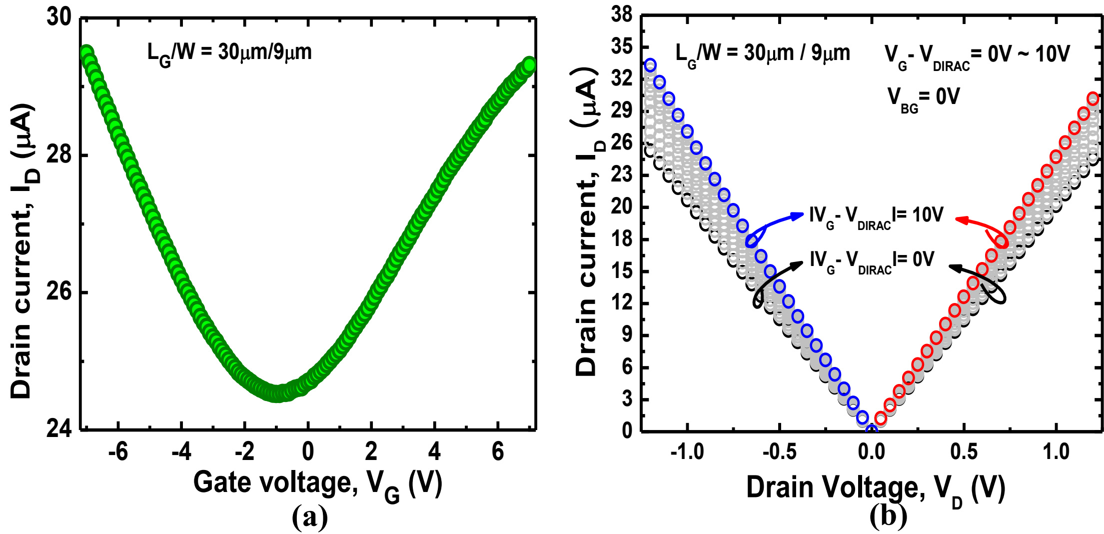


Figure 4.6 (a) I_{DS}-V_{GS} and (b) I_{DS}-V_{DS} characteristics of EOTM with SLG channels. EOTM transistor with L_G/W=15μm/7μm shows current drivability approaching 85μA.

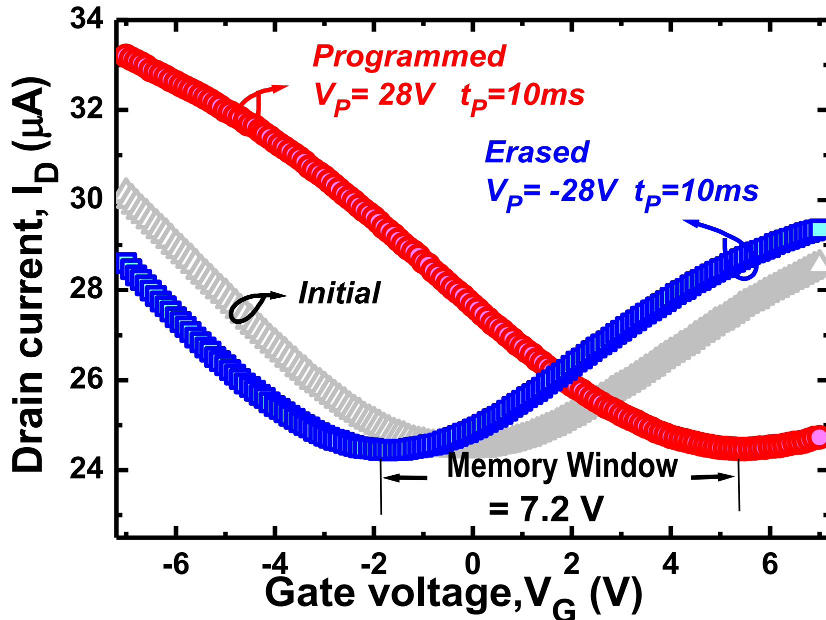


Figure 4.7 Memory function of EOTM sample fabricated on flexible and transparent PEN substrate.

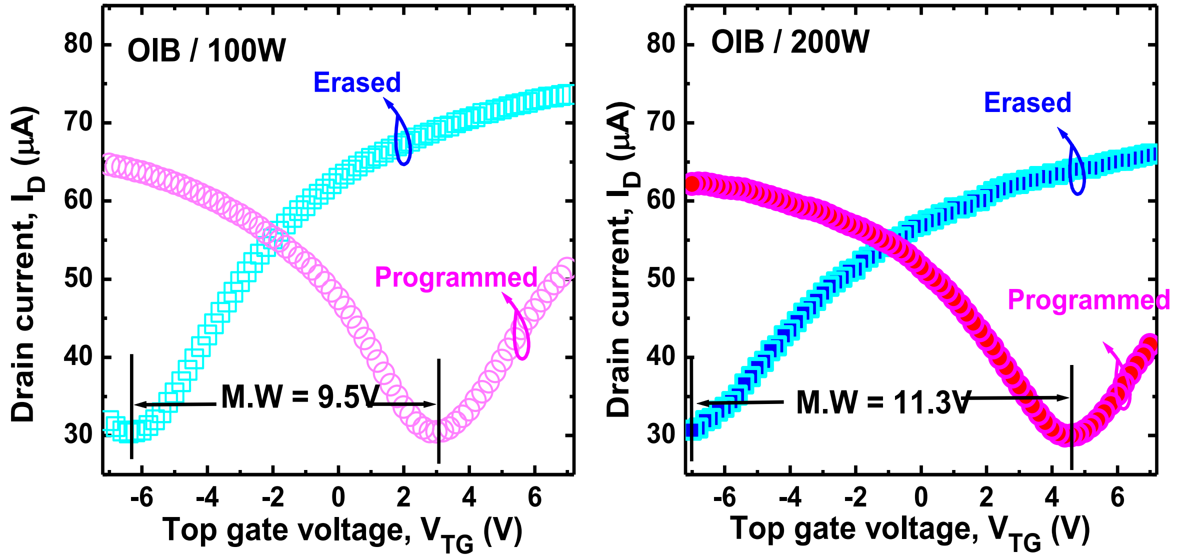


Figure 4.8 Comparison of memory characteristics depends on OIB power, EOTM fabricated with higher OIB process showed wider memory window. The MW of 11.3V for 200W and 9.5V for 100W are achieved by using a P/E conditions of V_P=24V, 10ms and V_E=-22V, 30ms.

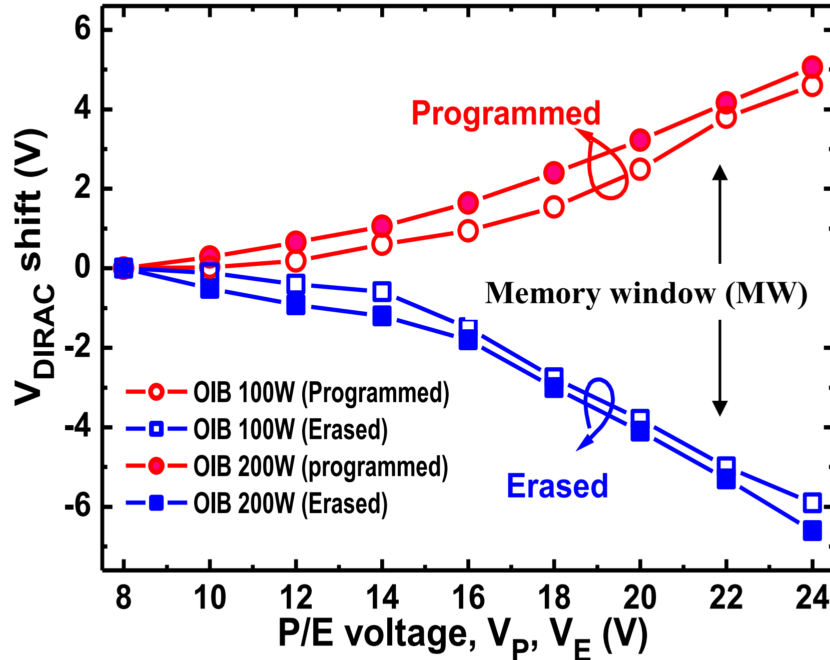


Figure 4.9 V_{DIRAC} shifts depend on the program and erase voltage (V_P and V_E). EOTM samples fabricated with higher OIB power shows wider MW.

Figure 4.7 shows the memory function of EOTM with AAA. The EOTM was programmed and erased by a positive voltage stress (V_P) of 28V and by a negative voltage stress (V_E) of -28V for 10ms on the ITO gate electrode.

The memory window (MW) of the two states is approximately 7.2V, which is wider than conventional SONOS memory.[6] Figure 4.8 and 4.9 show the memory characteristics of the EOTM devices fabricated on Si substrates, depending on the OIB power during the formation of AlO_x charge storage layers. The memory window (MW), which is defined by the V_{Dirac} shift (ΔV_{Dirac}), is ~9.5 and ~11.3V in the gEOTM devices consisting of the AlO_x layers formed under the OIB power of 100 and 200W, respectively.

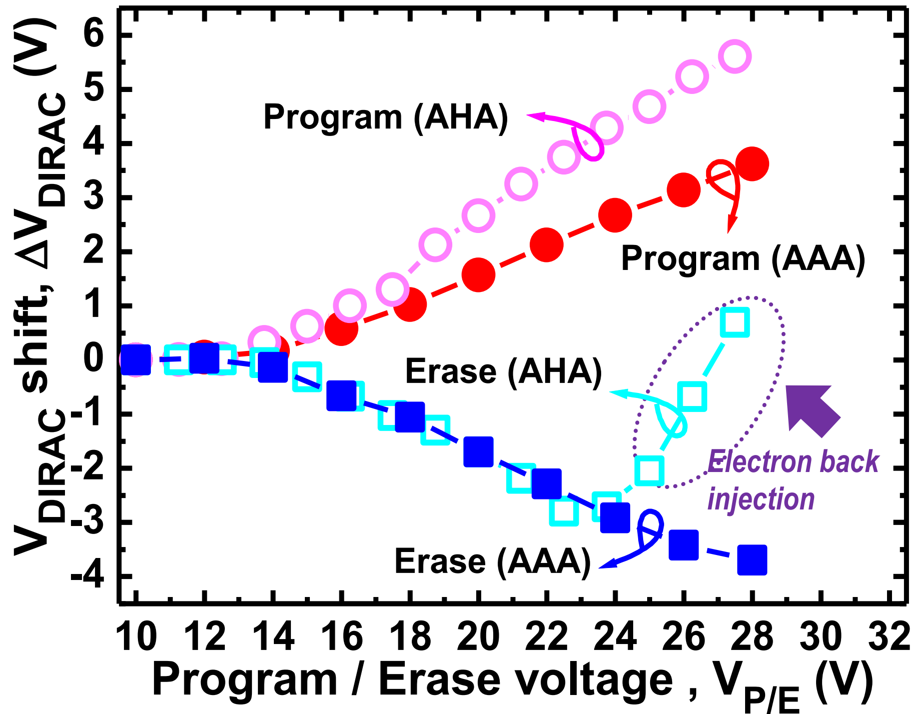


Figure 4.10 V_{DIRAC} shifts depending on the program and erase voltage (V_P and V_E). Adoption of AAA effectively suppresses electron back injection from the gate electrode.

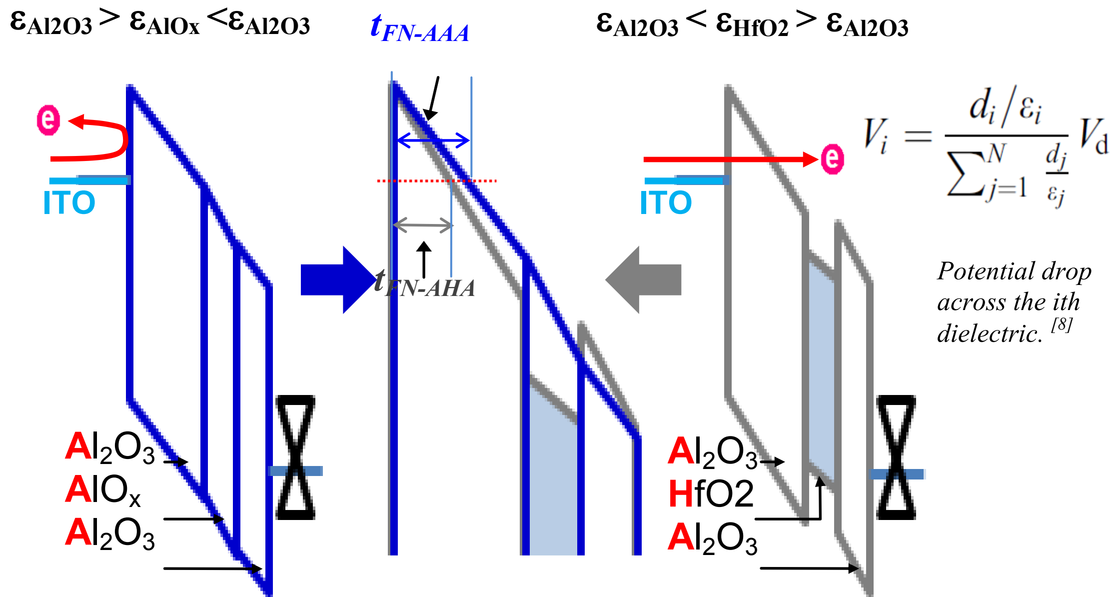


Figure 4.11 A low dielectric constant of AlO_x results in a larger potential drop across the charge storage layer and reduces the slope of the conduction band in the control oxide. Hence, the thickness of the F-N tunneling barrier increases making it difficult for the electron back injection to occur.

Figure 4.10 compares the V_{DIRAC} shift of EOTMs with AAA and AHA layers depending on V_P and V_E. As shown in 4.10, V_{DIRAC} shifts towards the positive direction with an increase of programming voltages and V_{DIRAC} shifts towards the negative direction with an increase of erasing voltages. In the FTM, a negative gate voltage stress of -22V starts to generate electron back injection from the gate electrode. One way to alleviate this is by replacing the AHA with AAA. The trap-rich Al_2O_3 formed by OIB has lower dielectric constant (   ) than the pure Al_2O_3. This creates a larger potential drop across the storage layer [8] and reduces the conduction band slope of the control oxide. Therefore, the FTM with AAA stack has a thicker F-N tunneling barrier (t_{FN}) making it difficult for

electron back injection to happen at large V_E. This promotes stable erase operations up to -28V. [Figure 4.11]

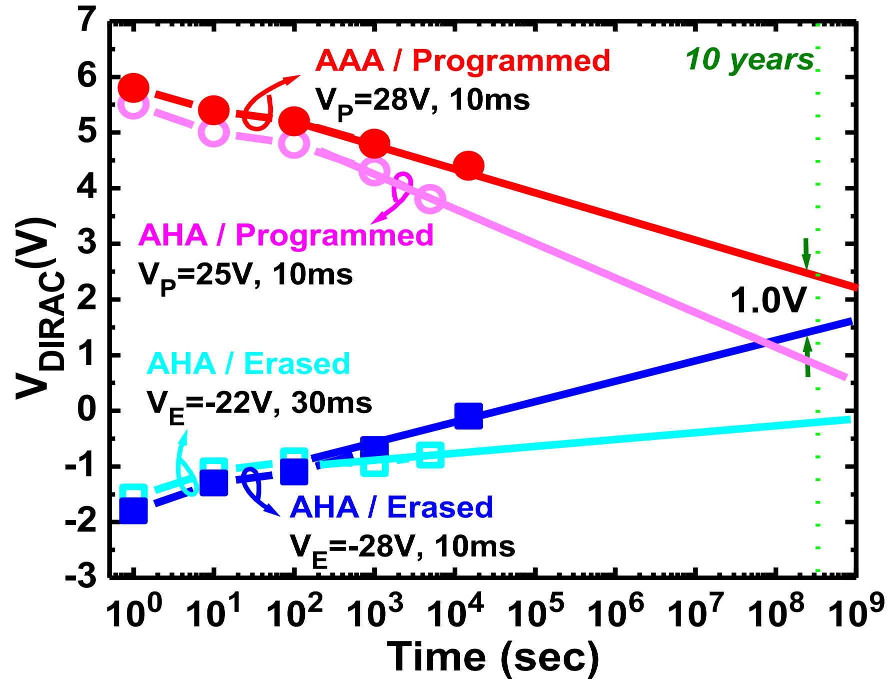


Figure 4.12 Data retention characteristics of FTMs with different charge storage layers. FTMs can maintain memory window of 1V up to 10 years.

4.4. Summary

The graphene channel flexible and transparent non-volatile-memory devices with Al_2O_3 gate oxide layer, in which an ion-bombarded AlO_x data storage have been successfully fabricated through low thermal budget processes. The EOTM shows excellent electrical characteristics with memory window larger than 7.2V. Adoption of AAA Triple high-k stack effectively suppressed electron back injection from gate electrode. This technology has great great potential to be used as an ultra high density

memory cell for flexible electronics. EOTM could pave the way for completely see-through flexible electronics and change the paradigm of future electronics.

4.5. Reference

[1] J. Jang, H-S. Kim, W. Cho, H Cho, J. Kim, S. I. Shim, Y. Jang, J-H. Jeong, B-K. Son, D. W. Kim, J-J. Shim, J. S. Lim, K-H. Kim, S. Y. Yi, J-Y Lim, D. Chung, H-C Moon, S Hwang, J-W Lee, Y-H Son, U-I. Chung and W-S Lee., "Vertical cell array using Terabit Cell Array Transistor technology for ultra high density NAND flash memory" Tech. Digest. VLSI Tech. symposium pp.192-193 (2009).

[2] S. Bae, H. Kim, Y. Lee, X. Xu, J-S. Park, Y. Zheng, J. Balakrishnan, T. Lei, H. R. Kim, Y. I. Song, Y-J. Kim, K. S. Kim, B. Özyilmaz, J-H Ahn, B. H. Hong and S. Iijima "Roll-to-roll production of 30-inch graphene films for transparent electrodes", Nature Nanotechnology 5, pp.574–578 (2010)

[3] K. S. Kim, Y. Zhao, H. Jang, S. Y. Lee, J. M. Kim, K. S. Kim.6, J-H. Ahn, P. Kim, J-Y. Choi and B. H. Hong., "Large-scale pattern growth of graphene films for stretchable transparent electrodes", Nature 457, pp. 706-710 (2009)

[4] S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tutuc and S. K. Banerjee., " Realization of a high mobility dual-gated graphene field-effect transistor with Al_2O_3 dielectric", Applied Physic Letter 94, 062107 (2009)

[5] J. R. Weber, A. Janotti and C. G. Van de Walle., "Native defects in Al_2O_3 and their impact on III-V/Al2O3 metal-oxide-semiconductor-based devices" Journal of Applied Physics 109, pp.033715-033720, (2011)

[6] S. Jeon, S. Choi, H. Park, H. Hwang, J. H. Han, H. Chae, S. D. Chae, J. H. Kim, M. K. Kim, Y. S. Jeong, Y. Park, S. Seo, J. W. Lee and C. W. Ki, "Triple high-K stacks ($A1_20_3/Hf0_2/Al_20_3$) with high pressure H2 and D2 annealing for SONOS type flash

memory device applications", Tech. digest of IEEE Conf. on Nanotech. pp. 53-55 (2004)

[7] S. M. Kim, S. Seo, E. B. Song, D. H. Seo, H. Seok and K. L. Wang, "Non-volatile graphene channel memory (NVGM) for flexible electronics and 3D multi-stack ultra-high-density" data storages Tech. Digest of VLSI Tech. Symposium, pp.118–119. (2011)

[8] B. Govoreanu, P. Blomme, M. Rosmeulen, J. Van Houdt and K. De Meyer., "A model for tunneling current in multi layer tunneling current," Solid-State Electronics 47, pp.1045–1053 (2003)

Chapter 5

Suspended few-layer Graphene beam electro-mechanical Switch (SGS) with abrupt on-off characteristics and minimal leakage current

5.1. Introduction

Graphene has recently received great attention for its unique electronic and mechanical properties [1-2] and has been considered as a promising candidate to replace conventional semiconducting materials used in metal-oxide-semiconductor field-effect transistors (MOSFET) and MEMS/NEMS devices. Graphene FETs, however, possess fundamental issues, such as high off-leakage current, because of its semi-metallic zero bandgap electronic structure. Mechanical switching, on the other hand, enables electronic systems to operate with a zero off-leakage current and an abrupt on-off transition,[3-5] which can both reduce the static and dynamic power consumption in electronic switching devices.[6] By incorporating MEMS/NEMS devices into CMOS circuits the inherent problems in short-channel devices can be resolved.[7-9]

In order to reduce the switching voltage and speed of mechanical switches, the moving parts need to be miniaturized and thinned. In general, three-dimensional (3D) materials, such as metals or poly-Si, have been used for the active part of NEMS/MEMS devices.[Figure 5.1] However, they become brittle when they are scaled down to

nanometers. [Figure 5.2] Contrarily, 1D and 2D materials, such as carbon-nanotubes and graphene, sustain its mechanical properties even at the nanoscale.[10-13] Moreover, they exhibit outstanding electronic properties suitable for low-power and high-speed MEMS/NEMS applications.

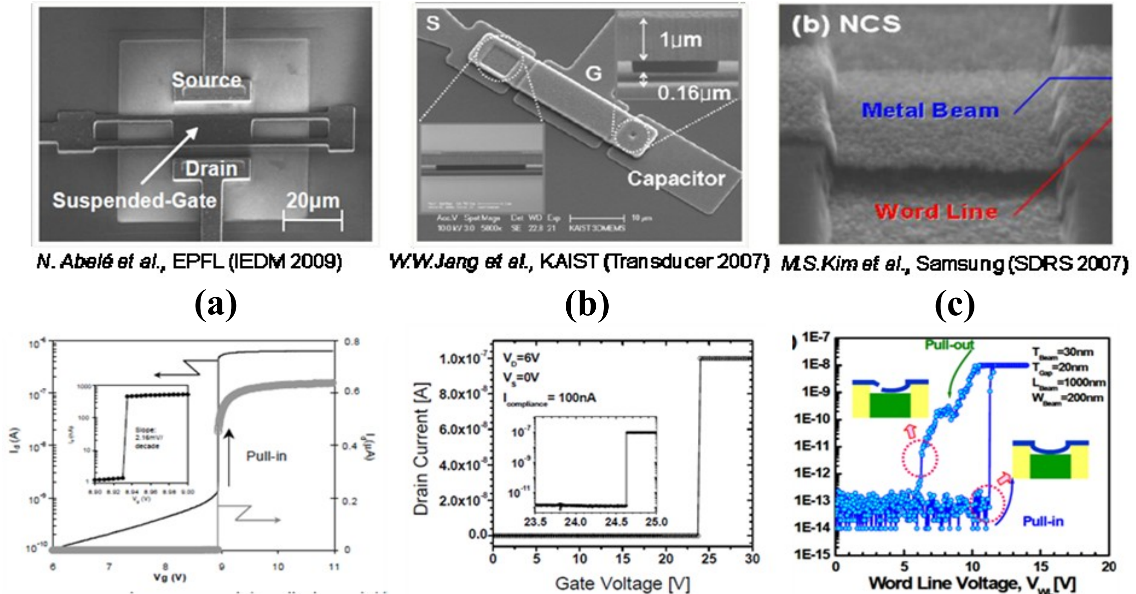


Figure 5.1 Various types of poly-crystalline material based MEMS devices and their switching characteristics. Moving parts of MEMS switch have been made of poly-crystalline materials such as (a,b) poly-Si or (b) metal (TiN). For this reason, pull-in voltages of conventional MEMS switches are still too high to be integrated with CMOS circuits.

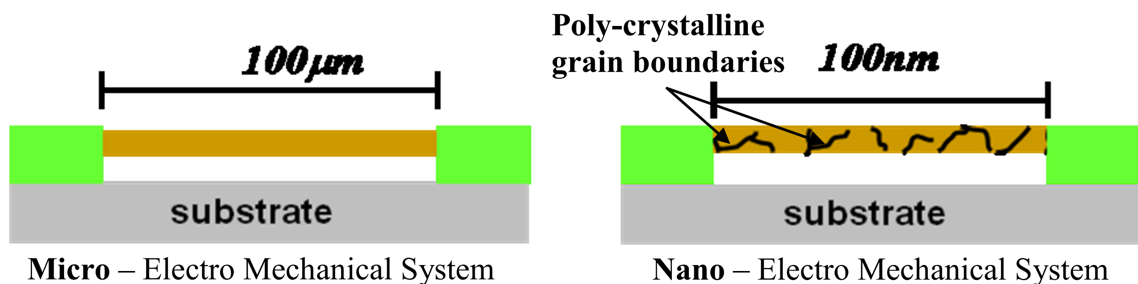


Figure 5.2 Comparison of (a) MEMS and (b) NEMS suspended beam structure. The size of the moving part become comparable to the size of poly-crystalline grain when it scaled down bellow hundred nanometer regimes. Durability of moving part is degraded mainly due to the cracks originates from grain boundaries.

Recently, large scale pattern growth of graphene technology has been demonstrated and could provide effective solutions satisfying selectivity and mass production.[14]

In this chapter, we present a unique fabrication method and the switching characteristics of suspended few-layer graphene (FLG) beam mechanical switches with ideal-like on/off characteristics and minimal off-current. Furthermore, we investigate the pull-in voltage characteristics depending on the length of the suspended graphene beam.

5.2. SGS structure and fabrication process flow

Figure 5.3 illustrates the fabrication steps of SGS. First, a 100 nm-thick SiO_2 was thermally grown on a highly doped n-type Si wafer. The chemical vapor deposited (CVD) few-layer graphene films grown on Ni catalyst were characterized by Raman spectroscopy [Figure 5.5(a)] and transferred onto the SiO_2 using thermal release tape.[15] Next, FLG beams were defined through photolithography, etched by oxygen plasma, and characterized by atomic force microscopy (AFM) to confirm the thickness of the actual FLG beam (< 2.5 nm) [Figure 5.4(b)]. After depositing Cr/Au for the top electrode formation [Figure 5.4-3], the FLG beam is suspended by selectively removing the exposed rectangular region of 100 nm-thick SiO_2 using diluted HF acid [Figure 5.4-4]. In order to prevent hydrofluoric (HF) acid from infiltrating into the interface of graphene and SiO_2 under the Cr/Au electrodes, the top electrodes were intentionally designed to be larger in size than the underlying graphene sheet. In addition, to avoid initial stiction from capillary forces, a critical point drier is used.[15]

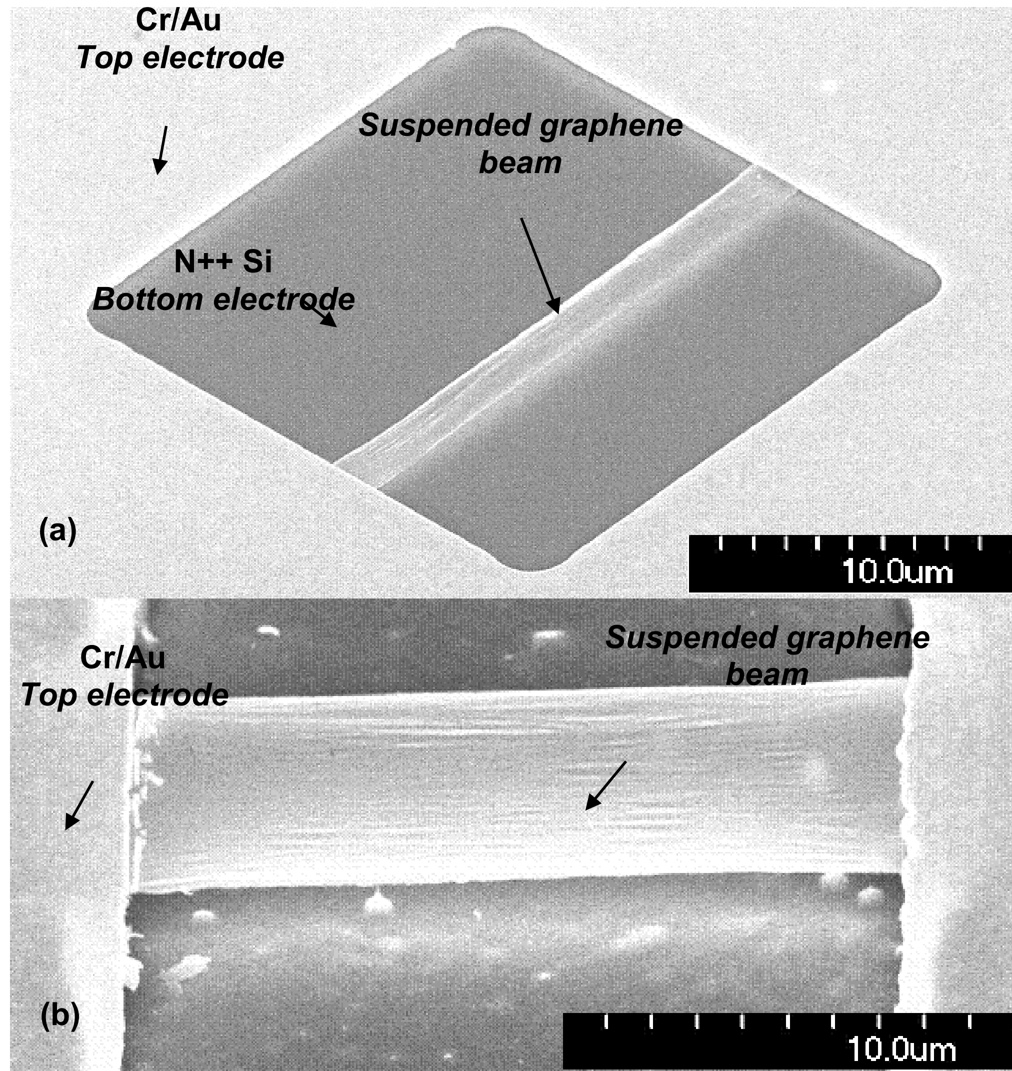


Figure 5.3 Scanning electron microscope (SEM) images of suspended graphene beam switches. (a) Bird's eye view of graphene beam length/width of 15μm/2μm and air gap of 0.15μm, (b) Tilted view of grapehen beam length/width of 15μm/5μm and gap of 2μm.

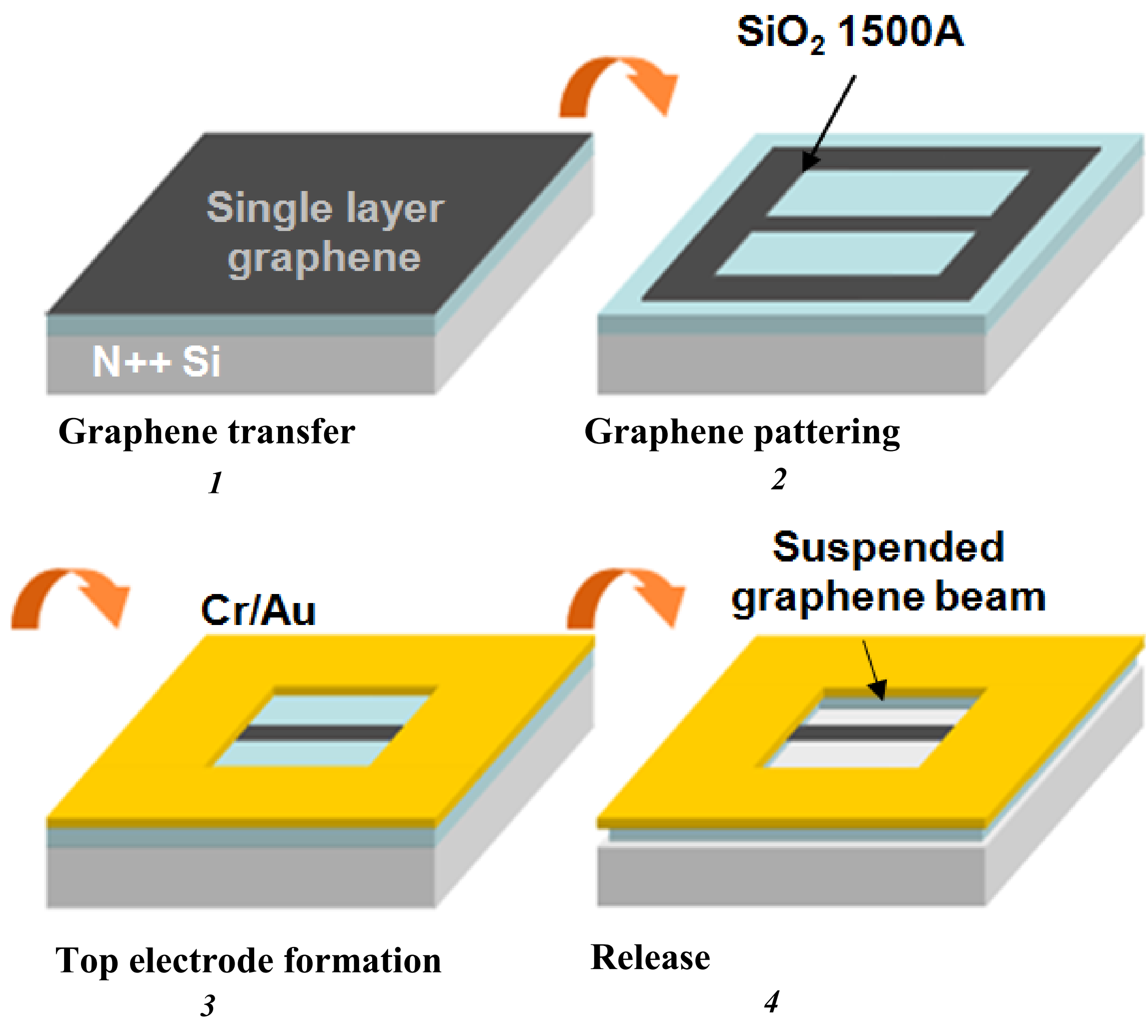
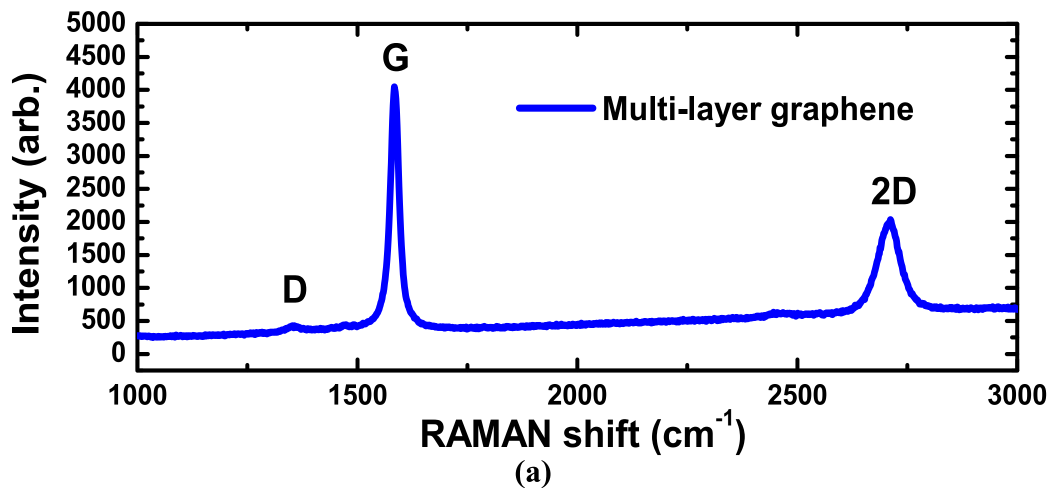
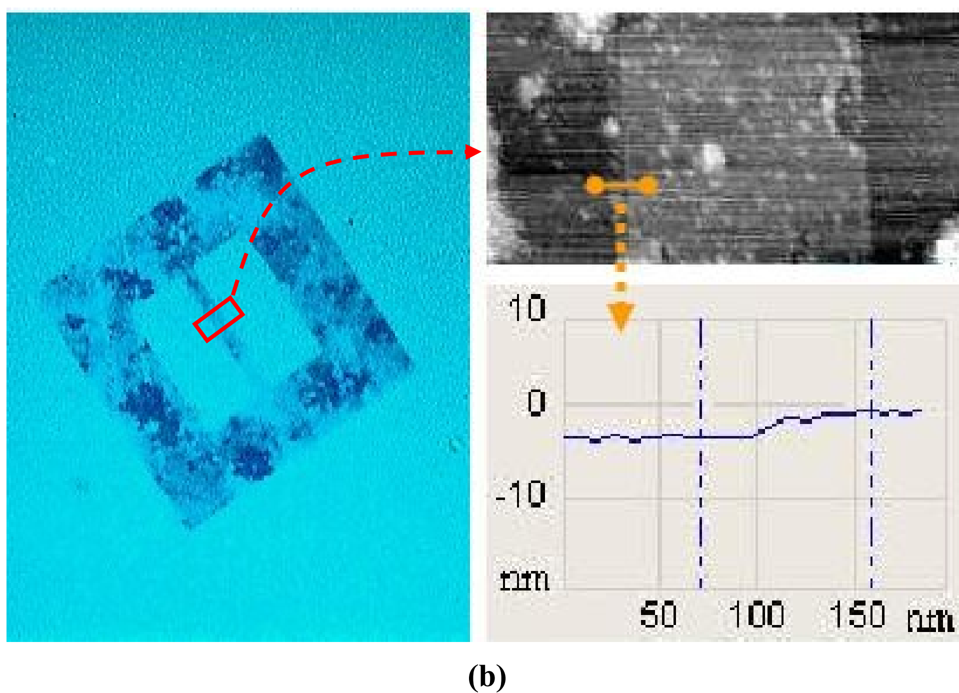


Figure 5.4 Schematic of fabrication process flow for SGS. *1:* A 6-inches wafer scale CVD grown multi layer graphene film is transferred onto a SiO_2 layer thermally grown on highly doped n-type Si substrate. *2:* Graphene beam is patterned using photolithography and O_2 plasma etching process. *3:* Au/Cr top electrode is formed by e-beam evaporation and following metal lift-off and *4:* graphene beam is released by selective removal of SiO_2 layer using diluted HF and the height is controlled by successive etching of Si substrate using diluted KOH solution. Then sample is dried by super critical point drying.



(a)



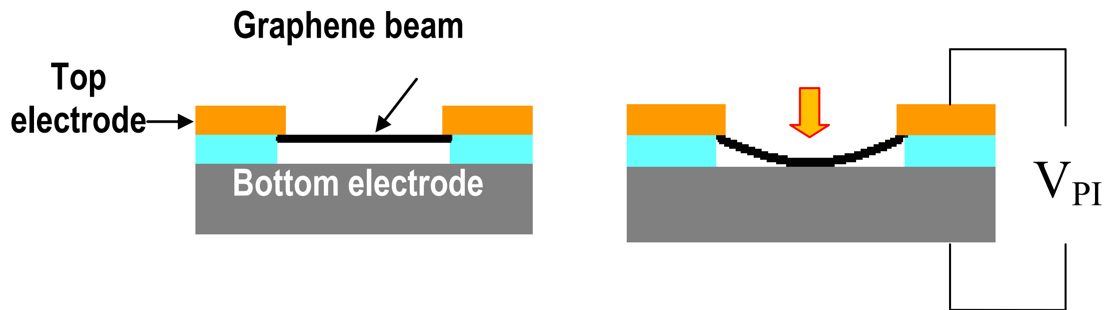
(b)

Figure 5.5 (a) RAMAN spectrum of transferred multi-layer graphene. (b) Optical microscope image of patterned graphene, transferred graphene is measured to be around 3nm in thickness.

The air-gap between the suspended FLG bridge and the underlying Si is modified by controlling the KOH etching time. Finally, a thin Al_2O_3 layer of 30 Å was coated onto the underlying Si substrate by atomic layer deposition (ALD) to prevent possible welding of FLG beam onto Si during switching operations. As shown in Figures. 5.3 (a) and (b), the scanning electron microscope (SEM) images of as-fabricated SGS structures display suspension of FLG beams over the Si substrate.

5.3. Switch characteristics of SGS

The electromechanical motions of the suspended FLG beam switches are investigated by measuring the current-voltage (I-V) characteristics. Upon applying a voltage between the FLG and Si substrate, the electrostatic force pulls the suspended FLG beam towards the bottom Si electrode. A pull-in operation is achieved once the FLG bridge makes a physical contact to the substrate, which is indicated through an abrupt increase of current.[16,17] The voltage where the abrupt transition occurs is the V_{PI} of an electromechanical switch, which is an important parameter relevant to the power consumption of MEMS devices. As shown in Figure 5.6 the SGS (length/width = l/w ~ 20μm/2μm, air-gap = h ~ 0.15 μm) shows an abrupt on/off current transition with a sub-threshold swing below 7 mV/dec at an average V_{PI} of 1.85 V. This value is similar to the operation voltage of conventional MOSFET devices and is well suited for integrating MEMS switches with CMOS. Here we note that the V_{PI} is not consistent on a run-to-run basis.



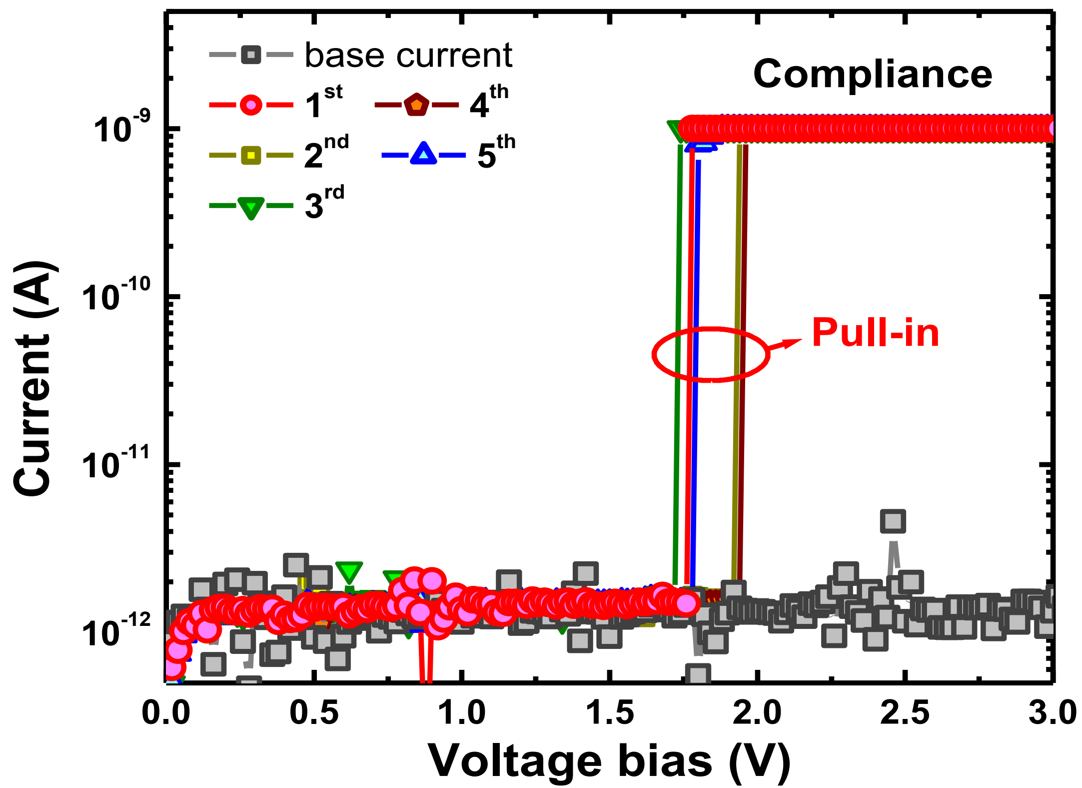


Figure 5.6 Current-Voltage characteristics between the top and bottom electrodes. The average pull-in voltage of SGS with 20 μm graphene beam and 0.15 μm gap was lower than 1.85 V.

We propose two possible reasons. One is that the physical contact point and/or the air-gap height are not guaranteed to be identical among successive switching operations. The other is that, when the switch is ON, the joule heating can cause ambient molecular species to adsorb/desorb onto graphene[24] and thus modify the mechanical and surface properties of the FLG beam.[18] [Figure 5.8]

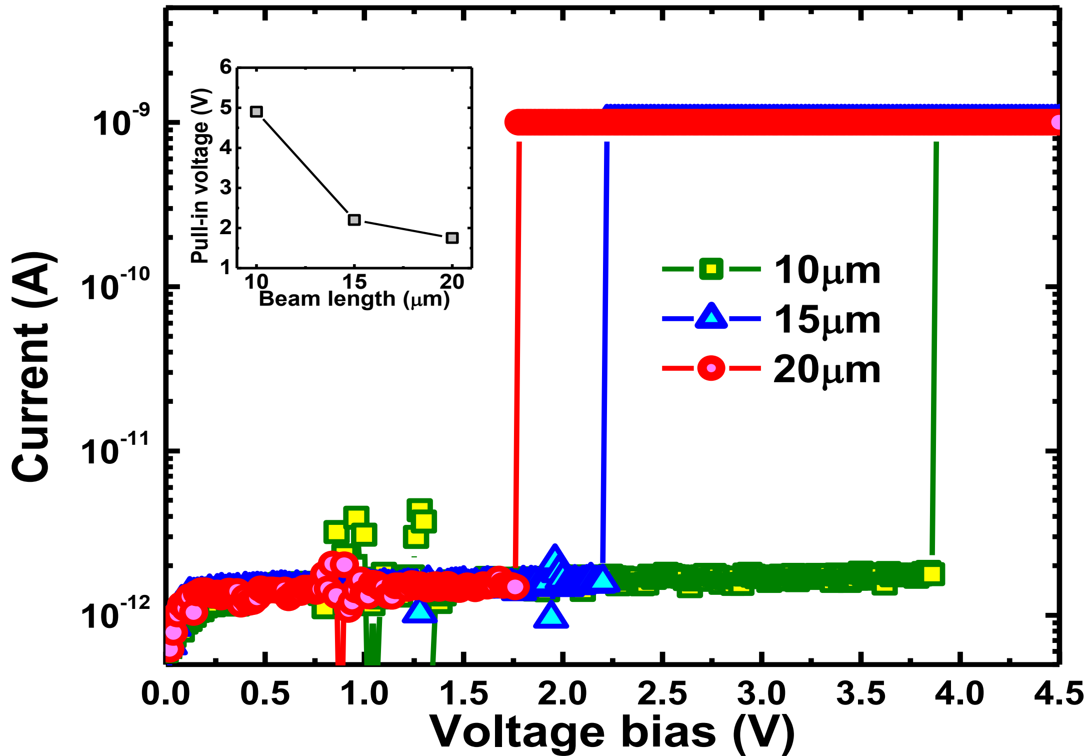


Figure 5.7 Pull-in voltage (V_{PI}) dependence on graphene beam length. V_{PI} decreases ($\sim 1/l^2$) as the beam length increases for a constant beam width (inset).

In order to minimize such undesirable effects, a cross-bar beam-gate SGS structure with encapsulation techniques, such as electrostatic bonding of Pyrex glass,[19] and deposition of silicon nitride[20] or polysilicon,[21] can be implemented to form a hermetically vacuum sealed capsule. Considering that the non-capsulated SGS degrades

after performing 4 – 6 successive switching operations, protection from moisture and contaminants is mandatory for reliable long-term usage.[2,6] Furthermore, we characterize the I-V characteristics of SGS for various beam lengths [Figure. 5.7]. As shown in the inset of Figure 5.6, the V_{PI} decreases ($\sim 1/l^2$) as the beam length increases for a constant beam width, which is consistent with the model proposed by Pamidighantam et al.,[22] and is attributed to the lowering of the bending stiffness.

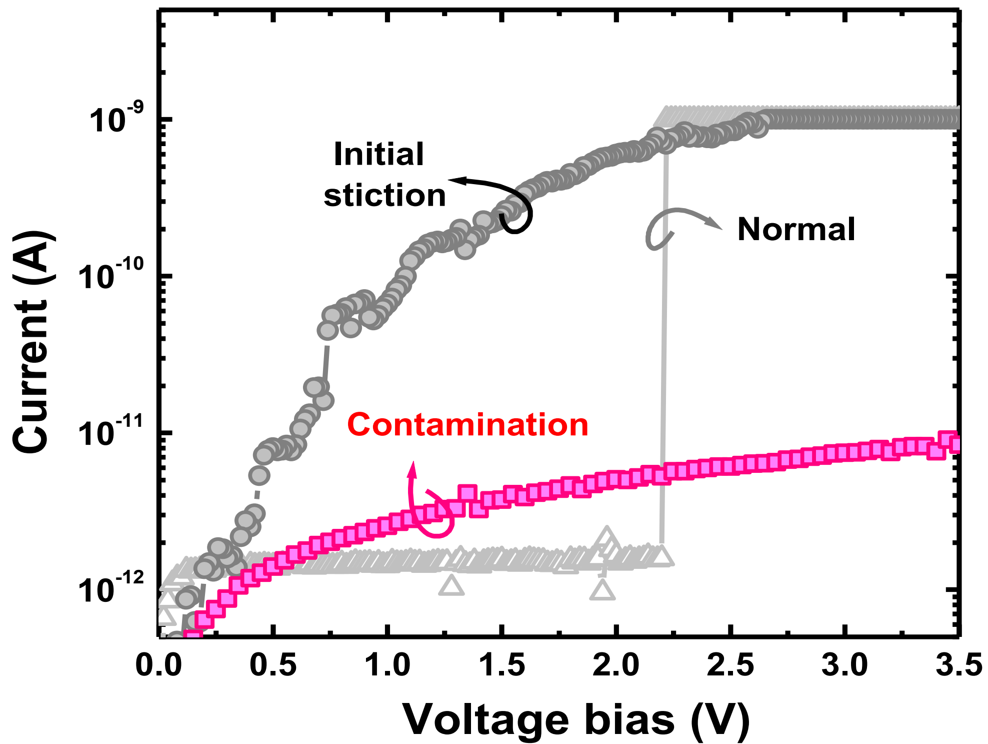


Figure 5.8 Degradation of switching characteristic resulting from initial stiction and contamination.

Another important parameter for a mechanical switch is the switching time. In general, conventional MEMS/NEMS has a switching time of a few microseconds.[23,24] In graphene-based MEMS/NEMS, however, the extremely low mass density and high

Young's modulus results in a very large resonant frequency (~ tens of MHz),[10,18] which shows possible operation in the nanosecond regime. Based on Muldavind and Rebeiz model,[25] the switching time is estimated to be $t_s = 3.67 (V_{PI}/V_{op}\omega_o) = 40$ ns ($V_{PI} = 1.85$ V, $V_{op} = 1.3V_{PI}$, and $\omega_o = 70$ MHz), where V_{op} is the operation voltage and ω_o is the resonant frequency. Graphene based nano-mechanical switch could be combined with FTM cell replacing MOSFET transistors. Figure 5.9 is a conceptual combination of FTM and suspended graphene beam mechanical switch. We expect this kind of combination can greatly reduce energy consumption that is important for wearable electronics.

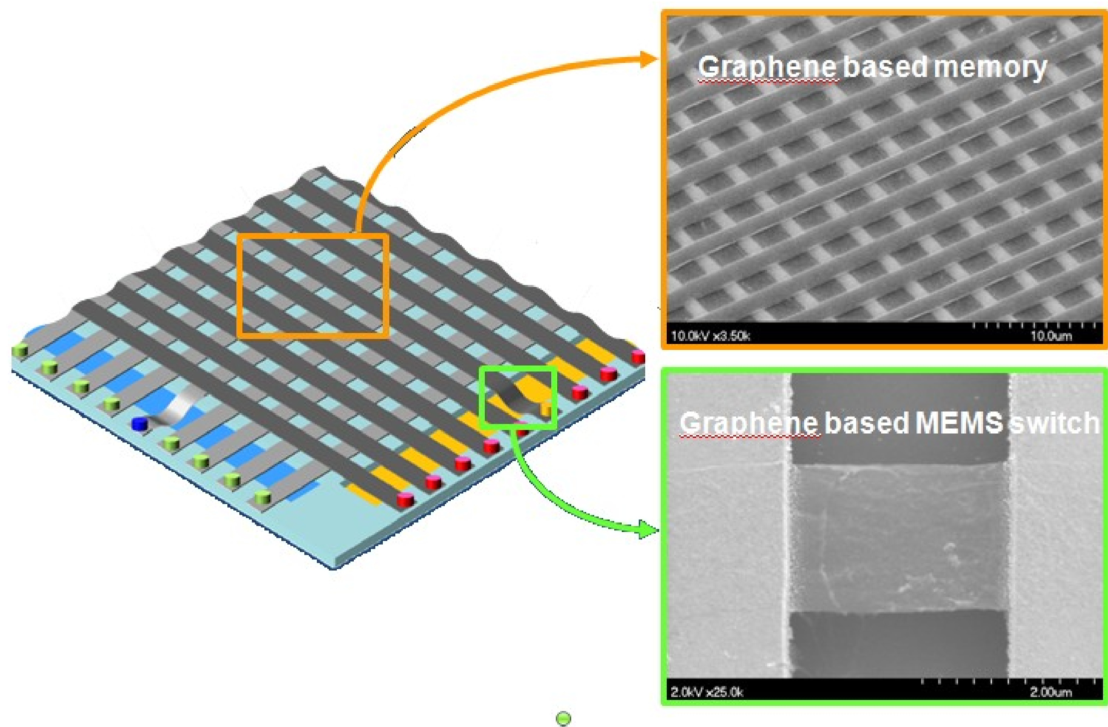


Figure 5.9 Conceptual combination of graphene based memory with MEMS switch.

5.4. Summary

Suspended few-layer graphene beam electro-mechanical switches (SGS) with 0.15 μm air-gap are fabricated and electrically characterized. The SGS shows an abrupt on/off current characteristics with minimal off current. In conjunction with the narrow air-gap, the outstanding mechanical properties of graphene enable the mechanical switch to operate at a very low pull-in voltage (V_{PI}) of 1.85 V, which is compatible with conventional CMOS circuit requirements. In addition, we show that the pull-in voltage exhibits an inverse dependence on the beam length. We believe that this study will benefit future applications of graphene for MEMS/NEMS devices.

5.6. References

1. A. H. Castro Neto, F. Guinea, N. M. R. Peres, K. S. Novoselov, and A. K. Geim, “The electronic properties of grapheme,” Rev. Mod. Phys. 81, pp.109-113, (2009).
2. C. Lee, X. Wei, J. W. Kysar, and J. Hone, “Measurement of the Elastic Properties and Intrinsic Strength of Monolayer Graphene,” Science 321, 385 (2008)
3. W. W. Jang, J. O. Lee, J. B. Yoon, M. S. Kim, J. M. Lee, S. M. Kim, K. H. Cho, D. W. Kim, D. Park, and W. S. Lee, “Fabrication and characterization of a nanoelectromechanical switch with 15-nm-thick suspension air gap”, Appl. Phys. Lett. 92, pp.103110-103113 (2008).
4. N. Abelé, R. Fritschi, K. Boucart, F. Casset, P. Ancey, and A. M. Ionescu, “Suspended-gate MOSFET: Bringing new MEMS functionality into solid-state MOS transistor,” Tech. Dig. - Int. Electron Devices Meet., pp.1075-1078, (2005)

5. H. Kam, D. T. Lee, R. T. Howe, and T.-J. King, “A new nanoelectromechanical field effect transistor (NEMFET) design for low-power electronics,” Tech. Dig. - Int. Electron Devices Meet., pp.477-480, (2005)
6. International Technology Roadmap for Semiconductors (ITRS), Design, Semiconductor Industry Association (SIA, San Jose, 2007).
7. R. Badzey, G. Zolfagharkhani, A. Gaidarzhy, and P. Mohanty, "A controllable nanomechanical memory element," Appl. Phys. Lett. 85, pp.3587-3590, (2004).
8. N. Abele, A. Villaret, A. Gangadharaiah, C. Gabioud, P. Ancey and A. M. Ionescu, “1T MEMS memory based on suspended gate MOSFET,” Tech. Dig. - Int. Electron Devices Meet. , pp.509-512, (2005)
9. W. W. Jang, J. O. Lee, and J. B. Yoon, "A DRAM-like mechanical non-volatile memory," Proc. 14th Int. Conf. Solid-State Sens. & Actuators 2, pp.2187-2191, (2007).
10. J. S. Bunch, A. M. van der Zande, S. S. Verbridge, I. W. Frank, D. M. Tanenbaum, J. M. Parpia, H. G. Craighead, and P. L. McEuen, “Electromechanical Resonators from Graphene Sheets,” Science 315, pp.490-493, (2007).
11. M. Dequesnes, S. V. Rotkin and N. R. Aluru., "Calculation of pull-in voltages for carbon-nanotube-based nanoelectromechanical switches," Nanotechnology 13, pp.120-124, (2002).
12. L. M. Jonsson, S. Axelsson, T. Nord, S. Viefers, and J. M. Kinaret. "High frequency properties of a CNT-based nanorelay," Nanotechnology 15, pp.1497-1502, (2004).
13. A. B. Kaul, E. W. Wong, L. Epp, and B. D. Hunt., "Electromechanical carbon nanotube switches for high-frequency applications," Nano Lett. 6, pp. 942-947, (2006).
14. K. S. Kim, Y. Zhao, H. Jang, S. Y. Lee, J. M. Kim, K. S. Kim, J.-H. Ahn, P. Kim, J.-Y. Choi, and B. H. Hong, "Large-scale pattern growth of graphene films for stretchable transparent electrodes," Nature 457, pp.706-710, (2009).

15. C. Gomez-Navarro, M. Burghard, and K. Kern, "Elastic properties of chemically derived single graphene sheets," Nano Lett. 8, 2045-2050, (2008).
16. G. M. Rebeiz, RF MEMS: theory, design, and technology (Hoboken, Wiley, 2003).
17. K. M. Milaninia, M. A. Baldo, A. Reina, and J. Kong, "All graphene electromechanical switch fabricated by chemical vapor deposition," Appl Phys Lett. 95, pp.183105-13108, (2009).
18. C. Chen, S. Rosenblatt, K. I. Bolotin, W. Kalb, P. Kim, I. Kymissis, H. L. Stormer, T. F. Heinz and J. Hone, "Performance of monolayer graphene nanomechanical resonators with electrical readout," Nat. Nanotech. 4, pp.861-867 (2008).
19. K. Najafi, "Micropackaging technologies for integrated Microsystems: Applications to MEMS and MOEMS" Proc. SPIE, pp.4979-4982, (2003).
20. K. D. Leedy, R. E. Strawser, R. Cortez and J. L. Ebel., "Thin-film encapsulated RF MEMS switches," J. Microelectromech. Syst. 16, 304 , (2007).
21. R. N. Candler, M. A. Hopcroft, B. Kim, W. T. Park, R. Melamud, M. Agarwal, G. Yama, A. Partridge, M. Lutz, and T. W. Kenny, "Long-Term and Accelerated Life Testing of a Novel Single-Wafer Vacuum Encapsulation of MEMS Resonators," J. Microelectromech. Syst. 15, 1446, (2006).
22. S. Pamidighantam, R. Puers, K. Baert, and H. A. C. Tilmans, "Pull-in voltage analysis of electrostatically actuated beam structures with fixed–fixed and fixed–free end conditions," J. Micromech. Microeng. 12, 458 (2002).
23. T. Yamamoto, T. Sogo, S. Obata, T. Miyagi, and S. Hiura., "Millimeter-Wave MEMS capacitive switch in vacuum-sealed in-line wafer level package," Tech. Dig. - Microwave Conf., 198, (2009)
24. B. Bae, J. Han, R. I. Masel, and M. A. Shannon, "A bi-directional electrostatic microvalve with microsecond switching performance," J. Microelectromech. Syst. 16, 146 (2007).
25. B. Muldavin and G. M. Rebeiz, Symp. "Nonlinear electro-mechanical modeling of MEMS switches," Dig. - Int. Microwave., 2119, (2001)

Chapter 6

Conclusion and Future works

Developing a memory module for a fully flexible and transparent electronic device has motivated this research. Several types of graphene FET based memory devices have been demonstrated in this thesis.

First, a non-volatile memory (NVM) exploiting single-layer graphene (SLG) and multi-layer graphene (MLG) as channel materials were fabricated on Si substrate and the electrical performance were characterized. The injection of electrons into the trap sites of a HfO_2 high-k dielectric data storage results in excellent memory characteristics, such as a wide memory window of 11.0V with high program and erase speeds. The impact of the gate material's work-function (Φ_M) on the memory characteristics was investigated using different types of metals [Ti ($\Phi_{Ti} = 4.3$ eV) and Ni ($\Phi_{Ni} = 5.2$ eV)]. The optimum memory characteristics with stable program/erase conditions were achieved by the combination of SLG channel with high Φ Ni metal gate electrode. The increase in memory window is attributed to the change in the flat-band condition and the suppression of electron back-injection within the gate stack. The NVGMs fabricated by processes compatible with flat panel display (FPD) can be utilized for high-density 3D multi-stack memory cells.

Second, a flexible and transparent graphene charge trap memory (FTM) composed of a single-layer graphene channel and a ITO gate electrode was fabricated on a poly-

ethylene naphtalate substrate below glass transition temperatures (~110°C). The FTM exhibits memory functionality of ~8.6 V memory window and 30% data retention per 10 years, while maintaining ~80% of transparency in the visible wavelength. Under both tensile and compressive stress, the FTM shows minimal effect on the program/erase states and the on-state current. The Low temperature process of FTM can be essential to integrate flexible logic, display, solar cell and memory on an identical substrate and eventually unify the fabrication processes of each module into the same production line. The FTM may be instrumental for fully flexible and completely see-through electronics.

Third, we demonstrate Embedded Oxide Trap Memory (EOTM), another type of FTM. It uses trap-rich Al_2O_3 as a data storage layer, which is formed by using an oxygen ion bombardment (OIB) process. The triple high-k dielectric stack Al_2O_3-AlO_x-Al_2O_3 (AAA) allows the FTM to have stable memory characteristics that effectively suppresses electron back injection from the transparent gate electrodes including graphene, which generally has low Φ_M.

At the last, suspended few-layer graphene beam electro-mechanical switches (SGSs) feasibly integrated with graphene transistor based memory or CMOS circuits were presented. SGS with 0.15µm air-gap were fabricated using compatible processes with FTM and were electrically characterized. The SGS shows an abrupt on/off current characteristic with minimal off current. In conjunction with the narrow air-gap, the outstanding mechanical properties of graphene enabled the mechanical switch to operate at a very low pull-in voltage (V_{PI}) of 1.85 V, which is compatible with conventional

complimentary metal-oxide-semiconductor (CMOS) circuit requirements. In addition, we showed that the pull-in voltage exhibits an inverse dependence on the beam length.

Through this thesis, I also proposed an all graphene electronic devices consist of FTM and SGS fabricated using compatible processes with each other. I believe that the experimental results demonstrated through this research would be the cornerstone of a fully flexible and transparent device with integration technology.

From the study that has been done so far, we already looked at some of the limitations. Here are some of the key innovations in process, material and device structure which can bring the implementation of FTM and SGS closer to reality:

Process: A large scale graphene growth and transfer technology has been used for preparing the substrate. But this process has not been matured enough for mass production, so the inhomogeneity of transferred graphene film results in very low yield (10%) of test devices. Thus, the innovation in graphene growth and patterning process is required. Improved graphene growth and transfer technology would further enhance the FTM performance and SGS durability.

Material: Finding novel tunneling barrier dielectric materials with excellent properties would greatly improve the data retention characteristics of FTM. Tailoring materials and the electrical band structure of gate stack is also crucial to suit the data retention requirements of a commercial flash memory product.

Device: Even though solutions for the low on/off ratio have been proposed and demonstrated through graphene quantum dots, bi-layer graphene, hydrogenated graphene, graphene nano-ribbons etc., the low on/off current ratio of grapheme channel transistor is still the biggest challenge. So it is mandatory to find an effective way to open a band gap in graphene and develop a high yield devices structure.