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An Interleaved 6-Level GaN Bidirectional Converter With an Active Energy Buffer for Level II Electric Vehicle Charging

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***Abstract*—On-board electric vehicle (EV) chargers provide ac to dc conversion capability to charge a high-voltage battery pack. As they are carried within a vehicle at all times, high efficiency and high power density are desirable traits for such a converter, in order to reduce the size, weight, and power loss of the system. Bidirectional capability is also desirable for an on-board charger to support vehicle-to-grid ancillary applications. This paper presents the implementation of a bidirectional single-phase ac-dc converter, converting between universal ac (120-240 V_{AC}) and 400 V_{DC}. Discussions of system architecture, control, mechanical design and assembly, and thermal management of an interleaved 6-level flying capacitor multilevel (FCML) power factor correction (PFC) stage with a twice-line-frequency series-stacked buffer (SSB) stage are included. Experimental results demonstrating dc-ac inverter operations at the kilowatt scale are provided. A peak efficiency exceeding 99% is observed, and a maximum power of 6.1 kW is tested.**

I. Introduction

Level II on-board electric vehicle (EV) chargers interface with the ac grid to charge a high-voltage battery. This provides the capability to take advantage of widespread infrastructure providing single-phase ac grid voltages (120-240 V_{AC}) with power capabilities at kilowatt levels [1]. Since the charger is carried within the vehicle at all times, designs that are compact, highly efficient, and lightweight are highly desirable due to space and range constraints in EVs. In this work, we seek to improve the overall gravimetric and volumetric power density of the single-phase ac-dc stage of a level II EV charger, considering converter topology, mechanical design and assembly, and thermal management simultaneously.

In a conventional design, an ac-dc stage is usually implemented with a boost converter connected to a large electrolytic capacitor bank. The current through the boost inductor is controlled to regulate the ac current with a high power factor and low distortion. The capacitor bank buffers the twice-line frequency power pulsation characteristic of single-phase ac-dc and dc-ac applications. The boost inductor and the electrolytic capacitor bank are some of the largest contributors to volume and weight in such designs. In some designs, the same hardware can be run in reverse to become a dc-ac stage.

A system architecture featuring the flying-capacitor multilevel (FCML) converter as the rectified sine waveform generation or power factor correction (PFC) stage, and a series-stacked buffer (SSB) [2] as the energy buffer stage, is used to improve gravimetric and volumetric power density as compared to conventional designs. It has been shown that the flying capacitor multilevel (FCML) topology [3], [4] has the potential to dramatically reduce passive component volume and weight in inverter [5]–[7] and PFC applications [8], [9]. For mechanical packaging, the overall assembly maximizes the utilization of the 3D space with a low-profile and modular design philosophy. The heat-generating components are placed on a single side to allow for simple thermal circuit routing and higher thermal efficiency for automotive cooling systems.

In this paper, system architecture, hardware and control, packaging and thermal design are discussed. Test results demonstrating dc-ac inverter operation from 400 V_{DC} to 240 V_{AC} at kilowatt levels are provided, building on the PFC and inverter demonstration of the bidirectional architecture and control described in [10]. The remainder of the paper is organized as follows: Sections II and III describe system architecture and design. Section IV describes the physical hardware prototype, Section V details experimental results, and Section VI provides concluding remarks.

II. System Architecture

The overall system electrical schematic is shown in Fig. 1. From the ac side to the dc side, it is comprised of an active rectifier/unfolder, an interleaved FCML PFC/inverter stage, and then a series-stacked buffer across the dc bus. The overall control diagram for the inverter and SSB operation is shown in Fig. 2.

A. FCML Stage

The PFC/inverter stage is comprised of two interleaved FCML boost converters, and controls the input ac current to be in phase with the input voltage. When the system is run as an inverter, the FCML stage generates a rectified sine wave to be filtered by the inductors and then run through the unfolder to form a full sine wave. Since the FCML topology has a frequency multiplication effect, the inductor size may be reduced by $(N-1)^2$ times as compared to conventional two-level converters, where N is the number of levels [3]. For PFC operation, this smaller inductor size increases the

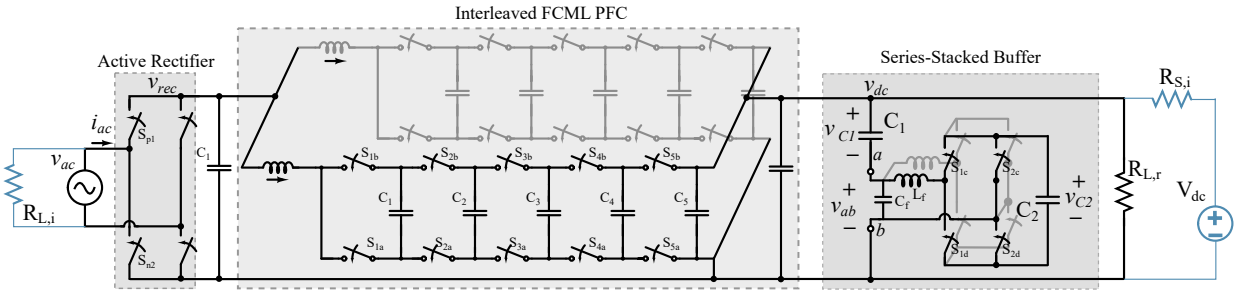

Fig. 1: Schematic of the overall system with active rectifier (unfolder), interleaved FCML PFC, and series-stacked buffer.

complexity and difficulty of control, due to increased control bandwidth requirements. For PFC control, this can be solved with a feedforward term as discussed in [8], [11], [12]. In this work, the inverter mode control in Fig. 2 is implemented for the final high power test.

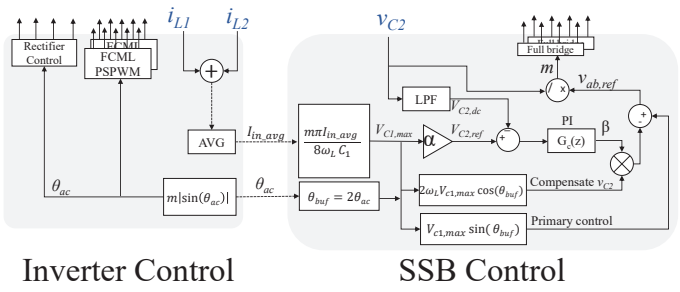

Fig. 2: Overall control system in inverter mode.

B. Series-Stacked Buffer

The schematic of the SSB is shown in Fig. 1. Capacitor C_1 is the main energy-buffering capacitor, and is connected in series with a full H-bridge converter. The voltage ripple on V_{C1} is actively canceled with a waveform generated at v_{ab} by the full-bridge converter. Because the dc bus can be controlled to a very low ripple with this method, the voltage ripple on V_{C1} can be increased, which decreases the required size of C_1 by a factor of the voltage ripple. Furthermore, since the full dc bus voltage is only displaced across C_1, the full-bridge converter sees a reduced operating voltage, and only processes a fraction of the total system power, which improves system efficiency. The voltage V_{C2}, required to generate the canceling waveform v_{ab}, is regulated with a feedback loop that causes the SSB to draw real power into the full-bridge converter. This introduces some voltage ripple on the dc bus, but keeps the voltage on C_2 from decaying from the losses in the full-bridge converter. A detailed description of the operation and component sizing of the SSB architecture can be found in [9], [13].

A control scheme that combines the SSB controller with PFC/inverter control is implemented to synchronize power and phase relationships between the two stages. In PFC mode, the voltage-loop factor k that scales the input current and the angle of the ac voltage are passed to the SSB controller to determine the magnitude and phase of the reference voltage for v_{ab}. In the inverter mode in Fig. 2, the magnitude of v_{ab} can be determined from the average inductor current. If the ac voltage is $V_{ac}\sin(\omega_L t)$, the ideal voltage v_{ab} is

$$v_{ab} = \frac{P_0}{2\omega_L V_{dc} C_1}\sin(2\omega_L t), \tag{1}$$

where P_0 is the load power, ω_L is the line angular frequency, V_{dc} is the average dc-bus voltage [9]. Detailed implementation of both control software and sensing hardware for both PFC and inverter modes can be found in [10].

III. Thermal Design

To manage the heat generated by components in the electrical system, a liquid cooling solution is proposed, to take advantage of possible existing liquid cooling loops in vehicles. The heat is dissipated by a 50/50 in volume mixture of water and ethylene glycol (WEG) flowing in an aluminum single-inlet/single-outlet cold plate that we designed. The main heat-generating components are the GaN devices, estimated at upwards of 5 W each and the inductors upwards of 7.5 W each. The design of the cold plate was guided by thermo-fluidic CFD simulations performed in ANSYS IcePAK. The simulations, coupled with analytical models, enabled rapid iteration and convergence to a design that has an equitable tradeoff between pressure drop and sufficient cooling for the power electronic components. The 0.125 inch diameter channel is directed such that the majority of the fluid is routed toward the most power dense components (Figure 3). Additional paths were added to reduce the temperature gradient across the cold plate. The cold plate shape was designed such that it matches the different heights once attached to the EV charger, to ensure good thermal contact and minimize thermal resistances.

The ANSYS IcePAK domain that we used to model the cold plate contains ∼10 million cells. We chose this number after performing a mesh independence study that showed that finer meshes lead to almost the same results. We run the steady-state simulations with a turbulent solver until all residuals fall below 10^{-6}. The fluid input temperature was set to 70 °C as the maximum specified temperature of an automotive cooling loop. With a flow rate of 1.1 LPM, the maximum electronics temperature rise from inlet temperature was ∼20 °C and the inlet-to-outlet pressure drop was 12.5 mbar. Figure 5 shows how the maximum electronics temperature and the inlet-to-outlet pressure drop vary with the liquid flow rate based on the ANSYS IcePAK simulations. When increasing the flow rate from 1.1 to 5 LPM, a 4.5 °C

reduction in the maximum temperature leads to a 24× increase in pressure drop.

We manufactured the designed cold plate using 6063 aluminum alloy, owing to its high thermal conductivity and light weight. The fabricated cold plate has a weight of 300 ± 0.5 g and a volume of 0.17 ± 0.01 L. We manufactured it (Fig. 4) according to the following steps:

- Rough milling to remove large material portions and create the height differences and the cylindrical inlet/outlet.
- Finishing pass to remove last few millimeters and minimize roughness.
- Drilling to create the inlet/outlet and the interior channels.
- Plugging the holes with press-fitted epoxy to close the holes on the edges and leave only the inlet/outlet open.

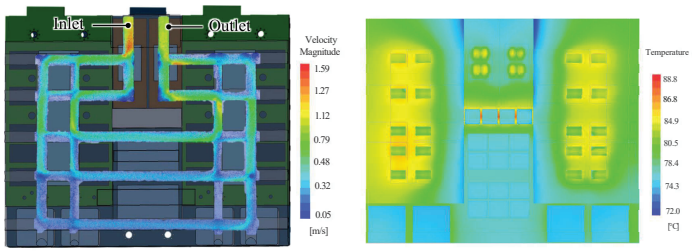

Fig. 3: The velocity magnitude contour plots and temperature estimates of the ANSYS IcePAK simulation of a 1.1 LPM flow inside the designed cold plate superimposed over the EV charger.

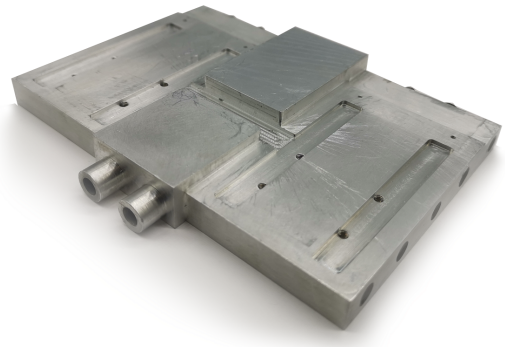

Fig. 4: The manufactured cold plate.

IV. Hardware Implementation

This prototype was designed to balance electrical, mechanical, and thermal design aspects. The electrical design takes advantage of the modularity of the FCML structure, and was done with consideration to the mechanical and thermal layouts. The mechanical design takes advantage of 3D space to pack components at a high density, and is also modular. Finally, the thermal management drove both the electrical and the mechanical aspects towards a single-sided cooled design so as to simplify thermal circuit routing.

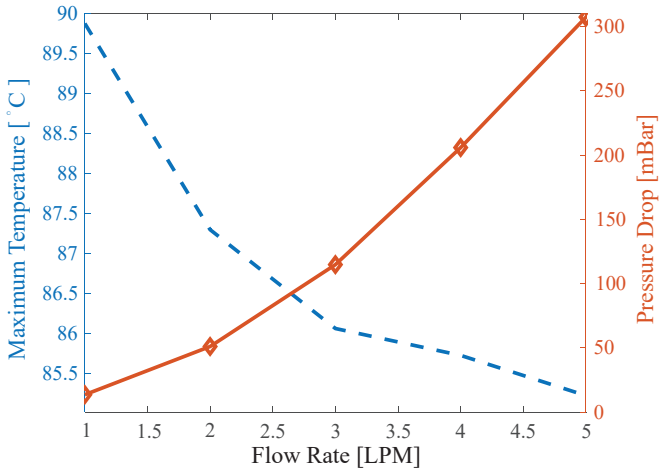

Fig. 5: ANSYS IcePAK simulation results of the maximum electronics temperature and the inlet-to-outlet pressure drop vs. the flow rate inside the designed cold plate.

TABLE I: Data Acquisition and Thermal Management Equipment

Equipment	Description	Part Number
Chiller	Thermo Scientific Polar Series Accel 500	223422800
Flow meter	Kobold MIM Series Electromagnetic Flow Meter	MIM-1215HG5C3T0
RTDs	REOTEMP RTDs	AT-PX1123YLR4S1T2T
Data Acquisition Chasis	NI cDAQ-9189 CompactDAQ Chassis	785065-01
Analog Data Module	NI 9201	779013-01
RTD Data Module	NI 9216	785186-01

A hardware prototype has been constructed with the proposed architecture and control, as shown in Fig. 6. A modular FCML converter design was done to streamline manufacturing and debugging (Fig. 7). The hardware prototype consists of two interleaved FCML converters, a series-stacked buffer twice-line frequency buffer stage, an H-bridge rectifier/unfolder, and energy buffering capacitors. To control the converter, a TI C2000 microcontroller was selected, which connects through a signal backplane board. Power is transferred through bolt-type connections between major power boards. An exploded-view detail render of the electrical portion of the prototype is shown in Fig. 8. For the thermal management system, the custom cold plate design (Fig. 4) discussed in Section III is used. The bench setup with liquid cooling loop and temperature monitoring is shown in Fig. 9. The equipment used to collect data and diagnostics in the liquid cooling loop is displayed in Table I.

In the FCML stage, which sees a maximum dc voltage of 400 V_{DC}, each switch is required to block 80 V ($V_{dc}/5$). Therefore, 100 V rated GaN devices from GaN Systems were selected as the main power devices. For the H-bridge unfolder stage, 650 V rated GaN Systems devices were chosen to handle the 240 V_{AC} line voltage. For the series-stacked buffer, the switches must withstand 110 V, so 150 V GaN devices from EPC Co. are used. Key components used in the charger system and their characteristics are described in Table II.

V. Experimental Results

To validate the control architecture and high density implementation, the converter has been operated in the inverter

TABLE II: Component listing

Subsystem	Component	Part No.	Parameters
Interleaved 6-Level FCML (per leg)	GaN FETs Isolated Gate Drivers Flying Capacitors Inductors	GaN Systems GS61008T Si8271GB-IS TDK C5750X6S225K250KA Vishay IHLP6767GZER100M11	100 V, 7 $m\Omega$ Silicon Labs Si827x Series 2.2 μF $\times$ 2–5 (parallel, $\sim$ 2.6μF effective) 10 μH
Active Rectifier / Unfolder	GaN FETs Isolated Gate Drivers	GaN Systems GS66516T Si8274GB1-IS1	650 V, 25 $m\Omega\times$ 3 (parallel) Silicon Labs Si827x Series
Interleaved Series-Stacked Buffer (per leg)	GaN FETs Isolated Gate Drivers Inductors	EPC 2033 Si8274GB1-IM1 Coilcraft XAL7070-472	150 V, 7 $m\Omega$ Silicon Labs Si827x Series 4.7 μH $\times$ 2 (series)
Buffer Capacitors	C_1 C_2	TDK C5750X6S225K250KA TDK C5750X7S2A156M250KB	820 (parallel) 200 (parallel)
Control	Microcontroller	TI F28379D controlCARD	C2000 Series Microcontroller

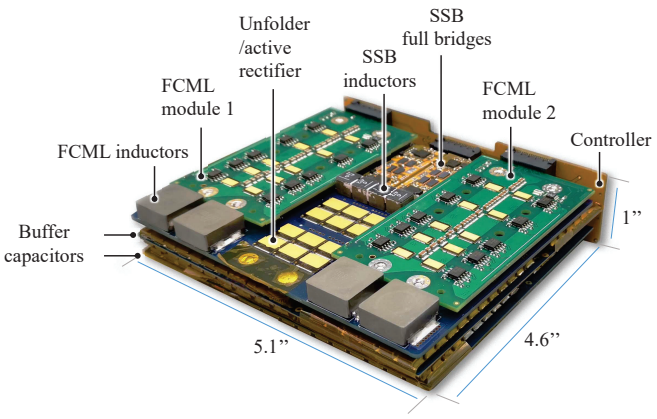

Fig. 6: The EV charger assembly, not including thermal management. Key subsystems are labeled.

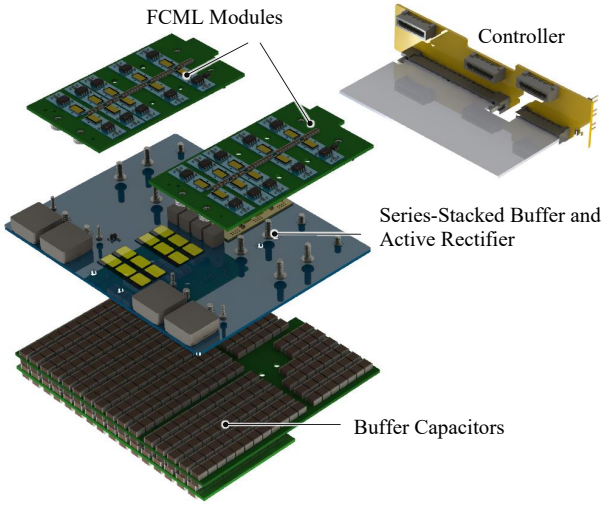

Fig. 8: Exploded view render of the hardware assembly.

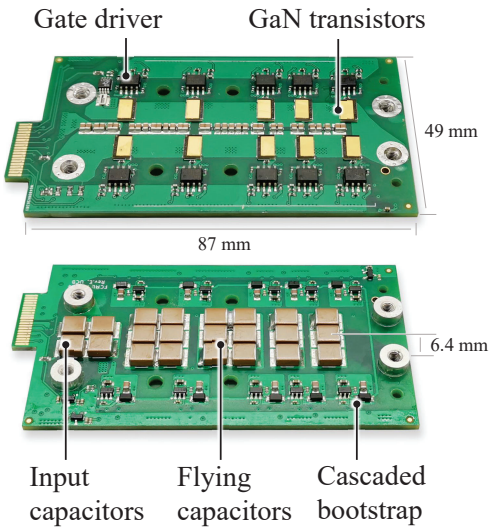

Fig. 7: Single FCML module with key components annotated.

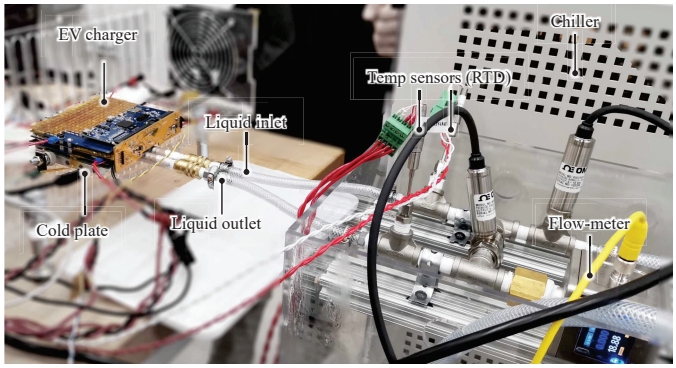

Fig. 9: Experimental bench setup.

mode at high power. A 400 V_{DC} input was used to produce a 240 V_{AC} output. The system was tested while connected to the cold plate system set at 25 °C.

Figure 10 shows a plot of efficiency for the inverter stage up to 6.1 kW input. We note that the peak efficiency values are well above 98.5% for most of the range, with a peak above 99%. To capture such high conversion efficiencies, a high precision power analyzer (Keysight PA2201) was used.

Table III lists converter performance specifications, including important efficiency and power density metrics. The system achieves a volumetric power density of 260 W/in^3 without the cold plate and a power density of 201 W/in^3 with the cold plate. Oscilloscope traces of typical converter waveforms are shown in Fig. 11. The switch nodes of the FCMLs (v_{sw1} and v_{sw2}) are filtered to generate the ac voltage. The SSB twice-line frequency buffering waveform (v_{ab}) works to cancel the 120-Hz ripple on the dc bus. The v_{C2} waveform demonstrates the SSB feedback control which draws sufficient real power into the circuit branch to keep the voltage on C_2 from decaying.

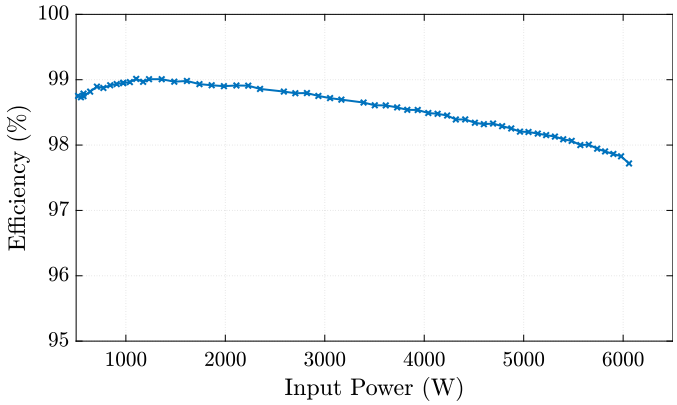

Fig. 10: The efficiency of the 6.1 kW inverter test, 400 V_{DC} to 240 V_{AC}

TABLE III: Key Performance Specifications

Parameter	Value	Notes
DC Voltage	400 V_{DC}	Tested
AC Voltage	240 V_{AC}	Tested
AC Current	25 A	Tested
AC Power	6.1 kW	Tested
Efficiency	99.01%	Peak Eff. (At 1.1 kW)
	97.7%	At 6.1 kW
Switching Frequency	150 kHz	Per switch
Effective Frequency	750 kHz	At inductor
Rect. Box Dimensions	5.1" × 4.6" × 1.0" (12.95 cm × 11.68 cm × 2.54 cm)	Excl. cold plate
Cold plate Dimensions	5.1" × 3.6" × 0.375" (12.95 cm × 9.14 cm × 0.95 cm)	
Volumetric Power Density	260 W/in^3 (15.9 W/cm^3)	Excl. cold plate
Volumetric Power Density	201 W/in^3 (12.3 W/cm^3)	Incl. cold plate

VI. Conclusions

This paper presents a Level II single-phase EV charger system featuring an interleaved flying-capacitor multilevel converter (FCML) stage and the series-stacked buffer topology. The charger converts between universal ac (120-240 V_{AC}) and 400 V_{DC} The design process of the overall system architecture, digital control, mechanical assembly, and thermal management is detailed. A hardware prototype has been constructed demonstrating dc-ac inverter operation from 400 V_{DC} to 240 V_{AC}, building on the pfc and inverter demonstration of the architecture and control described in [10]. A peak efficiency over 99% is observed, and a maximum power of 6.1 kW is tested.

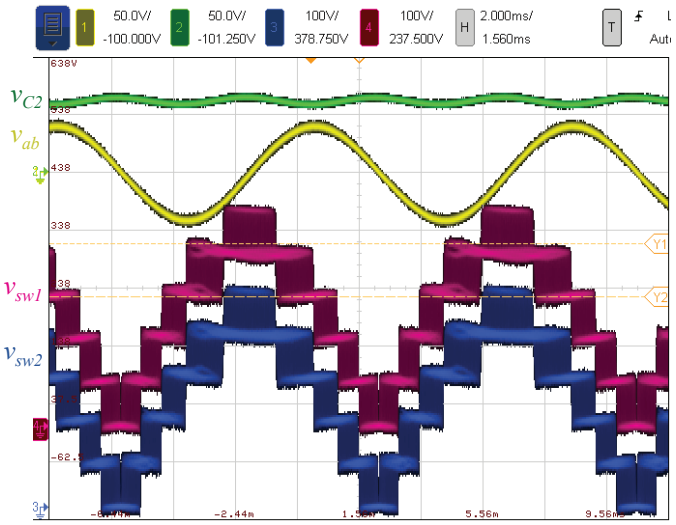

Fig. 11: Typical SSB voltage waveforms for v_{c2} and v_{ab}, and FCML switching node voltages from 400 V_{DC} to 240 V_{AC}, 6.1 kW.

VII. Acknowledgement

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