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Authors

Chen, Aiping
Zhang, Wenrui
Dedon, Liv R
et al.

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Couplings of Polarization with Interfacial Deep Trap and Schottky Interface Controlled Ferroelectric Memristive Switching

Aiping Chen, Wenrui Zhang, Liv R. Dedon, Di Chen, Fauzia Khatkhatay, Judith L. MacManus-Driscoll, Haiyan Wang, Dmitry Yarotski, Jun Chen, Xingsun Gao, Lane W. Martin, Andreas Roelofs, and Quanxi Jia*

Memristors with excellent scalability have the potential to revolutionize not only the field of information storage but also neuromorphic computing. Conventional metal oxides are widely used as resistive switching materials in memristors. Interface-type memristors based on ferroelectric materials are emerging as alternatives in the development of high-performance memory devices. A clear understanding of the switching mechanisms in this type of memristors, however, is still in its early stages. By comparing the bipolar switching in different systems, it is found that the switchable diode effect in ferroelectric memristors is controlled by polarization modulated Schottky barrier height and polarization coupled interfacial deep states trapping/detrapping. Using semiconductor theories with consideration of polarization effects, a phenomenological theory is developed to explain the current–voltage behavior at the metal/ferroelectric interface. These findings reveal the critical role of the interaction among polarization charges, interfacial defects, and Schottky interface in controlling ferroelectric resistive switching and offer the guidance to design ferroelectric memristors with enhanced performance.

1. Introduction

Owing to their simple device architecture, high resistive switching (RS) on/off ratios and scalability, memristors with a metal/insulating oxide/metal (MIM) structure have been widely investigated as possible next-generation ultrahigh density nonvolatile random access memories and neuromorphic computation elements.[1–3] Oxide thin films such as TiO_2,[2,3] NiO,[4] and Cu_xO,[5] or doped perovskite oxides such as Cr/Fe-doped $SrTiO_3$[6,7] and Co-doped $BaTiO_3$ (BTO)[8] have been widely studied as the RS layer. Conducting filaments induced by thermally driven electromigration, defect percolation, as well as local redox processes based on oxygen-vacancy diffusion have been proposed as the underlying switching mechanisms.[9–12] In contrast to

Dr. A. P. Chen, Dr. D. Yarotski, Dr. A. Roelofs
Center for Integrated Nanotechnologies (CINT)
Los Alamos National Laboratory
Los Alamos, NM 87545, USA
E-mail: apchen@lanl.gov

Dr. W. Zhang, Dr. F. Khatkhatay
Department of Electrical and Computer Engineering
Texas A&M University
College Station, TX 77843, USA

L. R. Dedon, Prof. L. W. Martin
Department of Materials Science and Engineering
University of California
Berkeley, CA 94720, USA

L. R. Dedon, Dr. L. W. Martin
Materials Sciences Division
Lawrence Berkeley National Laboratory
Berkeley, CA 94720, USA

The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/adfm.202000664.

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Prof. D. Chen
Texas Center for Superconductivity
University of Houston
3369 Cullen Blvd, Houston, TX 77204, USA

Prof. J. L. MacManus-Driscoll
Department of Materials Science and Metallurgy
University of Cambridge
27 Charles Babbage Road, Cambridge CB3 0FS, UK

Prof. H. Wang
School of Materials Engineering
Department Electrical and Computer Engineering
Purdue University
West Lafayette, IN 47907, USA

Prof. J. Chen
School of Mathematics and Physics
University of Science and Technology Beijing
Beijing 100083, China

Prof. X. Gao
Institute for Advanced Materials and Laboratory of Quantum Engineering and Quantum Materials
South China Normal University
Guangzhou 510006, China

Prof. Q. X. Jia
Department of Materials Design and Innovation
University at Buffalo – The State University of New York
Buffalo, NY 14260, USA

the above mentioned metal oxides that are mostly nonferroelectric, the use of ferroelectric materials as the RS layer for memristors may lead to the design of high-performance, nonvolatile memory devices. For instance, ferroelectric tunneling junctions (FTJs) with an ultrathin ferroelectric layer have been proposed to realize memristive switching.[13–16] One of the advantages of using ferroelectric materials as the RS layer is that the polarization switching can provide another degree of freedom to control the RS behavior. It gives a diode-like current versus voltage characteristic, which could minimize sneak currents (at $V/2$) in crossbar resistive random access memory devices.[17] Therefore, systematic studies of memristive switching in ferroelectric materials are critical in understanding the underlying operation mechanisms and enabling ferroelectric memristors for neuromorphic computing and nonvolatile memory.[18]

The switchable diode effect (SDE) is considered as one of the most intriguing phenomena in metal/ferroelectric/metal (M/FE/M) memristors, where a relatively thick ferroelectric layer is used in comparison with an ultrathin ferroelectric layer used in FTJs. The SDE has been observed in memristors based on different ferroelectric materials including 5% $Al_{0.5}Nb_{0.5}O_3$-doped $Pb(Zr_{0.52}Ti_{0.48})O_3$ (PZT),[19] 30% Sr-doped BTO,[20] Ca-doped $BiFeO_3$,[21] $BiFeO_3$ (BFO),[22–25] and BTO (assuming a high dopant/acceptor concentration).[26] Different mechanisms have been proposed to explain the SDE. For example, oxygen-vacancy accumulation induced band bending,[18,27,28] polarization controlled depletion width,[29] and trapping/detrapping[20] and polarization[30] modulated Schottky barrier have been considered to explain the current injection in M/FE/M memristors. Additionally, bulk-controlled (e.g., charges, traps, and dopants) and interface-controlled conduction mechanisms have been studied at the M/FE interface.[25,31–37] It is well-known that defect movement is one of the key elements in filament-type switching memristors. However, the interplay among surface defect states, the M/FE interface, and the polarization of the ferroelectric is unclear,[38,39] which hinders the design of memristors that could take full advantage of ferroelectric materials as the RS layer. In this work, we develop a phenomenological model to quantitatively explain the current transport in ferroelectric memristors where Schottky interfaces and interfacial deep states are fully integrated into the model. We have confirmed that the polarization charge modulated Schottky barrier height and polarization coupled interfacial-deep states filling/emptying determine the SDE and the memristive switching in ferroelectric memristors.

2. *I–V* Hysteresis and Four Types of Switching Sequences

It is well-known that the rotation direction of pinched current–voltage (I–V) curves is a critical feature to understand the underlying physics of bipolar resistive switching. To facilitate the discussion, we compared four common bipolar I–V hysteresis characteristics reported in oxide films and defined them as type-I(A), type-I(B), type-II, and type-III. **Figure 1** shows schematic illustrations of I–V curves of the typical M/I/M structures with different bipolar RS behaviors. Many memristors using oxides as the RS layers show type-I(A)-like I–V characteristics

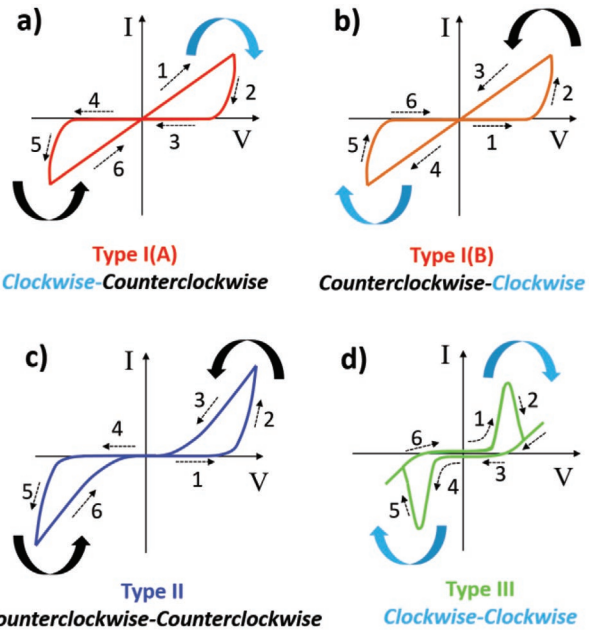

Figure 1. Four different rotation directions from bipolar RS I–V curves. a) Type-I(A), "clockwise–counterclockwise". b) Type-I(B), "counterclockwise–clockwise". c) Type-II, "counterclockwise–counterclockwise". d) Type-III, "clockwise–clockwise". It is noted that the detailed I–V curves in real devices may deviate considerably from these schematic sketches. The nonzero current at $V = 0$ in (c) and (d) could be due to the built-in field from polarization charge, trapped charge, and photovoltaic charge.

(clockwise–counterclockwise, also called "counter eight-wise"),[40] as shown in Figure 1a. This type-I(A) I–V curve has been widely reported in bilayer oxides such as TiO_2/TiO_{2-x} and Ta_2O_{5-x}/TaO_{2-x} systems.[1,3] On the other hand, a variety of oxide-based M/I/M memristors show different rotation directions such as the counterclockwise–clockwise curves shown in Figure 1b. Various mechanisms have been used to explain these type-I I–V characteristics including filament formation, oxygen-vacancy migration, Schottky-barrier-height modulation, and redox processes.[12,41] Interestingly, if a ferroelectric oxide is used as the active switching layer, I–V characteristics are completely different. Figure 1c shows the I–V curve for ferroelectric memristors where BFO deposited by pulsed laser deposition (PLD) is used as the ferroelectric layer. We defined this SDE[25] as the type-II like I–V curve (counterclockwise–counterclockwise). Figure 1d shows the I–V sketch of a typical ferroelectric capacitor (clockwise–clockwise, defined as type-III), which is different from type-II. The current humps shown in Figure 1d arise from the ferroelectric–polarization-switching current. Comparing the I–V data to that reported in the literature, it can be found that the type-II I–V curves are typically observed in BFO films with defects such as bismuth and oxygen deficiencies. The type-III I–V curves are reported in ferroelectric films such as BTO and BFO films without bismuth deficiency. We hypothesize that the existence of deep-level traps in the ferroelectric layer plays a critical role in determining I–V characteristics, schematically illustrated as type-II I–V curves shown in Figure 1c. As discussed later, the coupling between polarization and interfacial deep-level traps in the forbidden gap is one of the key factors to current transport across the M/FE interface.

3. Current Injection across Metal/Ferroelectric Oxide Interfaces

We first focus on the current transport in a M/FE/M structure, as shown in **Figure 2**a. Using classical semiconductor theory, we can treat the $Bi_{1-x}FeO_{3-\delta}$ as a p-type semiconductor (Section S1, Supporting Information) and divide the layer into three regions (Figure 2b).[42,43] The equivalent circuit of a M/FE/M memristor can be treated as two Schottky diodes connected back-to-back in series with a resistor (Figure 2c).[43] Disregarding the voltage polarity and the carrier types of the semiconductor, only one of these two Schottky diodes is reverse biased under a DC bias, and is where most of the voltage drop happens.[44] It is well-known that the *I*–*V* characteristics of a reverse-biased Schottky diode are mainly controlled by the barrier height. The current under reverse bias, defined by the blocking Schottky diode, is given by[42]

$$I_R = A^* A T^2 e^{-\beta(\phi_b - \Delta\phi)} \tag{1}$$

where $\beta = q/k_B T$, ϕ_b is the Schottky barrier height, $\Delta\phi$ is the barrier height modulation induced by charges near the electrode surface, A^* is the Richardson's constant, A is the contact area, k_B is the Boltzmann constant, and T is the temperature. The positive current is defined as the current moving from the gold electrode to the $SrRuO_3$ (SRO) when a positive voltage is applied to the top gold electrode with respect to the bottom SRO electrode.

At the metal–semiconductor interface, the image charges at the reverse-biased interface always decrease the barrier height, independent of the carrier type. The barrier lowering induced by the image charge in semiconductors is given by[42,44]

$$\Delta\phi_{\text{lowering}} = \sqrt{\frac{qE_m}{4\pi\varepsilon_0\varepsilon_{op}}} \tag{2}$$

where ε_0 is the permittivity of vacuum ($\varepsilon_0 = 8.85 \times 10^{-12}$ F m^{-1}), ε_{op} is the dynamic high-frequency dielectric constant of the film, and q is the electron charge ($q = 1.6 \times 10^{-19}$ C). If the semiconducting film is also a ferroelectric, polarization charges and polarization direction need to be considered for barrier height modulation. The maximum electric field E_m across the depletion region is given by[44,45]

$$E_m = \left| \sqrt{\frac{2qN_{\text{eff}}}{\varepsilon_0\varepsilon_{st}}(V + V_{bi})} + \frac{P}{\varepsilon_0\varepsilon_{st}} \right| \tag{3}$$

where ε_{st} is the static low-frequency dielectric constant, V is the voltage drop across the reverse bias contact, V_{bi} is the built-in voltage, and N_{eff} is the effective fixed charge density in the depletion region. The term $\frac{P}{\varepsilon_0\varepsilon_{st}}$ in Equation (3) is the polarization charge contribution wherein P is the polarization charge density in μC cm^{-2}. The polarization charge contribution in Equation (3) can be both positive and negative, depending on the polarization direction and it is often larger than the fixed charge contribution. To make Equations (2) and (3) mathematically valid, an absolute value function is included in

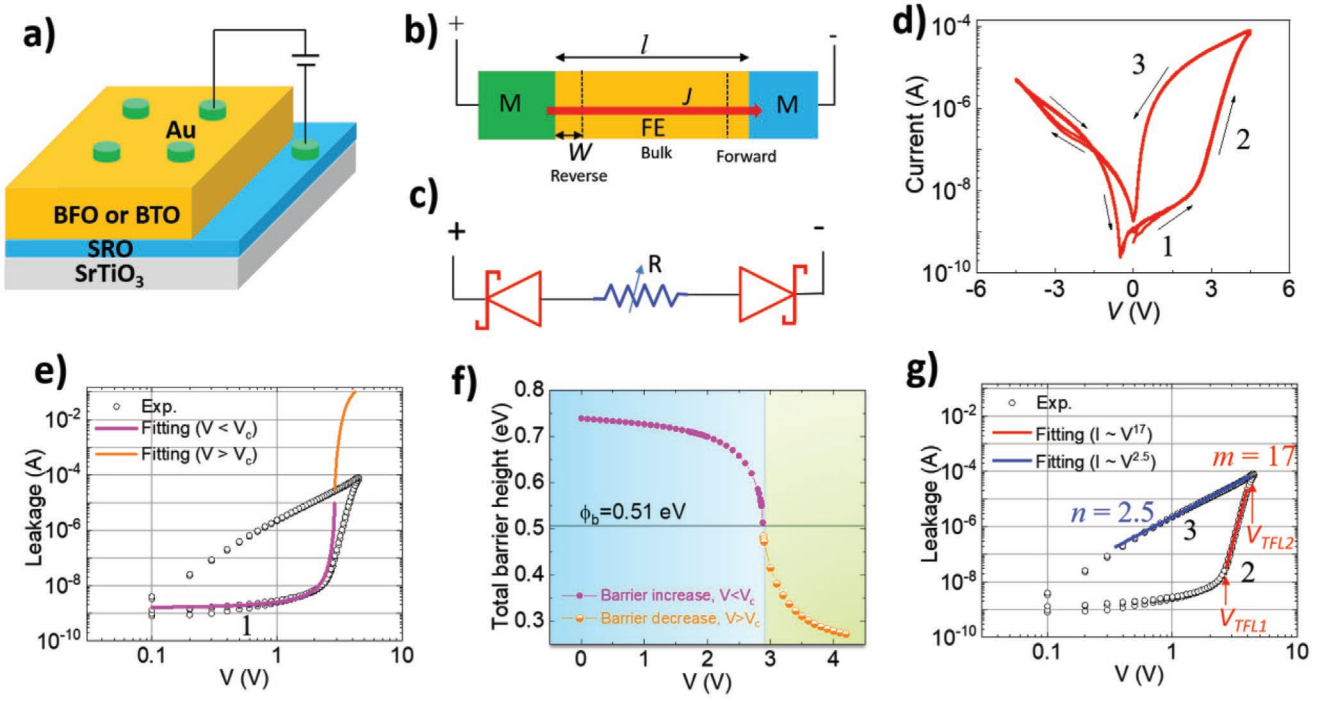

Figure 2. Current–voltage analysis of ferroelectric memristors with considering polarization effect. a) Schematic illustration of an M/FE/M device. b) Schematic illustration of the current injection in the M/FE/M structure. c) Equivalent circuit of the M/FE/M. d) A typical *I*–*V* characteristic of the Au/BFO/SRO device, where a BFO film was deposited using a $Bi_{1.05}FeO_3$ ceramic target. e) Fitting of the *I*–*V* curve in the segment 1 by Equations (1)–(3). f) Voltage dependent total barrier height. The barrier height is larger than the pristine barrier height (0.51 eV) for $V < V_c$ and smaller than that for $V > V_c$. g) Fitting of segments 2 and 3 shown in (d) by Equations (6) and (8), respectively.

Equation (3). When $V > V_c$ (V_c is the coercive voltage of the ferroelectric material), polarization charge has the same sign with fixed charge in the depleted region and both effects lower the Schottky barrier height, as discussed by Pintilie and coworkers.[37,44,45] It should be noted that when $V < V_c$, the polarization charge has an opposite sign with respect to the fixed charge. Under such circumstances, polarization charge actually increases the barrier height. To describe the barrier modulation by polarization in ferroelectrics, Equation (2) is rewritten as

$$\Delta\phi_{\text{increasing}} = -\sqrt{\frac{qE_m}{4\pi\varepsilon_0\varepsilon_{op}}}\ (V < V_c) \tag{4}$$

$$\Delta\phi_{\text{lowering}} = \sqrt{\frac{qE_m}{4\pi\varepsilon_0\varepsilon_{op}}}\ (V \geq V_c) \tag{5}$$

A dramatic barrier lowering occurs near V_c which results in an exponential increase of the injection current across the M/FE Schottky interface. Such behavior has rarely been seen in real ferroelectric devices.[32,34] When $V > V_c$, polarization significantly lowers the Schottky barrier height which allows this contact to supply enough carriers. In other words, the Schottky interface becomes a nonblocking contact and supplies a reservoir of carriers ready to enter the ferroelectric as needed.[46] In such circumstances, the conduction above V_c can be dominated by the bulk-limited conduction such as space-charge-limited-conduction (SCLC) or Poole–Frenkel emission and both of them are related to traps/dopants.[47,48] If deep-level traps exist, the SCLC current is given by[47,48]

$$I_{\text{trap}} \propto V^m, (V_{\text{TFL1}} < V \leq V_{\text{TFL2}}, m > 2) \tag{6}$$

$$I_{\text{trap free}} \propto V^2, (V > V_{\text{TFL2}}) \tag{7}$$

where V_{TFL1} represents the on-set voltage of the trap-filling limit (TFL) and V_{TFL2} is the voltage at which all deep-level traps are filled. When all traps are filled, Child's law governs the current flow ($V > V_{\text{TFL2}}$) as the material can be treated as a trap-free insulator. Unfortunately, there is no direct correlation between V_c and V_{TFL1} in the literature. In the case of $V > V_{\text{TFL1}} \geq V_c$, I_R in Equation (1) modulated by polarization charge can be far larger than I_{trap} in Equation (6). Therefore, the power law and square law in Equations (6) and (7) dominates the *I*–*V* curves when the applied bias is larger than V_{TFL1}.

During voltage ramping down, the *I*–*V* curves could maintain a similar power law if the trap filling process is coupled with ferroelectric polarization. Here, we define a new polarization coupled SCLC current for the voltage ramping down

$$I_{\text{polarization coupled SCLC}} \propto V^n, (0 < V, 2 \leq n < m) \tag{8}$$

One of the key features of the polarization coupled SCLC is that the space charges in surface deep traps will not be released when $V \leq V_{\text{TFL}}$. Therefore, the ferroelectric memristors form a "triangle" hysteretic *I*–*V* curves and polarization coupled trap filling/emptying plays a critical role. When the trap filling/emptying is fully engaged by polarization charges, $n = 2$. This is an ideal case for polarization coupled SCLC. There are two possible scenarios for $n > 2$. In the case that the applied voltage is less than V_{TFL2}, the trap filling process is partially coupled by polarization. In the case of the coexistence of interfacial and bulk traps, only interfacial traps are preferably coupled by polarization charges. In both cases, trap filling and emptying are only partially coupled by polarization charges. Therefore, the slope n of the power law described in polarization coupled SCLC is larger than 2 but is smaller than m shown in Equation (6).

From the above analysis, it can be seen that polarization charge increases the Schottky barrier height and suppresses the leakage current. This consequently results in an increase of the high resistance state (HRS), which therefore leads to much larger on/off ratios for ferroelectric memristors and reduced switching current. The low resistance state (LRS) can be optimized by maximizing polarization coupled SCLC and limiting the bulk traps. It should be noted that the above discussion of the current injection in M/FE/M structure, as illustrated in Figure 2b, assumes that $l > 2w$ and $l >> l_c$, where l is the film thickness, w is the depletion width (on the order of a few nanometers), and l_c is the charge screening length (on the order of 1 Å).[49,50] When the film thickness is reduced to just a few nanometers with $l \approx 2w$, the M/FE/M structure turns into an FTJ. The memristive behavior in FTJs has been explained by electroresistance effects.[50]

4. *I*–*V* Characteristics Analysis

Using the current injection theory discussed above, the conduction in M/FE/M can be quantitatively explained. Figure 2d shows the *I*–*V* hysteresis loops of Au/$Bi_{1-x}FeO_{3-\delta}$/SRO memristors. The asymmetric hysteresis is probably due to the asymmetric contact electrodes,[36] or stoichiometry variations through the film thickness. The *I*–*V* curve under positive bias is divided into three segments (1, 2, and 3, Figure 2d). Segment 1 is defined as the polarization assisted Schottky-interface limited conduction; segment 2 is defined as the polarization coupled trap filling limited conduction; and segment 3 is defined as the polarization coupled trap emptying limited conduction. Segment 1 in Figure 2e can be fitted by Equation (1), where the increase of the barrier height described by Equation (3) is taken into consideration. The relationship between P and V is described by a Landau-type model (Figure S1, Supporting Information).[51] The pristine barrier height without polarization effects is estimated to be 0.51 eV (see Section S2, and Figures S2–S4, Supporting Information). The fittings show that the total barrier height for hole injection at the Au/BFO interface is 0.74 eV at zero bias with polarization effects; a 45% increase with respect to the pristine barrier height. The total barrier height then decreases with increasing voltage (Figure 2f). The most significant reduction of the barrier height occurs near V_c, which should result in a significant increase of current near V_c (Figure 2e). Apparently, the deviation of *I*–*V* characteristics based on a Schottky model from experimental data near V_c (segment 2) indicates other conduction mechanisms when $V > V_c$. Indeed, the Au/BFO becomes nonblocking interface and the bulk conduction starts to dominate.

Segment 2 can be fitted by the power law described by Equation (6), where deep-level trap filling is the limiting factor

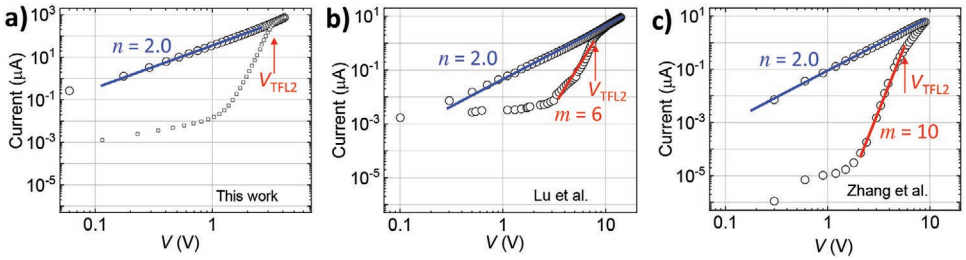

Figure 3. Fitting of *I–V* curves. Fitting of ramping down *I–V* curves (segment 3) for a) this work, Au/BFO(150 nm)/SRO(20 nm)/STO (001) grown from a $Bi_{1.05}FeO_3$ target. b) Pt/BFO (450 nm)/SRO(60 nm)/STO (001) grown from a stoichiometric BFO target.[53] c) Pt/(Sm, Ni)-doped BFO (250 nm)/FTO/glass from a $Bi_{0.925}Sm_{0.075}Fe_{0.95}Ni_{0.05}O_3$ target.[54] The *P–E* loops for these samples are shown in Figure S5 of the Supporting Information.

(Figure 2g). Log (I) versus Log (V) displays a linear relationship with a slope of $m = 17$. Different from Rose–Lampert theory,[47,48] Zhang and Pantelides proposed that the power law dependent current is due to the interplay between dopants and deep traps by considering the Poole–Frenkel emission.[52] When traps are filled by carriers, the BFO can be treated as a trap-free material. At voltage above the trap filling level ($V > V_{TFL2}$), the *I–V* curves follow Child's law ($I \approx V^2$).

Segments 2 and 3 are expected to overlap in a nonferroelectric M/I/M structure if the current is in the steady-state. Interestingly, segment 3 in the M/FE/M structure follows polarization coupled SCLC as shown in Equation (8). In Figure 2g, $n = 2.5$ was found. It was mainly due to the applied bias is slightly less than V_{TFL2} (i.e., not all interfacial deep traps were coupled by polarization charges). **Figure 3**a shows that an ideal $n = 2$ type *I–V* curve can be achieved in segment 3 by applying a bias larger than V_{TFL2}. Such a proposed model can also be used to fit some reported data.[53,54] Segments 2 and 3 of *I–V* curves for epitaxial BFO films and polycrystalline Sm/Ni-doped BFO films can also be fitted by Equations (6)–(8), as shown in Figures 3b,c. Both examples show an ideal Child's law type *I–V* curve with $V > V_{TFL2}$ (described by Equation (7)) during voltage ramping up and $n = 2$ was maintained during voltage ramping down. Generally, literature data shows $2 < n < m$ during voltage ramping down.[33] The reasons for such behavior have been discussed earlier. It is not surprising that the *I–V* characteristics at segment 1 are different in these samples as thermally activated free carriers as well as the trap/dopant concentration and energy level are different. In addition, although both type-I(B) and type-II in Figure 1 show the same *I–V* sequences for segments 1–3, the *I–V* behavior of segment 3 is different. In nonferroelectric M/I/M structures, segment 3 often shows an Ohmic behavior ($n = 1$) during the bias ramping down due to the formation of conducting filaments.[5] While in ferroelectric memristors with SDE, it follows Equation (8).

5. Band Diagram Analysis

To show a clear physical picture of the SDE process as discussed above, a flow chart of the band diagram and polarization modulation are illustrated. One of the important assumptions of this work is that the surface/interface trap states filling and emptying are coupled with polarization reversal. **Figure 4**a illustrates an SDE-type *I–V* curve with different segments. At zero bias, the device has just experienced a negative bias (segment 6) at the Au/BFO interface where the polarization is pointing up as shown in Figure 4b. All interfacial deep level traps at the Au/BFO (p-type) interface are coupled by positive polarization charges. If the holes are the majority carriers, only the Au/BFO (p-type) interface is relevant as it is reversely biased for hole injection. A dramatic effect is that the positive polarization charges at the Au/BFO interface actually increase the Schottky barrier for hole injection, compared to the pristine barrier height, as shown in Figure 4c. For example, the Schottky barrier height is 0.74 eV at zero bias with the established polarization, which is much larger than the pristine barrier height of 0.51 eV, as discussed before. When a small positive voltage ($V < V_c$) was applied to the Au/BFO interface (segment 1), such an external field suppresses the already established up polarization, but it is not large enough to switch the polarization (Figure 4d). The applied bias, however, is able to slightly reduce the total barrier height. This will result in the slow rise of the current in segment 1. It should be noted that the total barrier height (Figure 4e) is still larger than the pristine barrier height when $V < V_c$ as shown in Figure 2f. A further increase of the applied bias with $V > V_c$ switches the up polarization to down polarization (Figure 4f). Once the polarization is switched, the negative polarization charges at the Au/BFO interface significantly lower the barrier height (Figure 4g). In addition, the trap filling in segment 2 is coupled with the polarization and once all interfacial traps are filled, the *I–V* curves perfectly follow Child's law at $V > V_{TFL2}$ (Figure 3a). In this ideal case, the *I–V* curves could also follow Child's law in segment 3 as the space charges in the interfacial deep traps coupled with polarization stay immobile even when the voltage is reduced below V_{TFL2} (Figure 4h). As discussed before, the slope n for segment 3 is often larger than 2. In segment 3, the polarization modulates detrapping process and the current is defined by polarization coupled SCLC.

6. SDE Mechanisms Discussion

The underlying mechanism of SDE is one of the critical questions in memristors using ferroelectric materials as the RS layer.[32] It is well accepted that polarization mediated barrier modification plays a critical role in the electron transport at M/FE interface.[25] Pintilie and co-workers pointed out that SDE is not uniquely determined by the polarization reversal as it is absent in some ferroelectric films such as PZT,[32] and BTO films.[55] Indeed, literature data have shown that the

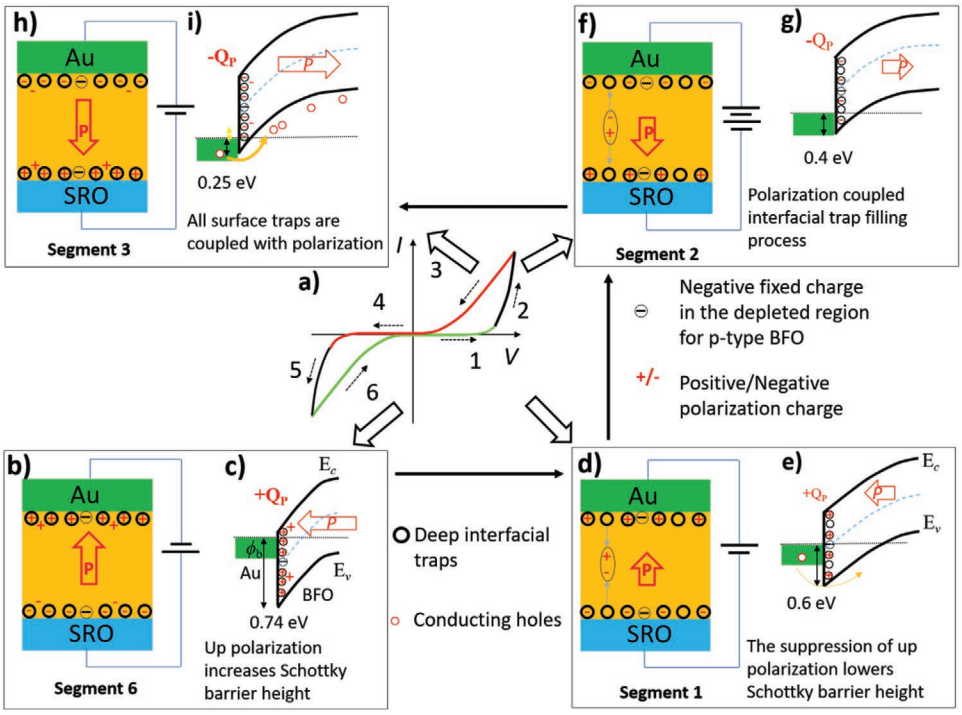

Figure 4. Band diagram analysis of Au/BFO/SRO memristors. a) A schematic illustration of an *I–V* curve with defined segments from 1 to 6. b–i) Schematic illustrations of the Au/BFO/SRO heterostructures with the interaction of traps and polarization charges and the energy band diagram for segments 1, 2, 3, and 6. In segment 6, left (up) polarization is pre-established. In segment 1, the established up polarization is weakened by the applied voltage. In segment 2, the applied bias switches the polarization. Both filling of interfacial deep traps and Schottky barrier height are influenced by polarization. The band edge offset values estimated from the fitting of the *I–V* curves are used to qualitatively illustrate the band bending.

type-II *I–V* curves were only observed in BFO and some other doped ferroelectric materials such as doped PZT,[19] Sr-doped $BaTiO_3$,[20] and Ca-doped BFO.[21] Therefore, SDE requires ferroelectricity, but ferroelectricity does not guarantee the SDE effect. The absence of the type-II *I–V* curves in some memristors with ferroelectric materials such as PZT, BTO, and BFO (≤213 K) as RS layers[32,53] suggests that other factors such as defects have to be considered to fully explain the SDE. Phase-field simulations have assumed high dopant/acceptor concentrations in BTO to generate SDE.[26] In addition, the impact of cation stoichiometry on current injection in BFO has been discussed.[56,57] Tsurumaki et al. reported that BFO films grown by a $Bi_{1.2}FeO_3$ target exhibit type-III *I–V* curves while films grown by $Bi_{1.1}FeO_3$ and $Bi_{1.0}FeO_3$ targets have shown type-II behavior at the Au/BFO interface.[56] Lee et al. found that BFO films with bismuth deficiency (grown by a $Bi_{1.0}FeO_3$ target) exhibit SDE (type-II) while bismuth-rich BFO films (grown by a $Bi_{1.1}FeO_3$ target) display a bipolar RS behavior.[57] It should be noted that this bipolar RS should be interpreted as a combination of type-II at the Au/BFO interface (segments 1→3 in Figure 1b) and type-III at the BFO/SRO interface (segments 4→6 in Figure 1c), rather than the type-I(B). These results indicate that the SDE is related to the bismuth deficiency. **Figure 5**a shows the *I–V* hysteresis of the Au/BFO/Nb:STO grown by the sol–gel method. This polycrystalline BFO capacitor exhibits a type-III hysteresis. The corresponding *P–E* loops and *I–V* curves are shown in Figure S6 of the Supporting Information. Rutherford backscattering spectrometry measurements show that Bi/Fe = 1.17 for this sample (Figure S7, Supporting Information). Therefore, it can be concluded that BFO films with excess Bi tend to exhibit the type-III *I–V* hysteresis and bismuth deficiency (probably also oxygen deficiency) promotes SDE with the type-II *I–V* hysteresis.

Another critical parameter is the Schottky contact at the Au/BFO interface as it determines the HRS. To prove the key role of the Schottky interface in SDE, *I–V* curves were measured for $SRO/Bi_{0.92}Fe_{0.98}O_{2.67}/SRO/DyScO_3$ (110) heterostructures which exhibit both bismuth and oxygen vacancies.[58] The rotation direction of *I–V* curves of these samples in Figure 5b is the same as the type-II, but the hysteresis is very limited. It indicates that the bismuth/oxygen deficiencies alone are not enough to generate SDE with large opening in hysteresis. The lack of Schottky contact between the SRO and the BFO could be the origin of such behavior. Therefore, both bismuth/oxygen vacancies and Schottky barrier are critical parameters to produce SDE in ferroelectric memristors with a large *I–V* hysteresis.

The above discussion is consistent with the physics described in the phenomenological model. It was proposed that the SDE in ferroelectric memristors is controlled by the polarization increased Schottky barrier height (dominating the HRS) and polarization coupled SCLC (dominating the LRS). The existence of deep-level traps and dopants could be tied to bismuth/oxygen vacancies and the electrode material controls the contact beahvior. Shallow traps/dopants contribute to thermally activated free carriers, which decrease the HRS in segment 1. In addition, because the filling and emptying of bulk traps are

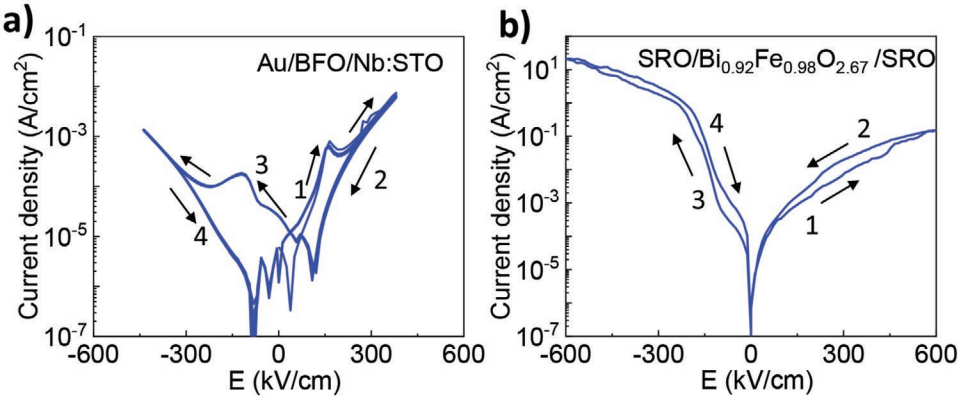

Figure 5. *I–V* curves of BFO memristors with different electrodes. a) *I–V* curves of Au/BFO/Nb:STO (001) heterostructures grown by the sol–gel method. It matches with the type III in Figure 1d. b) *I–V* curves of PLD grown SRO/$Bi_{0.92}Fe_{0.98}O_{2.67}$/SRO/$DyScO_3$ (110) heterostructures. *P–E* loops and *I–V* curves of these samples in log scale are shown in Figure S6 of the Supporting Information.

unlikely coupled to polarization, the slope in segment 3 deviates from the ideal value of 2, which affects the LRS. It is, therefore, important to limit the existence of bulk traps and shallow dopants to enhance the on/off ratio. With a Schottky contact at the M/FE interface, the HRS in the segment 1 can be significantly enhanced due to the increased barrier height by polarization. Therefore, the SDE in ferroelectric memristors can be explained by the polarization modulated Schottky barrier height and the polarization assisted SCLC.

7. Conclusion

By using $BiFeO_3$ as the RS layers in ferroelectric memristors, we have investigated the underlying mechanisms of current injections across the metal/ferroelectric interface. The type-II *I–V* curves have been explained by simple semiconductor theories by taking consideration of polarization modulated Schottky barrier and polarization coupled deep traps filling/emptying. The SDE is critically tied to bismuth/oxygen vacancies and contact materials which control the formation of interfacial deep states and the Schottky barrier, respectively. These findings provide insights to understand ferroelectric memristive switching behavior and demonstrate new strategies to tune ferroelectric memristors via defect and interface engineering.

8. Experimental Section

PLD (KrF excimer laser, $\lambda = 248$ nm) was employed to grow BFO films on SRO-buffered $SrTiO_3$ (STO) (001) substrates. A $Bi_{1.05}FeO_3$ target was used to deposit BFO films. The substrate temperature was maintained at 680 °C for the growth of both SRO and BFO layers. SRO bottom electrodes (≈18 nm) were deposited under 100 mTorr oxygen and 2 Hz repetition rate. BFO films with a thickness of ≈150 nm were grown at 10 Hz with an oxygen pressure of 20 mTorr. After deposition, the BFO/SRO/STO stacks were annealed at 400 °C and 1 atom oxygen for 1 h before cooling down to room temperature at 5 °C min^{-1}. The growth, structural and chemical characterization of ferroelectric heterostructures and thin films including Au/BTO/SRO/STO (001), Au/BFO/SRO/STO (001), SRO/BFO/SRO/$DyScO_3$ (110), Pt/BFO/SRO/STO (001), and Pt/(Sm, Ni)-doped BFO/FTO/glass have been reported elsewhere.[53–55,58,59] Au/BFO (400 nm)/Nb:STO(001) with Bi/Fe ratio of 1.17, fabricated by the sol–gel method (from MTI Corp.), were also investigated. The BFO films grown by the sol–gel method are polycrystalline. Circular Au (≈100 nm thick) top electrodes with a diameter of 350 µm defined by a shadow mask were deposited by magnetron sputtering at room temperature. The ferroelectric hysteresis loops of the devices were tested by an aixACCT TF Analyzer 1000 and ferroelectric tester Premier II (Radiant Technologies, Albuquerque) at 0.1–1 kHz. An Agilent E4980A precision LCR meter was used to conduct the *I–V* hysteresis loops. To reveal DC leakage currents, a voltage-step technique with longer charging and discharging time was used (≈250 ms per data point).[60] During the *I–V* and *C–V* measurements, a small AC field of 50 mV (10–20 kHz) was superimposed on the applied DC voltage in the LCR meter. The effect of this AC field on the total *I–V* curves can be ignored at the current DC bias measurement range (Figure S8, Supporting Information).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

ferroelectrics, memristive switching, metal/oxide interfaces, oxide thin films, semiconductors

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Aiping Chen is a staff scientist at the Center for Integrated Nanotechnologies (CINT) at Los Alamos National Laboratory. CINT is a U.S. Department of Energy funded nanoscience research facility that provides users from around the world with access to state of the art expertise and instrumentation in a collaborative, multidisciplinary environment with a focus on nanoscience integration. Chen is leading the efforts on the synthesis and characterization of complex oxide heterostructures and nanocomposites. His recent research focuses on emergent phenomena in quantum materials and the development of electronic devices.

Quanxi Jia is an Empire Innovation Professor and National Grid Professor of Materials Research at the University at Buffalo (UB) – the State University of New York. He is also the Scientific Director of New York State Center for Excellence in Materials Informatics. Prior to joining UB in 2016, he was the Director of the CINT, a DOE Nanoscale Science Research Center operated jointly by Los Alamos and Sandia National Laboratories. Jia's research includes the synthesis and study of structure–property relationships of nanostructured materials, multifunctional materials, and thin films, as well as the development of microelectronic/electro-optic devices.