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Innovative Solid-State Bonding Designs and Techniques for High Power Electronic and Laser Diode Packaging

DISSERTATION

submitted in partial satisfaction of the requirements for the degree of

DOCTOR OF PHILOSOPHY

in Engineering

by

Yi-Ling Chen

Dissertation Committee:
Professor Chin C. Lee, Chair
Professor James C. Earthman
Professor Frank G. Shi

2016

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DEDICATION

To

my dear family

For supporting, understanding, and encouraging me to believe in myself,
all of you help me make it possible to complete this dissertation.

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1. Y. L. Chen, and C. C. Lee, “Novel silver solid-state bonding designs between two copper structures”, under review

2. Y. Huo, S. W. Fu, Y. L. Chen, and C. C. Lee, “A reaction study of sulfur vapor with silver and silver-indium solid solution as a tarnishing test method”, under review

3. Y. Y. Wu, Y L. Chen, and C. C. Lee, “Solid state bonding of silicon chips to copper substrates using silver with cavities”, Journal of Materials Science: Materials in Electronics, vol. 27, pp. 3347-3354, Dec. 2015

4. Y. L. Chen, Y. Y. Wu, and C. C. Lee, “A solid-state bonding technique of large copper wires for high power devices operating at high temperature”, Journal of Materials Science: Materials in Electronics, vol. 26, pp. 3521-3529, Mar. 2015

- **Published Conference Proceedings and Conference Presentations**

1. Y. L. Chen, Y. Huo, and C. C. Lee, “Design and fabrication of silver solid solution layer on silicon and its solid-state bonding applications” in IEEE 66th Electronic Components and Technology Conference (ECTC), 2016, accepted

2. Y. L. Chen, Y. Y. Wu, and C. C. Lee, “Silver-assisted copper wire bonding using solid-state processes,” in IEEE 64th Electronic Components and Technology Conference (ECTC), 2014, pp. 1529-1532

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4. Y. L. Chen and C. C. Lee, “Strength of solid-state silver bonding between copper,” in IEEE 63rd Electronic Components and Technology Conference (ECTC), 2013, pp. 1773-1776

ABSTRACT OF THE DISSERTATION

Innovative Solid-State Bonding Designs and Techniques for High power Electronic and Laser Diode Packaging

by

Ying-Ling Chen

Doctor of Philosophy in Engineering

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Professor Chin C. Lee, Chair

Rapid evolution of electronics industry has made the adoption of high performance chips more urgent. In fact, those chips cannot be used unless high temperature die attach materials and methods are available. The conventional die attach methods typically require a processing temperature 20-30 °C above the melting temperature of bonding material, which melts and reacts with to-be–bonded parts to form the bonding joint. For high temperature applications (> 400 °C), the processing temperature will sharply increase along with the increased melting temperature to reach the molten phase. However, such high processing temperature will damage nearly all electronic components. To respond to such challenge, the metal bonding is considered to be a possible solution.

In this dissertation, the solid-state bonding technique is employed for various bonding designs by electroplating Ag-based and In-based systems as bonding media. No molten phase or flux is involved. For most cases, the bonding conditions are conducted at 300 °C with 6.89 MPa (1,000 psi) pressure for a dwell time of 3 min in vacuum. The bonding time, 3 min, is constrained by the furnace. It is worth mentioning that this pressure is less than 10% of what is

used in industrial thermo-compression processes.

To begin with, silver (Ag) was chosen as a bonding medium because of its exceptional properties and reasonable price. There are two designs for the Ag layer. For the first design, the 50 μm Ag layer plated on the copper (Cu) substrate is initially annealed at 400 °C for 5 h to increase Ag grain sizes, thereby making it easier to deform during bonding. For the second design, the 10 μm Ag layer is plated on the substrate and followed another 5 μm Ag with cavities. The fundamental concept is to release the thermal induced stress by creating cavities in the Ag layer to allow easier plastic deformation for the bonding medium. The resulting Ag layers are then bonded to the Cu chips. For both designs, all samples are bonded well and pass MIL-STD-883J method 2019.9. The Ag layer is also applied to the Cu wire bonding. To overcome Cu oxidation issue, the bonding surface on the 1 mm Cu wire is plated a 50 μm Ag layer. An annealing step is followed to facilitate the Ag layer easier to deform and conform to the Cu or Si bonding surfaces. In-plane pull test and vertical pull test are performed to measure the breaking force of the wire bonds. For wire-bonds made on the Cu substrate, the breaking forces on in-plane pull test are greater than 20 kg. The breaking forces on vertical pull test are approximately one-half of in-plane pull test results. For wire-bonds made on Si chip, breaking forces are approximately 80% of those made on Cu substrate.

Next, the novel method is to bond the Si chips to Cu substrates directly. This structure design can provide low-resistance paths for electricity and heat. There is no specific joint used in between. The basic concept is to provide room for Cu and Si to deform without restriction by producing trenches inside the Cu substrate. When the bond between two surfaces is formed, the trenches inside the Cu substrate could release the part of thermal stress from the coefficient of thermal expansion CTE mismatch. Therefore, the bond could deal with the large CTE mismatch

between Si (3 ppm/°C) and Cu (17 ppm/°C). The cross-sectional images show that the Si chips are well bonded to the Cu substrates without visible voids and cracks. After the bonding process, the simple shear tests are conducted to evaluate the bond strength, while the Si chips are all broken first. It demonstrates that the bond is stronger than the Si chip itself.

Finally, the Ag-rich Ag-In solid solution layers have successfully developed on Si and silicon carbide (SiC) chips. Ag has definite advantages among metals, but it still has its own weaknesses, which can actually or potentially lead to failure. That is Ag can be tarnished not only when exposed to certain corrosive gases such as hydrogen sulfide or sulfur gas but also under normal atmospheric conditions for a long period of time. Ag-In solid solution is further studied while Ag-In binary system has been demonstrated with an exceptional anti-tarnish property. To fabricate the single phase Ag-In solid solution, the Ag/In/Ag multilayers are electroplated on the chips. Importantly, the bottom Ag layer is initially annealed at 350 °C to increase its grain sizes and to reduce grain boundaries, inasmuch as the reaction rate between Ag and In is subject to the microstructure of Ag layer. The In/Ag layers are followed to be plated onto Si chip. To decompose $AgIn_2$ and Ag_2In, the two-step annealing process is then performed in a vacuum environment at 180 °C and 350 °C, respectively. After the bonding process, the compositions of resulting joints are measured by SEM/EDX, which is a homogeneous Ag-rich Ag-In solid solution.

In this study, five different bonding designs are reported. All bonds made between the chips and the substrates are fabricated at relatively low processing temperatures. The bonding structures are designed to be used for high operating temperatures. The results are encouraging. These novel methods may bring a chance for those who need die-attach materials for high performance electronic devices under severe environmental conditions in industries.

Chapter One

Introduction

1.1 Electronic Packaging

In electronics manufacturing, electronic packaging is the bridge that interconnects the integrated circuits (ICs) and other components into a system level interconnection to form electronic devices. The functions of packaging mainly include power distribution, signal distribution, heat dissipation, mechanical support, physical protection, and environmental protection [1-2], as shown in Fig 1.1. Importantly, the improper packaging of IC could seriously limit device performance and degrade reliability. Electronic packaging materials and techniques in fact play a key role for electronic systems with excellent performance. Therefore, the rapid development of electronics industry has led to active research for advanced packaging technology.

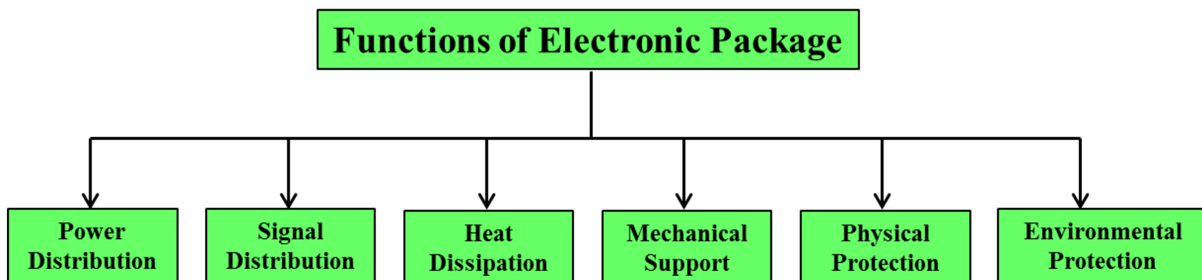

Fig. 1.1 Basic electronic package functions

Table 1.1 ITRS Single-chip Package Technology Requirements

Year of Production		2016	2018	2020	2022	2024	2026
Low-end, Low cost package	Cost (Cents/Pin)	0.20-0.32	0.20-0.29	0.20-0.26	0.19-0.25	0.19-0.25	0.17-0.25
	Power Density (W/mm^2)	0.5/40	0.5/40	0.5/40	0.5/40	0.5/40	0.5/40
	Pin Count (Maximum)	100	100	100	100	100	100
	Performance: On Chip (MHz)	50	50	50	50	50	50
High Performance	Cost (Cents/Pin)	1.15	1.04	0.94	0.85	0.77	0.73
	Power Density (W/mm^2)	0.70	0.80	0.90	1.00	1.10	1.20
	Pin Count (Maximum)	6501	7167	7902	8712	9148	9605
	Performance: On Chip (GHz)	9.18	10.65	12.36	14.34	15.41	16.18

The International Technology Roadmap for Semiconductors (ITRS) is one of the best sources for acquiring requirements of assembly and packaging based on continuing development of IC [3]. Table 1.1 lists some of the ITRS projections such cost, power density, pin count and operating frequency onto a single-chip packaging for low cost and high performance product categories. The data presented clearly indicates that high temperature, high power, and high frequency applications will increase along with increased functionality. In order to address the

common needs of high performance devices, the die attach materials are first reviewed to meet basic requirements to be operable at high temperatures. In what follows, challenges and techniques for high temperature die attach materials are then discussed. The dissertation outline is given at last.

1.2 The Die Attach Materials

Die attach materials are used to bond the chip (die) and the substrate. Fig. 1.2 portrays a simple packaging device. The popular bonding materials are solder alloys (eutectic and soft solders), polymer-based electrically conductive adhesives (ECAs), and silver (Ag) based pastes (Ag-glass and sintered nano-Ag pastes) [4-7]. Table 1.2 presents some bonding materials studied

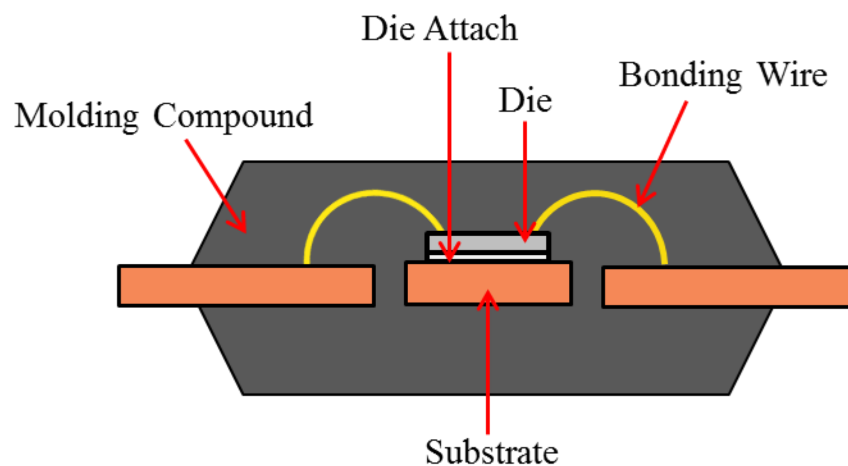

Fig. 1.2 A simple packaging device

Table 1.2 The popular die attach materials with melting and operating temperatures.

Die-attach materials	Melting Temperature (°C)	*Operating Temperature (°C)
Sn63Pb37	183	92
Sn96.5Ag3Cu0.5	217	119
Au80Sn20	280	170
Pb95.5Ag2.5Sn2	300	185
Au88Ge12	356	230
Au97Si3	363	236
Elecolit® 327 (ECA)	120-150 (Processing temperature)	275 (Literature review)
Sintered nano-Ag paste	280 (Processing temperature)	< 600 (Literature review)
Ag	961	715

from literatures, including their melting temperatures and their operating temperatures which are calculated by homologous temperature of 80 % [8-12]. From the Table 1.2, the lead-tin eutectic solder, lead-free solder, and gold-tin eutectic cannot sustain temperatures higher than 170 °C [13]. Even in the case of high lead lead-tin solder, the operating temperature is only 185 °C. The maximum operating temperature of gold (Au) based solders is approximately 240 °C; nevertheless, the cost is extremely high due to high percentage of Au [14]. In addition to the

solder alloys mentioned above, some of ECAs used in commercial devices, fail at temperature near 275 °C. Regardless of the category of the die attach materials, the relatively low melting temperatures of those materials is considered to be a serious issue, thereby preventing them from being employed as a possible solution for high temperature applications. For high temperature electronic modules incorporating silicon carbide (SiC) and gallium nitride-based (GaN) devices, a new bonding medium for high temperature applications is the nano-Ag paste [15]. After sintering, the paste can be turned into pure silver and then would be able to handle high operating temperature. The sintering process often requires relatively high temperature and pressure to obtain significant densification and create the joint [16-17]. The resulting Ag joints cannot be made pore-free. A major concern with pores involves the loss of thermal conductivity.

Rapid evolution of electronics industry has made the adoption of high performance chips more urgent. In fact, those chips cannot be used unless high temperature die attach materials are available. The development of high temperature bonding material not only is a technological challenge for achieving better performance, but also a critical step for possible new generation of the electronic products.

1.3 Challenges for High Temperature Die Attach Materials

There are two major issues for high temperature die attach materials. Firstly, the high operating temperature bonding joint has to be achieved without the high processing temperature. The conventional die attach method typically requires a processing temperature 20-30 °C above the melting temperature of bonding material. During the molten phase, the bonding material melts and reacts with to-be–bonded parts to form the bonding joint. For high temperature applications (> 500 °C), the processing temperature will sharply increase along with the increased melting temperature to reach the molten phase. However, such high processing temperature will damage nearly all electronic components. Clearly, increased operating temperature is required, but increased processing temperature is not desirable.

Secondly, high temperature electronic devices demand efficient thermal management. The most important thermal properties are coefficient of thermal expansion (CTE) and thermal conductivity. The concern of high temperature die attach materials is the difference of CTE between chips and substrates, for example, Si chips (3 ppm/°C) and Cu substrates (17 ppm/°C). This pair creates large CTE mismatch and results in thermal stress after the die attach process. A suitable die attach material must be able to deal with severe CTE mismatch. In addition, thermal dissipation is another concern. For example, the heat generated in the laser diode is dissipated by

attaching a heat sink. The die attach material must ensure an efficient heat transfer through the thermal interface, since their performance decreases drastically with increasing chip temperature [18-20].

To overcome these challenges, it is very essential to select the proper die attach material which has excellent properties, high melting temperature and low processing temperature. Table 1.3 lists some properties of popular die attach materials. From the Table 1.3, Ag is a possible solution as it has high melting temperature, excellent ductility, low yield strength, and superior electrical and thermal conductivity. The difficulty is how to find a method to form Ag joints at low temperature with low pressure.

Table 1.3 Some properties of popular die attach materials

Properties	Cu	Ag	Au	Sn	Sn3.5Ag
Melting temperature (°C)	1,083	961	1,063	231	221
Density (gm/cc)	8.94	10.5	19.3	7.29	7.4
Thermal conductivity (watt/cm-K)	3.862	4.075	3.151	0.665	0.78
Electrical conductivity ($x10^5$/Ω-cm)	5.88	6.25	4.17	0.87	0.812
CTE (ppm/°C)	16.4	18.6	14.2	22.2	30.2
Yield strength (psi)	10,000	1,000	250	1,300	3,600
Ultimate tensile strength (psi)	32,000	21,000	17,000	2,000	5,000~7,000
Young's modulus ($x10^6$ psi)	19.2	11.8	11.2	6.89	7.8
Elongation at break (%)	51	50	50	50~80	37
Hardness (Brinell)	37	25	18.5	3.7	14.8

1.4 Techniques for High Temperature Die Attach Materials

In the case of soldering process, the flux mainly react with metal oxides such as CuO and SnO. Once the metal oxides are removed by fluxing actions, the fresh solder and base metals can contact intimately to form solder joints. Simultaneously, flux residues are generated, which are known to cause voids and remain corrosive. It could say that flux residues not only are accompanied, but also lead to degrade the performance of device. Consequently, the use of flux is prohibited for many applications. Even if it is allowed, the assembled parts need to be cleaned to remove all flux residues. The fluxless process, thus, becomes very critical to improve reliability in the advanced electronic packaging.

Table 1.4 Four major steps for oxidation-free fluxless soldering technnique

Step	Process	Approach
1	Solder fabrication	Electroplating or Vacuum deposition
2	A capping layer over solder	Ag or Au
3	Bonding environment	Vacuum or Inert gas or H_2
4	Dealing with capping layer	Dissolution

Our group has developed an oxidation-free fluxless soldering technique to produce high temperature joints at low processing temperature since 1995 [21-23]. There are four major steps necessary to accomplish the fluxless bonding, as show in Table 1.4. First, solder materials should be fabricated in an oxidation-free environment such as vacuum deposition or electroplating method. Second, there should be a thin capping layer, usually Au or Ag layer, on the solder materials to protect inner solders from oxidation when solders are exposed to air. Third, the bonding process should be performed in vacuum, inert gas, or H_2 environment to inhibit oxidation. Finally, during the reflow process, this thin capping layer should become a part of joints and the fresh solders can react with base metals to form IMCs. This technique has been applied to develop various fluxless processes such as on Sn-Au, Sn-Cu, Sn-Ag, Sn-Bi, Sn-In, In-Au, In-Cu, In-Ag binary systems and In-Pb-Au ternary system [22-28]. The results are encouraged. However, this fluxless bonding technique is not feasible to form Ag joints due to its high melting temperature.

Among all possible metallic bonding materials for electronic packaging, Ag is a promising choice in terms of excellent physical, chemical, thermal, electrical, and mechanical properties. However, Ag does not melt until 952 °C. Obviously, taking the advantage of Ag is desirable, but increasing processing temperature is not desirable. To respond to this challenge, our group has successfully developed a solid-state atomic bonding technique to bond Ag to Au,

Ag, and Cu, respectively, at a temperature much lower than its melting point [29-32]. This is a solid-state bonding process without molten phases. No flux is used. The bonding is performed at 300 °C with 1,000 psi (6.9 MPa) pressure in 0.1 torr vacuum for a few minutes. The 300 °C bonding temperature makes Ag deform more easily to conform to the bonding chip's surface profile. The pressure is less than 1/10 of what used in industrial thermo-compression processes [33-36].

The fundamental concept of solid-state atomic bonding refers to the atomic interaction between solid material A and solid material B when A atoms and B atoms are brought within atomic range. On the interface, bonding between materials A and B will occur where A atoms and B atoms can share outer electrons. The ability to share outer electrons mainly depends on the electronic configurations. The bonding theory based on quantum mechanics was recently reported [37].

1.5 Dissertation Outline

This thesis is composed of 9 chapters, including the present one, and their content is concisely presented below:

Chapter 2 briefly reviews the solid-state bonding technology based on its bonding

mechanism and the three major parameters, including temperature, pressure, and time. The bonding can be accomplished within a reasonable time by choosing appropriate temperature and pressure values. The quantum theory of solid-state atomic bonding is further reported.

Chapter 3 is to report the materials, apparatus, fabrication processes, bonding furnace setup, and characterization analysis.

Chapter 4 is to present that a 50 μm Ag layer is used as a bonding medium between two Cu pieces. That is initially annealed at 400 °C for 5 h to increase Ag grain sizes, thereby making it easier to deform during bonding. The solid-state bonding process is performed at 300 °C with 6.89 MPa (1000 psi) static pressure for 3 min. The shear test results of 6 samples all pass MIL-STD-883J method 2019.9.

Chapter 5 is to present a novel method for advanced Cu wire bonding. The 1 mm Cu wires is cut a flat surface and then electroplated a 50 μm Ag layer. The Cu wires bond to Cu and Si chips, respectively. The bonding conditions are at 300 °C with 6.89 MPa (1,000 psi) for 3 min. For wire-bonds made on Cu substrate, in-plane pull test measured a breaking of force 20.7 to 23.7 kg, comparable to the 22.5 kg breaking force of the Cu wire itself. Breaking forces on vertical pull test are about one-half of in-plane pull test results. For wire-bonds made on Si chip, breaking forces are about 80% of those made on Cu substrate.

Chapter 6 is to present that a patterned Ag layer is used as a bonding medium between

two Cu pieces. With this design, the flow distance is not set by the chip size. That is determined by the pattern on the Ag bonding layer. Additionally, the patterned cavities could release the thermal induced stress by creating cavities in the Ag layer to allow easier plastic deformation for the bonding medium. The bonding conditions are the same as the Ag joints without cavities. The shear test results of 5 samples all pass MIL-STD-883J method 2019.9.

Chapter 7 is to present a novel design that Si chips have successfully bonded to Cu substrates directly. The Cu substrates are etched to produce the trench pattern, followed by thin layer of Ag (1 μm) to prevent Cu from oxidation. Si chips are deposited with thin Cr (30nm) and Au (100nm). The Si chip is placed over Cu substrate and bonded at 300°C with 6.89 MPa (1000 psi) for 3 min using the solid-state bonding process in vacuum. The simple shear tests are conducted to evaluate the bond strength, while the Si chips are all broken first.

Chapter 8 is to present that designs and fabrications of Ag-In solid solution layers on Si and SiC chips and subsequent solid-state bonding to Cu substrate. The Ag/In/Ag multilayers are electroplated on the chips. The initial annealing step carried out in between is to increase its grain sizes and to reduce grain boundaries, inasmuch as the reaction rate between Ag and In is subject to the microstructure of Ag layer. A two-step annealing process is followed in a vacuum environment at 180 °C and 350 °C, respectively. The SEM/EDX analysis studies the composition of bonding joints, which displays the single phase Ag-In solid solution. The simple shear tests

are conducted to evaluate the bond strength. After the test, the half Ag-In solid solution joints are still bonded on the Cu substrates. It could say that the bond is strong not weak.

Finally, chapter 9 is given to point out important conclusions in this dissertation.

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Chapter Two

Review of Solid-State Bonding Principle

2.1 Introduction

Solid-state bonding refers to the bonding process at temperatures below the melting temperatures of the bonding materials. No liquid or gaseous state is involved. Examples of vapor-phase bonding are sputtering and chemical vapor deposition processes [1]. Examples of molten-phase bonding are soldering and welding processes. The popular processes for achieving solid-state bonding are thermo-compression and diffusion bonding. Solid-state bonding is carried out at relatively lower temperature compared with molten-phase and vapor-phase bonding, which makes surface roughness difficult to overcome. Accordingly, the bonding between solids may be hard to occur.

The term diffusion bonding is often regarded as solid-state bonding [2]. It may cause confusion with respect to solid-state bonding and thermal-compression bonding. Brief definitions are given in this section. For the bonding mechanism, both diffusion and thermos-compression bonding are affiliated to solid-state bonding. Diffusion bonding requires a considerable amount of time for the atoms to interact with each other, and thus they can achieve the bond. On the

contrary, thermal-compression bonding can be achieved within a short period of time. In this dissertation, we are more interested in using solid-state bonding process to form a robust bond within a few tens of seconds.

2.2 Parameters in solid-state bonding

There are three major parameters of the solid-state bonding, temperature, pressure, and time, which are closely interrelated [3-4]. The role of these parameters is to achieve the intimate contact between the surfaces to be bonded, and thus the interaction can occur. Therefore, the bonding can be accomplished within a reasonable time by choosing appropriate temperature and pressure values. Fig. 2.1 depicts a simple solid-state bonding process. First, two dissimilar metallic surfaces are cleaned and ready to perform the bonding experiment, as shown in Fig. 2.1 (a). Second, both pressure and heat can be applied to create intimate contact between the surfaces to be bonded, as shown in Fig. 2.1 (b). During the creation of intimate contact, metals may undergo plastic deformation to conform the surface roughness. Next, the interaction can be activated. Finally, the bond is achieved, as shown in Fig. 2.1 (c). Ideally, no voids and gaps can be observed.

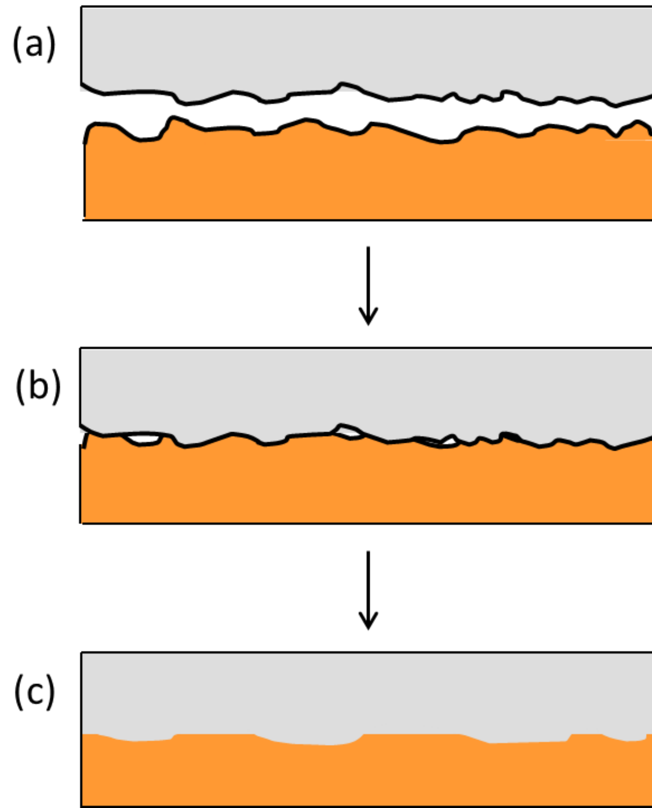

Fig. 2.1 A simple solid-state bonding process (a) Two dissimilar metal surfaces are ready for the bonding experiment, (b) The intimate contact is created, and (c) The bond is achieved

An important purpose of this dissertation is to determine the solid-state bonding conditions that can be applied to various metal combinations. One way to increase the percentage of bonding is to increase the pressure, which can greatly reduce the influence of surface roughness. But any pressure higher than 1,000 psi is not acceptable in our applications. The concern is that such high pressure may damage the chips to be bonded. On the other hand, high temperatures can provide a high rate of interaction, however, which may also result in the high defect densities on the chips. Our objective is looking for other ways to improve the bonding

strength without increasing the pressure or the temperature. Some novel designs are reported in the following chapters.

2.3 The Quantum Theory of Solid-state Atomic Bonding

Numerous experiments have been performed to show the possibility to achieve a robust bond using solid-state bonding process [5]. Neither principle nor theory at the atomic level has been reported. How is solid-state bonding possible?

Fundamentally, it is possible only if materials A and B can be brought within atomic distance. Over the past few years, we have proposed the solid-state atomic bonding principle as follows: "As A atoms and B atoms are brought within atomic distance, there is the interaction between them. On the atomic interface, if A atoms and B atoms can share outer electrons, bonding between materials A and B will occur. The ability of materials A and B to share outer electrons depends on their electronic configurations. Diffusion of A and B atoms alone does not guarantee bonding if A and B atoms do not want to share electrons. A and B atoms may share electrons to form A_xB_y compound. The A_xB_y compound may or may not bond with A or B atoms, depending on whether they are willing to share electrons." Our experimental bonding results have indicated that this bonding principle is correct [6-8]. At present, the ability to share

electrons is determined by the experimental data. The broader questions are: "how do we determine whether A atoms and B atoms would share electrons and how closely they require to be brought together to achieve bonding?" We searched the literature and could not find any publications in this subject. The fundamental mechanism and principle of solid-state bonding were seldom reported.

The solid-state bonding theory based on quantum mechanics was recently reported by our group [1]. Metal atoms such as Cu, Ag, and Au do form diatomic molecules in vapor state: Cu_2, Ag_2, Au_2, CuAg, AgAu, and CuAu [9-11]. Their binding energy, equilibrium separation, and vibrational frequency have been measured and presented [12-7]. The three parameters are used to construct the Morse potential energy versus atomic separation curves for all these molecules. Additionally, the breaking strength of the bonding interface is obtained by multiply the binding force and the number of atoms per area. Consequently, we could compute the bonding strength as a function of atomic separation on the interface. In the bonding experiment, the atomic separation on the interface is controlled by bonding and surface conditions rather than equilibrium value. Therefore, the purpose of our bonding theory is to estimate how close the interface atoms have to be brought to achieve adequate bonding strength approximately.

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Chapter Three

Experimental Setup and Techniques

3.1 Materials Fabrication

The die attach layer is the joint between die and substrate in electronic packaging. In order to create this layer, the following fabrication methods and apparatus are used to conduct experiments. These include wafer cleaning procedures, electron beam evaporation, electroplating, photolithography, etching processes. Prior to designing the experiment steps, one must choose the suitable materials for specialized applications. Table 3.1 shows a list of materials and its applications used in this study.

Table 3.1 Materials and its applications

Applications	Materials
Metallization	Chromium (Cr), Gold (Au)
Electroplating	Silver (Ag), Indium (In)
Bonding Wire	Copper (Cu)
Bonding Chip	Copper (Cu), Silicon (Si), Silicon Carbide (SiC)
Bonding Substrate	Copper (Cu)

3.1.1 Wafer Cleaning Procedures

Silicon wafers are cleaned by a solvent clean, RCA-1 clean, and hydrofluoric acid (HF) dip. This process takes one hour to complete in total [1].

Solvent clean is used to remove oils and organic residues from Si wafers. Unfortunately, solvents themselves (especially acetone) leave their own residues. This is the reason that a two-solvent method is adopted. Pour the acetone into a glass container and the methanol into a separate container. Place the acetone container on a hotplate to warm up (do not exceed 55 °C). Next, place the wafer in the warm acetone bath for 10 min. After that, place the wafer in methanol for 2-5 min. Rinse in deionized (DI) water and blow dry with nitrogen.

RCA-1 clean is used to remove organic residues from Si wafers. In the process, it oxidizes the Si and leaves a thin oxide on the surface of the wafer, which should be removed if a pure Si wafer is desired. RCA-1 cleaner is composed of 5 parts DI water, 1 part 27 % ammonium hydroxide (NH_4OH), and 1 part 30 % hydrogen peroxide (H_2O_2). Pour 325 ml DI water in a Pyrex beaker. Add 65 ml NH_4OH and then heat to 70 °C on the hotplate. Remove the beaker from the hot plate, Add 65 ml H_2O_2. The solution should bubble vigorously to indicate that it is ready to use. Soak the Si water into the solution for 15 min. Rinse in running DI water for 3 to 5 min and blow dry with nitrogen.

HF is used to remove native silicon dioxide from Si wafers. Due to the fast chemical reaction, one needs to expose the wafer to HF for a short period of time. The HF cleaner is composed of 24 parts DI water and 1 part 49 % HF. Pour 480 ml DI water into a polypropylene beaker and then add 20 ml HF. Never use a glass beaker with HF for the reason that HF attacks glass. Soak the wafer for 2 min in this solution. Remove the wafer and rinse in running DI water. Blow dry with nitrogen and store in a clean dry environment. Importantly, one can pour a little DI water on the surface of the wafer to verify hydrophobicity by performing the wetting test. The hydrophobic surface is water repellent. On the contrary, the hydrophilic surface is easily wetted [2]. Since oxide is hydrophilic and pure Si is hydrophobic, a non-wetting surface should be observed.

3.1.2 Electron Beam Evaporation

Electron beam (e-beam) evaporation is a form of physical vapor deposition (PVD), which is used to deposit layers of atoms from the vapor phase onto a solid substrate in a high vacuum chamber. As shown in Fig. 3.1, the equipment, Temescal CV-8, is a four-pocket e-beam evaporator used for depositing metals, such as Au, Ti, Ni, Cr, Si, Ge, and Pt [3]. The wafers are loaded on a stationary planetary substrate holder. The system will pump down to the base

pressure of 2×10^{-6} Torr using a cryo-pump. In the e-beam evaporation system, a target anode is bombarded with an electron beam which is generated from a charged tungsten filament [4-6]. The electron beam is accelerated to a high kinetic energy toward the target material directly. The electron beam with high energy then results in atoms from the target to transform into the vapor phase. The resulting vapor is able to evaporate freely and then condense on all surfaces inside the chamber. The entire process takes place inside of a vacuum chamber which is first evacuated to high vacuum. This system allows deposition of up to four different materials in one duty cycle. The thickness monitor is assembled inside the chamber and the metal deposition thickness is measured in real-time.

Fig. 3.1 Temescal CHA-600S/CV-8 (UC-Irvine INRF)

3.1.3 Electroplating

Electroplating is a relatively easy and inexpensive way of depositing thin and thick films on conductive substrates, which immersed in an electrolytic bath composed of a solution of the salt of the metal to be plated. The deposition rate is simply controlled by adjusting current [7]. Both oxidation and reduction reaction are involved in the plating process. At the anode, the metal to be plated is oxidized, which allows the metal atoms to dissolve in the plating solution. At the cathode, the dissolved metal ions in the plating solution are reduced onto the substrate surface.

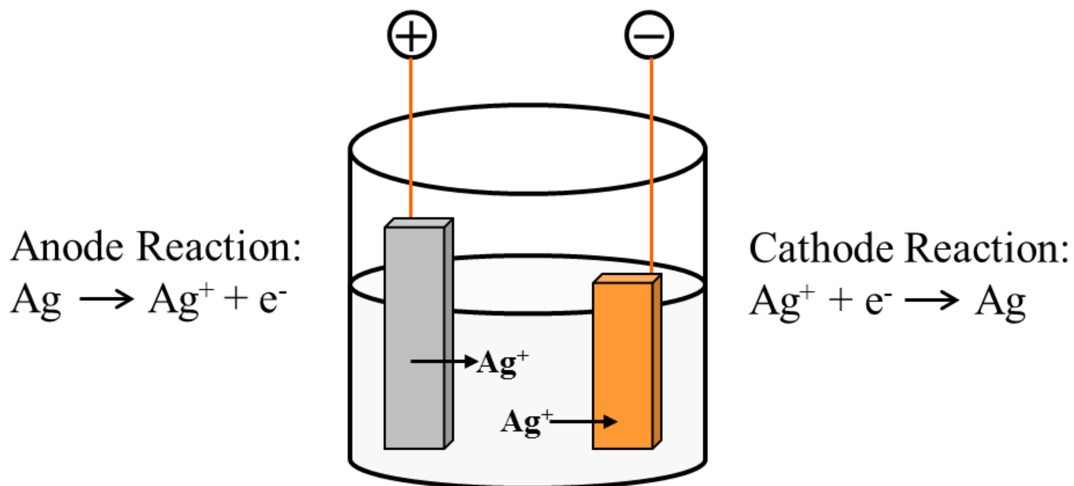

Fig. 3.2 Silver electroplating: Anode is a Ag plate. Cathode is a Cu substrate

In this study, the deposition is driven by external direct electric (DC) current. The anode is made of the metal to be plated, and the cathode connects to the substrate. Take silver (Ag) electroplating as an example. At the anode, Ag atoms are dissolved by $Ag \rightarrow Ag^{+} + e^{-}$, and the reduction reaction at the cathode is $Ag^{+} + e^{-} \rightarrow Ag$, as show in Fig. 3.2. The Ag ions, thus, are plated onto the substrate surface.

3.1.4 Photolithography

Photolithography is the process of transferring geometric pattern on a mask to the surface of a silicon wafer. Fig. 3.1.3 is a typical example of photolithographic processing steps.

In this study, all patterns are generated by using positive photoresist, AZ4620 [8]. Prior to coating with photoresist, the Si wafer is heated to 120 °C for 5 min to remove water residue. Drops of photoresist AZ4620 are dispensed on the Si wafer, which is spun on Laurell spinner to coat a uniform photoresist layer. It is followed by the soft baking, which is applied to remove some of the photoresist solvent and densify it. After the soft baking, the wafer is placed below a glass photomask and exposed with UV light of a Karl Suss MA6 Mask Aligner to define the pattern, as show in Fig. 3.4. The wafer is then developed using diluted AZ4620 developer. After rinsing and drying, the hard baking is used to drive off the remaining solvent from photoresist

and improve the adhesion of photoresist to the wafer surface. Next, etching step is performed to remove the undesired area. Last, the photoresist can be removed by stripper.

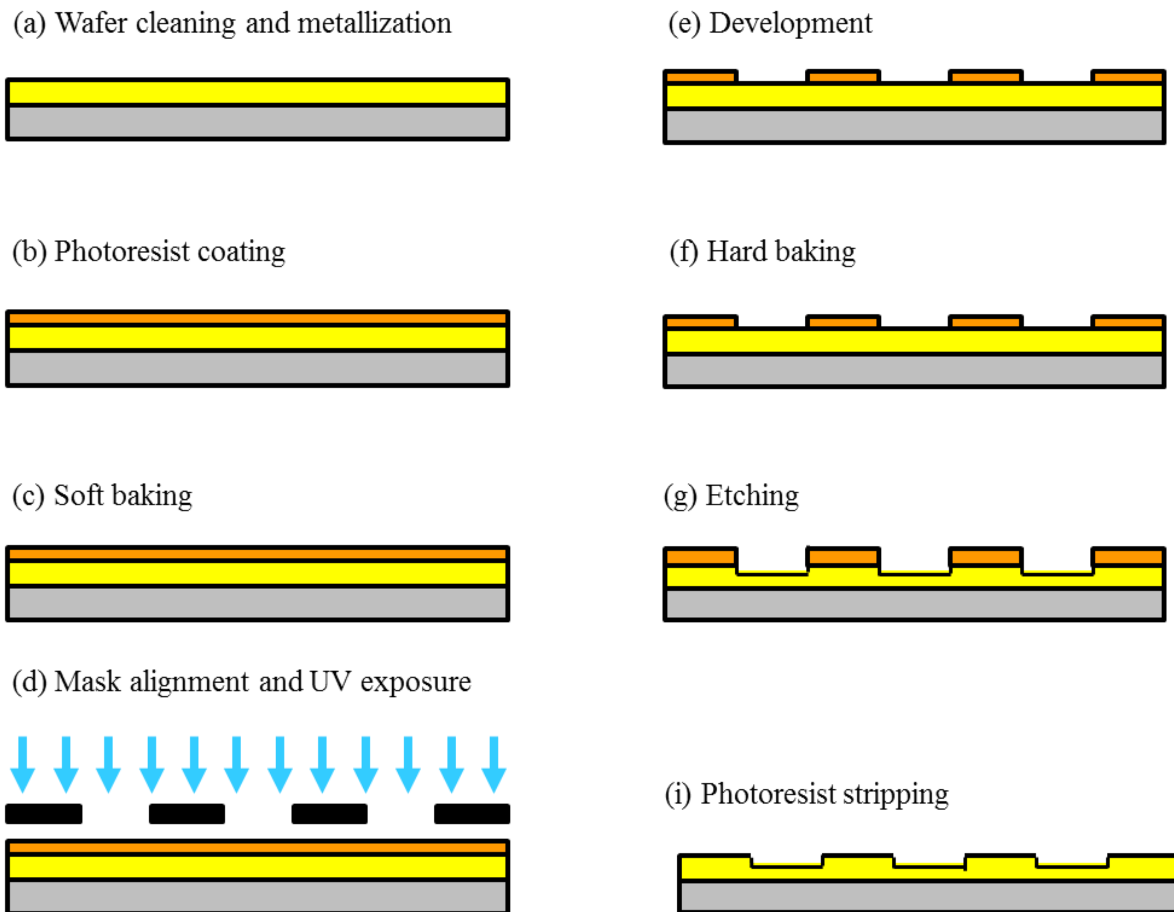

Fig. 3.3 An example of a typical sequence of lithographic processing steps (a) Wafer cleaning and metallization, (b) Photoresist coating, (c) Soft baking, (d) Mask alignment and UV exposure, (e) Development, (f)Hard baking, (g) Etching, and (i) Photoresist stripping

Fig. 3.4 Karl Suss MA6 Mask Aligner (UC-Irvine INRF)

3.1.5 Etching

The etching process is to remove materials from undesired areas identified by photolithography in the semiconductor fabrication. Take Cu etching as an example. In this study, this process etches copper by using ferric chloride ($FeCl_3$) solution, MG Chemicals 415 Ferric Chloride Liquid. The photolithography is also used to develop the designed pattern. Importantly, the etching rate of the $FeCl_3$ mainly changes along with the processing temperature (do not exceed 55 °C). The chemical reaction of Cu in $FeCl_3$ etchant is listed as follows [9]:

$$FeCl_3 + Cu \rightarrow FeCl_2 + CuCl \quad (3\text{-}1)$$

$$FeCl_3 + CuCl \rightarrow FeCl_2 + CuCl_2 \quad (3\text{-}2)$$

$$CuCl_2 + Cu \rightarrow 2CuCl \tag{3-3}$$

The Cu surface is first oxidized by ferric ions to form ferrous chloride ($FeCl_2$) and cuprous chloride (CuCl). Next, CuCl gets oxidized in $FeCl_3$ etchant to produce cupric chloride ($CuCl_2$) while CuCl is formed. Last, the $CuCl_2$ also reacts with the Cu surface to form CuCl. In fact, the Cu surface is chemically etched with $FeCl_3$ and $CuCl_2$.

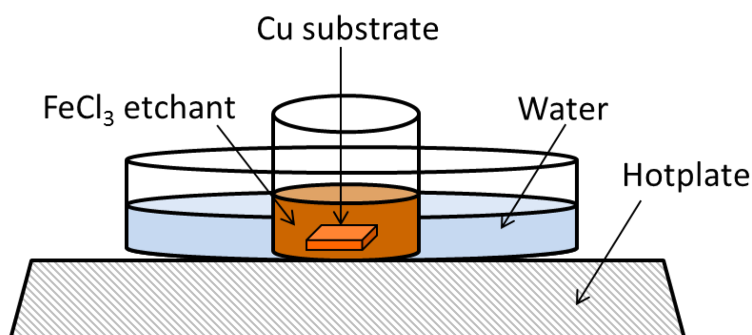

Fig. 3.5 Warm up the $FeCl_3$ etchant in the hot water bath

Prepare the etching solution in the following manner. Pour 100 ml $FeCl_3$ solution into a dry glass beaker (do not mix with water). As shown in Fig. 3.5, place the beaker in the hot water bath heated by a stirrer hotplate. Soak the Cu substrate into the solution with mild agitation. The soaking time depends on the desired depth of etch. Finally, rinse in running DI water for 3 min and blow dry with nitrogen. The depth of etch is examined and the etching rate of Cu in $FeCl_3$ etchant is 6 μm/min at 50 °C ± 2 °C approximately.

3.2 Vacuum Furnace and Bonding Setup

Fig. 3.6 depicts a compact vacuum furnace designed by our group [10]. In this study, all of bonding processes are performed in this vacuum furnace. The vacuum furnace consists of a quartz cylinder, two stainless steel plates, a heating platform, and a ceramic post. The quartz cylinder, having the inner diameter of 130 mm and height of 200 mm, is sandwiched between two steel plates to construct a vacuum chamber. The interference between the cylinder and the steel plate is sealed by an O-ring. The transparent quartz is chosen since it is easy for users to observe the sample during the bonding process. Inside the vacuum furnace, a graphite platform is supported by a ceramic poster standing at the center of the base stainless steel plate. The graphite platform, having the size of $75\times75\times10$ mm^3, is drilled with many holes to allow the heating wire (Nickel-Chromium alloy) going through the body of the block. The wire is electrically insulated from the graphite using ceramic tubes. Graphite is selected as the material of the platform because it has been experimentally proven that it absorbs 97% of radiation and is a nearly perfect emitter of radiation [11]. Therefore, the platform can absorb a maximum amount of heat given off by the wires. It is also easy to machine and can withstand very high temperature. The temperature is monitored by two type-K thermocouples (Chromel+ Alumel-) at two locations, the top surface of sample and the sidewall of platform.

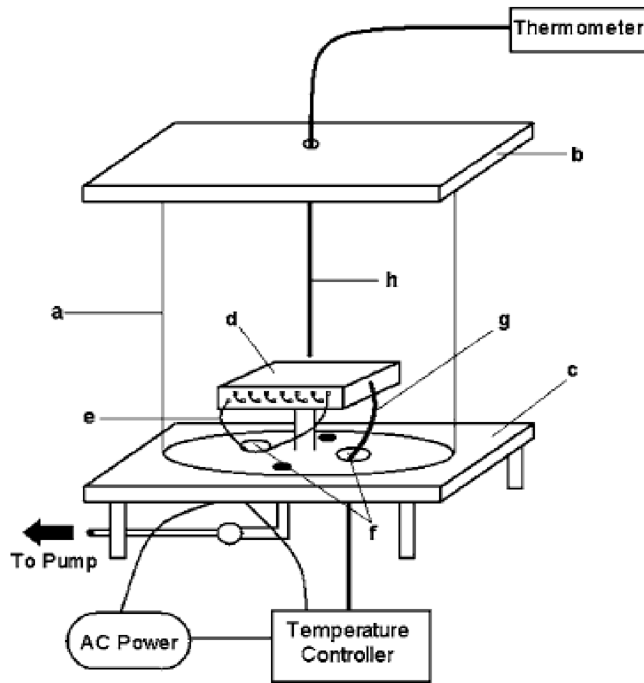

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Fig. 3.6 Schematic of the vacuum furnace showing key components: (a) quartz cylinder, (b) upper stainless plate, (c) base plate, (d) graphite platform, (e) heating wire, (f) electrical feedthroughs, (g) platform thermocouple, and (h) sample thermocouple

To achieve thermal isolation of the platform from the upper and base plates, a ceramic poster is utilized to support the platform due to its relatively low thermal conductivity. The ceramic beads have the same advantage for the hearing wire inside the holes of the graphite platform. Once the chamber is in a vacuum environment, heat transfers to the upper and base plates from the platform through radiation mechanism only. O-rings are used to seal the chamber to keep it in vacuum. Since the plates are constructed of stainless steel, being able to reflect and scatter radiation, the plates will not absorb much heat radiation and can keep cooled to low

temperature with natural convection by ambient air. It is designed so that the platform is well thermally isolated from the chamber enclosure that includes the cylinder wall and two steel plates. This is a unique feature of the furnace design. It allows for the platform to be heated to high temperatures while the temperature of the rest of the chamber remains relatively low, which is important to users regarding the safety. The upper plate is mounted with an ultra-Torr connector to take the small K-type thermocouple probe for measuring the sample temperature. The base plate contains four ports with National Pipe Thread (NPT). Two of these are occupied by feedthroughs. One feedthrough is for a pair of copper wires to pass into the chamber to connect to the two ends of the heating wire. The other is for thermocouple wires. The third port is used for the vacuum gauge, and the fourth port is for connecting to a mechanical pump. In this design, the chamber is allowed to pump down to 50 millitorrs and the maximum temperature of platform reaches up to 450 ºC.

To conduct the bonding experiment in the vacuum chamber, the samples are mounted in a graphite fixture and applied with a static pressure to ensure intimate contact. The assembly is then placed on the graphite platform. Once the vacuum furnace is pumped down and kept at 50 to 100 millitorrs to suppress oxidation during the bonding process, the temperature controller is turned on to heat up the platform. The bonding process is carried out at wide ranges of temperature and dwell time for different bonding systems. After reaching the peak temperature,

the heater is turned off and the assembly is allowed to cool down naturally to room temperature in a vacuum environment. Take the soldering process as an example. Compared to the soldering bonding in air, the amount of oxygen available to oxidize the molten solder is reduced by a factor of 15,200 in 50 millitorrs of vacuum.

3.3 Characterization Techniques

In this section, some characterization techniques are presented. These are used to study the microscopic structures and properties of materials. In this study, all samples are sent to an outside company, Nordson Dage, to perform the shear tests. Therefore, the technique of shearing test is not displayed.

3.3.1 X-Ray Diffraction (XRD)

The Rigaku SmartLab is the state of the art in highly automated, fully modular, multipurpose X-ray diffractometer, as show in Fig. 3.7 [12]. The most novel feature of Smartlab is the control software, called "Smartlab Guidance." It can provide an intelligent interface to guide users to select optimal hardware configurations and provides fully automated optics alignment, sample alignment, slit and scan condition settings, and measurements, which helps to

minimize the time-to-results for all users. Measurement packages are available for nearly any conceivable X-ray scattering experiment, including powder materials, thin films, small-angle X-ray scattering (SAXS), and micro-diffraction.

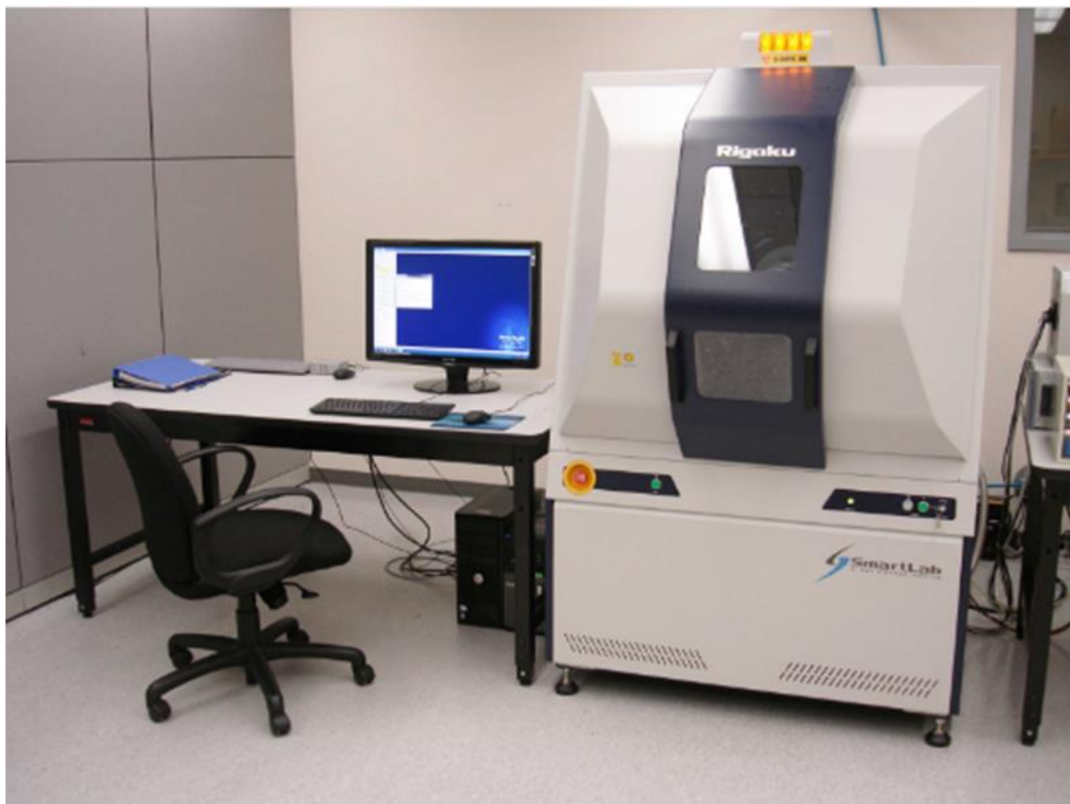

Fig. 3.7 Rigaku SmartLab X-ray Diffractomete (UC-Irvine Calit2)

X-ray diffraction is a method used for identifying the molecular structure of a crystalline material by measuring the diffracted X-rays. Based on XRD diffraction data analysis, one can obtain useful information, such as the lattice parameters, strain, average grain size, phase composition, preferred orientation, crystallinity, and crystal defect.

X-rays are generated by a cathode ray tube which produces electrons toward a target by applying a voltage. The specific wavelengths are characteristic of the target material (Cu, Fe, Mo, Cr). Characteristic X-ray spectra are filtered to produce monochromatic beam of X-rays needed for diffraction. These X-rays are then collimated and focused towards to the sample directly. The atoms should be arranged in a periodic array in a crystal and thus can diffract light. The constructive interference happens when the interaction of incident rays and lattice planes satisfy Bragg's Law, $n\lambda = 2d\sin\theta$, where λ is the wavelength of electromagnetic radiation, d is the lattice spacing in the crystalline sample, and θ is the diffraction angle. The diffraction peak intensities are determined by the atomic arrangement within the lattice planes. These diffracted X-rays are then detected, processed and counted. Therefore, the X-ray diffraction pattern is the fingerprint of periodic atomic arrangements of a sample. By scanning the sample through a range of 2θ angles, all possible diffraction directions of the lattice can be attained. In this study, the XRD method was applied to different materials and their results are presented as a plot of diffraction intensity corresponding to diffraction angles.

3.3.2 Scanning Electron Microscope (SEM)/Energy Dispersive X-ray Spectroscopy (EDX)

In this study, Philips XL-30 FEG SEM with EDX system is used, as shown in Fig. 3.8 [13]. It is a thermionic field emission SEM which is fully automatic gun configuration controlled by advanced computer technology. The magnification is up to 800,000 times with 2 nm resolution. It is easy to use for examining and survey the morphology of the nano-devices. This XL30 also equipped with EDX detector to provide the composition information.

Fig. 3.8 Philips XL-30 FEG SEM with EDX system (UC-Irvine LEXI)

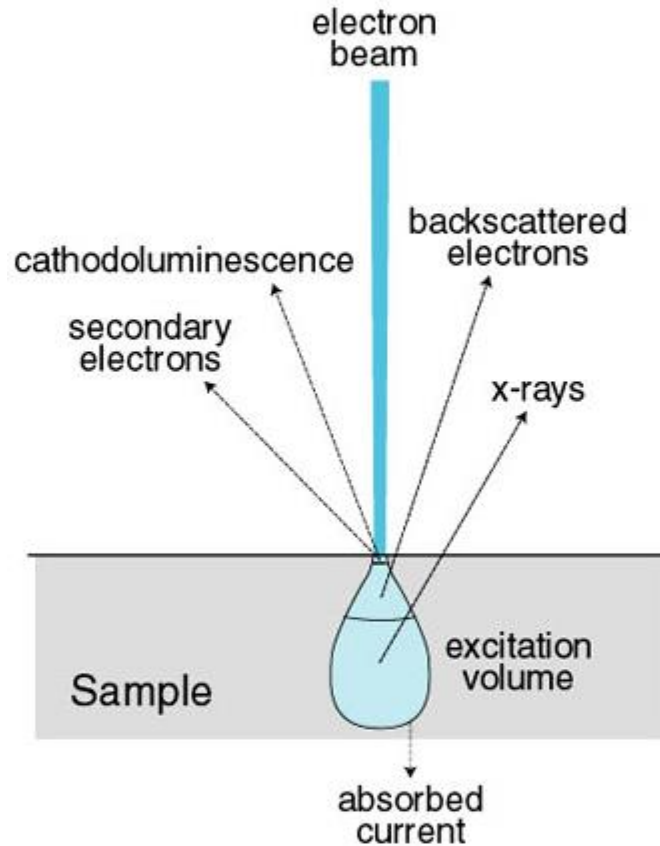

Fig. 3.9 The interaction volume and the signals produced by the interaction between the electron beam and specimen (Electron Microscope Laboratory, Northern Arizona University)

SEM is a type of electron microscope that equips a focused beam of high energy electrons to image specimens by scanning it. The high energy electrons interact with the atoms that make up the specimen to produce various signals from the surface of the specimens. These signals, which mainly includes secondary electrons (SE), back-scattered electrons (BSE), electrons backscatter diffraction (EBSD), characteristic X-rays, visible light (cathodoluminescence), , reveal the specimens' surface topographies, chemical compositions,

and crystalline structures. Fig. 3.9 displays the interaction volume and the signals, depending upon many factors, produced by the interaction between electron beam and specimens [14].

Due to the very narrow electron beam, SEM micrographs have a large depth of field, yielding a three-dimensional surface image of a specimen. SE and BSE detectors installed in the SEM are common used to image specimens. SE is most valuable for showing high-resolution morphologies and topographies on specimens. On the other hand, BSE is most valuable for displaying contrasts in the composition of multiphase specimens. For instance, a stronger BSE intensity is detected if a larger number of backscattered electrons reaching to a BSE detector. Larger atoms, with a greater Z-number, have a higher probability of producing elastic collisions. Thus, elements with a greater atomic number (Z) show brighter images than smaller atomic number in BSE images.

X-ray is also produced during the interaction of an electron beam with a specimen. The energy-dispersive X-ray Spectroscopy (EDX) detector is used to separate the characteristic X-rays of different elements into an energy spectrum. The EDX software system can analyze the energy spectrum for determining the specific elements in the specimen. Additionally, EDX can further find the chemical composition of materials in small area (~10^{-6} mm^2), and can create element composition mappings over this area.

3.3.3 Dektak 3 Surface Profilometer

The purpose of the Dektak is to give an engineer a quantifiable measurement of the surface profile of a wafer, as shown in Fig. 3.10 [15]. This can be used to measure the height or width of a feature of the wafer surface, such as an etching depth, a metal deposition, or resist thickness. The profile can also give the engineer a look at the roughness of the surface of a wafer.

Fig. 3.10 Dektak 3 Surface Profilometer (UC-Irvine INRF)

The profilometer operates by lightly dragging a sharp stylus over the surface of the substrate and recording the vertical profile of the surface. The radius of diamond stylus is 12.5

microns, and the horizontal resolution is controlled by the scan speed and scan length. The display range of the data is 200 Å to 655,000 Å (65.5 um) with a vertical resolution of ~ 5 Å. A video camera with variable magnification allows for manual placement of the stylus and the system is programmed for scan length and speed.

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Chapter Four

Strength of solid-state silver bonding between copper Structures

4.1 Introduction

Among all possible metallic bonding media for electronic packages, silver (Ag) is an obvious choice in terms of physical properties as Ag has the highest electrical conductivity and highest thermal conductivity. However, Ag does not melt until 952 ºC. To respond to this challenge, we have developed a solid-state atomic bonding technique to bond Ag to Au, Ag, and Cu, respectively at low bonding temperature and pressure [1-4].

It is well known that the bonding technology of different metals is an indispensable and primary one in the industrial fields. The solid-state process has been studied for years because of its great applications. A concern from industries is the strength of the bonding interface and the contact layer. We designed and set up an experiment to measure the bonding strength to respond to this question. In this paper, the Cu chip and substrate are held and pressed together with 1000 psi static pressure. It is worth noting that this pressure is less than one-tenth of the pressure used in conventional thermo-compression bonding [5-6]. The bonding process is performed at 300 ºC for 3 min. This 3 min time is constrained by our furnace. In theory, it should take seconds rather

than minutes for solid–state bonding to occur. This is a solid-state bonding process without any molten phase involved [7]. All samples pass the MIL-STD-883G standard, which proves that the bonding strength is robust. In what follows, we first present the experimental design and procedures. Experimental results are then reported and discussed. Finally, a short summary is given.

4.2 Experimental Design and Procedures

Our basic principle of solid-state bonding is to form a strong metallic bonding between metal A and metal B. Metal A and metal B are held and pressed together with 1000 psi (6.9 MPa) static pressure to bring atoms A to atoms B within the atomic distance. When the atomic spacing between atoms A and atoms B is brought within an atomic distance, they share electrons and bonding occurs. The study provides important information to the strength of the Cu/Ag/Cu structures produced by the solid-state bonding process.

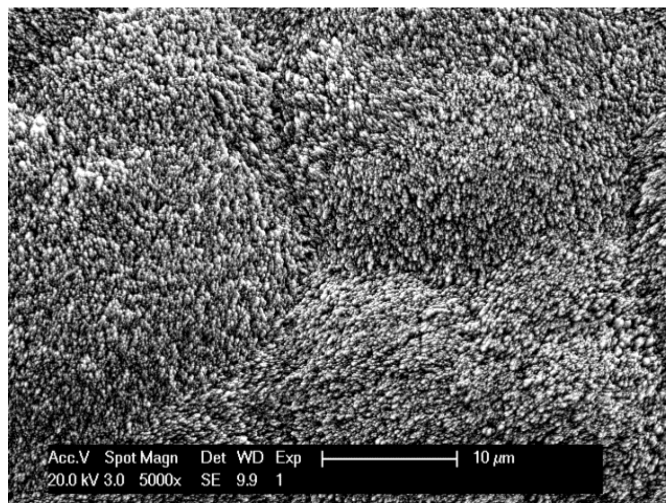
In experiments, Cu chips of 12 mm × 12 mm and Cu substrates of 8 mm × 10 mm are cut from a 0.8 mm thick Cu sheet. Both Cu chips and substrates are slightly polished to remove oxide from substances. Ag layer is coated on the Cu substrate by electroplating process at room temperature. The electroplating solution contains 5-8 % potassium hydroxide and 2-3 % silver

oxide. Annealing of the Cu substrates before bonding is at 400 ºC for 5 h. The assembly of the solid-state bonding is to set samples on the heating graphite platform under the vacuum atmosphere that is kept at 0.1 Torr to restrain oxidations. The Cu chip is bonded to the Cu substrate at a static pressure of 1000 psi and then heated to 300 ºC with a dwell time of 3 min. The bonding pressure is controlled by the spring-loaded mechanism. During the pressing process, the silicon rubber is placed between the sample and the fixture to facilitate the uniformity of plastic deformation. The vacuum chamber cools down naturally to room temperature when the bonding process is completed. The bonded sample is mounted in epoxy resin, cut into halves, and polished for cross-sectional examination. Scanning electron microscopy (SEM) is used to examine the quality of Ag joints, the Cu-Ag interfaces, and the microstructure. The strength of the bonding interface is measured by a standard shear test.

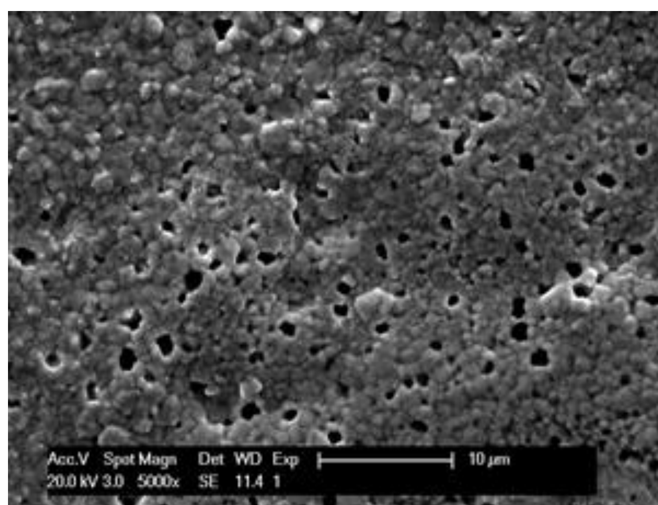
4.3 Experimental Results and Discussion

Ag grain sizes vary widely under different annealing conditions [8]. According to previous results, annealing temperature of 400 ºC is chosen because of the Ag grain size. Fig. 4.1 shows the Ag surface morphologies on Cu substrates observed by SEM (a) non-annealed Ag and (b) annealed Ag microstructures at 400 ºC for 5 h. As shown in Fig. 4.1(a), the Ag surface is

smooth with small grain sizes. As shown in Fig. 4.1(b), the Ag grains are accumulated and have grown from nanometer to micrometer-sized particle.

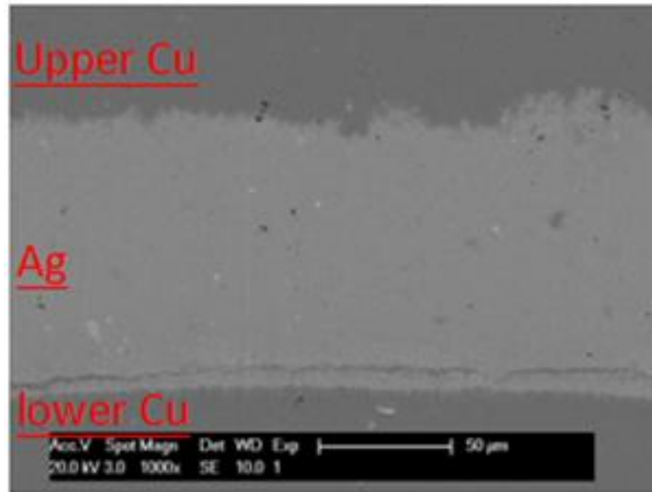


(a)

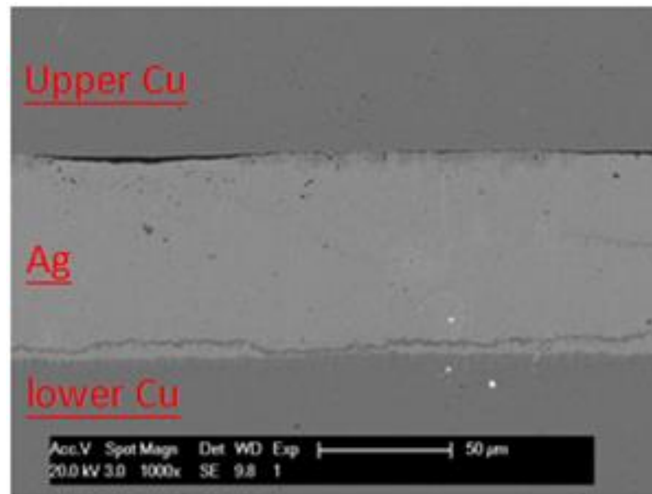


(b)

Fig. 4.1 SEM images of Ag surface morphologies on Cu substrates (a) non-annealed Ag microstructures and (b) annealed Ag microstructures at 400 ºC for 5 h



(a)



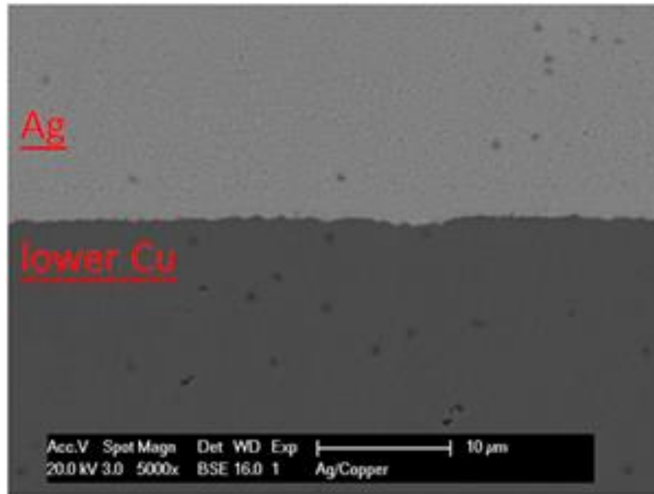
(b)

Fig. 4.2 Cross-sectional SEM images of the bonded sample at 250 ºC with static pressure 1000 psi (a) Cu/Ag/Cu structures and (b) Cu/Ag/Cu structures include gaps and voids

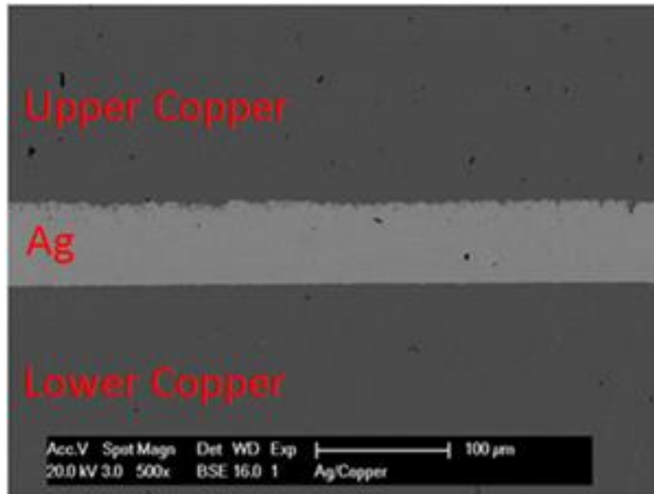
The bonded sample is mounted in epoxy resin, cut into halves and then polished for the bonding interface examination. SEM cross-sectional images are taken to observe the cross-

sectional structures. At first the Cu substrate was electroplated 80 μm Ag layer and then bonded the sample at 250 ºC with static pressure 1000 psi. Fig. 4.2 shows that the major portion of the upper Cu/Ag interface was bonded well. There are no voids or gaps in Fig. 4.2(a), however, the Cu/Ag/Cu bonded structures with voids and gaps are observed in Fig. 4.2(b). How to reduce the defects at the bonding interface is important in this project. To increase the bonding temperature is an effective way.

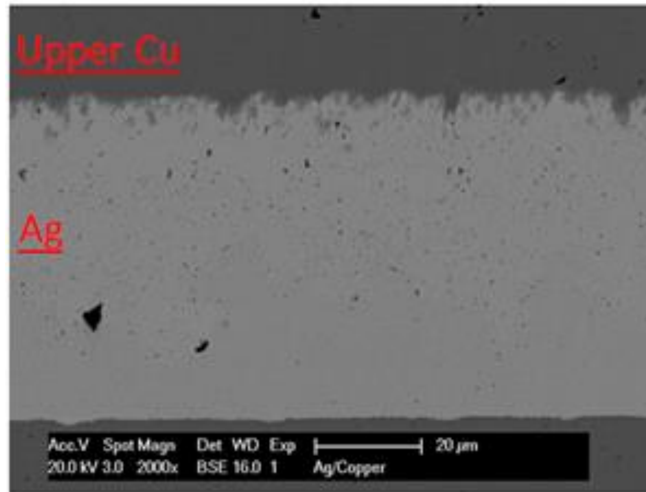
After many trials, the bonding process was determined to conduct at 300 ºC with static pressure 1000 psi. The thickness of Ag layer is 50 μm approximately. As shown in Fig. 4.3, the Ag layer was deformed and then conformed to create the intimate contact with the Cu chip to be bonded. Fig. 4.3(a) presents the sample at the Ag/Cu interface and the Ag layer was well electroplated to the Cu substrate. Fig. 4.3(b) displays the Cu/Ag/Cu bonded structure without any voids or gaps. Fig. 4.3(c) demonstrates Cu/Ag portion was bonded tightly. It explains why this structure can sustain a large break force.



(a)



(b)



(c)

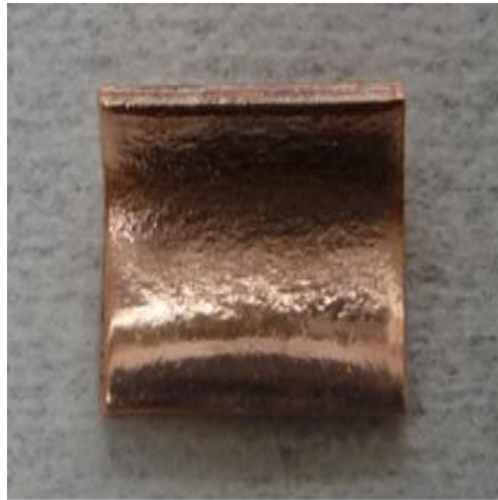
Fig. 4.3 Cross-sectional SEM images of the bonded sample at 300 ºC with static pressure 1000 psi (a) Ag/Cu structure, (b) Cu/Ag/Cu structure and (c) Cu/Ag structure

To obtain the shear strength of the bonding joints, a standard shear test is performed on six bonded samples. Before the test, the Cu substrate is fixed on the stage. Next, a tool wedge with a constant speed of 300 μm/s is applied to the Ag joints and Cu ship once a right angle is established. The breaking forces of the samples are presented in Table 4.1, ranging from 16.87 to 90.16 kg, and all of them are greater than 5 kg, It demonstrates that all samples pass the MIL-STD-883G standard by the size of the bonding area, 0.124 in^2. Fig. 4.4(a) and 4.4(b) are the Cu chip and the Cu substrate of sample 6 after the die shear test. As shown in Fig. 4.4(b), it is seen that the Cu chip bends greatly. Significantly, the bonding structure is strong.

Table 4.1 The shear test results of six samples

Samples	Breaking force (kg)
1	81.59
2	50.24
3	44.88
4	50.91
5	16.87
6	90.16

(a)



(b)

Fig. 4.4 The Cu chip and the Cu substrate after the shear test. (a) The Cu ship and the Cu substrate of bonded sample 6 after the shear test and (b) The Cu chip of bonded sample 6 after the shear test. The tool wedge bent the Cu chip and the breaking force is 90.16 kg. It shows the bonding structure is strong

4.4 Summary

Ag is a favorite choice of bonding media due to its highest electrical conductivity and highest thermal conductivity. Ag is preferred to be bonded to Cu because of its inherent ductility, which is capable to manage the CTE mismatch. From SEM images, it demonstrates that the Cu chip is well bonded to Ag layer on the Cu substrate as the Ag layer deforms perfectly during the bonding process. The whole bonding process is performed at 300 ºC with 1000 psi static pressure. It is a low temperature low pressure solid-state bonding process without any molten phase involved. As a result, the six samples all pass the MIL-STD-883G standard. Passing this criterion eliminates a concern from industries regarding its bonding strength. Therefore, this simple method should have a chance to be used widely in industrial fields.

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Chapter Five

Silver-Assisted Copper Wire Bonding Using Solid-State Processes

5.1 Introduction

In the electronic industry, wire bonding is still the most popular interconnect method even though tape automated bonding (TAB) and flip-chip technology have gained application moment [1-2]. At present, wire bonding is used in 75% of discrete and integrated circuit (IC) devices due to its technology maturity, established equipment, flexibility, and reliability [3-5]. There are three basic wire bonding techniques: thermo-compression, ultrasonic, and thermo-sonic [6-8]. Popular wire materials have been aluminum (Al) and gold (Au) [9-10]. Since Au is expensive and Al is not strong enough, copper (Cu) wire has recently been adapted. A major challenge for Cu wire is oxidation, making it difficult to bond to interconnect pads [11-13]. A great deal of research has been conducted to deal with Cu oxidation by coating Cu wires with noble metal such as palladium (Pd), Au, and Ag [14-15]. The coating metals except Pd could cause problematic ball shapes, for example, a spearhead-like ball shape or a center-deviated ball shape [16]. Pd-coated Cu wires also pose challenges. Cu can form hard alloys with Pd that damages the bond pad. During the free-air ball forming process, Pd would dissolve into Cu

instead of staying on the ball surface. During aging, Pd tends to diffuse and segregate to the bonding interface, which appears to degrade the bond strength [17-18]. It seems that Cu wire bonding technique is still in the developing stage.

This research is focused on developing processes to bond large Cu wires to silicon (Si) chips and Cu substrates using solid-state bonding principle [19]. Some preliminary results were recently presented and published [20]. In this paper, complete and thorough evaluations, data, and results are reported. In recent development of automobile power modules, large wires are needed to carry high electrical current [21]. Furthermore, the advances of high power and high temperature AlGaN and SiC semiconductor devices and resulting electronic modules have opened up the need of strong wire-bonds that can sustain high temperature. So far, high temperature molding compounds are still not available to reinforce the wire bonds and protect them against environment. Thus, in the foreseeable future, the wire-bonds probably have to stand alone without protection. In experiments, 1 mm diameter Cu wires are chosen for demonstration. Bare Cu wires have been used in nearly everywhere for centuries with high long-term reliability. Bare Cu wires can be protected further by plating with a layer of metals such as nickel (Ni) as needed. Among various bonding methods, the one that gives the wire-bond the highest melting temperature was chosen. That is to bond Cu wires directly to Si or Cu substrates without using any bonding medium. This is not an easy task because Cu oxidizes easily. To overcome this

issue, a layer of Ag is plated over the bonding surface of Cu wires. Ball forming process used in the wire bonding processes in industries was not used. Ag has the highest electrical conductivity among metals. It is also ductile and can be bonded more easily using the solid-state bonding principle. The only compromise is the reduction of melting temperature from that of Cu, 1,085 °C, to the eutectic temperature of the Cu-Ag binary system, 780 °C.

In what follows, the experimental designs and procedures are first presented. Experimental results are then reported and discussed. In this study, the solid-state bonding process requires only a single stage operation at 300 °C with 6.89 MPa (1000 psi) pressure for 3 min. According to the cross-sectional studies, the bonding results are nearly perfect. No voids and cracks are observed on the bonding interface. The breaking force of the wire-bonds is evaluated by pull tests [22]. As a result, the wire-bonds are strong enough to be used as they are without protection. At the end of the paper, a short summary is given.

5.2 Experimental Design and Procedures

To achieve maximum wire bond strength using solid-state bonding, the bonding surface must conform to the substrate to be bonded to. For flat substrates, the bonding surface on the wire must be flat too. So, the first step is to shape the bonding region of Cu wires to produce a flat surface. Since equipment is not available to produce flat surfaces on wires, a method was

designed. The Cu wire was first wound on a cylindrical core made of insulating material. MACOR was chosen for the core material because it is a ceramic that can be machined easily [23]. Grooves are machined on the MACOR core to fix the Cu wire in position so that the Cu coil does not move during the process of machining the flat surface on the Cu coil. Fig. 5.1 exhibits the major fabrication steps.

The MACOR core has a diameter of 12.7 mm (0.5 inch) and weighs only 0.02 kg. After winding the 1 mm Cu wire on the core to form a coil, the assembly is coated with lacquer. Flat surfaces on Cu coil are machined to a depth of 0.5 mm which is half of the wire diameter. Each elliptical flat surface has an area of 4.22 mm^2 (6.54×10^{-3} in2). The assembly is thoroughly washed and cleaned. The flat surfaces are electroplated with 50 μm thick Ag. The plating solution contains 5-8% potassium hydroxide and 2-3% Ag oxide. The lacquer that protects other areas from Ag plating is then removed by soaking in acetone bath at room temperature. The assembly is thoroughly cleaned again and annealed at 350 °C for 5 h to grow the Ag grains from 25 nm to a few microns, thus making it more ductile [24].

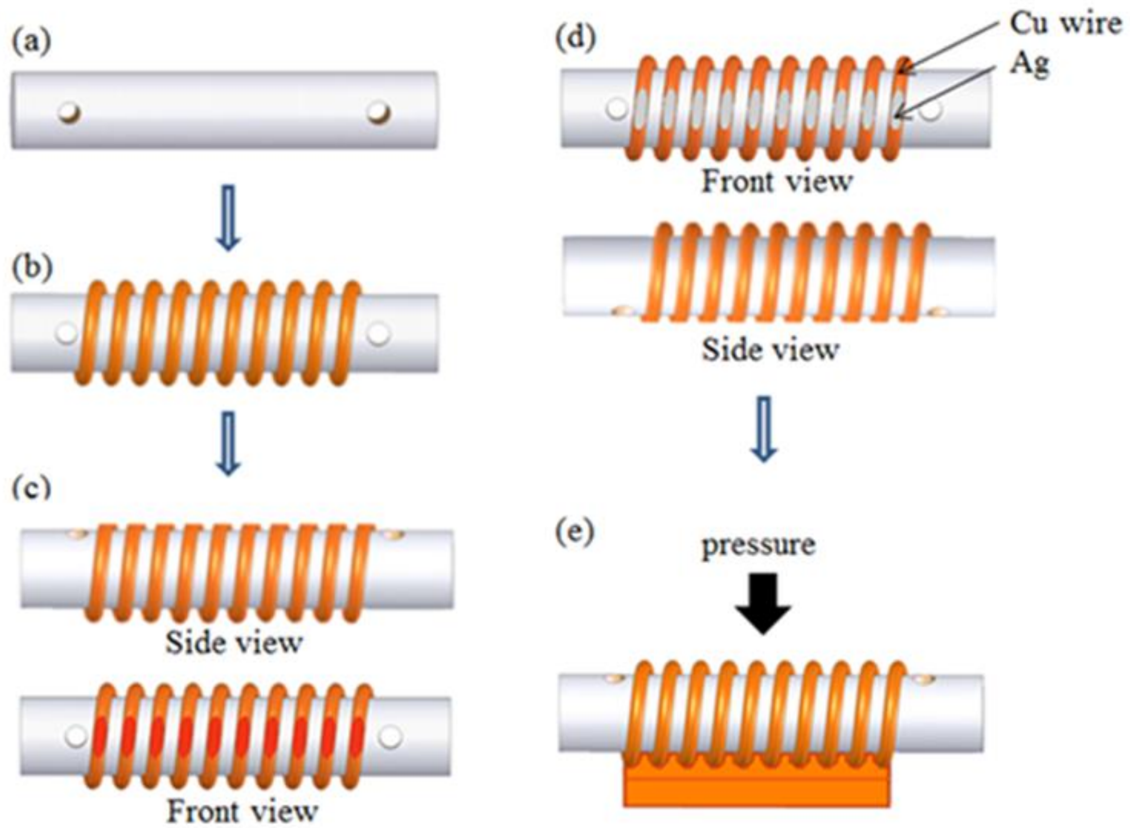


Fig. 5.1 Fabrication steps to bond flat surfaces of a Cu coil on a Si chip or Cu substrate using solid-state bonding process: (a) 12.7 mm (0.5 inch) diameter MACRO core with groove, (b) winding 1 mm Cu wire on the groove and coating the assembly with lacquer, (c) machining the coil to produce flat surfaces on the wire, (d) electroplating 50 μm Ag on the flat surfaces of Cu wire, removing lacquer, and annealing at 350 °C for 5 h, (e) solid-state bonding at 300 °C with 6.89 MPa in 1.33×10^{-5} MPa vacuum for 3 minutes.

Both Cu substrates and Si chips are chosen for the wire bonding experiments. The Si chip emulates a semiconductor device. The Cu substrate represents Cu pads on a package, a module, or a circuit board. Cu substrates of 20 mm × 25 mm are cut from 99.9 % pure 0.8 mm thick Cu sheet. The Si chips are scribed from 50.8 mm (2 inch) wafers that are deposited 30 nm chromium (Cr) and 100 nm Au by e-beam evaporation system at 3.99×10^{-11} MPa vacuum. The Cr layer is the seed layer for adhesion and the Au layer protects Cr from oxidation. The flat Ag surfaces of the Cu coil on the MACOR core are bonded to a Cu substrate or a Si chip, respectively. The assembly is mounted on the graphite platform and applied with 6.89 MPa pressure in a vacuum bonding chamber that is pumped to 1.33×10^{-5} MPa vacuum [25] and then heated to 300 °C with a dwell time of 3 min. The 6.89 MPa is determined by the applied force divided by the actual bonding area. For 1 mm × 3 mm bonding area, the corresponding force is only 2.13 kg. The applied force includes the weight of MACRO core. The 6.89 MPa pressure is 10 times lower than what has been used in industrial thermo-compression bonding processes [26-27]. The assembly is taken out of the bonding chamber after natural cooling in 1.33 × 10-5 MPa vacuum. It takes approximately 120 min to cool down to room temperature. Each turn of the Cu coil on the MACOR core is cut open and the core is removed. Fig. 5.2 is the sample after this step. For cross-sectional evaluations, samples are mounted in epoxy-resin, cut in halves, and polished. SEM and energy dispersive X-ray spectroscopy (EDX) are used to examine the bonding quality,

compositions and the microstructure. In-plane pull test and vertical pull test are performed to measure the breaking force of the wire bonds. The fracture modes and surfaces are studied using optical microscope, SEM, and EDX.

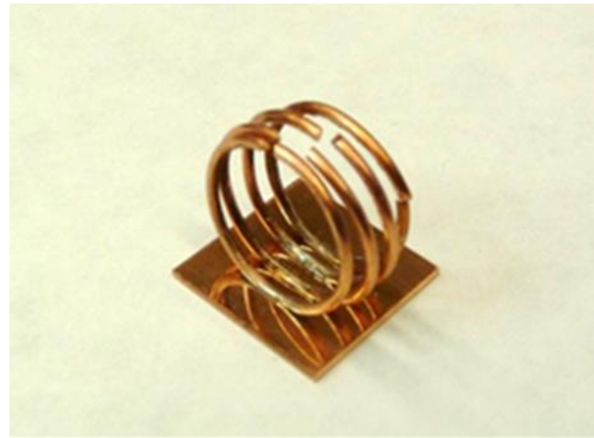


Fig. 5.2 The Cu coils bonded on Cu substrate after each turn was cut open and the MACOR winding core was removed

5.3 Experimental Results and Discussion

Prior to the bonding process, the Cu wires plated with Ag on the flat surface were annealed at 400 °C for 5 h. Fig. 5.3 displays the optical microscopy images of the cross-section of the wire-bond on Cu substrate. The bonding interface appears to be of high quality without voids or cracks. However, a dark line in the Ag layer near the electroplating interface shows up. From Fig. 5.4 and Table 5.1, EDX study reveals it to be the Cu diffusion band. A concern is that the strength of the Cu diffusion band is unknown.

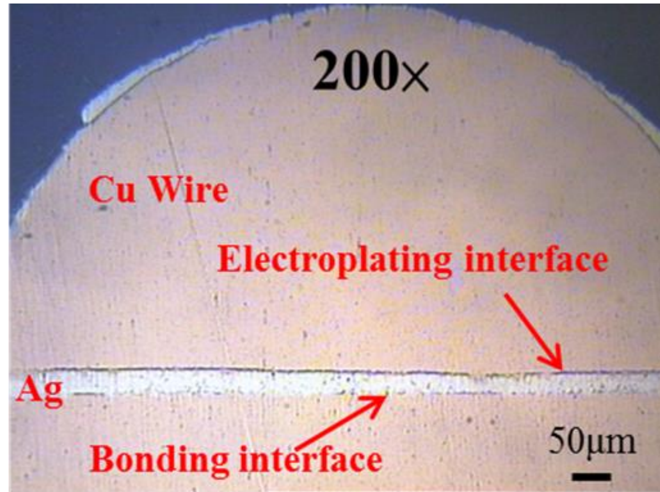


Fig. 5.3 Optical microscopy images of an Ag-plated Cu wire annealed at 400 °C for 5 h and then bonded to Cu substrate at 300 °C with 6.89 MPa pressure

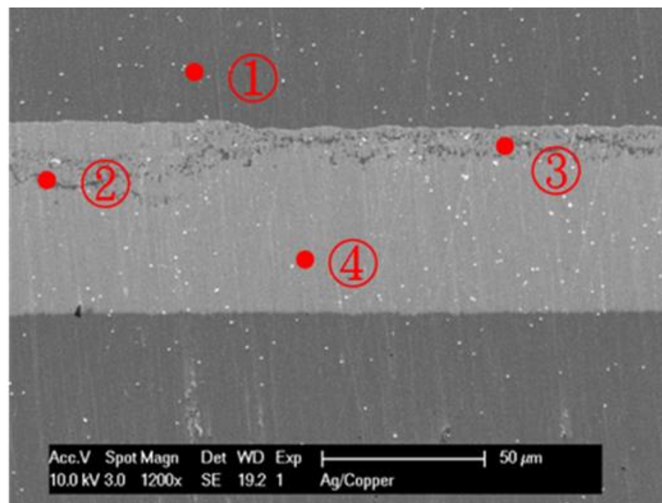
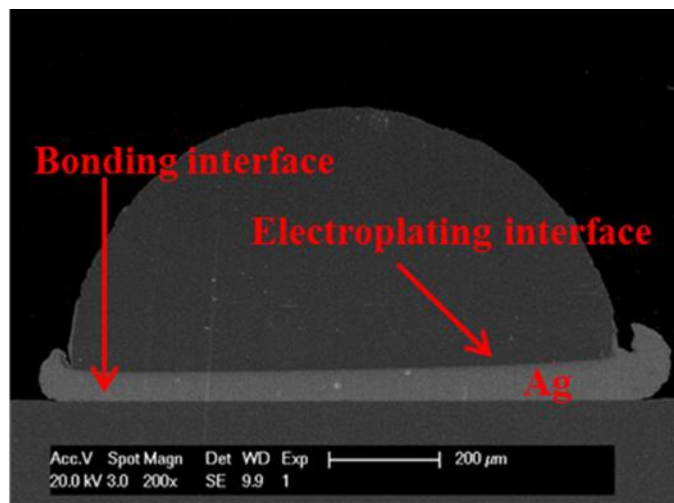


Fig. 5.4 The SEM image includes a black band inside the Ag layer and EDX data demonstrate that it is a Cu diffusion band inside the Ag layer

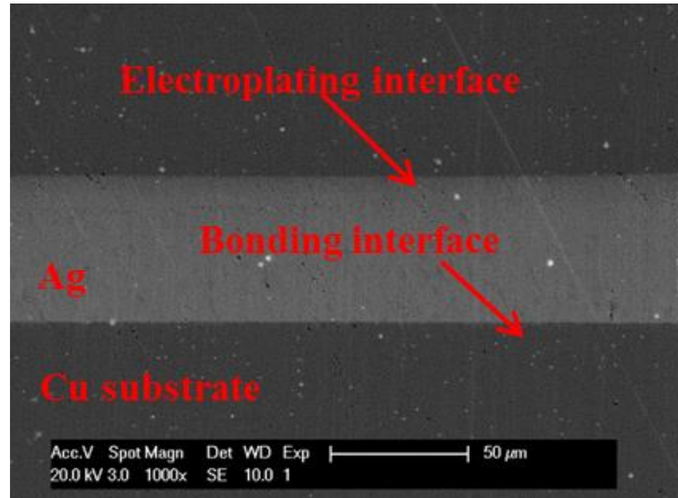
Table 5.1 EDX data on Fig. 5.4 showing the Cu diffusion into Ag

Location	Compositions (atomic %)	
	Cu	Ag
①	100.0	0.0
②	74.6	25.4
③	69.1	30.9
④	0.0	100.0

Therefore, the annealing temperature was reduced to 350 °C. Fig. 5(a) shows the new result of the entire bonding area. There is no black Cu diffusion band inside the Ag layer. It is also seen that the Cu wire is well bonded to the Cu substrate. Fig. 5(b) shows clearly both the plating Cu-Ag and interface bonding Ag-Cu interface. No voids, gaps, or cracks are observed.



(a)



(b)

Fig. 5.5 Cross-section SEM images of a typical wire bond annealed at 350 °C for 5 h and then bonded at 300 °C with 6.89 MPa pressure: (a) low magnification (200×), (b) high magnification (1000×)

In applications, the most important performance parameter is the breaking force of the wire-bond. Two pull tests were performed, in-plane and vertical. The pull test settings are based on military standards MIL-STD-883J method 2011.9 to measure the bond strengths [28]. The in-plane pull test applies the pulling force in a direction on the plane of the bonding interface, as depicted in Fig. 5.6(a). For in-plane pull test, the wire connecting to the Cu substrate is cut to provide two ends accessible with the Cu substrate clamped firmly. The vertical pull test applies force in a direction perpendicular to the plane of the bonding interface, as portrayed in Fig. 5.6(b). The pull is applied by inserting a hook under the Cu wire with Cu substrate clamped

firmly. Table 5.2 presents the pull test results of five typical wire-bonds made on Cu substrates. Three samples were pulled in-plane and two were pulled in vertical direction. The breaking force of in-plane pull test ranges from 20.7 to 23.7 kg, which is comparable to the breaking force of 1mm Cu wire (22.5 kg) [29]. These values should be good enough to survive abuse in real applications. The corresponding shear strength ranges from 48 to 55 MPa. The breaking force of samples 4 and 5 on vertical pull test is 8.7 and 12.2 kg, respectively. The corresponding peel strength is 20.2 and 28.3 MPa. This is called peel strength because the force is in the peel direction. It seems that the peel strength is about one-half of the shear strength. The breaking force of five wire bonds made on Si chips is shown in Table 5.3. Overall, the breaking forces are about 80% of those of wire bonds made on Cu substrates.

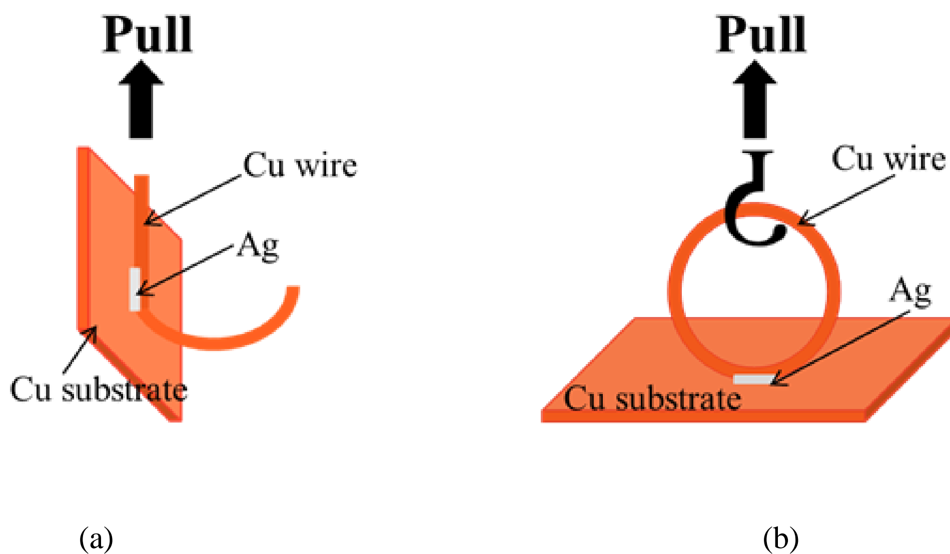


Fig. 5.6 Two pull tests: (a) In-plane pull test and (b) Vertical pull test

Table 5.2 Pull test breaking forces of Cu wire-bonds made on Cu substrates

Sample	Breaking force (kg)	Pull force direction	Shear or peel strength (MPa)
1	20.7	in-plane	48.1 (shear)
2	23.7	in-plane	55.0 (shear)
3	23.3	in-plane	54.1 (shear)
4	12.2	vertical	28.3 (peel)
5	8.7	vertical	20.2 (peel)

Table 5.3 Pull test breaking forces of Cu wire-bonds made on Cu substrates

Sample	Breaking force (kg)	Pull force direction	Shear or peel strength (MPa)
6	15.8	in-plane	36.7 (shear)
7	17.8	in-plane	41.3 (shear)
8	15.1	in-plane	35.1 (shear)
9	8.0	vertical	18.6 (peel)
10	8.5	vertical	19.7 (peel)

We then studied the fracture modes and fracture interfaces. Sample no. 2 broke at two interfaces: near Cu-Ag electroplating interface and Ag-Cu bonding interface. This is the only sample for which Cu wire broke first. Otherwise, the wire-bond is stronger than the Cu wire. All other samples broke at three interfaces: (A) near Cu-Ag electroplating interface, (B) inside Ag layer, and (C) Ag-Cu bonding interface, as illustrated in Fig. 5.7. Fig. 5.8(a) is the SEM image of

the Cu wire of sample 3 in Table 5.2 after being pulled off the Cu substrate. It broke at three interfaces with percentages below: mode A - 40%, mode B - 25%, and mode C - 35%. Figs. 5.8(b), 8(c), and 8(d) are the high magnification images of fracture modes A, B, and C, respectively. To identify accurately where mode A fracture is, EDX analysis on Fig. 5.8(b) was performed and the data were presented in Table 5.4. It is seen that significant amount of Ag was detected. This indicates that the fracture occurs not exactly on the Cu-Ag plating interface, but rather inside the Ag and near the plating interface. EDX data on Fig. 5.8(d) are provided in Table 5.5. The small amount of Cu detected is within measurement error. Thus, it can be said that the mode C fractures at the Ag-Cu bonding interface. Some regions on Fig. 5.8(d) (mode C) are flat because Ag is ductile and deforms when the bonding force is applied.

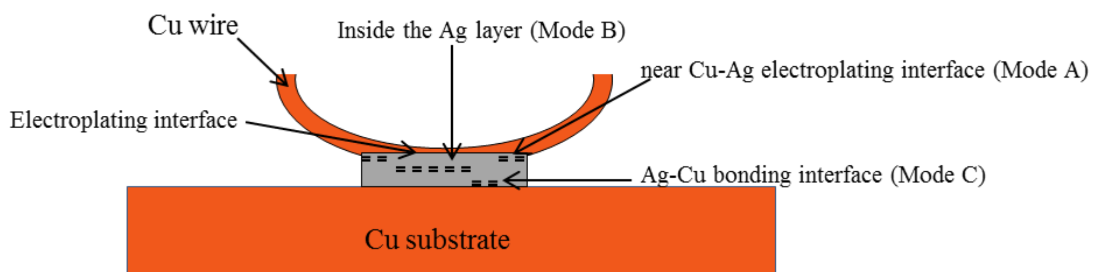
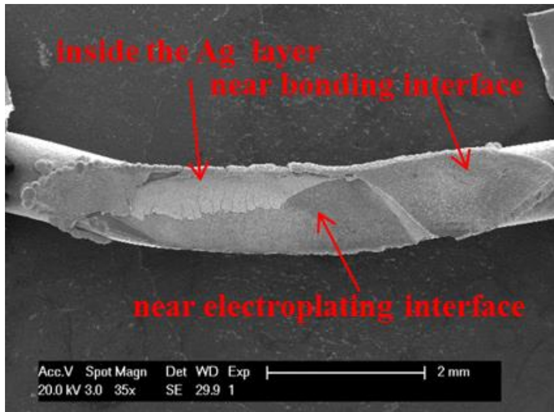
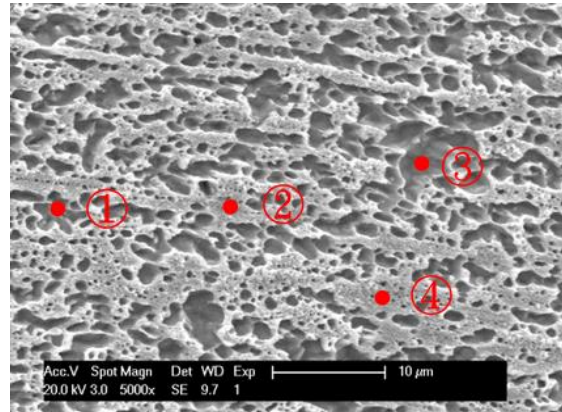
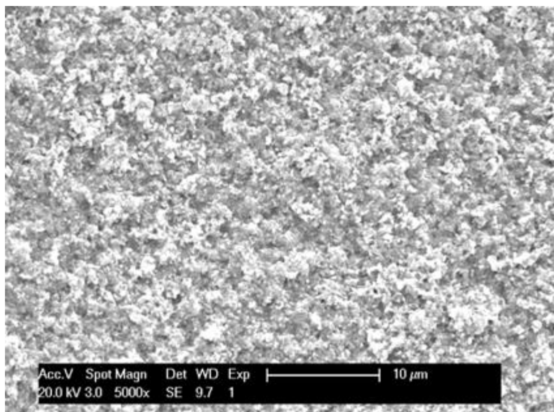


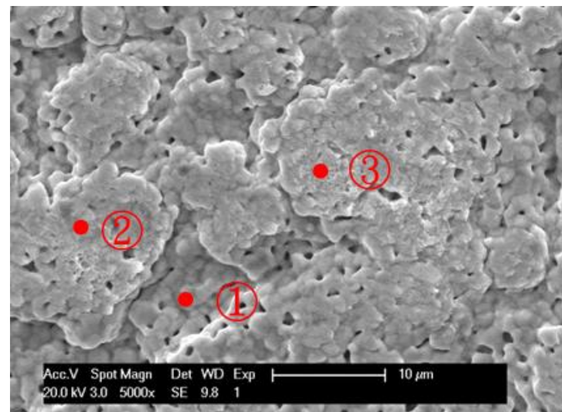
Fig. 5.7 A cross-sectional sketch showing three fracture modes: A, B, and C. Mode A is not exactly on the Cu-Ag electroplating interface, but inside Ag and near the interface





(a) (b)





(c) (d)

Fig. 5.8 SEM images of the bonding region of sample 3 in Table 5.2 after Cu wire being pulled off the Cu substrate: (a) the entire bonding region, (b) mode A: fracture near Cu-Ag electroplating interface, (c) mode B: fracture surface inside Ag layer, and (d) mode C: fracture on Ag-Cu bonding interface

Table 5.4 EDX data on Fig. 5.8(b) showing mode A fracture surface of sample 3 after in-plane pull test

Location	Compositions (atomic %)	
	Cu	Ag
①	81.5	18.5
②	52.0	48.0
③	95.1	4.9
④	68.4	31.6

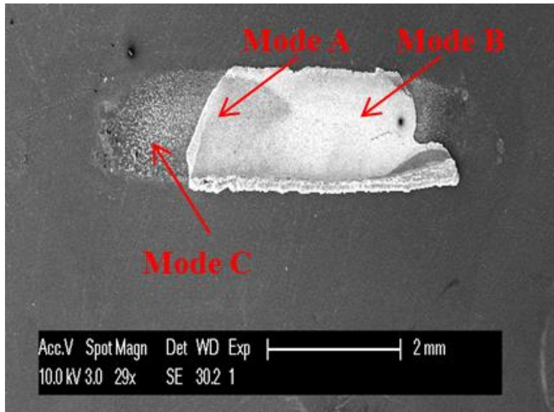
Table 5.5 EDX data on Fig. 5.8(d) showing mode C fracture surface of sample 3 after in-plane pull test

Location	Compositions (atomic %)	
	Cu	Ag
①	0.0	100
②	1.3	98.7
③	0.9	99.1

We next observed the wire bond residue on the Cu substrate after in-plane pull test. The Cu substrate on which Cu wire sample 3 was bonded also had three fracture modes. All three fracture modes on the Cu substrate are presented in Fig. 5.9, to show how they look. Figs. 5.9(b)

and 5.9(c), and 5.9(d) are symmetrical to Figs. 5.8(b), 5.8(c), and 5.8(d). For Figs. 5.9(b) and 5.9(c), they are very similar to Figs. 5.8(b) and 5.8(c). Fig. 5.9(d) it displays small amount of Ag traces on the Cu substrate. Thus, it still can be said that most of this region fractures at the Ag-Cu bonding interface.

Fig. 5.10 exhibits the wire-bond of sample 4 which is bonded to Cu substrate after vertical pull test. It broke in three modes. Fig. 5.11 presents the wire-bond of sample 7 which is bonded to Si chip after in-plane pull test. The wire-bond of sample 9 made on Si chip after vertical pull test is presented in Fig. 5.12. Similarly, they also broke in three modes.



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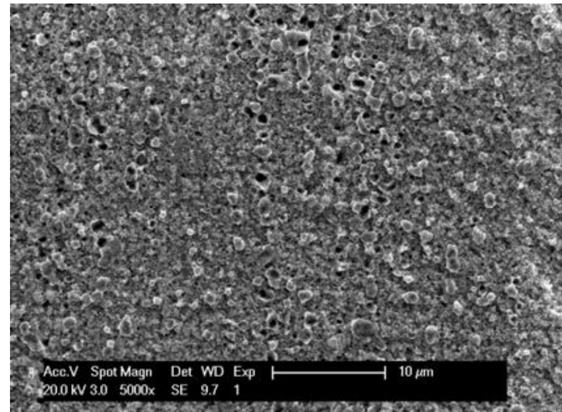

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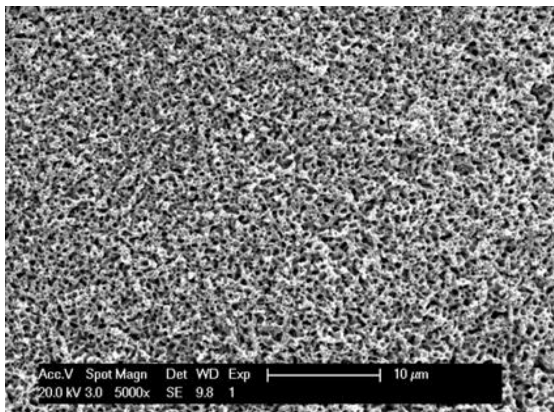

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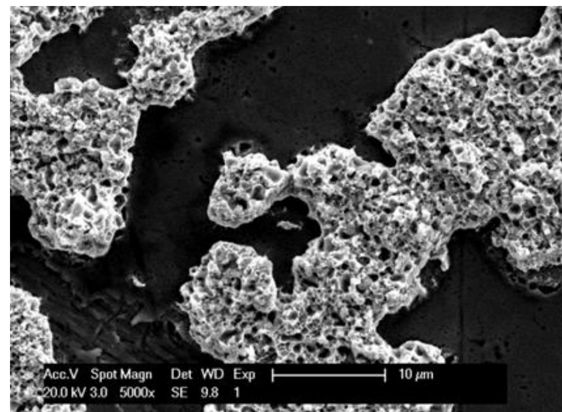
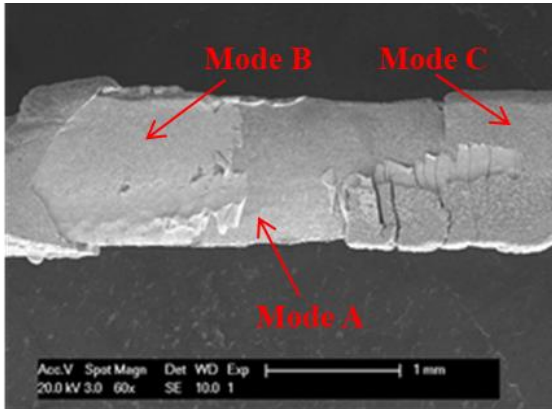


(d)

Fig. 5.9 SEM images of wire bond residue of sample 3 on Cu substrate after pull test: (a) the entire bonding region, (b) mode A: fracture near Cu-Ag electroplating interface, (c) mode B: fracture surface inside Ag layer, and (d) mode C: fracture on Ag-Cu bonding interface



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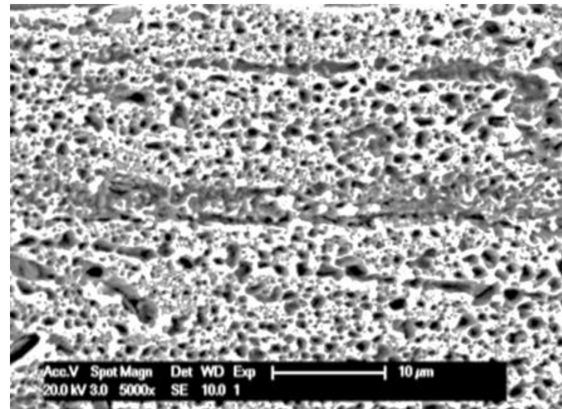

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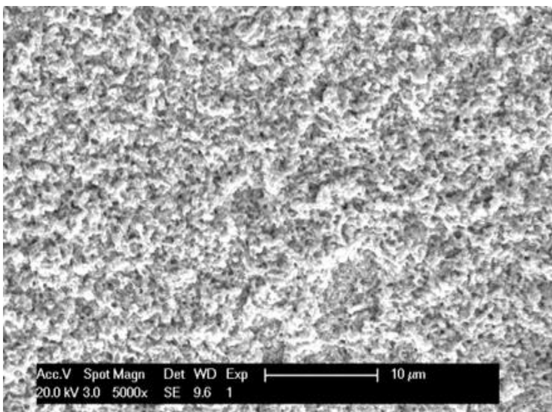

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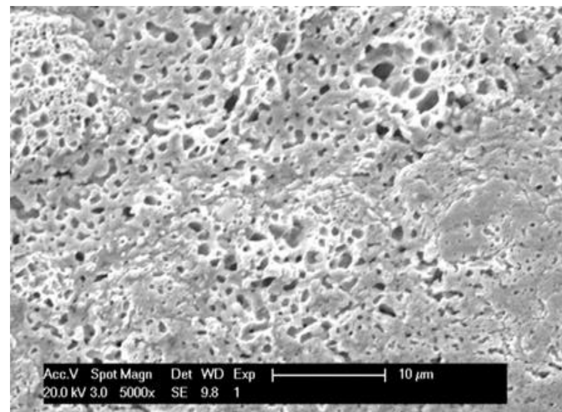
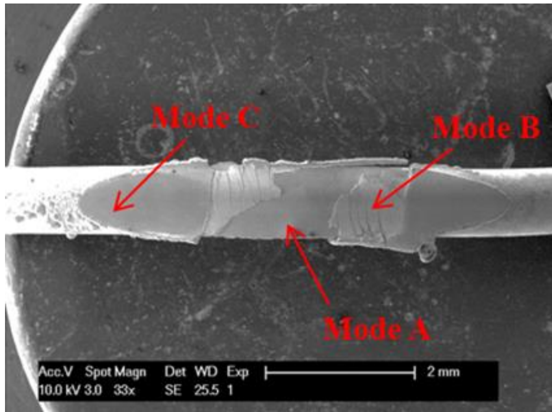


(d)

Fig. 5.10 SEM image of the Cu wire bond sample 4 which is bonded to Cu substrate after vertical pull test: (a) the entire bonding region, (b) mode A: fracture near Cu-Ag electroplating interface, (c) mode B: fracture surface inside Ag layer, and (d) mode C: fracture on Ag-Cu bonding interface



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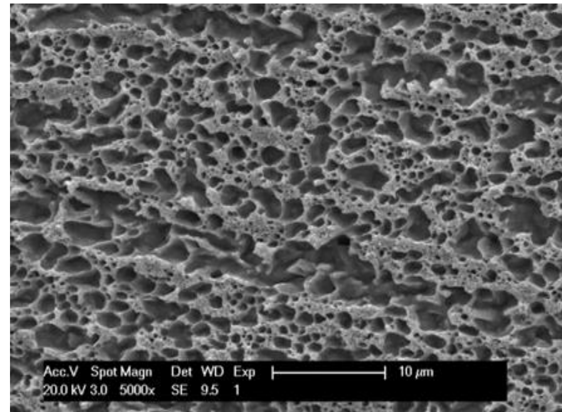

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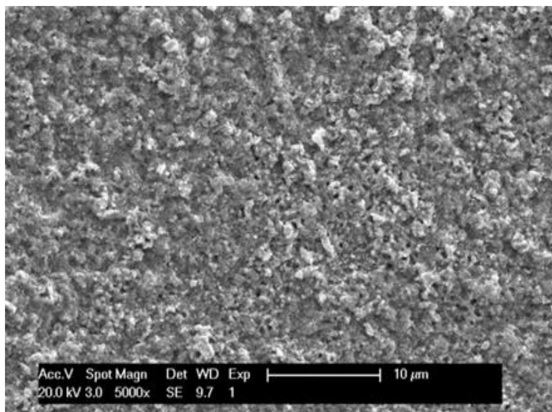

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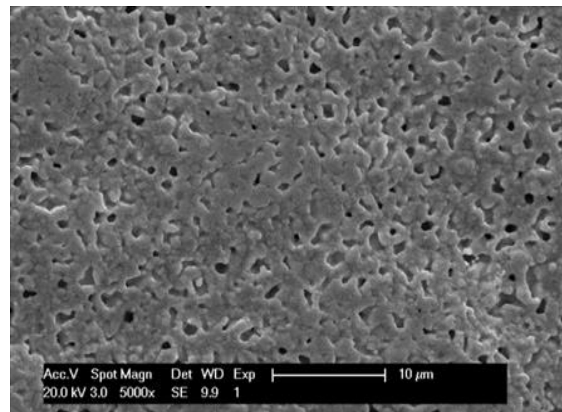
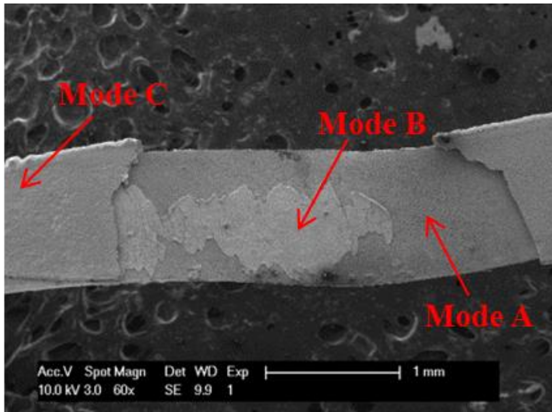


(d)

Fig. 5.11 SEM image of the Cu wire bond sample 7 which is bonded to Si chip after in-plane pull test: (a) the entire bonding region, (b) mode A: fracture near Cu-Ag electroplating interface, (c) mode B: fracture surface inside Ag layer, and (d) mode C: fracture on Ag-Si bonding inter



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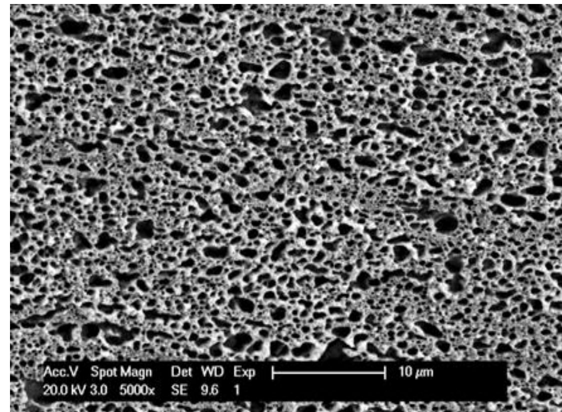

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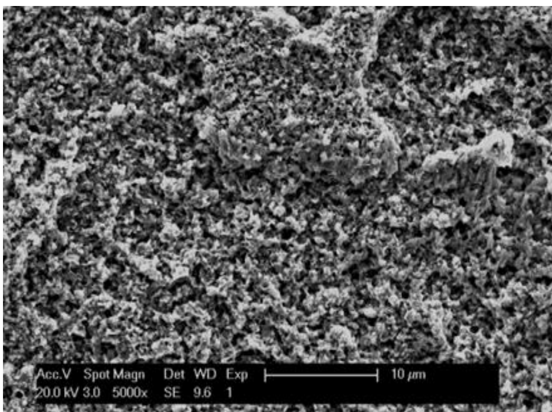

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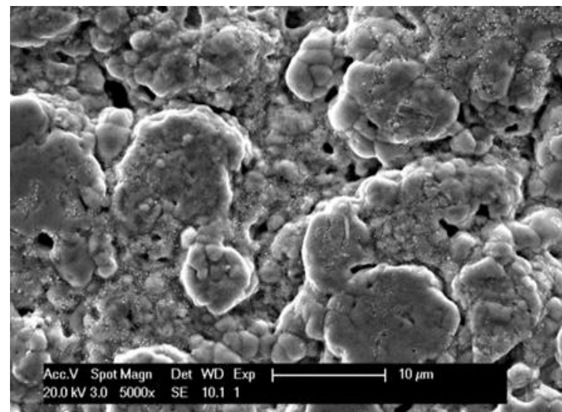

(d)

Fig. 5.12 SEM image of the Cu wire bond sample 9 which is bonded to Si chip after vertical pull test: (a) the entire bonding region, (b) mode A: fracture near Cu-Ag electroplating interface, (c) mode B: fracture surface inside Ag layer, and (d) mode C: fracture on Ag-Si bonding interface

5.4 Summary and Outlook

In this research, we developed solid-state bonding processes to bond 1 mm large Cu wires on Cu substrates and Si chips, respectively. To reduce the bonding pressure, the bonding surface on the Cu wire was plated with Ag and annealed to make it deform more easily. The bonding process was performed at 300 °C with 6.89 MPa for 3 min. This pressure is 10 times lower than what has been used in industrial thermo-compression processes. For 1 mm × 3 mm bonding surface, the force applied is only 2.13 kg. In-plane (shear) pull test measured a breaking of force 20.7 to 23.7 kg, comparable to the 22.5 kg breaking force of the Cu wire. With further improvement on bonding conditions, it is possible to make the wire-bond stronger than the Cu wire itself. There is also room to reduce the bonding temperature and pressure.

This research is a preliminary process development to demonstrate the feasibility of wire-bonds that are strong and can sustain continuous high operating temperature such as 350 °C. With the materials involved, the upper operating temperature limit is the eutectic temperature of the Cu-Ag binary system, 780 °C. Further experiments are required to access the lifetime of the wire-bonds at specific operating temperatures.

Fundamental research on process development has always been some distance away from production. For the wire bonding process reported here, it is practically possible for the industry to turn it in production if the industry is willing to invest in and develop the equipment needed. The path to production is outlined below: a) shape the end of Cu wires into the geometry needed, b) plate the bonding surface of Cu wires with Ag and anneal the Cu wires, c) design and build a machine with a bonding head that grabs the end of the Cu wires, heat it, and press it onto the bond pad is already preheated. In future high temperature electronics operating at 350 °C or above, the wire bonding method reported should be valuable to the electronic industry.

Acknowledgement

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5.5 References

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Chapter Six

Solid-State Bonding of Copper Chips to Copper Substrate Using Silver with Cavities

6.1 Introduction

In electronic devices and packages, bonding of two objects is often needed on various interfaces of the packages. The resulting joints provide structure buildup, electrical connection, and heat dissipation. Fundamentally, all of the bonding methods can be divided into two categories. The first type of method involves molten phase of the bonding medium. The most popular example is the soldering process [1] and [2]. The other method utilizes solid-state process. An example of solid-state bonding is the wire bonding process for interconnection using thermal and ultrasonic energy [3]. For either bonding method, various bonding media are available in the market for different applications. Traditional bonding media include conductive adhesives, lead-free tin-based solders, and gold-tin (Au-Sn) eutectic solders [4], [5], and [6]. The conductive adhesives and lead-free solders cannot sustain temperatures higher than 150 °C [7]. The maximum operating temperature of eutectic Au-Sn solders is 200 °C [8]. For high temperature electronic modules incorporating silicon carbide (SiC) and gallium nitride-based

(GaN) devices, a new bonding medium for high temperature applications is the nano-silver (Ag) paste [9]. After sintering, the paste can be turned into pure silver and then would be able to handle high operating temperature. The sintering process often requires relatively high temperature and pressure [10] and [11]. The resulting Ag joints cannot be made pore-free.

In this research, the solid-state bonding processes between two copper (Cu) pieces using Ag as the bonding medium have successfully developed. The upper Cu piece emulates the semiconductor chip and the lower one is the substrate. Chips of Cu instead of Si were chosen to ensure that the breakage during shear test does not start inside the chip. On the Ag/Cu bonding interface, Ag and Cu need to deform and flow so that the Ag and Cu surface profiles can mate within atomic distance to realize solid-state bonding [12]. Thus, the bonding processes were performed at 300 °C with the pressure of 6.89 MPa (1,000 psi) to bring the Ag and Cu surface profiles within atomic distance. It is worth mentioning that this pressure is less than 10% of what is used in industrial thermo-compression processes [13], [14], and [15]. Some preliminary results were recently presented [16].

In this paper, the fracture modes and fracture surface analyses were studied. In addition, an innovative structural design of creating cavities in the Ag bonding layer is reported to make easier plastic deformation occur in the solid-state bonding process. With this design, the flow distance is not set by the chip size. That is determined by the pattern on the Ag bonding layer. In

other words, the material flow distance is made independent of the chip size. Importantly, the structures bonded with the Ag solid-state process are expected to sustain high operating temperatures, constrained only by the 780 °C eutectic temperature of the Ag-Cu binary system. In the bonding designs, electromigration is also not a concern. The Ag joints are mainly used as a die-attach joints to provide a mechanical fixation of the die on its substrate. No current flows through the Ag joints. On the other hand, if current flow through Ag joints, current density would be relatively small because of the large bonding area. For another form of migration which is caused by bias, it will not occur in this bonding design due to the absence of dielectric layer [17].

In what follows, experiment designs and procedures are first presented. Experimental results are reported and discussed. A summary is then given.

6.2 Experimental Design and Procedures

The fundamental concept of solid-state bonding refers to the atomic interaction between solid material A and solid material B when A atoms and B atoms are brought within atomic range. On the interface, bonding between materials A and B will occur where A atoms and B atoms can share outer electrons. The ability to share outer electrons depends on the electronic configurations. The bonding theory based on quantum mechanics was recently reported [12].

According to the solid-state quantum bonding theory, Ag and Cu atoms must be brought within atomic distance for the Ag and Cu atoms on the interface to share outer electrons and bond. The distance required is 1 nm or less. It is necessary to develop bonding methods to deform the Ag layer in order to conform to the Cu surface profile.

6.2.1 Fabrication steps of Ag layer with the annealing step

For the first design, the fabrication steps of bonding Cu using Ag layer without cavities are as follows. A Cu sheet of 0.8 mm in thickness and 99.9% in purity is diced into 8 mm × 10 mm Cu chips and 12 mm × 12 mm Cu substrates, respectively. The upper piece is called the chip and the lower one is the substrate. Both Cu chips and substrates are slightly polished to remove contamination and Cu oxide. Cu substrates are electroplated with 50 μm Ag layer at room temperature. The electroplating solution contains 5% potassium hydroxide and 6% silver oxide. The plating current density is 13 mA/cm^2. Before the solid-state bonding process, the Ag (50 μm)/Cu substrates are annealed at 400 °C for 5 h to increase Ag grain size to reduce the yield strength for the Ag layer so that it can deform more easily [18] and [19]. The assembly is to fix the position of samples on the heating graphite platform with a static pressure in a vacuum chamber [20]. The Cu chip is placed over the resulting Cu substrate and a spring-loaded fixture is mounted over the assembly to apply a static pressure of 6.9 MPa (1,000 psi) to ensure intimate

contact. The chamber is pumped down to 1.33×10^{-5} MPa. The graphite platform is heated to 300 °C with dwell time of 3 min and cools down to room temperature naturally. The bonding time, 3 min, is constrained by the furnace. In theory, it should take a few seconds rather than minutes for solid–state bonding to occur. The bonded samples are mounted in epoxy resin, cut into halves, and polished for cross-section examination. Based on previous experimental results, the electroplating Ag layer is not able to bond to Cu chips without the annealing step at the same bonding condition [16].

6.2.2 Fabrication steps of Ag layer with cavities

For the second design, the fabrication steps of Ag joints with cavities at room temperature are presented. A 0.8 mm thick Cu sheet, 99.9% pure, is diced into 7 mm × 7 mm Cu chips and 23 mm × 23 mm Cu substrates, separately. Both Cu chips and Cu substrates are slightly polished to remove Cu oxide and clean the samples. Cu substrates are first electroplated with a 10 μm Ag layer to prevent the formation of Cu oxides inasmuch as Cu oxidizes easily. After rinsing and drying, the Cu substrate is heated to 120 °C for 5 min to remove water residue. The photolithography process of Ag layer with cavities is depicted in Fig. 6.1. Drops of photoresist AZ4620 are dispensed on the Cu substrate, which is spun on Laurell spinner at 2500 rpm for 30 s to coat a uniform photoresist layer. The approximate thickness of the photoresist is

9 μm, as measured by Dektak 3 surface profilometer. After the soft baking, the sample is placed below a glass photomask and exposed with UV light of a Karl Suss MA6 Mask Aligner. The photomask has the pattern of 2-dimensional array of black dots on clear background. The sample is then developed using diluted AZ4620 developer. After rinsing and drying, it is baked at 120 °C for 10 min to increase the adhesion and strength of the resulting photoresist pattern. Using this photolithographic process, the photoresist pattern with 50 × 50 array of columns with 50 μm diameter and 100 μm pitch is produced. Afterwards, 5 μm Ag layer is electroplated on the Cu substrate with photoresist columns at room temperature. Thus, Ag is deposited everywhere except where the photoresist columns are. The photoresist is stripped by soaking in acetone until it is removed completely. The resulting sample has 50 × 50 array of 5 μm deep cavities on 10 μm thick Ag layer on the Cu substrate. The bonding area is 44.1 mm^2 by subtracting the area of cavities from the total area of the Cu chip. The bonding conditions of samples with cavities are the same as those without cavities: at 300 °C with 6.89 MPa of pressure for 3 min. Using the same procedure as before, the bonded samples are mounted in epoxy resin, cut into halves, and polished for cross-section examinations.

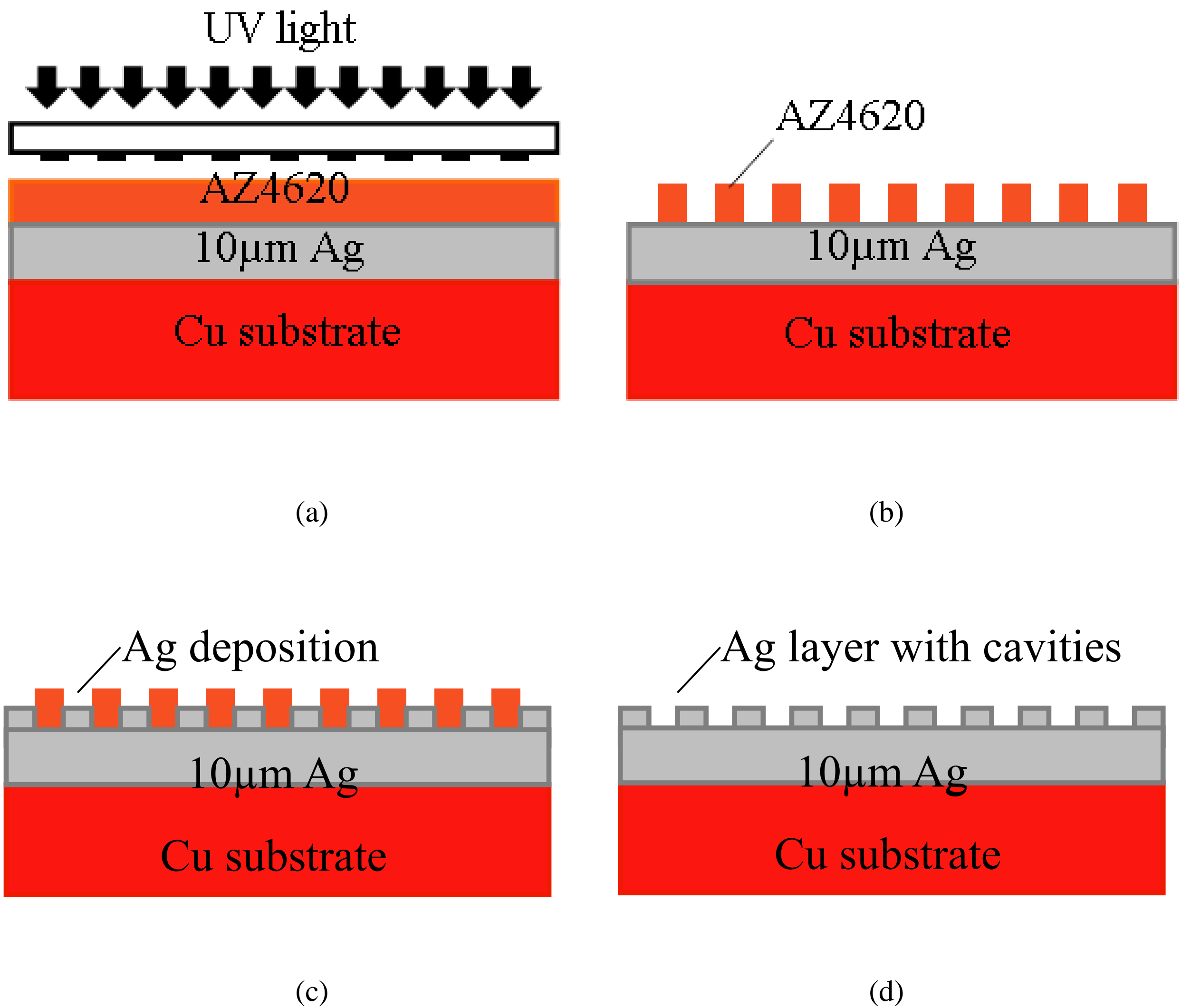


Fig. 6.1 Fabrication steps of Ag layer with cavities: (a) Photoresist coating on Cu substrate with Ag layer and UV exposure through a photomask, (b) Photoresist development, (c) Electroplating Ag on the Cu substrate, and (d) Ag layer with cavities after photoresist stripping

Fig. 2 illustrates bonding mechanisms for two different types of Ag bonding designs. Optical microscope and scanning electron microscopy (SEM) are used to examine the bonding quality, and the microstructure. A standard shear test, performing by Nordson Dage 4000

multipurpose bond-tester, is used to measure the breaking force. The fracture surfaces are studied using optical microscope, SEM, and energy dispersive X-ray spectroscopy (EDX).

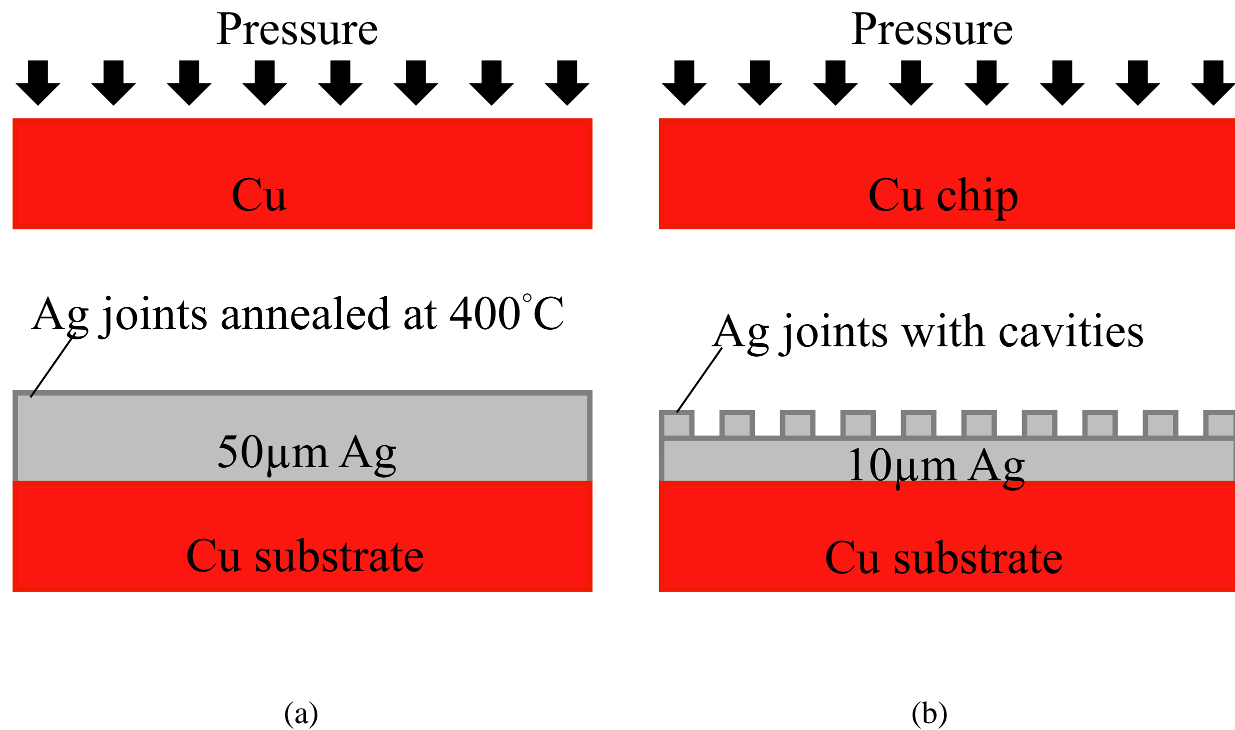


Fig. 6.2 The bonding mechanism for two designs: (a) Ag layer with the annealing step, and (b) Ag layer with cavities

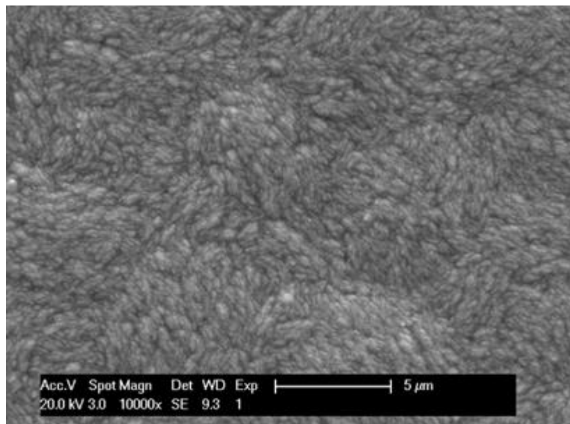
6.3 Experimental Results and Discussion

6.3.1 The bonding design of Ag layer with the annealing step

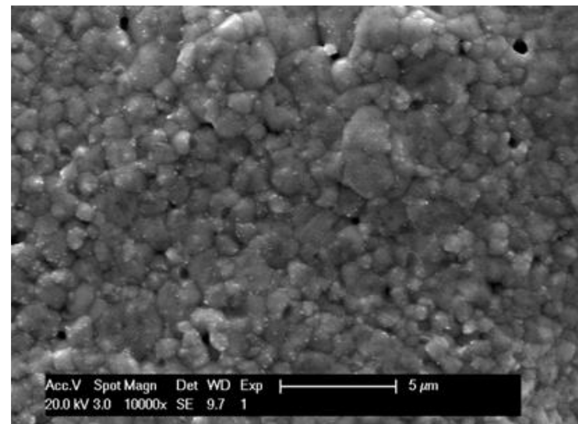
Based on Hall-Petch relation, the yield strength of crystalline metallic materials is related to its grain size, expressed below,

$$\sigma_y = \sigma_o + k_y(d)^{-1/2} \quad (1)$$

where σ_y is yield strength, σ_o and k_y are constants of a specific material, and d is the average grain parameter [19] and [21]. Hence, the yield strength depends on grain size while the grains are not extremely coarse or ultrafine [22] and [23]. For the first design, to reduce the yield strength by increasing the grain size, the 50 μm Ag layers electroplated on Cu substrates were annealed at 400 °C for 5 h [18]. As shown in Fig. 6.3, the Ag average grain size has grown from tens of nanometers to a few micrometers. Lower yield strength is expected to make the Ag layer deform more easily during the bonding process.



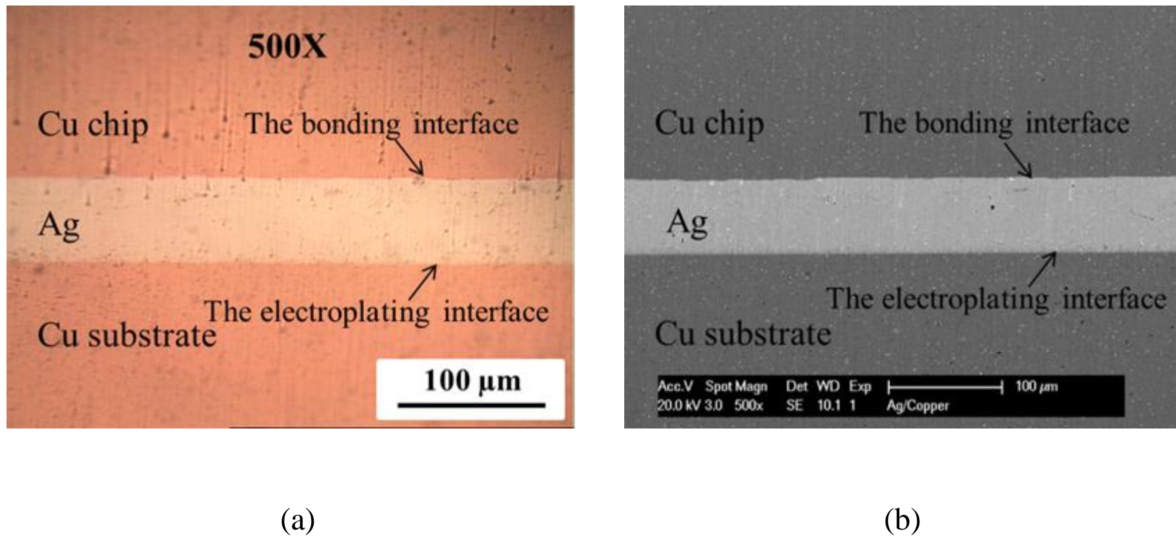
(a)



(b)

Fig. 6.3 SEM images of Ag morphologies on Cu substrates: (a) Ag layer was not annealed, and (b) Ag layer was annealed at 400 °C for 5 h to grow grains

After the annealing step, the resulting Cu substrate was bonded to the Cu chip by solid-state bonding process. The bonding quality is examined by optical microscope and SEM, as shown in Fig. 6.4. The thickness of Ag layer is approximately 50 μm. The Cu/Ag bonding interface and Ag/Cu plating interface are sharp. Both cross-section images demonstrate that the Cu chip is well bonded to the Ag joints on the Cu substrate without visible voids or gaps.



(a) (b)

Fig. 6.4 Cross-section images of a bonded sample used 50 μm Ag joints with annealing step: (a) optical microscopic image, and (b) SEM image

To evaluate the breaking force, a standard shear test was performed on five bonded samples. During the shear test, the sample was fixed on the stage and a tool wedge pushed the entire 8 mm width of the edge face of the Cu chip with a constant speed of 300 μm/s. Fig. 6.5 is a photo of sample #1 after being sheared off. The breaking forces of five samples, ranging from 45

to 90 kg, are presented in Table 6.1. It corresponds to shear strength from 5 to 11 MPa. Based on MIL-STD-883J method 2019.9 in semiconductor die attachment, the breaking force requirement depends on the bonding area [24]. In this case, the bonding area of the sample is larger than 4.1 mm^2 (64×10^{-4} in^2). A breaking force lager than 5 kg is considered to be an absolute pass of the die shear test. All samples tested far surpass this requirement.

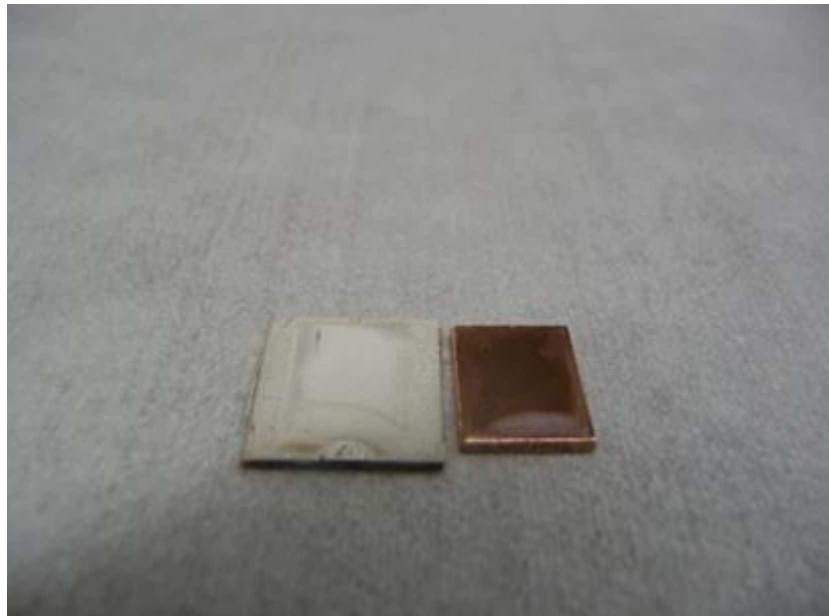


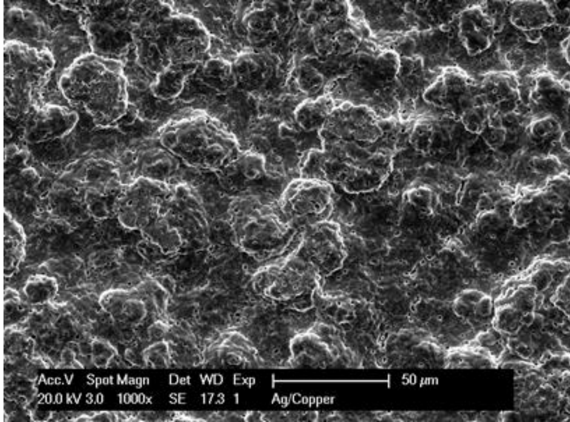
Fig. 6.5 The photo of sample #1 after the shear test

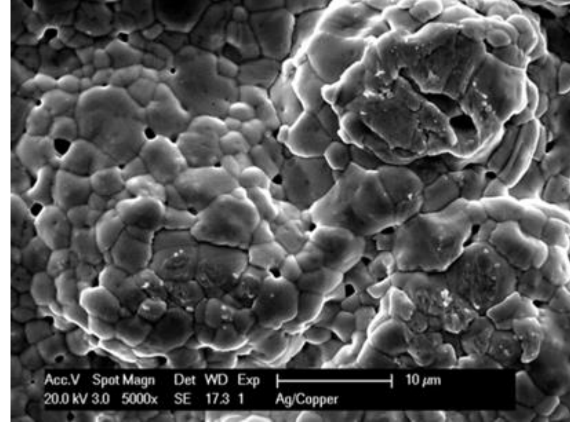
Table 6.1 Shear test results of five samples of Cu chip bonded to Ag layer with the annealing step on Cu substrate

Samples	Breaking force (kg)	Bonding area (mm^2)	Shear strength	
			(MPa)	(psi)
#1	81.6	80	10.0	1400
#2	50.2	80	6.1	900
#3	44.9	80	5.5	800
#4	50.9	80	6.2	900
#5	90.2	80	11.0	1600

During shear test, a ductile metal such as silver normally goes through a few microstructural changes before fracture occurs. With the increase of shear stress, the Ag joints deform, small voids grow and coalesce to form cracks. The cracks propagate and fracture occurs along the most severe crack. At present, there is no means to observe the deformation, voids coalesce, and crack formation actions during shear test. Accordingly, it is important to study the fracture modes. Both the Cu chip and Cu substrate are examined in details. Basically, there are two modes. Mode I: the breakage occurs at the Cu/Ag bonding interface. Mode II: the breakage occurs inside the Ag joints. Fig. 6.6 exhibits SEM images of the Ag joint on Cu substrate of sample #5 after shearing off. Fig. 6.6(a) gives a 1000× magnification view. It is seen that only the hilltops are flattened and contact the Cu chip. Most Ag surface does not contact the Cu

surface and thus is not bonded. Fig. 6.6(b) zooms in the regions that are flattened. The fractured marks on the three hilltops are clearly seen. The Ag hilltops were sheared, deformed and broke. The fracture mode belongs to the ductile mode. The Cu chip of sample # 5 after shearing off is shown in Fig. 6.7. The optical image in Fig. 6.7(a) shows Ag traces in 5–25 μm size on the Cu chip. EDX analysis on the SEM image of Fig. 6.7(b) was performed. The EDX data points of 2 and 3 in Table 6.2 contain small amounts of Ag. In contrast, the EDX data point of 1 in Table 6.2 nly contains Cu. The EDX data confirm that the traces are indeed Ag. These traces are the Ag that remained bonded on the Cu chip after shear test. On these traces, the breakage occurs in the Ag layer rather than on the Cu/Ag bonding interface. The percentage of Ag traces on the entire area was estimated using image processing software. It is approximately 8%. This indicates that only 8% of the entire bonding interface is strongly bonded. If the entire interface is all bonded strongly, the shear strength could be increased from 11 to 137 MPa and the breaking force could increase to 1,100 kg. Preliminary results on Ag-coated Cu wires bonded to Cu substrates have shown shear strength higher than 50 MPa [25].



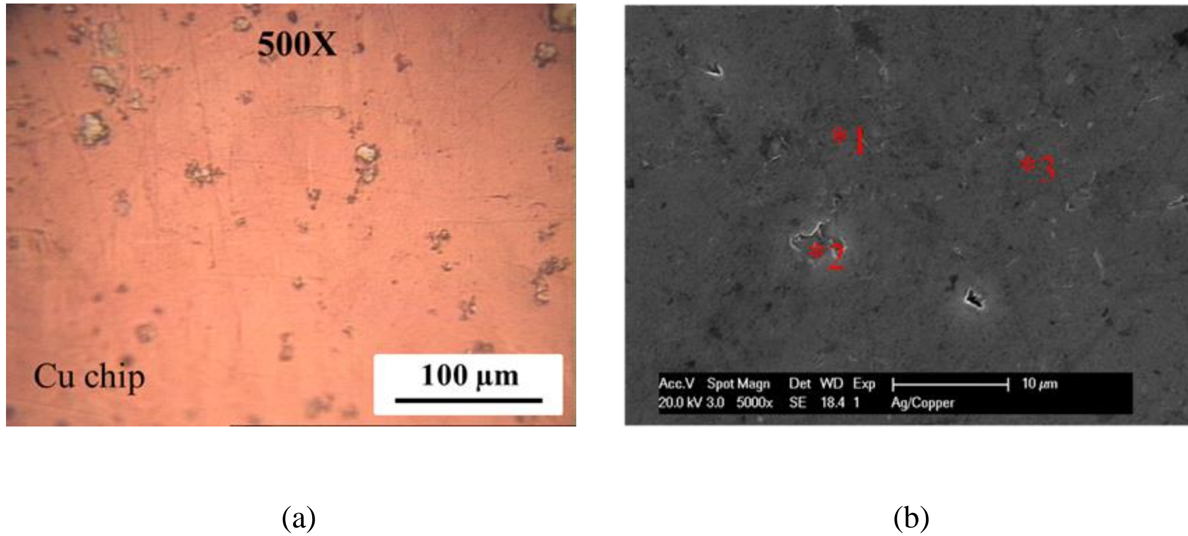


(a) (b)

Fig. 6.6 SEM images of the Ag layer on Cu substrate of sample #5 after shear test: (a) 1,000× magnification showing Ag surface being flattened on some regions, and (b) 5,000× magnification zooming in three hill-tops that were clearly flattened during the solid-state bonding process

Table 6.2 EDX data on the Cu chip that was sheared off sample #5

Location	Compositions (atomic %)	
	Cu	Ag
*1	100.0	0.0
*2	96.5	3.5
*3	95.4	4.6



(a) (b)

Fig. 6.7 Images of Cu chip that was sheared off sample #5: (a) Optical microscopic image of Cu chip showing Ag traces, and (b) SEM image of Cu chip with Ag traces and EDX analysis locations

Based on shear test results, the strongest sample gives a breaking force of 90 kg. Fracture mode analysis indicates that only 8% of the 8 mm x 10 mm chip area was strongly bonded. It could be said that the Ag bonding surface did not conform fully to the Cu surface profile within atomic distance. In order to form atomic contact between Cu and Ag, the Ag surface region has to deform and flow along the lateral direction for some distance to mate the Cu surface within atomic distance. One way to achieve this is to apply high pressure to force materials to move and flow. An example is the thermo-compression bonding technique in industries where the pressure is higher than 68.95 MPa (10,000 psi) [26] and [27]. For advanced applications, such a high

pressure is not an option. The challenge is how to increase strong bonding area without increasing bonding pressure.

6.3.2 The bonding design of Ag layer with cavities

For the second design, the novel idea is to build cavities in the Ag layer for excess Ag to flow into. The fundamental concept is to reduce the flow distance and facilitate plastic deformation. Therefore, the flow distance is now independent of the chip size, so is the bonding pressure. The flow distance is determined by the pitch of the array of cavities. As a result, the annealing step was not required to be done. The Cu chips can be bonded to the Cu substrates with the same conditions as the first design.

To build Ag layers with cavities, photolithography and electroplating processes were developed. Fig. 6.8 exhibits the optical images of the sample at major fabrication steps except that 6.8(e) is a SEM image. Fig. 6.8(a) shows AZ4620 photoresist pattern with array of columns with 50 μm diameter and 100 μm pitch on Ag layer plated over Cu. Fig. 6.8(b) is the same sample after additional Ag layer was plated over the photoresist pattern. The additional Ag thickness is approximately the 60% height of the photoresist columns. After the photoresist columns were removed, cavities were created, as shown in Fig. 6.8(c) and 6.8(d). On Fig. 6.8(c), the microscope was focused on the top surface. On Fig. 6.8(d), the microscope was focused on

the bottom of cavities to observe if the photoresist was stripped completely. Fig. 6.8(e) is the resulting sample with array of 50 × 50 cavities. Afterwards, the bonding conditions were kept the same at 300 °C with the pressure of 6.89 MPa (1,000 psi) for 3 min. The Cu chip was bonded to Ag layer with cavities on the Cu substrate by solid-state bonding process. Fig. 6.9 shows the cross-section SEM image of a representative bonding region. The thickness of Ag joint is 15 μm including 10 μm Ag layer and 5 μm Ag layer with cavities. No visible voids and gaps are observed at the Cu/Ag bonding interface. Fig. 6.10 shows a typical cavity, 50 μm diameter, before the bonding process. The diameter is used as reference to examine the deformation of Ag layer. As seen in Fig. 6.9, the diameter of cavities shrank to 45 um while the edge-edge distance extended to 55 μm, approximately. In average, the diameter of the cavities has reduced from 50 to 45 μm, i.e., 10% of reduction of diameter, after the bonding process. That indicates that some Ag deformed and flowed into the cavities. Surprisingly, some Cu on the Cu chip also protruded and got into the cavities during the bonding process. As a result, the cavities seem completely filled. However, the shear test results to be presented below show otherwise.

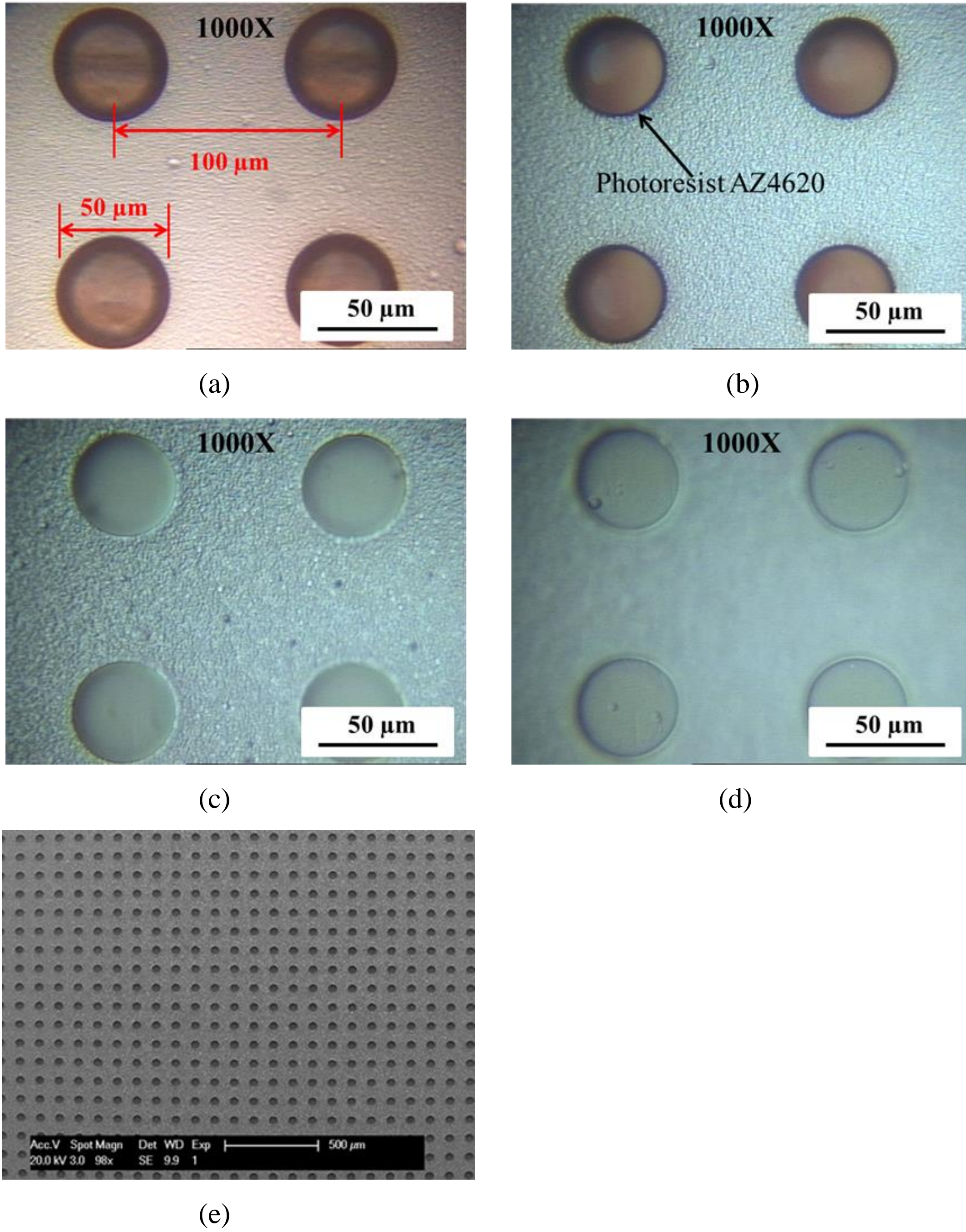


Fig. 6.8 Images of fabricating steps: (a) photoresist with columns with 50 μm in diameter and 100 μm pitch made on 10 μm Ag layer on a Cu substrate, (b) after electroplating 5 μm thick Ag, (c) after removing photoresist, (d) focusing on the cavity bottoms to ensure that photoresist was removed completely, and (e) Ag layer with an array of 50 × 50 cavities.

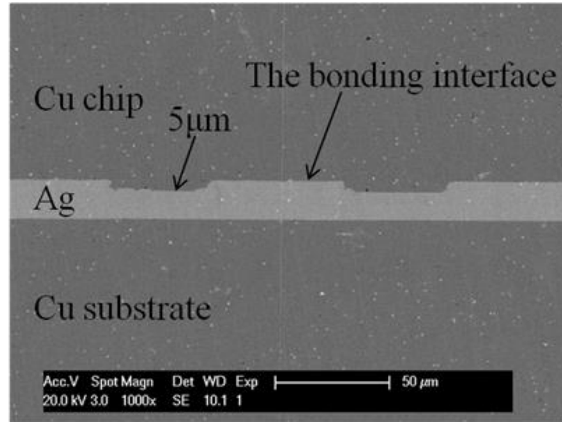


Fig. 6.9 Cross-section SEM image of a sample of Cu chip bonded on Ag layer with cavities plated on a Cu substrate

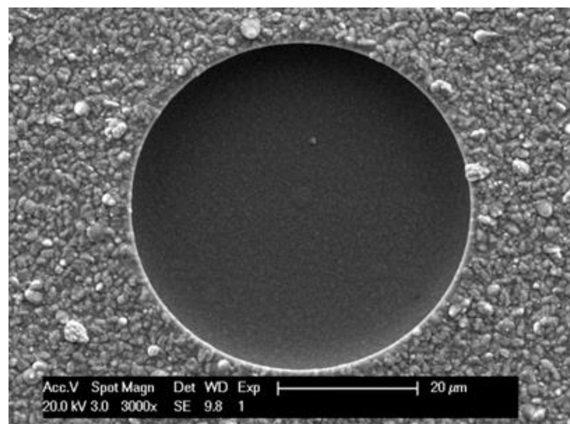


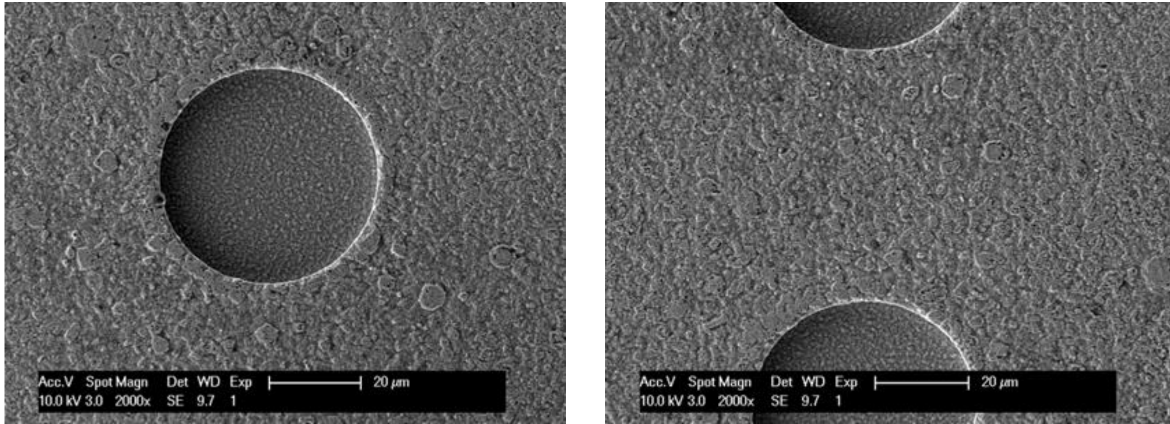
Fig. 6.10 Close-up SEM image of a single cavity

A standard shear test was performed on five bonded samples to determine the bonding strength. The breaking force is given in Table 6.3. It ranges from 22 to 48 kg, corresponding to the shear strength from 5 to 11 MPa. Since the sample size is larger than 4.1 mm^2 (64×10^{-4} in^2), all five samples well exceed the 5 kg breaking force requirement in MIL-STD-883J standards. It

is vital to study the fracture modes and surfaces. As mentioned earlier for the bonding design without cavities, two fracture modes were observed, designated Mode I and Mode II. Fig. 6.11(a) and 6.11(b) are SEM images of two representative regions on the substrate of sample #8 after the Cu chip was sheared off. Fig. 6.11(a) shows a representative cavity and 6.11(b) is a region between two cavities. The Ag material near and between cavities can deform and flow easily because of the space provided by the cavities. It is displayed that the hilltops on the Ag layer were flattened. Examination of the entire Ag terrain shows that the deformation is global, exhibiting that all the hilltops were flattened to mate the Cu surface and achieve solid state bonding.

Table 6.3 Shear test results of five samples of Cu chip bonded to Ag layer with cavities on Cu substrate

Samples	Breaking force (kg)	Bonding area (mm^2)	Shear strength	
			(MPa)	(psi)
#6	35.3	44.1	7.8	1100
#7	38.0	44.1	8.4	1200
#8	48.4	44.1	10.8	1600
#9	41.9	44.1	9.3	1300
#10	21.8	44.1	4.8	700



(a) (b)

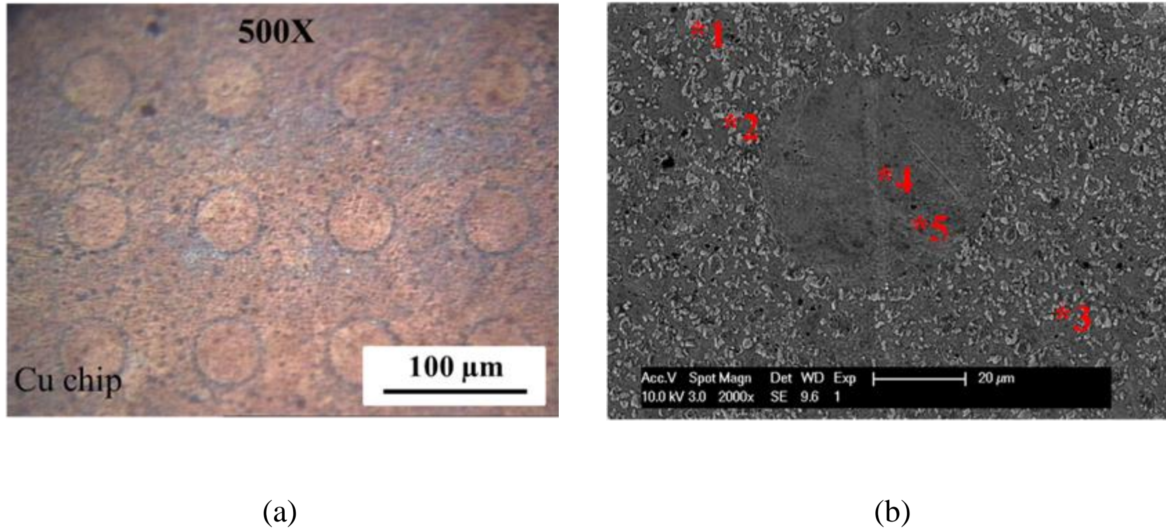
Fig. 6.11 SEM images of Ag layer with cavities on Cu substrate that was sheared off sample #8: (a) Ag material near the cavities was flattened, and (b) Ag surface between cavities was flattened

Fig. 6.12 exhibits the SEM images of the Cu chip that was sheared off sample #8. Fig. 6.12(a) clearly show numerous Ag traces at 500× magnification that still bonded to the Cu substrate after shear test. It also provides some crucial information as to whether Cu filled the cavities. If Cu indeed filled the cavities, the circles should have protruded by 5 μm. At 1,000× magnification, the optical microscope was able to focus on the circles and the chip surface at the same time. This demonstrates that the circles are on the same plane as the substrate within 0.5 μm, which is the depth of the focus of the microscope objective. The Cu that appears filling the cavities could be caused by smearing during the polishing process. Fig. 6.12(b) zooms in the image to display the Ag traces more clearly. The EDX data points of 1, 2 and 3 in Table 6.4,

which are located outside the circle in Fig. 6.12(b), contain large amounts of Ag. In contrast, the EDX data points of 4 and 5 in Table 6.4, which are located inside the circle in Fig. 6.12(b), only contain Cu. Based on EDX data, all white marks are Ag traces. The percentage of Ag traces on the entire bonding area is 22%, which can be calculated using image processing software. On these trace locations, the Ag joints break inside the Ag layer rather than along the Cu/Ag interface. These are the regions where the Ag is strongly bonded to the Cu chip. If the entire bonding area were strongly bonded, the shear strength would have increased from 11 to 42 MPa and the breaking force could increase to 220 kg. It is essential to observe the strongly bonded percentage in two bonding designs. Using the Ag layer with cavities, the strongly bonded percentage has been increased from 8 to 22% compared to the design without cavities. Therefore, the result of building cavities inside Ag joints is encouraging.

Table 6.3 EDX data on the Cu chip that was sheared off sample #8

Location	Compositions (atomic %)	
	Cu	Ag
*1	6.6	93.4
*2	40.3	59.7
*3	43.1	56.9
*4	100.0	0.0
*5	100.0	0.0



(a) (b)

Fig. 6.12 Images of Cu chip that was sheared off sample #8: (a) The optical microscopic image shows that Ag traces reminded bonded on the Cu chip, and (b) The SEM image shows that Ag traces on the Cu chip with EDX analysis locations

6.4 Summary

Solid-state bonding processes were successfully developed between Cu chips and Cu substrates using two different types of bonding designs. In this research, two bonding designs were presented to meet requirements for different applications. For the first design, 50 μm Ag layer was plated over Cu substrate and annealed at 400 °C for 5 h to make the Ag layer easier to deform during bonding. The photolithographic process is not required. For the second design, 10 μm Ag layer was plated over Cu substrate, followed by another 5 μm Ag layer with cavities. Note that in the first design the electroplating Ag layer is not able to bond to Cu chips without

the annealing step at the same bonding condition. The purpose of this new design with cavities inside the Ag bonding layer is to reduce the flow distance and acquire more plastic deformation. Thus, the annealing step is not necessary for bonding the chips to the substrates. The percentage of the Ag layer that is strongly bonded in the second design is 22%, which is higher than that 8% in the first design.

For both designs, Cu chips were placed on Cu substrates so produced and bonded at 300°C with 6.9 MPa pressure in 1.33×10^{-5} MPa vacuum for 3 min. This is a solid-state bonding process. No molten phase was involved and no flux was used. The shear strength of 10 samples was tested and reported. The shear test results of 10 samples show both Ag joints are strongly bonded and far exceed MIL-STD-883J method 2019.9. It eliminates a concern of bonding strength from industries for practical applications. Based on phase diagram, typically, Ag joints with Cu do not contain any intermetallic compound (IMC). Compared with solder joints used in industries, most of reliability issues associated with IMC and IMC growth do not exist. The bonded structure consists of only Cu/Ag/Cu, which has the 780°C eutectic temperature of the Ag-Cu binary system. In addition, both Cu and Ag have relatively high electrical/thermal conductivities and superior mechanical properties. This bonding structure may be applied to electronic devices that high thermal performance or high operating temperature is required.

Acknowledgement

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Chapter Seven

Solid-State Bonding of Silicon Chips Directly on Copper Substrates With Trenches

7.1 Introduction

The thermal management solutions for high performance electronic devices have continued to grow. To address such problems, metal bonding is considered to be a possible method. The challenge is how to bond the dies to metal substrates without forming voids and gaps at relatively low temperature? For instance, direct bonding copper (DBC) substrates have been largely used in the packaging due to its exceptional properties, including high thermal conductivity, high current carry capacity, and excellent mechanical properties [1-2]. This technology still needs to bond copper (Cu) to silicon (Si) or silicon carbide (SiC) or other types of chips. Nano-silver (Ag) paste could be a promising die attach material. At present, the Ag paste sintering process often requires relatively high temperature and pressure [3-4]. The resulting Ag joints cannot be made pore-free.

In order to response this challenge, the novel method is developed to bond the Si chips to Cu substrates directly. The basic concept is to provide free space for Cu and Si to deform without restriction by producing trenches inside the Cu substrate. When the bond between two surfaces is formed, the trenches inside the Cu substrate could release the part of thermal stress from the coefficient of thermal expansion CTE mismatch. Therefore, the bond could deal with the large CTE mismatch between Si (3 ppm/°C) and Cu (17 ppm/°C).

In this paper, we report results of bonding Si chips to Cu substrates with trenches using the solid-state bonding process. After the samples were bonded, the etching pattern, bonding quality, and microstructure were examined using optical microscopy and scanning electron microscopy (SEM). The bond strength was examined by a simple shear test. The fracture modes were studied. In what follows, we first present the experimental design and procedures. Experimental results are then reported and discussed. Finally, a short summary is given.

7.2 Experimental Design and Procedures

The fabrication steps of Cu substrates with trenches at room temperature are presented. Fig.7.1 illustrates the major steps of fabricating the pattern on the Cu substrates. A 0.8 mm thick Cu sheet, 99.9% pure, is diced into 23 mm × 23 mm Cu substrates. Cu substrates are slightly polished to remove Cu oxide and clean the samples. The photolithography process is performed

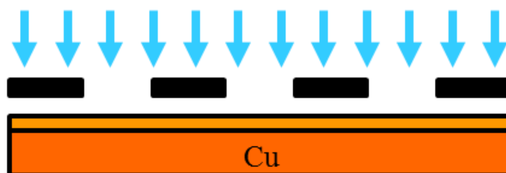
to build the pattern on Cu substrates immediately after polishing the samples. To begin with, drops of photoresist AZ4620 are dispensed on the Cu substrate, which is spun on Laurell spinner at 2500 rpm for 30 s to coat a uniform photoresist layer. The approximate thickness of the photoresist is 9 μm, as measured by Dektak 3 surface profilometer. After the soft baking at 90°C, the sample is next placed below a glass photomask and exposed with UV light of a Karl Suss MA6 Mask Aligner. The samples are then developed using diluted AZ4620 developer. After rinsing and drying, it is baked at 120 °C for 3 min to increase the adhesion and strength of the resulting photoresist pattern. Finally, the photoresist pattern is produced as the designed photomask, as shown in Fig.7.2. Table 7.1 lists the cumulative radial distribution using the diagonal line from the center to the vertex on the square photomask, 5 mm × 5 mm. For the photomask design, the black region is protected and the white region is exposed to UV light. It consists of that the width of trenches is 25 μm and the diameter of the hole at center is 25 μm. Additionally, the gaps between trenches are 100 μm, while the thickness of the ring 1,2, and 3 is 500 μm, and the thickness of ring 4,5,6,7, and 8 is 250 μm. The gaps functions as the bridges to connect the bonding area together, which are along the diagonal lines to form 6 gaps for each.

(a) Polishing and cleaning Cu substrates

(b) Photoresist coating

(c) Soft baking

(d) Mask alignment and UV exposure



(e) Development

(f) Hard baking

(g) Cu etching

(i) Photoresist stripping

Fig. 7.1 The major steps of fabricating the pattern on Cu substrate (a) Polishing and cleaning the Cu substrates, (b) Photoresist coating, (c) Soft baking, (d) Mask alignment and UV exposure, (e) Development, (f) Hard baking, (g) Cu etching, and (i) Photoresist stripping

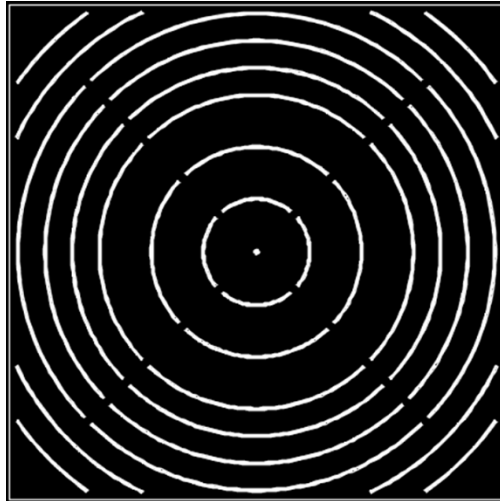


Fig. 7.2 The pattern of photomask

Table 7.1 The designed pattern for the Cu etching process

Designed Pattern	Width	Cumulative Radial Distribution
The hole at center	25 µm	25 µm
Ring 1	500 µm	525 µm
Trench 1	25 µm	550 µm
Ring 2	500 µm	1050 µm
Trench 2	25 µm	1075 µm
Ring 3	500 µm	1575 µm
Trench 3	25 µm	1600 µm
Ring 4	250 µm	1850 µm
Trench 4	25 µm	1875 µm
Ring 5	250 µm	2125 µm
Trench 5	25 µm	2150 µm
Ring 6	250 µm	2400 µm
Trench 6	25 µm	2425 µm
Ring 7	250 µm	2675 µm
Trench 7	25 µm	2700 µm
Ring 8	250 µm	2950 µm
Trench 8	25 µm	2975 µm
From the center to vertices		3536 µm

The depth of trenches is 30 μm, which is acquired by using the Cu etching process. The etchant is ferric chloride ($FeCl_3$) solution, MG Chemicals 415 Ferric Chloride Liquid. Importantly, the etching rate of the $FeCl_3$ mainly changes along with the processing temperature. In this project, the Cu substrates with photoresist are soaked into the $FeCl_3$ solution for 5 min at 50 °C. Therefore, the etching rate of Cu in $FeCl_3$ etchant is 6 μm/min at 50 °C ± 2 °C approximately. After the etching step, the photoresist is stripped by soaking in acetone. The following is a simple mechanism of Cu etching in $FeCl_3$ solution. The Cu surface is first oxidized by ferric ions to form ferrous chloride ($FeCl_2$) and cuprous chloride (CuCl). Next, CuCl gets oxidized in $FeCl_3$ etchant to produce cupric chloride ($CuCl_2$) while CuCl is formed. Last, the $CuCl_2$ also reacts with the Cu surface to form CuCl. In fact, the Cu surface is chemically etched with $FeCl_3$ and $CuCl_2$. The chemical reaction of Cu in $FeCl_3$ etchant is listed as follows [5]:

$$FeCl_3 + Cu \rightarrow FeCl_2 + CuCl \quad (7\text{-}1)$$

$$FeCl_3 + CuCl \rightarrow FeCl_2 + CuCl_2 \quad (7\text{-}2)$$

$$CuCl_2 + Cu \rightarrow 2CuCl \quad (7\text{-}3)$$

To prevent Cu from oxidation, 1 μm Ag layer is electroplated on the Cu substrate at room temperature. Ag is deposited everywhere including the bottom of the trenches. There is no annealing step carried out in between the material preparation and the solid-state bonding process. The bonding conditions of samples with trenches are the same as those without trenches

in previous chapters: at 300 °C with 6.89 MPa (1000 psi) of pressure for 3 min [6]. Using the same procedure as before, the bonded samples are mounted in epoxy resin, cut into halves, and polished for cross-sectional examinations. Optical microscopy and scanning electron microscopy (SEM) are first used to study the etching pattern, the bonding quality, and the microstructure. Next, a simple shear test is conducted to evaluate the bond strength. Finally, the fracture modes and surfaces are studied.

7.3 Experimental Results and Discussion

To build Cu substrates with trenches, photolithography, etching and electroplating processes were developed. Fig. 7.3 exhibits the optical image of the sample with AZ4620 photoresist after the etching process. It is clearly seen that the trenches are inside the Cu substrate. Prior to the plating process, the photoresist were stripped off. Fig. 7.4 is the same sample after additional Ag layer of 1 μm was plated over the photoresist pattern. Due to the lateral etching of Cu, the width of gaps between the bridges is reduced to 50 μm. The trenches are also increased from 25 to 75 μm, which result in that the thicknesses of the rings are decreased from 250 to 200 μm and 500 to 450 μm, respectively. Fig. 7.5 shows cross-sectional SEM images after the etching process. The depth of trenches is 30 μm approximately. The

distance between the tranches is the thickness of the ring. At present, the Cu substrate is ready to be bonded to the Si chip.

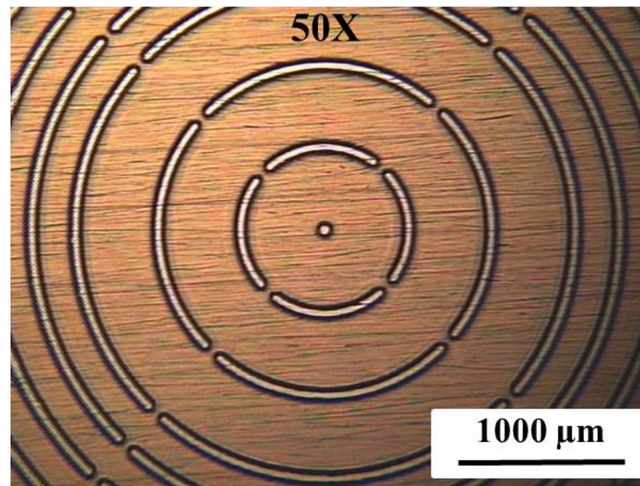


Fig. 7.3 The optical microscopic image of Cu substrate after the Cu etching process

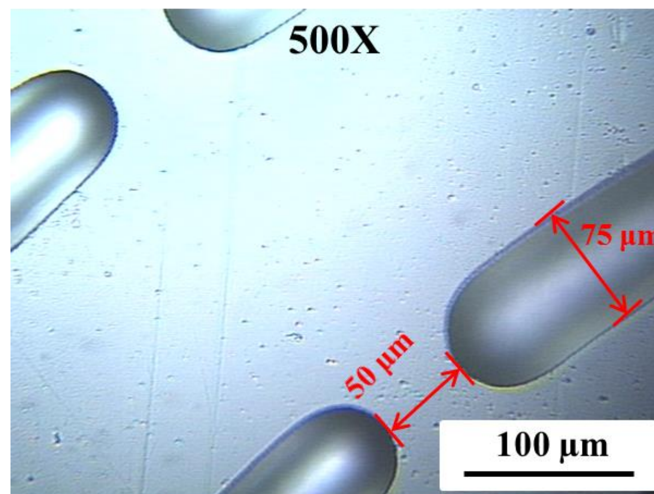
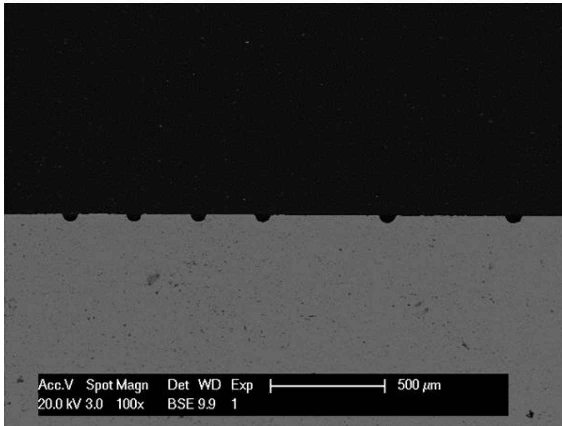
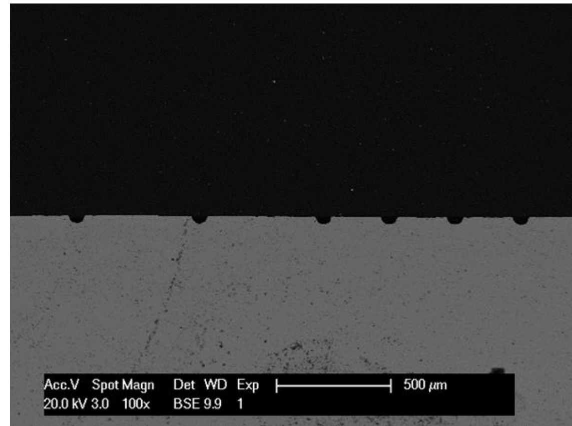


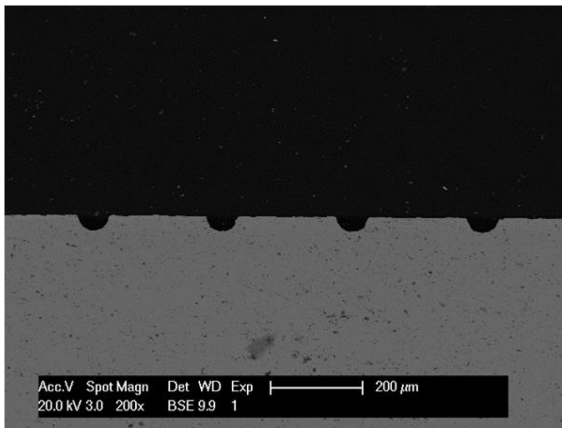
Fig. 7.4 The optical microscopic image of Cu substrate after the Ag electroplating process



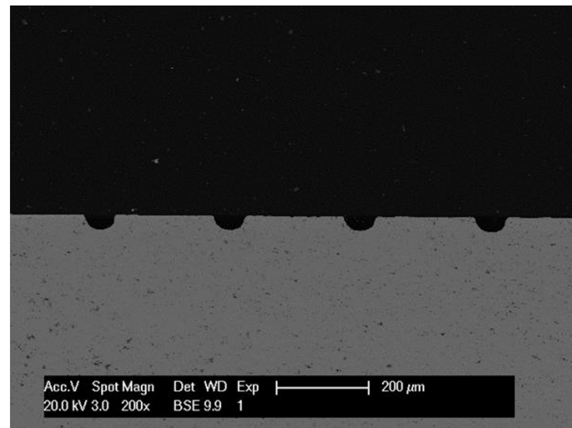
(a)



(b)



(c)



(d)

Fig. 7.5 The cross-sectional SEM image with trenches before the solid-state bonding process (a) The left side of trenches at 100× magnification, (b) The right side of trenches at 100× magnification, (c) The left side of trenches at 200× magnification, and (d) The right side of trenches at 200× magnification

Table 7.2 Typical CTE values of the materials

Materials	Coefficient of thermal expansion (ppm/°C)
Si chip	2.6
Ag capping layer	18
Cu substrate	17

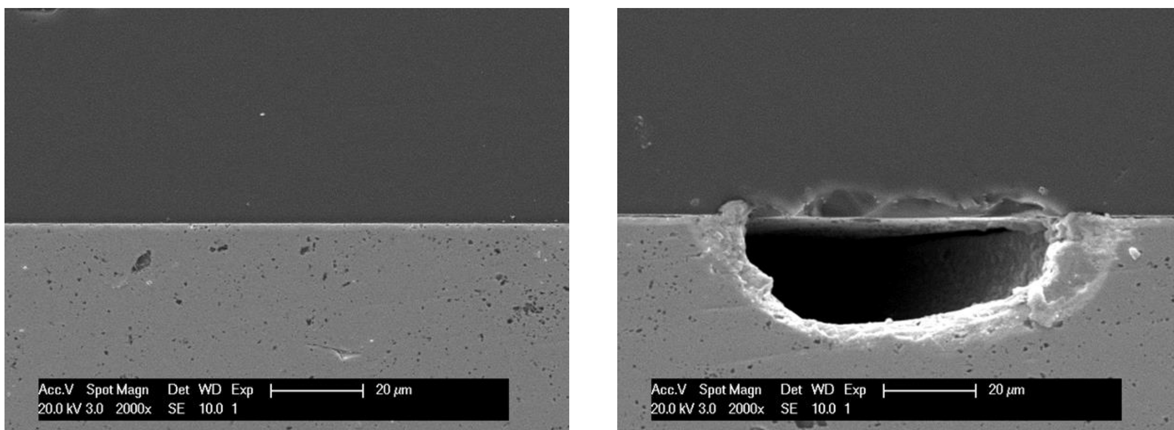


Fig. 7.6 The cross-sectional SEM image of a bonded sample (a) A bonded region without trenches at 2000× magnification (b) A bonded region with a trench at 2000× magnification

The Si chip was then bonded to Cu substrates with trenches using solid-state bonding process same at 300 °C with the pressure of 6.89 MPa (1,000 psi) for 3 min. The bonding area is approximately 19.7 mm^2 by subtracting the area of trenches and the hole at center from the total area of the Si chip. As can be seen in Fig. 7.6, the cross-sectional SEM images of the bonded sample, the Si chip is well bonded to the Cu substrate. It is also observed that, in Figs. 7.6(a) and 7.6(b), no voids and gaps are generated at the bonding interface without trenches and at the

bonding interface with trenches. Additionally, there are no cracks or breaks within the Si chip. It was suspected that the cracks or breaks could form during the heating and cooling processes due to the considerable CTE mismatch between Si and Cu. Table 7.2 lists the typical CTE values of the materials. The capping Ag layer of 1 μm is too thin to be able to manage the large CTE mismatch, inasmuch as Cu has larger expansion or contraction than Si when they are bonded to each other. How can the Si chip withstand the thermal stress while it cools down from the bonding temperature to room temperature, from 300 °C to 25 °C? The etching pattern is designed to address the resulting stress. On the Si/Cu bonding interface, the trenches provide free space for Cu and Si to deform without restriction. Therefore, we could say that the trenches inside the Cu substrate release the part of thermal stress from the CTE mismatch to strengthen the bond.

A simple shear test was performed on one bonded sample to evaluate the bond strength in our laboratory, as shown in Fig. 7.7 [7]. Surprisingly, the Si chip is broken rather than being sheared off. Fig. 7.8 exhibits the photo of the broken Si chip after the simple shear test. This result indicates that the bond between the Si chip and the Cu substrate is stronger than the Si chip itself. Therefore, the concern regarding the bond strength is eliminated.

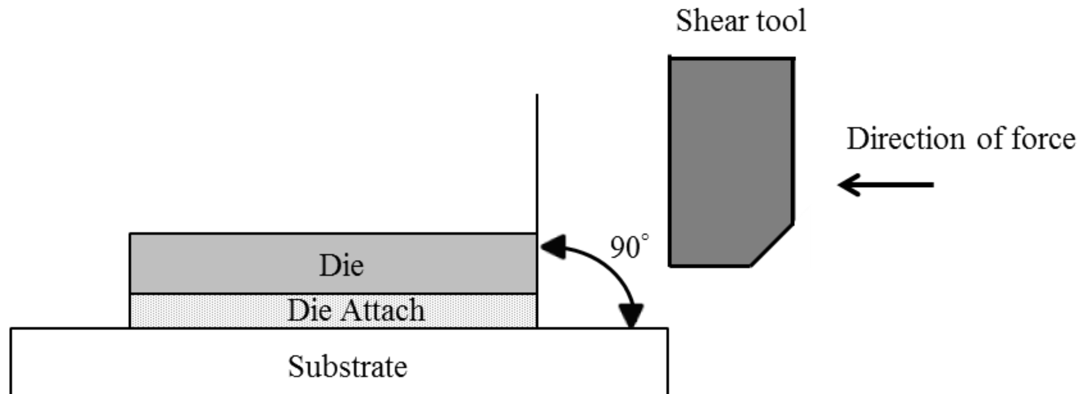


Fig. 7.7 Die shear test

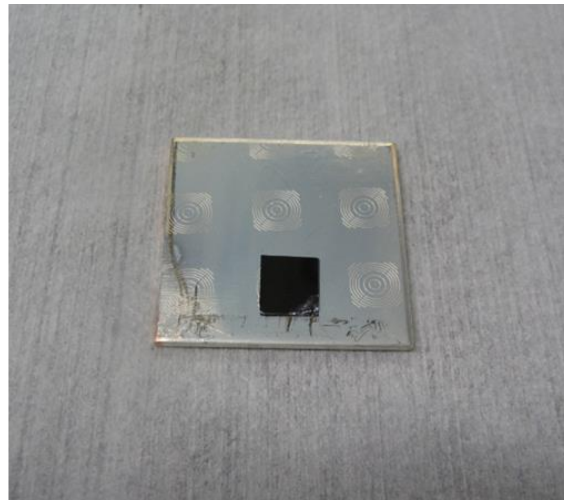


Fig. 7.8 The broken Si chip still bonded to the Cu substrate after the simple shear test

7.4 Summary

In this work, we have successfully developed a solid-state bonding process of bonding Si chips to Cu substrate using the patterned design directly. The Cu substrates were etched first to

produce the trench pattern, followed by thin layer of Ag (1 μm) to prevent Cu from oxidation. Si chips were deposited with thin Cr (30nm) and Au (100nm) using E-beam evaporation in high vacuum environment. The Si chip was placed over Cu substrate and bonded at 300°C for 3 min using solid-state bonding process in vacuum. There is no specific joint used in between the Si chip and the patterned Cu substrate. The resulting joints are examined by optical microscope and SEM. Both the cross-sectional images show that the Si chips are well bonded to the Cu substrates without visible voids and cracks. The simple shear tests are conducted to evaluate the bond strength, while the Si chips are all broken first. It certified that this bonding structure is stronger than the Si chip itself. This process provides a new method to bond Si chips to patterned Cu substrates without specific joints that may expand the scope of bonding design in electronic packaging.

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Chapter Eight

Design and Fabrication of Silver Solid Solution Layers on Silicon and Silicon Carbide Chips and Subsequent Solid-State Bonding to Cu Substrate

8.1 Introduction – Si Chips

The major functions of an electronic package are to provide interconnections of integrated circuits (ICs) to form electrical system, mechanical fixation, excellent heat dissipation, and protection to electronic components in harsh environments. With reasonable price, superior electrical and thermal conductivities, and excellent mechanical properties, silver (Ag) is a promising material according to the above viewpoints. However, Ag still has its own weaknesses despite advantages, which can actually or potentially lead to failure. That is Ag can be tarnished not only when exposed to certain corrosive gases such as hydrogen sulfide or sulfur gas but also under normal atmospheric conditions for a long period of time [1]-[3]. The challenge is what kind of materials can expand applications for Ag.

Indium has a relatively low yield strength of 310 psi (2.1 MPa), only one-tenth that of Sn-3.5Ag eutectic solders. Also, its low melting temperature of 157 °C is 61 °C lower than that of

Sn-Ag-Cu (SAC) ternary eutectic solders [4]. Low yield strength and low processing temperature make In become a possible solution.

Ag solid solution with indium is further studied while Ag-In binary system has been demonstrated with an exceptional anti-tarnish property. In this study, firstly, the authors have successfully developed Ag-rich Ag-In solid solution joints between Si chips and Cu substrates. Based on phase diagram, the melting range for Ag-rich Ag-In solid solution is from 670 °C to 962 °C, depending on In composition. This indicates that the bonding joints can sustain high operating temperatures. Cross-sectional SEM images show that the bonding joints on Si chips are well bonded to the Cu substrates without visible voids and cracks. Importantly, this displays that the Ag-rich Ag-In solid solution can deal with the large mismatch in coefficient of thermal expansion between semiconductors, such as Si (3 ppm/°C) and Cu (17 ppm/°C) [5]. The chemical compositions are determined by SEM/EDX. From the SEM/EDX analysis, the bonding joints are identified as Ag-rich Ag-In solid solution. The bonding results are encouraging.

Since the need for high temperature applications continue to grow, silicon carbide (SiC) is chosen as a bonding chip due to its excellent properties. After many experiments are performed, the authors finally successfully developed an Ag-rich Ag-In solid solution layer on SiC chips. These chips are then bonded to Cu substrates using the solid-state bonding process.

The chemical compositions are acquired by SEM/EDX as above. The simple shear test is conducted to determine the bond strength for the practical applications.

In what follows, the experimental design and procedures are first presented. Experimental results are then reported. Finally, a summary is given.

8.2 Experimental Design and Procedures – Si Chips

In the experiments, 2-inch (50.8 mm) Si wafers are deposited 30 nm chromium (Cr) and 100 nm Au via electron beam evaporation system in a high vacuum, 2×10^{-6} Torr. The Si wafers are then diced into 8 mm × 8 mm pieces to be ready for plating. The 15 μm thick Ag, the bottom Ag layer, is plated onto the Si chip. The Ag plating process is conducted at 10 mA/cm^2 at room temperature with gentle stirring in the cyanide-free and weak alkaline Ag plating solution at the operating pH around 8 [6]. In order to coarsen the size of Ag grains, the initial annealing step is carried out at 350 °C for 5 h in air, since the reaction rate between Ag and In is strongly related to the microstructure of Ag layer [7]-[8]. It is also worth noting that the thermal process is the trade-off between annealing time and annealing temperature. A higher annealing temperature coupled with shorter time might have the same effect to the lower annealing temperature coupled with a longer time [9]-[10]. After the initial annealing, 4 μm In and 3 μm Ag layers are sequentially plated onto Si chip at room temperature. The In plating process is conducted at 22

mA/cm^2 at room temperature with gentle stirring in the sulfamate indium plating solution in the pH range from 1 to 3.5 [11]. The 3 μm thin Ag, the top Ag layer, is used as a capping layer to avoid the surface oxidation of In.

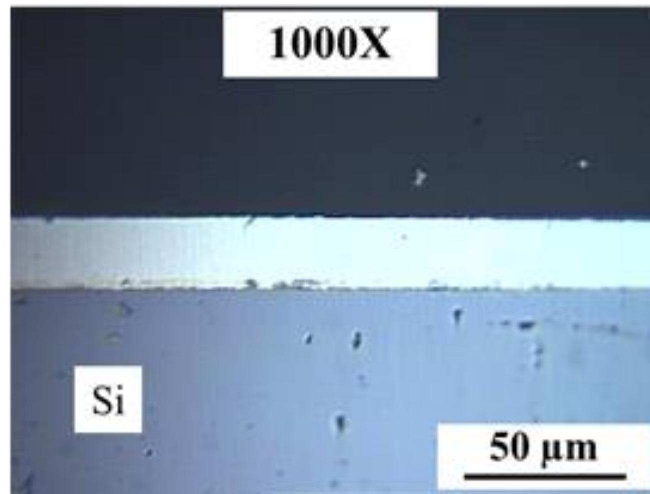


Fig. 8.1 Cross-sectional OM image of Ag layer after electroplating 50 min

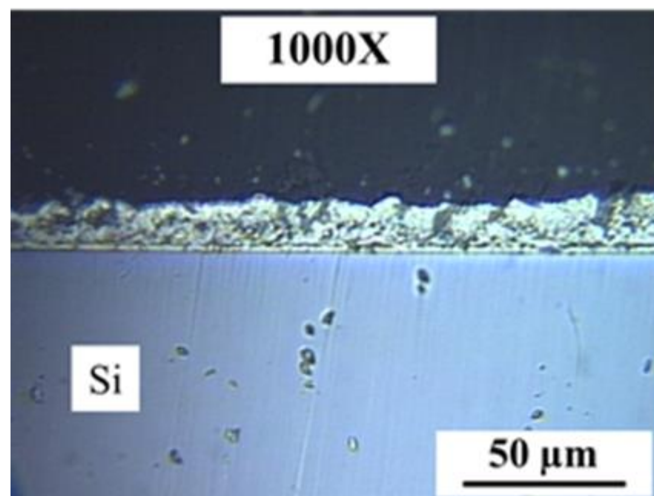


Fig. 8.2 Cross-sectional OM image of In layer after electroplating 30 min

To obtain the accurate thickness by electroplating is essential. Fig. 8.1 shows the Ag thickness of approximately 22 μm on top of a Si chip deposited Cr(30 nm)/Au(100 nm), after electroplating 50 min. Fig. 8.2 presents the In thickness of approximately 13 μm on top of a Si chip deposited Cr(30 nm)/Au(100 nm), after electroplating 30 min.

Next, the electroplating Ag(15 μm)/In(4 μm)/Ag(3 μm) multilayers on Si chips are put inside of a 6 inch quartz tube. That is sealed under vacuum by hydrogen-oxygen torch operation. The following two-step annealing process is first performed at 180 °C for 5 h in the annealing furnace and followed by heating at higher temperature up to 350 °C for 5 h. The Si chips are now ready for the solid-state bonding to the Cu substrates.

The 10 mm × 10 mm Cu substrates are cut from a 0.8 mm think Cu sheet having 99.9% purity with mirror-like finish on one side. All Cu substrates are slightly polished to remove the Cu oxides and contamination before the solid-state bonding. The assembly is to fix the position of samples on the heating graphite platform with a static pressure in a vacuum chamber [12]. Both of the Si chip and Cu substrate are held together by a fixture with static pressure of 800 psi (5.5 MPa). The platform is then heated to 300 °C with a dwell time of 30 min, and the bonding temperature is monitored using a miniature thermocouple. After that, the vacuum chamber cools down naturally to room temperature.

To evaluate the quality, the resulting samples are mounted in epoxy-resin, cut in halves,

and polished for the cross-sectional study by scanning electron microscope (SEM) and optical microscope (OM). The microstructures of samples are examined by SEM. SEM/EDX analysis is used to determine the chemical positions and possible intermetallic compounds.

8.3 Experimental Results and Discussion – Si Chips

8.3.1 Phase diagram and intermetallics

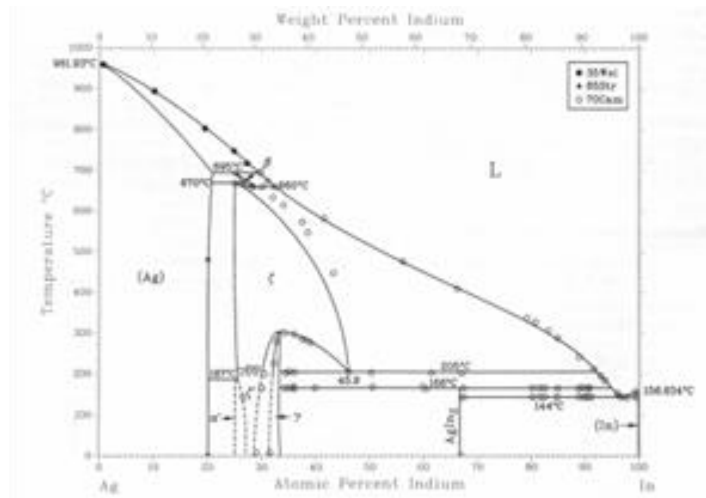
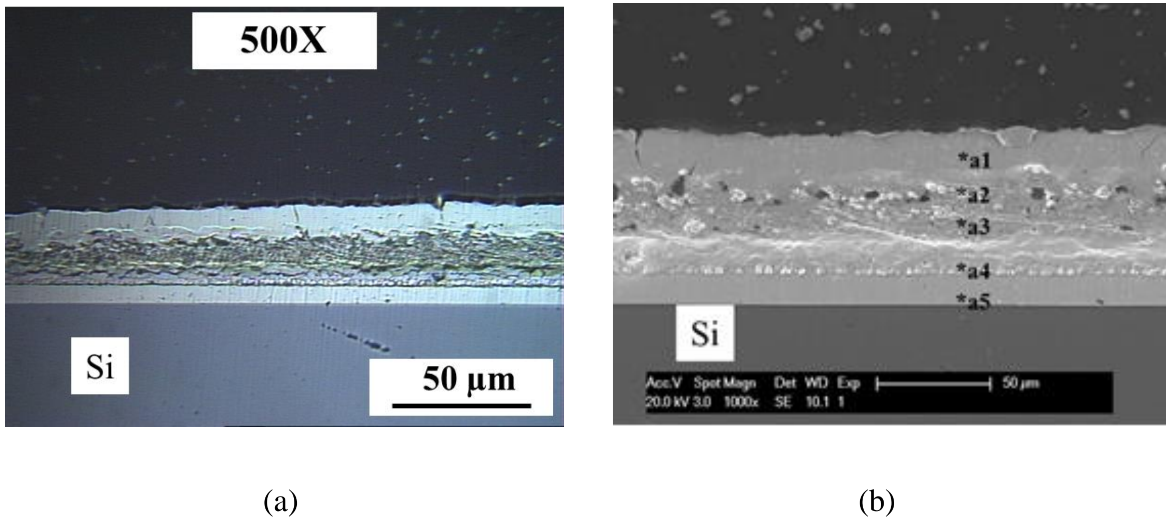


Fig. 8.3 Ag-In phase diagram [13]

In order to elaborate the fabrication of Ag solid solution with In, it is vital to briefly review the Ag-In binary system and its intermetallic compounds. The Ag-In phase diagram is shown in Fig. 8.3. Two solid solution phases, (Ag) and (In), are found on the diagram. For (In) phase, the maximum solubility of Ag atoms in In crystal lattice is less than 1 at.% at room

temperature, which is extremely limited. For (Ag) phase, the maximum solubility of In atoms in Ag crystal lattice is 20 at.% at room temperature. This phase has a solidus temperature range of 670 °C to 962 °C, which makes it especially attractive as a high temperature stable binary alloy.



(a) (b)

Fig. 8.4 Cross-sectional images of Ag-In binary system after two weeks at room temperature (a) OM image (b) SEM image

Table 8.1 EDX analysis data on the cross-section of Ag-In binary system after two weeks at room temperature

Layer on Fig.8.4(b)	Composition (at.%)	Corresponding Phases
a1	Ag:100	Ag
a2	Ag:67-100, In:0-33	(Ag) + Ag_2In
a3	Ag:0-33, In:100-67	$AgIn_2$ + (In) + In
a4	Ag:67-100, In:0-33	(Ag) + Ag_2In
a5	Ag:100	Ag

There are two identified intermetallic compounds (IMC), $AgIn_2$ and Ag_2In on the diagram. Both $AgIn_2$ and Ag_2In are formed at room temperature after the electroplating process, when Ag and In are intimate contact to each other [14]. That is demonstrated in Fig.8.4. Fig. 8.4(a) and Fig. 8.4(b) show the cross-sectional images after electroplating Ag(25 μm)/In(15 μm)/Ag(25 μm) multilayers. Each layer of Ag-In alloys can be clearly distinguished. SEM/EDX analysis also confirms the compositions of each layer. Table 8.1 lists the compositions of Ag and In and corresponding phases at locations a1-a5 marked in Fig. 8.4(b). Importantly, $AgIn_2$ and Ag In begin to decompose at 166 °C and at 312 °C, respectively. Thus, the annealing temperatures of 180 °C and 350 °C are chosen to decompose $AgIn_2$ and Ag_2In.

8.3.2 Structure design I: Si/Cr/Au/Ag/In/Ag without initial annealing on the bottom Ag layer & with following 2-step annealing in air

In the first design, the Ag(15 μm)/In(7 μm)/Ag(15 μm) multilayers are consecutively electroplated on Si chip. There is no initial annealing on the bottom Ag layer before plating In/Ag layers. After the electroplating process, the following two-step annealing process is performed at 180 °C for 10 minutes and 350 °C for 5 h, respectively.

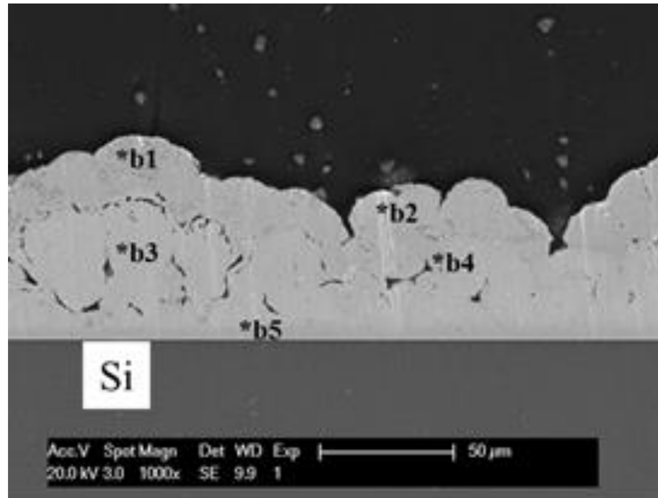


Fig. 8.5 For design I, cross-sectional SEM image of Ag-In binary system when the annealing process is completed

Table 8.2 For design I, EDX analysis data on the cross-section of Ag-In binary system when the annealing process is completed

Points on Fig.8.5	Composition (at.%)	Corresponding Phases
b1	Ag:100	Ag
b2	Ag:100	Ag
b3	Ag:67-88, In:12-33	(Ag) + Ag_3In_2 + Ag_2In
b4	Ag:67-88, In:12-33	(Ag) + Ag_3In_2 + Ag_2In
b5	Ag:67-88, In:12-33	(Ag) + Ag_3In_2 + Ag_2In

The cross-sectional image is first examined when the following two-step annealing process is completed. Surprisingly, the scallop-like morphology of IMC (Fig. 8.5) is generated. Table 8.2 lists the compositions of Ag and In and corresponding phases at locations b1-b5

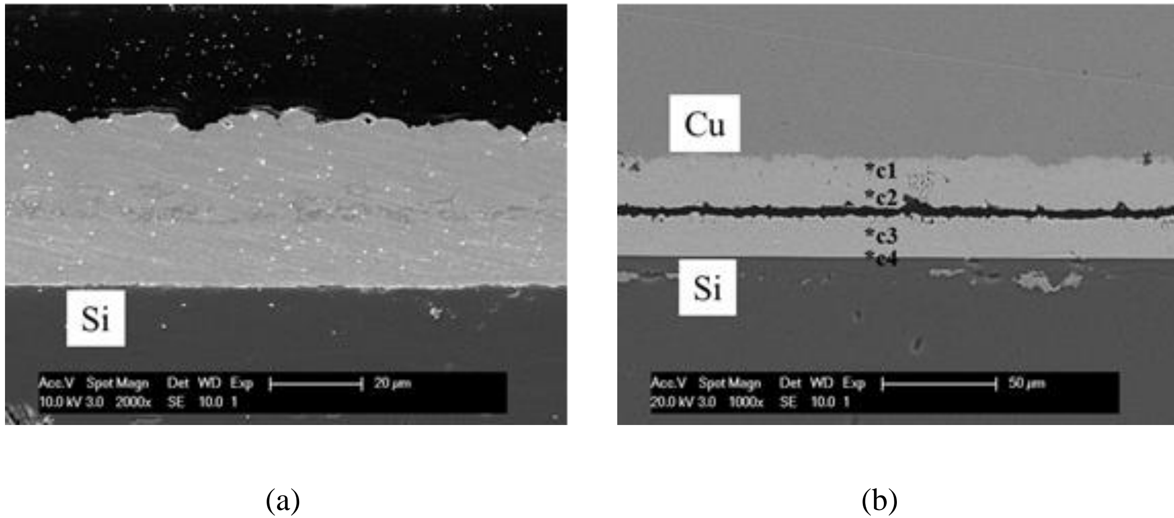
marked in Fig. 8.5. According to the reports from other group, scallop IMCs are often seen in In-Ag, Sn-Cu, and Sn-Ag binary systems. Possibly, the molten (L) phase and $AgIn_2$ do have enough time to react with pure Ag. Thus, the scallop-like $AgIn_2$ still largely remains after annealing at 180 °C and this morphology gradually forms during the following two-step annealing process. It could be said that to prolong annealing time at 180 °C may be essential.

8.3.3 Structure design II: Si/Cr/Au/Ag/In/Ag without initial annealing on the bottom Ag layer & with extension time of following 2-step annealing in air

In the second design, the Ag(15 μm)/In(7 μm)/Ag(15 μm) multilayers are also consecutively electroplated on Si chip. Similarly, there is no initial annealing on the bottom Ag layer before plating In/Ag layers. After the electroplating process, the following two-step annealing process is performed at 180 °C for 5 h and 350 °C for 5 h, respectively. The difference between design I and design II is to prolong the annealing time from 10 min to 5 h at 180 °C.

Fig. 6(a) is the SEM cross-sectional image when the following two-step annealing process of design II is completed. It seems that the resulting layer is ready to be bonded to the Cu chip. However, the bonding result is not as expected. Fig. 8.6(b) is the cross-sectional SEM image of a bonded sample. Table 8.3 lists the compositions of Ag and In and corresponding phases at locations c1-c5 marked in Fig. 8.6(b). Possibly, during the annealing process, there is

no enough (L) phase to fill the voids and gaps or some oxygen is trapped inside the Ag-In alloys. Therefore, the bonding joints are not strong enough and it breaks at the weakest point. It could be said that to obtain more (L) phase and to be in a vacuum environment may be essential.



(a) (b)

Fig. 8.6 For design II, cross-sectional SEM image of Ag-In binary system (a) before the solid-state bonding process (b) after the solid-state bonding process

Table 8.3 For design II, EDX analysis data on the cross-section of Ag-In binary system after the solid-state bonding process

Points on Fig.8.6(b)	Composition (at.%)	Corresponding Phases
c1	Ag:96-98, In:2-4	(Ag)
c2	Ag:94-96, In:4-6	(Ag)
c3	Ag:69-82, In:18-31	(Ag) + Ag_3In + Ag_2In
c4	Ag:82-84, In:16-18	(Ag)

8.3.4 Structure design III: Si/Cr/Au/Ag/In/Ag with initial annealing on the bottom Ag layer & with extension time of following 2-step annealing in vacuum

In the third design, the thicknesses of the upper two layers of Ag/In/Ag are reduced. That is considered to be able to enhance the uniformity of the resulting Ag-In layer. It is worthwhile to note that the Ag(15 μm)/In(4 μm)/Ag(3 μm) multilayers are not consecutively electroplated on Si chip. The intial annealing step is carried out in between. The 15 μm thick Ag is annealed at 350 °C for 5 h in air to coarsen the size of Ag grains from 30 nm to 1~2 μm, inasmuch as the reaction rate between Ag and In is subject to the microstructure of Ag layer [7]. Ag with small grains results in rapid growth rate of $AgIn_2$ through grain boundary diffusion. The increased grain size slows down the $AgIn_2$ growth rate due to reduced grain boundaries. Consequently, the (L) phase stays at the molten state with sufficient time to fill the gaps and voids during the reaction. After the initial annealing process, 4 μm In and 3 μm Ag layers are sequentially plated onto Si chip. That is sealed inside of a quartz tube under vacuum to perform the following two-step annealing process at 180 °C and 350 °C, respectively. By the whole process above, most AgIn2 and Ag2In is expected to be decomposed in the system. Fig. 8.7 is the SEM cross-sectional image of the resulting layer.

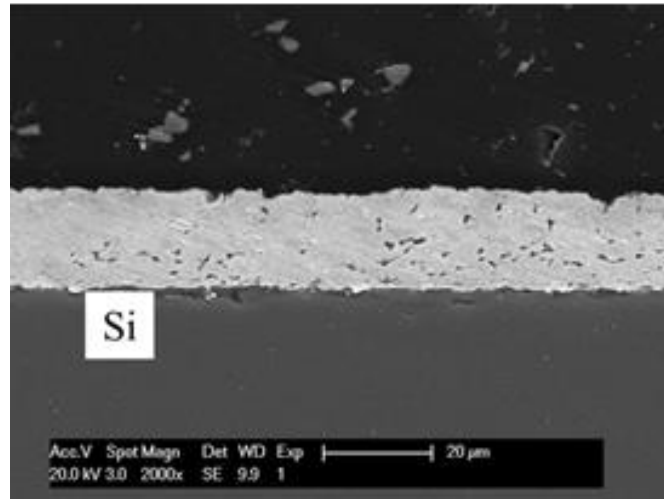


Fig. 8.7 For design III, cross-sectional SEM image of Ag-In binary system, before the solid-state bonding process

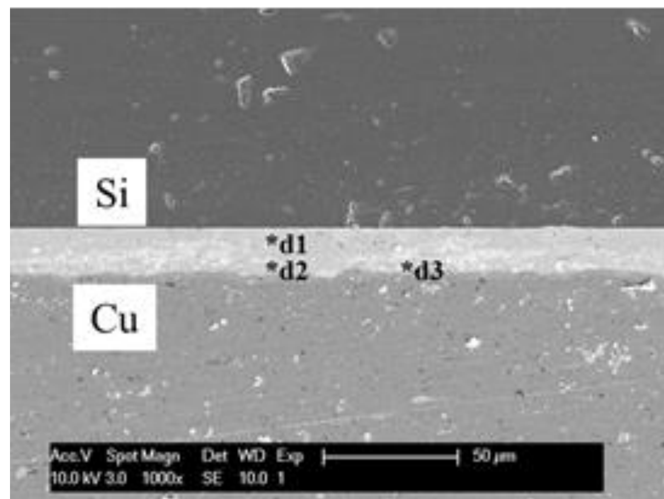


Fig. 8.8 For design III, cross-sectional SEM image of Ag-In binary system, after the solid-state bonding process

The Si chip are then bonded to Cu substrate at 300 °C with 800 psi (5.5 MPa) pressure in 0.1 torr vacuum for 30 min. The cross-sectional SEM image shows that the Ag-In solid solution

joints on Si chips are well bonded to the Cu substrates without visible voids and cracks, as shown in Fig. 8.8. Table 8.4 lists the compositions of Ag and In and corresponding phases at locations d1-d3 marked in Fig. 8.8. According to the SEM/EDX analysis, the compositions of bonded joints are homogeneous Ag-rich Ag-In solid solution.

Table 8.4 For design III, EDX analysis data on the cross-section of Ag-In binary system after the solid-state bonding process

Points on Fig.8.8	Composition (at.%)	Corresponding Phases
d1	Ag:81-83, In:17-19	(Ag)
d2	Ag:80-81, In:19-20	(Ag)
d3	Ag:80-82, In:18-20	(Ag)

8.4 Conclusions – Si Chips

This paper presents a novel method of electroplating Ag(15 μm)/In(4 μm)/Ag(3 μm) multilayers on the Si chips to fabricate Ag-In alloys. Importantly, the bottom Ag layer is initially annealed at 350 °C to increase its grain sizes and to reduce grain boundaries, inasmuch as the reaction rate between Ag and In is subject to the microstructure of Ag layer. Afterwards, the In/Ag layers are sequentially plated onto Si chip. In order to decompose $AgIn_2$ and Ag_2In, the following two-step annealing process is performed in a vacuum environment at 180 °C and 350 °C, respectively. The resulting Ag-In alloys made on Si chips are then bonded to Cu

substrate at 300 °C with 800 psi (5.5 MPa) pressure in 0.1 torr vacuum for 30 min, by introducing the solid-state bonding process. That requires only a single stage operation at low bonding temperature and pressure without any molten phase involved. The quality of bonding joints is examined by SEM. No voids and gaps are observed at the bonding interface. The compositions of resulting joints are measured by SEM/EDX, which is a homogeneous Ag-rich Ag-In solid solution.

This unique Ag-rich Ag-In solid solution is showing the anti-tarnish ability, having melting temperatures exceeding 670 °C, and capable of managing large CTE mismatch. This novel method may bring a chance to utilize the Ag-In binary system for those who need die-attach materials for high operating temperatures under severe environmental conditions in industries.

8.5 Experimental Design and Procedures – SiC Chips

In the experiments, 2-inch (50.8 mm) SiC wafers are deposited 30 nm chromium (Cr) and 100 nm Au via electron beam evaporation system in a high vacuum, 2×10^{-6} Torr. The Cr layer acts as an adhesion layer. The Au layer not only protects Cr from oxidation when exposed to air, but also functions as a seed layer for the electroplating process. The Si wafers are then diced into 8 mm × 8 mm pieces to be ready for plating. The 19 μm thick Ag, the bottom Ag layer, is plated

onto the SiC chip. The Ag plating process is conducted at 10 mA/cm^2 at room temperature with gentle stirring in the cyanide-free and weak alkaline Ag plating solution at the operating pH around 8 [6]. The reaction rate between Ag and In is strongly related to the microstructure of Ag layer once In is plated on the Ag layer [7]-[8]. In order to slow their reaction rate, the initial annealing method is carried out at 300 °C for 5 h in air to coarsen the size of Ag grains. It is also worth noting that the thermal process is the trade-off between annealing time and annealing temperature. A higher anneal temperature coupled with shorter time might have the same effect to the lower temperature coupled with a longer time [9]-[10]. After the initial annealing, 4 μm In and 1 μm Ag layers are sequentially plated onto SiC chip at room temperature. The In plating process is conducted at 22 mA/cm^2 at room temperature with gentle stirring in the sulfamate indium plating solution in the pH range from 1 to 3.5 [11]. The 1 μm thin Ag, the top Ag layer, is used as a capping layer to avoid the surface oxidation of In. Next, the electroplating Ag(19 μm)/In(4 μm)/Ag(1 μm) multi-layers on SiC chips are put inside of a 6 inch quartz tube. That is sealed under vacuum by hydrogen-oxygen torch operation. The two-step annealing method, annealing at low temperature before annealing at high temperature, is first performed at 180 °C for 5 h in the annealing furnace and followed by heating at higher temperature up to 350 °C for 15 h. By this two-step process, a mixture of Ag-In alloys, mainly composed of Ag_3In and (Ag)-xxIn solid solution, is expected to obtain. Surprisingly, EDX data show that the resulting film is

a single phase (Ag)-xxIn solid solution. Thus, the SiC chips are now ready for the solid-state bonding to the Cu substrates. The 10 mm × 10 mm Cu substrates are cut from a 0.8 mm think Cu sheet having 99.9% purity with mirror-like finish on one side. All Cu substrates are slightly polished to remove the Cu oxides and contamination before the solid-state bonding. The assembly is to fix the position of samples on the heating graphite platform with a static pressure in a vacuum chamber [12]. To achieve the solid-state bonding, the SiC chip is placed face-down on the Cu substrate. The bonding pressure is applied on the backside of Si chip. Both of the SiC chip and Cu substrate are held together by a fixture with static pressure of 1000 psi (6.9 MPa) to ensure intimate contact. The bonding pressure is controlled by the spring-loaded mechanism. The platform is then heated to 300 °C with a dwell time of 15 min, and the bonding temperature is monitored using a miniature thermocouple. The electrical power applied to the heater of the graphite platform is shut down when the temperature reaches 300 °C. After that, the vacuum chamber cools down naturally to room temperature.

To evaluate the bonding quality, the resulting samples are mounted in epoxy-resin, cut in halves, and polished for the cross-sectional study by scanning electron microscope (SEM) and optical microscope (OM). The microstructures of samples are first examined by SEM. The scanning electron microscope with energy-dispersive X-ray (SEM/EDX) analysis are then used

to determine the chemical compositions and possible intermetallic compounds. Finally, the simple shear test is conducted to determine the bond strength and observe fracture modes.

8.6 Experimental Results and Discussion – SiC Chips

In this design, the thicknesses of the upper two layers of Ag/In/Ag are reduced. That is considered to be able to enhance the uniformity of the resulting Ag-In layer. The purpose is to make a single phase layer, (Ag)-xxIn solid solution, before performing the soild-state bonding process. It is worthwhile to note that the Ag(19 μm)/In(4 μm)/Ag(1 μm) multilayers are not consecutively electroplated on Si chip. The initial annealing step is carried out in between. The 19 μm thick Ag is annealed at 300 °C for 5 h in air to coarsen the size of Ag grains from 30 nm to 1~2 μm, inasmuch as the reaction rate between Ag and In is subject to the microstructure of Ag layer [7]. Ag with small grains have rapid growth rate of $AgIn_2$ through grain boundary diffusion, which tend to result in many voids and gaps inside the layer. Only the small amount In left because In is consumed rapidly. Therefore, the remaining In is not enough to fill the gaps and voids. On the contrary, the increased grain size slows down the $AgIn_2$ growth rate due to reduced grain boundaries. Consequently, the (L) phase stays at the molten state with sufficient time to fill the gaps and voids during the reaction.

After the initial annealing process, 4 μm In and 1 μm Ag layers are sequentially plated onto Si chip. That is sealed inside of a quartz tube under vacuum to perform the following two-step annealing process at 180 °C and 350 °C, respectively. By the whole process above, most $AgIn_2$ and Ag_2In are expected to be decomposed in the system. Fig. 8.9 is the OM cross-sectional image of the resulting layer. Fig. 8.10 is the SEM cross-sectional image of the resulting layer with EDX data, which demonstrate that it is a single phase (Ag)-10In solid solution layer. Table 8.5 lists the compositions of Ag and In and corresponding phases at locations e1-e5 marked in Fig. 8.10.

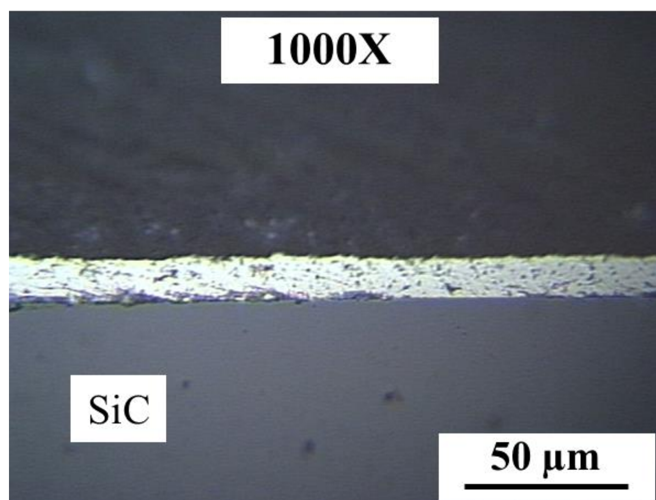


Fig. 8.9 The cross-sectional OM image of Ag-In binary system, after the 2-step annealing process

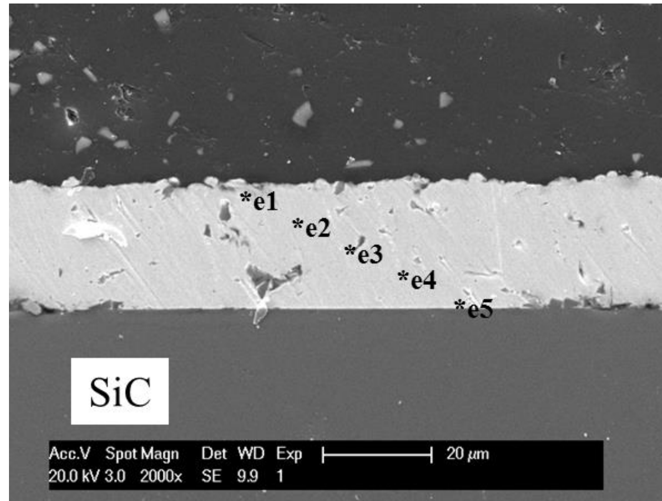
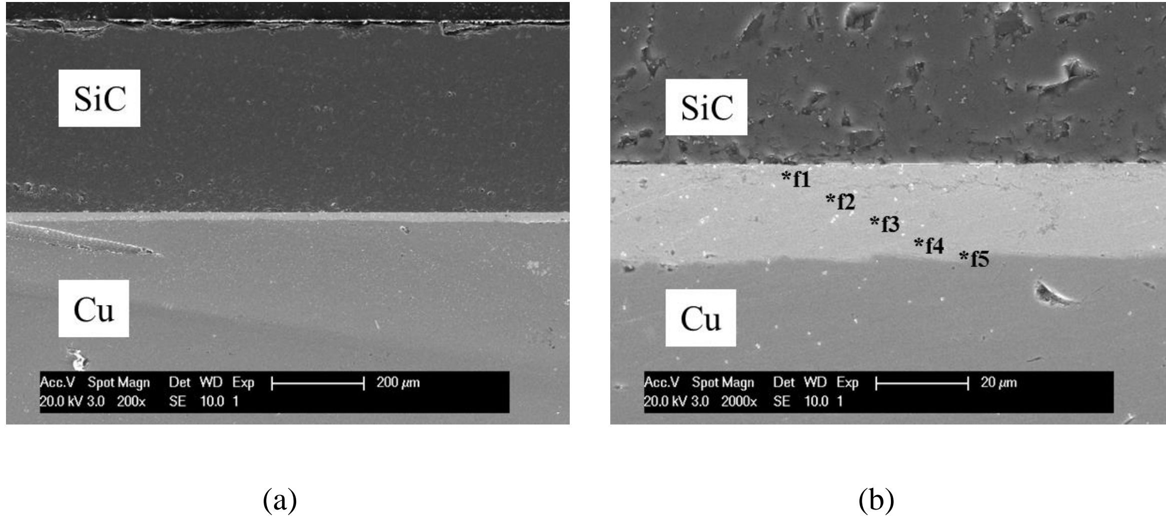


Fig. 8.10 The cross-sectional SEM image of Ag-In binary system with EDX analysis, after the 2-step annealing process

Table 8.5 EDX analysis data on the cross-section of Ag-In binary system after the 2-step annealing process

Points on Fig. 8.10	Composition (at.%)	Corresponding Phase
e1	Ag:89.5, In:10.5	(Ag)
e2	Ag:90.7, In:9.3	(Ag)
e3	Ag:91.4, In:8.6	(Ag)
e4	Ag:90.6, In:9.4	(Ag)
e5	Ag:90.1, In:9.9	(Ag)



(a) (b)

Fig. 8.11 The cross-sectional SEM image of Ag-In binary system (a) 200× magnification (b) 2000× magnification

Table 8.6 EDX analysis data on the cross-section of Ag-In binary system after the solid-state bonding process

Points on Fig. 8.11 (b)	Composition (at.%)	Corresponding Phase
f1	Ag:90.6, In:9.4	(Ag)
f2	Ag:90.3, In:9.7	(Ag)
f3	Ag:90.6, In:9.4	(Ag)
f4	Ag:89, In:11.0	(Ag)
f5	Ag:91.1, In:8.9	(Ag)

The Si chip are then bonded to Cu substrate at 300 °C with 1000 psi (6.9 MPa) pressure in 0.1 torr vacuum for 15 min. The cross-sectional SEM image shows that the Ag-10In solid solution joints on SiC chips are well bonded to the Cu substrates without visible voids and

cracks, as shown in Fig. 8.11. It presents that the Ag-10In can deform to deal with the surface roughness and formed an intimate bond firmly. Table 8.6 lists the compositions of Ag and In and corresponding phases at locations f1-f5 marked in Fig. 8.11. According to the SEM/EDX analysis, the compositions of bonded joints are the homogeneous Ag-rich Ag-In solid solution.

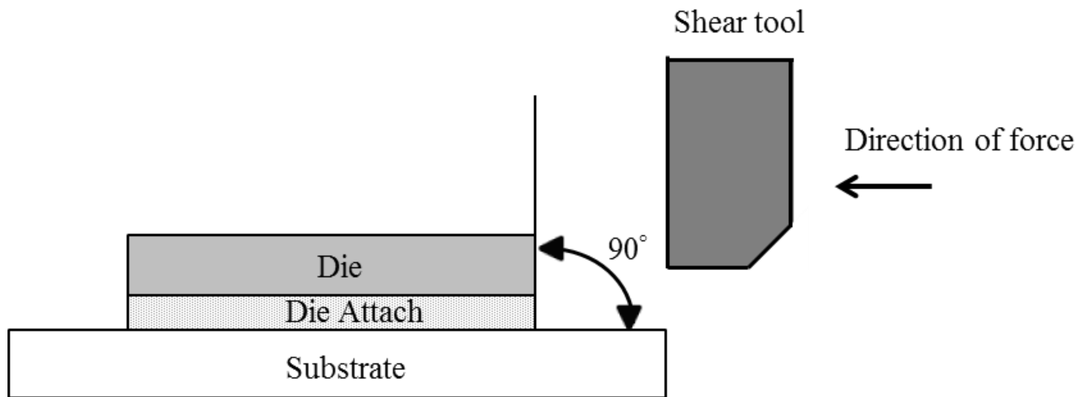


Fig. 8.12 Die shear test

A simple shear test was performed on one bonded sample to estimate the bond strength, as shown in Fig. 8.12 [15]. The fracture modes and surfaces were observed. Fig. 8.13 exhibits the photo of the SiC chip that was sheared off. This sample broke at three interfaces, including SiC-Cr E-beam evaporating interface, inside Ag-10In joints, and Ag-10In-Cu bonding interface. It clearly shows numerous Ag-10In traces that still bonded to the Cu substrate after the shear test. The Ag-10In traces on the Cu substrate prove that the bonding joints are stronger than E-beam

evaporating interface. Therefore, the unique Ag-10In material may bring a chance for practical applications.

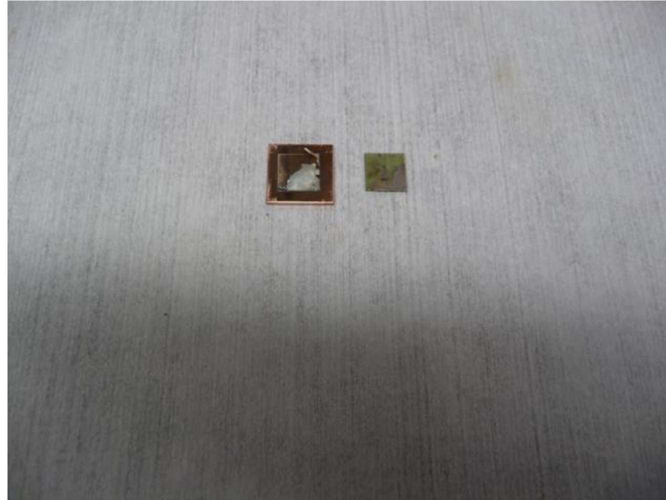


Fig. 8.13 The bonded sample was sheared off

8.7 Conclusions – SiC Chips

Ag solid solution with In is further studied since Ag-In binary system has been demonstrated with an extraordinary anti-tarnish property and superior mechanical properties, such as malleability, strength, and ductility. How to fabricate that kind of bonding materials at relative low temperatures is a challenge. In this paper, the unique Ag-In solid solution joints are produced successfully between SiC chips and Cu substrates. The Ag(19 μm)/In(4 μm)/Ag(1 μm) multilayers are electroplated on SiC chips. In order to control the reaction rate between Ag and

In during the electroplating step, the 19 μm Ag layer is initially annealed at 300 °C to increase its grain size and electroplated the following In(4 μm)/Ag(1 μm) layers at room temperature. A two-step annealing process is followed in a vacuum environment at 180 °C and 350 °C, respectively. These two different annealing temperatures are chosen to decompose $AgIn_2$ and Ag_2In. After the annealing process, the Ag-In alloys made on Si chips are then bonded to Cu substrate at 300 °C with 1000 psi (6.95 MPa) pressure in 0.1 torr vacuum for 15 min. Cross-sectional scanning electron microscopic (SEM) images show that the Ag-In solid solution joints on Si chips are well bonded to the Cu substrates without visible voids and cracks. The scanning electron microscope with energy-dispersive X-ray (SEM/EDX) analysis studies the composition of bonding joints, which displays the homogeneous bonding layer structure. The melting range for Ag-rich Ag-In solid solution is from 670 °C to 962 °C, depending on In composition. Thus, the bonding joints are expected to exhibit impressive performance at high temperatures. This novel method may bring a chance to utilize the Ag-In binary system for those who need die-attach materials for high operating temperatures under severe environmental conditions.

Acknowledgement

The authors greatly appreciated the support and encouragement from II-VI Foundation.

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Chapter Nine

Conclusions

Due to increasing numbers of integrated functions per chip, the needs of die attach materials and techniques for high performance electronic devices have continued to grow. To address such challenges, the metal bonding is considered to be a possible solution. In this dissertation, the purpose is to produce a robust bond between the chips to metal substrates without forming voids and gaps on the bonding interfaces at relatively low processing temperatures, which could be used for high temperature and high power electronic devices. To achieve this objective, solid-state bonding technology is employed for various bonding designs. All details are reported in previous chapters, including experimental designs, procedures, results, and discussions. In this chapter, the clear and concise conclusions will be presented.

9.1 Silver Joints and Patterned Silver Joints

Both Cu and Ag have been studied extensively for electrical conductor applications due to reasonable prices and excellent properties. To expand the applications, Ag layer was used as a bonding medium between two Cu pieces. The upper piece is called chip and the lower one is the substrate. Two bonding designs were successfully developed. For the first design, 50 μm Ag

layer was initially plated on the Cu substrate and annealed at 400 °C for 5 h to increase Ag grain sizes, thereby making it easier to deform during bonding. The Cu chip was then placed on the Cu substrate and bonded at 300 °C with 6.89 MPa (1,000 psi) pressure for 3 min. The photolithographic process is not required, since there is no pattern. For the second design, 10 μm Ag layer was plated on the substrate. Another 5 μm Ag with 50 × 50 array of cavities with 50 μm in diameter was added. The fundamental concept is to release the thermal induced stress by creating cavities in the Ag layer to allow easier plastic deformation for the bonding medium. The Cu chip was bonded to the substrate with the same conditions as the first design. No annealing process was used. Note that in the first design the electroplating Ag layer is not able to bond to Cu chips without the annealing step at the same bonding condition. The percentage of the Ag layer that is strongly bonded in the second design is 22%, which is higher than that 8% in the first design.

For both designs, no molten phase was involved and no flux was used. Cross-sectional images of bonded samples show no visible voids or gaps on Cu/Ag and Ag/Cu interfaces. The shear test results of 10 samples show both Ag joints are strongly bonded and far exceed MIL-STD-883J method 2019.9. It eliminates a concern of bonding strength from industries for practical applications. Based on phase diagram, typically, Ag joints with Cu do not contain any intermetallic compound (IMC). Compared with solder joints used in industries, most of

reliability issues associated with IMC and IMC growth do not exist. In this work, the bonded structure consists of only Cu/Ag/Cu, which has the 780 °C eutectic temperature of the Ag-Cu binary system. In addition, both Cu and Ag have relatively high electrical/thermal conductivities and superior mechanical properties. This bonding structure may be applied to electronic devices that high thermal performance or high operating temperature is required.

9.2 Silver-Assisted Copper Wire Bonding

Solid-state processes of bonding 1 mm Cu wires on Cu substrates and Si chips, respectively, were developed. To overcome Cu oxidation issue, the bonding surface on the wire was plated an Ag layer. An annealing step followed to facilitate the Ag layer easier to deform and conform to the Cu or Si bonding surfaces. The bonding process was performed at 300 °C with 6.89 MPa (1,000 psi) for 3 min. Wire-bond cross sections were studied using optical and electron microscopy. The images obtained exhibit nearly perfect Ag-Cu bonding interface. For wire-bonds made on Cu substrate, in-plane pull test measures a breaking of force 20.7 to 23.7 kg, comparable to the 22.5 kg breaking force of the Cu wire itself. The breaking forces on vertical pull test are about one-half of in-plane pull test results. For wire-bonds made on Si chip, breaking forces are about 80% of those made on Cu substrate. Fracture modes were evaluated in details.

90% of the wire-bonds broke with three modes mixed together: near Cu-Ag plating interface, inside Ag layer, and Ag-Cu bonding interface. Thus, the bonding interface is as strong as other regions of the wire-bond.

Fundamental research on process development has always been some distance away from production. For the wire bonding process reported here, it is practically possible for the industry to turn it in production if the industry is willing to invest in and develop the equipment needed. The path to production is outlined below: a) shape the end of Cu wires into the geometry needed, b) plate the bonding surface of Cu wires with Ag and anneal the Cu wires, c) design and build a machine with a bonding head that grabs the end of the Cu wires, heat it, and press it onto the bond pad is already preheated. This solid-state wire bonding process is expected to have valuable applications in high power and high temperature devices and modules where the wire-bonds have to stand alone without protection due to lack of high temperature molding compound and reinforcing materials.

9.3 Silicon Chips Directly Bond to Pattered Copper Substrate

In this work, we have successfully developed a solid-state bonding process of bonding Si chips to Cu substrate using the patterned design directly. The Cu substrates were etched first to produce the trench pattern, followed by thin layer of Ag (1 μm) to prevent Cu from oxidation. Si

chips were deposited with thin Cr (30nm) and Au (100nm) using E-beam evaporation in high vacuum environment. The Si chip was placed over Cu substrate and bonded at 300°C for 3 min using solid-state bonding process in vacuum. There is no specific joint used in between the Si chip and the patterned Cu substrate. The cross-sectional images show that the Si chips are well bonded to the Cu substrates without visible voids and cracks. The simple shear tests are conducted to evaluate the bond strength, while the Si chips are all broken first. Clearly, this bonding structure is stronger than the Si chip itself. It also demonstrates that the robust bond could deal with the large CTE mismatch between Si (3 ppm/°C) and Cu (17 ppm/°C). This process provides a new method to bond Si chips to patterned Cu substrates without specific joints that may expand the scope of bonding design in electronic packaging.

9.4 Silver-Indium Joints

Ag solid solution with In is further studied since Ag-In binary system has been demonstrated with an extraordinary anti-tarnish property and superior mechanical properties, such as malleability, strength, and ductility. In this work, the unique Ag-In solid solution joints are produced successfully between Si chips and Cu substrates. The Ag(15 μm)/In(4 μm)/Ag(3 μm) multilayers are electroplated on Si chips. In order to control the reaction rate between Ag and In during the electroplating step, the 15 μm Ag layer is initially annealed at 350 °C and

electroplated the following In(4 μm)/Ag(3 μm) layers at room temperature. The initial annealing step carried out in between is to increase its grain sizes and to reduce grain boundaries, inasmuch as the reaction rate between Ag and In is subject to the microstructure of Ag layer. A two-step annealing process is followed in a vacuum environment at 180 °C and 350 °C, respectively. These two different annealing temperatures are chosen to decompose $AgIn_2$ and Ag_2In. Since the need for high temperature applications continue to grow, silicon carbide (SiC) is also chosen as a bonding chip due to its excellent properties. The Ag(19 μm)/In(4 μm)/Ag(1 μm) multilayers are electroplated on SiC chips to facilitate the uniformity.

After the annealing process, the Ag-In alloys made on Si and SiC chips are then bonded to Cu substrate using solid-state bonding process. That requires only a single stage operation at low bonding temperature and pressure without any molten phase and flux involved. Cross-sectional images show that the Ag-In solid solution joints on Si and SiC chips are well bonded to the Cu substrates without visible voids and cracks. The SEM/EDX analysis studies the composition of bonding joints, which displays the homogeneous bonding layer structure. This unique Ag-rich Ag-In solid solution is showing the anti-tarnish ability, having melting temperature exceeding 670 °C, and capable of managing large CTE mismatch. Thus, the bonding joints are expected to exhibit impressive performance at high temperatures. This novel method may bring a chance to

utilize the Ag-In binary system for those who need die-attach materials for high operating temperatures under severe environmental conditions.