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Frequency synthesis using concurrency: Reaching a solution to a few classical and hard headed RF and mm-wave integrated circuit problems

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A dissertation submitted in partial satisfaction

Of the requirements for the degree Doctor of Philosophy

In Electrical Engineering

By

Alborz Jooyaie

2012

ABSTRACT OF THE DISSERTATION

Frequency synthesis using concurrency:

Reaching a solution to a few classical and hard headed RF and mm-wave integrated circuit problems

by

Alborz Jooyaie

Doctor of Philosophy in Electrical Engineering

University of California, Los Angeles, 2012

Professor Mau-Chung Frank Chang, chair

The goal of achieving a multi-band, multi-standard and globally connected, as well as a self-healing or reconfigurable smart radio that can optimize its performance in different circumstances and situations in order to maintain a high performance yield and reliability, has imposed many requirements on the frequency synthesizer unit of the transceiver system, hence the oscillator. One significant requirement is the frequency tuning, which is being pursued by various schemes in the lower GHz regime (below the Ku band). However, there is a growing interest in transceiver design applications in the higher GHz bands using similar ideas. For example, there is the unlicensed 57-64 GHz band and the three licensed bands of 71-76 GHz, 81-

86 GHz, and 92-95 GHz applicable for wide-band short range wireless communication and point-to-point fixed wireless communication, such as last-mile access, respectively. Wireless chip-to-chip communication is another field where multi-band and concurrent frequency generation is of interest.

A technique to achieve ultra-wideband continuous frequency generation is introduced. It is based on orthogonal E-wall and H-wall tuning of distributed resonators, in standing wave mode configurations. The tuning scheme in fact serves dual purposes for generating concurrent tones as well as wide-band tuning operation. It is scalable and could be applied to any frequency band, but since it is designed around distributed resonators, it is more desirable for higher frequencies. In comparison with alternative methods, the technique requires less silicon space, lower power consumption, better phase noise, as well as a wider tuning range. A V-Band VCO, with a continuous tuning range from 58 GHz to 76.2 GHz, designed and validated in 65-nm CMOS technology, in accordance with this technique is illustrated, and a new figure of merit (FoM) is reported.

A novel technique is introduced for extending the frequency pulling range in circuits employing injection locking. It relies on the concurrent resonant frequencies that could co-exist in a concurrent oscillator, each of which being orthogonal to each other, and individually perturbed. Thus, the technique relaxes the classical constraint of limited tuning/locking range in injection locked circuits. A distributed, standing wave, divider-by-two is designed and fabricated, illustrating the idea. The divider measures a continuous locking range of greater than 20 GHz, without using any varactor, and establishes a new figure of merit. The idea is scalable and applicable to injection locking circuits at any frequencies, in particular, varying modulus division/multiplication

The dissertation of Alborz Jooyaie is approved

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2012

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Acknowledgement

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Second I thank my advisor, Prof. M.F. Chang for his continuous support, both scientifically and financially. He always guided me through the loop holes and cracks with his wisdom and experience. I hope one day I could help others like myself the way he did.

Vita

Education

- **B.Sc**, Electrical Engineering, University of Toronto, Toronto, Canada (June 2005)
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- **Texas Instruments**, *wireless R&D group*, Internship, Dallas, Texas (June 2006 – Sept. 2006)
    - **Design Engineer**, design of novel low noise front end circuit building blocks (Mixer and VCO for 2.4 GHz ISM) to reduce flicker noise degradation in nano-meter CMOS.
- **Texas Instruments**, *wireless R&D group*, Internship, Dallas, Texas (Jan. 2007 – Sept. 2007)
    - **Design Engineer**, design of novel wireless system architectures (2.4 GHz ISM) with the goal of merging front end blocks functionality and thus bringing the ADC closer to the antenna, thus improving multi-functionality while reducing the cost.
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Publications

- **A. Jooyaie,** M. F. Chang, "A V-band voltage controlled oscillator with greater than 18 GHz of continuous tuning-range based on orthogonal E-mode and H-mode control", IEEE RFIC 2011, June 2011
- **A. Jooyaie,** M. F. Chang, "Orthogonal E-mode and H-mode tuning of distributed resonators: using concurrency for continuous ultra-wideband frequency generation", *Invited*, IEEE MTT Transactions, Dec. 2011.

- C. Wang, A. Badmaev, **A. Jooyaie,** M. Bao, K. L. Wang, K. Galatsis, C. Zhou, "Radio frequency and linearity performance of transistors using high purity semiconducting carbon nanotubes", ACS Nano, April 2011.
- **A. Jooyaie,** M. F. Chang, "Ultra-wideband band injection locked dividers based on concurrency principle", *to be submitted to IEEE RFIC 2012.*

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- **UCLA Teaching Assistant Conference,** panelist (2009)
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Chapter 1: Introduction

Multi-band and multi-standard transceivers have gained an accelerated interest in both industry and academia; with industry focusing on the already existing infrastructures (such as WiFi and GPS) and academia focusing on emerging technology (such as WiMAX and 60 GHz short range gigabit wireless transmission). The primary goal is to integrate as much functionality into a given silicon real state as possible and in this way plan for a re-configurable system that in addition to being able to function as single radio with single standard with high yield (under any condition), it is also able merge the functionality of multiple different radios (each with its own specific goal) into a single package and create an all-in-one multiple-radio-systems on chip. The ultimate goal is to create the sleeker product for the end-users.

At the heart of any transceiver lives the frequency synthesizer/phase locked loop, which is in charge of setting the reference communication tones, as well as synchronization of the received signal with that of the locally produced clock. In multi-band/multi-standard systems, the synthesizer will also have to be a multi-band design.

In the millimeter wave (mm-wave) regime (such as V-band and E-band) challenges are the same, but much more complicated than in the lower frequency. Many techniques that work in the low frequency analog/digital domain don't cut it anymore simply because many factors that were considered un-important (such as the small routing parasitic) have now become of utmost importance. Therefore, along with the vast

potentials of the emerging multi-gigabit wireless communication, comes the need for longer and much stringent R&D time and effort. This research is aimed at studying and designing frequency synthesizers, and novel techniques, for this multi-standard/multi-band/multi-gigabit mm-wave radio system era. In the following sections of this introductory chapter the significance and application of such frequency synthesizer in emerging products is highlighted, along with an introduction to the operation of the frequency synthesizer, pin-pointing the bottleneck elements and the ones investigated in this research.

1.1. The Frequency Spectrum and the Potentials

Different mm-wave frequency bands have been historically referred to by abbreviations, so that each frequency range is designated with the corresponding letter name. Figure 1, summarizes the lettering, to ease the future reference to each particular band, as well as the common application as assigned by the FCC.

Band	Frequency range	Applications
L	1 to 2 GHz	Satellite, navigation (GPS, etc.), cellular phones
S	2 to 4 GHz	Satellite, SiriusXM radio, unlicensed (Wi-Fi, Bluetooth, etc.), cellular phones
C	4 to 8 GHz	Satellite, microwave relay
X	8 to 12 GHz	Radar
K_u	12 to 18 GHz	Satellite TV, police radar
K	18 to 26.5 GHz	Microwave backhaul
K_a	26.5 to 40 GHz	Microwave backhaul
Q	30 to 50 GHz	Microwave backhaul
U	40 to 60 GHz	Experimental, radar
V	50 to 75 GHz	New WLAN, 802.11ad/WiGig
E	60 to 90 GHz	Microwave backhaul
W	75 to 110 GHz	Automotive radar
F	90 to 140 GHz	Experimental, radar
D	110 to 170 GHz	Experimental, radar

Figure 1, mm-wave frequency band lettering, and range, by FCC

The V-band and E-band have recently attracted much attention due to the potential of wideband and high date-rate communication. As wireless transmission uses air as the medium, atmospheric absorption characteristics are of much significance and determine the range of radio wave propagation. Figure 2 depicts the absorption properties in different frequency bands.

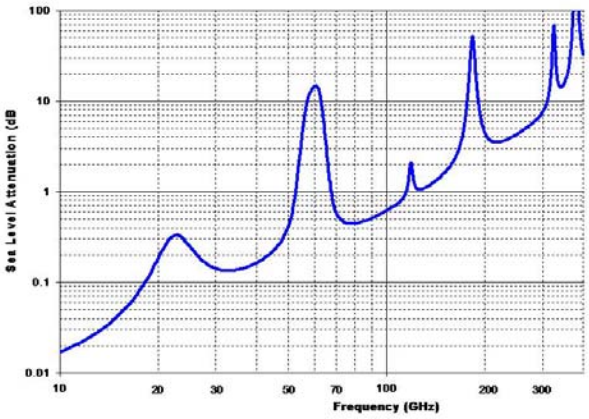


Figure 2, atmospheric attenuation and absorption vs. frequency [1]

The 57-66 GHz band suffers from a greater absorption factor, is identified as a license free ISM (Industrial-Scientific-Medical) band, and is good for short range communications. As a result the spectral design requirements, such as dynamic range and blocker levels/adjacent channel power emission, for the systems designed in the 57-66 GHz are relaxed significantly. The 70 and 80 GHz bands, on the other hand, don't have the atmospheric absorption problem and are consequently useful for long range (point to point) communication and are thus licensed. The focus and application of the 60, 70 and 80 GHz bands, as reserved by the FCC are further expanded in Figure 3. In the following sections, the potential applications and emerging market for each of these bands is further elaborated on.

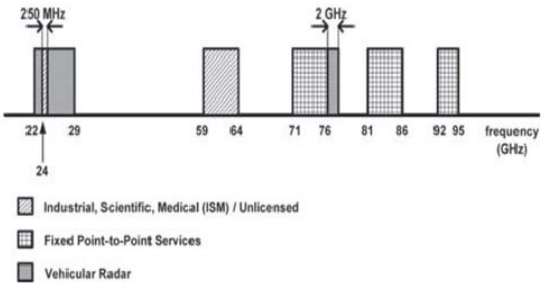


Figure 3, available gigabit wireless transmission bands and their applications, FCC [3]

1.2. Gigabit Wireless Personal Area Network (WPAN)

The potential of gigabit wireless communication and the possibility of being able to transfer high definition media and large data packet sizes over the large bandwidths enabled by the ISM band in the 57-66 GHz have attracted much attention. Because of the limited communication distance in this band, owing to the high atmospheric absorption, the requirements on the channel density, and the competition of demand over available communication bandwidth and resource is relaxed, and large channels could be dedicated to information transmission. Moreover, the specifications on the dynamic range and its deterioration because of the adjacent channels or blocker levels are significantly relaxed. Of course one should keep in mind that in this frequency range, and with the current available technologies, high power emission levels are hard to produce at the first place, in comparison to the lower GHz frequency range. The 57-66 GHz band is further broken down to four channels, of each 2.16 GHz in bandwidth, including the spacers, over the 9 GHz range. Figure 4, illustrates the abundance of bandwidth at the 57-66 GHz band, in

comparison with the limitations in the more common wireless communication bands in the lower GHz frequency range.

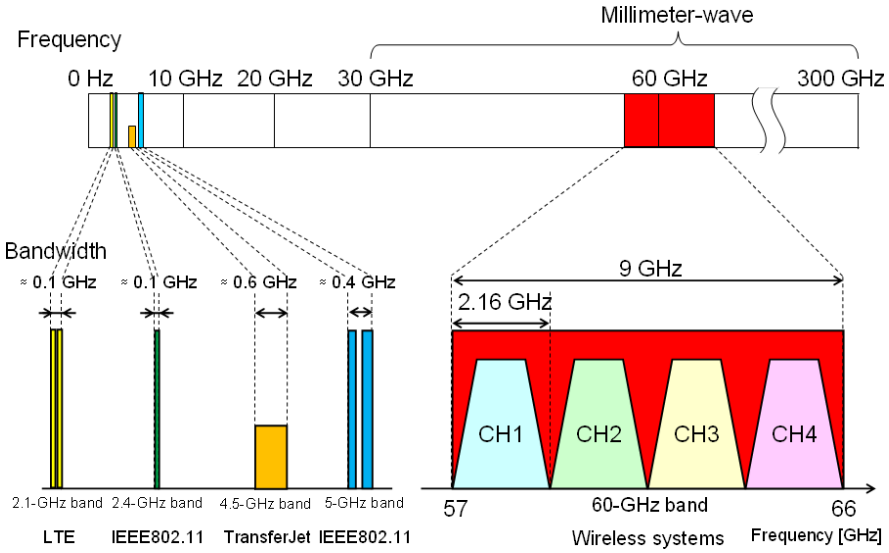


Figure 4, the 60GHz ISM channel bandwidth vs. lower GHz [2]

With the wide bandwidth afforded by the 57-66 GHz, high definition connectivity products are possible, where essentially any information could be transmitted or received amongst various mobile devices, from cell-phones to TV, to personal computers, and to other gaming or entertainments devices. The dream of global wireless connectivity a`mongst one's personal devices and perhaps those of others is visualized in Figure 5.

Figure 5, the multi-gigabit wireless connectivity and the WPAN [4]

The synthesizer unit driving the transceiver unit should be able to synthesize a wideband width signal, from 57 to 66 GHz, continuously, while having a high fabrication yield. Given the variations in the semiconductor manufacturability, it is important that the synthesizer performs, meets the specifications, and is immune to the so called 3 sigma variations over the PVT (Process, Voltage, Temperature) corners. Consequently, the nominal synthesizer design should cover slightly more than the range of 57-66 GHz in order to have enough safety margins. Furthermore, as could be observed the wireless multi-gigabit connectivity, WPAN, in the 57-66 GHz band is highly directional. This mandates the use of beam forming and phase-array techniques, where different phases of spectrum are transmitted spatially from an antenna array to make the beam pattern unidirectional, otherwise the loss would be significant, particularly due to multi-path. As a result the frequency synthesizers is required to be able to generate the phase diversity needed for the phase array operation. There are alternative methods of generating this phase diversity, using passive networks; however, their loss tends to be detrimental thus

degrading both the phase noise and mismatch in amplitude. In the sections that follows the various requirements on the frequency synthesizer, as applied in the case of a WPAN system, are further analyzed and the bottleneck building blocks in the frequency synthesizer are highlighted.

1.3. Long Distance, Point-to-Point Communication

Fiber-optics is common place for backhaul of high data rate communication, where the fiber channels are usually dug under the ground or over the tower. Fiber-optics carry the information to the local servers or hosts and from then on the distribution is branched down to regular coaxial cable, which is of a much more limited bandwidth, and of lower data carrying capability. The problem of last mile fiber is classical and is posing as much more challenging as information transmission requirement is increasing, and there are more demands for the high data rate, high definition information transmission. Moreover, wherever there is the need for new hosts or servers, new fiber optic lines have to be constructed and routed to the location, which adds additional over head time for construction, along with costs and feasibility issues. In this way, fiber optics is not very a very scalable approach. A wireless approach could resolve many of these issues. The incorporation of multi-gigabit wideband wireless is a possible resolution, which is also very scalable, without the need for any special constructions. The requirement here, of course, is that the wireless signal should be able to travel long distance with minimal degradation, atmospheric absorption, and where mandated with as few relaying stations as possible. The idea is presented pictorially in Figure 6.

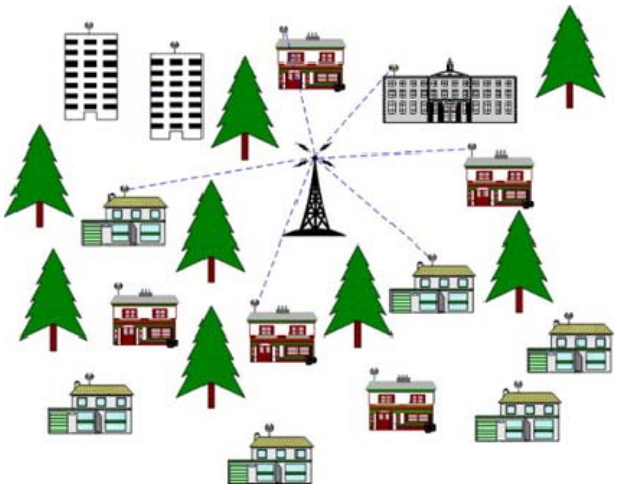


Figure 6, wireless gigabit distribution, broad range networking

As discussed previously, the 71-76 GHz and the 81-86 GHz bands, referred to as the E-bands, are attenuated to a very limited degree over distance, owing to the atmospheric absorption profile and properties. However, the communication is still very directional, requiring special directional antennas that are calibrated relative to the precise location of the transmitting and receiving antennas. Another advantage of the E-band is that since it is restricted, FCC has strict control over the spectrum utilization and thus it is almost free of any jammers or disturbing artifacts that could degrade signal quality; all-in-all, this enables a scalable multi-gigabit information transmission infra-structure, which is also cost effective. The deployment of E-band could potentially resolve the last mile fiber conundrum, as illustrated in Figure 7, where only a base station is required to be equipped with fiber optic, and the other server-lets could be connected via the E-band wireless link, and additional hosts could be added via wireless connectivity of the E-band where needed in a very cost effective manner. Moreover, in future, the E-band receivers could be brought closer to the consumers and homes for end user applications, to satisfy the hunger for higher information data rate.

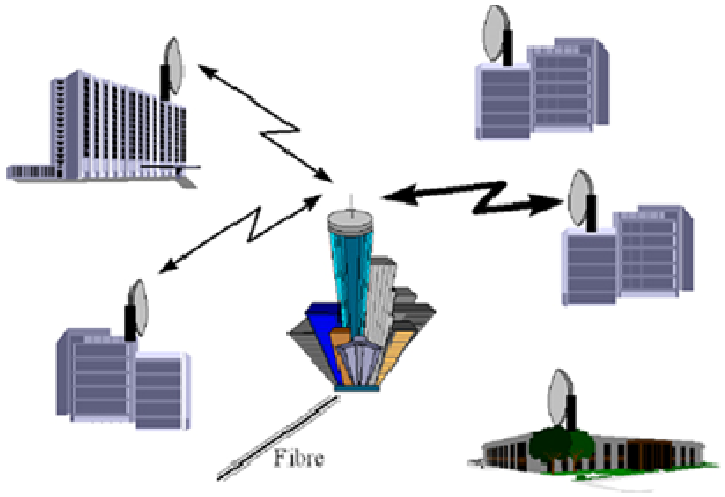


Figure 7, last mile fiber and deployment of E-band wireless communication [5]

The benefits of the E-band communications, as presented and boasted by the E-band Communications Corporation, are summarized in Figure 8. One of the required circuit blocks for the E-band system is a dual band wideband frequency synthesizer for the 71-76 GHz and the 81-86 GHz frequency bands. The trade-offs and challenges to design of such synthesizer, along with the bottleneck building blocks are discussed in the following sections.

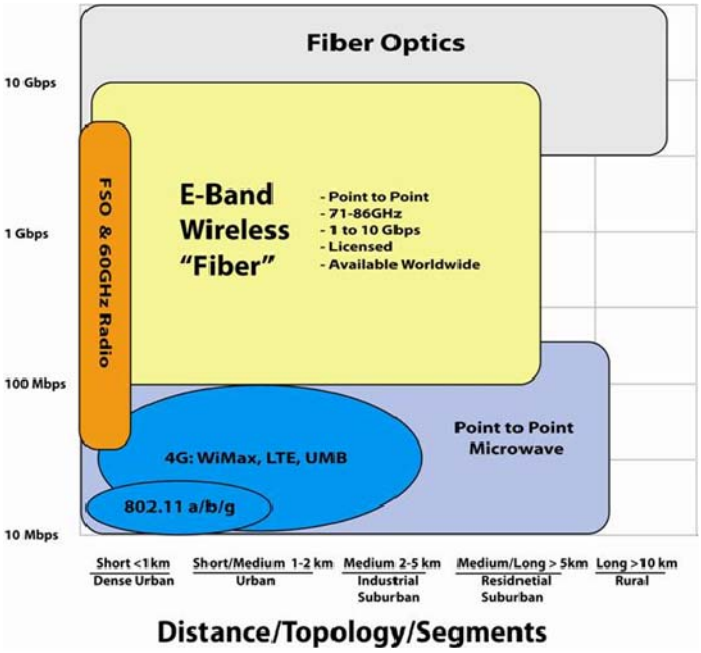


Figure 8, E-band gigabit wireless communication landscape [6]

1.4 Wireless/RF Interconnect

High speed networking and communication is challenging, especially at gigabit rates, in both micro-meter and kilo-meter dimensions. In order to improve computation power and efficiency while keeping the power consumption low multi-threading and multi-core processing is becoming the new strategy amongst powerful microprocessor designers. The challenge is to be able to route information amongst the cores, while minimizing the routing overhead requirements. As the number of cores increases, the amount of data bus for interconnects increases exponentially. Furthermore, cross-talk and coupling amongst the high speed data buses poses a major difficulty. Wireless/RF interconnect a promising solution to the multi-core computing. Particularly, the multi-gigabit bandwidth available at such small scales in the gigahertz frequencies, a much

efficient interconnecting could be deployed. The idea is to use multi-carriers, in a multi-band wireless transmission setting. This way enough isolation amongst neighboring cores and data busses is enforced, and the cross-talk and coupling due to routing is minimized. The idea is presented pictorially in Figure 9 [7]. As illustrated, various channels' data modulates different carriers that are widely spaced apart, and the resulting multi-carrier signal is transmitted via a single transmission medium, illustrated as a single transmission line. In this system, the frequency synthesizer is a bottleneck building block. While the other blocks and the modulation could be very simple to implement, the frequency synthesizer is the challenging component due to the fact that not only it should be able to generate multiple carriers, but the carriers should be also sufficiently separable and controllable in the frequency domain. A concurrent frequency synthesizer is of particular benefit here, in which each of the concurrent tones is separately tune-able and the tones are not harmonics of each other.

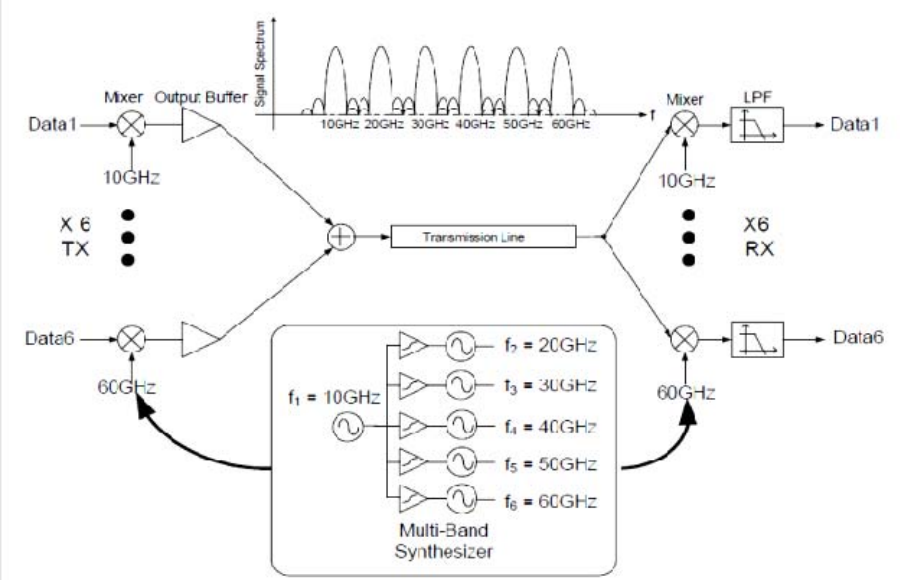


Figure 9, RF interconnect [7]

1.5. Orthogonal Frequency Division Multiplexing (OFDM)

Orthogonal Frequency Division Multiplexing (OFDM) is a recent modulation scheme that is gaining significant popularity due to its many advantages, including immunity to multi-path, use of diversity, and high data rate communication due to its high spectral efficiency. It is a multi-carrier system and its primary advantage over signal carrier scheme is the ability to cope with severe channel conditions, with the need of complex equalization. It is quite immune to inter-symbol interference (ISI), without the need of guard or spacer intervals. Moreover, it is robust against narrow-band co-channel interference. On the other hand, OFDM is very sensitive to frequency synchronization and features a high Peak to Average Ratio (PAR), thus mandating a linear power amplifier in the system level. Operation of OFDM and its multi-carrier nature are illustrated in Figure 10.

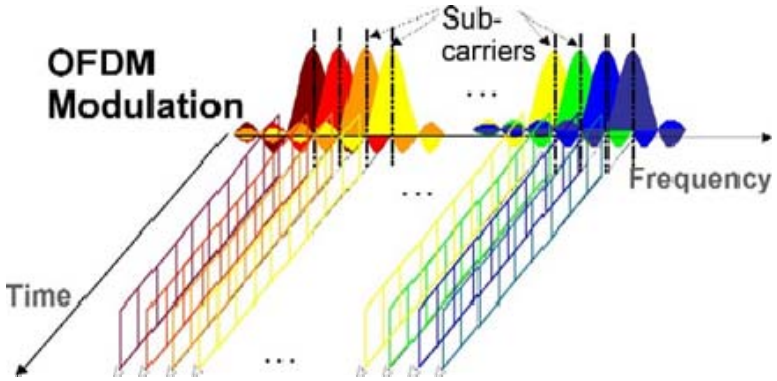


Figure 10, OFDM principle and diversity in time and frequency

OFDM has been implemented in many wireless products and the emerging market also relies on it heavily along with MIMO (Multiple Input/Multiple Output). The

cellular 4G LTE standard is based on OFDM MIMO. OFDM relies on a frequency hopper frequency synthesizer, where settling time and locking time of the frequency tones should be quick and precisely controlled. The settling time requirements for such synthesizer are on the orders of micro-seconds. As in the case of RF Interconnect, a well controlled concurrent synthesizer could be advantageous. A typical frequency planning for a frequency hopping in the 900 MHz and the 2.4 GHz ISM band are illustrated in Figure 11.

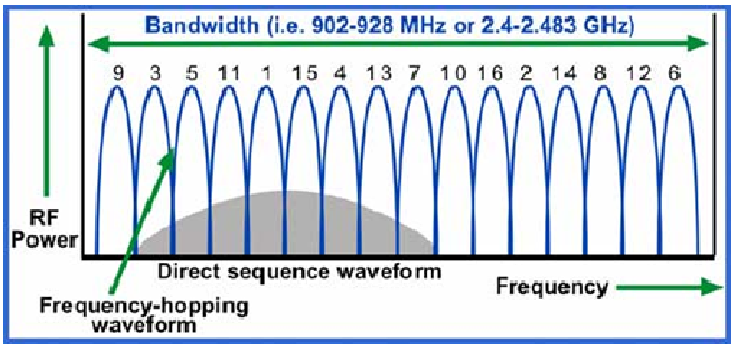


Figure 11, OFDM frequency hopping in 900 MHz and 2.4 GHz ISM [7]

1.6. CMOS Implementation and Challenges

CMOS is the technology of choice for all digital signal processing and logic applications, due to the fact that it's the best for making digital switches. Moreover the continuous feature size scaling of the CMOS is very beneficial for applications that require extreme computational and processing power, requiring many functions and millions of logic gates for their implementation; the feature size scaling allows more and more functionality squeezed in a given silicon solid state area. Furthermore, many RF building block applications, that might not necessarily use a circuit in their core

implementation, rely on digital signal processing routines and algorithms to achieve superior performance, and almost always the count of the digital transistors in an RF system exceeds the count of RF transistors. On top of all this, the microprocessor industry's aggressive push on the CMOS technology scaling and manufacturability has considerably reduced the nominal cost of circuits implemented with CMOS. On the other hand, CMOS has many disadvantages and negatives for the high performance RF design. The transistors implemented in CMOS have a low power density, along with a limited available power gain, as compared to other semiconductor technologies desirable for RF design, such as GaAs and SiGe. Also, CMOS has a low break down voltage, which couples with a relatively poor linearity performance and due to many interstitial trap densities at the oxide interface, CMOS exhibits low electron mobility and a high flicker noise corner. The low electron mobility translates into a low current cut-off frequency, f_T, as well as a low maximum power gain frequency, f_{MAX}. Moreover, due to the gate's structure (poly silicon), the finite resistance of the gate deteriorates and lowers the f_{MAX} even further. f_{MAX}, the maximum power gain frequency, also translates into maximum achievable oscillation frequency, since in an oscillator the transistor is supposed to provide active power to compensate the loss of the passive resonator elements. Certain technological advancements have improved on these figures of merit, and have increased the f_T and f_{MAX}, as illustrated in Figure 12, but nevertheless the shortcomings, as compared to the other semiconducting technologies are noticeable.

The above discussion only considered the active circuit implementation in CMOS vs. other competing semiconductor technologies. There are also the passive components, the inductor, capacitor, transformers and resistor that need to be considered for the

comparison purpose. The passive components play a major role in RF circuit blocks and play various roles such as impedance matching, to filtering, isolation, and stability improvements.

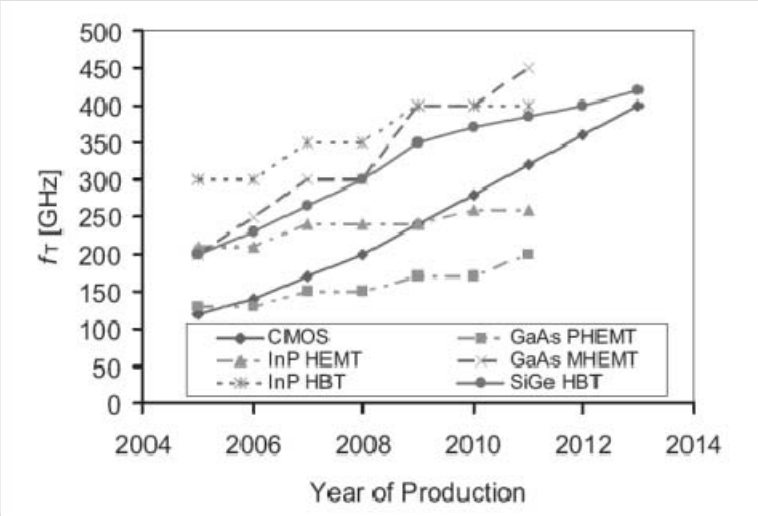


Figure 12, CMOS fT improvement in comparison with other semiconducting technologies desirable for RF performance design [3]

There are two figures of merit associated with passive elements, inductors and capacitors: the self resonance frequency (S_{RF}) and the quality factor (Q). The effective inductance and capacitance are functions of frequency, and as frequency changes the effective inductance and capacitance value change. There are always parasitic capacitance and magnetic coupling to the substrate present in any passive element, which could be modeled as shown in Figure 13 in case of an inductor. These parasitic elements result in a self resonance frequency, by resonating with the main element, be it an inductor or capacitor. S_{RF} is an undesired phenomena that happens because of the parasitic, and the less conductive (more isolating) the substrate over which the passive element is deposited

on the less the parasitic and the higher the S_{RF} is. Beyond the S_{RF} the component switches its reactance property, so that an inductor becomes a capacitor and a capacitor becomes an inductor; in a sense the S_{RF} is maximum usable frequency for the passive element.

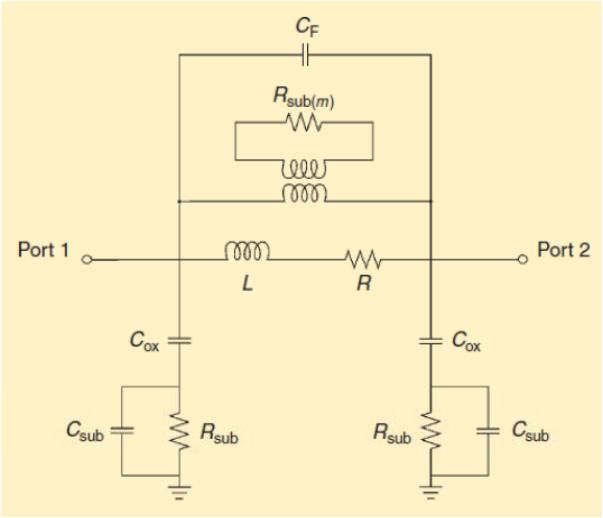


Figure 13, modeling of an inductor, illustrating the parasitic elements

Quality factor is another figure of merit for the passive elements. By the nature of the reactive elements, inductors store magnetic energy whereas capacitors store charge leading to electric field. In an ideal world, the capacitor and the inductor would hold on to their stored magnetic and electric energy indefinitely. However, because of the resistive losses involved, as illustrated in case of the inductor of Figure 13, the energy stored will be lost over time. Quality factor captures this loss, as shown in the equation below, and as expected, the higher the quality factor is the better the passive element is.

$$Q = 2\pi \frac{\text{maximum energy stored}}{\text{energy dissipated per cycle}}.$$

Once again, as expected, the quality factor of the passive element depends on the technology, the substrate and the metallization employed in implementation of the passive element. The thicker the metal is the lower the DC losses, the less conductive (more isolating) the substrate is the lower the magnetic coupling and eddy losses, and the thicker the dielectric layer is the lower the coupling capacitor and the higher the S_{RF}. There are also factor such as skin depth that govern the loss in the passive elements at higher frequencies, but these are common amongst various semiconducting technologies, and are not necessarily unique to the CMOS process.

CMOS is mainly a digital process, and it is optimized in order to serve the microprocessor and digital signal processing community. As a result, its features are those favorable by an economical digital processing scheme. To name a few of these features of the CMOS process that are highly favorable by the digital technology, but not so much by the RF community, the doping of the substrate in order to make it conductive, and the high stack of the thin metallization are emphasized. Because of the nature of the CMOS process, lateral bipolar transistors are possible in the N-well and P-well, forming NPN and PNP lateral bipolar transistors. In the normal operation these lateral transistors are to have a reverse biased junction, so that they could never conduct. However, a slight negative swing on the drain or source of a transistor could forward bias a junction, causing an exponential current flow, and a positive feedback in the lateral bipolar transistor of the wells which is termed the latch up problem. The latch up would cause a well to either hit the ground rail or the maximum permissible supply voltage rail, either of which would destroy the functionality of the block. In order to minimize the risk of latch up, the CMOS substrate is doped to be slightly conductive. By making the substrate (p-

type) slightly conductive, the positive feedback factor is reduced substantially. However, a conductive substrate is very lossy for a passive element implemented on top. As mentioned previously, and illustrated in Figure 13, the conductive substrate results in major eddy current loss, along with potential drop throughout, which would bring down both the quality factor and S_{RF} of the lump element implemented. It is important to recognize that passive elements (such as an inductor), are not really needed in a microprocessor or a DSP system, as a result this hit wouldn't cause any headache for them. It is however a major disaster for the RF blocks. CMOS has been tailored to offer options to slightly improve the scenario. For example it is possible to mask the layer underneath the inductor to be a lower doped well, so that the entire substrate will have gradients of lower doping underneath the passive element, in the hope of lowering the substrate conductance and thus improving the quality factor. Metallization is another factor where the RF designers cope with it, whereas it is in favor of the digital designers. For microprocessors, and logic implementation, it is ideal to have many metals available. Moreover, since the frequency of operation barely exceed a few GHz, the primary loss in these metals is the resistive loss, and as a result the metals are not made thick. The thicker the metal stack is the harder the deposition, which is usually done with sputtering, and the more stringent the mechanical aspects of the work such as strain and breaking/cracking of the metallization and the substrate. This is usually relaxed by chemical mechanical polishing (CMP), but the problem of making a large stack of metallization exists. In order to address this problem CMOS is once again tailored with an option of making top metals thicker, while cutting down on the number of available metals, so that the overall metallization stack height stays the same.

Even though CMOS clearly falls behind most other semiconducting technologies, especially for high performance RF applications, the economical aspects and advantages of CMOS have increased the urge amongst the RF community to adopt it, struggle with it, and design around its constraints and limitations. After all a system on chip (SOC) that encapsulates both the RF blocks and the digital signal processing blocks, is much more robust and economically feasible, than one with discrete chip and technologies employed for each separate block, where possible. There are of course applications, such as cellular power amplifier, where this integration is not feasible and different semiconducting technologies are implemented together in different chips. Throughout this thesis and for the design and implementation of the novel circuit blocks to be discussed, the challenge is to cope with CMOS's difficulties and bend the corners by introducing novel techniques. In particular, the novelty of the passive resonator introduced is a clear attempt towards this goal.

Chapter 2: Frequency Synthesis Techniques

As discussed in the previous introduction chapter, frequency synthesizer plays a critical role and is an enabling building block for almost all systems, and it sits at the heart of any radio. Many products have failed due to the poor functionality of the frequency synthesizer block; after all frequency synthesizer acts as the reference and carrier for the modulation and demodulation. Moreover, as was observed in the previous chapter, all emerging systems rely heavily on a special feature or requirement of the frequency synthesizer in order to be able to deliver their potential advantage and novelty. The multi-gigabit Wideband Personal Area Network (WPAN), in the 55-67 GHz band, required a wideband continuous tune-able frequency synthesizer. The last mile fiber, long distance, point-to-point wireless communication, in the E-band (71-76 GHz and 81-86 GHz) required a dual band, continuous tune-able frequency synthesizer. The RF interconnect, relying on the multiple widely space carriers (which are not harmonically related to each other), would benefit potentially from a concurrent synthesizer, so that multiple concurrent carriers, independently tune-able from each could co-exist and could be used for modulation. In an OFDM system, frequency hopping is required. Moreover, the settling time for each hopping should be very quick, on the order of few micro seconds. This calls for a super fast locking time for the frequency synthesizer. It is also important to minimize the power consumption, as well as area, in almost all of these

applications. Consequently, while one might think of having multiple synthesizer units which could be turned on or off depending on which band/frequency is to be synthesized, the overhead of area and additional power, together with a non-ideal switching and multiplexing, particularly at higher GHz frequencies, would force the abandonment of the idea and search for techniques which would minimize the use of such techniques.

In what follows the structure of frequency synthesizers, as applied to the aforementioned applications, is reviewed and the bottleneck/critical building blocks of the frequency synthesizer loop for each of the application specific requirements is highlighted and elaborated on.

2.1. The Frequency Synthesizer Loop and Architecture, Overview

A typical Frequency synthesizer loop is presented in Figure 14. The loop is very similar to a phase locked loop (PLL), and the operation merits are quite similar aside from the fact that the frequency synthesizer requires a variable division logic in the feedback path, and has the additional figure of merit of settling time. Generally speaking, the frequency synthesizer is composed of four main elements: the Phase Frequency Detector (PFD), loop filter, voltage controlled oscillator (VCO), and a divider chain to close back the loop. Each of these elements could be implemented in various manners, as well as various degrees of detail and complexity depending on the application at hand and the figures of merit to be targeted for.

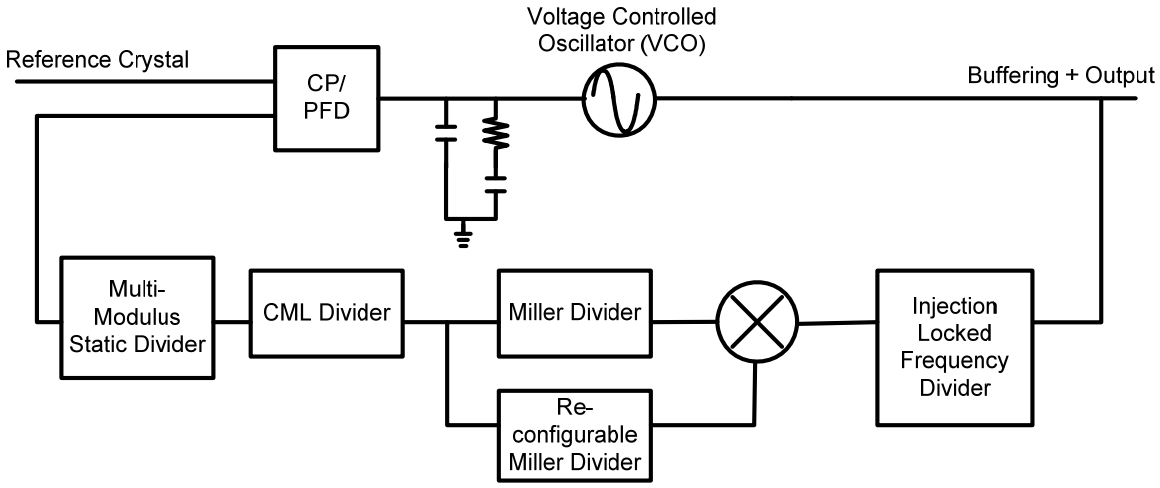


Figure 14, a typical frequency synthesizer loop

In the frequency synthesizer loop of Figure 14, the phase/frequency detector compares the phase and frequency of the feedback frequency/phase, and divided down, of the VCO with that of the reference oscillator, usually implemented in form of a crystal oscillator. The phase/frequency detector tries to match the divided down version of the VCO frequency with that of the reference oscillator. By having a multi-modulus or variable divider chain in the negative feedback loop, one is able to synthesize a particular frequency, provided it is within the locking range of the VCO.

The frequency/phase detector feeds the result of the comparison between the feedback frequency and the reference frequency into the loop filter as either a voltage or current/charge. In the trade off involved between voltage computation or current/charge computation, current/charge computation/comparison is favorable in the case of frequency synthesizers as could be further studied in reference texts on frequency synthesizers, due to the removal of the dead locking zone, as well as the introduction of

an ideal pole at the origin which means an ideal integration [8]. Charge pumping is a popular block for this purpose. The charge pump either creates a positive or negative pulse of current, by sourcing from the positive supply or sinking into ground, depending on a lag or lead of the comparison edges of the reference clock and the feedback signal. The resulting pulse of current is deposited on a loop filter, which is usually implemented off-chip due to the big size of the capacitor involved, as well as its required high quality factor, thus forming another non-ideal integrator, creating a second order loop feedback system. In order to ensure stability, a zero is introduced in parallel with the charging capacitor created by a series connection of a resistor and the capacitor, as illustrated in Figure 14. This configuration is not idea by any measures and regardless of any careful design, there will always be a finite feed through of the reference clock causing distortion and harmonics in the charge thus deposited on the capacitor.

The charge thus deposited on the capacitor of the loop filter converts to an equivalent voltage, hence controlling the Voltage Controlled Oscillator (VCO) oscillation frequency, in an analog and continuous fashion. The VCO is generally implemented using lumped passives, inductors and capacitors. The resonance frequency of the VCO is determined by the connection of the inductor and the capacitor, as well as the parasitic capacitance of the oscillator's active devices and the buffering stages that follow it. The VCO's resonance frequency is typically controlled by tuning and varying the effective capacitance in shunt with the inductance. This is because, as will be discussed, an inductor is harder to tune, in comparison with the capacitor. The effective total capacitance incorporated for tuning purpose is implemented with two type of capacitance: ones that are digitally controlled, using logic gates as controlling elements in

form of a capacitor banks, and ones that are controlled by analog means in form of varactors and MOSCAP capacitances. The voltage induced by the loop filter controls the varactor capacitance of the VCO, in a continuous fashion. As could be expected, the resonance frequency range spanned by varactor is very limited, and hence the digital control of the capacitor banks is introduced to enhance this, mandating array control logic.

The frequency synthesizer loop is completed by including the frequency dividers in the feedback path from the VCO to the Phase/Frequency detector. As discussed above, the frequency dividers ratio determines the oscillation frequency of the VCO in the negative feedback loop. There are different types of frequency dividers, depending on the operating center frequency, bandwidth, and power consumption. There is a tradeoff involved in the choice of the frequency dividers, which will be discussed in the following sections. Moreover, depending on the implementation of the frequency divider chain, various types of frequency synthesizer loops have evolved. There are the integer-N frequency synthesizers and the fractional-N frequency synthesizers. Fractional-N synthesizer are generally applicable for cases where the channel resolution is very fine, on the order of few kHz, where there are strict dynamic range requirements on the radio element due to the number of the customers and the requirements on the adjacent and alternate channel. They are more complex to implement and usually require some form of delta-sigma control in their divider loop, moreover, the loop filter implementation should be enhanced in order to filter the additional distortion introduced by the action of the charge pump in these circuits. Integer-N is easier to implement and is typically chosen for the higher GHz frequency synthesis configurations where channel spacing is wide, and

the dynamic range requirements are more relaxed. Aside from type of divider (modulus) control, there are also different architecture choices for the frequency synthesizer. Two different styles are popular, especially when there is the need to accommodate both wide and small band channels (fine resolution and coarse frequency resolution): multiple loops, with multiple voltage/current controlled oscillators (for each frequency band), or signal loop to cover all bands. The first option is the simpler one, but requires the most power and silicon area; this is un-avoidable in systems that require fast frequency tuning (such as frequency hopped systems). The second option is the cheaper in terms of power and area, but requires ingenious design techniques. Considering the cost issues, as well as robustness and portability, the second option is of course the desired one.

Figures of merit for the frequency synthesizers of third order type two, in terms of the locking time, settling time, and bandwidth, in relation with stability and damping factor are summarized in Figure 15.

Damping factor	$\zeta = \frac{\omega_n R \cdot C}{2}$
Natural frequency	$\omega_n{}^2 = \frac{K_P K_0}{N \cdot C_l}$
Lock range	$\Delta\omega_L \approx 4\pi\zeta\omega_n$
Lock time	$T_L \approx \frac{2\pi}{\omega_n}$
Pull in time	$T_P = \Delta\omega_0 \cdot \frac{N \cdot C_l}{K_P K_0 \pi}$
Pull out range	$\Delta\omega_{p0} \approx 11.55 \cdot \omega_n \cdot (\zeta + 0.5)$

Figure 15, third order type two frequency synthesizer timing FoM

In the table of Figure 15, the lock time and the pull in time are of particular significance, as they capture the time required for the frequency synthesizer to synthesizer a particular frequency. For the aforementioned applications, the locking range in going from the lowest frequency to the highest frequency should be in the order of few micro seconds. In the equations of Figure 15, the C and R are the capacitance and resistance of the loop filter for the third order type-two frequency synthesizer depicted in Figure 14.

In considering which of the blocks in the generic frequency synthesizer shown in Figure 14 are the critical bottlenecks in the design, the aforementioned applications are recalled. For the wideband multi-gigabit wireless communications (WPAN), a continuous tunable frequency synthesizer is required to cover at least 10 GHz of frequency range, considering the corner conditions and sigma variations. As a result the requirement is for an ultra wideband VCO, as a well as he following high frequency divider, the pre-scalar. For the last mile fiber communication, the need is for a dual continuous tuneable frequency synthesizer, whose frequency range is slightly narrower than the case for WPAN (71-76 and 81-86 GHz). Once again, the bottleneck is on the VCO and the following high frequency divider, the pre-scalar. This time they should be dual band operations. For the RF interconnect, as discussed, there is the need for a frequency synthesizer that could generate widely spaced carrier frequencies, none of which are harmonically related. Moreover, since the carriers could co-exist, one could potentially modulate with multiple carriers at the same time, without any interference. As a result, a concurrent frequency synthesizer is desired. A concurrent frequency synthesizer requires a concurrent VCO and a concurrent frequency divider at its heart. For the case of OFDM communication the need is for fast hopping frequency production. While it is possible to

have multiple VCOs on at the same time in the frequency synthesizer loop, and whenever there is the need to jump to another frequency, just swap the VCOs, turning on and off a VCO, or connecting and disconnecting a VCO in the feedback loop is troublesome and could introduce unwanted spikes in the loop which could render the system unstable. Moreover, keeping multiple VCOs on at the same time adds additional overhead power which is not desirable specially for portable devices which goal is to have a long battery life. Once, again a concurrent VCO and frequency divider could be beneficial. So that the concurrent tones exist within the same VCO core, and whenever there is the need to select a particular frequency tone, all other tones are dampened by means of adding a selective loss, whereas the single desired tone survives. As can be observed in above arguments, in the emerging markets, as far as the performance of the frequency synthesizer is concerned, the VCO and the frequency divider are the bottleneck elopements, and the goal should be to implement wideband VCO and frequency dividers as well as possible concurrent operation. Figure 16 presents the frequency synthesizer proposed in this work, which is capable of covering the WPAN frequency, as well as the E-band frequency, which essentially forms a tri-band frequency synthesizer. The frequency planning table is illustrated in Figure 17.

In the following sections a general overview of different types of VCO and frequency dividers is provided, before talking about the proposed enhancement techniques.

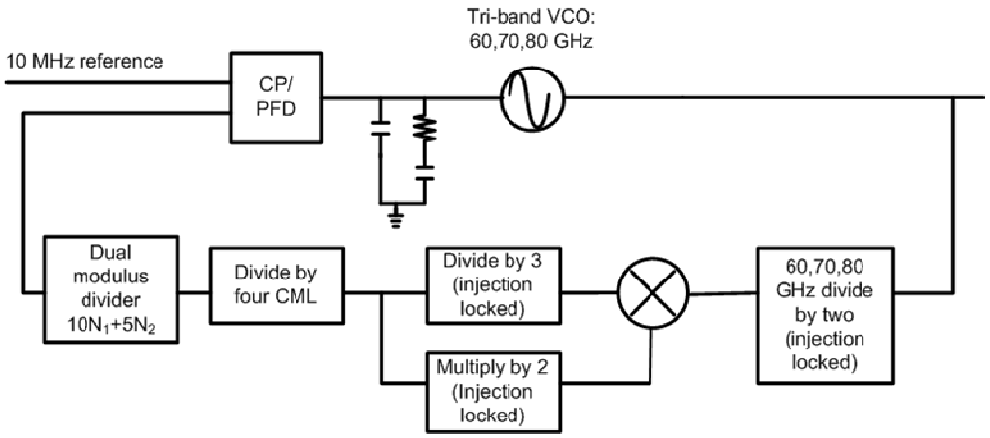


Figure 16, the proposed tri-band frequency synthesizer structure

Reference (GHz): 0.01

Tone (GHz)	Prescaler		10 Frequency (GHz)	Static Divider		4 Frequency (GHz)	Multi-modulus Mod		10 Mod	5
58	5800	580	5.8		145	1.45			14	1
60	6000	600	6		150	1.5			14	2
62	6200	620	6.2		155	1.55			14	3
64	6400	640	6.4		160	1.6			14	4
70	7000	700	7		175	1.75			14	7
72	7200	720	7.2		180	1.8			14	8
74	7400	740	7.4		185	1.85			14	9
76	7600	760	7.6		190	1.9			14	10
80	8000	800	8		200	2			14	12
82	8200	820	8.2		205	2.05			14	13
84	8400	840	8.4		210	2.1			14	14

Figure 17, the proposed tri-band frequency synthesizer frequency planning

2.2. Voltage Controlled Oscillator (VCO)

By correcting the control voltage of the Voltage Controlled Oscillator (VCO), the frequency synthesizer is capable of producing the frequency tones required. As such, it is important for the VCO to be able to cover the entire frequency range required, in cases where the single VCO is incorporated to implement the entire frequency band. In addition to the required frequency range, the VCO's design should also allow for a margin, to sigma variation allocation purposes. The synthesizer loop controls the VCO by analog means, via the charge pump and the loop filter. The voltage control is implemented in form a varactor (MOSCAP), where the gate-source capacitance is a function of the bias voltage on the MOSCAP. As mentioned, for passive elements, especially the ones implemented in an oscillator, the quality factor is an important figure of merit, as it determines the losses for which the active part of the oscillator is supposed to compensate for in order to ensure a steady oscillation. There is a trade off in the varactor choice for the VCO, involving the tuning frequency range and the quality factor: the wider the tuning range is, the lower the quality factor and the higher the quality factor is the lower the tuning range. Moreover, in order to ensure a proper locking time and stability mechanism it is important that the VCO's control voltage is precise and not too sensitive to the tuning voltage, as any slight variations, from noise and any other outside means could easily cause a drift in the oscillation frequency, and thus losing the frequency lock. The sensitivity of the VCO tuning voltage is characterized by K_{VCO}. For a given allowable tuning voltage range (twice the rail for a MOSCAP biased at zero), the VCO with a lower K_{VCO} could cover a smaller frequency range, but it is more stable and precise, whereas a VCO with a large K_{VCO} is able to cover a large frequency range but is prone to instability and false locking at times. In order to address this issue, the VCO

control is implemented by two methods: digital and analog. Variously sized banks of fixed capacitors, in the form of Metal-Insulator-Metal (MIM), or Metal-Over-Metal (MOM) are switched-in/connected to the VCO's resonator tank or switched-out/disconnected to the VCO's resonator tank. This control is done by a digital logic block and it is crucial to ensure sufficient overlap across the various capacitor bands. The function of the analog tuning varactor is to continuously tune the smaller bands within each regime encompassed by the fixed capacitor banks. This techniques is illustrated further in Figure 18. While this is very feasible in lower GHz frequency works (less than 10 GHz), and is almost always used for commercial products, this technique is not viable for higher GHz frequency bands for the reason that the switches lose their functionality to act as a switch. Their finite R_{on} resistance degrades the loaded quality factor of the tank, and should one decide the increase the size of the switch to address this problem, the parasitic of the switch limit the tuning range, as well as the center frequency of the VCO. As such, implementing a broad tuning range VCO at high GHz frequencies (greater than 10 GHz), is a challenging task due to the parasitic aware requirements.

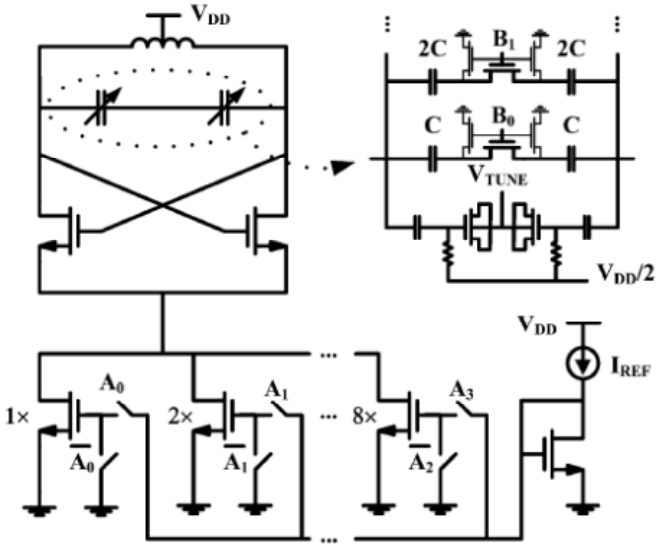


Figure 18, digital control of capacitor banks and analog control of the varactor for VCO tuning purpose [9]

Aside from the tuning range, the other figure of merits that are of significance, especially for portable, handheld, devices are the power consumption and the phase noise performance. The more loss the tank presents to the active core of the VCO, the higher the power consumption has to be to injection enough power into the device for sustaining the oscillation. Furthermore, at higher GHz frequencies, the device power gain drops rapidly (40 dB/decade after the unconditionally stable regime), with f_{MAX} characterizing the highest possible oscillation frequency that is the higher frequency where power gain of one is possible (analyzed from a small signal point of view). Higher power consumption is required to only bring up the power gain slightly, in order to meet the trans-conductance required for the oscillation startup purpose. Phase noise is another critical figure of merit especially for systems that require wide dynamic range specifications. The phase noise skirt of the frequency tone produced by the frequency synthesizer could mix with adjacent channel signals, down convert and self mix and cause spurious response as well as lower the SNR. There have been various theories regarding phase noise in oscillators, a famous one is Leeson's model as expressed in equation below:

$$\Gamma(f) = \frac{FkT}{8P_0} \frac{1}{Q_{\text{loaded}}^2} \left(\frac{f_s}{f}\right)^2$$

According to this model, the phase noise is inversely proportional to the square of the quality factor of the oscillator. Consequently, the higher the quality factor of the tank is,

the better the phase noise performance. Lumped inductor and capacitor elements incorporated in the resonator structure of VCO, posses an interesting property as function of frequency. In the lower GHz frequency (less than 10 GHz), the inductor's quality factor is limiting quality factor to the resonator, whereas the capacitor is able to achieve very high quality factors. However, in the higher GHz frequency range (greater than 10 GHz), the inductor quality factor reaches a high value, where the capacitor becomes a problem. This phenomenon is due to the nature of loss in these elements, magnetic loss for the inductor, and electric field loss for the capacitors.

Phase noise is also directly proportional to the noise factor of the oscillator, F. The noise factor is an empirical value which depends on the nature of the oscillator's active core. There has been numerous research on the noise factor of the oscillator and techniques of minimizing it [10-12]. The common theme is that different types of transistor energy injections in to the resonator result in different phase noise profiles. Particularly, if the transistors inject the recovery energy (to compensate for the resonator's loss) during the peak amplitudes of oscillation, the phase noise is much better than if the energy is injected during the zero crossing of the waveforms. The oscillator core that best approaches this line of reasoning is Colpitts oscillator, three flavors of which are illustrated in Figure 19.

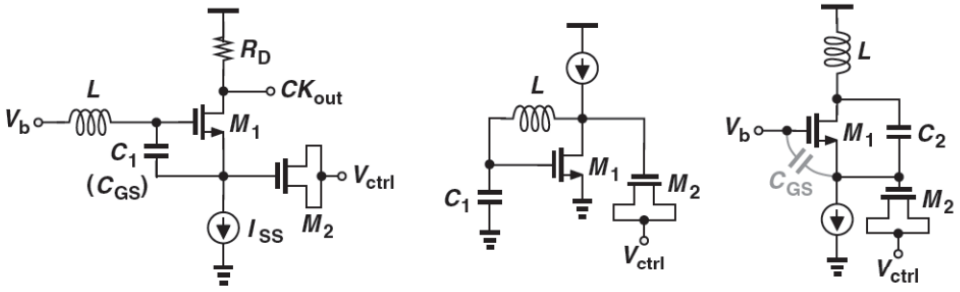


Figure 19, different types of Colpitts oscillator

While the Colpitts oscillator could ideally have a better phase noise performance, its other draw backs usually inhibit its use. Particularly, the Colpitts oscillator requires a higher power for start-up, which is a major issue especially at higher frequencies. Moreover, differential operation and signal generation is a must and mandate for many communication system, due to its many benefits and advantage, in particular the common mode rejection and excellent linearity performance, by killing the even harmonics. The Colpitts oscillator doesn't blend into differential operation naturally. There has been various attempts to creating a differential Colpitts, as illustrated in Figure 20; however, any slight mismatch in the value of the inductors or capacitors incorporated on the two half-sides of the Colpitts would cease the differential oscillator to exist. Consequently, cross-coupled core design styles are of favor, especially for commercial products, to their ease of design, robustness, as well as reliability over corner conditions. In the following section the requirements and specification of the frequency synthesizer are translated from the VCO onto the frequency divider, as discussed previously, in order to consider the possible options available before discussing the enhancement techniques.

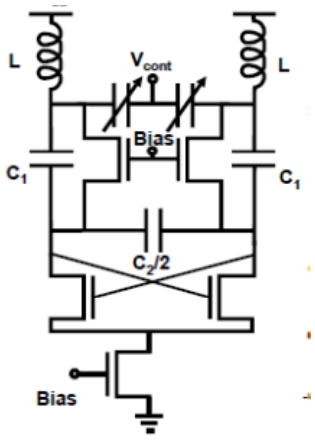


Figure 20, differential Colpitts VCO from [13]

2.3. High Frequency Divider, Pre-scalar of the Frequency Synthesizer Loop

In order to complete the negative feedback loop around the VCO, thus forming its control voltage via the reference frequency and the phase/frequency detector, divider chains are required to bring the VCO frequency down to the same frequency as the reference clock. There are multiple ways of implementing the frequency dividers, depending on the limitations of the technology at use. However, the first frequency divider following the VCO is the most critical one in the design. Multi-modulus design in case of integer-N or delta-sigma control in case of fractional-N are applied to the later stages of the frequency division, once the frequency is divided down to about 1 GHz. As such, the first frequency divider is the one of the highest frequency, and also of the widest bandwidth. The most critical issue is that the frequency divider (pre-scalar) should be able to cover the entire range of the VCO, as well as allowing sufficient margin for sigma variations. Moreover, in order to simplify the design process and the control loop of the frequency synthesizer, unlike the case of the VCO where digital logic blocks were used for switching the frequency bands, the frequency dividers shouldn't employ any kind of band switching or varactor controls. As a result, the divider should be wide-band width without any tuning mechanism, and in case of multi-band frequency synthesizers should be able to accommodate all the bands. The frequency divider ideally degrades the phase noise of the VCO by the following factor, where N is the division factor:

$$20\log_{10} N \text{ dB}$$

There are various ways of implementing the pre-scalar frequency divider. The three popular types are the: injection locked frequency division, miller frequency division, and static frequency division. Injection locked frequency dividers rely on injecting a tone into the common mode point of a cross-coupled oscillator, in a form similar to push-push operation, thus forcing a frequency division operation. Miller frequency dividers rely on feedback and low pass filtering, along with mixing in order to create different frequency harmonics out of the original one applied. The static frequency dividers are the digital ones that use flip-flops for division operation. In the discussion below the three types are further elaborated on, and the trade-offs are studied. Figure 21 below illustrate a generic injection locked frequency divider, implementing a divide by two operations.

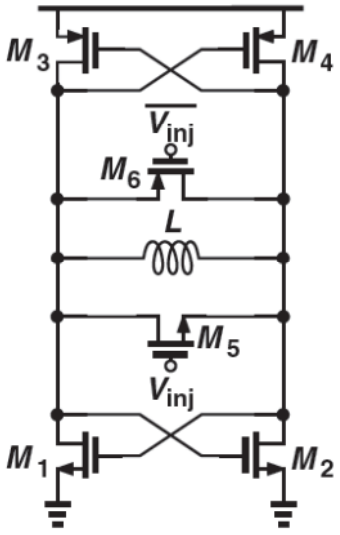


Figure 21, divide by two injection locked frequency divider

The core of the injection locked divider in Figure 21, is the classical cross coupled pair, in this case a complementary pair. The signal to be divided by two is injection across the thank, in parallel with the inductor and the cross-coupled pair thus pulling the oscillation frequency in a push-push manner to half the incoming signal. As could be expected due to the tuned tank nature of the injection locked frequency divider its frequency bandwidth is small. Morever, since it mandates the use of the inductor it is mostly favorable for higher frequency operation where the size and losses of the inductor could be tolerated. On the other hand, because the same tuned tank feature, the injection locked frequency divider is able to operate at very high center frequency, permit-able by the natural oscillation frequency of the core oscillator and is also low power in operation. The injection locking range could be express as follows:

$$\omega_{lock} \approx \frac{\omega_0}{2 \cdot Q} \times \frac{I_{inj}}{I_{osc}}$$

Where the Q is the quality factor of the tuned tank, I_{inj} is the strength of the injection signal, and I_{osc} is the oscillation current. As can be seen the locking range is inversely proportional to the quality factor of the tank. One technique to enhance the locking range is to reduce the quality factor of the tank intentionally by adding losses. This however comes at the price of oscillation instability as well as higher power required to sustain the oscillation.

Figure 22 depicts a miller divider, which is also called the regenerative frequency divider. The operation of the miller divider relies on the use of the frequency mixer, along with selective filtering of the generated inter-modulation tones.

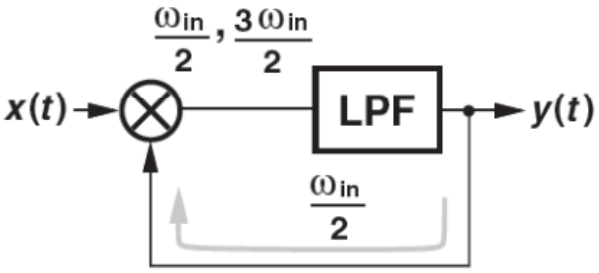


Figure 22, Miller frequency divider

As illustrated in Figure 22, in the miller frequency divider, the incoming signal is mixed by an inter-modulation product of itself and upon filtering it is able to realize any modulus required. The problem with this divider is the complexity of the design involved; in particular, the need for mixing and filtering the tones is a major one. Efficient mixing operation is a major issue as frequency is increased, let alone completing the feedback loop. As a result, the miller divider, while being able to produce an arbitrary ratio of division modulus, is limited in highest frequency of operation.

Figure 23 illustrates the static division by two frequency divider. The design is based on using flip-flops in achieving the division by two ratios. However, using more elaborate frequency counters or pulse swallowers along with delta-sigma decimation it is possible to achieve any division ratio required.

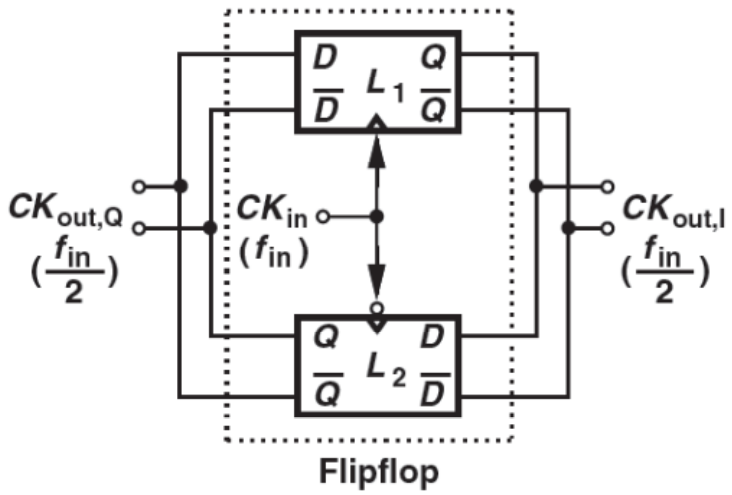


Figure 23, static divider-by-two frequency divider

The flip-flops illustrated in Figure 23 for the static divider could be implemented in various ways. The Current-Mode-Logic (CML) is able to achieve the highest frequency of operation; figure 24 illustrates a D-flip flop implemented using the CML to highlight the features.

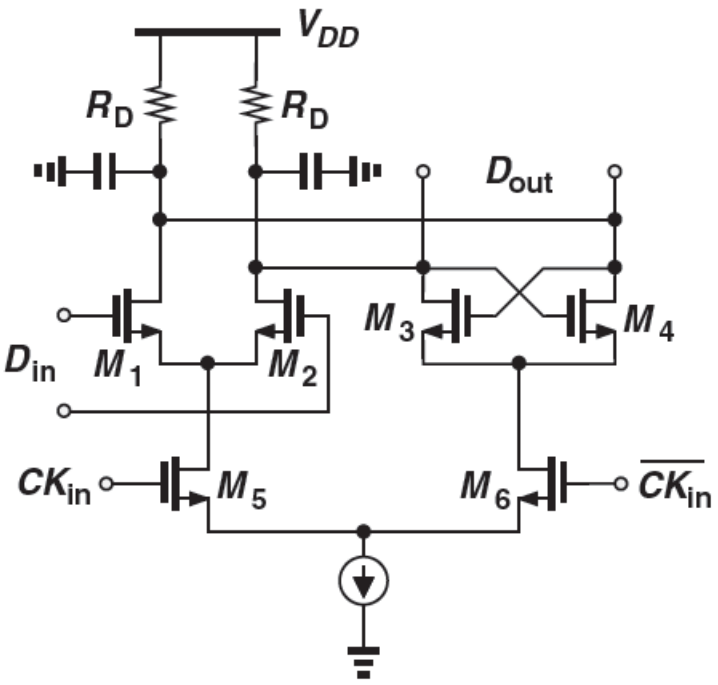


Figure 24, CML D flip-flop

The CML D-flip flop is able to achieve the highest frequency of operation amongst the different styles of frequency dividers due to the use of current re-cycling through a differential pair, along with positive feedback implemented in form of the latch. Compared to other types of frequency dividers, a very small voltage swing on the input is required to be sensed by the differential pair and steer the current from one side of the latch to the other side, thus flipping the state of the flop-flop. Nevertheless, the operation frequency of the CML is limited.

As discussed above, the trade-offs involved for frequency dividers are for power consumption, center frequency, and frequency bandwidth. Figure 25 compares the center frequency of operation for the injection locked, miller and static divider. It is concluded that the injection locked class of frequency dividers is the optimal choice for high frequency operation, as well as complexity and power consumption. However, the frequency bandwidth of the divider should be extended in order to accommodate the specifications. In the following sections techniques for enhancing the tuning range of the VCO as well as the injection locked divider in addressing the multi-band and concurrent operation are discussed.

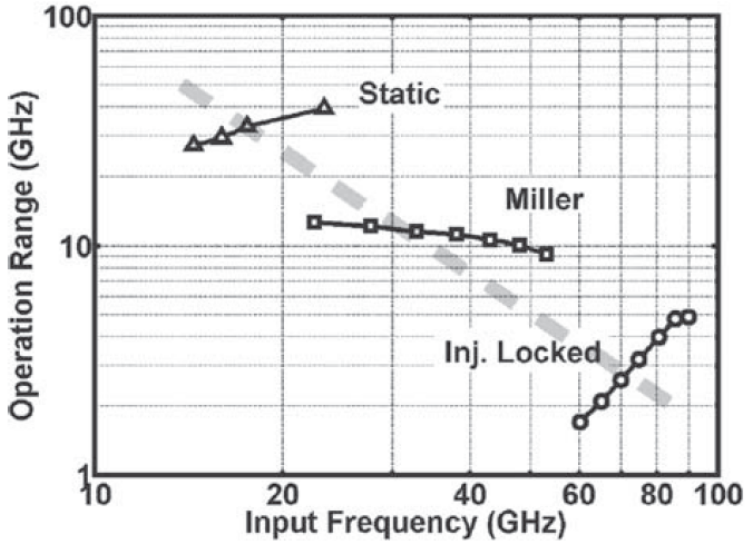


Figure 25, comparison of different divider structure's center frequency of operation [3]

Chapter 3: Distributed Passive Elements

As frequency increases, elements tend to lose their lumped-ness behavior, and begin to act as if they are made of multiple elements attached together forming the single lumped element. This is because standing wave patterns could develop in these elements and the assumption of uniformity of voltage and current is no longer valid. Throughout the length of the lumped element, voltage and current could have varying phase and amplitude. As a result of the traveling wave and standing wave response, distributed elements could results in unique resonating elements. In a sense, the distributed element could be approximated as a 1 dimensional array of inductors resulting in an overall inductance with superior qualities than that of a single inductor, or as a 1 dimensional array of capacitors resulting in an overall capacitance with super qualities than that of a single capacitor. By inductive or capacitive quality, the Quality factor and the resolution (maximum to minimum) ratio of achievable capacitance or inductance is implied. In what follows, transmission lines are studied as such distributed elements.

3.1. Quarter wave transmission line

The quarter wave transformer is a useful and practical circuit for impedance matching and also provides a simple transmission line circuit that further illustrates the properties of standing waves on a mismatched line. The quarter wave transformer is a simple and useful circuit for matching a real load impedance to a transmission line. An additional feature of the quarter wave transformer is that it can be extended to multi section designs in a methodical manner, for broader bandwidth. If only a narrow band impedance match is required a single section transformer may suffice. As it will be shown later multisection quarter wave transformer design can be synthesized to yield optimum matching characteristics over a desired frequency band.

One drawback of the quarter wave transformer is that it can only match a real load impedance. A complex load impedance can always be transformed to a real impedance, however, by using an appropriate length of transmission line between the load and the transformer, or an appropriate length of transmission line between the load and the transformer, or an appropriate series or shunt reactive stub. These techniques usually alter the frequency dependence of the equivalent load, which often has the effect of reducing the bandwidth of the match. In a single section quarter wave matching transformer the

following relationship between the characteristic impedance of the line and the load and network impedances could be stated:

$$Z_1 = \sqrt{Z_0 \times Z_L}$$

Where the Z_1 is the source impedance of the line, Z_0 is the characteristic impedance of the line and the Z_L is the load impedance of the line. At the design frequency, f0, the electrical length of the matching section is λ/4, but at other frequencies the length is different, so a perfect match is no longer obtained. This is because standing wave patterns could develop in these elements and the assumption of uniformity of voltage and current is no longer valid. Throughout the length of the lumped element, voltage and current could have varying phase and amplitude. As a result of the traveling wave and standing wave response, distributed elements could results in unique resonating elements. In a sense, the distributed element could be approximated as a 1 dimensional array of inductors resulting in an overall inductance with superior qualities than that of a single inductor, or as a 1 dimensional array of capacitors resulting in an overall capacitance with super qualities than that of a single capacitor. By inductive or capacitive quality, the Quality factor and the resolution (maximum to minimum) ratio of achievable capacitance or inductance is implied.

At mm-wave frequencies, the reactive elements needed for matching networks and resonators become increasingly small, requiring inductance values on the order of 50 to 250 pH. Given the quasi-transverse electromagnetic (quasi-TEM) mode of propagation, transmission lines are inherently scalable in length and are capable of

realizing precise values of small reactances. Additionally, interconnect wiring can be modeled directly when implemented using transmission lines. Two complex parameters are needed to completely capture the properties of any quasi TEM transmission line at a given frequency. A transmission line can be characterized by its equivalent frequency dependant RLGC distributed circuit model, as in Figure 26.

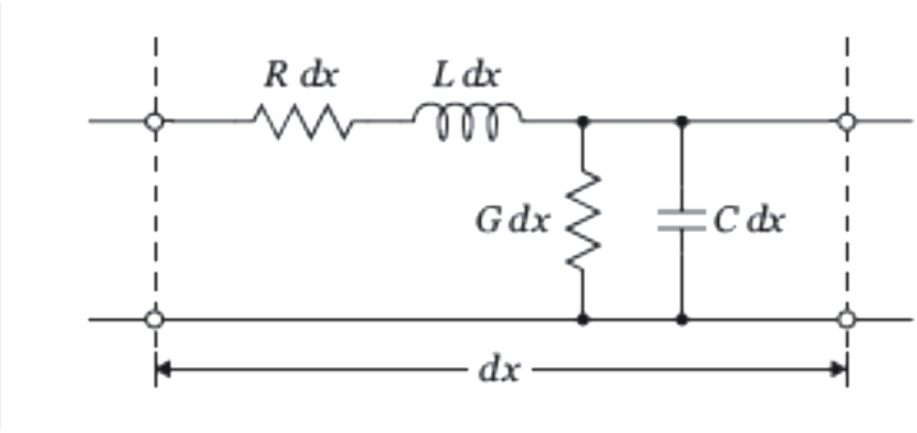


Figure 26, RLGC model of transmission line.

Unlike transmission lines implemented on GaAs, where G is essentially zero, due to the insulating nature of the GaAs substrate, transmission lines implemented on low resistivity silicon often have capacitive quality factors (Q_c) due to t he substrate coupling. For transmission lines that store mostly magnetic energy, the inductive quality factor (Q_L) is the most critical parameter when determining the loss of the line, as opposed to the resonator quality factor or the attenuation constant. Transmission lines are often used to resonate with the intrinsic capacitance of the transistors, such as when used in matching networks, in which case the line stores mostly magnetic energy, and is therefore most appropriate to consider the power lost for a given amount of net reactive energy stored in

the line, as opposed to the total stored energy. Thus, for matching networks the most meaningful metric is

$$Q = 2\omega_0 \frac{\text{net energy stored}}{\text{avg. power loss}} = \frac{2\omega_0(W_m - W_e)}{P_R + P_G}$$

Where W_m and W_e are the average magnetic and electric energy stored, and P_R represent the series resistive losses and P_G is shunt conductive losses. If the line is inductive the loss in the line is completely determined by Q_L. For example consider a shorted transmission line. In this case the Q_L dominates, which greatly reduces the impact of the shunt losses on the inductive line. This is particularly important for integrated transmission lines on silicon where the low resistivity substrate causes Q_C to be non-negligible.

In what follows a unique perspective to the excitation and implementation of quarter wave transmission line via orthogonal E and H modes is introduced.

3.2. The four port excitation technique

Driven by the goal of achieving a multi-band, multi-standard, as well as a reconfigurable radio or one that can adjust and optimize its performance under any operating condition, many different tuning and reference signal generation schemes have been envisioned and implemented in the lower GHz regime (below the Ku band). There is a growing interest in implementing similar ideas in the higher GHz band. For example, there is the unlicensed 57-64 GHz band, applicable for wide-band communication, as well as the three licensed 71-76 GHz, 81-86 GHz, and 92-95 GHz applicable for point-to-point fixed wireless communication such as last-mile access bottlenecks. There is also an interest in wireless chip-chip communication. Wide-band tuning techniques commonly implemented in the lower GHz regime are in the form of varactor/capacitor-bank sizing, inductor switching [14], or transistor core size switching [15]. In case of capacitor switching variously sized varactors/capacitors are connected to the resonator and enabled with switches. In case of inductor switching [14], either variously sized inductors are switched and connected to the resonator, or various inductors' coupling is switched and controlled [14] so that the effective total inductance is changed. These techniques, however, are not as readily applicable to higher GHz bands for the reason that the

switches are along the path of the signal oscillation and as a result themselves as well as their parasitic deteriorates the loaded Q-factor. As a result, various techniques have been proposed to address the problem and attain a wider frequency range.

Multiplexing multiple VCOs has been proposed, and implemented in a PLL [15]; the disadvantage is in added area for multiple VCOs and power consumption for the multiplexer, as well as the loss introduced. In order to minimize the effect of the switches in the signal path, [16,17] mode selection/capacitor control switches have been implemented so that they are not enabled during the whole cycle of oscillation. In [17], due to the dynamics of the system two resonances are possible, and the switches control which tone to oscillate at; once a tone is selected that is the only stable oscillation frequency for the circuit, the switches are not needed anymore, and they are opened. The timing for the switch control (enabling/disabling) has to be well controlled/modeled, otherwise the tone could drift to the other resonance condition and create confusion. Moreover, the asymmetry of the oscillation could cause flicker noise up-conversion and thus poor phase noise performance. In [18], a technique has been introduced to exploit the capacitance in differential mode vs. common mode, to create two different discrete oscillation frequencies, and also ideally minimize the effect of the switches. However, to get more discrete tones, and produce 2^N tones, many inductors are still needed. Transmission lines could be exploited for higher frequency and bandwidth operation due to their distributed nature. In [19] a standing-wave VCO is implemented with coplanar-stripline (CPS), and oscillation tuning is achieved by shorting different lengths of the transmission line, as well as varactors. Since the switches are used to short the length of the transmission line their parasitic and series resistance directly affects the Q-factor of

the resonator and to mitigate it the switches. are made very big. The parasitic capacitance thus introduced as well as the poor R_{on}/R_{off} ratio of the switches affects the center frequency, as well as bandwidth, power consumption, and phase noise.

In order to address the aforementioned problems, a technique based on E and H mode excitation of a transmission line resonator configured in a standing-wave VCO topology is proposed in this paper, that is able to achieve very wide bandwidth, high frequency, as well as good phase noise with low power consumption, while occupying a small die area, since only one resonator is required for the entire frequency band.

3.3. The resonator

Transmission lines in various configurations, in particular the quarter wave resonator, and their various applications have been discussed extensively in the literature. Moreover, the wave propagation on transmission lines with both open, and short ended configurations have also been elaborated on. In this work the loaded transmission lines is excited under both open and short termination, via the E-mode or H-mode excitation, as means of mode selection, in order to achieve a wide tuning range while avoiding the detrimental switches. When a transmission line is excited to be shorted at one end, any capacitor at that end would be ineffective, whereas the capacitor at the open-end will be effective at determining the resonance frequency.

Figure 27, illustrates the structure of the resonator, with the capacitor/varactor bank, axis of symmetry, and the four excitation ports highlighted. Cross-coupled pairs control the excitation ports in the way that ports 1 and 3 are connected to one complementary (NMOS and PMOS) set, whereas ports 2 and 4 to another. In this way, ports 1 and 3 are always 180 degrees out of phase, as well as ports 2 and 4. Ports 1 and 2, and 3 and 4 are controlled to be either in phase, or 180 degrees out of phase, as pictured in Figure 28. When ports 1 and 2 are in phase, ports 3 and 4 are also symmetrically in phase, whereas when ports 1 and 2 are 180 degrees out of phase, ports 3 and 4 are also 180 degrees out of phase.

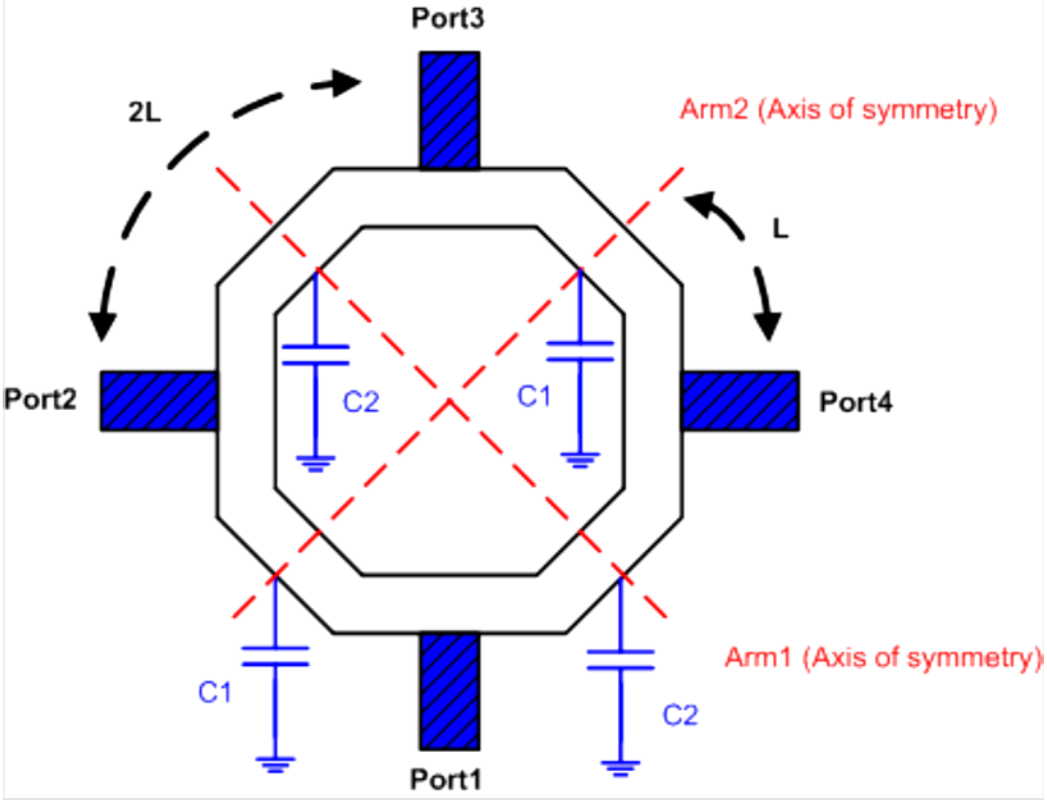


Figure 27, The resonator structure, illustrating the transmission line, capacitor banks, axis of symmetry, as well as the excitation ports.

Transmission lines in various configurations, in particular the quarter wave resonator, and their various applications have been discussed extensively in the literature. Moreover, the wave propagation on transmission lines with both open, and short ended configurations have also been elaborated on. In this work the loaded transmission lines is excited under both open and short termination, via the E-mode or H-mode excitation, as means of mode selection, in order to achieve a wide tuning range while avoiding the detrimental switches. When a transmission line is excited to be shorted at one end, any capacitor at that end would be ineffective, whereas the capacitor at the open-end will be effective at determining the resonance frequency. Figure 27, illustrates the structure of the resonator, with the capacitor/varactor bank, axis of symmetry, and the four excitation ports highlighted. Cross-coupled pairs control the excitation ports in the way that ports 1 and 3 are connected to one complementary (NMOS and PMOS) set, whereas ports 2 and 4 to another. In this way, ports 1 and 3 are always 180 degrees out of phase, as well as ports 2 and 4. Ports 1 and 2, and 3 and 4 are controlled to be either in phase, or 180 degrees out of phase, as pictured in Figure 28. When ports 1 and 2 are in phase, ports 3 and 4 are also symmetrically in phase, whereas when ports 1 and 2 are 180 degrees out of phase, ports 3 and 4 are also 180 degrees out of phase.

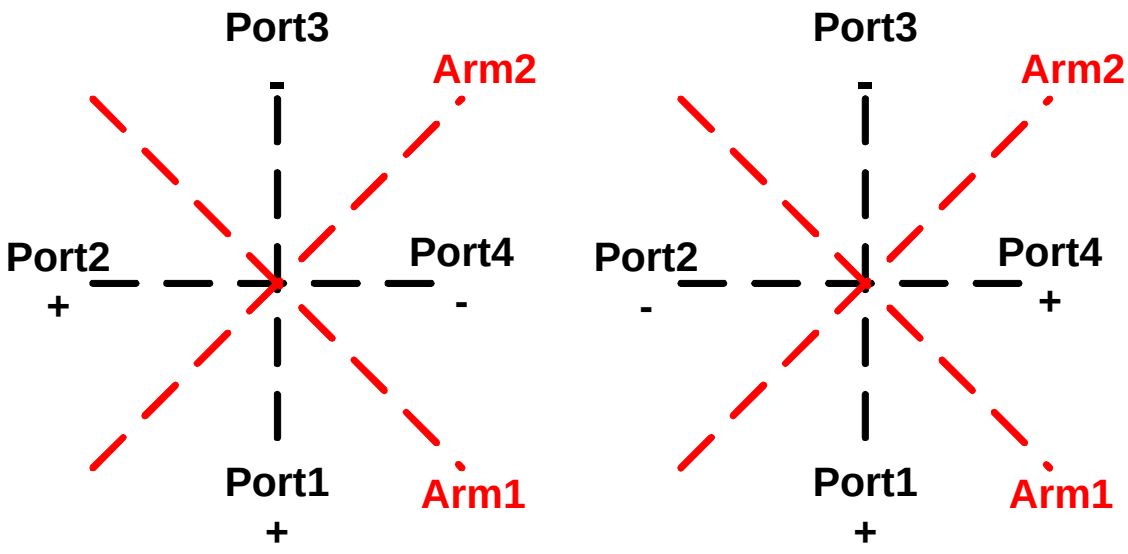


Figure 28, Resonator excitation ports polarity. 1 and 3 (2 and 4) always 180 degrees out of phase, whereas in (a) 1 and 2 (3 and 4) are in phase, and in (b) 1 and 2 (3 and 4) are 180 degrees out of phase.

Depending on how the ports are excited, when ports 1 and 2 (3 and 4) are in phase, as in Fig. 2(a) Arm2 is an H field boundary, forming an open circuit, and Arm1is an E field boundary, forming a virtual ground, Fig. 29. On the other hand, when ports 1 and 2 (3 and 4) are out of phase, as in Fig. 2(b), Arm2 is an E field boundary and Arm1 is an H field boundary, Fig. 30. The in-phase control is implemented with switches, as explained later. When the switch is turned on ports 1 and 2 (3 and 4) are in phase, and when it's open, ports 1 and 2 (3 and 4) are out of phase by 180 degrees and instead 1 and 4 (2 and 3) are switched to be in phase. As the resonator has only two degrees of freedom, only one of the modes is favored at any time. The significant point is that the switch is only turned-on to inhibit one unwanted mode, and does not degrade the other desirable mode. The resonance condition corresponding to each case is discussed below. Due to the symmetry of the design only one pair of ports are taken into analysis.

The resonance condition corresponding to the configuration in Figure 29 can be stated as in:

$$\omega \cdot C_1 \cdot Zline = 2 \cdot \cot\left(2 \cdot \theta\right)$$

The resonance condition corresponding to Figure 30 can be stated in:

$$\omega \cdot C_2 \cdot Zline = 2 \cdot \cot\left(2 \cdot \theta\right)$$

As can be seen in the equations above the resonance frequency depends on four designable variables, C_1 and C_2 capacitance/varactor banks, Z_{line} the characteristic impedance of the transmission line, and θ the electrical length of the transmission line. As a result an optimization scheme is required to fit the frequency range while achieving the best performance from the VCO.

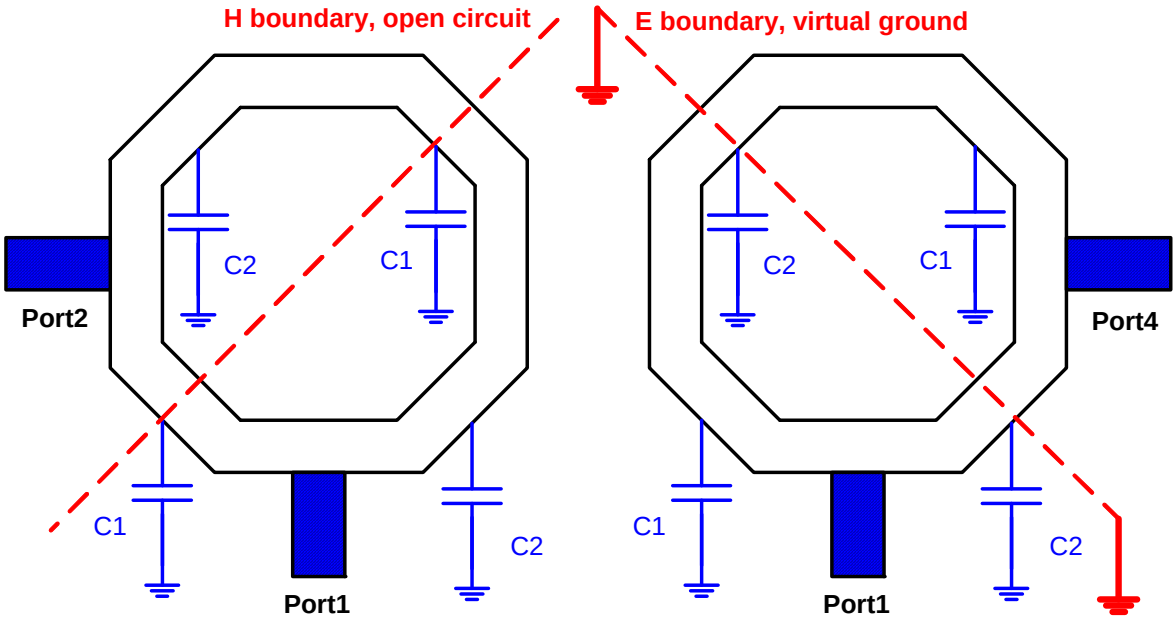


Figure 29, Resonator structure analysis when ports 1 and 2 are in phase and 1 and 4 are 180 degrees out of phase.

A design curve is presented in Figure 31, where the sweep of characteristic impedance vs. the capacitance bank for Arm1 is studied for the higher V-Band coverage. As can be seen in (1) and (2) the resonance frequency depends on four designable variables, C_1 and C_2 capacitance/varactor banks, Z_{line} the characteristic impedance of the transmission line, and θ the electrical length of the transmission line. As a result an optimization scheme is required to fit the frequency range while achieving the best performance from the VCO.

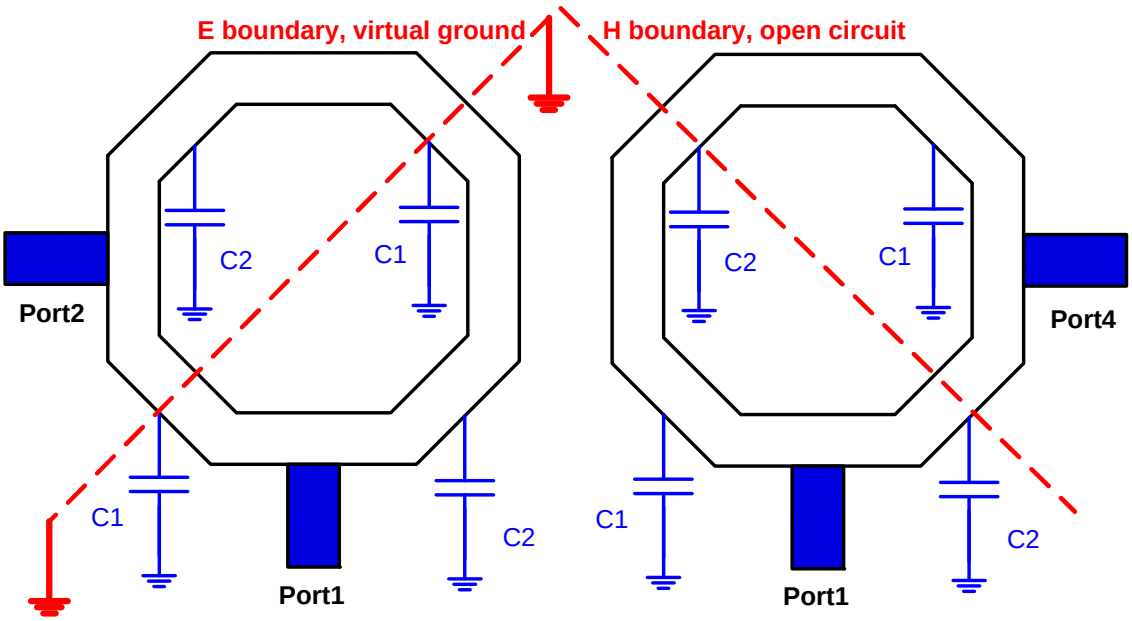


Figure 30, Resonator structure analysis when ports 1 and 2 are 180 degrees out of phase and 1 and 4 are in phase.

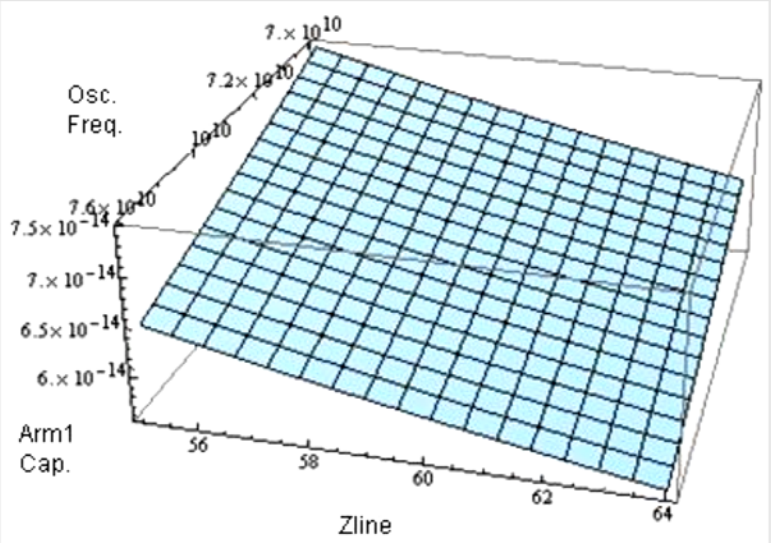
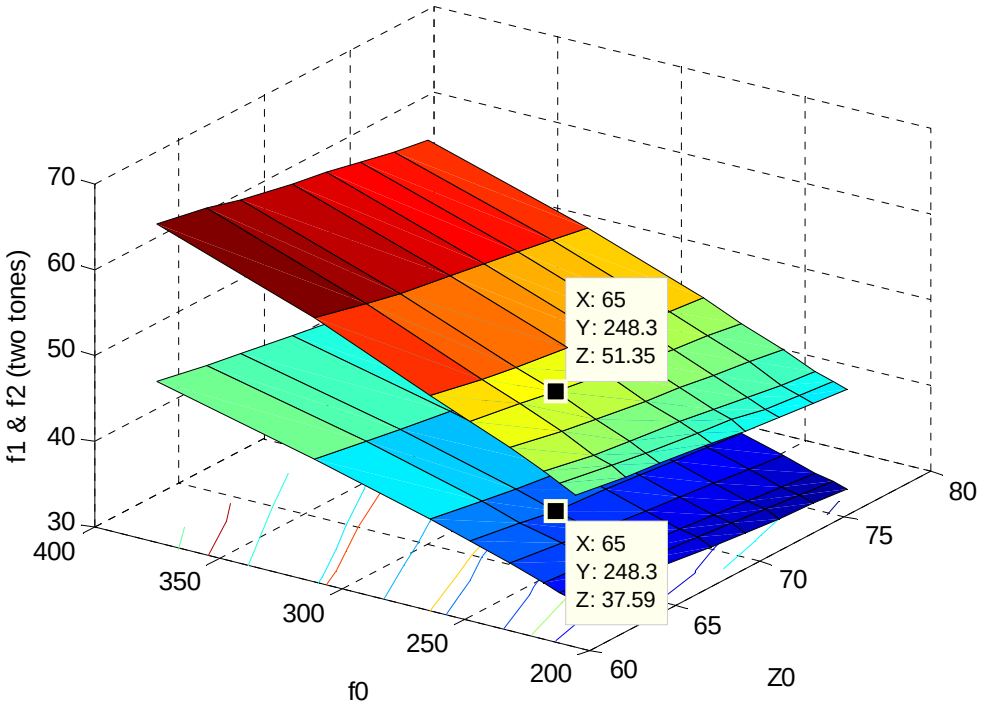
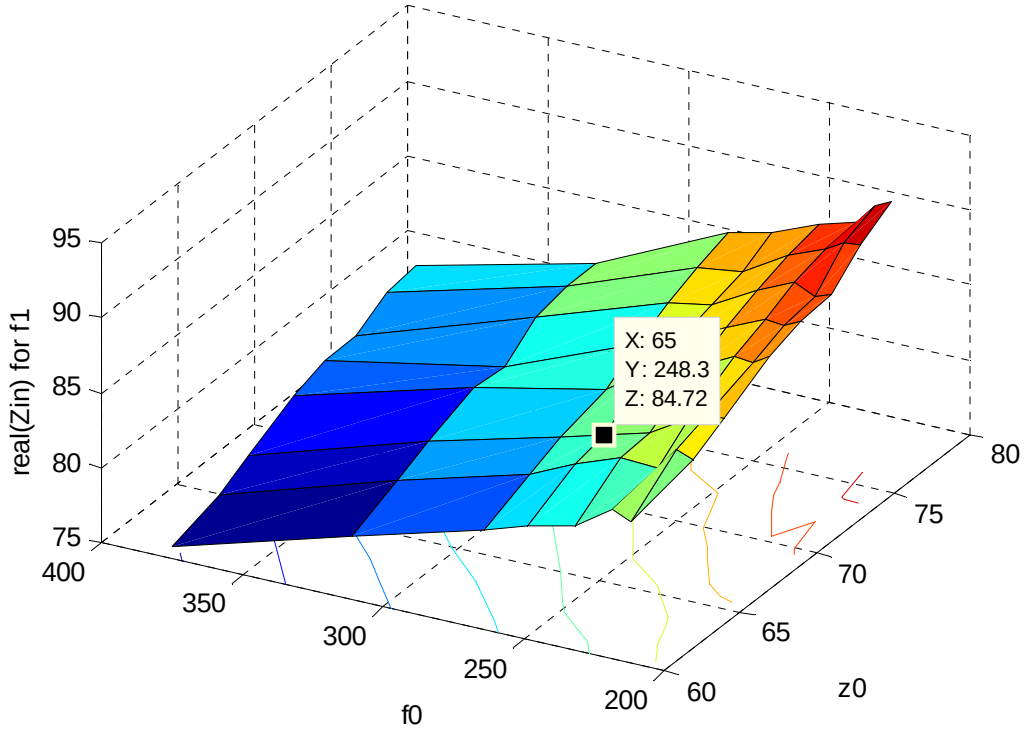


Figure 31, Sample design curve for high V-band coverage.

Further design curves are illustrated in Figure 32 to reflect the significance of the different transmission line parameters in determining the resonance frequency.




real(Zin) for f1
95
90
85
80
75
400
350
300
250
200
f0
60
65
70
75
80
z0
X: 65
Y: 248.3
Z: 84.72

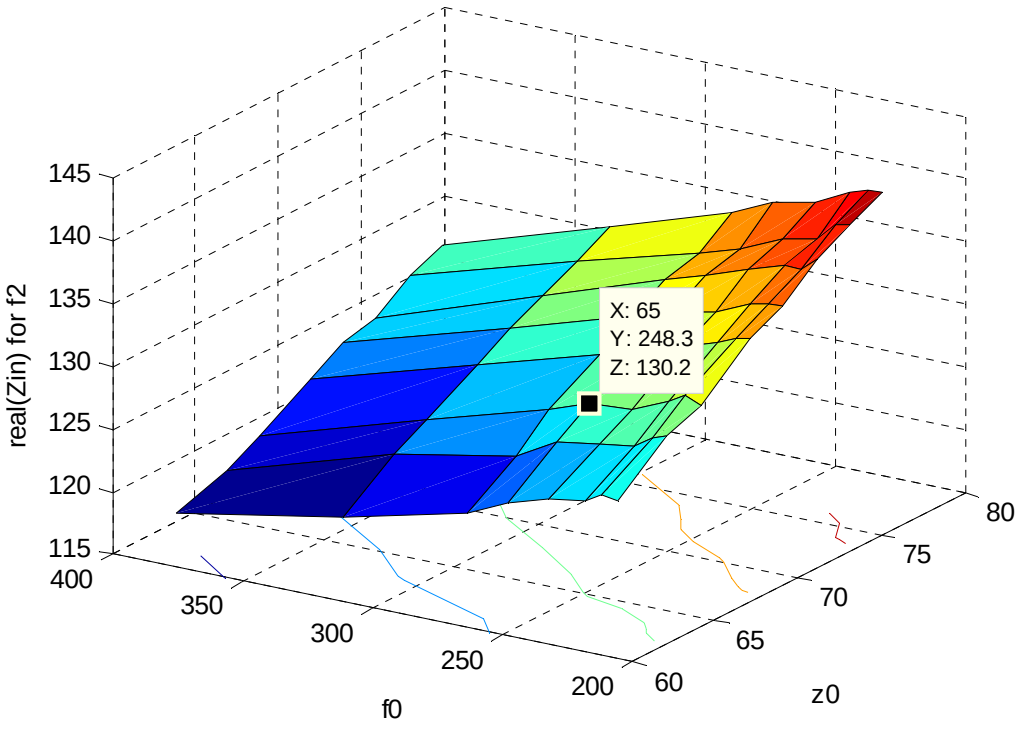
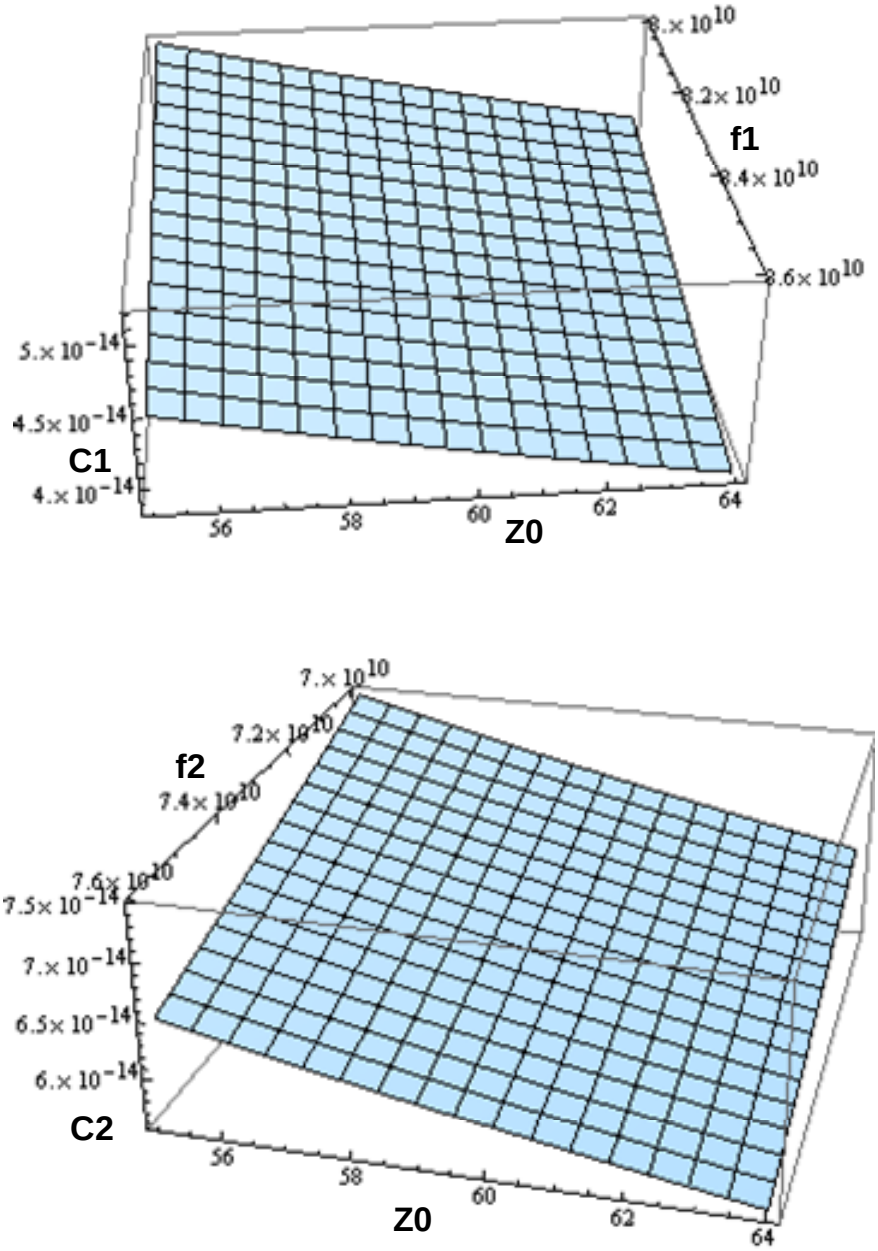

real(Zin) for f2
145
140
135
130
125
120
115
400
350
300
250
200
f0
60
65
70
75
80
z0
X: 65
Y: 248.3
Z: 130.2

Figure 32, characterizing the transmission line in determining the two resonance frequencies



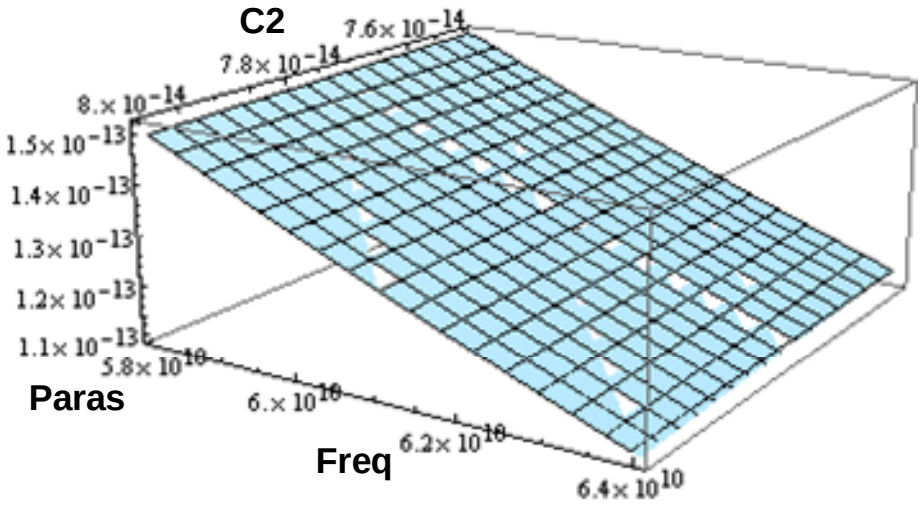


Figure 33, V-band coverage optimization

As can be seen in (1) and (2) the resonance frequency depends on four designable variables, C_1 and C_2 capacitance/varactor banks, Z_{line} the characteristic impedance of the transmission line, and θ the electrical length of the transmission line. As a result an optimization scheme is required to fit the frequency range while achieving the best performance from the VCO.

3.4. Mode Selection

A mode selection switch exists between port 1 and 2, 1 and 4, as well as port 3 and 2, 3 and 4. The switches are a single small NMOS device (4 um/0.065 um) and their only purpose is to separate the two modes (E and H). Since the two modes are orthogonal and could co-exist, the switches parasitic and Ron inserted in one mode does not degrade the performance in the other mode. Their only goal is to provide a higher loss for the undesired mode, so that the undesired mode doesn't resonate as readily as the desired one. For example, in case of H-mode (Fig. 34), the switch is short between ports 1 and 2, and 3 and 4 to force them in phase, thus making 1 and 4, and 2 and 3 out of phase inhibiting the E-field oscillation.

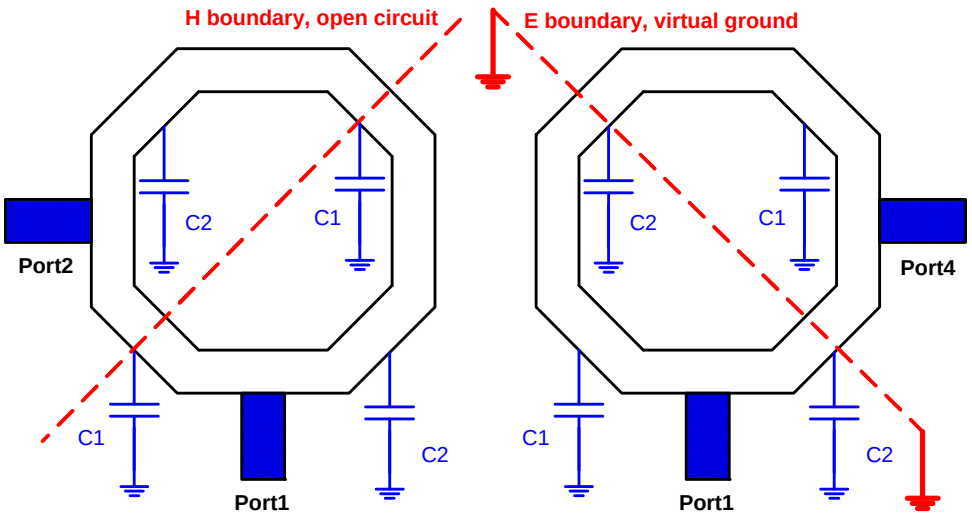


Figure 34, H mode selection

Two identical cross coupled pairs are connected to the resonator at the excitation ports as shown in Figure 35.

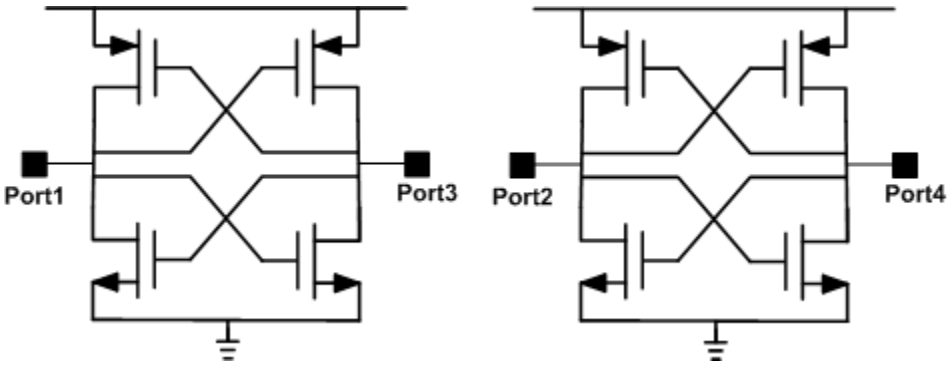


Figure 35, Cross coupled pairs connection at the excitation ports

A complementary (NMOS and PMOS) style is chosen to lower the power consumption (taking advantage of negative trans-conductance from PMOS and NMOS with the same current), as well as improve the flicker noise performance in the close-in phase noise spectrum due the symmetrical waveforms of the structure. The only two identical small varactors (not degrading the Q) are inserted across the cross-coupled pairs, ports 1 and 3 (2 and 4), controlled with same voltage. Fixed MoM capacitors are used for C_1 and C_2, with C_1 being smaller, thus providing the higher V band. To fully exploit the symmetry of the structure for finer controls, fixed MoM capacitors are also implemented between ports 1 and 2 (3 and 4), and 1 and 4 (2 and 3). When the ports are in phase the capacitor is open and in-effective, where as when 180 degrees out of phase the effective capacitance is doubled.

3.5. Resonator Implementation

The VCO is implemented in 65 nm CMOS technology, and the die picture is presented in Figure 36. In order to create contact points for the excitation ports and minimize the routing, the transmission line is bent in-ward at the ports. The area is 177 µm x 177 µm.

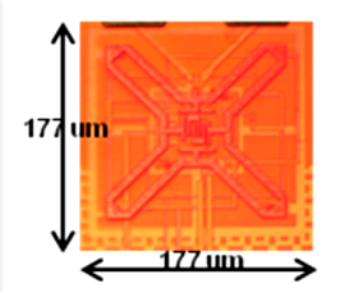


Figure 36, resonator die area picture, 177 um x 177 um

Figure 37 summarizes the measured tuning range for the implemented resonator shown in Figure 36 above.

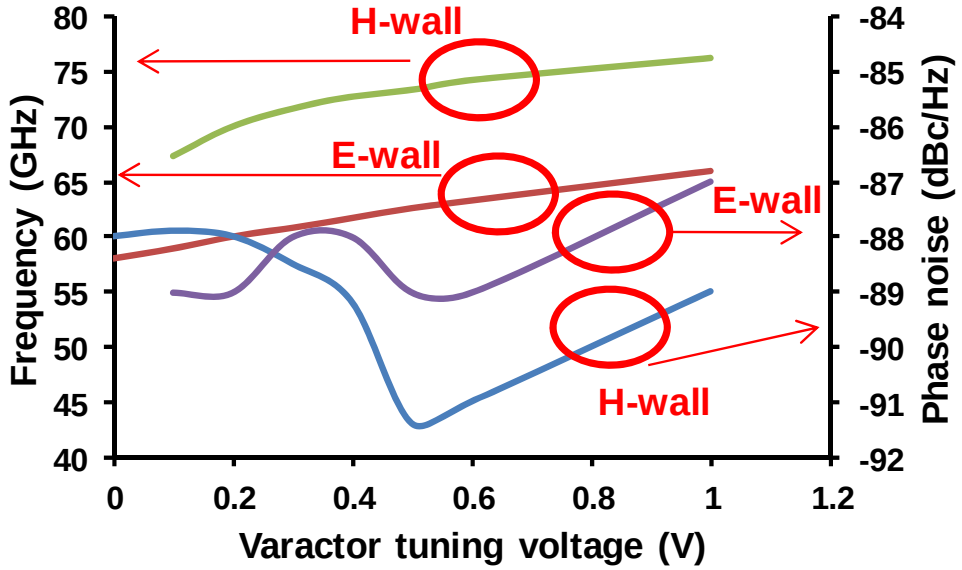


Figure 37, measured tuning curves the implemented resonator of Fig. 36

Chapter 4: VCO Implementation and Measurement

The goal of achieving a multi-band, multi-standard and globally connected, as well as a self-healing or reconfigurable smart radio that can optimize its performance in different circumstances and situations in order to maintain a high performance yield and reliability, has imposed many requirements on the frequency synthesizer unit of the transceiver system, hence the oscillator. One significant requirement is the frequency tuning which is being pursued by various schemes in the lower GHz regime (below the Ku band). However, there is a growing interest in transceiver design applications in the higher GHz bands, following similar ideas. For example, there is the unlicensed 57-64 GHz band, and the licensed trio of 71-76 GHz, 81-86 GHz, and 92-95 GHz applicable for wide-band short range wireless communication, and point-to-point fixed wireless communication such as last-mile access, respectively. Wireless chip-to-chip communication is another field where multi-band and concurrent frequency generation is of interest.

In the lower frequency range, switched capacitor banks [20] along with varactors, and often with switched inductors [21], are commonly incorporated. In the case of the switched capacitor banks, banks of capacitors of varying sizes (usually binary weighted) are switched in to control the resonance frequency, along with the varactors that control

the frequency in the analog sense. In the case of the switched inductors, the effective value of the inductance is changed by either switching in inductors of varying sizes, in analogy with the capacitor banks, or varying the mutual inductance amongst the inductors, thus providing a wider tuning range. Parasitic elements could desensitize the tuning elements, thus reducing the tuning range. Consequently, core transistor elements (e.g. cross coupled pairs) sustaining the oscillation are also switched in where not necessary to further enhance the frequency range [22]. In all these techniques, switches are used to enable the selectivity of the capacitor, inductor, or active cores. The transistor switches are in the resonating signal path and as the frequency increases, their loss and parasitic reactance deteriorates the performance by degrading the loaded-Q of the resonator, as well as reducing the frequency and tuning range. Consequently, other techniques have been envisioned in the millimeter wave frequency range to circumvent the switch issue as much as possible.

Another technique is to include multiple VCO units in the synthesizer and multiplex them, corresponding to each frequency range/band [23]. However, additional area is required for each VCO, and the multiplexer add loss. In order to minimize the deficiencies of the switch in the signal path, techniques have been introduced to minimize its operation in the oscillation cycle [24], [25].

In the resonator structure of [24], switches are still in the signal path, but are timed to control the dynamics of the bistable system, made of a network of capacitors and inductors, and they are only used to steer the oscillation from one state to the other. Once an oscillation is sustained, the switches are disabled, minimizing their defects on the

oscillation. The timing for the switches has to be precise, otherwise either a wrong frequency will be generated or the oscillation ceases to exist. Furthermore, the asymmetry of the oscillation could cause flicker noise up-conversion and thus poor phase noise performance.

In [25], differential mode vs. common mode capacitance is utilized in a network of capacitors and inductors to achieve two discrete tones. However, in order to produce more frequencies a much larger network of many inductors and capacitors is needed, increasing the complexity and area requirement.

The distributed nature of a transmission line has the capability of absorbing parasitic reactance and thus could be incorporated in oscillators. To achieve higher frequencies as well as wider bandwidths, a distributed resonator structure based on standing-wave Coplanar Stripline (CPS) is introduced in [26] where the length of the CPS is varied using transistor switches located along the line that short the two sides of the CPS. Varactors are also included as fine tuning elements. In [26], in order to cope with the aforementioned problems of the switch, particularly the ON-channel resistance, the switches are very big. The parasitic capacitance and poor R_{on}/R_{off} ratio degrades the frequency tuning, as well as phase noise and power requirements. The terminal parasitic capacitance and finite impedance of the cross-coupled pair could be a reason for both degrading the loaded quality factor (Q) of the tank, as well as limiting the negative trans-conductance introduced by the cross coupled pair at high frequencies. Consequently, the design in [27] introduces additional inductors at the gate of each of the cross coupled transistors, thus giving it a quasi-distributed nature. While effective, the work doesn't

exploit the full potential of a distributed design and introduces more lumped elements in the topology, which adds complexity and layout issues.

In this work, a technique is introduced that takes advantage of introducing orthogonal electrical-walls and magnetic-walls in a transmission line, thus controlling the tuning. As demonstrated, the technique is applicable to both concurrent frequency tones generating as well as achieving a continuous and very wide-bandwidth frequency sweep. The switching transistors that degrade the performance are avoided, and thus a good phase noise and low power consumption are achieved, as well as a small silicon space, compared to the aforementioned alternatives. The VCO results, designed and measured in 65-nm CMOS [28], using this technique, are presented. The VCO achieves greater than 18 GHz of continuous tuning range, and an improved Figure of Merit (FoM) when compared with that of prior techniques.

4.1. The concept of E-wall and H-wall control and its applications

Transmission lines, and wave propagation along them, have been investigated extensively in the literature [29]. Moreover, transmission lines of different lengths, corresponding to different electrical lengths, have been incorporated as tuning or resonating elements in various configurations. The unique distributed nature of transmission lines have been exploited in standing wave and travelling wave oscillators. Quarter wave-length transmission lines are of significance, where the resonance behavior is a function of the termination/loading of the line, in particular, open termination vs. short termination.

The idea of E-wall and H-wall control is to control the loading of a transmission line ring resonator, through inducing certain boundary conditions via the excitation, so that a short or open termination is invoked. Assuming capacitors are terminating a port of the resonator, if the transmission line is excited so that the port is a short circuit, the capacitors are ineffective in determining the resonance frequency. On the other hand, if the resonator is excited so that the port is invoked as open circuit, the terminating capacitors are effective in determining the resonance frequency.

Fig. 38 introduces the E-wall and H-wall control in a ring resonator. The four ports are the excitation sites, pair-wise, and the capacitor banks C_1 and C_2, identical along each axis of symmetry, are effective in determining the resonance frequency in each mode of operation, as discussed below.

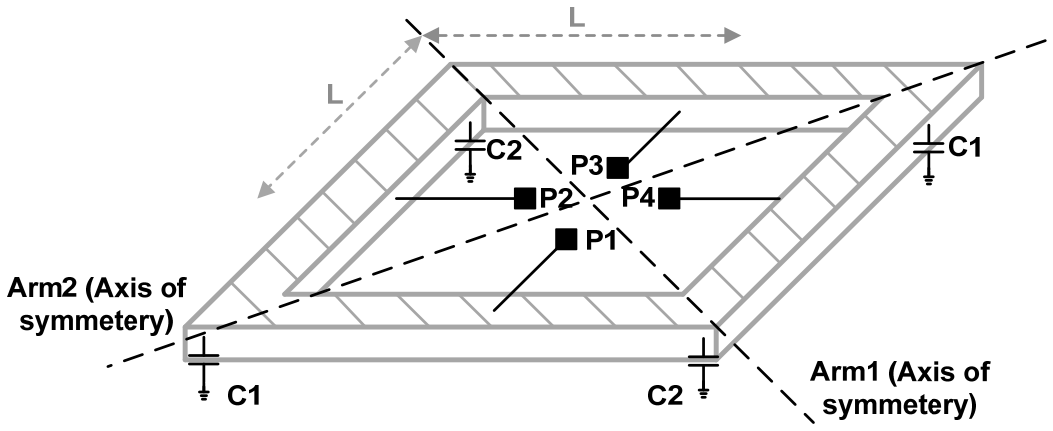


Figure 38, Ring shaped transmission line incorporating E-wall and H-wall excitation

In Fig. 38, port 1 and port 3 are always driven to be 180 degrees out of phase. Similarly port 2 and port 4 are always driven to be 180 degrees out of phase. On the other hand, port 2 and port 3 (and similarly port 1 and port 4) could either be in phase, or 180 degrees out of phase. Fig. 39 demonstrates the two scenarios.

Each of the two scenarios presented in Fig. 39 produce different resonance conditions; either a pure E-wall condition or H-wall condition is enforced, or a combination of the two, as discussed below. In Fig. 38, port 1 and port 3 are always driven to be 180 degrees out of phase. Similarly port 2 and port 4 are always driven to be 180 degrees out of phase. On the other hand, port 2 and port 3 (and similarly port 1 and port 4) could either be in phase, or 180 degrees out of phase. Fig. 39 demonstrates the two scenarios.

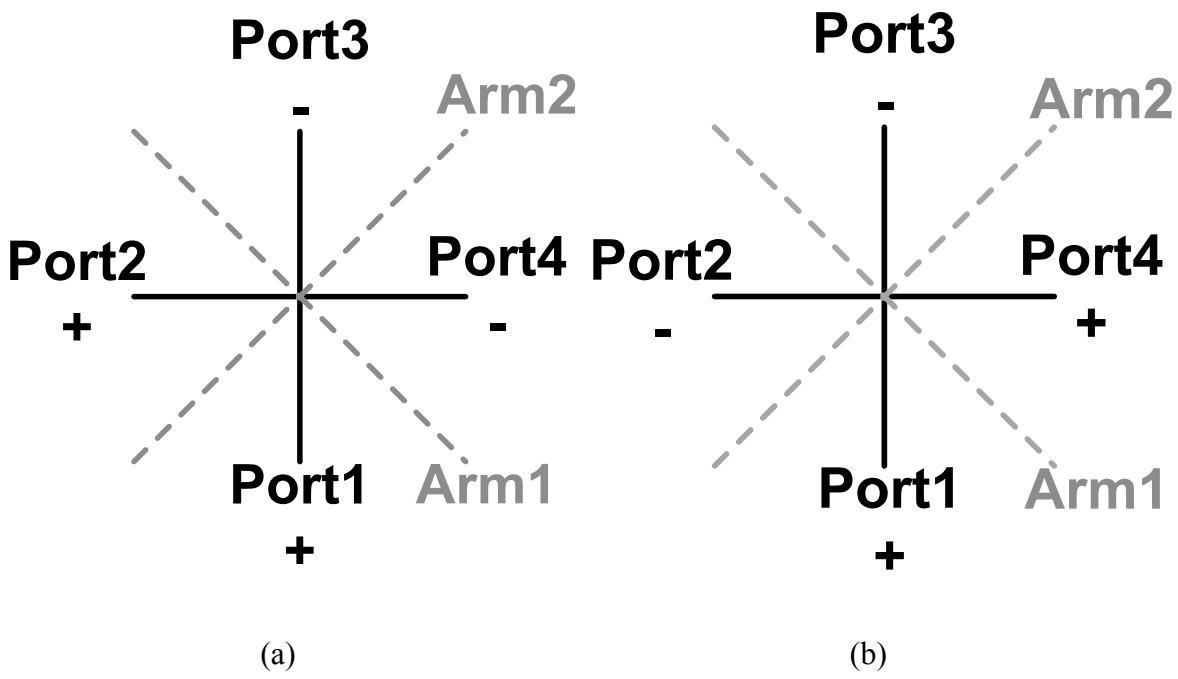


Figure 39, The four ports excitations for the ring shaped transmission line and the two scenarios (a) port 2 and port 3 (port1 and port 4) are 180 degrees out of phase (b) port 2 and port 3 (port 1 and port 4) are in phase.

Each of the two scenarios presented in Fig. 39 produce different resonance conditions; either a pure E-wall condition or H-wall condition is enforced, or a combination of the two, as discussed below. When ports 1 and 2 (ports 3 and 4) are excited in phase, as in Fig. 39 (a), Arm2 is an H-boundary and Arm1 is an E-boundary, thus creating an open circuit on Arm2 and a virtual ground on Arm1, as illustrated in Fig. 40. In the other scenario, Fig. 39 (b), when ports 1 and 2 (ports 3 and 4) are out of phase by 180 degrees, Arm2 is an E-boundary and Arm1 is an H-boundary, making Arm2 the virtual ground, and Arm1 the open, as illustrated in Fig. 41. Recognizing the symmetry of the structure, in the derivation that follows, only a pair of ports is considered. The two cases are analyzed to determine the resonance conditions.

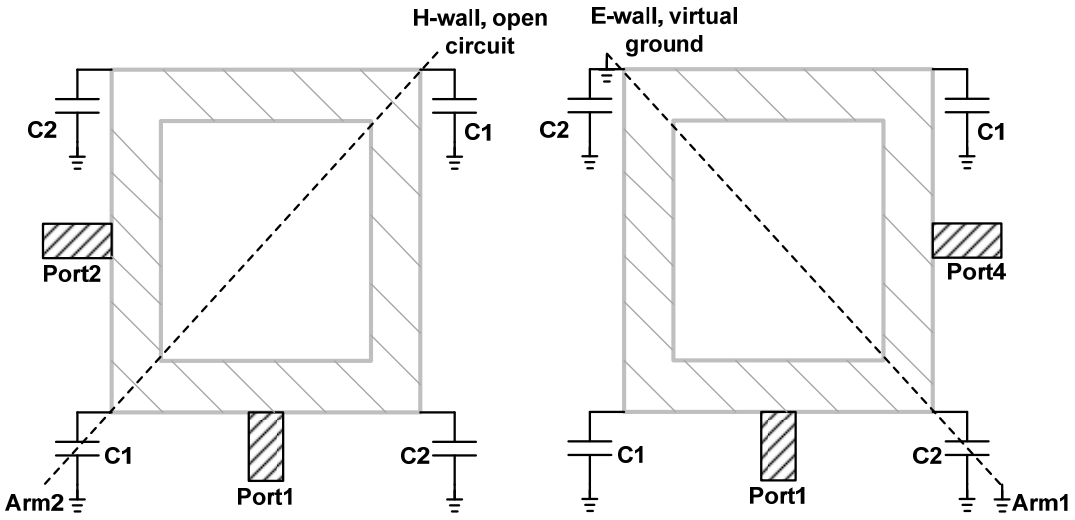


Figure 40, Transmission line resonator structure when ports 1 and 2 are in phase and ports 1 and 4 are 180 degrees out of phase.

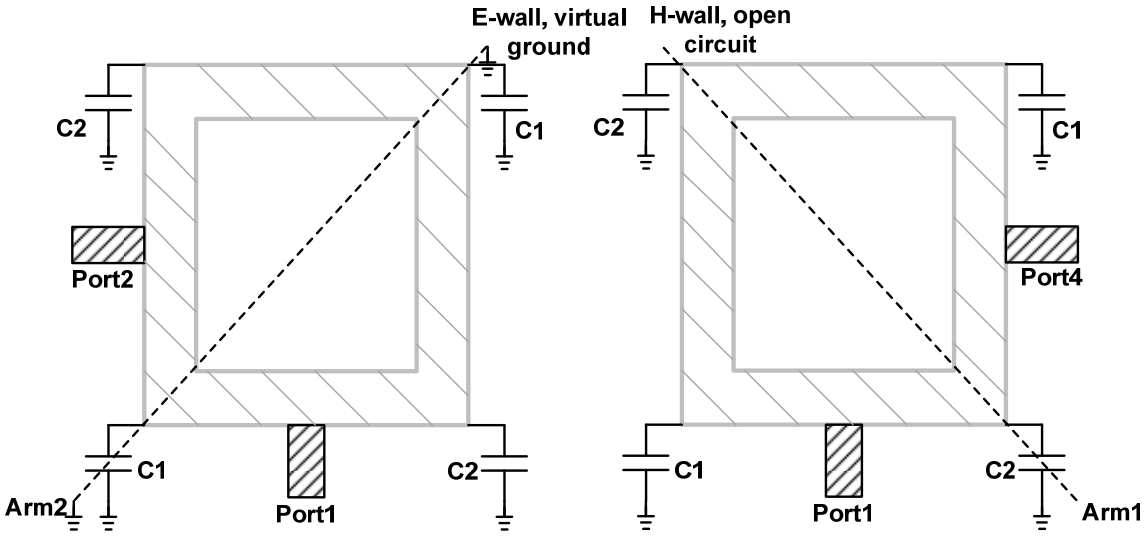


Figure 41, Transmission line resonator structure when ports 1 and 2 are excited 180 degrees out of phase and ports 1 and 4 are in phase.

Recognizing the symmetry of the structure, in the derivation that follows, only a pair of ports is considered. The two cases are analyzed to determine the resonance conditions. Fig. 40, where ports1 and 2 create an H-boundary, and ports 1 and 4 create an E-boundary, is expanded in Fig. 42.

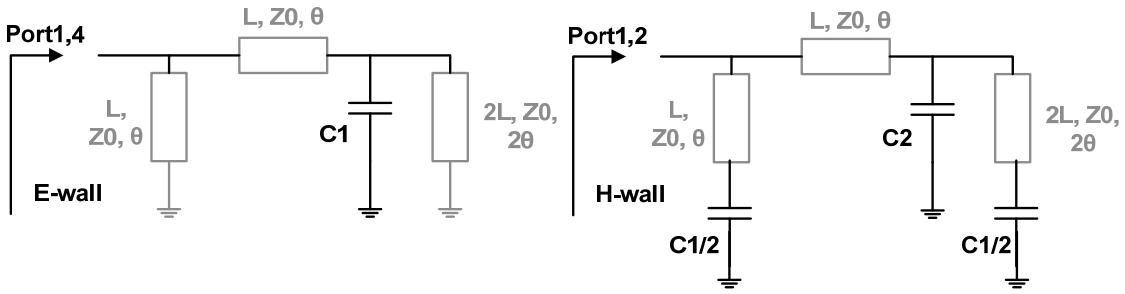


Figure 42, Ring shaped transmission line resonator analysis corresponding to Fig. 40, when ports 1 and 4 invoke an E-boundary and ports 1 and 2 an H-boundary.

In Fig. 42, L is the actual length of the transmission line (in accordance with Fig. 1), Z_0 is the characteristic impedance, and θ the electrical length. Solving for the equivalent impedance at the ports indicated in Fig. 42, and solving for resonance condition when the imaginary part is zero, (1) is derived. As can be seen, the Arm1 capacitance bank (C_2) is ineffective in determining the resonance condition.

$$\omega \cdot C_1 \cdot Z_0 = 2 \cdot \cot(2 \cdot \theta)$$

Fig. 41, where ports 1 and 2 invoke an E-boundary and ports 1 and 4 invoke an H-boundary is expanded in Fig. 43. Similar to Fig. 42, L denotes the actual transmission line length (in accordance with Fig. 36), Z_0 the characteristic impedance of the transmission line, and θ the electrical length.

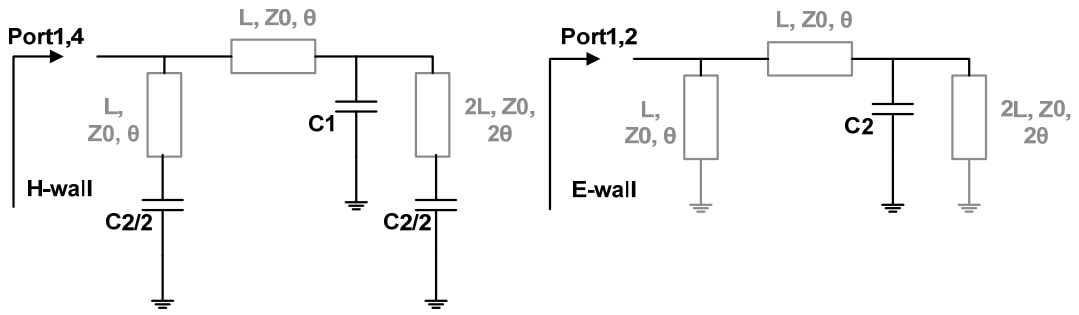


Figure 43, Ring shaped transmission line resonator analysis when ports 1 and 4 develop an H-boundary and ports 1 and 2 develop an E-boundary, corresponding to Fig. 41.

Solving for the resonance condition at the ports indicated in Fig. 43, (2) is derived. In this case, only the Arm1 capacitance bank (C_2) is effective in determining the resonance condition, and Arm2 is ineffective.

$$\omega \cdot C_2 \cdot Z_0 = 2 \cdot \cot\left(2 \cdot \theta\right)$$

As can be seen in the above equations, the resonance conditions are complements of each other, and could be tuned independently by selecting C_1 and C_2. The other designable parameters, common to both equations, are the characteristic impedance of the line and the electrical length.

4.2. Concurrent resonance tones

The orthogonal E-wall and H-wall control creates two co-existing resonance conditions, each one independently controlled, which could give rise to concurrent oscillation conditions; in fact, this is another way of looking at the orthogonal E-wall and H-wall control. Fig. 44 illustrates the impedance seen at the ports; the peaks happen when the imaginary part is zero.

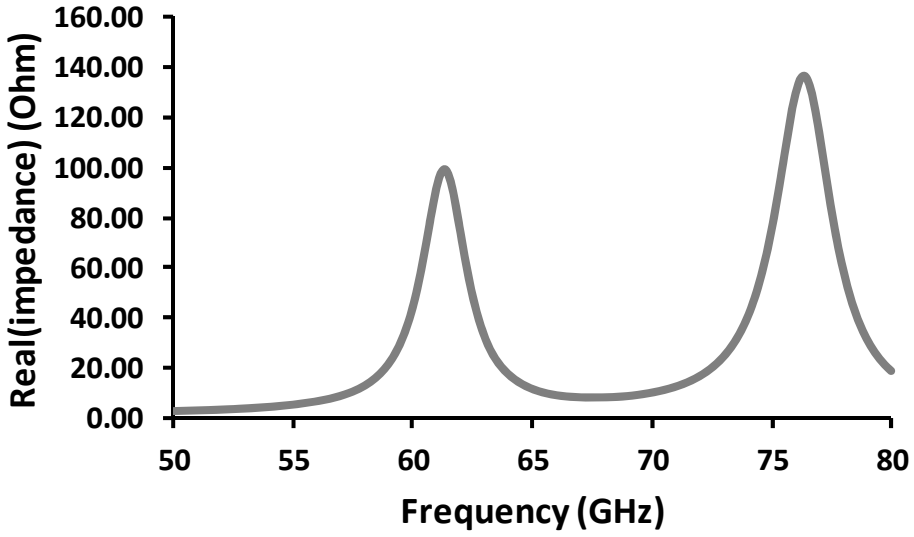


Figure 44, Real part of the impedance at the ports, imaginary part is zero at the peaks, demonstrating the possibility of co-existing resonance.

The two resonance of Fig. 44 are independently tunable, as predicted. This effect is illustrated in Fig. 45 and Fig. 46. In Fig. 45, C_2 is changing while C_1 is fixed. Notice how the lower resonance peak changes while the higher one (corresponding to Arm2) is fixed.

In Fig. 46, C_1 is changing while C_2 is fixed, and this time, the lower resonance peak corresponding to Arm1 is fixed whereas the higher resonance peak corresponding to Arm2 varies. The tuning independence of the E-wall and H-wall are clearly observable in these two figures.

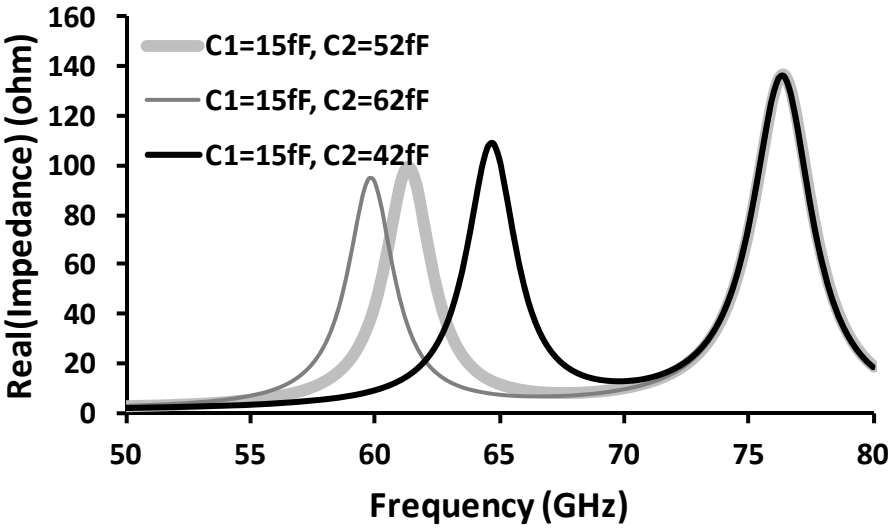


Figure 45, Coexisting resonance peaks, tuning the Arm1 capacitance. Notice how the higher peak corresponding to Arm2 is fixed.

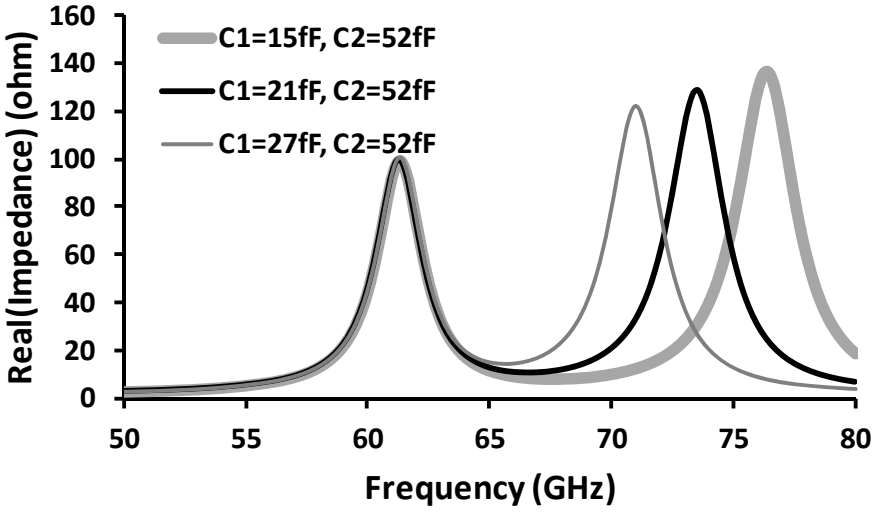


Figure 46, Coexisting resonance peaks, tuning Arm2 capacitance. Notice how the lower peak corresponding to Arm1 is fixed.

The concurrency principle just mentioned could also be exploited in designing ultra-wide bandwidth frequency generation circuits, such as Voltage Controlled Oscillators (VCO) and frequency dividers/multipliers. For example, the resonator could be excited under E-wall to generate the lower frequency bands, and independently excited under H-wall to cover the higher frequency bands. The above mentioned resonator, though implemented as single transmission line, could also be implemented as a differential CPS line, as illustrated in Fig 47.

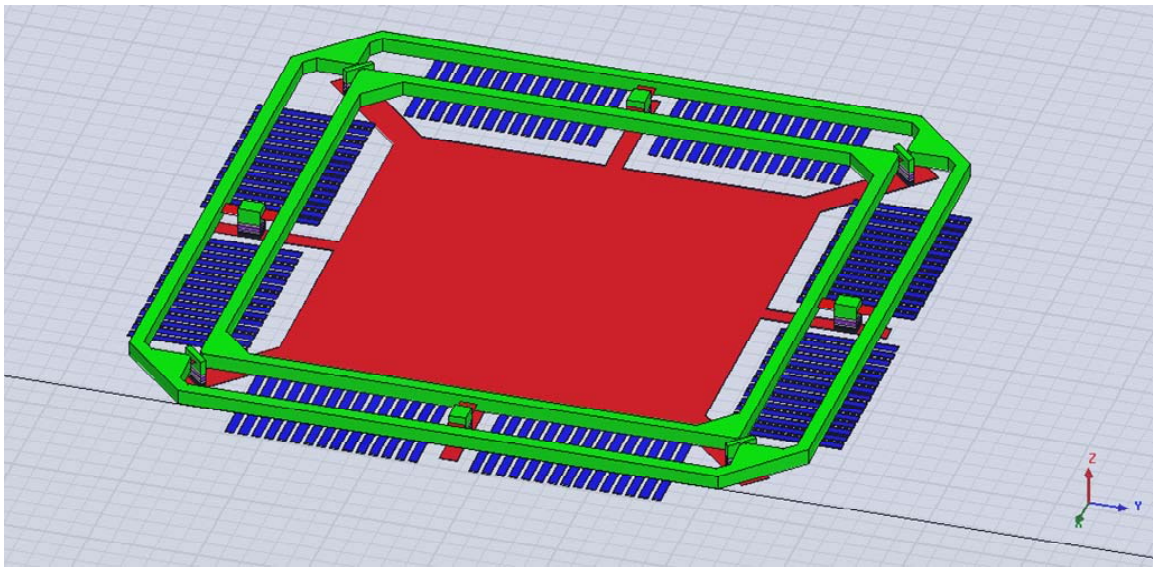
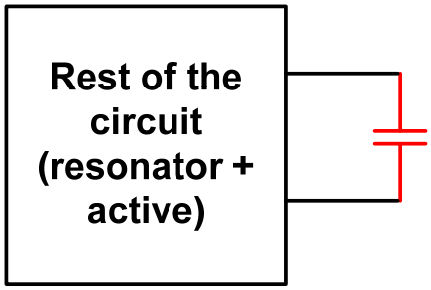


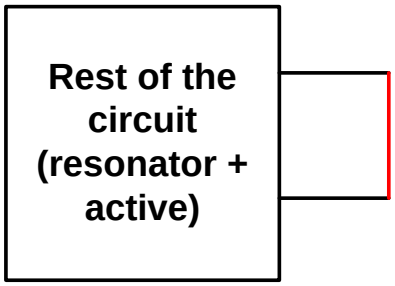
Figure 47, differential CPS implementation of the resonator

The idea of concurrency and multiple tone selection vs. ultra wideband signal frequency sweep could be generalized and summarized as in Fig 48, where depending on the excitation/boundary conditions the capacitor determines the resonance frequency; such that if the capacitor is shorted or open circuited, it factors into the resonance frequency. This ensures the potential for orthogonal co-existing resonance conditions, without the need for any switching.



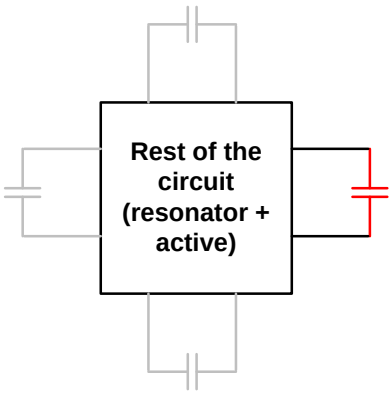
Mode 1

Case1:
Capacitor determines the resonance



Mode 2

Case2:
Capacitor doesn't determine the resonance



Generalization

Figure 48, generalization of the concurrent tone generation

4.3. Switch mode selection

In order to function as a wide-bandwidth resonator, instead of a concurrent tone one, it is important to dampen one of the tones so that only one tone is excitable, focusing the excitation energy. The idea is to selectively add sufficient loss to the undesired tone to dampen its response, selecting either the H-wall or E-wall boundary conditions. Since loss is only added to the undesired tone, the other desired one should be un-affected. This is performed by switching the phases of ports 1 and 2 (port 3 and 4). Since there are only two different phase orientations possible, diminishing one will enforce the other naturally. As illustrated in Fig. 49, four transistor switches are inserted between the ports, one between each of ports 1 and 2, ports 1 and 4, ports 3 and 2, and ports 3 and 4.

If the switch between ports 1 and 2 (ports 4 and 3) is closed, then ports 1 and 2 (ports 4 and 3) are in phase, making ports 1 and 4 (ports 3 and 2) 180 degrees out of phase. This condition is depicted in Fig. 45(a). In this case, the switch between ports 1 and 4 (ports 3 and 2) is left open. The result of such switching is presented in Fig. 50. Comparing the switch-less response in Fig. 50, with the switched response, the higher resonance peak is untouched, whereas the lower peak is dampened a lot. The switch does not deteriorate the desired response; it only diminishes the undesired.

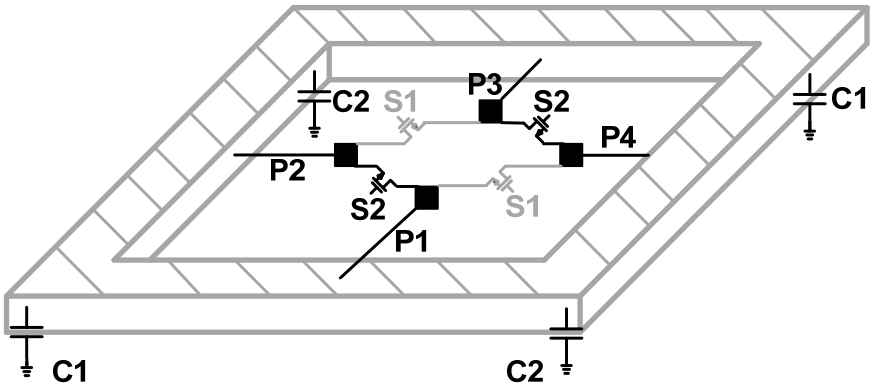


Figure 49, location of the four switches used for phase selection. S1 forces ports 2 and 3 (ports 1 and 4) to be in phase (corresponding to Fig. 45(b)), while ports 1 and 2 (ports 3 and 4) are out of phase. S2 forces the alternate configuration (corresponding to

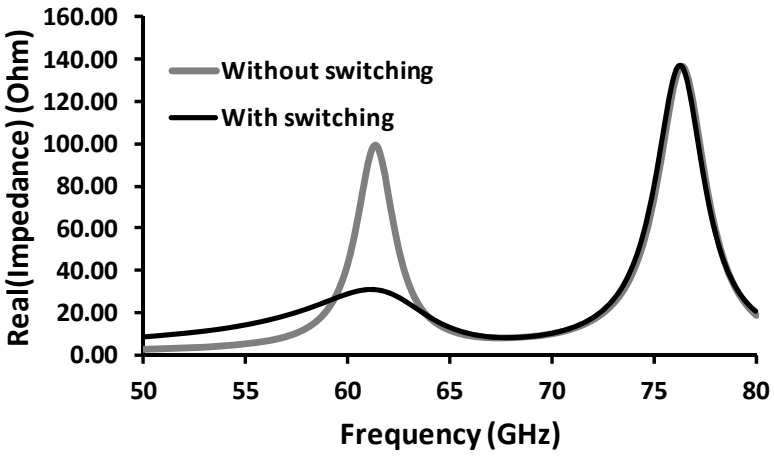


Figure 50, Switching and mode selection, ports 1 and 2 (ports 4 and 3) are in phase, whereas ports 1 and 4 (ports 3 and 2) are 180 degrees out of phase, corresponding to Fig. 45(a).

If the switch between ports 1 and 2 (ports 4 and 3) is closed, then ports 1 and 2 (ports 4 and 3) are in phase, making ports 1 and 4 (ports 3 and 2) 180 degrees out of phase. This condition is depicted in Fig. 45(a). In this case, the switch between ports 1 and 4 (ports 3 and 2) is left open. The result of such switching is presented in Fig. 49. Comparing the switch-less response in Fig. 49, with the switched response, the higher resonance peak is

untouched, whereas the lower peak is dampened a lot. The switch does not deteriorate the desired response; it only diminishes the undesired.

On the other hand, if the switch between ports 1 and 4 (ports 3 and 2) is closed, then ports 1 and 4 (ports 3 and 2) are in phase, making ports 1 and 2 (ports 3 and 4) 180 degrees out of phase. This condition is depicted in Fig. 45(b). In this case, the switch between ports 1 and 2 (ports 3 and 4) is left open. The switching response is illustrated in Fig. 51. Similar to the previous case, comparing the switched versus switch-less case, the desired resonance tone is untouched, while the other is heavily dampened.

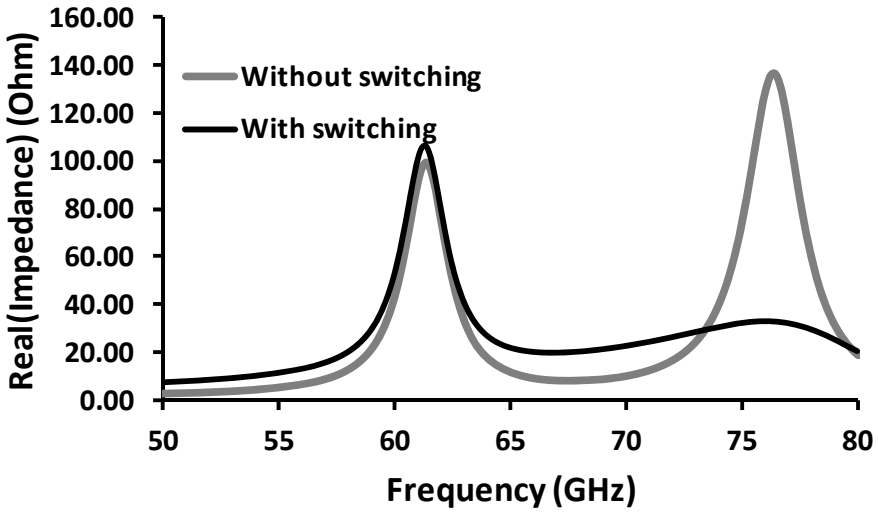


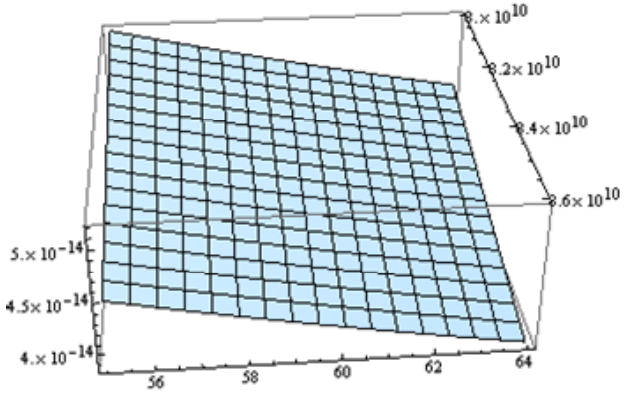
Figure 51, Switching and mode selection, ports 1 and 4 (ports 3 and 2) are in phase, whereas ports 1 and 2 (ports 3 and 4) are 180 degrees out of phase, corresponding to Fig. 45(b).

As observed, in the case of E-wall and H-wall control, the mode selection switches don't degrade the desired resonance response and only affect the undesired tone. This is due to the fact that there are two degrees of freedom and by diminishing one, the other is untouched. As a result, the proposed technique doesn't suffer from the downfalls

of the others involving the switches, in particular, the Q-limitations and parasitic capacitance and resistance. In the next section, the V-band VCO designed using this technique, achieving a record FoM is presented.

4.4. The V-band VCO

The four parameters of C_1, C_2, Z_0 and θ are optimized in the design of the VCO [19] to achieve the continuous frequency tuning of 58 GHz to 76.2 GHz. A representative optimization curve for the higher V-band coverage is presented in Fig. 52. In this figure the selection of Arm1 capacitance bank and the characteristic impedance of the transmission line are considered.



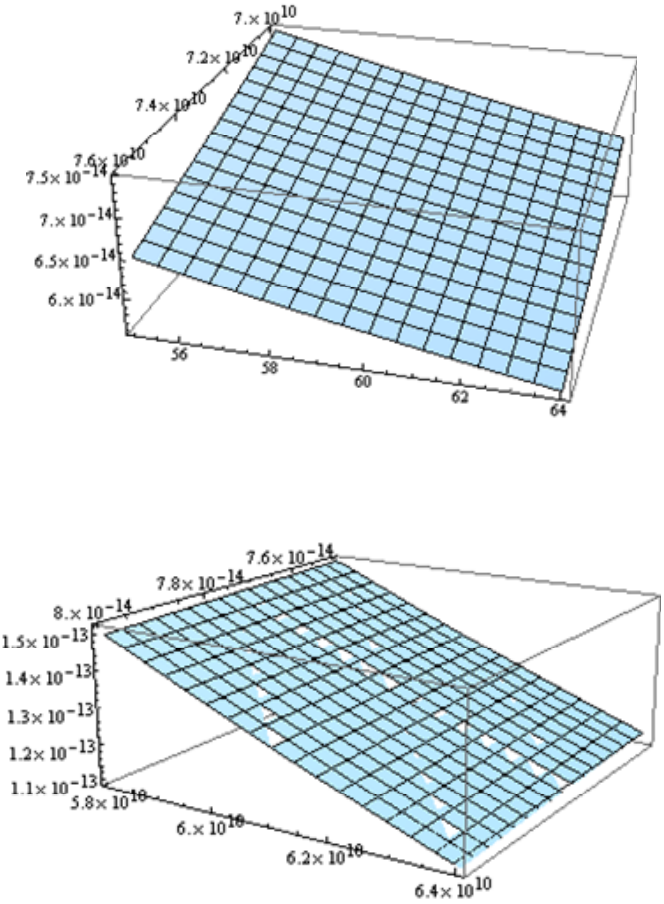


Figure 52, Optimization of Arm1 capacitance bank and the transmission line characteristic impedance for the higher V-band frequency coverage.

The VCO is implemented in the 65-nm CMOS technology. The ring resonator is optimized using full-wave simulators (Ansoft HFSS) to optimize the Q in accordance with the designed characteristic impedance from the frequency selection optimization stage just described. The transistor switches are implemented using a single NMOS. As discussed, the switches, when enabled, only affect the undesired mode (E-wall/H-wall, damping the resonance). They have no influence on the desired mode (H-wall/E-wall), and there is no restriction on their parameters. So that the dampening ratio is sufficient, they are chosen small (4 μm/0.065 μm). Amongst the oscillator core topologies possible (Colpitts, Hartley, to name a few), the four ports are excited with complementary cross coupled pairs (with NMOS and PMOS), as illustrated in Fig. 53. Due to the symmetry, the required 180 degrees phase shifts between the mutual ports 1 and 3 (ports 2 and 4) are generated inherently. Although a differential Colpitts core is also possible, similar to [20], additional lumped elements are required, as well as a higher DC current for start-up, increasing the power and design complexity, not to mention the sensitivity to parasitic capacitance which could drift the phase. Moreover, the cross-coupled pair has the additional benefit that taking advantage of the negative trans-conductance from both the PMOS and NMOS drawing the same current, it is possible to lower the power consumption, as well as to improve the flicker noise performance in the close-in phase noise spectrum due to the symmetrical waveforms of the structure.

The VCO silicon die photo is presented in Fig. 54; it occupies 177 μm x 177 μm. The axis of symmetry (in accordance with Fig. 1), as well as the location of the ports and cross coupled pairs, are also highlighted.

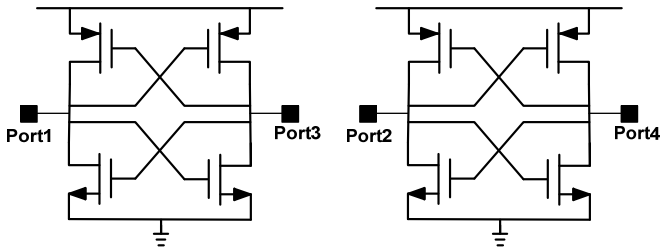


Figure 53, The two cross-coupled pairs exciting the resonator at the ports.

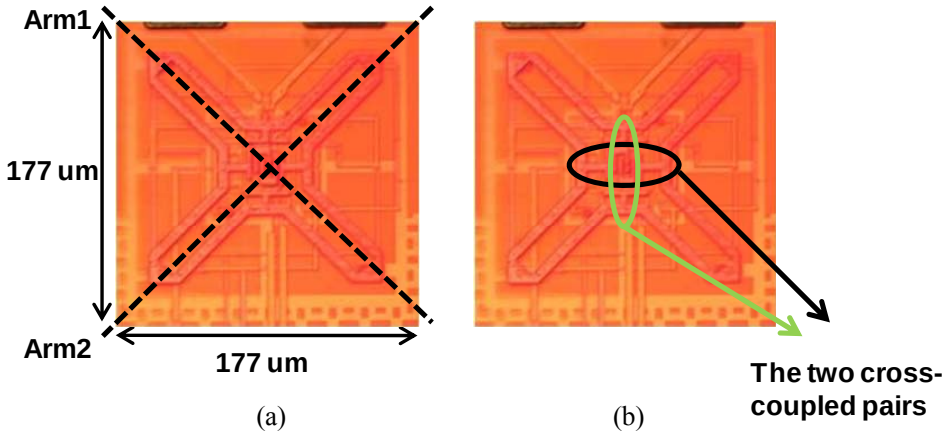


Figure 54, VCO silicon die, showing (a) the two axis of symmetry and (b) the location of the ports/cross-coupled pairs connection, in accordance to Fig. 1.

The ring transmission line resonator is bent in order to create contact points for the ports and the cross coupled pairs, minimizing the routing and loss. The output is extracted single-ended from port 1 through an open drain buffer, probed as GS. The buffering transistor has the same size as the cross coupled pair NMOS. In order to balance the loading, ports 2, 3 and 4 are also loaded by a similarly sized buffering transistor. A varactor is connected across the ports 1 and 3, ports 2 and 4, and fixed metal-over-metal (MoM) capacitors are used as capacitor banks C_1 and C_2, connecting at Arm2 and Arm1 respectively, as illustrated in Fig. 55.

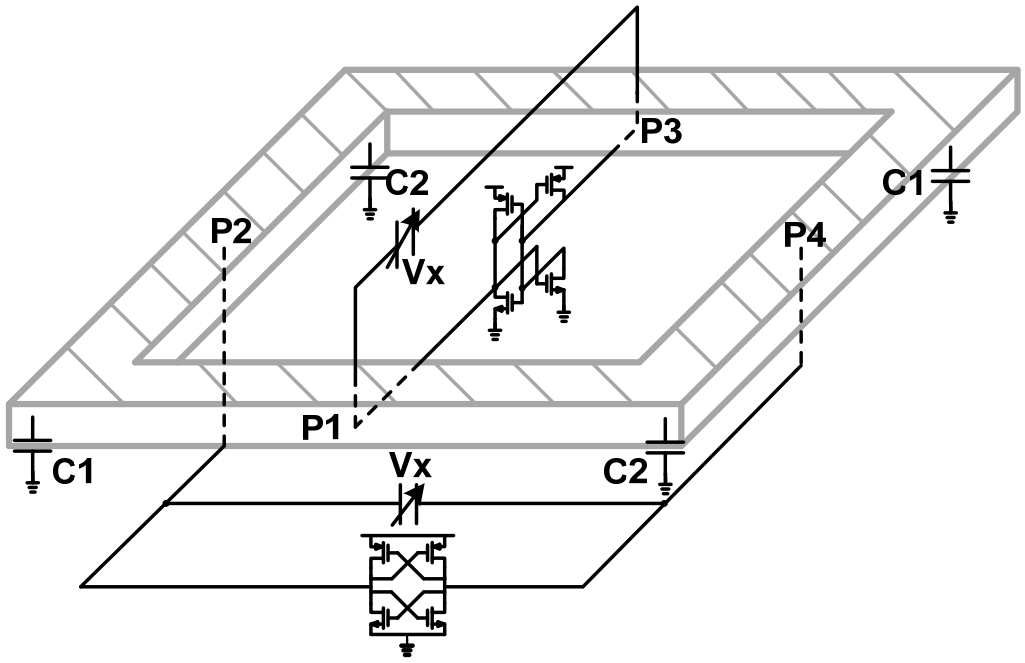


Figure 55, location of the two varactors implemented along with the cross-coupled pairs across ports 1 and 3 (ports 2 and 4). The four switches (Fig. 10) are not shown to improve clarity.

To further introduce tuning control and a finer resolution, varactors could also be added with the MoM capacitors at Arm1 and Arm2, as well as between ports 2 and 3 (ports 1 and 4), and ports 1 and 2 (ports 3 and 4), where each set is controlled with the same tuning control, as illustrated in Fig. 56. An additional advantage of the structure is the effective doubling of the varactor tuning range, due to phase reversal. Referring to Fig. 56, when ports 2 and 3 (ports 1 and 4) are in phase, the varactor controlled by V_{t2} are ineffective; whereas when the ports 2 and 3 (ports 1 and 4) are out of phase, the same varactor is effectively doubled in tuning. The same holds for varactor controlled by V_{t1}. Varactors controlled by V_{tC2} and V_{tC1} are effective, when Arm1 and Arm2 are magnetic walls (as illustrated in Fig. 2), respectively, and are ineffective in case Arm1 and Arm2 are electrical walls, respectively.

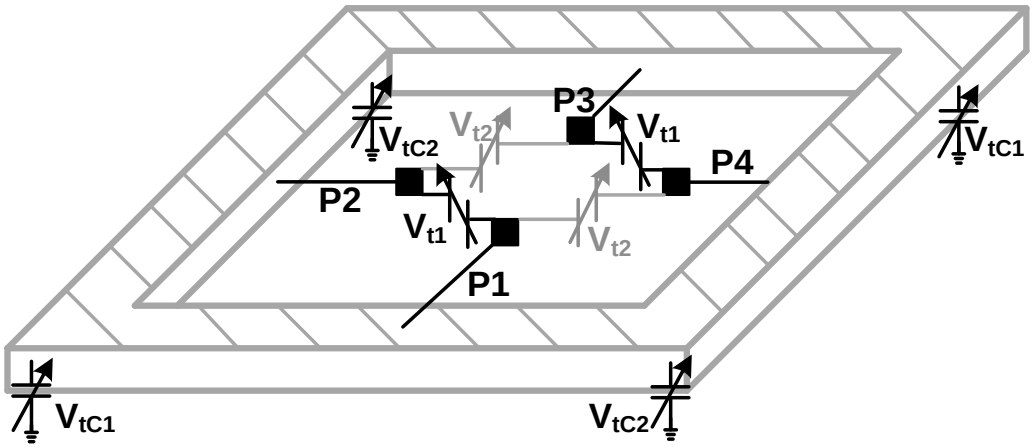
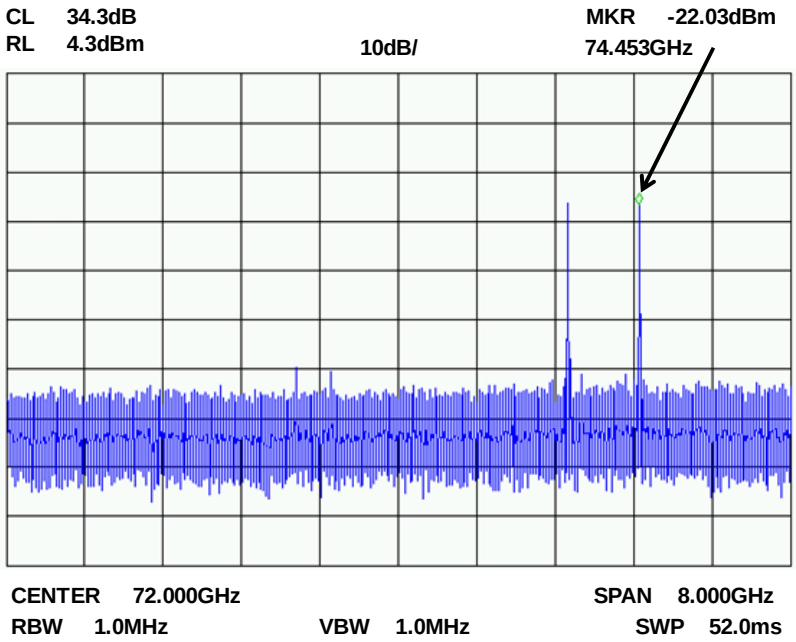


Figure 56, other possible varactor locations for further tuning control. Varactors are controlled pair-wise. When ports are in phase, the varactors are ineffective, whereas when ports are out of phase varactors' tune-ability is doubled.

The VCO is measured using a harmonic mixer on the spectrum analyzer. Two sample tones are presented in Fig. 57. In the spectrums captured, the right tone is the signal and the left is the image. The loss in the harmonic mixer is de-embedded, but the loss in the cable is not and is about -15 dB.



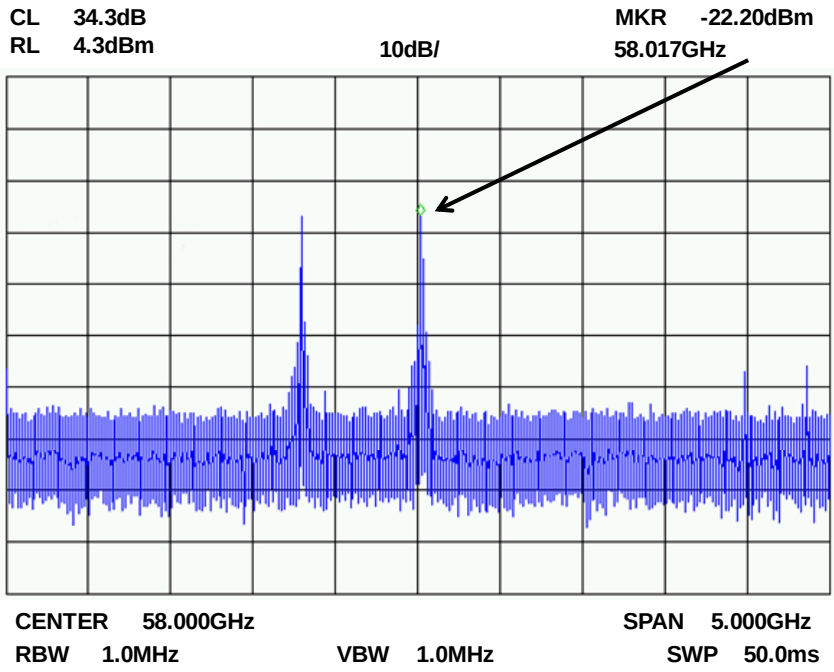


Figure 57, output spectrums from VCO, measured using harmonic mixer. The left tone is the image signal.

A sample phase noise plot is illustrated in Fig. 58. The VCO is free-running, and the phase noise is averaged out over 10 measurements to improve accuracy. As mentioned, for proof of concept, and to demonstrate the continuous wide-band tuning capability of the technique, only one pair of varactor is used. Fig. 59 captures the tuning, and phase noise performance corresponding to E-wall and H-wall tuning modes. More varactors could be included at the points of symmetry (as mentioned before) in order to produce a finer control. The VCO consumes 5.8 mW from a 1.0 V supply, excluding the output buffer. A comparison with previously published continuous tuning VCO in literature is conducted in Table 60. Figure of Merit (FoM) is evaluated according to

$$FoM(\Delta f) = L\{\Delta f\} - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P_{DC}}{1mW}\right) - 20\log\left(\frac{TR}{10}\right)$$

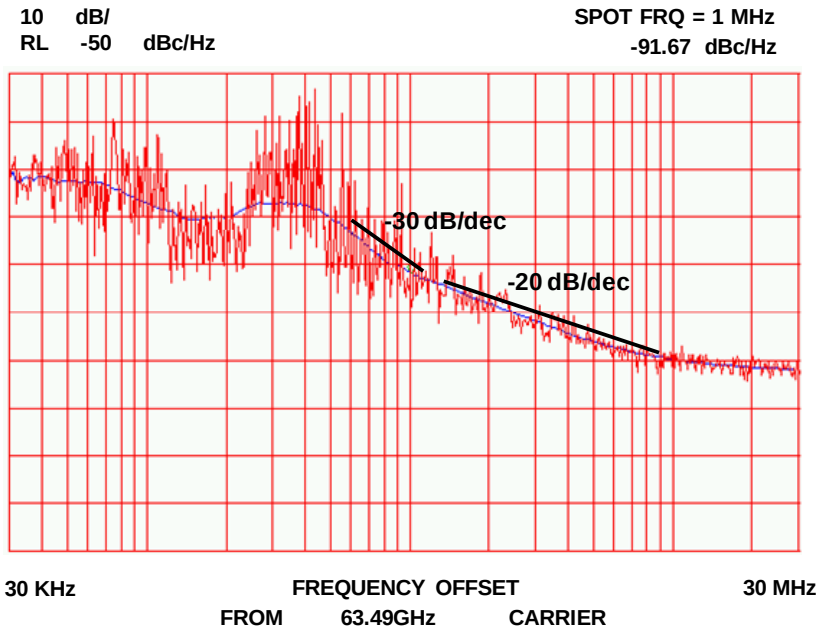


Figure 58, sample phase noise plot, measured at 1 MHz offset from the carrier frequency at 63.49 GHz, -91.67 dBc/Hz

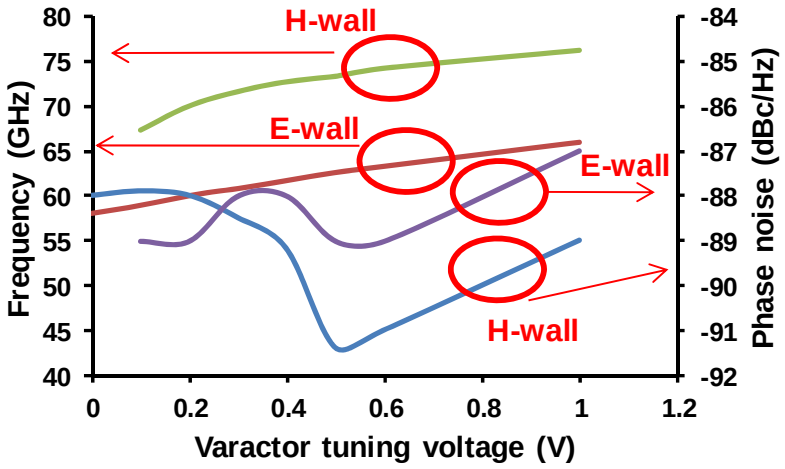


Figure 59, Tuning frequency and phase noise for mode 1 (E-wall) and mode 2 (H-wall)

Ref.	F_0 (GHz)	TR (%)	Phase noise (dBc/Hz)	Pdc (mW)	FoM (dBc/Hz)	Tech.
[15]	58.4	9.32	-91@1MHz	8.1	-176.7	90nm, CMOS
[16]	49.9	12	-87@1M	10.4	-172.4	90nm, CMOS
[17]	60	16.7	-97.1@1M	30	-182.3	65nm, CMOS
[18]	39.9	15.1	-98.1@1M	14.4	-182.1	65nm, CMOS
[19]	64	8.75	-95@1M	3.16	-185	90nm, CMOS
[20]	56.5	14.7	-92@1M	21	-177.3	90nm, SOI
[21]	70.2	9.55	-106.1@10M	5.4	-175.4	65nm, SOI
[22]	56.5	10.3	108@10M	9.8	-173.4	0.13µm CMOS
[23]	49.5	2.21	-99.7@1M	13	-169.3	0.25µm CMOS
This	**67.1**	**27**	**-89.5@1M**	**5.8**	**-187**	**65nm, CMOS**

Figure 60, state-of-the-art FoM comparison table for continuously tuned VCOs

Chapter 5: Ultra-wideband concurrent frequency divider

Injection locked circuits, including frequency dividers, are capable of achieving high center frequency and low power due to the resonance characteristic of the tuned tank; which coincidentally translates into a narrow bandwidth, compared with other architectures that don't rely on injection locking. The availability of new high frequency bands, for wider bandwidths and information transfer, at 60 GHz and beyond, for applications such as wireless media and interconnect, require high frequency/performance frequency synthesizers. This, in turn, mandates the use of wide-bandwidth injection locked frequency dividers in the loop, following the Voltage Controlled Oscillator (VCO). In order to simplify the synthesizer control loop it is crucial to avoid the use of varactor in the divider. As a result the divider should be robust and cover the entire VCO frequency band in presence of process/voltage/temperature (PVT) variations.

In order to enhance the limited locking range of injection locked circuits, many research have been invested in optimizing the injection mechanism, as well as optimizing the tuned tank structure. Since the pulling range is inversely proportional to the tank's quality factor (Q), intentional lowering of the Q (by adding losses) could improve the

locking range [25]. However, the problem would be the higher power required to startup and sustain the oscillator. Considering the injection locking operation principle and the effect of the signal harmonics, boosting the second order harmonics of the input injection is introduced. Following this approach, shunt peaking/resonance of the biasing transistor's parasitic at the second harmonic, and that of the buffering transistor are investigated [26]. In applications where injection locking is employed for frequency division, considering the similarities of the injection locked divider and miller divider, the injecting transistor is treated as a current mode mixer and designed accordingly [27]. However, due to process variations, the techniques are hard to optimize to tune out the parasitic, and thus produce unwanted spurs.

In this work a novel idea is introduced, in continuation of the work presented by the authors earlier on an ultra-wideband VCO, utilizing the concurrent orthogonal resonance modes of a distributed standing ware structure [28]. The technique achieves a very wide band injection locking range, without the additional trade-off/complexity side-effects of the earlier methods. To illustrate the idea, a divider-by-two injection locked divider is fabricated in CMOS 65nm process, and measures a new Figure of Merit (FoM).

5.1. The concept of orthogonal modes and application to injection locking

The frequency pulling range around the resonance frequency of classical injection locked circuits is pictorially illustrated in Fig. 61(a), and could be approximated by the equation below, where ω_0 is the tank's resonance frequency, Q is the tank's loaded quality factor, I_{inj} and I_{osc} are the injection and the oscillation current amplitudes, respectively.

$$\omega_{lock} \approx \frac{\omega_0}{2 \cdot Q} \times \frac{I_{inj}}{I_{osc}}$$

In Fig. 61(a), the resonance frequency is the single unstable point of the circuit, where oscillation is possible. If there were multiple such unstable points, the oscillator could potentially oscillate at more than one frequency, thus creating a concurrent oscillator. Moreover, this could be helpful in enhancing the pulling range, thus the locking frequency range, as depicted in Fig. 61(b), and explained below.

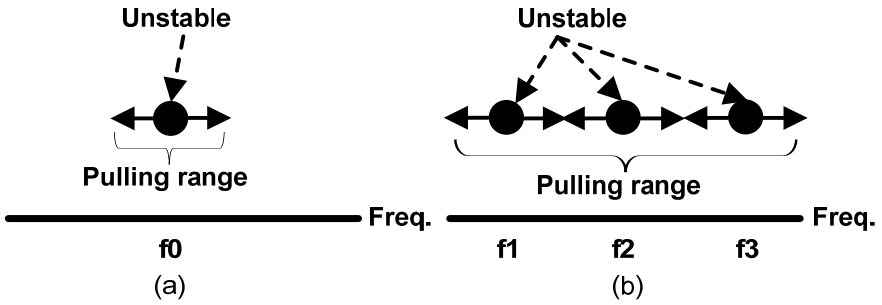


Figure 61, Frequency pulling around (a) single unstable point (b) multiple (three) unstable points

Out of the multiple possible unstable points, one could be selected as the resonance frequency over the others by forcing and thus shifting the equilibrium point. The shifting of the equilibrium point could be achieved by either adding losses selectively to resonance peaks, or forcing the condition by applying an external signal, thus injection locking. In the scenario where the external injected signal manipulates the equilibrium, the injected signal decides which of the unstable points will be the only oscillation frequency, since only one of the unstable points would be perturbed and thus only that one will sink all the energy. An alternative thinking is that since the injected signal is outside the pulling range of one resonance tone, that particular unstable point will be dampened, and instead the other unstable point within the range will resonate; this view point is further depicted in Fig. 62.

Considering the aforementioned discussion, a wideband locking range could be achieved by having a multiple-resonance block, where the pulling range around each resonance tone could add up to an overall ultra-wideband locking range, as depicted in Fig 61(b), and captured in equation below.

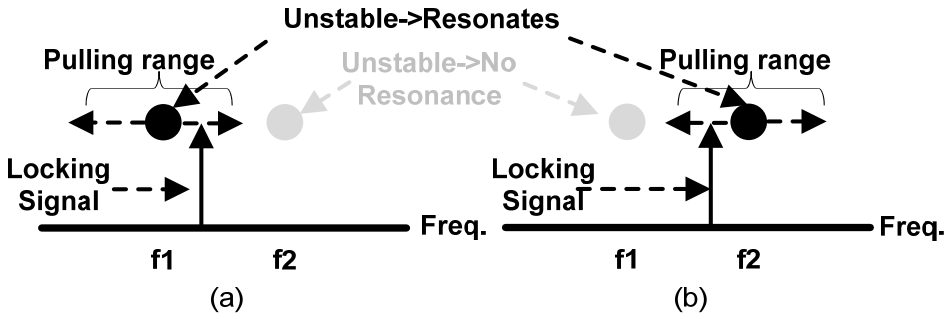


Figure 62, selecting the resonance point, between the two unstable points, by injecting and locking an external signal (a) when injection signal frequency is within f1's pulling range (b) when injection signal frequency is within f2's pulling range.

$$\omega_{lock} \approx \frac{\omega_{o1}}{2 \cdot Q_1} \times \frac{I_{inj1}}{I_{osc1}} + \frac{\omega_{o2}}{2 \cdot Q_2} \times \frac{I_{inj2}}{I_{osc2}} + \cdots \frac{\omega_{on}}{2 \cdot Q_n} \times \frac{I_{injn}}{I_{oscn}} - \omega_{overlap}$$

In the equation, the loaded quality factors (Q), depend on each individual unstable resonance at the corresponding resonance frequency (ω). The current injection amplitude, as well as the oscillation current amplitude, are functions of frequency also, given the parasitic and the f_T limitations of the transistor. The $\omega_{overlap}$ factor accounts for the overlap in the pulling range of individual resonance tones, in order to ensure a continuous range.

Realizing the potential advantage of the aforementioned idea for injection locked circuits, the goal is to device a concurrent oscillator which oscillation frequencies could be tuned/perturbed independently of each other; being orthogonal.

5.2. Concurrent and orthogonal modes

The required concurrency, and orthogonality, aforementioned could be implemented in a distributed style using the E-wall (electric-field wall) and H-wall (magnetic-field wall) technique [29]. The idea of E-wall and H-wall technique is to control the loading of a transmission line, by various excitations, so that a short or open termination is invoked. Assuming capacitors are terminating a port of the transmission line, if the transmission line is excited so that the port is a short, the capacitors are ineffective in determining the resonance frequency. On the other hand, if the transmission line is excited so that the port is invoked as open, the terminating capacitors are effective in determining the resonance frequency. Fig. 51 introduces the E-wall and H-wall control in a ring shaped transmission line. As it is elaborated below, in this scenario there are only two concurrent and orthogonal frequencies possible. The technique could be further expanded to achieve more unstable points.

In Fig. 51 the four ports (P1-4) are the excitation sites, pair-wise, and the capacitor banks C_1 and C_2, identical along each axis of symmetry, determine the resonance frequency in each mode of operation, as described below. In Fig. 51, port 1 and port 3 are always excited to be 180 degrees out of phase. Similarly, port 2 and port 4 are always excited to be 180 degrees out of phase. On the other hand, port 2 and port 3 (and similarly port 1 and port 4) could either be in phase, or 180 degrees out of phase. Fig. 52 demonstrates the two scenarios.

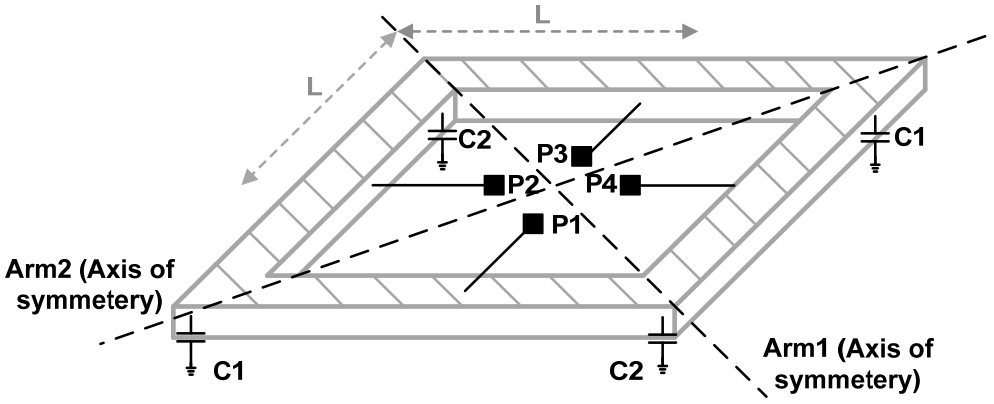


Figure 63, ring shaped transmission line incorporating E-wall and H-wall excitation

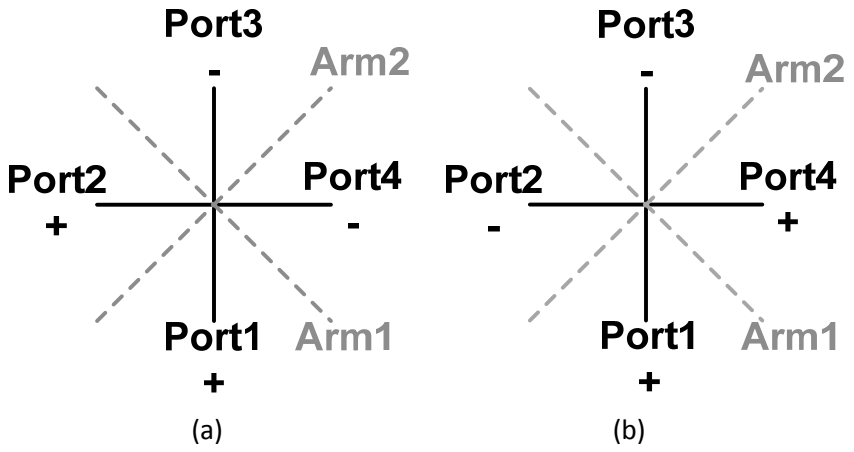


Figure 64, The four ports excitations for the ring shaped transmission line and the two scenarios (a) port 2 and port 3 (port1 and port 4) are 180 degrees out of phase (b) port 2 and port 3 (port 1 and port 4) are in phase

Each of the two scenarios presented in Fig. 64 produce different resonance conditions; either a pure E-wall condition is enforced or an H-wall condition, or a combination of the two. When ports 1 and 2 (ports 3 and 4) are excited in phase, as in Fig. 64(a), Arm2 is an H-boundary and Arm1 is an E-boundary, thus creating an open circuit on Arm2 and a virtual ground on Arm1, as illustrated in Fig. 65.

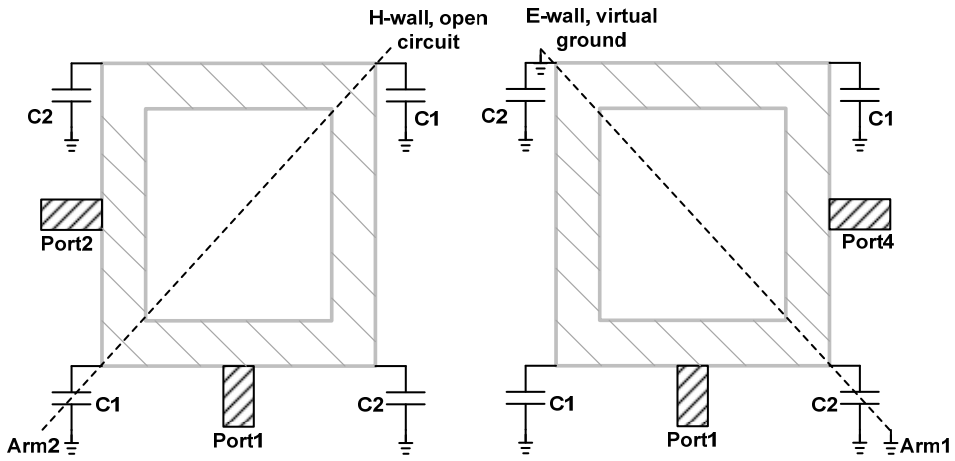


Figure 65, Transmission line resonator structure when ports 1 and 2 are in phase and ports 1 and 4 are 180 degrees out of phase.

In the other scenario, Fig. 4(b), when ports 1 and 2 (ports 3 and 4) are out of phase by 180 degrees, Arm2 is an E-boundary and Arm1 is an H-boundary, making Arm2 the virtual ground, and Arm1 the open, as illustrated in Fig. 6. Recognizing the symmetry of the structure, in the derivation that follows, only a pair of ports is considered. Fig. 5, where ports 1 and 2 create an H-boundary, and ports 1 and 4 create an E-boundary, could be expanded as in Fig. 7. Similarly, Fig. 6, where ports 1 and 2 invoke an E-boundary and pots 1 and 4 invoke an H-boundary could be expanded as in Fig. 8.

In Fig. 7 and Fig. 8, L is the actual length of the transmission line (in accordance with Fig. 3), Z_0 is the transmission line characteristic impedance, and θ is the electrical length of the transmission line. Solving for the equivalent impedance at the ports indicated in Fig. 7, the resonance condition, when the imaginary part of the impedance is zero, is arrived at.

$$\omega \cdot C_1 \cdot Z_0 = 2 \cdot \cot(2 \cdot \theta)$$

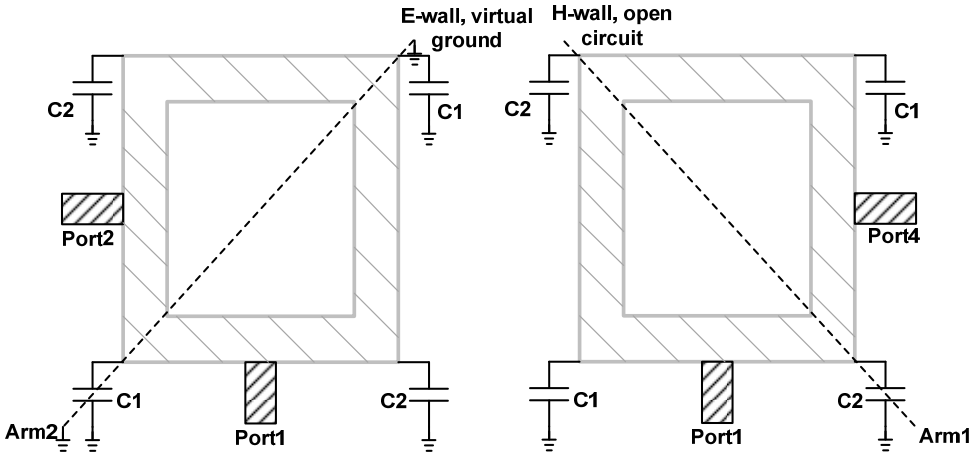


Figure 66, Transmission line resonator structure when ports 1 and 2 are excited 180 degrees out of phase and ports 1 and 4 are in phase.

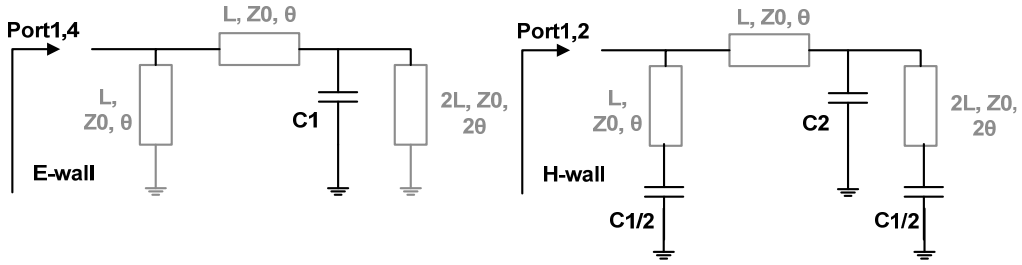


Figure 67, Ring shaped transmission line resonator analysis corresponding to Fig. 3, when ports 1 and 4 invoke an E-boundary and ports 1 and 2 an H-boundary

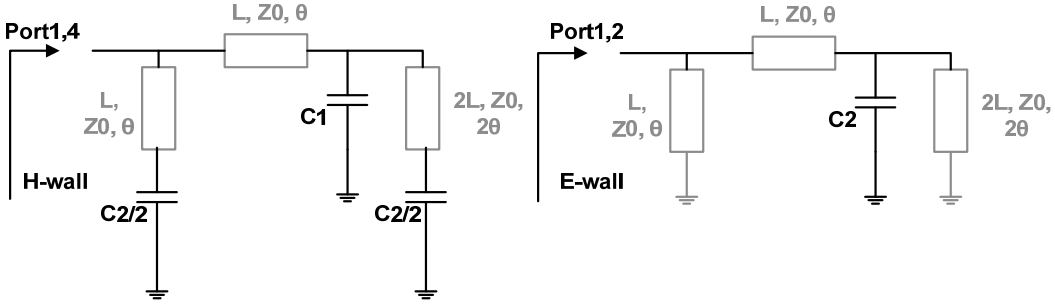
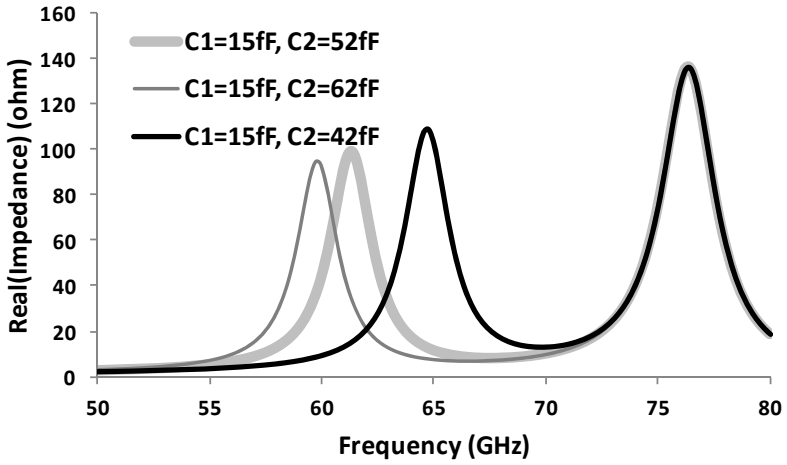


Figure 68, Ring shaped transmission line resonator analysis when ports 1 and 4 develop an H-boundary and ports 1 and 2 develop an E-boundary, corresponding to Fig. 4.

As can be seen in the above equations, the resonance conditions for the scenarios when E-wall or H-wall are invoked are complements of each other, and could be tuned independently of each other by selecting C_1 or C_2. The other designable parameters, common to both (3) and (4), are the characteristic impedance of the transmission line and the electrical length. The E-wall and H-wall control creates two co-existing resonance conditions, each one independently controlled, which could give rise to concurrent oscillation. Fig. 9 shows the impedance seen at the differential ports (ports 1 and 3, or equivalently ports 2 and 4); the peaks happen when the imaginary part is zero. The two resonances of Fig. 9 are independently tunable, as predicted by (3) and (4). This effect is further illustrated in Fig. 10(a) and Fig. 10(b). In Fig. 10(a), C_2 is changing while C_1 is fixed. It is noticeable the lower resonance peak changes while the higher one (corresponding to Arm2) is fixed.



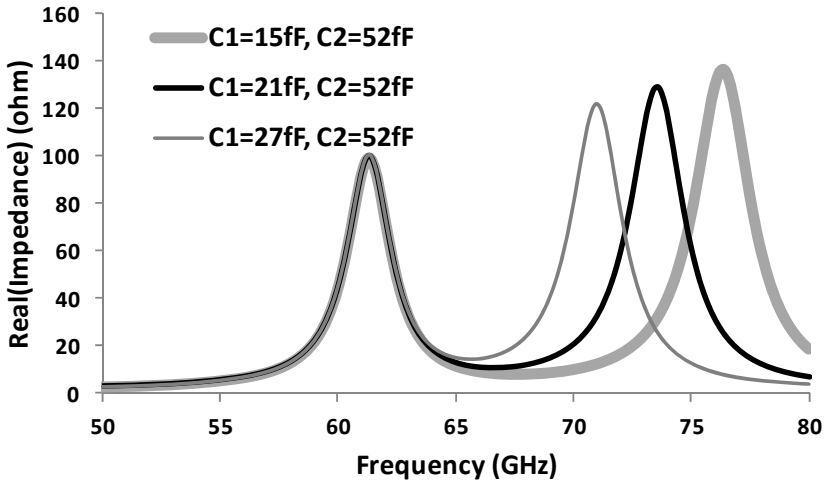


Figure 69, Coexisting resonance peaks (a) tuning the Arm1 capacitance (b) tuning Arm2 capacitance.

In Fig. 10(b), C_1 is changing while C_2 is fixed, and this time, the lower resonance peak corresponding to Arm1 is fixed, where as the higher resonance peak corresponding to Arm2 varies. The co-existence and independence of the E-wall and H-wall are clearly observable in Fig. 10. This orthogonality is in fact the feature we are interested in exploiting for the extended pulling range injection locking. This technique could be further expanded to more concurrent resonance/unstable frequency points, and could also be implemented in lumped element approach, as it is to be discussed in a future publication.

5.3. Divider implementation

A divider-by-two injection locked frequency divider is implemented in TSMC 65nm CMOS process, employing the aforementioned structure. The divider core is completed by creating the pair-wise out of phase excitations. Cross-coupled pairs are selected due to their inherent differential operation. A complementary cross coupled pair is connected at ports 1 and 3, and one is connected at ports 2 and 4. The incoming signal (to be divided) is injected across the cross-coupled pairs, as illustrated in Fig. 70.

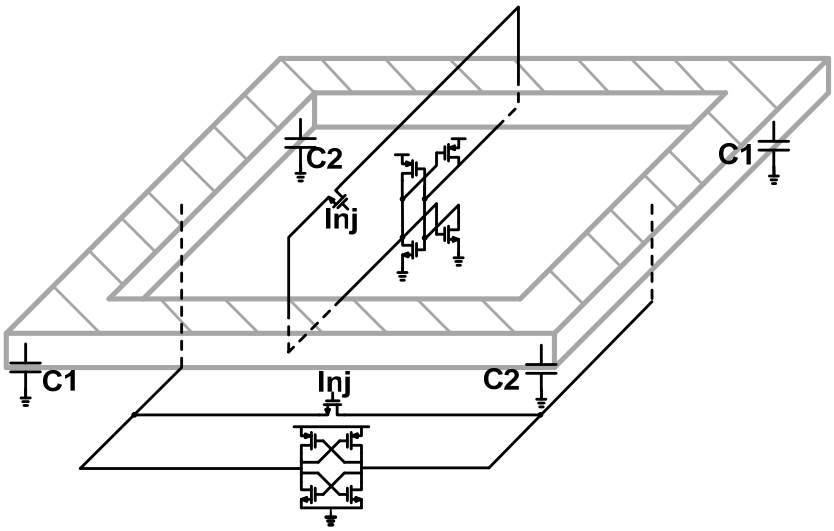


Figure 70, , injection locked divider-by-two circuit, illustrating the ring resonator, cross-coupled core, and injection points.

The divider structure is not only distributed in its resonator structure, but is also distributed in its excitation and injection points, and as a result is more immune to

parasitic and able to achieve a wider and higher locking frequency range. The die photo is presented in Fig. 71, and occupies 228 µm x 228 µm, excluding the pads. The loop is bent inward at the excitation points in order to create contacts and minimize the loss due to routing.

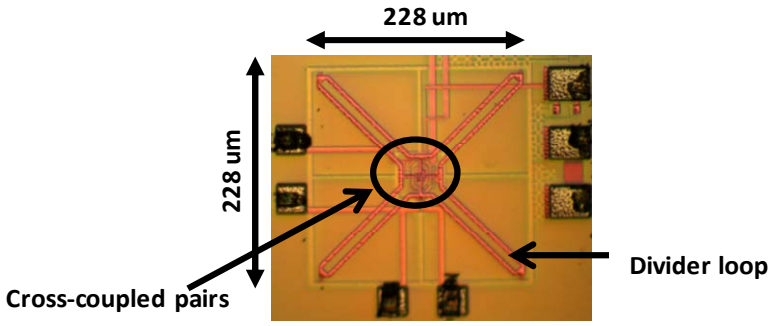


Figure 71, divider-by-two injection locked frequency divider die photo

The loop is bent inward at the excitation points in order to create contacts and minimize the loss due to routing.

5.4. Measurement results

The Output of the divider is probed with GS through an open-drained buffer connected to port 1. The remaining ports are connected to open drain buffers terminated on die. The oscillator's two free-running tones are measured at 29.5 GHz and 26.2 GHz. The injection signal is generated using an Agilent mm-wave source (50-75 GHz), controlled by a sweep generator. The mm-wave source could generate up to 3dBm power, which wasn't sufficient considering the 7 dB power losses in the cabling to the probe tips. Consequently, a power amplifier module, and a V-band attenuator were used

to tune the power. The highest locked tone spectrum of 32.60 GHz, and the phase noise corresponding to the lowest locked tone of -91.67 dBc/Hz at 1MHz offset from tone at 22.50 GHz are presented in Fig. 71. The phase noise is poor due to the use of the attenuator in front and that the power amplifier unit was saturated in the signal injection path from the source, thus deteriorating the source phase noise. Moreover, the power level to the tip of the probes was limited to 3 dBm.

The divider-by-two locking range, simulation and measurement, are summarized in Fig. 72. As indicted on the plot, the dips are at twice the free-running oscillation frequencies and the middle hump is in the overlap region of the two pulling-ranges, as discussed in equation (2) and an expected result. The total DC power, excluding the open drain buffer is 2.2 mW. The divider is compared with previous record divider-by-two injection locked dividers, operating in similar frequency band, as illustrated in Table 73.

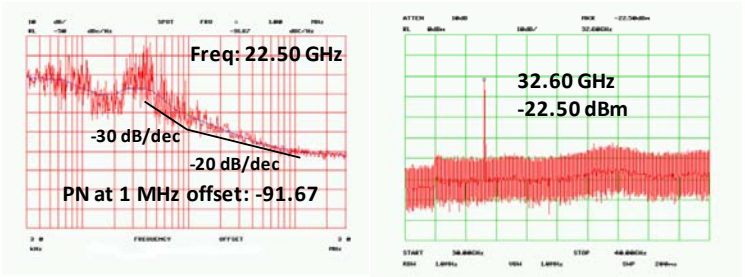


Figure 72, (a) lowest locked frequency phase noise, at 1 MHz offset from 22.50 GHz (b) highest locked frequency spectrum.

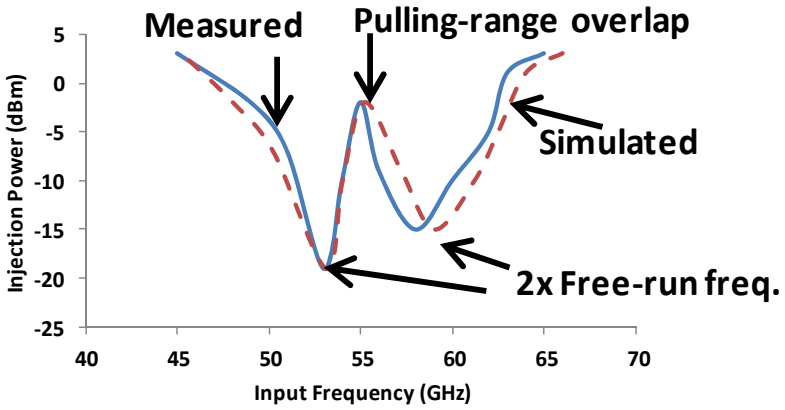


Figure 73, measured vs. simulated locking range of the divider

Ref	f_H (GHz)	Frequency range (GHz)	P_{DC} (mW)	FOM
[31]	40	10.6	6	70.6
[32]	40	15	3	200
[33]	30	6.2	1.86	100
[34]	70	1.6	2.75	40.72
This work	**65.2**	**20.2**	**2.2**	**598.6**

Figure 74, comparison of results with previous records

Chapter 6: Conclusion

The goal of achieving a multi-band, multi-standard and globally connected, as well as a self-healing or reconfigurable smart radio that can optimize its performance in different circumstances and situations in order to maintain a high performance yield and reliability, has imposed many requirements on the frequency synthesizer unit of the transceiver system, hence the oscillator. One significant requirement is the frequency tuning, which is being pursued by various schemes in the lower GHz regime (below the Ku band). However, there is a growing interest in transceiver design applications in the higher GHz bands using similar ideas. For example, there is the unlicensed 57-64 GHz band and the three licensed bands of 71-76 GHz, 81-86 GHz, and 92-95 GHz applicable for wide-band short range wireless communication and point-to-point fixed wireless communication, such as last-mile access, respectively. Wireless chip-to-chip communication is another field where multi-band and concurrent frequency generation is of interest.

As a possible solution, a new technique based on orthogonal E-wall and H-wall control of distributed resonators is discussed in this work. The technique produces co-existing resonance conditions, which are independently controllable. This property could be utilized in two ways: continuously tuned concurrent frequency generation, or continuously tuned ultra-wideband frequency generation. In order to operate as a wide-band design, one of the concurrent resonance conditions (corresponding to one of the two

modes) should be damped so that the excitation energy is only focused on one tone. The mode control is achieved using switches, either forcing the E-wall or the H-wall boundary conditions. The switch only adds loss to the undesired mode, and as a result, it is ineffective on the desired one; consequently, the technique does not possess the downfall of the others where the Q-limiting or the parasitic of the switch is a bottleneck.

A V-band VCO is designed using the technique in CMOS 65-nm technology, achieving greater than 18 GHz of continuous tuning range, measuring 177 μm x 177 μm, and establishing a new FoM record of -187 dBc/Hz.

Moreover, concurrent resonant and orthogonal modes are introduced as a novel technique to extend the limited locking range of injection locked circuits. Orthogonal E-boundary and H-boundary are introduced for achieving this feature, and a divider-by-two injection locked divider is demonstrated, measuring a new FoM. The principle is scalable in frequency, and could also be implemented in lumped element approach with inductors and capacitors. This could pave the way for wide bandwidth/high performance frequency synthesizers required for the emerging mm-wave applications, for wireless media and interconnect, at 60 GHz and beyond.

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