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AMPLIFIER-PREAMPLIFIER SYSTEM FOR RELATIVISTIC HEAVY ION DETECTORS

Authors
Landis, D.A.
Lu, S-L.
Schimmerling, W.

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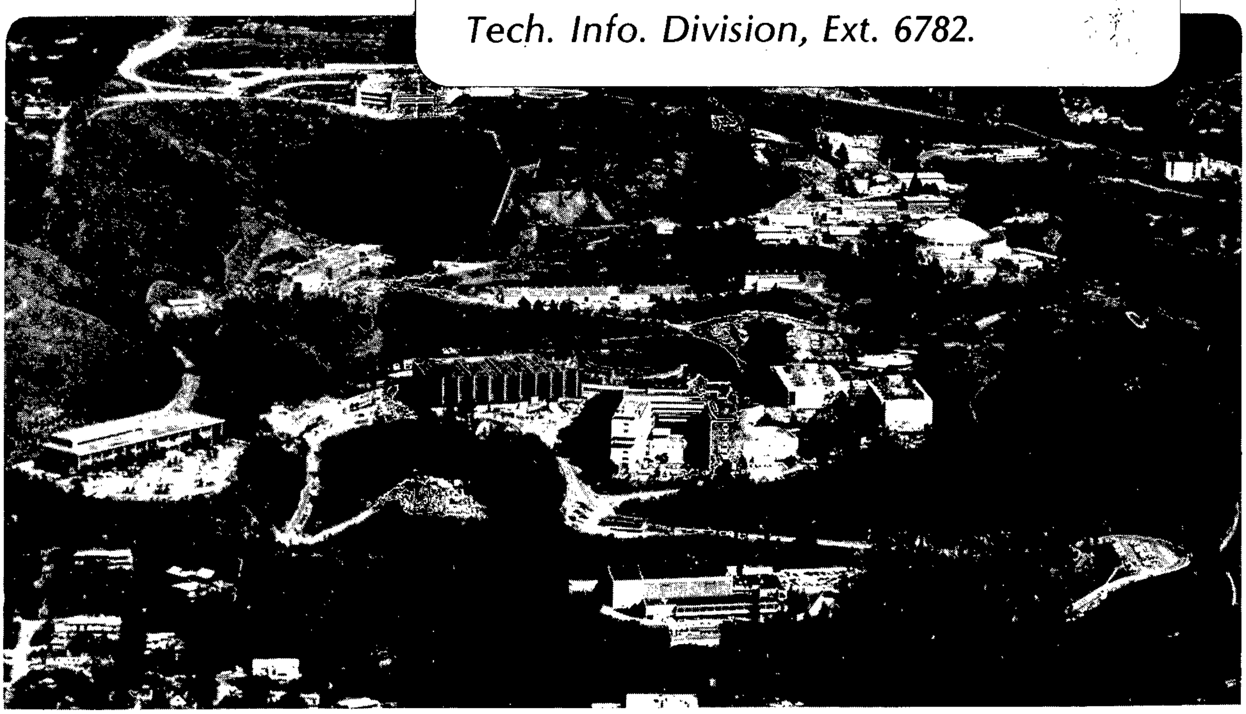

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DISCLAIMER

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AMPLIFIER-PREAMPLIFIER SYSTEM FOR RELATIVISTIC HEAVY ION DETECTORS

D. A. Landis, *S-L Lu, and W. Schimmerling

Lawrence Berkeley Laboratory
University of California
Berkeley, California 94720

INTRODUCTION

Multiple semiconductor arrays ("telescopes") are increasingly used for identification of the particles emitted in reactions of relativistic heavy ions.[1-3] These telescopes, consisting of large numbers of detectors, are used in a high-energy physics environment and require electronics that satisfy criteria different from those customary in conventional nuclear physics experiments. The most important of these criteria are: low cost, wide range of amplification gain, modest resolution, high counting-rate capability, compatibility with CAMAC and NIM standards, ease of interfacing with fast logic signals, and ease of calibration.

Low cost is mandated by the relatively large number of detectors required for satisfactory particle identification (several dozen detectors, in some cases). Such a detector array demands at least one channel of signal processing, consisting of preamplifier and amplifier, for each detector.

The wide range of amplification gain is determined by the ratio of energy loss of the heaviest particles stopping in a detector to the minimum ionization imparted by the lightest particle traversing it. For example, if the heaviest particle is a uranium nucleus stopping in a typical 3-mm thick silicon detector, this ratio is approximately 3×10^4 (uncorrected for electron capture by the stopping U). Since this exceeds the dynamic range of electronics satisfying the other constraints of this application, easy and reproducible gain switching must be provided. In particular, the ease and accessibility of the gain-switching controls is a very desirable feature when this must be done several times during a single experiment.

The resolution required of the semiconductor detectors used in this application is modest by comparison with gamma spectroscopy. The finite energy loss of nuclei with charge Z and mass A, at constant velocity, is a function

*Shanghai Institute of Nuclear Research, Shanghai, China.

of A/Z^2. The energy deposition of an intermediate nucleus such as Argon will differ from that of a nucleus with one charge unit more or less by 11%. Even for uranium, the relative difference will be 2%. This difference will be reduced by half for nuclei with the same A/Z ratio but one unit of Z different charge. For an energy deposition of several hundred MeV, a resolution of less than a few MeV will thus be adequate. This requirement also implies that constraints on detector noise become considerably relaxed.

The high counting rate capability is dictated by the fact that reaction cross sections of relativistic heavy nuclei are generally greater than those for low-energy nuclear physics, and have a greater number of rection channels open at the energies of interest here. As a consequence, the detectors must operate in a high fluence of particles, and the signals induced by these particles must be recognized, even if only to reject the majority of them.

Experiments with relativistic heavy nuclei typically involve many other detectors in addition to those used for particle identification. An event consists of more signals than can conveniently be handled with conventional multichannel analyzers, and computer-controlled data acquisition is the rule in all such experiments. This means that CAMAC and NIM standard electronics must be used to process the signals. A wide range of modular, high-density analog-to-digital converters (ADC's) are available that satisfy this standard. These units typically communicate via 50-Ohm signal cables and accept input pulses with a maximum amplitude of 2-4 V (either positive or negative, but not often both polarities).

Particle identification in this environment requires a variety of fast logic signals for efficient data analysis. Some of these are pattern-recognition signals (e.g., which detectors fired) used to mask selected events. Others are used for trigger logic, pile-up rejection, normalization, etc. Thus, a fast logic signal related to the time of detection of a particle in a given detector is an indispensable requirement.

Finally, the relatively harsh environment in which the detectors and their associated electronics must operate (e.g., radio-frequency fields, poorly controlled temperature and humidity, etc.), as well as the often rapidly changing experimental demands, requires frequent calibration. For this reason, ease and reproducibility of the electronic calibration (calibration of energy loss is a separate problem) are a highly desirable feature.

The system of preamplifier, amplifier and calibration pulser described in this report represents our current best effort to achieve an engineering compromise designed to meet the above criteria. The units are built with easily available commercial electronics in order to meet the goals of low cost and simplicity.

PREAMPLIFIER AND CALIBRATION PULSER

The preamplifiers along with their calibrating pulsers are built with two channels on a single plug-in card, and a group of cards (usually 2 or 4) are mounted in a single chassis box. The boxes are made from standard chassis parts to minimize the mechanical cost and complexity. A single set of voltage lines (± 24 V) are supplied by a NIM supply and are reduced to ± 15 V in the preamplifier box providing locally regulated and filtered power to the preamplifier cards. Figure 1 (a-b) are photographs of a preamplifier box showing the input and output connections. The block diagram of one channel of the preamplifier and calibrating pulser is shown in Fig. 2. The input to the preamplifer is AC coupled to the detector and contains the high voltage filter and detector load resistor. The charge sensitivity of the preamplifier is adjusted by switching in different feedback components (DIP switches on PC board) and covers the ranges of 0.1, 1.0, and 10 GeV full scale. The output of the preamplifier is DC coupled and back terminated to drive 50 ohm coaxial cable.

The calibrating pulser is coupled to the input of the preamplifier through a switched series (DIP switches) of accurately adjusted test capacitors to allow the full scale range of the pulser dial to be 0.1, 1.0, or 10 GeV (calibrated for Si detectors ϵ = 3.61 eV/h-e pair). The pulser has some features worth noting:

1) The pulser produces a square wave rather than a tail pulse so the pole-zero correction works as effectively as the detector signals. The square wave is about 20 μs wide with a 20 μs dead time so the maximum frequency is about 25 KHz. If the pulser is externally triggered at a higher rate, the one shot circuit automatically scales down to a maximum rate of 25 KHz.

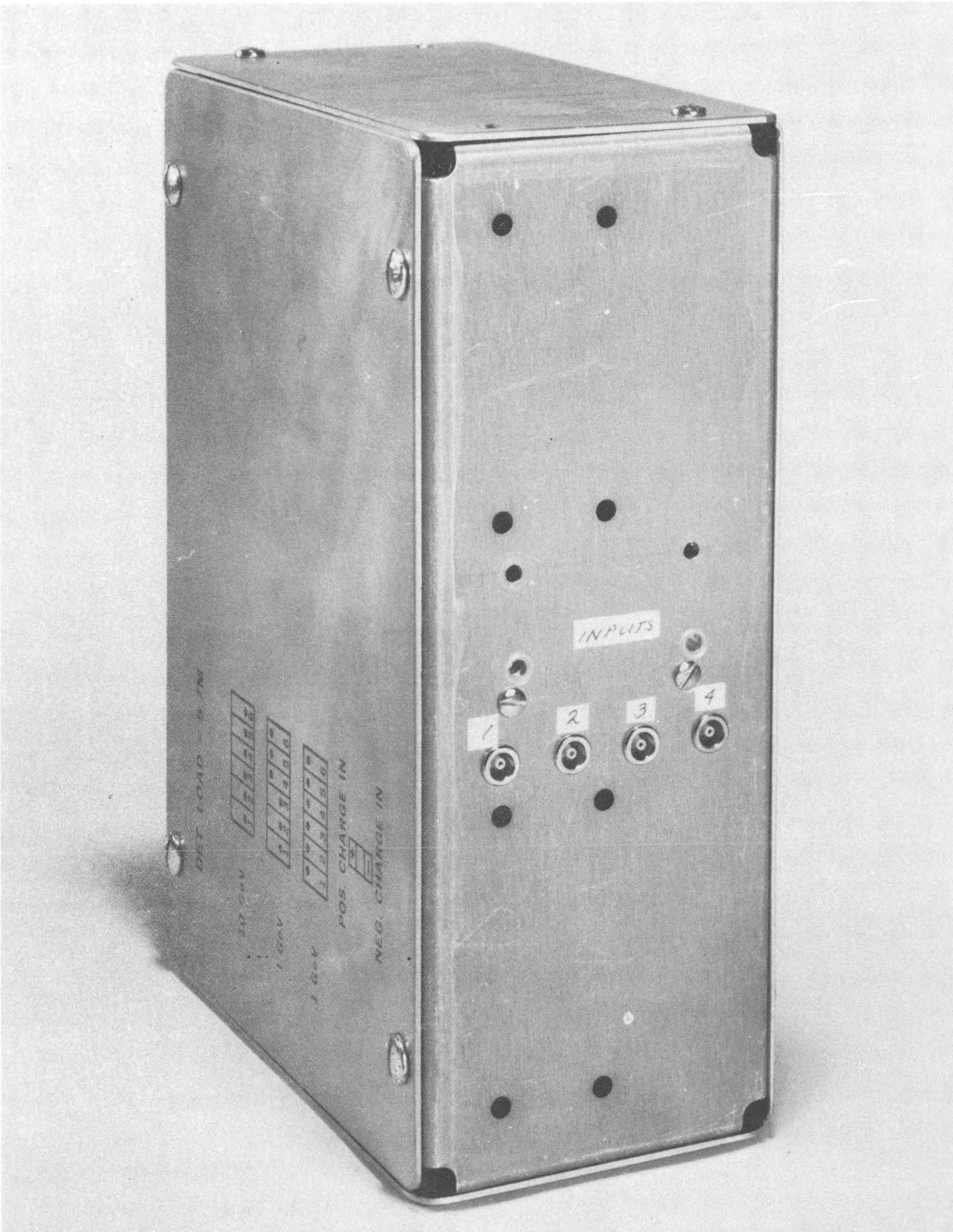

Figure 1 (a) XBB 821-902

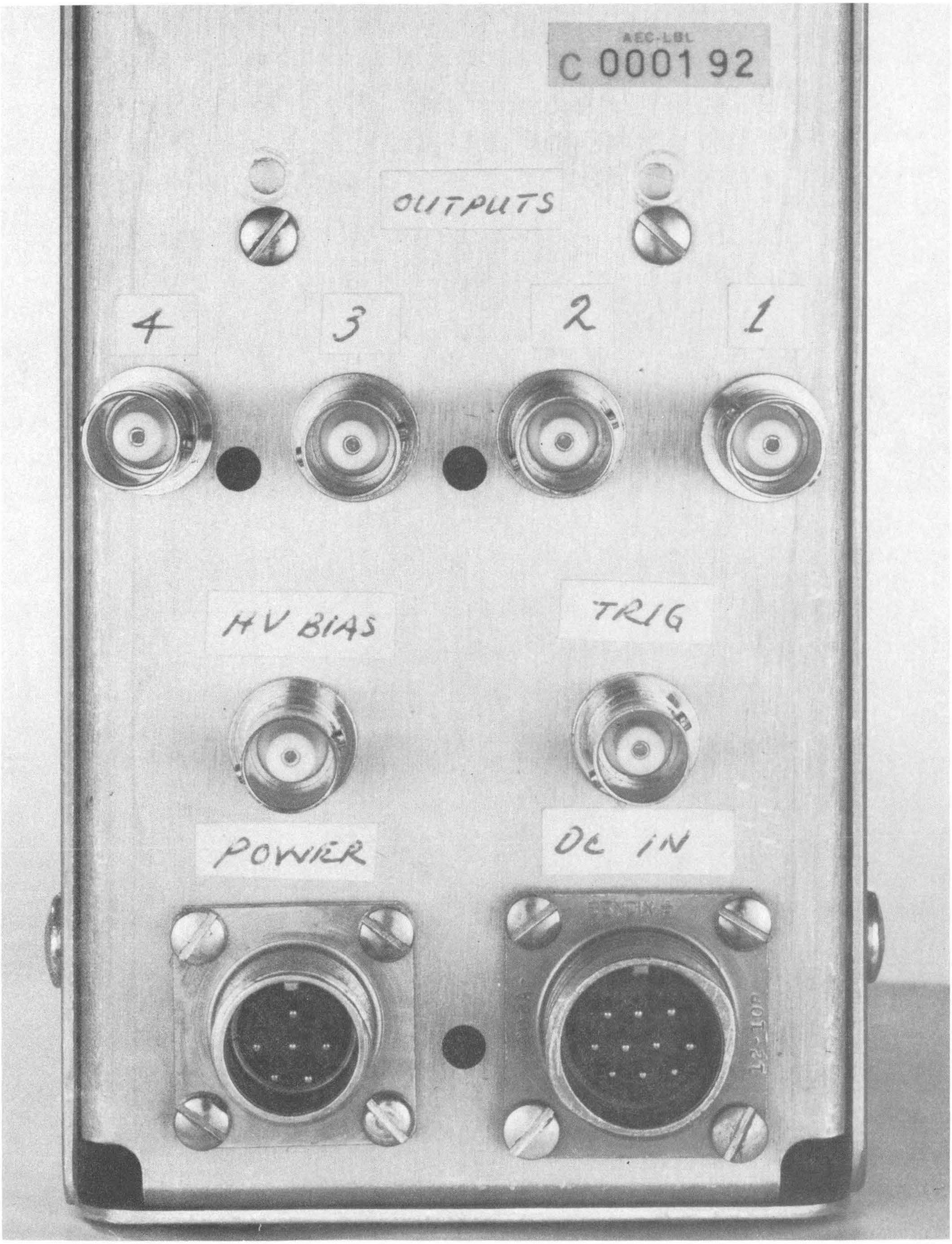

Figure 1 (b)

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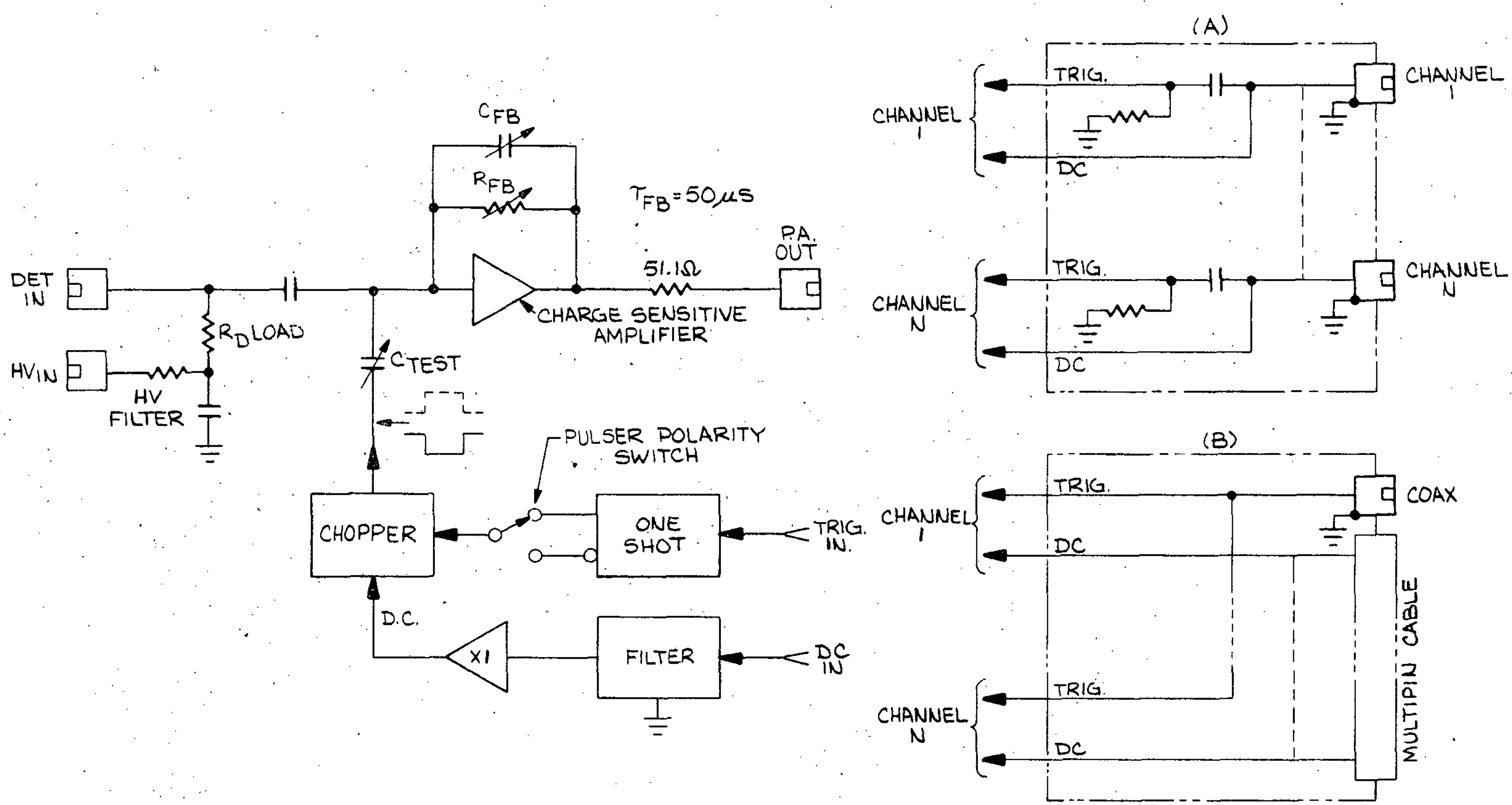

XBL 823-8413

Figure 2

2) The polarity of the pulser is easily changed to accommodate different detector configurations with a small slide switch on the preamplifier board.
3) The pulser has two inputs. One is a DC voltage (0 to +10 V) that determines the amplitude of the pulser (energy deposition) and the other is a trigger pulse that determines when the pulse will occur. The DC input goes through a low pass filter to a high input impedance buffer amplifier. The filter is used to remove any hum or AC pick-up from the pulser cables, and the high input impedance ensures that there is no cable loss making the pulser calibration independent of the length of the pulser cable.

The DC and trigger signals are supplied by a pulser drive module that is described later. These signals can be combined in different ways and two versions are shown in the block diagram. In the A version, the pulser signals for each preamplifier are supplied through a separate coaxial cable. The trigger pulse is separated from the DC signal in the preamplifier box by appropriate high and low pass filters. The second version (B) shown can be used when there are many preamplifier channels and not enough coaxial cables. This version has one coaxial cable that supplies a common signal to all the trigger pulse inputs and a multi-wire cable such as a power or computer cable that supplies the separate DC signals to each preamplifier channel. Both versions are used at LBL.

Figure 3 (a) shows a photograph of a four channel preamplifier box with the top cover removed. The range (DIP) switches, pulser polarity (slide) switches, and test input calibration capacitor can be seen mounted at the top of the plug in preamplifier boards. Figure 3 (b) shows the drawing on the cover showing how to set the range and polarity switches.

The measured characteristics of the preamplifier are shown in Table I. The noise is seen to be well within the desired limits. The rise time is reasonably fast, and the unit operates at a counting rate above 50 KHz. The output decay time constant is 50 μs and the output DC level is adjustable to zero volts. The maximum output signal amplitude into 50 ohms is + 3 V or – 2 V.

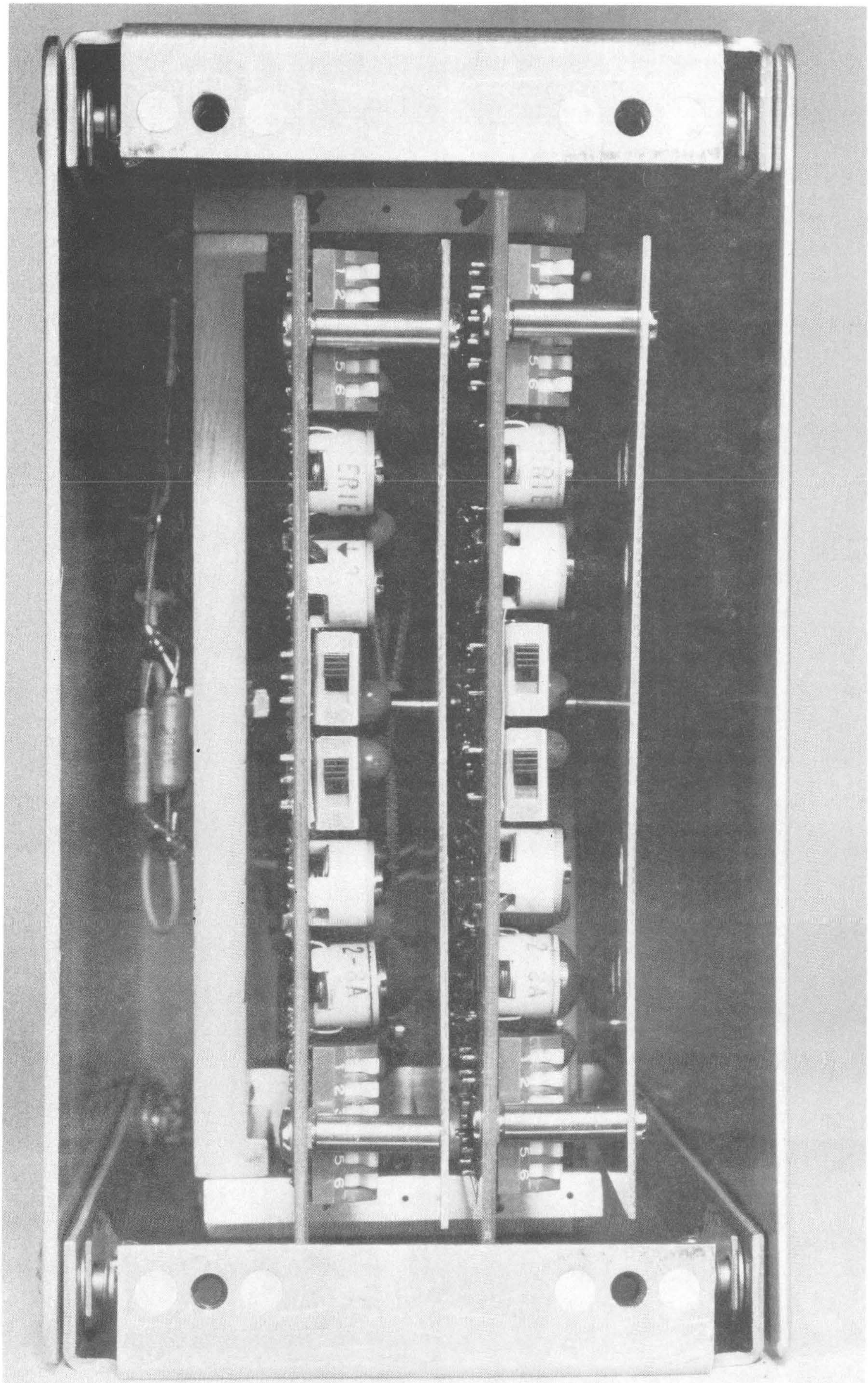

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Figure 3 (a)

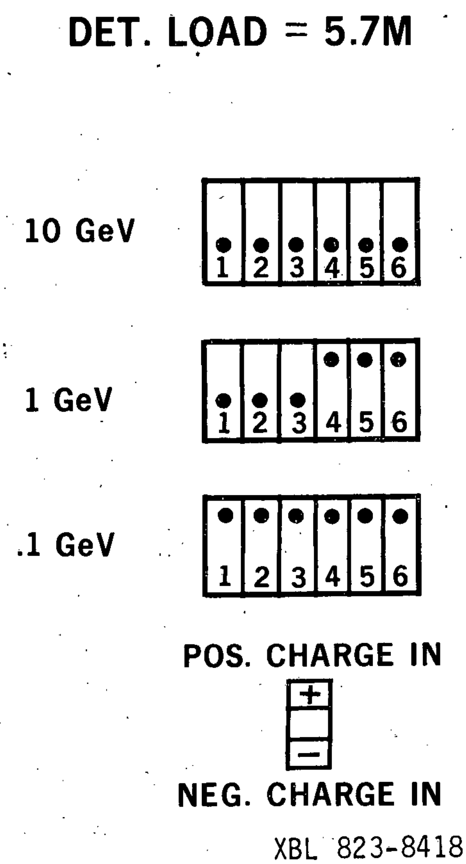
DET. LOAD = 5.7M
10 GeV
1 2 3 4 5 6
1 GeV
1 2 3 4 5 6
.1 GeV
1 2 3 4 5 6
POS. CHARGE IN
+
−
NEG. CHARGE IN
XBL 823-8418

Figure 3 (b)

TABLE I. Preamplifier Characteristics

Range (GeV)	Noise (keV)		Rise Time (ns)	
	C_i = 0 pF	Slope (eV/pF)	C_i = 0 pF	C_i = 100 pF
0 - 0.1	< 13	70	40	60
0 - 1.0	< 50	100	32	35
0 - 10	< 250	250	25	25

PULSE DRIVE MODULE

Figure 4 is a photograph of the pulser drive module and shaping amplifier module (to be described later). This pulser module has separate amplitude controls for eight channels. Four-channel pulser modules have also been built. Figure 5 is a block diagram of the pulser drive module showing the two versions (described in the preamplifier section) used to combine the signals from the drive module, before being sent to the calibrated pulser in the preamplifier. The pulse module can be triggered with an internal oscillator over a continuously variable rate from 10 Hz to 10 KHz, or can be externally triggered with a positive pulse greater than 2 V. Each pulser drive can be individually turned on or off and the energy level can be individually set, but all pulsers are triggered at the same time. The pulser dials are adjusted to supply exactly 10.00 V full scale and the energy calibration is accomplished by adjusting the individual test capacitor on the preamplifier boards. The test capacitors are adjusted by comparing pulser signals through the system with an accurately calibrated series of external test capacitors. The external test capacitors are calibrated for silicon detectors at room temperatures (ϵ = 3.61 eV/h-e pair). The calibration may be incorrect near the end of the range of heavy ions (due to charge defects) and this must be taken into consideration when the pulser calibration is used. The pulser zero amplitude or pedistal between different preamplifiers is within ± 0.2% of full scale. This could be improved if a more completed chopper were used in the calibrated pulser. The overall stability of the pulse system is around ± 0.1%.

DUAL SHAPING AMPLIFIER

The dual shaping amlifier module consists of two identical circuits, each consisting of a shaping amplifier and fast timing filter amplifier. They are mounted in a single-width NIM module (see Fig. 4). Figure 6 is a block diagram of one channel of the module. The shaping amplifier has pole-zero cancellation, around the input differentiator followed by four-pole integration that provides an output pulse of nearly Gaussian shape.

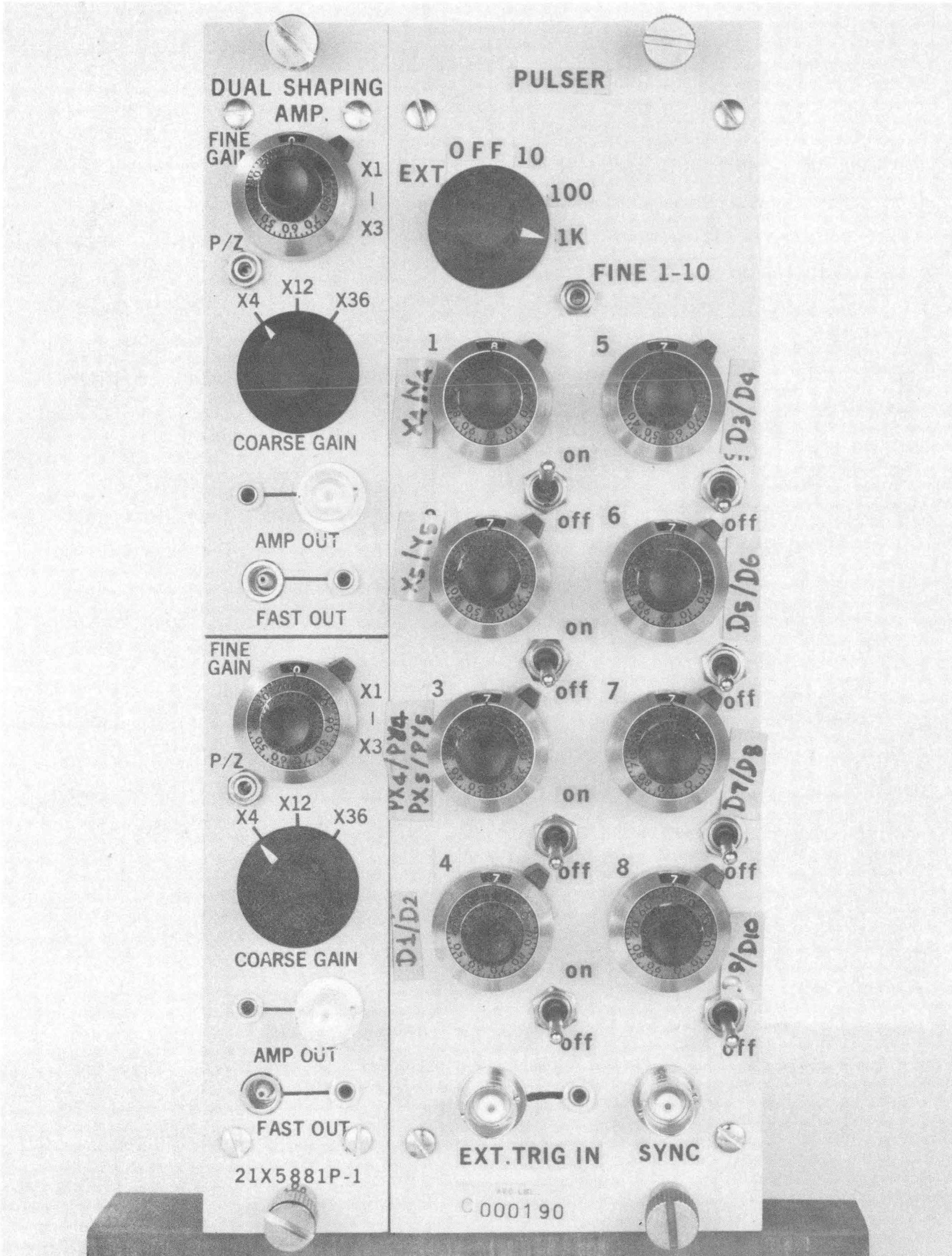

Figure 4

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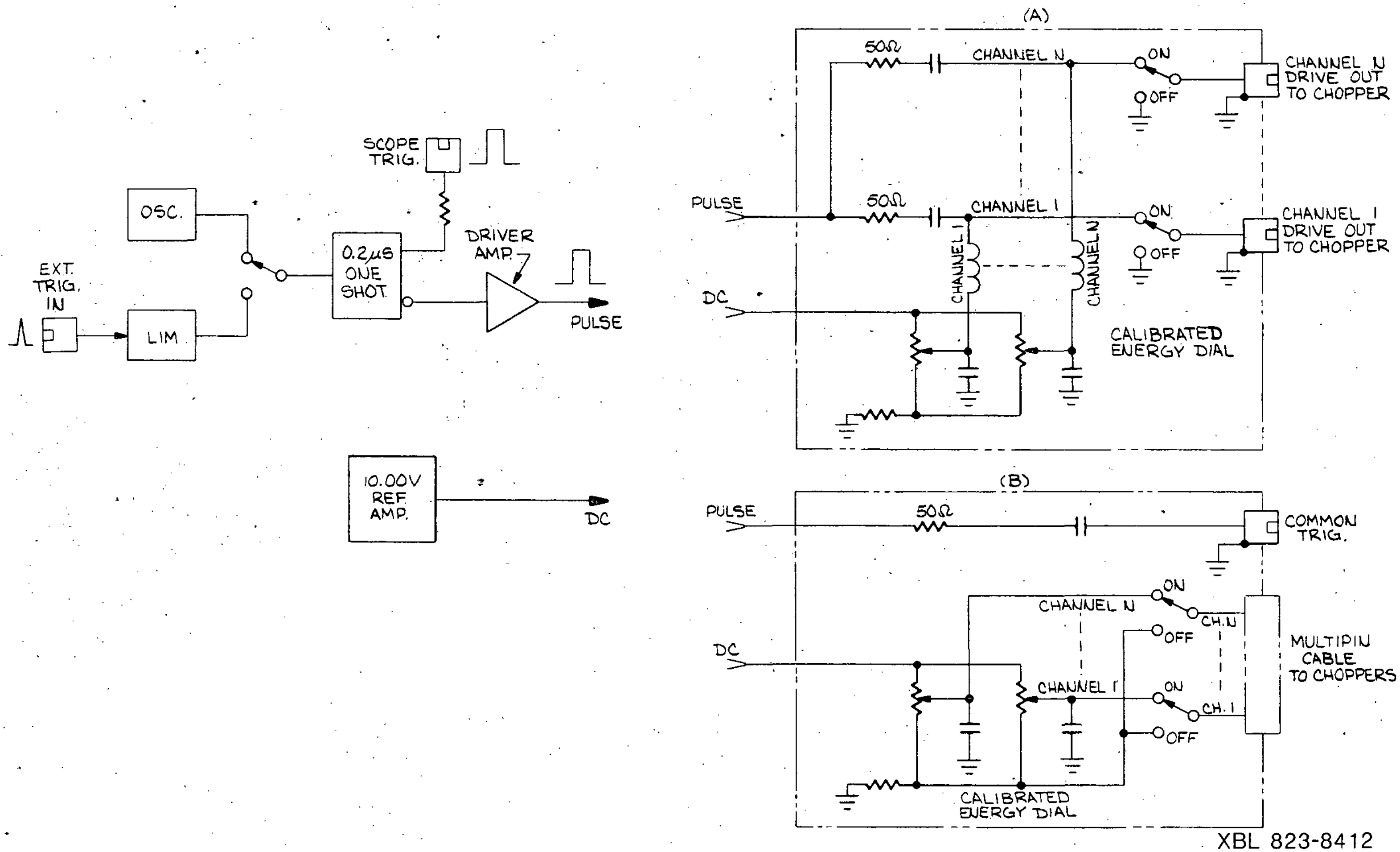
SCOPE TRIG.
OSC.
EXT. TRIG. IN
LIM
0.2μS ONE SHOT
DRIVER AMP.
PULSE
10.00V REF. AMP.
DC
(A)
50Ω
CHANNEL N
ON
OFF
CHANNEL N DRIVE OUT TO CHOPPER
PULSE
50Ω
CHANNEL 1
CHANNEL 1 DRIVE OUT TO CHOPPER
CHANNEL 1
CHANNEL N
DC
CALIBRATED ENERGY DIAL
(B)
PULSE
50Ω
COMMON TRIG.
CHANNEL N
ON
OFF
CH. N
DC
MULTIPIN CABLE TO CHOPPERS
CHANNEL 1
ON
CH. 1
OFF
CALIBRATED ENERGY DIAL
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Figure 5

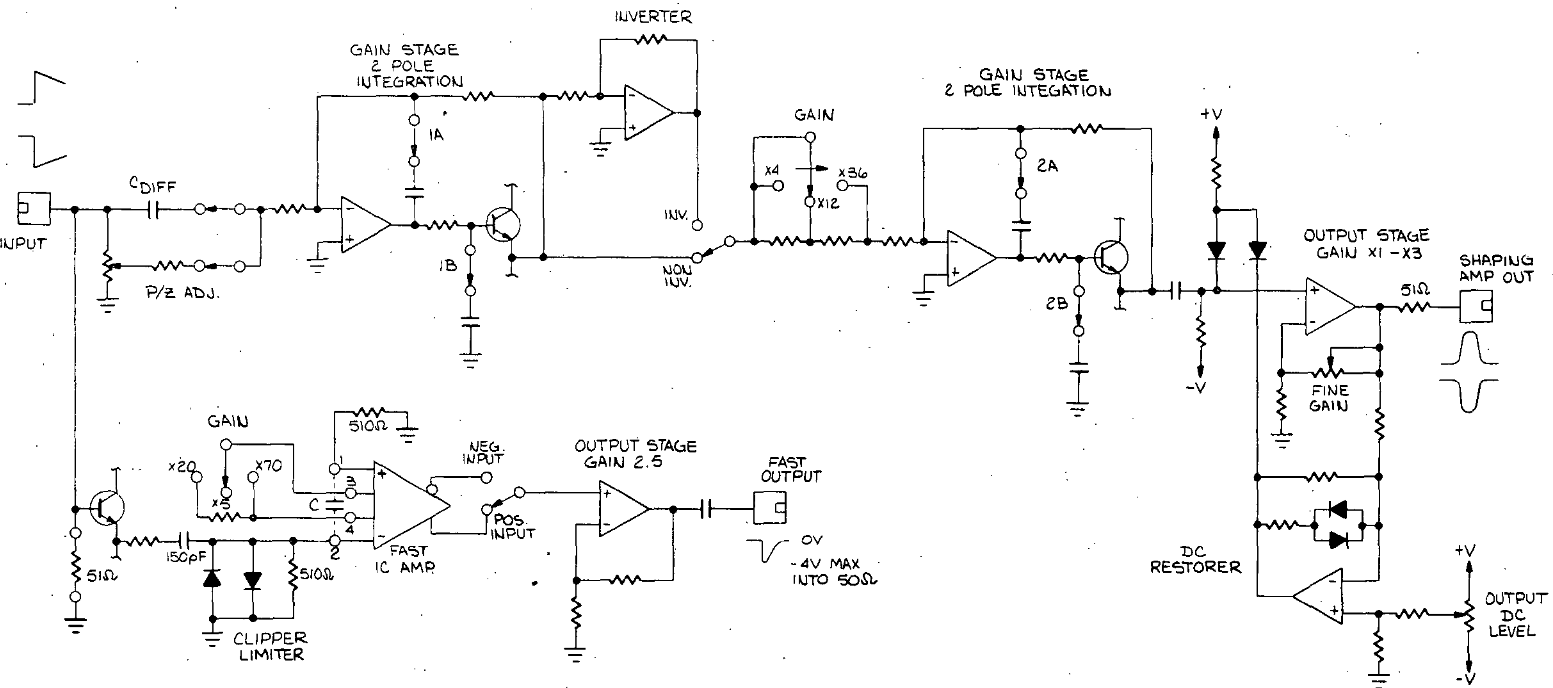

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Figure 6

The peaking time can be switched fom 1 to 9 μs and the gain can be continuously adjusted from x 4 to x 100. The input-to-output polarity can be inverted and the output can drive signals into 50 ohm cable allowing the amplifier to accommodate positive or negative inputs and provide positive or negative output. The output range in the positive direction is + 10 V into an open circuit (1 K ohm or higher) or + 5 V into 50 ohm, and in the negative direction - 8 V into an open circuit and -4 V into 50 ohm. This accommodates all the ADC's at LBL. The shaping amplifier has an active (bipolar) DC restorer that will handle high counting rates and has an output zero adjustment. The input impedance of the shaping amplifier is nominally 50 ohm, but can be changed to 125 ohm (input termination plugs into socket on amplifier board).

The fast timing filter amplifier is added for coincidence and pile-up rejection capabilities. The gain of the fast amplifier along with the rise time can be varied. Figure 7 is a photograph of the inside of the dual shaping amplifier showing the internal switches and controls. Figure 8 is a drawing of the side cover of the module showing how to set the internal switches. The gain of the fast amplifier can be changed in older versions by plugging in a jumper or resistor into points 3 and 4 (see Figs. 6 and 8) or in later versions by a three position switch on the rear panel of the module. The overall fast amplifier gains are x 12, x 50, or x 150. The rise time of the fast amplifier pulse can be made longer if needed (for signal to noise consideration) by inserting a small capacitance into points 1 and 2 of the fast amplifier. The fast amplifier will provide a maximum negative 4 V pulse into 50 ohm (a good match for the constant fraction discriminators in use at LBL). The specifications of the dual shaping amplifier are shown in Table II.

The switches for selection of the amplifier peaking times and input-output polarity are mounted on the printed circuit board. Pole-zero adjustments are made using a trimpot accessible through the front panel. Such adjustments are critical in high counting rate applications and are made in the usual manner, by minimizing the undershoot (or overshoot) of the output pulses. Pole-zero cancellation adjustments should be retrimmed whenever the preamplifier range or the amplifier peaking time is changed.

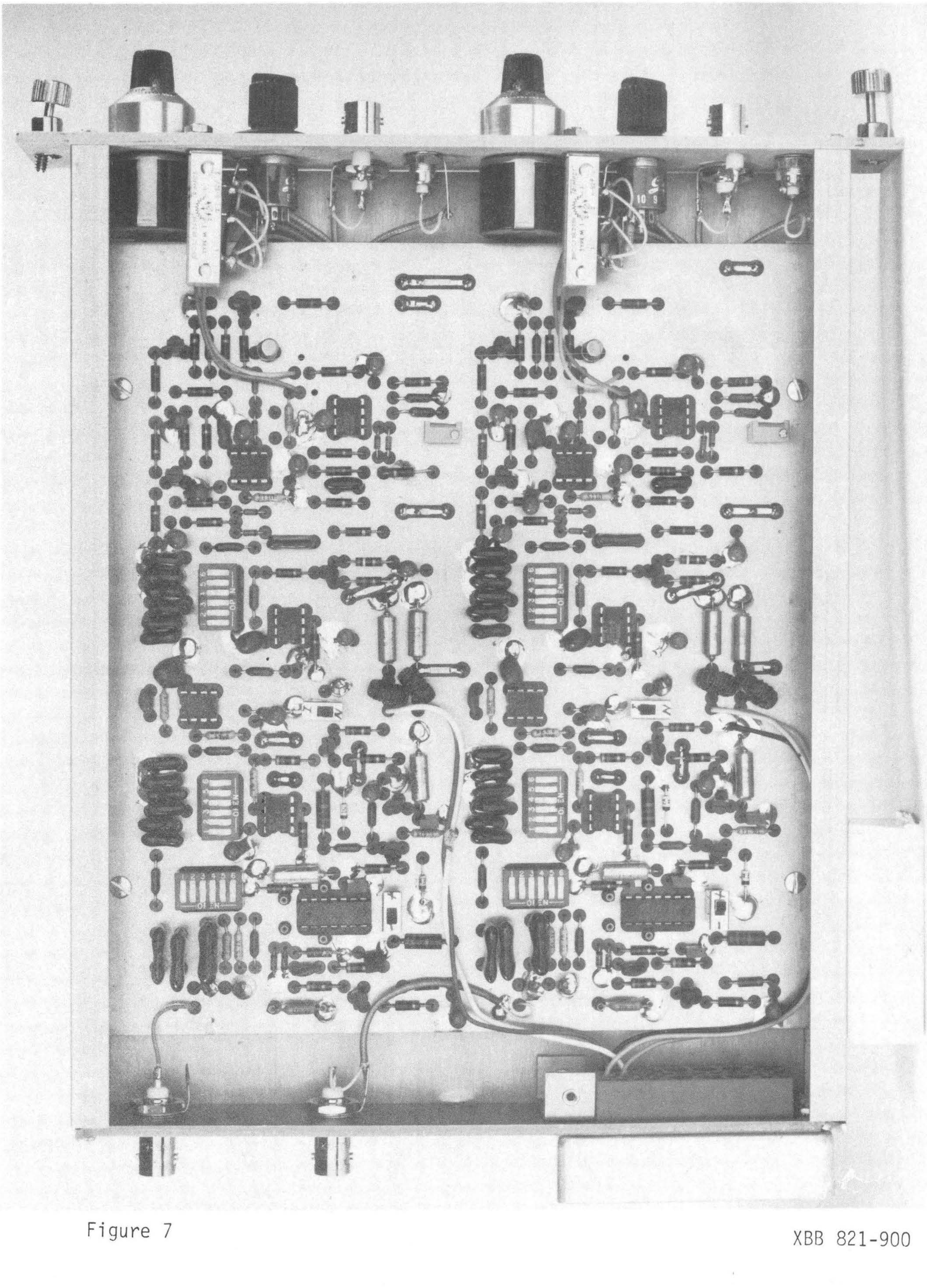

Figure 7

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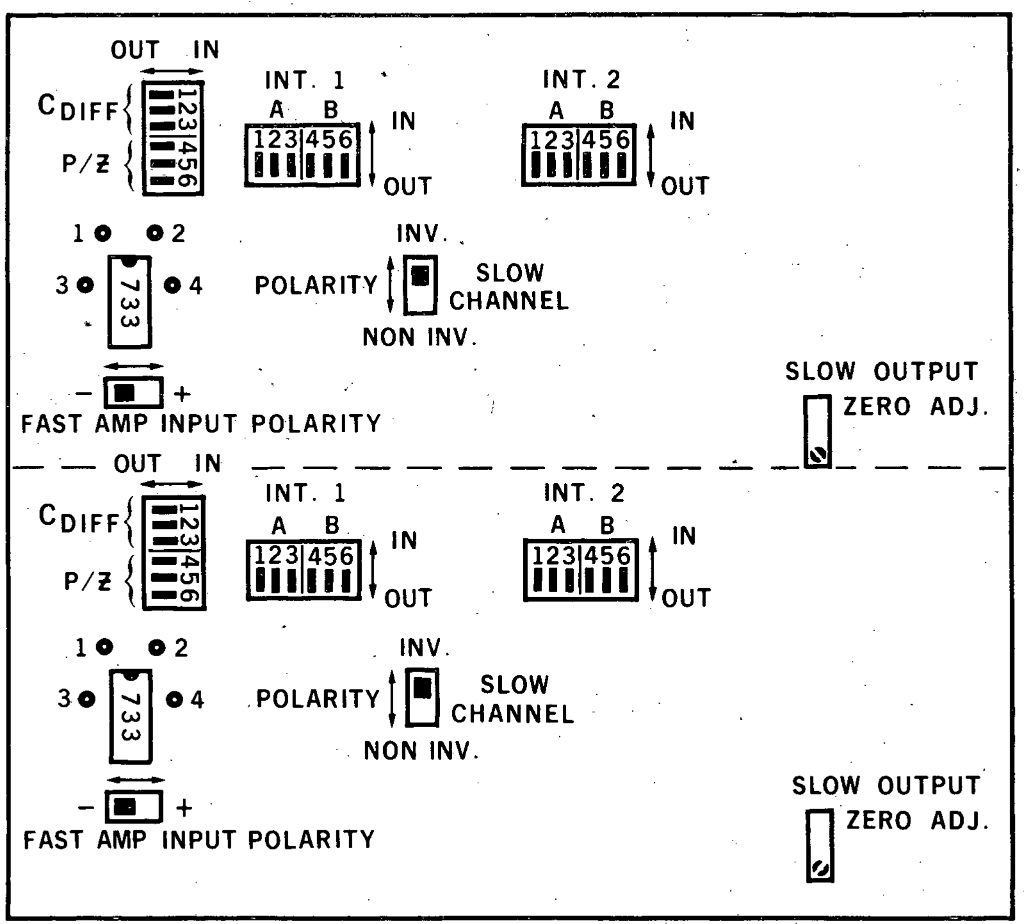
DUAL SHAPING AMP. 21X5881 P-1



PEAKING TIME SWITCHES
(C_{DIFF}, P/Z, INT. 1 & 2)

Tpμs	ALL SWITCHES
1	1,4
2	2,5
3	1,2,4,5
6	3,6
7	1,3,4,6
8	2,3,5,6
9	1,2,3,4,5,6

INPUT + OR −	Z IN = 51Ω
SLOW OUT + OR −	Z0 = 51Ω
FAST OUT − ONLY	Z0 ≈ 0Ω

+24V @ 30mA
+12V @ 150mA
−12V @ 150mA
−24V @ 36mA

XBL 823-8417

Figure 8.

TABLE II. Dual Shaping Amplifier Specifications

A. Shaping Amplifier

1. Gain Control: Coarse – x4, x12, x36, selected by a rotary switch
   Fine – x1 to x3, adjusted by 10-turn Helipot.
2. Peaking Time (μs): 1,2,3,6,7,8,9 selected by dip switches.
3. Pole-zero Cancellation: trimpot to adjust for decay times from 30 μs to .
4. Input Polarity: positive or negative (switch selected).
5. Input Impedance: 51 or 121 ohms.
6. Output Amplitude (Max): +10 V or –8 V (open circuit)
   +5 V or –4 V (50 ohms).
7. Output Impedance: 50 ohms.
8. Noise: < 15 μV (referred to input using 1 μs peaking time and gain = 100.
9. Baseline Drift: < 2 mV.
10. Maximum Counting Rate: > 50 kHz (1 μs peaking).

B. Fast Amplifier

1. Gain Control: x12 ("Lo"), x50 ("Mid"), x150 ("Hi"),
   selected by toggle switch on rear panel.
2. Rise Time: < 10 ns.
3. Input Polarity: positive or negative (switch selected).
4. Input Clipping Time Constant: 75 ns.
5. Output Amplitude (Max): –5 V (50 ohms).

C. Power Requirements

+24 V	at	30 mA	–24 V	at	36 mA
+12 V	at	150 mA	–12 V	at	150 mA

The output impedance of the amplifier is 50 ohms, and signal cables should be terminated especially if they are longer than 10 m. For short cables, termination may not be necessary. Signal input connectors are mounted on the rear panel, and gain control and pole zero adjustment of the shaping amplifiers and output connectors, along with test point for both the shaping amplifier and fast amplifier, are placed on the front panel.

CONCLUSIONS

The units have been used in several experiments and have performed well up to specifications. The estimated cost for a production run of sufficient units to provide 50 channels of preamplifier, pulser and amplifier (not counting the pulser driver unit) is about $600 per channel. The units are reliable, easy to adjust, and have proven to be flexible in a variety of experimental configurations.

ACKNOWLEDGMENTS

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D. Hendrie and J. Symons suggested several improvements on a preliminary version of the electronics. N. Madden also provided valuable advice during this development.

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3. Schimmerling, T.S. Subramanian, G. Gabor, A Sadoff, and W.J. McDonald, to be published.

FIGURE CAPTIONS

Fig. 1 a) Photograph of front of preamplifier box showing input cxonnectors.
b) Photograph of back of preamplifier box showing outputs, pulser, and power in connectors

Fig. 2 Block diagram of one channel of the preamplifier-calibrated pulser and two examples of how the pulser signals can be connected.

Fig. 3 a) Photograph of the top of the preamplifier box with the cover removed, showing energy range and input polarity switches and test input calibrating capacitors.
b) Drawing on top cover showing how to set energy range and polarity switches.

Fig. 4 Photograph of the front panels of the pulser driver and shaping amplifier modules.

Fig. 5 Block diagram of the pulser driver module with two examples of how the DC and pulse signals are combined.

Fig. 6 Block diagram of the shaper amplifier.

Fig. 7 Photograph of the inside of the dual shaping amplifier showing the internal switches and controls.

Fig. 8 Drawing of side cover for the dual shaping amplifier showing how to set the internal switches.

TECHNICAL INFORMATION DEPARTMENT
LAWRENCE BERKELEY LABORATORY
UNIVERSITY OF CALIFORNIA
BERKELEY, CALIFORNIA 94720