# **UC Berkeley**

**UC Berkeley Previously Published Works** 

# Title

Publisher's Note: "Differential voltage amplification from ferroelectric negative capacitance" [Appl. Phys. Lett. 111, 253501 (2017)]

## Permalink

https://escholarship.org/uc/item/3q53s9hd

**Journal** Applied Physics Letters, 112(8)

**ISSN** 0003-6951

## Authors

Khan, Asif I Hoffmann, Michael Chatterjee, Korok <u>et al.</u>

## **Publication Date**

2018-02-19

## DOI

10.1063/1.5024548

## **Copyright Information**

This work is made available under the terms of a Creative Commons Attribution-ShareAlike License, available at <u>https://creativecommons.org/licenses/by-sa/4.0/</u>

Peer reviewed

#### Differential voltage amplification from ferroelectric negative capacitance

Asif I. Khan, Michael Hoffmann, Korok Chatterjee, Zhongyuan Lu, Ruijuan Xu, Claudy Serrao, Samuel Smith, Lane W. Martin, Chenming Hu, Ramamoorthy Ramesh, and Sayeef Salahuddin

Citation: Appl. Phys. Lett. **111**, 253501 (2017); View online: https://doi.org/10.1063/1.5006958 View Table of Contents: http://aip.scitation.org/toc/apl/111/25 Published by the American Institute of Physics

#### Articles you may be interested in

Chemical vapour deposition of freestanding sub-60 nm graphene gyroids Applied Physics Letters **111**, 253103 (2017); 10.1063/1.4997774

Enhanced recoverable energy storage density and high efficiency of SrTiO<sub>3</sub>-based lead-free ceramics Applied Physics Letters **111**, 253903 (2017); 10.1063/1.5000980

Nanoparticle detection in an open-access silicon microcavity Applied Physics Letters **111**, 253107 (2017); 10.1063/1.5008492

Resistive switching and photovoltaic effects in ferroelectric BaTiO<sub>3</sub>-based capacitors with Ti and Pt top electrodes Applied Physics Letters **111**, 252901 (2017); 10.1063/1.4999982

Spin-phonon coupling in antiferromagnetic nickel oxide Applied Physics Letters **111**, 252402 (2017); 10.1063/1.5009598

Double Fe-impurity charge state in the topological insulator Bi<sub>2</sub>Se<sub>3</sub> Applied Physics Letters **111**, 251601 (2017); 10.1063/1.5002567





#### Differential voltage amplification from ferroelectric negative capacitance

Asif I. Khan,<sup>1,a),b)</sup> Michael Hoffmann,<sup>2,a)</sup> Korok Chatterjee,<sup>2</sup> Zhongyuan Lu,<sup>2</sup> Ruijuan Xu,<sup>3</sup> Claudy Serrao,<sup>4</sup> Samuel Smith,<sup>2</sup> Lane W. Martin,<sup>3,5</sup> Chenming Hu,<sup>2</sup> Ramamoorthy Ramesh,<sup>3,4,5</sup> and Sayeef Salahuddin<sup>2,5,b)</sup>

 <sup>1</sup>School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, Georgia 30326, USA
<sup>2</sup>Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, California 94720, USA

<sup>3</sup>Department of Material Science and Engineering, University of California, Berkeley, California 94720, USA <sup>4</sup>Department of Physics, University of California, Berkeley, California 94720, USA

<sup>3</sup>Material Science Division, Lawrence Berkeley National Laboratory, Berkeley, California 94720, USA

(Received 28 September 2017; accepted 4 November 2017; published online 18 December 2017; publisher error corrected 21 December 2017)

We demonstrate that a ferroelectric can cause a differential voltage amplification without needing an external energy source. As the ferroelectric switches from one polarization state to the other, a transfer of energy takes place from the ferroelectric to the dielectric, determined by the ratio of their capacitances, which, in turn, leads to the differential amplification. This amplification is very different in nature from conventional inductor-capacitor based circuits where an oscillatory amplification can be observed. The demonstration of differential voltage amplification from completely passive capacitor elements only has fundamental ramifications for next generation electronics. *Published by AIP Publishing*. https://doi.org/10.1063/1.5006958

Amplification forms the cornerstone of modern electronics. Amplification boosts an otherwise weak change of an electrical signal into a measurable quantity. Conventional circuit blocks are made of three different elements: resistors, capacitors, and inductors. Working alone, none of these elements can provide amplification. Due to this reason, these are often called the "passive" elements. Amplification in today's electronics is provided by transistors (often called the "active" elements) that draw additional energy from an external voltage source for amplifying signals. An exception to this rule came in 1953 with the invention of tunnel diodes by Esaki.<sup>1</sup> The tunnel diode can provide a negative differential resistance in the region where quantum mechanical tunneling is blocked by misalignment of the bands. It was shown<sup>2</sup> that in this region of negative differential resistance (NDR), a differential voltage amplification is possible. The tunnel diode amplifiers have found myriads of applications in electronics. Nonetheless, they remain to be the only example of an element that can provide a differential amplification by itself. In this work, we show that the recently discovered negative differential capacitance (NDC)<sup>3,4</sup> in a ferroelectric material can provide a similar differential amplification of a voltage signal. Unlike, the tunnel diodes, however, the amplification comes from the imaginary part of the impedance (NDC vs NDR). Also, NDC is obtained in a simple capacitor configuration, an insulator sandwiched between two metallic plates, rather than needing a p-n junction.

A ferroelectric material is characterized by a double well energy (U) landscape [Fig. 1(a)].<sup>5</sup> Typically, the material is stabilized in one of the minima of the landscape. But when it is switched, it goes through the maximum where the capacitance  $[\partial^2 U/\partial Q^2]^{-1}$ , with Q being the charge, is negative. The fact that the ferroelectric material can exhibit such a state of negative capacitance has already been demonstrated.<sup>3,4,6–18</sup> Therefore, if another dielectric capacitor is placed in series with the ferroelectric [as shown schematically in Fig. 1(b)], a voltage amplification is expected across the dielectric capacitor. By amplification, we specifically refer to differential amplification  $A_V$  which is equal to the rate of change of the voltage across the dielectric capacitor  $V_D$  with respect to the source voltage  $V_S$  (i.e.,  $A_V = dV_D/dV_S$ ). In the rest of this letter, we will use the terms "amplification" and "differential amplification" interchangeably. We note that the rate of change in the voltage across the dielectric capacitor  $V_D$  can be written in terms of the source voltage  $V_S$  and the capacitance of the ferroelectric ( $C_{FE}$ ) in the following way:

$$\frac{dV_D}{dt} = \frac{dV_S}{dt} - \frac{1}{C_{FE}}\frac{dQ}{dt} = \frac{dV_S}{dt} + \frac{1}{|C_{FE}|}\frac{dQ}{dt}.$$
 (1)

Again, note that the amplification is differential  $(dV_D/dt > dV_S/dt)$  and not absolute (i.e.,  $V_D$  may not be larger than  $V_S$ ).

To test this hypothesis, we have built model systems where thin film capacitors of  $Pb(Zr_{0.2}Ti_{0.8})O_3$  (PZT) are placed in series with parallel plate capacitors with variable



FIG. 1. Voltage amplification due to ferroelectric negative capacitance: (a) Energy landscape of a ferroelectric capacitor. The capacitance, C, is negative in the region enclosed by the dashed box. (b) The experimental setup.  $V_S$  and  $V_D$  are the source voltage and the voltage across the dielectric capacitor, respectively.

<sup>&</sup>lt;sup>a)</sup>A. I. Khan and M. Hoffmann contributed equally to this work.

<sup>&</sup>lt;sup>b)</sup>Authors to whom correspondence should be addressed: asif.khan@ece. gatech.edu and sayeef@berkeley.edu.

capacitance ( $C_D = 77-440 \text{ pF}$ ). Epitaxial PZT films (thickness = 70-100 nm) are grown using the pulsed laser deposition technique on metallic SrRuO<sub>3</sub> buffered SrTiO<sub>3</sub> (001) substrates, and Ti/Au top metal electrodes were sputtered and patterned. The series circuit is connected to a pulse function generator, and the voltage across the dielectric  $(V_D)$  and the source voltage  $(V_S)$  are monitored with an oscilloscope. In Fig. 2(a), we show the response of the series combination of a 100 nm thick PZT capacitor with area  $A_F = (35 \,\mu\text{m})^2$ and a dielectric capacitor  $C_D = 440 \,\mathrm{pF}$  to a bipolar triangular voltage pulse  $V_S: 0 \text{ V} \rightarrow +10 \text{ V} \rightarrow -10 \text{ V} \rightarrow 0 \text{ V}$  with period  $T = 50 \ \mu s$ . The inset shows the  $V_D$  and  $V_S$  waveforms for the entire cycle, and the main panel shows a blown-up version of the  $V_D$  waveform during 4.2  $\mu$ s  $\leq$  time (t)  $\leq$  6.7  $\mu$ s. The red dashed lines in the main panel in Fig. 2(a) indicate the slope of  $V_S$  in this time duration. We clearly observe that during the segment AB,  $V_S$  increases and  $V_D$  increases faster than  $V_S$  (i.e.,  $dV_D/dt > dV_S/dt$ ), indicating amplification of the source voltage at the node between the ferroelectric and the dielectric capacitor. The voltage across the ferroelectric capacitor  $V_F$  actually decreases during this time segment; Fig. S2 (supplementary material) shows the corresponding  $V_F$  waveform. In segment AB, the changes in  $V_D$  ( $\Delta V_D$ ) and  $V_S$  ( $\Delta V_S$ ) are ~1.7 V and ~1.4 V, respectively, leading to an average amplification  $\Delta V_D / \Delta V_S \cong 1.21$ . Similarly, in the latter part of the transient response when  $V_S$  decreases, an amplification in the  $V_D$  waveform is observed in segment *CD*, which is shown in Fig. 2(b). In *CD*,  $\Delta V_D \cong 1.66$  V and  $\Delta V_S \cong 1.4 \text{ V}$ , leading to an average amplification of ~1.19. Figure 2(c) shows the amplification  $A_V = dV_D/dV_S$  as a function of  $V_S$  [see the caption of Fig. 2 and Sec. I of the supplementary material for the  $A_V$  calculation method]. The  $A_V - V_S$  curve has a butterfly shape, in which  $A_V > 1$  in the segments, AB and CD. When the ferroelectric-dielectric combined system is in an amplification state, the ferroelectric capacitor is essentially in a negative capacitance state. To demonstrate that, the ferroelectric charge ( $\Delta Q$ )-voltage  $(V_F)$  characteristics extracted from the waveforms are plotted in the inset of Fig. 2(c) (see Sec. I of the supplementary material for the extraction method). The extracted chargevoltage curve of the ferroelectric capacitor is hysteretic and has distinctive negative slopes at the knees of the hysteresis loop (segments AB and CD), indicating negative capacitance in these regions. Starting at point O at t=0 ( $V_S=0$ ), with the increase of  $V_S$  ( $V_S$ : 0  $\rightarrow$  +10 V), the state of the ferroelectric capacitor  $[(V_F, \Delta Q) \text{ pair}]$  traces the path OABP in the hysteresis loop [Fig. 2(c) inset]; when it is in segment AB, the system responds with an amplification, which corresponds to the AB segment in the  $V_D$  waveform in Fig. 2(a) and in the  $A_V - V_S$  curve in the main panel in Fig. 2(c).



FIG. 2. Voltage amplification in a ferroelectric-dielectric series circuit. (a) and (b) Waveforms corresponding to the voltage across the positive capacitor  $V_D$  in response to a bipolar triangular voltage pulse  $V_S: 0 \vee \to +10 \vee \to -10 \vee \to 0 \vee$  with period  $T = 50 \mu s$  during 4.2  $\mu s < t < 6.7 \mu s$  (a) and 22.6  $\mu s < t < 25.3 \mu s$  (b).  $C_D = 440 \text{ pF}$ . The dashed red lines have the same slew rates as those of the  $V_S(t) - t$  curves in these time frames (i.e., they are || to the  $V_S$ -t curves). The inset in (a) shows the waveforms corresponding to the source voltage  $V_S$  and  $V_D$  during the entire cycle. Differential amplification is observed in the regions corresponding to the green shades, segments AB and CD in (a) and (b), respectively. (c) Amplification  $A_V (=dV_D/dV_S)$  as a function of  $V_S$ . The inset in (c) shows ferroelectric charge ( $\Delta Q$ )-voltage ( $V_F$ ) characteristics extracted from the waveforms.

In the latter part of the voltage pulse  $(V_S: +10 \text{ V} \rightarrow -10 \text{ V})$  $\rightarrow 0 \text{ V})$ , the ferroelectric goes through the rest of the hysteresis curve, and when it goes through the other negative capacitance segment *CD* [in Fig. 2(c) inset], the system again exhibits an amplification corresponding to segment *CD* in the  $V_D$  waveform [Fig. 2(b)] and in the  $A_V - V_S$  curve [Fig. 2(c) main panel]. We note that exactly similar shapes of ferroelectric hysteresis loops with negative capacitance were reported in Ref. 4 by using a completely different experimental setup with a series resistor.

We next study the nature of the amplification response of the ferroelectric-dielectric system by varying the dielectric capacitance  $C_D$ . Figures 3(a) and 3(b) show the  $A_V - V_S$ characteristics of the system for  $C_D = 240$  pF and 145 pF, respectively, and Figs. 3(c) and 3(d) plot the corresponding ferroelectric charge-voltage characteristics overlaid on the ferroelectric hysteresis loop calculated for  $C_D = 440$  pF. The corresponding transient responses are shown in supplementary Figures (Figs. S4 and S5). Comparing Figs. 2(c) and 3(a), we observe that the amplification in the ramp-down segment decreases when  $C_D$  is changed from 440 pF to 240 pF. For  $C_D = 145$  pF, amplification ceases in the rampdown segment as shown in Fig. 3(b). In Figs. 3(c) and 3(d), it is clear that unlike the case for  $C_D = 440 \text{ pF}$ , the ferroelectric hysteresis loops do not saturate at the positive  $V_F$  side for  $C_D = 240$  pF and 145 pF. As such, the ferroelectric capacitor traverses through minor loops for these two smaller  $C_D$ values. We note for the ferroelectric hysteresis loop for  $C_D = 440 \,\mathrm{pF}$  that the negative capacitance states occur only in a certain range of  $(V_F, \Delta Q)$ . For  $C_D = 240$  pF, the shape of the minor loop is such that it contains a smaller range of negative capacitance  $(V_F, \Delta Q)$  states in the reverse sweep path [compare the segments CD and  $C_2D_2$  on the ferroelectric loops for  $C_D = 440 \,\mathrm{pF}$  and 240 pF in Fig. 3(c)], thereby resulting in a reduced amplification in the ramp-down compared to that for  $C_D = 440 \text{ pF}$ . For  $C_D = 145 \text{ pF}$ , the minor loop is much smaller and does not contain any of the negative capacitance states, leading to no amplification during the ramp-down. Note that in the forward sweep, the negative capacitance states remains intact on the ferroelectric loops



FIG. 3. Effect of dielectric capacitance on amplification. (a) and (b) Amplification  $A_V$  as a function of  $V_S$  for  $C_D = 240 \text{ pF}$  (a) and 145 pF (b). (c) and (d) The extracted charge-voltage characteristics of the ferroelectric capacitor for  $C_D = 240 \text{ pF}$  (c) and 145 pF (d). These loops are overlaid on the ferroelectric charge-voltage characteristics extracted for  $C_D = 440 \text{ pF}$ , which is also shown in the inset of Fig. 2(c). The load lines for the dielectric capacitor  $\Delta Q = C_D \times (V_S - V_F)$  corresponding to  $V_S = +10 \text{ V}$  are plotted for  $C_D = 240 \text{ and } 145 \text{ pF}$  in (c) and (d), respectively. The load-line ( $V_S = +10 \text{ V}$ ) for  $C_D = 440 \text{ pF}$  is plotted in both of them.

for  $C_D = 240$  pF and 145 pF [see segments  $A_2B_2$  and  $A_3B_3$  in Figs. 3(c) and 3(d)]. This is why, during the ramp-up, the system shows an amplification in the ramp-up for both 240 pF and 145 pF.

To understand why the value of  $C_D$  determines the shape of the ferroelectric hysteresis loop, we employ the load-line technique-a widely used method for analyzing operating points in non-linear electronic circuits.<sup>19</sup> In Figs. 3(c) and 3(d), the load lines for the dielectric capacitor  $\Delta Q = C_D$  $\times (V_S - V_F)$  corresponding to  $V_S = +10$  V are plotted for  $C_D = 240$  pF and 145 pF, respectively, along with that for  $C_D = 440 \,\mathrm{pF}$  in both of them. The intersection of the loadline and the ferroelectric charge-voltage characteristics is the state of the ferroelectric when  $V_S = +10$  V—the state with the highest value of  $\Delta Q$ . With the decrease in  $C_D$ , the loadline becomes more slanted and intersects the hysteresis loop at smaller  $\Delta Q$  values. Note that at t=0, the ferroelectric capacitor is in a uniformly polarized state with the polarization pointing towards the SRO-PZT interface [indicated by ]  $\downarrow$  in Figs. 3(c) and 3(d)]. For  $C_D = 440 \text{ pF}$ , the ferroelectric polarization completely switches at  $V_S = +10$  V, which is indicated by  $\uparrow\uparrow$  in Figs. 3(c) and 3(d). On the other hand, the ferroelectric polarization does not switch completely [indicated by  $\downarrow\uparrow$  in Figs. 3(c) and 3(d)] at  $V_S = +10$  V for  $C_D = 240$  pF and 145 pF, for which the ferroelectric chargevoltage characteristics trace a minor loop in the return path. This analysis shows that a smaller value of  $C_D$  results in a larger voltage drop across the dielectric capacitor  $(\Delta Q/C_D)$ and a smaller current that can flow in the circuit  $(C_D dV_D/dt)$ , essentially limiting the amount of charge that can transfer onto the ferroelectric capacitor from the source, which, for the particular cases of  $C_D = 240$  pF and 145 pF, leads to incomplete switching of the polarization in response to the bipolar triangular pulse  $V_{\rm S}$ : 0 V  $\rightarrow$  +10 V  $\rightarrow$  -10 V  $\rightarrow$  0 V.

Similar functional behavior of the nature of the differential voltage amplification was also observed in the same system for much larger time periods ( $T = 500 \,\mu s$  and 5 ms), which is detailed in Sec. III of the supplementary material. As a self-consistent check, we performed independent timedependent measurements on ferroelectric-resistor series circuits using the same PZT capacitor and obtained ferroelectric charge-voltage hysteresis loops showing the negative slope of the P - V characteristics similar in shape to that in Fig. 3(b) (see Sec. VIII and Fig. S32 of the supplementary material for details). It should also be noted that the characteristic timescale of the negative capacitance phenomena can be in the sub-ps regime.<sup>20</sup> In this work, we intentionally chose to work at a much slower timescale (microseconds to milliseconds) such that the voltage amplification could be measured cleanly without complications arising due to parasitic components in our experimental set-ups. The robust behavior of amplification in the ferroelectric-dielectric series network over a span of time periods varying by 2 orders of magnitude as well as negative capacitance transience in the ferroelectric-resistor series circuit provides a self-consistent proof of the underlying physics of the differential amplification occurring through negative capacitance.

To gain a deeper understanding of our experimental results, we performed transient simulations that consider both homogeneous and inhomogeneous switching of the ferroelectric polarization. In the presence of the intermediate metal electrode between the ferroelectric and the dielectric capacitor, the dielectric capacitor does not result in a depolarizing field in the ferroelectric at  $V_s = 0$ —this is unlike the cases in ferroelectric-dielectric heterostructures without intermediate metallic layers.<sup>7,8,11,12,15</sup> As such, the ferroelectric can be polarized even at  $V_S = 0.^{22}$  For the homogeneous switching simulations (details in Sec. VI, supplementary material), the Landau-Khalatnikov equation<sup>21</sup> and Kirchhoff's current and voltage laws are self-consistently solved; the simulated  $V_D$  waveform, amplification  $A_V - V_S$  curve, and the ferroelectric charge-voltage characteristics extracted from the simulated waveforms shown in Figs. 4(b) and 4(c) are in qualitative agreement with the results shown in Fig. 2. The effect of inhomogeneous switching on the amplification in our ferroelectric-dielectric system was simulated using a timedependent Ginzburg-Landau (TDGL) framework which is described in Sec. VII of the supplementary material and in Ref. 23. The TDGL based simulations can capture the quantitative features of our results as shown in Figs. S28 and S30 of the supplementary material.

To summarize, we have directly measured differential voltage amplification in a combination of purely passive elements: a ferroelectric capacitor connected in series with an ordinary dielectric capacitor. As the ferroelectric switches from one state to the other, it imparts some of its stored energy onto the dielectric, leading to the amplification. We



FIG. 4. Simulation results. (a) Circuit diagram of the simulation.  $C_F$ ,  $\rho$ , and  $R_F$  represent the capacitance, the internal resistance, and the leakage resistance of the ferroelectric capacitor.  $C_D$  and R represent the capacitance and the leakage resistance of the dielectric capacitance. (b) Simulated waveforms corresponding to  $V_S$  and  $V_D$  of the circuit shown in (a) in response to a bipolar triangular pulse  $V_S$ :  $0 V \rightarrow +10 V \rightarrow -10 V \rightarrow 0 V$  with period  $T = 50 \,\mu s$ . Amplification is observed in the segments, AB and CD. (c) Simulated amplification  $A_V$  as a function of  $V_S$ .  $A_V \ge 1$  in the segments, AB and CD. The inset shows the ferroelectric charge-voltage characteristics extracted from the waveforms in (b).

note that in this process, there is no amplification of energy; the dielectric eventually gives back that energy to the ferroelectric during the time when the amplification falls below 1. Since such an energy transfer is dependent upon the combined potential energy landscape of the ferroelectricdielectric combination, the amplification depends upon how well the capacitances are matched (note that the potential energy is linear with capacitance). Note that while the amplification in Esaki diodes is based on the negative differential behavior of the *Real* or resistive part of the impedance, our work is based on the imaginary or reactive part of the impedance. Thus, together with the Esaki diodes, our work provides a complete picture: negative differential behavior in either part of the impedance will lead to a differential voltage amplification. The amplification demonstrated here can overcome the limits of voltage requirement in conventional transistors, often termed as the Boltzmann Tyranny,<sup>24–26</sup> and therefore has a direct consequence for energy efficient electronics. Such amplification could also find applications in very high frequency transistors (by boosting the transconductance) and also for improving the sensitivity of sensor circuits beyond conventional limits. As research on phase transitions in various material systems is gaining momentum, similar amplification should be expected in many other materials and for different types of state variables such as spin, magnetism, or correlated phases.<sup>27–29</sup>

See supplementary material for experimental procedures, electrical measurement data from different ferroelectric samples under different conditions, details on the loadline analysis, single domain and multi-domain simulation results, and structural characterization.

This work was supported in part by the Office of Naval Research, the Center for Low Energy Systems Technology (LEAST), one of the six SRC STARnet Centers, sponsored by MARCO and DARPA, and Entegris and Applied Materials under the I-Rice Center at the University of California, Berkeley. R.X. acknowledges support from the National Science Foundation under Grant No. DMR-1608938. L.W.M. acknowledges support from the Army Research Office under Grant No. W911NF-14-1-0104.

<sup>2</sup>L. Esaki, "Fundamentals of Esaki tunnel diode in circuit applications," in *Monograph on Radio Waves and Circuits* (Elsevier, 1963), p. 359.

- <sup>3</sup>S. Salahuddin and S. Datta, Nano Lett. 8, 405 (2008).
- <sup>4</sup>A. I. Khan, K. Chatterjee, B. Wang, S. Drapcho, L. You, C. Serrao, S. R. Bakaul, R. Ramesh, and S. Salahuddin, Nat. Mater. **14**, 182 (2015).
- <sup>5</sup>M. E. Lines and A. M. Glass, *Principles and Applications of Ferroelectrics and Related Materials* (Oxford University Press, 1977).
- <sup>6</sup>A. I. Khan and S. Salahuddin, "Extending CMOS with negative capacitance," in *CMOS and Beyond: Logic Switches for Terascale Integrated Circuits* (Cambridge University Press, 2015), p. 56.
- <sup>7</sup>A. I. Khan, D. Bhowmik, P. Yu, S. J. Kim, X. Pan, R. Ramesh, and S. Salahuddin, Appl. Phys. Lett. **99**, 113501 (2011).
- <sup>8</sup>W. Gao, A. I. Khan, X. Marti, C. Nelson, C. Serrao, J. Ravichandran, R. Ramesh, and S. Salahuddin, Nano Lett. 14, 5814 (2014).
- <sup>9</sup>A. Rusu, G. Salvatore, D. Jiménez, and A. M. Ionescu, in *Proceedings of International Electron Devices Meeting (IEDM)* (IEEE, 2010), pp. 16.3.1–16.3.4.
- <sup>10</sup>M. Hoffmann, M. Pesic, K. Chatterjee, A. I. Khan, S. Salahuddin, S. Slesazeck, U. Schroeder, and T. Mikolajick, Adv. Funct. Mater. 26, 8643 (2016).
- <sup>11</sup>D. J. R. Appleby, N. K. Ponon, K. S. K. Kwa, B. Zou, P. K. Petrov, T. Wang, N. M. Alford, and A. O'Neill, Nano Lett. **14**, 3864 (2014).
- <sup>12</sup>S. DasGupta, A. Rajashekhar, K. Majumdar, N. Agrawal, A. Razavieh, S. Trolier-McKinstry, and S. Datta, IEEE J. Exploratory Solid-State Computational Device Circuits 1, 43 (2015).
- <sup>13</sup>A. I. Khan, U. Radhakrishnan, K. Chatterjee, S. Salahuddin, and D. A. Antoniadis, IEEE Electron Device Lett. **37**, 111 (2016).
- <sup>14</sup>J. Jo, W. Y. Choi, J.-D. Park, J. W. Shim, H.-Y. Yu, and C. Shin, Nano Lett. **15**, 4553 (2015).
- <sup>15</sup>P. Zubko, J. C. Wojdel, M. Hadjimichael, S. Fernandez-Pena, A. Sene, I. Luk'yanchuk, J.-M. Triscone, and J. Niguez, Nature **534**, 524 (2016).
- <sup>16</sup>M. H. Lee, P.-G. Chen, C. Liu, K.-Y. Chu, C.-C. Cheng, M.-J. Xie, S.-N. Liu, J.-W. Lee, S.-J. Huang, M.-H. Liao *et al.*, in *Proceedings of International Electron Devices Meeting (IEDM)* (IEEE, 2015), pp. 222–225.
- <sup>17</sup>J. Zhou, G. Han, Q. Li, Y. Peng, X. Lu, C. Zhang, J. Zhang, Q.-Q. Sun, D. W. Zhang *et al.*, in Proceedings of International Electron Devices Meeting (IEDM) (IEEE, 2016).
- <sup>18</sup>A. Nourbakhsh, A. Zubair, S. Joglekar, M. Dresselhaus, and T. Palacios, Nanoscale 9, 6122 (2017).
- <sup>19</sup>A. S. Sedra and K. C. Smith, *Microelectronic Circuits* (Oxford University Press, New York, 1998), Vol. 1.
- <sup>20</sup>K. Chatterjee, A. J. Rosner, and S. Salahuddin, IEEE Electron Device Lett. 38, 1328 (2017).
- <sup>21</sup>L. Landau and I. Khalatnikov, Dokl. Akad. Nauk SSSR **96**, 469 (1954).
- <sup>22</sup>A. I. Khan, U. Radhakrishna, K. Chatterjee, S. Salahuddin, and D. A. Antoniadis, IEEE Trans. Electron Devices **63**, 4416 (2016).
- <sup>23</sup>M. Hoffmann, A. I. Khan, C. Serrao, Z. Lu, S. Salahuddin, M. Pešić, S. Slesazeck, U. Schroeder, and T. Mikolajick, arXiv:1711.07070 [cond-mat.mes-hall].
- <sup>24</sup>J. D. Meindl, Q. Chen, and J. A. Davis, Science **293**, 2044 (2001).
- <sup>25</sup>V. V. Zhirnov, R. K. Cavin, J. A. Hutchby, and G. I. Bourianoff, Proc. IEEE **91**, 1934 (2003).
- <sup>26</sup>T. N. Theis and P. M. Solomon, Science **327**, 1600 (2010).
- <sup>27</sup>J. T. Heron, J. L. Bosse, Q. He, Y. Gao, M. Trassin, L. Ye, J. D. Clarkson, C. Wang, J. Liu, S. Salahuddin *et al.*, Nature **516**, 370–373 (2014).
- <sup>28</sup>S. Salahuddin and S. Datta, Appl. Phys. Lett. **90**, 093503 (2007).
- <sup>29</sup>M. Imada, A. Fujimori, and Y. Tokura, Rev. Mod. Phys. 70, 1039 (1998).

<sup>&</sup>lt;sup>1</sup>L. Esaki, Phys. Rev. 109, 603 (1958).