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Physics-Based Electromigration and Time Dependent Dielectric Breakdown Modeling and Reliability Analysis for Nanometer VLSI Circuits

A Dissertation submitted in partial satisfaction of the requirements for the degree of

Doctor of Philosophy

in

Electrical Engineering

by

Xin Huang

August 2016

Dissertation Committee:

Professor Sheldon X.-D. Tan, Chairperson
Professor Daniel Wong
Professor Kambiz Vafai

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The Dissertation of Xin Huang is approved:

Committee Chairperson

University of California, Riverside

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ABSTRACT OF THE DISSERTATION

Physics-Based Electromigration and Time Dependent Dielectric Breakdown Modeling and Reliability Analysis for Nanometer VLSI Circuits

by

Xin Huang

Doctor of Philosophy, Graduate Program in Electrical Engineering
University of California, Riverside, August 2016
Professor Sheldon X.-D. Tan, Chairperson

Reliability has become a more serious design challenge for current nanometer very-large-scale integrated (VLSI) circuits especially as the technology has advanced into 7nm. It was expected that the future chips would show sign of reliability-induced age much faster than the previous generations. Among many reliability effects, electromigration (EM) and time- dependent-dielectric-breakdown (TDDB) induced back-end-of-line (BEOL) reliability have become major design constraints. EM is a physical phenomenon of the oriented migration of metal (Cu) atoms due to the momentum exchange between atoms and the conducting electrons. It can cause wire resistance change thus functional failure of the system. With aggressive technology scaling, EM signoff is becoming more difficult than before using traditional EM analysis approaches. TDDB is caused by formation of a conducting path through the low-k dielectric between metal. It results in a significant leakage increase between interconnects that degrades the circuit performance and causes the chip operation failure. There is still no universal agreement between the proposed TDDB models and the underlying physics of the dielectric breakdown, especially in backend low-k interconnects,

is still not completely defined.

This research focuses on developing new physics-based EM and TDDB models and chip-scale assessment techniques for nanometer VLSI circuits, which have overcome the problems existing in the traditional analysis approaches and can help reliability signoff at the design stage. Specifically, first, we have developed physics-based models for estimating the EM-induced stress evolution, void nucleation time and void motion. Interconnect-tree based analysis method is discussed to account for the inter-dependency between the branches in a tree. Second, we have proposed a novel IR-drop based full-chip EM assessment method to analyze the EM-induced degradation in the power grid networks. This method is further integrated with full-chip thermal and residual stress analysis techniques so that the impact of cross-layout temperature and residual stress distributions can be taken into account. Furthermore, we have proposed a new physics-based dynamic compact EM model, which for the first time can accurately model the EM process under time-varying current density and temperature stressing conditions. The proposed model can predict the transient EM recovery effect in a confined metal wire, which can be further exploited to significantly extend the chip lifetime. Last but not least, we have presented a novel approach for the physics-based chip-scale assessment of backend low-k TDDB, where the extracted TDDB lifetime model agrees with the observations obtained from the experimental results. The proposed flow provides a capability to evaluate chip-scale low-k TDDB reliability based on the calculated time-to-failure and can detect most leaking shapes in the layout.

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Chapter 1

Introduction

1.1 Motivation

1.1.1 Electromigration

Electromigration (EM) is the primary failure source for VLSI interconnects. As technology advances into the sub-10nm regime with FinFET devices, EM-induced failure is projected to get even worse due to the increasing current densities and elevated temperature thanks to the shrinking interconnect geometries and high temperature around the fins in the FinFET transistors. The EM assessment and verification is critical in the development of VLSI circuits to guarantee the metal wires and vias that connect the various devices in the chip do not fail and cause functional failure of the chip over years of continuous use.

To ensure the EM signoff, design rules based on the worst cases (highest possible temperature and power consumption) and simple empirical EM models can lead to very conservative overdesigns, which can significantly increase the chip areas, powers and

costs [7]. Lack of the accurate EM models, which can be used at the circuit and system levels for optimizing the EM-induced lifetime, limits our capability of properly handling the EM reliability.

Currently employed Blech limit [8] (for the out filtration of immortal segments) and Black's equation [9] (for calculating MTTFs for segments characterized by known current densities and temperatures) are subjects of the hard criticism [10] [11]. Across-die variation of residual stress makes the Blech's "critical product" to be layout-dependent variables rather than experimentally determined constants. The Black equation's current density exponent and the EM activation energy are the functions of current density and temperature, making the widely accepted methodology of calculating the MTTF at use condition groundless. This is because, conventionally, the value of activation energy and current density exponent at chip use condition are assumed to be the same as the value determined at the stressed (accelerated) condition, characterized by high current densities and elevated temperatures. Recently proposed physics-based models based on solving the basic mass balance equations using the finite element method, for instance [12], can only deal with very small structures such as one TSV. Complicated look-up table or models have to be built for different TSVs and wire segments for full-chip EM analysis with reduced accuracy, thus novel compact EM models are required.

Widely predicted decrease in EM lifetime due to transition to advanced technological nodes is responsible for the "performance-reliability" paradigm: high chip performance must be accompanied inevitable by a poor reliability and vice versa, a very reliable chip cannot demonstrate the top performance. This pessimistic conclusion is based on the currently

employed assessments, which consider an EM-induced failure rate of the individual interconnect segment as a measure of the chip-scale EM-induced reliability. In the extreme end, a mean time-to-failure of the weakest segment is accepted as a measure for the chip life-time. It results in very conservative EM-aware current density design rules for the leading-edge technology nodes. Instead, a very different way can be proposed from the positions of interconnect functionality, when the failure means its inability to function properly. Besides, the residual stresses such as thermal stress and mechanical stress can affect the EM failure. It is necessary to consider their impacts for accurate EM checking.

All semiconductor integrated circuit (IC) chips operate with time-dependent, for example AC or pulse, electric currents. Today's multi/many-core microprocessors are working on different performance (power) states. It results in large variations in current density and temperature, which can have huge impacts on the EM-induced stress evolution in interconnect wires, thus affect the failure development. The EM stress recovery effect, which is an important transient behavior, can be employed to extend the EM lifetime. Majority of existing physical EM models convert the time-varying currents to the effective DC currents. However using the effective DC current method ignores important transient effects. It is possible that the predicted wire is EM immortal but in reality it can be failed by EM. A number of dynamic EM models, which consider the time-dependent current waveforms, have been proposed [13–15]. However, the EM model in [15] is still based on traditional semi-empirical Black's equation, where the current density exponent is not a constant but a function of residual stress and current density. Especially, the recovery effect is not properly considered and the weighted average current is still used. Recently, a new dynamic EM

model was proposed [16]. However, this model is based on Korhonen's continuity equation with constant current density. It fails to predict stress recovery effect and inappropriately predicts a increasing/constant stress when current is reduced significantly.

1.1.2 Time-Dependent Dielectric Breakdown

With aggressive technology scaling accompanied by employment of new advanced materials, Time-Dependent Dielectric Breakdown (TDDB) is becoming, a second, after electromigration killer of on-chip interconnects. In general, the TDDB is a failure mechanism in back-end-of-line interconnects (BEOL), when the inter-metal dielectric (IMD) breaks down as a result of long-time application of relatively low electric field. The breakdown is caused by formation of a conducting path through the IMD oxide between metal lines due to electron tunneling current. It results in a significant leakage increase that degrades the circuit performance and causes the chip operation failure. Early works on TDDB have been mainly focused on the gate oxide TDDB, caused by the excessive electric fields in thin gate oxides. In contrast, TDDB in the BEOL stacks has not been a concern until recent years, due to wide dielectric spacing between metal lines and high electric strength of the inter-metal silicon dioxide. This situation has changed with the layout feature dimensions shrink and design complexity growth. The drastically reduced wiring pitches lead to escalating electric fields among interconnects. In order to decrease the RC delay, dynamic power consumption, and cross-talk noise, low-k dielectric materials, and more recently, ultra low-k porous dielectrics with the dielectric constant $k < 3$, had been integrated with copper metallization, for instance, fluorinated silicon oxide (SiOF), carbon doped silicon oxide (SiOCH), spin-on methl-silisesquioxanes (MSQ) and organic polymers. However, the

low-k materials are characterized by poor mechanical, thermal, and electrical properties in comparison with silicon dioxide [17]. Some of the process steps such as chemical mechanical planarization (CMP) and plasma etch can potentially damage the dielectric sub-surfaces regions, generating charge carrier traps and assisting the conduction [18]. As a result, the IC chips integrated with the copper/low-k interconnects tend to be vulnerable to TDDB failure. A number of dielectric reliability models have been proposed to explain and predict the TDDB phenomenon in low-k dielectrics under electrical stressing since 2003. However, the state of understanding of this field is far more limited than that for TDDB in thin gate oxides (in 1990s).

1.2 Dissertation contributions

This dissertation presents new advances in the physics-based modeling and full-chip assessment techniques for EM and TDDB reliability of VLSI systems. The major contributions of this dissertation are summarized as follows:

- For the physical modeling of EM, analytical models based on Korhonen's continuity equation have been proposed for stress evolution in both void nucleation phase and void growth phase. Approximation of void nucleation time is derived and the void volume evolution is modeled to account for the wire resistance degradation. The physics-based models can naturally consider the impact of other residual stress, thus can more accurately predict the EM-induced failure. The proposed models have solved the problems in the semi-empirical Black's equation and Blech limit, resulting in less pessimistic results that can help EM signoff at the design stage for VLSI circuits. Due

to the independence between connected branches in a multi-branch tree, an interconnect tree-based analysis technique is developed to avoids over optimistic prediction of the TTF made with the Blech-Black analysis of individual branches of interconnect tree.

- For the chip-scale EM assessment, a novel methodology has been proposed based on the developed physics-based formalism for void nucleation and growth. The new method takes a IR-drop based failure criteria, replacing a currently employed conservative weakest branch criterion, which does not account an essential redundancy for current propagation existing in the P/G networks. This method is further incorporated with thermal and residual stress analysis techniques so that the impacts of cross-layout temperature and residual stress variations on EM effect can be taken into account for more accurate failure prediction.

- The recovery effect becomes more significant and relevant due to available low power and energy optimization and management techniques at multiple system levels. we have proposed a new model for EM-induced degradation, which for the first time accounts for the transient stress recovery effect. The new dynamic model is based on the direct analytical solution of the Korhonen's equation with arbitrary unipolar or bipolar current loads at varying temperatures. The demonstrated application shows the potential of leveraging the recovery effect to extend the lifetime of the on-chip interconnect if the driving powers will be properly controlled and managed at the run time.

- The underlying physics of low-k TDDB still not clearly understood. A new physics-based TDDB modeling and assessment method has been proposed and implemented for the copper/low-k interconnects in VLSI chips. The new TDDB model accounts for the kinetics of electric current path generation and evolution in the IMD gap, which is governed by both electric field and metal ion diffusion. It replaces the widely accepted across-layout electrostatic field based TDDB assessment. Based on the proposed physical mechanism, a power-law lifetime model is extracted for the first time for the low-k TDDB, which agrees with the conclusion obtained from experimental results. The developed full-chip assessment flow has the ability to predict the TDDB induced chip lifetime and detect the locations in the layout that are most vulnerable to TDDB failure, which can be further employed in the reliability-aware circuit design.

1.3 Organization

The rest of this dissertation is organized as follows. Chapter 2 provides the background knowledge about fundamentals of EM and introduces the numerical analysis of stress and void evolution. It then focuses on physics-based analytical modeling of void nucleation and growth. Chapter 3 presents a novel approach for physics-based EM assessment in power grid networks and analyzes the impacts of the spacial variations of temperature and thermal stress on the EM failure rate. The new dynamic EM model considering time-varying temperature and current density is developed in Chapter 4, based on which the EM recovery effect is discussed to extend the system lifetime. Chapter 5 investigates another reliability threat, TDDB in Copper/low-k interconnects, where the physics-based TDDB

modeling method and full-chip analysis flow are presented. Finally, Chapter 6 concludes the dissertation.

Chapter 2

Physics-Based Electromigration Modeling

This chapter gives an overview of the fundamentals of EM and presents the development of physics-based formalism for void nucleation and growth, which are derived analytical solutions to the corresponding mass balance equations. Interconnect tree-based stress anaysis method is proposed to take into account the stress redistribution inside the branches composing a tree. The numerical analysis of stress and void evolution in confined metal lines is also discussed in this chapter.

2.1 Why physics-based EM models?

Standard industrial practice employed for estimating the EM-induced degradation of VLSI circuits is based on the approximate statistical Black's equation [9]:

$$MTTF = \frac{A}{j^{-n}} exp\{\frac{E_a}{k_B T}\} \tag{2.1}$$

, which calculates the mean time-to-failure (MTTF) or t_{50} of individual lines characterized by known current densities and temperatures. Here, j is the current density; k_B is the Boltzmann's constant; T is the absolute temperature; n is the current density exponent (which Black found to be approximately equal to 2); E_a is the activation energy of the failure process, and A is a constant which depends on a number of factors, including grain size, line structure and geometry, test conditions, current density, thermal history, etc. Parameters n and E_a are extracted from measurements. Majority of measurements show that n varies over the commonly observed range of $1 - 2$. Two limiting cases of $n = 1$ and $n = 2$ are traditionally attributed to the void growth and void nucleation modes of failure. All other cases characterized by $1 < n < 2$ are considered as a mix of these two failure modes. However, this kind of Black's equation based method is the subject of growing criticism. It is a today's common understanding that n depends on residual stress and temperature [10, 19], and its value is highly controversial. In addition, as it was shown in a number of experiments [11], E_a is a function of the current density. The widely accepted methodology of calculating the MTTF at use condition, represented by chip operation current density and temperature, is using n and E_a determined at the stressed (accelerated) condition, which is characterized by high current densities and elevated temperatures as

shown in Eq. (2.2).

$$MTTF_{\text{use}} = MTTF_{\text{stress}} \left(\frac{j_{\text{stress}}}{j_{\text{use}}} \right)^n exp \left\{ \frac{E_a}{k_B} \left(\frac{1}{T_{\text{use}}} - \frac{1}{T_{\text{stress}}} \right) \right\} \tag{2.2}$$

However, based on above observations, the interdependency of the n and E_a on the current density and temperature, makes this method rather controversial.

The Blech limit [8]:

$$(j \times L) \leq (j \times L)_{\text{crit}} = \frac{2\Omega\sigma_{\text{crit}}}{eZ\rho} \tag{2.3}$$

is employed for the out-filtration of immortal branches, which is also required a serious justification. Here, L is the branch length, Ω is the atomic volume; e is the electron charge, eZ is the effective charge of the migrating atoms, ρ is the wire electrical resistivity, σ_{crit} is the critical stress needed for the failure precursor nucleation for void or hillock. Condition of immortality equation (2.3) means that the atomic flux, generated by stress gradient in the metal lines characterized by $(j \times L) \leq (j \times L)_{\text{crit}}$, compensates the atomic flux caused by electrical current density. It should be mentioned that the Blech limit is valid only for branches with the diffusion blocking boundaries. Accumulation of the hydrostatic stress, caused by redistribution of the metal atoms under the current density action, exceeding the critical stress responsible for void nucleation or the liner rupture, followed by metal extrusion into intra metal dielectric (hillock formation), takes place in branches with the confined metal atoms only.

For a practical integrated circuit layout, the on-chip interconnects such as clock and power grid networks are often with complex structures. Instead of simple straight lines with two-line end terminals, there are interconnect trees representing continuously

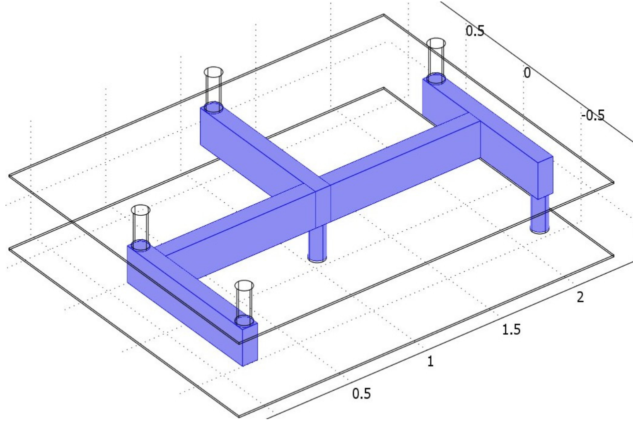


Figure 2.1: Interconnect tree confined by diffusion barriers/liners

connected, highly conductive metal lines within one layer of metallization, terminated by diffusion barriers (Fig. 2.1). The EM effects in those branches are not independent and they have to be considered simultaneously. Absence of blocking boundaries at one or both ends of the individual branches of interconnect trees prevents atoms from accumulation/depletion at the branch ends, and, hence, makes the traditional immortality assessment and MTTF calculation as groundless [20]. A widely practiced decomposing the multi-branch interconnect tree on individual branches and applying the immortality condition to these individual branches makes the EM assessment over optimistic. While all individual branches can satisfy the condition of immortality, the interconnect tree can be mortal [21]. In addition, the presence of residual stresses in the interconnect wires and possible variation of these stresses across on-chip interconnect undermines the procedure of outfiltration of immortal branches based on Blech effect (2.3). Indeed, we need to compare the $(j \times L)$ product calculated for the each interconnect tree with the variable critical product, different for different branches:

$$(j \times L)^i_{\text{crit}} = \frac{2\Omega\Delta\sigma^i}{eZ\rho}; \sigma^i_{\text{init}} + \Delta\sigma^i = \sigma_{\text{crit}} \tag{2.4}$$

Here, σ^i_{init} is the residual stress existing in the interconnect branch before EM stressing was applied. $\Delta\sigma^i$ is the stress developed in the branch after EM stressing was applied. For initial residual stress estimation, many attempts have been made in the past at different granularities. Existing works range from package-scale simulations, which provided large-scale stress/strain variations across the smeared chip layout, which can be zoomed in the area of interests for the detailed analysis, and to the recent development of the multi-scale approach linking the stress generated by different sources with the real layout, see for example [22,23]. Hence, the critical product is not a constant anymore but a variable, which depends on branch location and relates to all possible stress sources. Hence, new, physics-based EM models, which is free of all discussed flaws related to the Black-Blech formulation, should be developed for a robust methodology for the full-chip EM assessment,

The reminder of this chapter is organized as follows: Section 2.2 reviews the physics of electromigration. Section 2.3 discusses the numerical analysis of pre-voiding and post-voiding stress evolution accompanying the void shape motion. Section 2.4 and Section 2.5 introduces the physics-based analytical models for void nucleation time and voiding induced resistance change respectively. The derivation of analytical solutions to predict the kinetics of post-voiding stress and void volume evolution is discussed in Section 2.6. Section 2.7 introduces the technique to assess the evolution of hydrostatic stress inside a multi-branch interconnect tree for more accurate time-to-failure (TTF) prediction. Section 2.8 concludes the chapter.

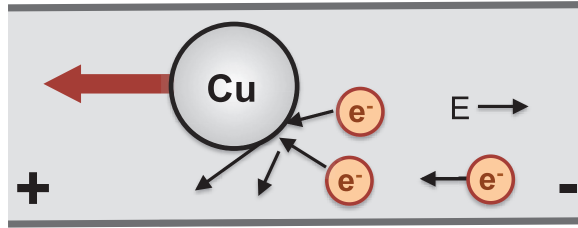


Figure 2.2: Momentum transfer between copper atoms and conducting electrons

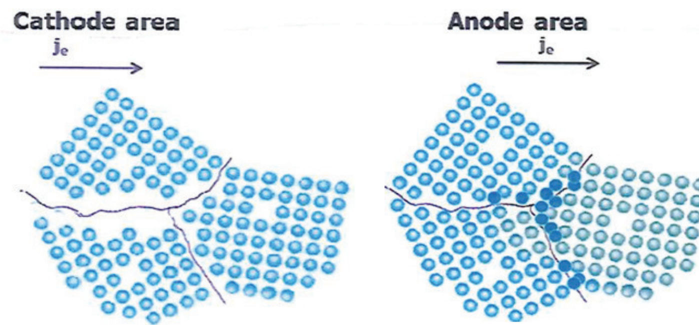


Figure 2.3: Schematic of the plated layers dissolution, (a), and accumulation, (b), at the cathode and anode end of line.

2.2 Electromigration fundamentals

EM is a physical phenomenon of the migration of metal atoms along a direction of the applied electrical field. Atoms (either lattice atoms or impurities) migrate toward the anode end of the metal wire along the trajectory of conducting electrons. This oriented atomic flow, which is caused mostly by the momentum exchange between atoms and the conducting electrons (Fig. 2.2), results in metal density depletion at the cathode, and a corresponding metal accumulation at the anode end of the metal wire (Fig. 2.3). This depletion and accumulation happen because atoms cannot easily escape the metal volume. The rate of EM, as defined by the Nernst-Einstein equation, depends on the atomic diffusivity, meaning different materials are characterized by different rates of EM. Typical interconnect metals,

such as copper (Cu) and aluminum (Al), are prone to EM, due to their high self-diffusivity. Refractive metals, such as tungsten, tantalum, and titanium, demonstrate strong resistance to EM. Because of this big difference in diffusivities of the conducting and barrier metals the interconnect tree is the EM reliability unit of the on-chip interconnects. Thin layers of refractive metals form the diffusion barriers for Cu atoms, preventing them from diffusing into inter-layer (ILD) and inter-metal dielectrics (IMD).

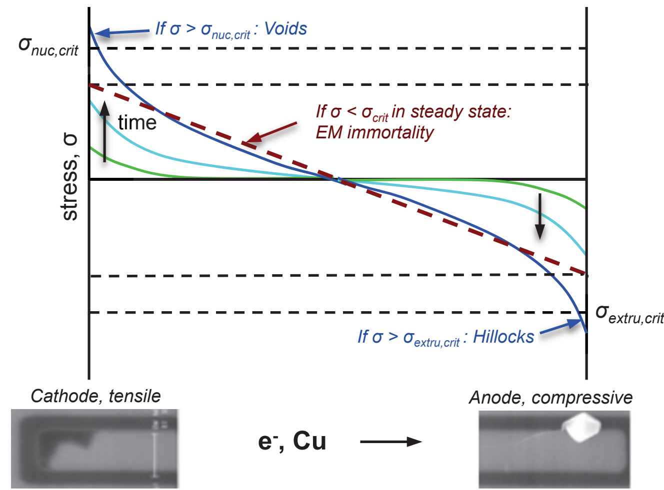


Figure 2.4: The stress development and distribution in EM [1].

When metal wire is embedded into a rigid confinement, which is the case with interconnect metallization, the intention of the wire volume changes (induced by the atom depletion and accumulation due to migration) create tension at the cathode end and compression at the anode end of the line. Over time, the lasting unidirectional electrical load increases these stresses, as well as the stress gradient along the metal line. Electrical current density induced flux is constant throughout the metal line, if the current density and all other parameters are the same everywhere along the line. It is different for the stress

gradient induced atomic flux. Initially, the stresses and corresponding stress gradients were generated at the very ends of the line. These stress gradients initiate a backflow of atoms toward the cathode end at the cathode proximity, and from the anode end in the anode proximity. These stress gradients and generated atomic flows vanish a lot in the portions of line located a little bit away from the line ends, where an inflow of atoms is equal to an outflow. However, with time duration the portions of line characterized by the atomic flux divergence are extended. Indeed, the line branch where one end is already stressed and another is still the stress free is characterize by the flux divergence, which results in accumulation/depletion of atoms and in turn transforms into the generated stress. In some cases, usually when a line is long, the generated stress can reach critical levels, resulting in a void nucleation at the cathode and/or hillock formation at the anode end of line, Fig. 2.4. Different physical mechanisms can be responsible for generating these damages. In the case of voiding, existing cohesive or interfacial micro-cracks near or at the barrier/Cu interfaces can develop into a void by action of the appropriate stresses. Hillock formation, which is a compression-induced extrusion of metal into the surrounding dielectric, that can cause a shortage between neighboring metal lines, can be initiated by micro-cracks in the adhesion/barrier layers.

In the case when an initially void-less confined metal line is stressed with the electric current density a void-related failure process consists of two steps: void nucleation and void growth to the critical volume resulting the critical (say, for example, 10%) increase of line resistance. Void nucleates near the cathode edge of line when the ever increasing tensile stress creates a condition for a stable growth of flaws located at the metal/barrier

interface, [24, 25]. An estimation of the critical stress σ_{crit} needed for forming the growing void on the basis of the classical model of the homogeneous nucleation [26] can be found in [24,25]. It is shown that introduction of a spherical flaw of a radius r into a solid stressed with a tension σ changes its free energy as:

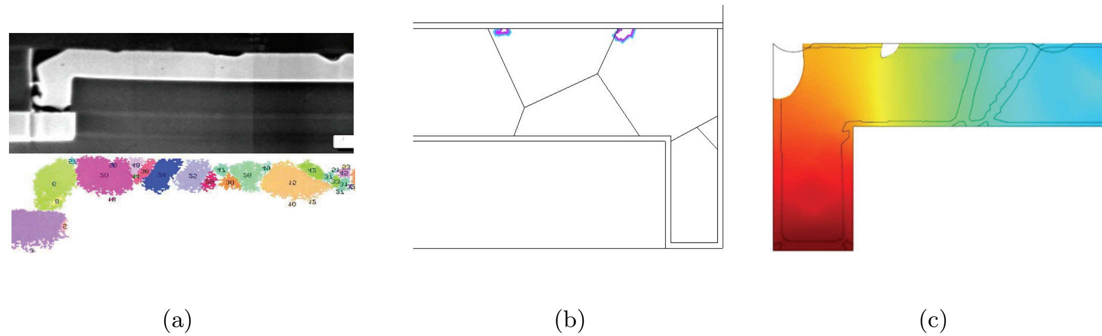
$$\Delta F(r) = 4\pi r^2 \gamma - \frac{4}{3}\pi r^3 \sigma \tag{2.5}$$

Here, γ is the surface energy per unit area, $4\pi r^2 \gamma$ is the increase of the free energy by flaw insertion; $4\pi r^3 \sigma/3$ is the work done by the stress σ to relocate atom, originally occupying the flaw volume, to the solid. Analysis of the equation (2.5) shows that the growth of the flaw with an initial size exceeding $r_{\text{crit}} = 2\gamma/\sigma$ reduces the free energy. Assuming that a void can be originated from a pre-existing flaw only, we can conclude that the flaw with the initial size r_f will grow if the stress exceeds the value:

$$\sigma_{\text{crit}} = \frac{2\gamma}{r_f} \tag{2.6}$$

The assumption about the pre-existing flaws needed for the void nucleation is supported by calculations done by Gleixner and Nix in [24]. They have demonstrated that an enormous energy is required for the homogeneous nucleation of the critical void by agglomeration of vacancies. But their estimation, performed with the representative values of $\gamma = 1J/m^2$, shows that a preexisted flaw with the size of $4nm$ will start growing when the hydrostatic stress will reach the level of $500MPa$. Hence, the void nucleation time t_{nuc} can be determined from the known kinetics of stress evolution caused by electric current density stressing as the instant in time when stress reached the critical level of σ_{crit}, Fig. 2.4.

In addition to voids nucleated at the cathode end of line, where a divergence in atomic flux happens (atom flux is terminated at the barrier interface), additional voids



(a) (b) (c)

Figure 2.5: (a) TEM picture of voids nucleated at the top interface [2], (b) and (c) simulated kinetics of the void nucleation at the triple points and growth (electron flow from right to left), [3], (c) simulated growth of the line corner void by scavenging the vacancy flux and agglomerating with the small voids drifting along the top interface [4].

can be nucleated down to the polycrystalline metal line toward the anode end at any location characterized by the atom flux divergence. These are the triple points formed by intersections between grain boundaries (GB) and the top dielectric barrier (typically composed of SiCN), or contacts between three neighbor grains (Fig. 2.5(a) and Fig. 2.5(b)). Those triple points where the number of outward diffusion channels exceeds the number of inward channels, which can be responsible for the flux divergence, can develop depletion in metal density, leading to the development of tension and possible void nucleation. As shown in Fig. 2.5(c), two major mechanisms of void growth are: (i) scavenging the vacancies that migrate to the void due to the stress gradient between the void surfaces (zero stress) and the surrounding metal (tensile stress), (ii) agglomeration of voids traveling along the metal line toward the cathode end (against the electron flow) due to the capillarity effect. It should be mentioned that we does not consider the hillock-induced failure since its less frequent appearance in comparison with the void-induced failure. Experiments demonstrate that the level of stress needed for the generation of hillocks is much higher than in the case of voiding. In addition, more severe process-induced flaws, such as ruptures of the barrier

liners, should be presented, that are also less frequent than small cavities playing a precursor role for voiding.

2.3 Stress and void evolution in confined metal lines: numerical analysis

In this section we provide the formalism developed for the finite-element analysis (FEA)-based simulation of pre-voiding stress evolution in the confined metal line loaded with the unidirectional electric current, and the further post-voiding stress evolution accompanying the void shape evolution and void motion.

2.3.1 Pre-voiding stress evolution

When the deformation of metal is generated by volumetric causes such as atom density redistribution, the stress is generated by the interaction with confinement. Therefore, the theories of EM-induced stress build-up consider two main inter-related processes: atomic diffusion due to electron wind force and the corresponding strain-stress generation.

A vacancy mechanism of atomic diffusion accepted in these theories is valid for the interconnect metals: atoms migration through the vacant lattice sites is described as a flow of vacancies. The kinetic equation for the vacancy concentration $N(r,t)$, describing the rate of the vacancy concentration as a divergence of the vacancy flux, should take into account an equilibration of the vacancy concentration with the hydrostatic stress. This equilibrium achieves by the generation-annihilation of the vacancy-extra (plated) atom pairs. In the confined polycrystalline copper lines, the copper interfaces with barriers and grain bound-

aries are the sites for these pair generation-annihilation. The equilibrium concentration of vacancies is determined by the energy of GB or interface deformation by the plated atoms and the energy of volume relaxation around the formed vacancy. This concentration is defined by the local hydrostatic stress σ_{Hyd} and the thermal energy $k_B T$:

$$N_{\text{eq}} = N_0 exp\left\{\frac{f\Omega\sigma_{\text{Hyd}}}{k_B T}\right\} \tag{2.7}$$

where N_0 is the thermodynamic vacancy concentration in the stress-free state, f is the ratio of the vacancy and atomic volumes. The rate of the generation-annihilation of the vacancy-plated atom pairs can be presented in the relaxation time τ approximation:

$$G_V = -\frac{N - N_{\text{eq}}}{\tau} \tag{2.8}$$

A detailed description of the vacancy generation/annihilation modeling approach could be found in [4,27] and in the literature cited there. Thus, evolution of the vacancy concentration is described by the following continuity equation:

$$\begin{aligned} &\frac{\partial N}{\partial t} + \nabla J_{\text{vac}} + G_V = 0 \\ &J_{\text{vac}} = -D\nabla N - \frac{DN}{k_B T}\left\{(1-f)\Omega\nabla\sigma_{\text{Hyd}} - eZ\rho j\right\} \end{aligned} \tag{2.9}$$

where J_{vac} is the flux of vacancies, N is the vancancy concentration and D is the diffusivity of vacancies. It should be mentioned that the term G_v is described by (2.8) on the interfaces and GBs and is equal to zero in the grain interiors. The diffusivity D is also stress-dependent:

$$D = D_0 exp\left\{-\frac{E_D - \Omega\sigma_{\text{Hyd}}}{k_B T}\right\} \tag{2.10}$$

and has much larger values on the interfaces and GBs, than in the grain interior.

Since the plated on GBs and interfaces extra atoms are practically immobile, the kinetics of their concentration M is governed by the rate of its generation-annihilation:

$$\frac{\partial M}{\partial t} + G_V = 0 \tag{2.11}$$

In order to obtain the solutions of the equations (2.9)-(2.11), we need, as it was mentioned earlier, to couple them to the equations describing the evolution of the strain/stress and the current density taking place under the redistribution of vacancies and plated atom densities. The current density $j = \nabla V/\rho$ is determined by means of Laplace's equation for the electric potential V:

$$\nabla\left(\frac{1}{\rho}\nabla V\right) = 0 \tag{2.12}$$

where ρ is the resistivity of the wiring metal. Stress is caused by a deformation of the metal line volume, which is characterized by two strain components: elastic deformation, which is a result of inhomogeneities in the vacancy/plating atom distributions and interaction with the confinement, and inelastic deformation, due to vacancy/plating atom generation/annihilation and vacancy migration. By representing the concentration of vacancies and plated atoms in $1/\Omega$ units, we get the inelastic volume deformation as a strain tensor: $\varepsilon^{\mathrm{inel}} = -(1-f)(N-N_0)+(M-M_0)$. The generated strain includes also the elastic component $\varepsilon^{\mathrm{el}}$, which determines the stress components according to the Hook's law. The total strain is defined by the displacement vector u as $\varepsilon_{\mathrm{ij}} = (\partial u_i/\partial x_j + \partial u_j/\partial x_i)/2$ (here values of the index $i = (1,2,3)$ correspond to the coordinates $x_i = (x,y,z)$ and components of displacement vector $u_i = (u_x,u_y,u_z)$). Final equations for the displacement vector components are:

$$(\lambda+\mu)\frac{\partial \varepsilon}{\partial x_i} + \mu\Delta u_i + \frac{E}{3(1-\nu)}\frac{\partial(M-(1-f)N)}{\partial x_i} = 0 \tag{2.13}$$

Here, λ, μ, E, and ν represent the Lame constant, shear modulus, Young's modulus, and Poisson's ratio of the metal. Coupled solution of equations (2.7)-(2.13) allows us to describe the kinetics of the stress, vacancy, and plating atom concentration for realistic 3-D problems.

In the case when the achieved steady state stress does not exceed the critical value $\sigma_{\mathrm{Hyd}}^{\mathrm{crit}}$ required for void nucleation, the wire remains immortal. The steady state is established when the electron wind induced vacancy flux vanishes by the opposite stress gradient induced flux and the equilibrium vacancy concentration is established. The conditions: $J_{\mathrm{vac}} = 0$ and $N = N_{\mathrm{eq}}$ for a single line result in the Blech equation for the critical product current density j and line length L: $(j \times L)_{\mathrm{crit}} = \sigma_{\mathrm{Hyd}}^{\mathrm{crit}} \Omega / eZ\rho$. In the case of interconnect trees, the steady state stresses in all nodes are inter-related and depend on segment lengths L_{ij} and current densities j_{ij} in all branches:

$$\sum_{\mathrm{i,j}} \left(\sigma_{\mathrm{Hyd}}^{i} - \frac{eZ\rho j_{\mathrm{ij}} L_{\mathrm{ij}}}{2\Omega} \right) L_{\mathrm{ij}} = 0 \tag{2.14}$$

2.3.2 Void motion and post-voiding stress evolution

If the applied current is large enough to generate stress exceeding the critical value, voids can be nucleated in the region with large tensile stress. EM theory presented above can be employed for the description of the post-voiding stress evolution, by combining it with phase-field methodology [28]. This method allows to get zero normal stress on the void surface. Voids are described as sinks for vacancies: outflow of atoms from the void surface are considered as inflow of vacancies, resulting in motion of the void-metal interface.

Phase-field method describes the void and metal regions as two different phases of

the medium: an order parameter ϕ is introduced, which is defined as:

$$\phi = \begin{cases} 1, & \text{in metal} \\ -1, & \text{in void} \end{cases} \tag{2.15}$$

A smooth transition between these two phases and corresponding values of ϕ in a narrow region d represents the void-metal interface. Evolution of the order parameter describes the interface motion that changes the distribution of two phases in space and time; hence, the term “phase-field is used. The details of this approach are presented below.

The basic non-linear equation of the model is

$$\eta \frac{\partial \phi}{\partial t} - \xi \nabla^2 \phi + (\phi^2 - 1)\phi + (\eta v)\nabla \phi = 0 \tag{2.16}$$

Here the viscosity η is responsible for duration of void formation process (as it is considered below). The meaning of the parameters ξ and v becomes clear from the analytical solution of equation (2.16) in 1-D case:

$$\phi(x,t) = tanh \frac{x - x_0 - vt}{\sqrt{2\xi}} \tag{2.17}$$

where the coordinate x_0 corresponds to the void surface location at nucleation time instance. This solution demonstrates, that the thickness of void surface is $d = \sqrt{2\xi}$, and v represents the velocity of the surface motion.

Equation (2.16) shows that that in equilibrium, i.e. when $\partial\phi/\partial t = 0, v = 0$, the order parameter can have values 1 or -1. Follow equation (2.15), we choose the condition $\phi(t < t_{\text{nuc}}) = 1$. Void nucleation i.e. origination of a region with $\phi = -1$ is described by the same equation (2.16) by adding a term F:

$$\eta \frac{\partial \phi}{\partial t} - \xi \nabla^2 \phi + (\phi^2 - 1)\phi + (\eta v)\nabla \phi = F(\sigma_{\text{Hyd}}) \tag{2.18}$$

Here the "external" force F depends on the developed stress in the metal as

$$F(\sigma_{\text{Hyd}}) = -F_0 \cdot (\phi + 1) \cdot \begin{cases} 0, & \text{if } \sigma_{\text{Hyd}} < \sigma_{\text{Hyd}}^{\text{crit}} \\ 1, & \text{if } \sigma_{\text{Hyd}} \geq \sigma_{\text{Hyd}}^{\text{crit}} \end{cases} \tag{2.19}$$

Here the parameter F_0 (along with the viscosity η) defines the duration of the nucleation process. The force (2.19) originates at any site where the critical tensile stress is achieved, and provides a local shift of the phase field from the initial state $\phi = 1$. This force influences on the system during a short period of time $\tau \sim \eta/F_0$, when the order parameter evolves locally in the range $-1 < \phi < 1$. As the new state $\phi = -1$ is achieved, which denotes void nucleation, the force F vanishes (due to multiplier $(\phi + 1)$ in (2.19)).

Further dynamics of the nucleated void is described by equation (2.16), which provides the interface motion with velocity v. This motion is caused by inflow or outflow of atoms from the void surface, as well as by the atoms migration on the void interface. In the employed vacancy diffusion model, this velocity is proportional to the gradient of inflow/outflow flux of vacancies and gradient of the void surface flux:

$$v = \nabla J_{\text{vac}} + \frac{\partial J_{\text{vac}}^{\text{surf}}}{\partial s} \tag{2.20}$$

Here s is a unit tangent vector, the surface flux of vacancies is determined by the directional derivative of the curvature K and by the surface tension energy g: $J_{\text{vac}}^{\text{surf}} = \frac{DNg}{k_B T} \frac{\partial K}{\partial s}$.

Thus, equations (2.16) and (2.20) describe the dynamics of nucleated voids as evolution of regions characterized by the phase field value $\phi = -1$. It is obvious that the conductivity ($c = 1/\rho$) and Young's modulus of metal, diffusivity of vacancies, and their generation/annihilation rate become equal to zero in the voided regions. This is done by

replacing these parameters by the expressions:

$$\begin{gathered} c_\phi = c\psi, E_\phi = E\psi, D_\phi = D\psi, \\ G_\phi = G_V\psi, \psi = \frac{1+\phi}{2} \end{gathered} \tag{2.21}$$

Along with the definitions (2.21) we introduce large surface diffusivity, using an empiric parameter $\zeta >> 1$:

$$D_{\text{surf}} = \zeta \cdot D \cdot (1 - |\phi|) \tag{2.22}$$

Combination of phase-field equations (2.15)-(2.22) with EM equations (2.7)-(2.14) represents a self-consistent model for study of EM-induced void nucleation and growth.

This formalism has allowed simulating of many interesting cases such as effect of interfaces [29] and GB [27] on the stress and vacancy concentration evolution in the confined metal branches, role of grain crystallography on voiding [2], void migration along metal line with GB [4], etc. While being successful in simulating the EM related physics in the frame of the FEA, this type of modeling cannot be employed for predicting EM-induced degradation in modern VLSI circuits, which needs the simultaneous analysis of stress evolution caused by the electrical load in hundreds of millions interconnect branches. A reason is the enormous size of the computational problem. To address this problem it is desirable to have analytical descriptions of the void nucleation time and kinetics of void size evolution which, while being simple enough to provide fast simulations, should contain the dependencies on all major parameters such as material properties, segment geometries, grain size and morphology, temperature, diffusivities, etc.

2.4 Nucleation phase and nucleation time

Such analytical formulation has been proposed and developed by Korhonen [30], and further developed by other researchers, see for example [25, 31, 32]. In a simple 1-D approximation, which was used by Korhonen [30], for deriving a model of the stress evolution in a confined and electrically loaded metal line, a standard assumption was employed: the divergence of the atomic flux Γ_A generates a volumetric stress Θ:

$$\frac{\partial \Theta}{\partial t} = \Omega \frac{\partial \Gamma_A}{\partial x} \tag{2.23}$$

Here, Γ_A is a total atomic flux comprised by the fluxes caused by the EM force and stress gradient:

$$\Gamma_A = \frac{D_a}{\Omega k_B T} \left(eZ\rho j + \frac{\partial \Omega \sigma}{\partial x} \right) \tag{2.24}$$

Here, D_a is the effective atomic diffusivity, eZ is the effective charge of migrating atoms, B is the effective bulk elasticity modulus, Ω is the atomic lattice volume, ρ is the metal resistivity, j is the current density, k_B is the Boltzmann constant, T is the temperature, x is the coordinate along the line, and t is time. We assume here that the lattice cite concentration is taken as $N_a = 1/\Omega$. Substituting the total flux Γ_A and the volumetric strain as $\Theta = \sigma/B$ in equation (2.23) provides:

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x} \frac{D_a B \Omega}{k_B T} \left(\frac{eZ\rho j}{\Omega} + \frac{\partial \sigma}{\partial x} \right) \tag{2.25}$$

Equation (2.25) is the well-known Korhonen's equation describing evolution of the stress distribution along the confined metal line caused by the applied electric current [19]. A number of the simplifying assumptions are adopted: it is assumed that the confinement (metal and dielectric barriers) is absolutely rigid, the atom diffusivity does not depend on

stress; vacancy concentration is in the equilibrium with stress at any instant in time everywhere including grain interior; stress evolution is caused just by the atomic flux divergence, the additional stress evolution due to vacancy equilibration with the stress isn't accounted. It should be mentioned, while the derivation of equation (2.25) was done for 1-D line, the employed effective valence Z and atomic diffusivity D_a allow accounting some elements of wire texture and 3-D geometry [10].

A solution to this initial-boundary value problem in the case of a finite line with the diffusion blocking ends located at $x = 0$ and L, where L is the line length, loaded with the DC current density j was obtained by the method of separation of variables in [19]:

$$\sigma = \sigma_T + \frac{eZ\rho jL}{\Omega}\left\{\frac{1}{2} - \frac{x}{L} - 4\sum_{n=0}^{\infty}\frac{cos\left(\frac{(2n+1)\pi x}{L}\right)}{(2n+1)^2\pi^2}e^{-\kappa\frac{(2n+1)^2\pi^2}{L^2}t}\right\} \tag{2.26}$$

Here, σ_T is the residual stress preexisting in the line, $\kappa = \frac{D_a B\Omega}{k_B T}$, and $D_a = D_0 e^{-\frac{E_D - \Omega^* \sigma_T}{k_B T}}$, where E_D is the activation energy of the atom diffusion, and an activation volume $\Omega^* \approx 0.95\Omega$ is the combination of the vacancy formation and the migration volumes [33].

Approximate value of void nucleation time extracted from equation (2.26), which is determined as an instant in time when the stress at the cathode end of line ($x = 0$) is reached σ_{crit} is:

$$t_{\text{nuc}} \approx \frac{L^2 k_B T}{2D_a B\Omega} ln\left\{\frac{\frac{eZ\rho jL}{2\Omega}}{\sigma_T + \frac{eZ\rho jL}{2\Omega} - \sigma_{\text{crit}}}\right\} = \frac{L^2}{2D_0}\frac{k_B T}{\Omega B}e^{\frac{E_V + E_{\text{VD}} - \Omega^* \sigma_{\text{crit}}}{k_B T}} \times ln\left\{\frac{\frac{eZ\rho jL}{2\Omega}}{\sigma_T + \frac{eZ\rho jL}{2\Omega} - \sigma_{\text{crit}}}\right\} \tag{2.27}$$

where $D_a \approx N_V D_V = D_0 e^{(-\frac{E_V + E_{\text{VD}} - \Omega^* \sigma_{\text{crit}}}{k_B T}}$. Here N_V and D_V are the vacancy concentration and vacancy diffusivity, E_V and E_{VD} are the activation energy of vacancy formation and diffusion, σ_T is the thermal stress developed in the metal line confined in the ILD/IMD

dielectric during cooling from the zero stress temperature T_{ZS} down to the temperature of use condition.

2.5 Growth phase and the rate of wire resistance change

The second phase is the void size growth mode. Void is formed at t_{nuc} and grows at $t > t_{nuc}$. It is clear that only the void growth mode can be responsible for the line resistance degradation. Indeed, continuous reduction of the metal line cross section area at the location of the growing void, which in the extreme case forces the current to flow through the highly resistive metal diffusion barriers when void cuts the entire metal cross section, is accompanied by line resistance increase. A void nucleation, which represents a transformation of the process-induced flaws located at the metal/passivation interface into the stable growing void that happens when a level of the EM-induced hydrostatic tensile stress reaches the critical, cannot introduce any noticeable changes in the line resistance. Hence, the kinetics of EM-induced degradation of the line resistance should be characterized by the presence of an initial incubation time, needed for void nucleation, followed by the resistance increase caused by the void growth. Exactly this type of kinetics is observed in experiments [34]. An accurate description of the void growth kinetics is quite complicated. It involves atom migration along the void surface and the atom transfer into the metal under the action of electric current density and stress field. When the post-voiding evolution of stress is considered, two different cases characterized by different initial conditions at the moment when the electric current density is applied should be analyzed.

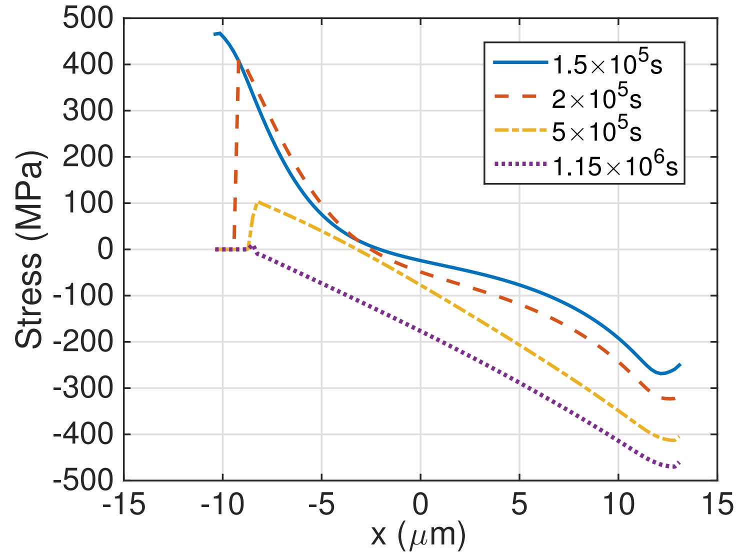
The first one is the case when the thermal stress-induced void pre-exists inside

analyzed segment. At the equilibrium the stress everywhere in the metal line is zero [25,35]. Later, upon loading the line with electric current, the stress is developing along the growth of the preexisting void. In this case, initially, the void volume grows linearly with current density [25,35]. This type of kinetics, strictly speaking, is valid in the cases of the unconfined line edge drift [36], and the initial growth of a saturated void, preexisted in the confined metal line [35], when the stress in the line has a negligible effect on the movement of the free surface. Quite different void volume evolution takes place when an initially void-less metal line embedded into the rigid confinement is stressed with electric current density. In this case we have a void evolution consisting of two steps: already discussed void nucleation and void growth. A portion of metal neighboring the surface of growing void is under essential tension, which can be estimated from Eq. (2.28). A large stress gradient, which is developed between the zero normal stress void surface and the surrounding metal with the hydrostatic stress of the order of magnitude of σ_{crit}, pushes the atoms to escape the void surface toward the metal bulk.

$$\sigma_{\text{crit}} = \sigma_T + \frac{eZ\rho jL}{\Omega}\left\{\frac{1}{2} - 4\sum_{n=0}^{\infty}\frac{1}{(2n+1)^2\pi^2}e^{-\kappa\frac{(2n+1)^2\pi^2}{L^2}t_{\text{nuc}}}\right\} \tag{2.28}$$

Fig. 2.6 shows the evolution of stress in the initially void-less metal line taking place after the void nucleation. This result was obtained from the numerical solution of the system of PDEs presented in Sec. 2.3 describing the void evolution with COMSOL FEA tool. It can be seen from this figure that in initial times, the atomic flux at the void surface is mainly determined by the large stress gradient. We will demonstrate in Section 2.6 that the initial evolution of the void volume does not depend on the electric current density contrary

(a)



(b)

Figure 2.6: (a) Simulated void evolution at the cathode end, contours correspond to the center of the void/metal interface and (b) post-voiding stress evolution when the void was nucleated by electrical stressing calculated with COMSOL FEA tool.

to the case of the line edge drift approximation characterized by the linear dependence of the initial void growth rate on the current density. At long-time limit the derived solution provides the same steady state with the stress linearly distributed along the line as in the case of preexisted void.

Void growth is accompanied by redistribution of the extra atoms, previously occupied the void volume, through the metal line. It reduces tensile stress at the cathode side of the line and increases compressive stress at the opposite anode side. Conventional

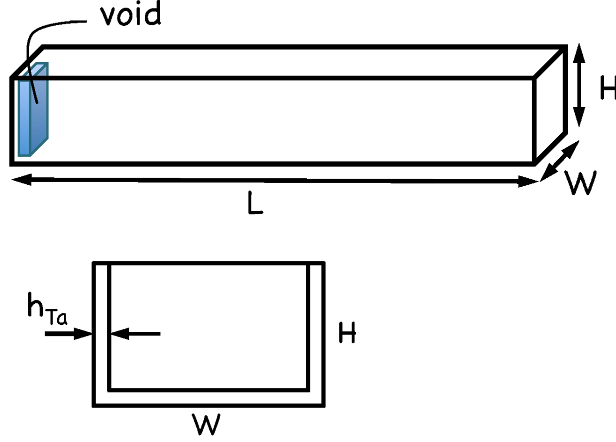


Figure 2.7: Schematics of the line geometry.

method (pre-existing void case) accepts that the drift velocity of the void edge relates to atomic flux ($J = \frac{D_a eZ\rho j}{\Omega k_B T}$) as $\vartheta = \Omega J$ [25], we can express it as:

$$\vartheta = \frac{D_a}{k_B T} eZ\rho_{\mathrm{Cu}} j \tag{2.29}$$

Kinetics of the change of the branch resistance can be described as:

$$\Delta r(t) = \vartheta \cdot (t - t_{\mathrm{nuc}}) \cdot \left[\frac{\rho_{\mathrm{Ta}}}{h_{\mathrm{Ta}}} \cdot \frac{1}{2H + W} - \frac{\rho_{\mathrm{Cu}}}{HW} \right] \tag{2.30}$$

Where ρ_{Ta} and ρ_{Cu} are the resistivities of the barrier material (Ta/TaN) and copper, W is the line width, H is the copper thickness, and h_{Ta} is the barrier layer thickness schematically shown in Fig. 2.7. It is assumed that a void occupies the whole cross section of the line and the current is forced to flow through the barrier layer at that portion of the line. Void growth continues until its volume reaches the so-called saturation value. This so-called saturated void is formed when the flux of atoms previously located in the part of metal, which is consuming by the growing void, is balanced by the back flux of atoms generated by the gradient of the building up stress. If the wire is stressed under constant current density,

we can derive the void saturated volume by using the following equation [25],

$$\frac{V_{\text{SS}}^{\text{volm}}}{V_{\text{line}}^{\text{volm}}} = \frac{\sigma_T}{B} + \frac{eZ\rho jL}{2B\Omega} \tag{2.31}$$

Here, $V_{\text{SS}}^{\text{volm}}$ is the void saturated volume, and $V_{\text{line}}^{\text{volm}}$ is the total volume of the metal line. Expression (2.31) was obtained under the assumption of a constant current density load. On the other hand, when a constant voltage V is applied to the line ends, then the change in the current density, caused by the growing void Eq. (2.30), should be taken into account. In other words, the current density is no longer constant in this case. Based on the obvious relations $j(t) = j_0/(1 + \Delta r(t)/r_0)$ and $\Delta r(t)/r_0 \approx V^{\text{volm}}(t)/V_{\text{line}}^{\text{volm}}$, where j_0 and r_0 are the current density and line resistance before void was nucleated, the condition of the formation of saturated void volume takes the form:

$$\frac{V_{\text{SS}}^{\text{volm}}}{V_{\text{line}}^{\text{volm}}} = \left(\frac{\sigma_T}{B} + \frac{eZ\rho j_0 L}{2B\Omega}\right)/(1 + \frac{eZ\rho j_0 L}{2B\Omega}) \tag{2.32}$$

Based on Eq. (2.29), Eq. (2.30) and Eq. (2.32) we can derive the void growth kinetics:

$$\frac{V^{\text{volm}}(t)}{V_{\text{line}}^{\text{volm}}} = \frac{D_a eZ\rho j_0}{k_B TL \cdot \left(1 + \frac{V^{\text{volm}}(t)}{V_{\text{line}}^{\text{volm}}}\right)} \cdot (t - t_{\text{nuc}}) \approx \frac{D_a eZ\rho j_0}{k_B TL} \cdot (t - t_{\text{nuc}}) \times \left[1 - \frac{D_a eZ\rho j_0}{k_B TL} \cdot (t - t_{\text{nuc}})\right] \tag{2.33}$$

and time needed to reach the void saturated volume:

$$t_{\text{VS}} = t_{\text{nuc}} + \frac{k_B TL^2}{2B\Omega D_a} \cdot \left(1 + \frac{2\sigma_T \Omega}{eZ\rho j_0 L}\right) \tag{2.34}$$

Upon reaching the saturation, the further void growth is stopping and the line resistance comes to saturation. This steady state lasts as long as the applied voltage is keeping constant. When the voltage is changed the void size and line resistance again start evolving toward the new steady state.

2.6 Post-voiding stress and void volume evolution

Now we will describe the analytical solution of the initial boundary value problem (IBVP), Eq. (2.25), that provides the post-voiding stress and void volume evolution. We assume that the time is counted from the moment when the void was nucleated t_{nuc}. Void is nucleated at the cathode edge of line: $x = 0$. We also introduce the effective thickness of the void interface δ, which is infinitely small in comparison with all other involved length. It allows us to introduce a stress gradient between the zero stress void surface and the surrounding metal as $\nabla\sigma = \sigma(\delta, t)/\delta$, where $\sigma(\delta, t) \approx \sigma(0, t)$ is the time dependent stress in the metal near the void surface. Thus, the considered IBVP can be written as

$$\begin{cases} PDE: \dfrac{\partial\sigma}{\partial t} = \kappa^2 \dfrac{\partial^2\sigma}{\partial x^2} \ ; 0 < x < L, 0 < t < \infty \\ BC: \dfrac{\partial\sigma}{\partial x}(0,t) = \dfrac{\sigma(0,t)}{\delta}; 0 < t < \infty \\ BC: \dfrac{\partial\sigma}{\partial x}(L,t) = -G; 0 < t < \infty \\ IC: \sigma(x,0) = \sigma_T - Gx + \dfrac{GL}{2} - \\ 4GL \displaystyle\sum_{n=0}^{\infty} \frac{\cos\frac{(2n+1)\pi x}{L}}{\pi^2(2n+1)^2} exp\left\{-\left(\kappa\frac{(2n+1)\pi}{L}\right)^2 t\right\} \end{cases} \tag{2.35}$$

Here, "PDE" is for the "partial differential equation", $\kappa^2 = D_a B\Omega/k_B T$, $G = eZ\rho j/\Omega$. The solution of this problem can be obtained by the standard separation variable method. It yields:

$$\sigma(x,t) = -Gx + \sum_{m=0}^{\infty} \frac{A_m}{\sin(\lambda_m L)} \cos[\lambda_m(L - x)] exp\left\{-(\kappa\lambda_m)^2 t\right\} \tag{2.36}$$

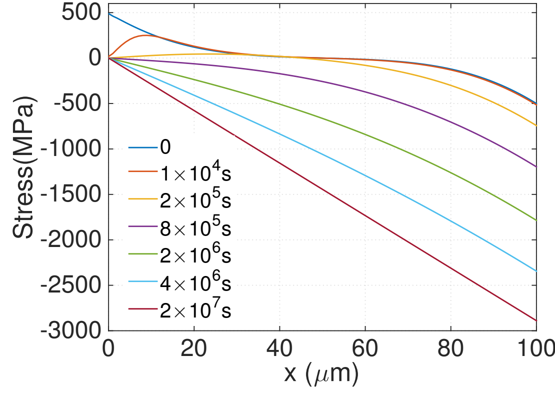
Here, the eigenvalues λ_m of this IBVP can be obtained from a solution of the equation:

$$\lambda_m L = \frac{L}{\delta} \cot \lambda_m L \tag{2.37}$$

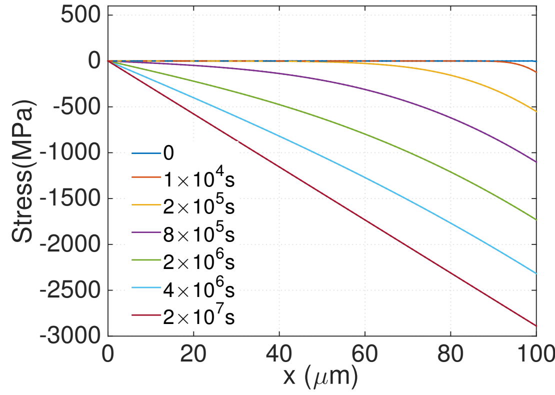
which is derived from the BCs, and all coefficients A_m, which are derived from the IC, take the form:

$$\frac{A_m}{\sin(\lambda_m L)} = \frac{4}{\pi}(\sigma_T + \frac{GL}{2})\frac{\sin(\lambda_m L)}{2m+1} - \frac{16}{\pi}GL \times \sum_{n=0}^{\infty} \frac{exp\{-(\kappa \frac{(2n+1)\pi}{L})^2 t_{\text{nuc}}\}}{\pi^2(2n+1)^2} \frac{(2m+1)\sin(\lambda_m L)}{(2m+1)^2 - 4(2n+1)^2} \tag{2.38}$$

It is easy to show, by employing the known relations [37]: $\sum_{m=0}^{\infty} \frac{(2m+1)\sin[(2m+1)\xi]}{(2m+1)^2 - 4(2n+1)^2} = \frac{\pi}{4}\cos[2(2n+1)\xi]$ and $\sum_{m=0}^{\infty} \frac{\sin[(2m+1)\xi]}{2m+1} = \frac{\pi}{4}$, that the expression (2.36) with A_m, described by (2.38), satisfies the initial condition (2.35), including: $\sigma(x = 0, t = 0) = \sigma_{crit}$. Fig. 2.8(a) shows the evolution of stress starting from the void nucleation time $t = 0$ till the steady state is achieved. All calculations were performed with the following parameters: $B = 3 \cdot 10^{10} Pa$, $\Omega = 1.66 \cdot 10^{-29} m^3$, $k_B = 1.38 \cdot 10^{-23} J/K$, $L = 1 \cdot 10^{-4} m$, $\sigma_T = 0$, $Z = 10$, $e = 1.6 \cdot 10^{-19} q$, $\rho = 3 \cdot 10^{-8} Ohm \cdot m$, $D_0 = 7.56 \cdot 10^{-5} m^2/s$, $E_a = 1.6 \cdot 10^{-19} J$, $D_a(T = 400K) = 1.58 \cdot 10^{-17} m^2/s$, $\sigma_{\text{crit}} = 500MPa$, $\delta = 1 \cdot 10^{-9} m$. Fig. 2.8(b) shows the evolution of stress distribution along the line with the preexisted saturated void [35]. Compare these two figures side by side one can notice the big difference in stress evolutions taking place in initial times, which disappears at long times, resulting the same steady state stress distributions. This initial difference in stress evolution results the different void growth kinetics occurring in these two cases. For the initially void-less line, the void volume



(a)



(b)

Figure 2.8: Evolution of the distribution of the hydrostatic stress along the metal line loaded with the DC current of $1\cdot10^{10}A/m^2$ at $T=400K$ at two different ICs: void-less metal line, (a), and the line with the preexisted saturated void at the cathode end, (b).

determined as: $V_{\text{void}}(t)=V_{\text{line}}\int_0^L\frac{\sigma(x,t)}{B}dx$, is

$$\begin{aligned}\frac{V_{\text{void}}(t)}{V_{\text{line}}}&=\left(\frac{\sigma_T}{B}+\frac{GL}{2B}\right)\left(1-\frac{8}{\pi^2}\sum_{m=0}^{\infty}\frac{exp\{-(\frac{\pi\kappa(2m+1)}{2L})^2t\}}{(2m+1)^2}\right)+\\ &\frac{32}{\pi^2}\frac{GL}{B}\sum_{n=0}^{\infty}\frac{exp\{-(\frac{\pi\kappa(2n+1)}{L})^2t_{\text{nuc}}\}}{\pi^2(2n+1)^2}\sum_{m=0}^{\infty}\frac{exp\{-(\frac{\pi\kappa(2m+1)}{2L})^2t\}}{(2m+1)^2-4(2n+1)^2}\\ &=\left(\frac{\sigma_T}{B}+\frac{GL}{B}\right)-\frac{8}{\pi^2}\sum_{m=0}^{\infty}\frac{exp\{-(\frac{\pi\kappa(2m+1)}{2L})^2t\}}{\pi^2(2m+1)^2}\\ &\times\left(\frac{\sigma_{\text{crit}}}{B}-16\frac{GL}{B}\sum_{n=0}^{\infty}\frac{exp\{-(\frac{\pi\kappa(2n+1)}{L})^2t_{\text{nuc}}\}}{\pi^2\left[(2m+1)^2-4(2n+1)^2\right]}\right)\end{aligned}\tag{2.39}$$

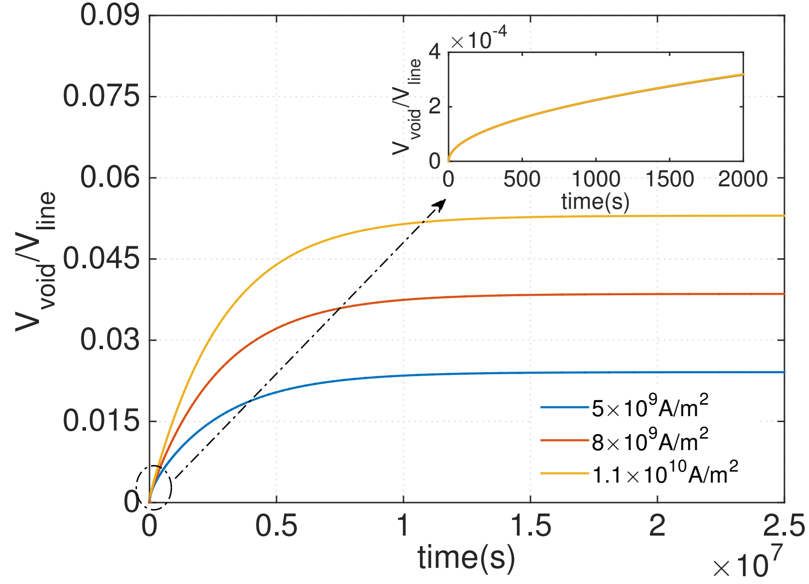
Here, $V_{\text{line}} = LWH$ is the line volume, W and H are the line width and thickness. Figures 2.9(a), and 2.9(b) demonstrate the void evolution kinetics caused by the same DC currents in two cases: (a) an initially void-less line where a void was nucleated when the stress has reached σ_{crit}, and (b) a line with initially preexisted void, characterized by the volume growth kinetics developed by He and Suo [35, 38]:

$$V_{\text{void}}(t) \quad = \quad V_{\text{sat}} \quad \times \quad \left(1 - \frac{32}{\pi^3}\sum_{n=0}^{\infty}\frac{(-1)^n}{(2n+1)^3} exp\left\{-\left(\kappa\frac{(2n+1)\pi}{2L}\right)^2 t\right\}\right) \tag{2.40}$$

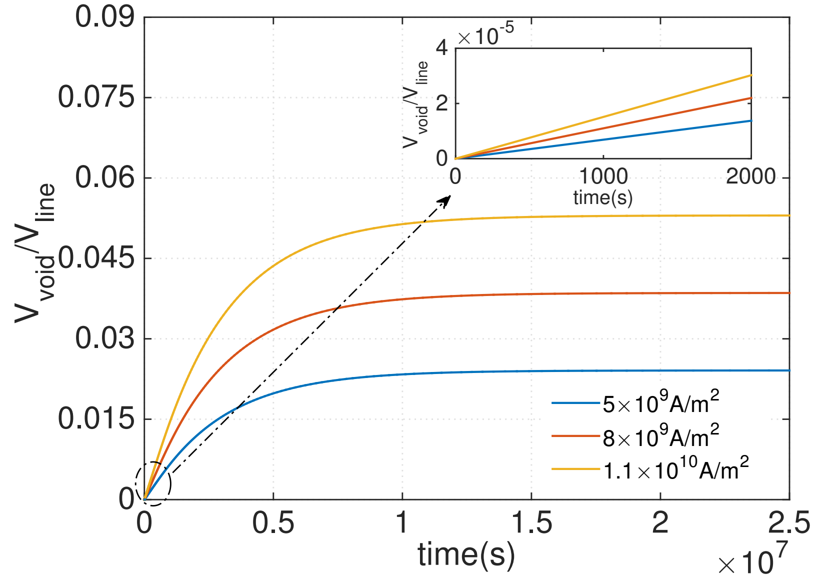
Here, $V_{\text{sat}} = WH\frac{GL^2}{2B}$ is the void saturation volume, which is developed when the EM-induced atomic flux is balanced by the stress gradient induced flux. The kinetics of the line resistance change caused by void evolution, as it was shown, for example in [20, 35], is $\Delta R(t) = V_{\text{void}}(t)\left(\frac{\rho_{\text{TaN}}}{h_{\text{lin}}(W+2H)} - \frac{\rho_{\text{Cu}}}{WH}\right)$. Here, ρ_{TaN} and ρ_{Cu} are the resistivity of the barrier material (Ta/TaN) and copper, h_{lin} is the thickness of the barrier layer. Fig. 2.7 shows the schematics of the line with void.

Two most important observations are the following. First, the void volume increases much faster in the case of initially void-less line, Fig. 2.10(a), and, second, at initial times (up to $10^4 s$ for the chosen parameter values) the void growth, in this case, does not depend on the current density. It contradicts to the case of a line with the preexisted void where the void growth at initial times is linearly proportional to the current density [35], (see insertions to the Fig. 2.9(a) and Fig. 2.9(b)). Analysis of the void growth kinetics (2.39) at the initial moments of time shows that a square root time dependence $\frac{V_{\text{void}}(t)}{V_{\text{line}}} = \frac{\sigma_{\text{crit}}\Omega}{k_B T}\frac{\sqrt{D_a t}}{L}$ fits very well to the model, Fig. 2.10(c).

Fig. 2.10 shows that 10% degradation of line resistance, which is calculated with, $\rho_{\text{TaN}} = 2.5 \cdot 10^{-6} Ohm \cdot m$, $\rho_{\text{Cu}} = 3 \cdot 10^{-8} Ohm \cdot m$, $H = 120nm$ and $h_{\text{lin}} = 10nm$, caused



(a)



(b)

Figure 2.9: (a) Evolution of void volume in the metal line loaded with the DC currents at $T = 400K$ and $\sigma_T = 0$ at two different ICs: void-less metal line,(b) the line with the preexisted saturated void at the cathode end.

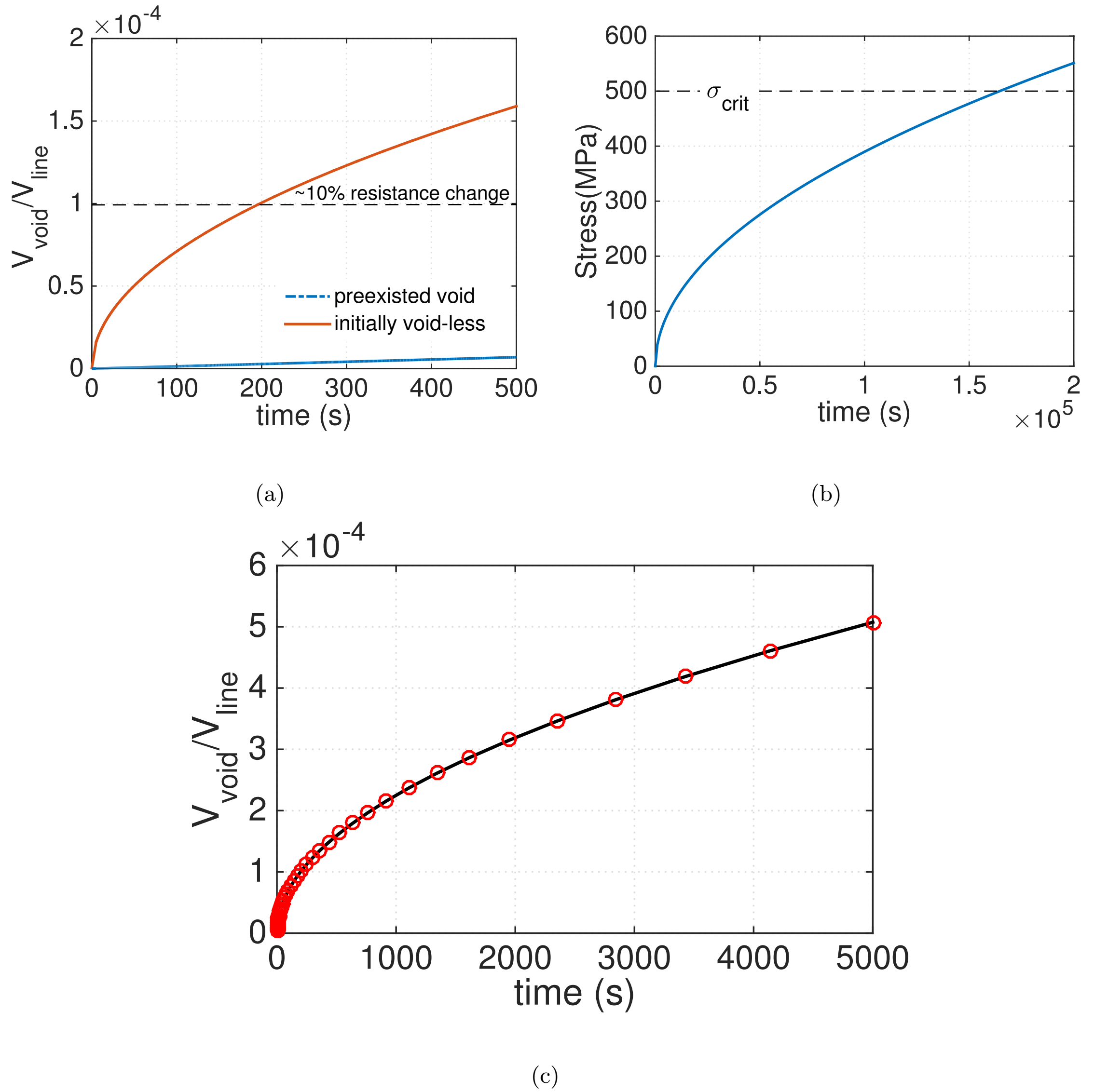


Figure 2.10: Void growth kinetics in the cases of initially void-less line and a line with the preexisted void, (a); and the pre-voiding kinetics of the stress buildup at the cathode end of line, (b); approximation of the initial growth kinetics by the square root time dependence (red dots), (c). For all cases: $j = 1 \cdot 10^{10} A/m^2$, $T = 400K$ and $\sigma_T = 0$.

by the growing void is developed in three order of magnitude shorter time (Fig. 2.10(a)) than the time required for the void nucleation (Fig. 2.10(b)). In the case of a line with the preexisted void, the time consumed by the void growth process to reach 10% resistance increase is about $10^4 s$, is just order of magnitude less the void nucleation time $\sim 10^5 s$. As it

will be discussed in Section V, the former can explain a good fit between the predicted [39], and measured [40], dependences of the current density exponent on the test temperatures, when predictions were done on the basis of calculated void nucleation times.

An independence of the initial EM-induced line resistance change on the current density was observed in experiment; see for example Fig. 12 in the paper by Hu and Rosenberg [34]. The observed absence of significant deviation between the high ($3.6 \cdot 10^{10} A/m^2$) and low ($3 \cdot 10^9 A/m^2$) current density line resistance data was explained by assuming that the line resistance increase is mainly due to penetration of Co from CoWP cap layer into the Cu line and the contribution from EM-induced line damage was small. Our results propose an alternative interpretation of that experimental observation on the basis of void evolution kinetics.

2.7 Tree-based EM analysis method

The proposed physics-based EM assessment models discussed above were attributed to a single confined interconnect line. However, the chip interconnects consist of large interconnect trees as shown in Fig. 2.1. These trees might have multiple voltage inputs/outputs and current source ports represented by inter-layer vias and contacts. The major difference between iso-lines and individual branches of interconnect trees is an absence of blocking boundaries at one or both ends of the branches. It prevents atoms from accumulation/depletion and eliminates related stress buildup at the branch ends, and, hence, makes traditional immortality assessment as a groundless. Fig. 2.11 shows distributions of the current density and hydrostatic stress developed in the three terminal metal segments

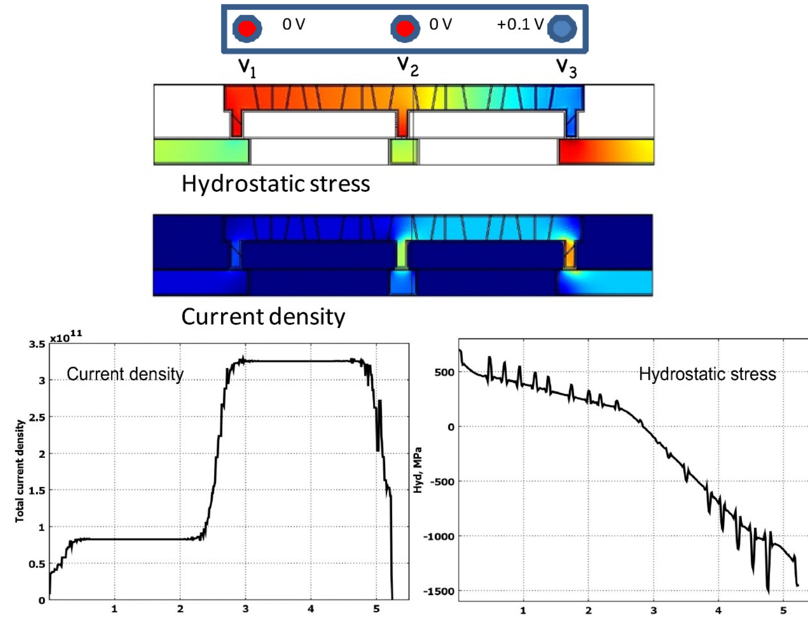


Figure 2.11: Current density and stress distributions in a metal tree

located at the upper metal layer. Two vias are used as electron flow inlets (v_1, v_2) and one positively biased as outlet (v_3). The hydrostatic stress obtained from the solution of the described in Appendix system of PDEs with the FEA tool COMSOL [41] demonstrates the two-slope distribution resulted by the intra branch interaction. It makes clear that in order to explain such distribution we should consider the whole metal tree for stress analysis but not separated single wires [21]. Below we will demonstrate how it affects the developed EM assessment flow.

Let's assume that for a given interconnect tree a distribution of the DC current densities and the current flow directions are known, and the void-less steady state was achieved. We will remove the void-less assumption in the course of development. In this case the steady state means that all atomic fluxes are vanished. It can be reached if the atomic flux in each branch caused by electron flow is balanced by the atomic backflow caused

by stress gradient. It provides a simple estimation of the stresses would be developed at the cathode and anode ends of each branch:

$$\sigma_i^c - \sigma_j^a = \triangle\sigma_{\text{ij}} = \frac{eZ\rho j_{\text{ij}} L_{\text{ij}}}{\Omega} \tag{2.41}$$

Here, σ_i^c and σ_j^a are the hydrostatic stresses at the cathode (electron flow inlet) and anode

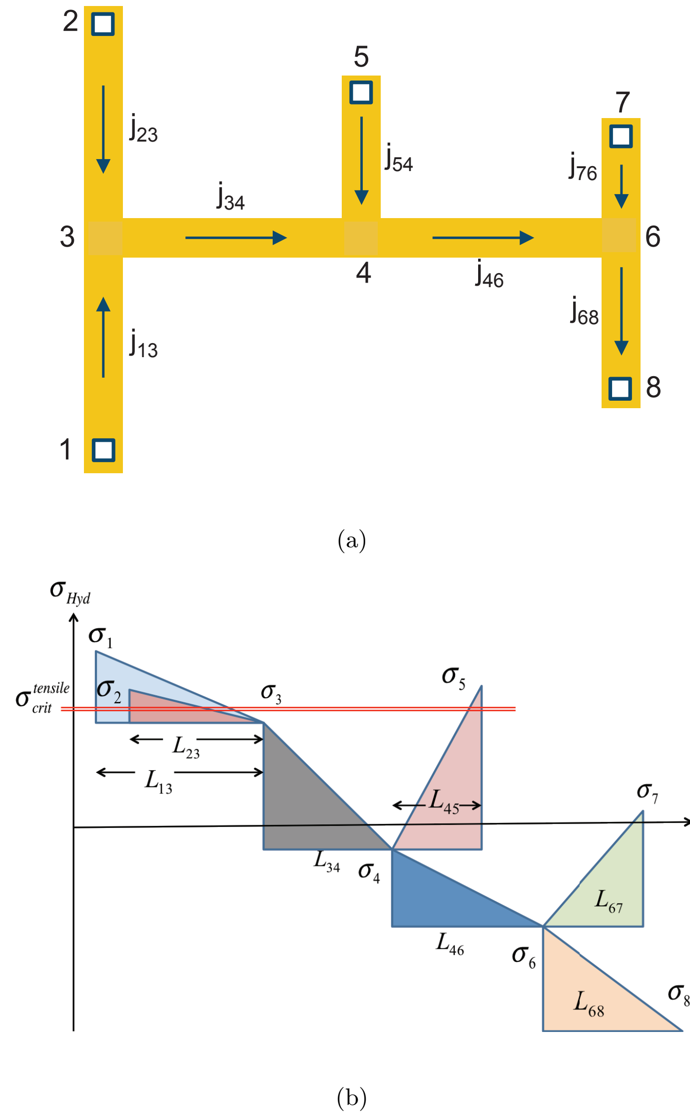


Figure 2.12: (a) Example of an interconnect tree, (b) Hydrostatic stress distribution in the interconnect tree.

(electron flow exit) ends of the ij-branch. Fig. 2.12 shows an example of the multi-branch interconnect tree. Equation (2.41) allows one to obtain the stresses at all branch ends as functions of the "reference" stress developed at any arbitrary chosen end. This uncertainty can be easily eliminated by adding to consideration the atom conservation condition. Indeed, due to unblocked ends of branches the atom redistribution between branches causes the final stress distribution, but keeps the total amount of atoms unchanged. It provides the equation for determination of the missing "reference" stress:

$$\sum_{i=1}^{k} \left[\sigma_i - \left(\sigma_T + \frac{eZ\rho j_{\mathrm{ij}} L_{\mathrm{ij}}}{2\Omega} \right) \right] L_{\mathrm{ij}} = 0 \tag{2.42}$$

Thus, the steady state stress distribution in the interconnect tree shown in Fig. 2.12(a) can be found from the solution of the following matrix equation:

$$\mathbf{M} \begin{bmatrix} \sigma_1 \\ \sigma_2 \\ \sigma_3 \\ \sigma_4 \\ \sigma_5 \\ \sigma_6 \\ \sigma_7 \\ \sigma_8 \end{bmatrix} = \begin{bmatrix} \chi j_{13} L_{13} \\ \chi j_{23} L_{23} \\ \chi j_{34} L_{34} \\ \chi j_{54} L_{54} \\ \chi j_{46} L_{46} \\ \chi j_{76} L_{76} \\ \chi j_{68} L_{68} \\ \Phi \end{bmatrix} \tag{2.43}$$

Where:

$$\mathbf{M} = \begin{bmatrix} 1 & 0 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & -1 \\ L_{13} & L_{23} & L_{34} & L_{54} & L_{46} & L_{76} & L_{68} & 0 \end{bmatrix} \tag{2.44}$$

$$\chi = \frac{eZ\rho}{\Omega}, \Phi = \sum_{i=1}^{7} \left(\sigma_T + \frac{eZ\rho j_{\text{ij}} L_{\text{ij}}}{2\Omega} \right) L_{\text{ij}}$$

Calculated stresses should be compared with the critical stress (σ_{crit}) responsible for the void nucleation. If any calculated stress exceeds σ_{crit} then the time for void nucleation at the cathode, characterized by the biggest stress σ_m, should be calculated as

$$t_{\text{nuc}}^m \approx \frac{L^2_{\text{max/min}}}{2D_0} e^{\frac{E_V + E_{\text{VD}}}{k_B T}} \frac{k_B T}{\Omega B} exp\left\{ -\frac{\Omega^* \sigma_{\text{crit}}}{k_B T} \right\} \times ln \left\{ \frac{\sigma_{m(j_1, j_2, \ldots, j_n)} - \sigma_T}{\sigma_{m(j_1, j_2, \ldots, j_n)} - \sigma_{\text{crit}}} \right\} \tag{2.45}$$

Eq. (2.45) is the extension of the Eq. (2.27) for the case of multi-branch interconnect tree. Here, $\sigma_{m(j_1, j_2, \ldots, j_n)}$ is the steady state stress at the cathode end of a branch characterized by the biggest tensile stress in the considered interconnect tree, and n is the number of branches, $L_{\text{max/min}}$ is the distance inside the tree, which connects the cathode (maximal tensile stress) with anode (maximal compressive or minimal tensile stress). In a case when several cathodes reveal stresses exceeding , the nucleation time still should be calculated for the cathode with the biggest stress. Indeed, the described method for finding the cathode with the steady

state hydrostatic stress exceeding σ_{crit} is just a simple way to find a location inside a tree where the σ_{crit} is first developed. A correct stress distribution inside considered tree at the

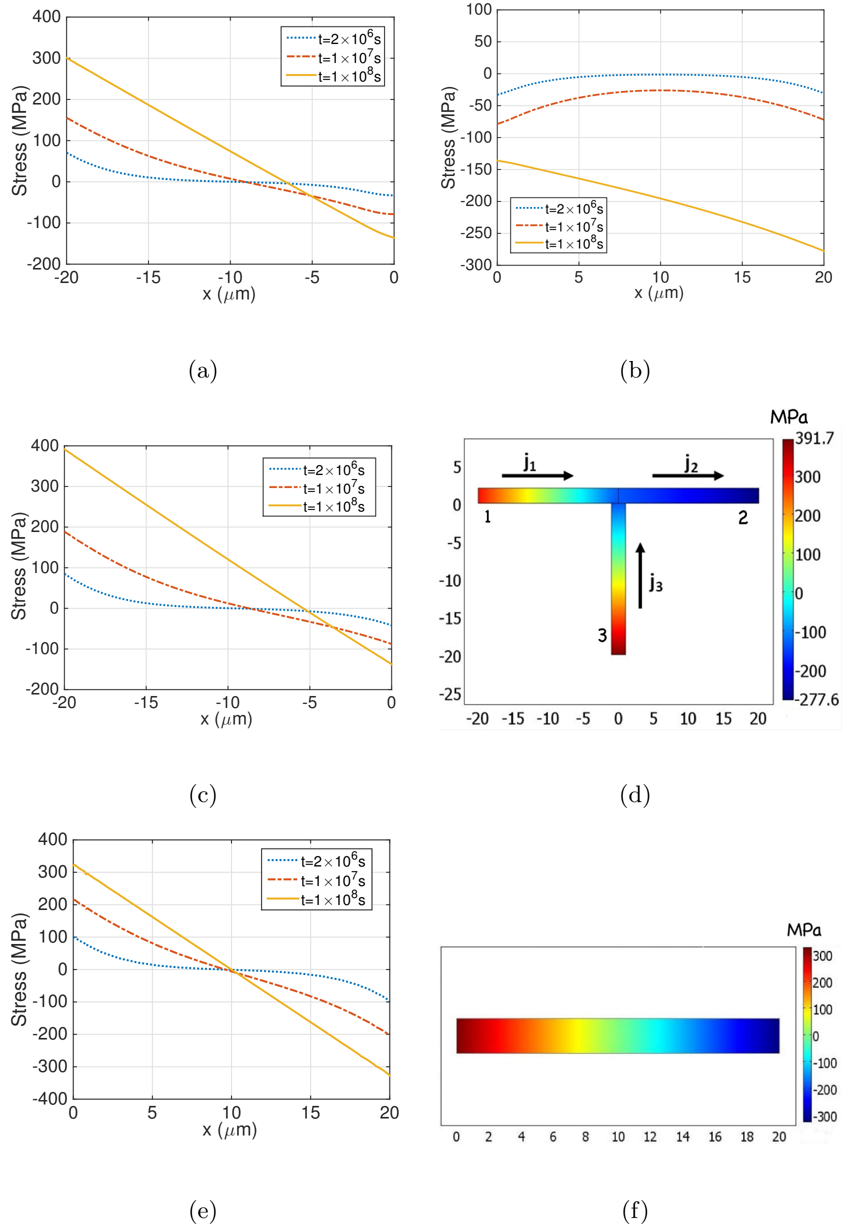


Figure 2.13: Evolution of the stress distribution along the branches: (a) line 1, (b) line 2, and (c) line 3 of the T-shaped tree shown (d). These distributions differ from stress evolution functions (e) in a single line (f).

moment of time when the first void is nucleated, and, which is most important, during the

time when the void evolves, can be derived from the solution of the system of equations, similar to equation (2.25), describing the simultaneous stress evolution in all branches of the tree. Boundary conditions (BC) representing the continuity of stress and the atomic flux conservation at the branch joints should be employed. A zero normal stress BC should be used at the edges of the growing voids. Fig. 2.13 demonstrates evolution of the pre-void stress distributions along the branches of T-shape tree, which was obtained from the solution of stress evolution equations [42, 43]. Analysis of the time-dependent stress distributions in all three branches provides that the largest steady state stress would be developed at the cathode of the branch "3". If we accept, just for illustration purposes, that σ_{crit}=200MPa, then Fig. 2.13(c) shows that indeed a void is nucleated at the branch "3" cathode area at $t_{\text{nuc}} = 1 \times 10^7 s$. The biggest stress in the branch "1" at this time will be 150MPa, which is smaller than σ_{crit}. Starting from this instant in time the stress evolution kinetics will not be described any more by the same dependencies that were valid for $t < t_{\text{nuc}}$. For times $t > t_{\text{nuc}}$ stress evolution inside all branches is described by the same system of equations but with the different BC at the cathode end of the branch "3", which now represents the edge of the growing void, i.e. $\sigma = 0$. Initial condition for the new solution will be the stress distribution at obtained for the void-less case [44].

As it was shown in [44], a nucleated void reduces the stress everywhere inside the interconnect tree. Depending on the current densities in different branches and the pace of atom redistribution through the tree branches, the first nucleated void can either prevent void nucleation in other branches or not. In order to demonstrate these two possible outcomes we have simulated the EM-induced degradation in the multi-branch interconnects

trees (M1-V1-M2-V1-M1) with the commercial FEA tool COMSOL. Full multi-physics system of PDEs described in Appendix was solved. Fig. 2.14 shows an EM-induced failure

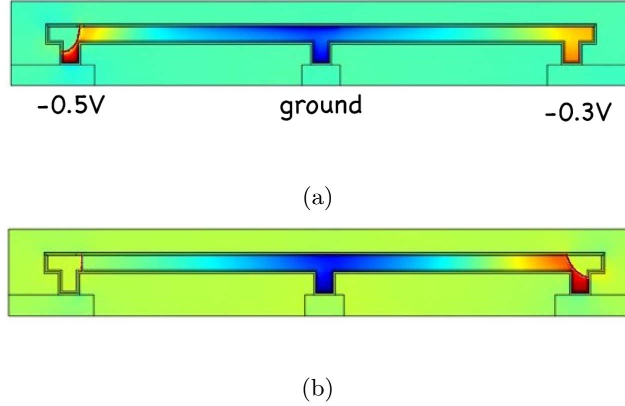


Figure 2.14: Failure of a two-branch tree: (a) voiding of the left branch, while the right branch is immortal due to smaller applied voltages; (b) voiding of the right branch due to current density redistribution after the left segment failed.

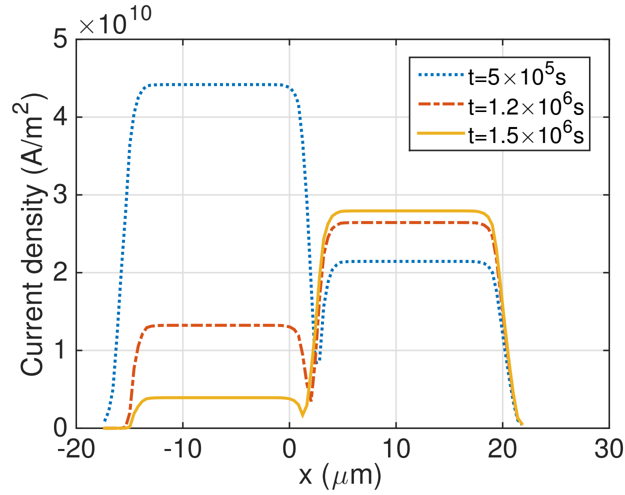


Figure 2.15: Current density redistribution due to left segment voiding in the structure shown in Fig. 2.14

development in two-branch tree. Fig. 2.15 demonstrates the kinetics of void-induced redistribution of the current densities inside interconnect tree shown in Fig. 2.14. Originally, a two-branch test-tree was loaded in a way that the right branch should be immortal, while

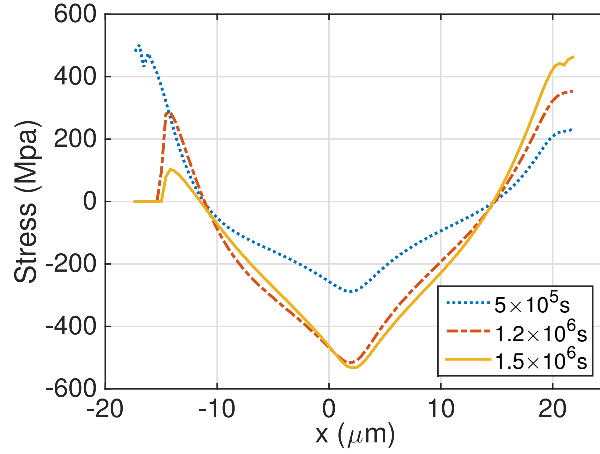


Figure 2.16: Hydrostatic stress evolution caused by the left segment voiding in the structure shown in Fig. 2.14.

the electric current density in the left branch should be able to build up the stress required for voiding. Due to void-induced increase of the resistance of left branch, the current in the right branch increases (Fig. 2.15), causing an increase in tensile stress at the right cathode end. As a result, the void is nucleated in the right branch as well. This process is accompanied by tensile stress reduction in the left branch due to atoms moved from the surface of expanding void to the metal bulk, Fig. 2.16. Thus, an accurate EM model should properly consider the void volume evolution responsible for the evolution of both the current density and stress.

This and similar simulations dealing with different electrical load conditions clearly demonstrate that both cases are possible: (i) first nucleated void prevents nucleation of other voids in the tree, and (ii) multiple voids are nucleated in the tree. For the sake of simplicity, we consider the former case: a nucleated void does not allow stress anywhere to reach the critical level until the current/voltage load is changed. It means that the tensile stress reduction in the void-less branches caused by the migration of atoms from the portion of

the branch occupied by growing void happens faster than the increase due to the action of the electric current passing through these branches. But, the increase in the resistance of the voided branch can cause an increase of the current densities in the void-less branches and can generate the stress exceeding somewhere in the interconnect tree. Thus a new void can be generated. All voids can grow until the saturated volumes (2.31) or (2.32) are developed. Another possible scenario is that all stresses corresponding to the adjusted current densities are smaller than σ_{crit}. In this case, the evolution of the branch resistance will stop upon development of the $V_{\text{SS}}^{\text{volm}}$. However, this state will last not long. Due to electrical interconnectivity of all trees the resistivity change in any of these trees caused by voiding will cause the change of the current densities in all neighboring trees, which will change the volume of the saturated voids, and the resistances of the corresponding branches. This interconnect tree-based stress analysis method is further applied in chip-scale EM assessment which is discussed in the next chapter.

2.8 Summary

In this chapter, we present the physics-based EM modeling for VLSI circuits. In order to provide an additional support to the obtained analytical results, we first perform the numerial analysis of stress and void evolution in a metal line, which models redistribution of metal lattice vacancies taking place under electric stressing with accounted equilibration of local vacancy concentration with stress. The proposed analytical EM models account the statistical nature of the EM phenomenon due to a random grain size distribution. It can also account the thermal and other process-induced residual stresses, which have been

ignored by the Black's equation based EM assessment. Void nucleation and growth are considered for assessing the resistance growth. We present the results of the analytical solution to the continuity equation describing both the pre-voiding and the post-voiding stress evolution kinetics in the confined metal line. Based on which, the approximate value of void nucleation time from the pre-voiding stress evolution equation is extracted, which can be further applied in the circuit/system level EM checking. Contrary to the known kinetics of the void growth caused by the electric current-induced evolution of the preexisted void, the initial growth kinetics of the current nucleated void does not depend on the current density. In order to consider the complex structures for practical on-chip interconnects, we have developed a technique that allows to assess the evolution of hydrostatic stress inside a multi-branch interconnect tree for more accurate prediction of the TTF in comparison with the traditional Blech-Black analysis of individual branches of the interconnect tree.

Chapter 3

Electromigration Assessment for Power Grid Networks

Electromigration-induced reliability threats is more severe for power delivery networks as they experience large unidirectional currents and thus are more susceptible to EM effects than signal circuits characterized by bidirectional currents. We propose a novel approach and techniques for physics-based EM assessment in power delivery networks of VLSI systems, which is based on the developed physics-based EM models in Chapter 2 and the EM-induced IR-drop degradation criterion that replaces the traditional conservative weakest segment method. Since both the temperature, which affects atom diffusivity, and the residual stress existing in each metal line before applying the electrical load are responsible for both void nucleation and growth, their distribution should be considered for accurate chip-scale EM assessment. Thus in the improved approach, we characterize the cross-layout temperature and thermal stress distributions by compact modeling and

consider their impact on EM through physics-based EM models.

3.1 Introduction

A physical meaning of the void-induced failure is an increase of the resistance of an individual line. Increase in the resistance above some critical value, for instance, 10% of the initial line resistance is considered as an EM-induced failure. In the traditional EM checking approaches the EM-induced failure rates of the individual branch are considered as a measure of EM-induced reliability and, in the extreme end, a MTTF of the weakest branch is accepted as a measure for the chip lifetime. It results in a very conservative design rule for the current densities that can be used in the chip design for a particular technology node in order to avoid EM failure. A very different way to EM assessment can be proposed from the positions of interconnect functionality, when the failure means its inability to function properly. There are two most important functions of the chip interconnect, which are: providing a connectivity between different parts of design for a proper signal propagating, and delivering a needed amount of voltage where it is required. While cutting-off the individual branches of the interconnect circuits can degrade both functions, the role of EM is quite different in these two cases of degrading the power supply chain and the signal circuits. The difference is in the types of electric currents employed in these two cases. Indeed, the signal lines carrying bidirectional pulse currents are characterized by very long times to the EM-induced failure. It is caused by a repetitive increase and decrease of the mechanical stress at the branch ends, caused by the excessive atom accumulation and depletion due to interaction with the electron flow. In contrast, power lines carrying unidirectional currents

can fail in much shorter time due to continuous stress buildup under the EM action. Thus, we can conclude that EM-induced chip failure is happening mostly when interconnect cannot deliver needed voltage to any gate of the circuitry. It means that loss of performance, which is a parametric failure, should be considered as the practical criterion of EM-induced failure. It is clear that a structure of the power grid, which is characterized by high level of redundancy, can affect the kinetics of failure development. Indeed, due to redundancy the failure of some of interconnect branches does not necessary result in a critical IR-drop on the grid causing an electrical malfunction [45,46]. Thus, more accurate and less pessimistic full-chip EM assessment and MTTF prediction will require development of new methods that deal with the grid structure and take redundancy into account.

EM effect on a metal wire is governed by a combination effect of current density, local temperature and residual stress, as shown in [3,20,39,47]. The rapid increase in chip power dissipation and power density results in thermal hot spots and temperature gradients on the die. Thermal stress is a major source of the residual stress, which is mainly due to the significant mismatch in the coefficients of thermal expansion of the metal and the silicon surrounding it. Therefore in order to accurately estimate the risk of EM-induced failure, the full-chip EM assessment methodology should not only account for the current densities but also consider the temperatures and residual stresses in different interconnect segments for different workloads. There have been many prior works focusing on EM analysis techniques under various scenarios. However, unfortunately, most of the published results were obtained under the assumption of uniformly distributed temperature and/or uniformly distributed residual stress across the chip [20,45,46,48]. These results will be not accurate

enough to characterize the kinetics of void nucleation and void volume evolution responsible for EM-induced degradation and, hence, result in ineffective reliability optimization techniques.

In this chapter, we to mitigate the mentioned problems for full-chip EM assessment and signoff techniques. We propose a novel approach and techniques for physics-based EM assessment in power delivery networks of chips. The new approach consists of the following contributions: (i) Instead of considering the failure of a single interconnect branch, we consider the failure criterion as the increase in the voltage drop above the threshold level, caused by the EM-induced resistance increase of the individual branches. The new approach takes full account of essential redundancy for current delivery existing in the power-ground (P/G) networks. (ii) The EM assessment method for P/G networks applies the new method to calculate the EM-induced resistance increase of the individual branches in terms of the developed physics-based formalism for void nucleation and growth. (iii) The new method employs the tree-based method for calculating the hydrostatic stress evolution inside a multi-branch interconnect tree and calculates the void nucleation times in the group of branches comprising the interconnect tree. It allows to avoid over optimistic prediction of the TTF made with the Black-Blech analysis of individual branches of an interconnect tree. (iv) We model the resulting P/G networks as time-varying linear networks, which was solved in the EM-time scale to estimate the time-varying voltage drops of P/G networks due to the EM effects over time and the resulting full-chip EM failure time. (v) We further characterize the power dissipation in devices and Joule heating in the interconnects. And next, we estimate the full chip temperature and thermal stress distributions by compact

modeling and account them in the flow of EM-reliability assessment of the power grids.

The reminder of the chapter is organized as follows: Section 3.2 describes the new power grid EM reliability analysis method based on the developed physics-based void nucleation time model and voiding-induced resistance change model. Section 3.4 and Section 3.5 present the enhanced power grid reliability analysis method that considers the with-in die temperature and thermal stress distributions based on the physics-based EM models. Section 3.6 concludes the chapter.

3.2 New power grid reliability analysis method

In this section, we present the proposed new power grid reliability analysis method using the nucleation and growth concepts and physics-based EM models we discussed in the previous sections.

3.2.1 Power grid models

Because of the concern with the long-term average effects of the current, in EM related work a DC model of the power grid is generally assumed [45]. As a result, we need to consider only the EM-induced kinetics of the power grid network resistances. For the transient current sources, we will show how to compute the effective EM current and EM current sources later. In our problem formulation, each mortal wire, which is the subject to the EM impact, will start to change its resistance value upon achieving the nucleation time. As a result, we end up with the power grid systems, which is a linear, time-varying

and driven by the DC effective currents. For a power grid network with n nodes,

$$G(t) \times v(t) = I(t) \tag{3.1}$$

where $G(t)$ is a $n \times n$ time-varying conductance matrix; $I(t)$ is transient current source vector; $v(t)$ is the corresponding vector of nodal voltages. In our problem, the time scale is the EM time scale, which can be months or years.

3.2.2 Effective-EM current density

EM is a long-term cumulative failure phenomenon. In reality the P/G nets are characterized by the time-dependent current densities. Small background DC currents distributed across the grid are perturbed with the unipolar pulses generated by switching cells. An intensity of these perturbations depends on the activity factors of standard cells, which are different for different workloads. In general, total current passing between the neighbor power vias is a unidirectional pulsed current. Unidirectional current and the long length of the power net segments can provide the conditions for σ_{crit} accumulation. In this case, the criterion for determination of the effective DC current should be established, [49]. The effective-EM currents will give the same lifetime as the transient waveforms. It can be understood from the following. Equation (2.25) provides the kinetics of the hydrostatic stress in the interconnect line caused by applied current. A simple integration provides:

$$\sigma(t,x) - \sigma_0 = \frac{\partial}{\partial x}\left[\int_0^t \kappa \frac{\partial \sigma}{\partial x} dt + \kappa \frac{eZ\rho}{\Omega} \int_0^t j dt\right] \tag{3.2}$$

It means that under assumptions made for derivation of the equation (2.25) in [30], the stress distribution at any particular instant in time is governed by the time integral of the applied current density. This can be used as a justification of the replacing the current

density waveforms with the time averaged DC current density. For most general cases of both uni-directional and bi-directional current densities, we have the following effective-EM current density [49,50]:

$$j_{\text{trans, EM, eff}} = \frac{1}{P}\left[\int_0^P j^+(t)dt - R\int_0^P |j^-(t)|dt\right] \quad (3.3)$$

where $j^+(t)$ and $j^-(t)$ are the current densities of the positive and negative phases of the bipolar current, R is the EM recovery factor determined by experiments, P is the period of the current density waveform. When the current density is unidirectional, the effective-EM current density $j_{\text{trans,EM,eff}}$ is the time averaged current density. Furthermore, if the current sources are time dependent, we can compute the effective EM current sources in a similar way, which will generate the same effective current densities in each interconnect tree so that only one DC analysis is required for EM analysis at each EM time point.

3.2.3 New analysis method flow

Now we present the new EM-induced reliability analysis algorithm and flow for P/G networks. In our formulation of the dynamic P/G networks, the wire resistance begins to change (increase) starting with the nucleation time (t_{nuc}). After this, their resistance changes will be computed by Eq. (2.30). First we compute initial current densities $j_{0,\text{mn}}$ for each branch of every tree. Then, by using the proposed tree-based EM analysis method, we obtain the stresses for all branches in all trees. Next, we identify the trees, which are the subjects for void nucleation: hydrostatic stress at any of the tree nodes is larger than σ_{crit}. Then, we compute the set of t^i_{nuc} for all suspicious branches. Branch characterized by the largest stress and smallest t_{nuc} among others sets up the initial (starting) time t_0,

which is indicated by $t_0 = min\{t^i_{\text{nuc}}\}$ in the step 4 in the algorithm, and the branch will be included in the growth phase pool. After this, we move to next step $t_1 = t_0 + \Delta t$. The chosen time-step Δt should be small enough to detect approximately an instant in time when the critical stress is developed in any branch of any interconnect tree. We update power grid conductance matrix G due to resistance change in the wire in the growth phase, re-compute current densities j for each wire of each tree again, and then repeat the previous steps: stress calculation, identification of the branches satisfying $\sigma > \sigma_{\text{crit}}$, putting the most vulnerable branch into growth phase pool if reaches its t_{nuc}, and moving to the next step: $t_2 = t_1 + \Delta t$. We continue this process until the IR-drops at one or more nodes reach the given threshold such as 10% of the supply voltage. We identify this instant in time as the TTF of the whole P/G network. It is worth noting that, in the step 7 in the algorithm, we consider the generation of the void saturated volume when updating the branch resistance. For each branch in the growth phase, we first obtain its void volume saturation time t_{VS}. Then we compare t_{VS} with last instant in time $t_{\text{i-1}}$. Only the branches in the growth phase pool with $t_{\text{VS}} > t_{\text{i-1}}$ have resistance increase during $[t_{\text{i-1}}, t_{\text{VS}}]$.

Algorithm 1 New power grid EM-induced reliability analysis algorithm

Input: power grid networks with current inputs, time step, and technology parameters

Output: The time reaching the threshold IR-drop and failed branches.

1: Compute the initial effective EM current density.

2: Divide the power grids into interconnect trees with a number of connected branches.

3: Compute the steady state distributions of hydrostatic stress inside each interconnect tree.

4: Conclude all suspicious branches whose tensile stress is larger than critical stress. Calculate the nucleation time $t_0 = min\left\{t^i_{\text{nuc}}\right\}$ for the most vulnerable branch(with the largest stress).

5: Start the analysis from time $t = t_0$. Branch with nucleation time t_0 enters into the growth phase.

6: **while** the largest IR-drop $\leq$ threshold **do**

7: Move to next instant in time $t := t + \Delta t$, update the wire resistances for wires with void volume increase.

8: Perform the DC analysis of the power grids. Recompute the current densities of each branch.

9: Compute the steady state distributions of hydrostatic stress inside each branch based on the updated EM current densities.

10: For each tree, identify new branches with the stresses exceeding the critical value. Calculate the $min\left\{t^i_{\text{nuc}}\right\}$ for suspicious branches in the nucleation phase. If $min\left\{t^i_{\text{nuc}}\right\} \leq t$, the corresponding branch steps into the growth phase.

11: **end while**

12: Output t and the failed branch

3.3 Numerical results and discussions

The proposed EM assessment method is implemented in C++ on a 2.3GHz Linux server with 132GB memory and validated by the IBM power grid benchmark circuits [51], which has both power networks and ground networks. The power networks are used to test our method and their source current values are modified to ensure that the initial IR-drop of any node is smaller than the threshold value. In this work, we assume the interconnect material is copper and the power grid circuit fails when the largest IR-drop exceeds $10\%V_{\text{DD}}$. Parameters used in our model are listed in Table 3.1.

Table 3.2 shows the power grid lifetime obtained from both Black's equation

Table 3.1: Parameters used in proposed model

Parameter	Value	Parameter	Value
E_V	0.75eV	T	373K
E_{VD}	0.65eV	σ_T	400MPa
T_{ZS}	623K	Z	10
B	1×10^{11}Pa	σ_{crit}	500MPa

Table 3.2: Comparison of power grid MTTF using Black's equation and proposed model

Power Grid		Time to Failure (yrs)				
		Black's Equation		Proposed Model		
Name	Nodes	Series	Mesh	no void sat	with void sat	Run Time
IBMPG2	61797	6.17	12.83	16.85	18.78	6.36 min.
IBMPG3	407279	12.79	17.90	23.56	31.97	5.83 hr.
IBMPG4	474836	13.23	22.27	26.97	33.41	14.71 hr.
IBMPG5	497658	4.41	12.34	19.13	25.16	40.64 min.
IBMPG6	807825	8.44	10.89	14.62	19.85	1.75 hr.
IBMPGNEW1	715022	12.85	13.96	18.84	25.97	16.78 hr.
IBMPGNEW2	715022	12.73	13.84	15.60	21.79	15.32 hr.

and our proposed approach. In Black's equation based analysis, equation (2.2) is used to estimate the MTTF of single metal line, where $T_{\text{stress}} = 600K$, $j_{\text{stress}} = 3MA/cm^2$, $Ea = 0.86eV$ and $MTTF_{\text{stress}}$ is obtained from equation (2.27) under stressed condition (use condition characteristics are the same as characteristics used in our predictive work). The current density exponent n is taken as 2 when failure is nucleation dominated and is taken as 1 when failure is nucleation dominated. Two different Black's equation based

models are used to compare with the proposed method. One is series model, under which the circuit is considered to have failed as soon as any branch fails. The other is mesh model that takes redundancy into account, defining the circuit fails when it cannot deliver required amount of voltage. From the experimental results, we can observe that the Black's equation based series model would lead to a too pessimistic prediction. The TTF estimated by Black's equation based mesh model is more conservative than our model because it assumes infinite resistance after the predicted TTF of each branch while actually the metal line continues to conduct voltage after TTF with increasing resistance. Fig. 3.1(a) and Fig. 3.1(b) shows the steady state hydrostatic stress distribution predicted by the initial current density, and the initial IR-drop distribution in the metal layer that directly connects to the underlying logic blocks respectively.

The locations of voids nucleated during the lifetime of the circuit are demonstrated in Fig. 3.2(a). We can observe from Fig. 3.1(a) and Fig. 3.2(b) that with uniformly distributed temperature, the failure is most likely to happen at the place where the hydrostatic stress predicted by the initial current density is large. It is due to the fact that the branches with larger stress are more likely to nucleate void and, since the void growth rate is almost independent on stress, and a larger stress would result in a larger void saturated volume, which means larger resistance change, the IR-drops at these places will more likely to exceed the threshold value.

We also implemented the assessment method, which assumes that the void keeps growing once it is nucleated. Fig. 3.3(a) and Fig. 3.3(b) are the experimental results obtained from the model in which the void volume saturation is not considered. The distribu-

tion of the voids in the p/g net and the distribution of IR-drops in the first metal layer at the instant in time the circuit fails are depicted respectively. It is observed that when the void saturated volume is taken into account, the more voids are distributed in the circuit when compared to the distribution where the voids keep growing upon nucleation. Table 3.2 summarizes the comparison between TTF obtained when considering and neglecting void volume saturation. We can conclude that for the same circuit, introducing void volume saturation would result in a larger number of nucleated voids, thus a larger number of branches in the circuit whose resistance have changed due to EM effect, but a longer TTF. It is due to the fact that when the void volume saturation has been considered, a void would stop growing when its volume reaches the saturation state. It starts growing again only when the current passing this branch increases due to voids generated in neighbor branches/trees. Thus the overall change of branch resistance is slower than in the case of neglected void volume saturation, more time and more voids will be needed for the circuit to meet the same failure criteria. So accounting for the void volume saturation in the EM analysis is necessary in order to get precise circuit lifetime.

Node voltage keeps changing with time after creation of the first void in the network and its value can be tracked as shown in Fig. 3.4. Effect of different average chip temperatures on P/G network's TTF is investigated. From Fig. 3.5, the experimental result reveals that TTF obtained from our proposed method obeys the same functional dependencies as the Black's equation, which is the Arrhenius dependence on temperature. So reducing the temperature can efficiently suppress the EM effect.

3.4 Cross-layout temperature and thermal stress characterization

Table 3.3: Geometry of power grid interconnects (μm)

Layer	contact	M1	V1	M2	V2	M3	V3	M4	V4	M5	V5	M6	V6	M7
Layer Number	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Width	-	0.066	-	0.066	-	0.2	-	0.2	-	0.36	-	6	-	6
Thickness	0.2	0.12	0.12	0.12	0.12	0.12	0.12	0.12	0.12	0.12	0.6	0.9	0.9	0.9

Layer1: Si-substrate; Layer2: device layer;

This section describes the estimation of within-die temperature and thermal stress distribution. We demonstrate the characterization of power dissipation in the devices and the Joule heating in interconnects, then, we detail the temperature simulation methodology, which builds a thermal netlist with the effective thermal properties. Further, the thermal stress variation across the layout will be obtained based on the temperature distribution. A 32nm test-chip is used as the case example to present the flow. Standard-cells are used in this design along with 7 metal (copper) layers. Fig. 3.6 shows the layout of this design with dimension $184\mu m \times 184\mu m$. There are 16 layers in total (the Si-layer is divided into a thin Si-device layer that includes power dissipation and a thick Si-substrate layer for thermal analysis purpose). The BEOL (Back-End-of-Line) geometry information is described in Table 3.3.

3.4.1 Full-chip power characterization

Power estimation is a challenging task since the result is highly dependent on the workload or typical usage of a chip. We consider both the power dissipation in the devices and Joule heating in interconnects. The chip power consists of static and dynamic components. Eq. (3.4) is the power model for each individual primitive block, where a block is considered to be a primitive if it cannot be further decomposed into smaller blocks based on an user settings. The dynamic power comes from the gate switching, in which the block dissipates power by charging the load capacitances of wires and gates and dissipates power during a very short period of time when a conduction path exists between the power and ground voltage connections. Thus, more active block is characterized by the higher dynamic power. In contrast, the static power is due to static current, including the leakage current and presents regardless of a block's activity level.

$$P_{\text{block}} = P_{\text{static}} + \alpha_{\text{switching}} \times P_{\text{dynamic}} \tag{3.4}$$

Here, P_{static} and P_{dynamic} are the static and dynamic powers of a block, $\alpha_{\text{switching}}$ is the switching estimate for signals that describes the switching activity of the block.

For time varying currents, the time scale is on the order of picosecond, which is too fine for the thermal time scale. As a result, power averaging is further applied to obtain the power consumption in the device layer. The current flowing through interconnects generates Joule heating. Similar to Eq. (3.4), we estimate the Joule heating in a wire by evaluating both static and dynamic components of generated heat. Fig. 3.7(a) is the power map for the device layer. We selectively show the Joule heating in M1, M3 and M6 layers in Fig. 3.7(b)–Fig. 3.7(d).

3.4.2 Thermal simulation methodology

Since the temperature affects atom diffusivity, the EM assessment requires accurate local temperature estimation at each interconnect layer in order to adequately account for the temperature-sensitive void nucleation and growth kinetics. In this section, we describe a thermal analysis flow that efficiently estimates the cross-die temperature variation by employing a compact thermal model that represents a die as arrays of cuboidal thermal cells with effective local thermal properties. The methodology includes three steps: (i) extract effective thermal properties of a thermal cell in a layer, (ii) generate thermal netlist of the whole chip, and (iii) calculate temperature at each thermal node by a circuit solver, see for example [52, 53]. As shown in Fig. 3.8, all considered composite layers are divided into a set of thermal cells defined by a layer thickness and a square window of size L which is chosen based on the simulation accuracy: the finer partitioning provides more accurate results at the expense of the run time. Each cell contains 6 thermal resistors representing heat propagation in the lateral and vertical directions; a thermal capacitance can be included for transient thermal analysis.

The effective thermal conductivities are functions of metal density and routing direction of wires in each metal layer based on the theory of effective thermal properties of anisotropic composite materials [54]. Based on the standard procedure [52, 53], with the extracted thermal resistances e.g. Fig. 3.9, estimated power sources, as well as the thermal boundary conditions, the chip can be represented as a thermal netlist, in which the nodal temperatures correspond to the nodal voltages and the powers corresponds to the currents. The electric circuit solver can then obtain temperature for each thermal node.

In the thermal simulation, performed in the analyzed design, a window size $L = 5\mu$m was chosen for computational efficiency while keeping reasonable temperature resolution. The top surface of the die was kept at T=330K, while all other sides were insulated. As shown in Fig. 3.10, the temperature varies across different layers. The temperature distribution in M1 interconnects is shown in Fig. 3.11.

3.4.3 Thermal stress estimation

Since the residual stress existing in each metal line before the electrical load is applied is responsible for both void nucleation and growth, its distribution should be considered for accurate chip-scale EM assessment. This work focuses on the thermal stress, which is a major source of the residual stress. In the case of metal line embedded into the rigid confinement, which, in the analyzed case of the on-chip interconnect, is comprised by refractive metal and dielectric diffusion barriers and ILD/IMD dielectrics, the initial stress is generated during the system cooling from the stress-free annealing temperature T_{ZS} down to the use temperature T. A primary source of this thermal stress is the difference in the coefficients of thermal expansion of the metal α_{M} and confinement α_{conf}, which is mainly determined by the silicon substrate:

$$\sigma_T = B(\alpha_{\mathrm{M}} - \alpha_{\mathrm{conf}})(T_{\mathrm{ZS}} - T) \tag{3.5}$$

The thermal stress distribution in the M1 layer is demonstrated in Fig. 3.12. Since a lower thermal stress corresponds to a higher layout temperature due to the smaller temperature gap $\Delta T = T_{\mathrm{ZS}} - T$, the regions with the highest T, Fig. 3.11, are characterized by the smallest σ_T, Fig. 3.12. Note that more accurate thermal stress estimation should consider

the elastic portion of the stress generated by interaction with confinement. This is reserved for the future analysis. Nevertheless, the calculated inelastic fraction of the thermal stress demonstrates well the trend caused by the thermal stress variation and its relation to the temperature distribution.

3.5 Impact of across-layout temperature and thermal stress on EM

3.5.1 Full-chip EM analysis flow

Now we present the new EM-induced reliability analysis flow flow for P/G networks of the 32nm test-chip, which accounts for the impacts of within-die temperature and thermal stress variations. The new Algorithm 2 is similar to Algorithm 1 stated in Sec. 3.2. But it first performs thermal analysis and mapped the temperature and thermal stress values to the P/G network interconnects before performing the EM assessment. Thus, different from the uniformly distributed temperature case, the minimum t_{nuc} here is determined by both the hydrostatic stress and the local temperature instead of the maximum hydrostatic stress only. The full-chip EM assessment is achieved through the following steps:

- **IP block modeling and power grid network extraction:** Model IP block's interaction with the P/G nets through pre-defined connections (pin locations) under various conditions (e.g. input slew and output loading capacitance): run circuit simulations of the transistor netlist annotated with the layout parasitic information; estimate block's activity based on realistic circuit behaviors, such as the percentage

of design switching within a clock cycle. Assuming that each standard cell used in this design has a power (V_{DD}) pin and a ground (V_{SS}) pin associated with the power grids, we extract the P/G networks as parasitic circuits with each P/G pin modeled as a DC current source: $I_{\text{DC}} = I_{\text{leakage}} + \alpha_{\text{switching}} I_{\text{ON}}$.

- **Cross-layout temperature and thermal stress characterization:** First, we characterize power dissipation in devices and Joule heating in interconnects by Eq. (3.4). Then, upon dividing each layer into multi thermal cells the local effective thermal properties are computed. The die is further modeled as an equivalent thermal circuit, where the power is represented as current and the temperature is denoted by voltage. We solve the thermal net and get the temperature distribution across the die. Further, the thermal stress distribution can be obtained based on Eq. (3.5). Finally, we map the temperatures and the thermal stresses into the layout.

- **Full-chip EM analysis considering within-die temperature and thermal stress distributions:** Each of the interconnect branches is now assigned a local temperature and a local thermal stress, replacing the average values used in the traditional EM analysis. In the formulation of the dynamic P/G networks, the hydrostatic stress is analyzed in interconnect trees; the wire resistance begins to change (increase) starting with the nucleation time (t_{nuc}), calculated by Eq. (2.27), and later their resistance changes are estimated by Eq. (2.30). The generation of void saturated volume should be checked before updating the resistance. As indicated in step7 in Algorithm1, the P/G network starts to degrade after the first void have nucleated at $t = \min\{t^i_{\text{nuc}}\}$, which is characterized by both hydrostatic stress and temperature. Then at each in-

stant in time $t := t + \Delta t$, we update resistance of all branches with non-saturated voids; recalculate current density and hydrostatic stress; and check if there are any new voids nucleated during the previous time increment Δt. The chosen time-step Δt should be small enough to detect approximately an instant in time when the critical stress is developed in any branch of any tree. We continue the process until the IR drops at one or more nodes reaches the given threshold, for example, $10\% V_{\mathrm{DD}}$ or when the time instant has reached the required life-time (LT_{REQ}).

Algorithm 2 New power grid EM-induced reliability analysis algorithm considering cross-layout temperature and thermal stress variations

Input: layout design files, required chip LT (LT_{REQ}), chip failure criteria, time step (Δt)

Output: TTF and failed segment (if $TTF < LT_{\mathrm{REQ}}$), largest IR drop, void locations

1: IP block power modeling and P/G network extraction.

2: Chip power consumption and interconnect Joule heating estimation.

3: Thermal analysis: obtain within-die temperature and thermal stress distribution. Apply results in following full-chip EM assessment.

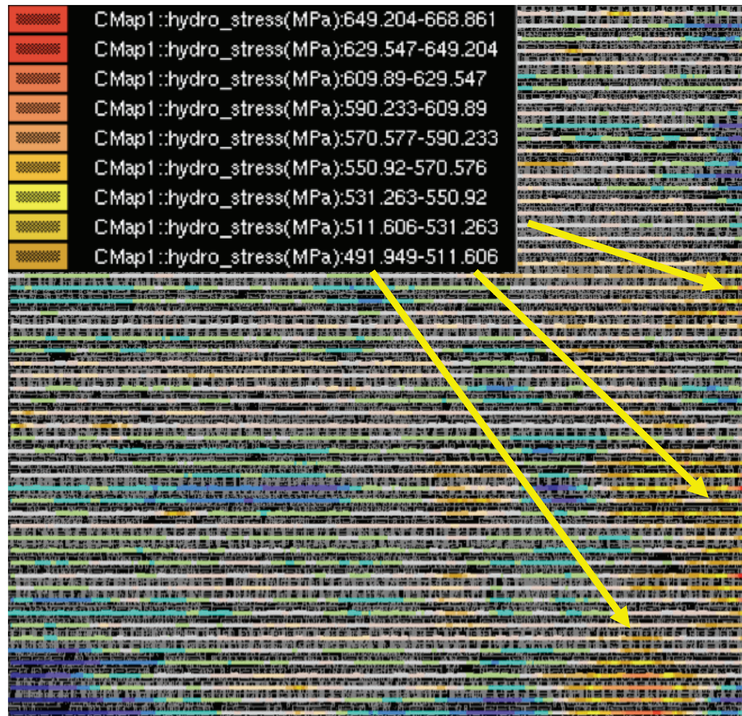
4:

5: Divide the P/G nets into a set of interconnect trees.

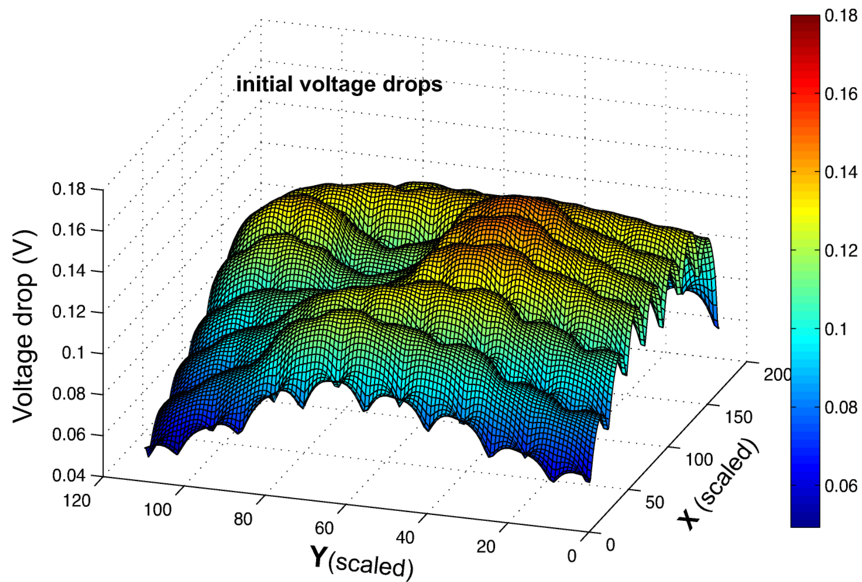
6: Calculate the initial effective EM current density for each branch and compute the steady state distributions of hydrostatic stress inside each interconnect tree.

7: Find all suspicious branches with the tensile stress larger than the critical value. Find nucleation time for the first void ($t_0 = \min\{t^i_{\mathrm{nuc}}\}$).

8: Start the analysis from time $t = t_0$. Branch with the first nucleated void enters the growth phase.

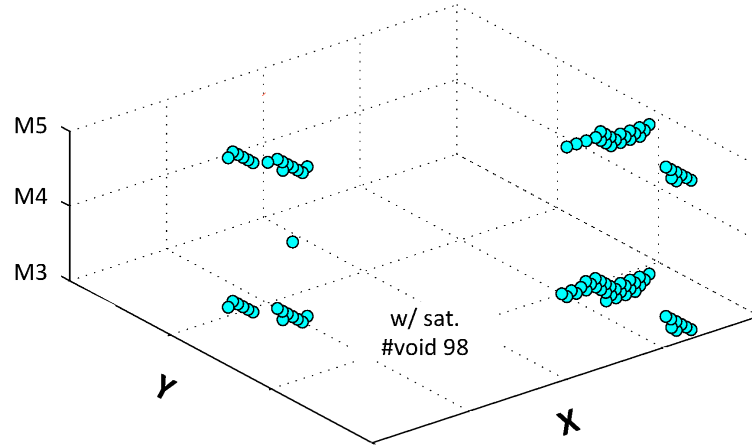


(a)

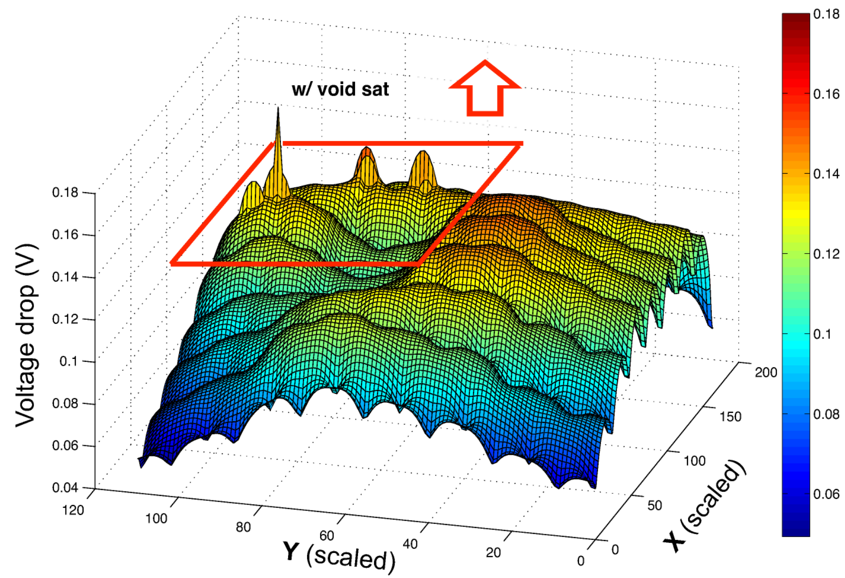


(b)

Figure 3.1: (a) Steady state hydrostatic stress (Pa) distribution predicted by the initial current densities and (b) initial IR-drop (V) distribution, in the layer that directly connects to circuits (M3) of IBMPG2.

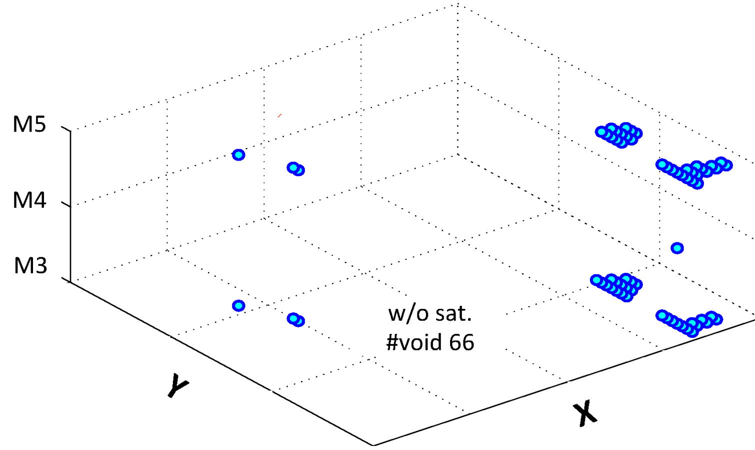


(a)

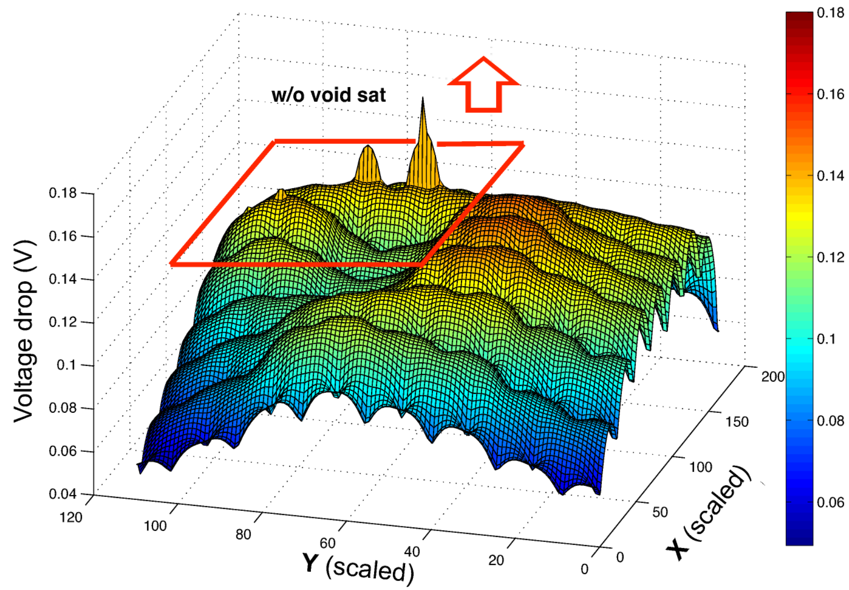


(b)

Figure 3.2: Void distribution,(a), and the IR-drop (V) distribution in the layer that directly connects to circuits (M3),(b), of IBMPG2 at t=TTF. Void volume saturation is taken into account.



(a)



(b)

Figure 3.3: Void distribution,(a), and the IR-drop (V) distribution in the layer that is directly connected to circuit (M3),(b), of IBMPG2 at t=TTF. Void volume saturation is not considered.

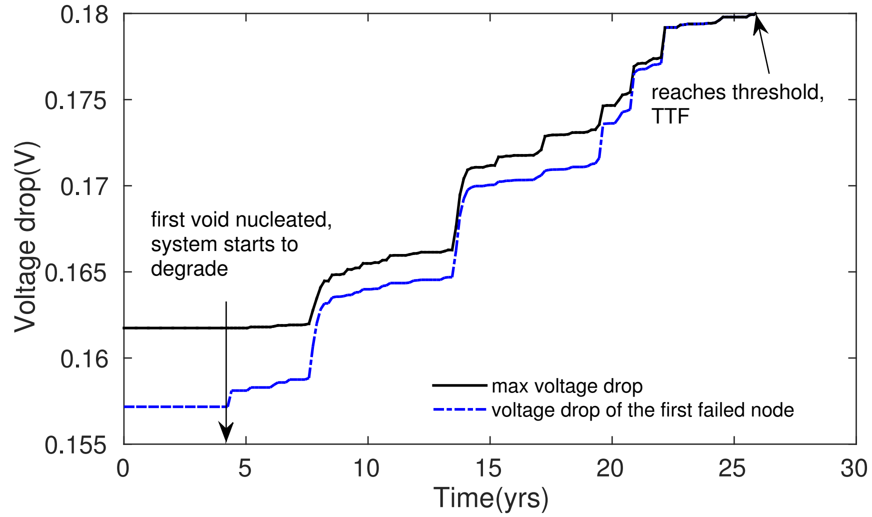


Figure 3.4: Voltage drop of the first failed node and maximum IR-drop in IBMPGNEW1 change over time.

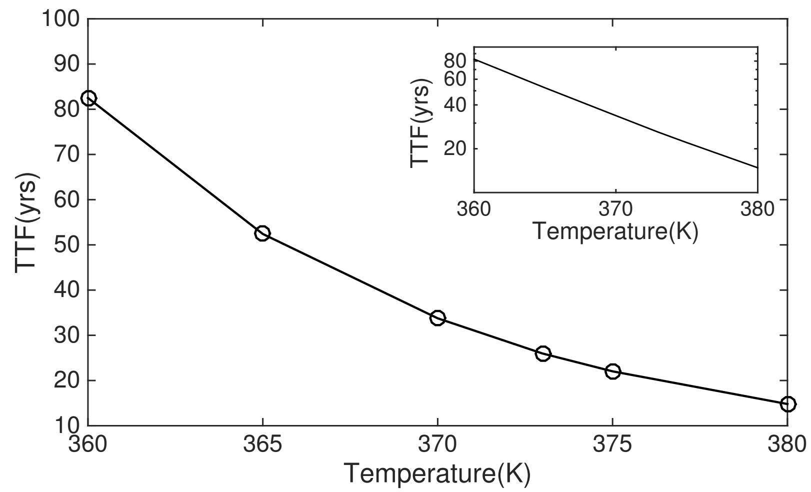


Figure 3.5: Effect of temperature on TTF.

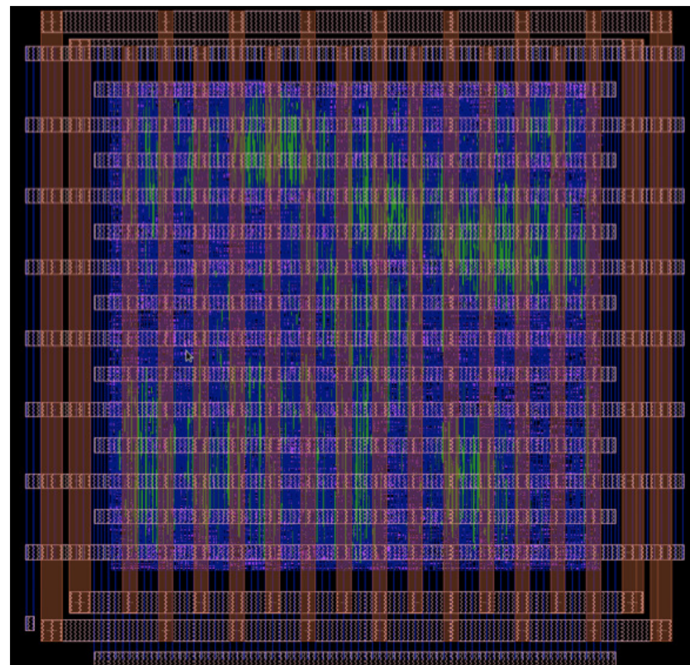


Figure 3.6: Layout of 32nm test-chip

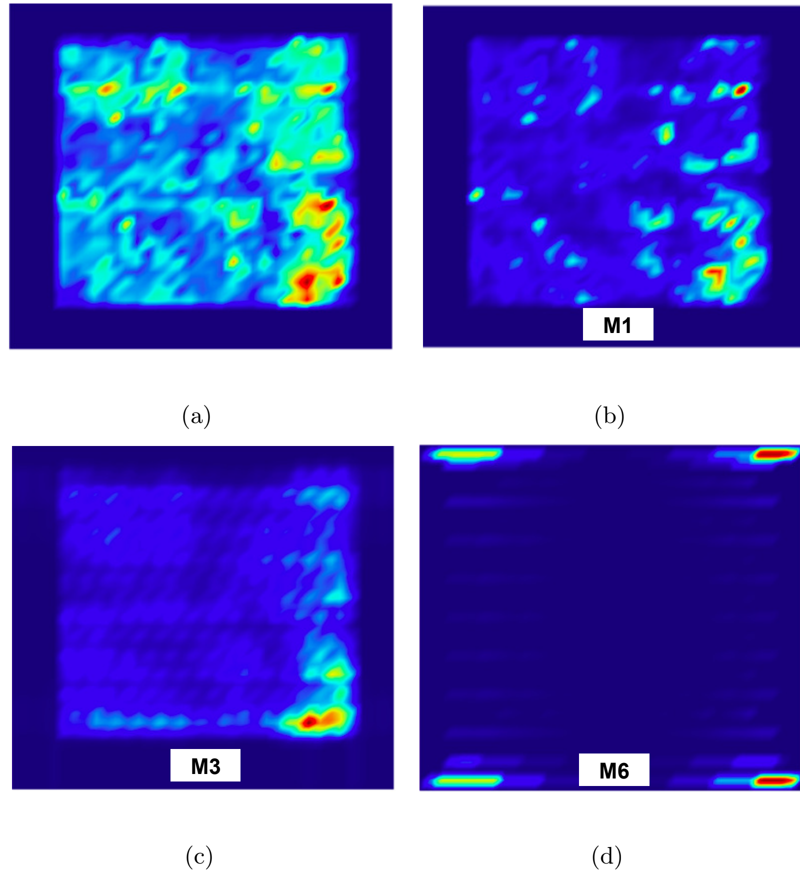


Figure 3.7: Power consumption in device layer (0-6.91mW), (a), and Joule in M1 (0-0.06mW), (b), M3 (0-0.33mW), (c), and M6 (0-4.53mW), (d), layers.

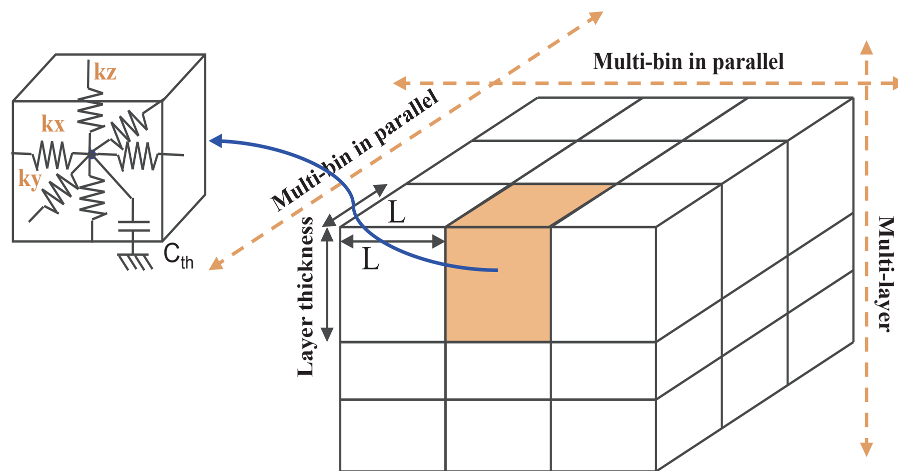
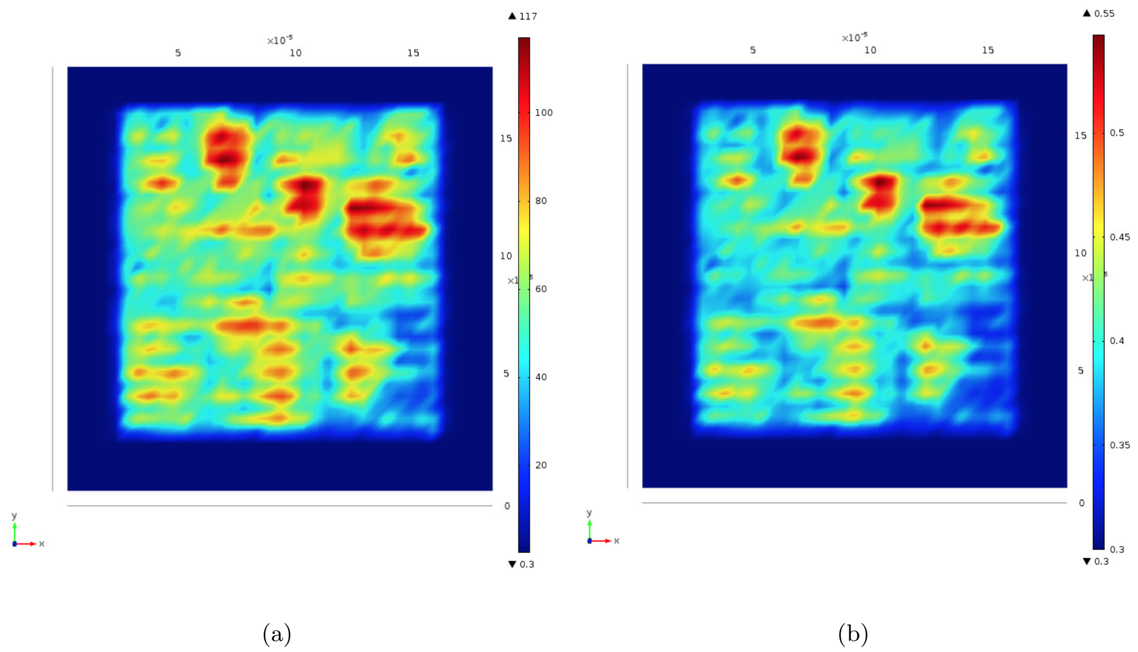


Figure 3.8: The die is divided into arrays of thermal cells with 6 thermal resistances in each cell (bin)



(a) (b)

Figure 3.9: Effective thermal resistance of M2 layer in (a) x direction and (b) y direction.

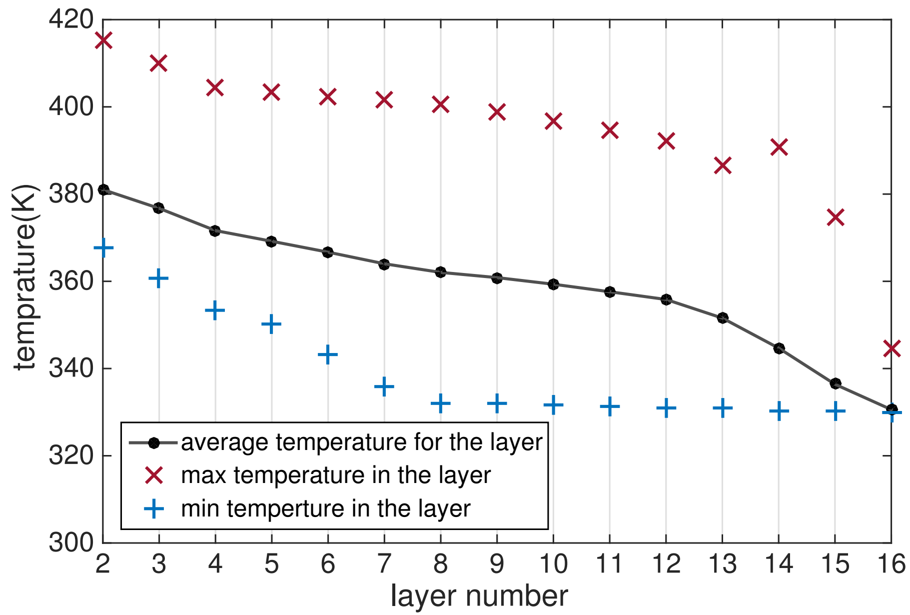


Figure 3.10: Temperature (K) variation across different layers

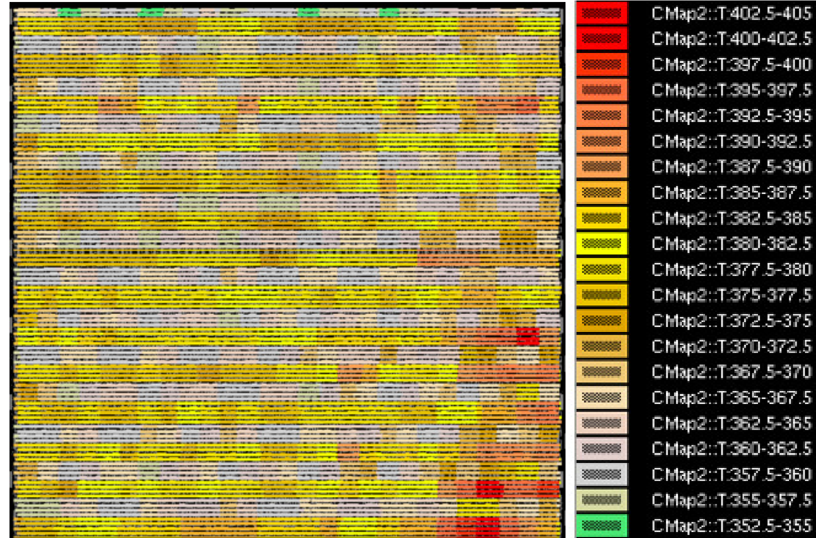


Figure 3.11: Temperature (K) distribution in M1 layer

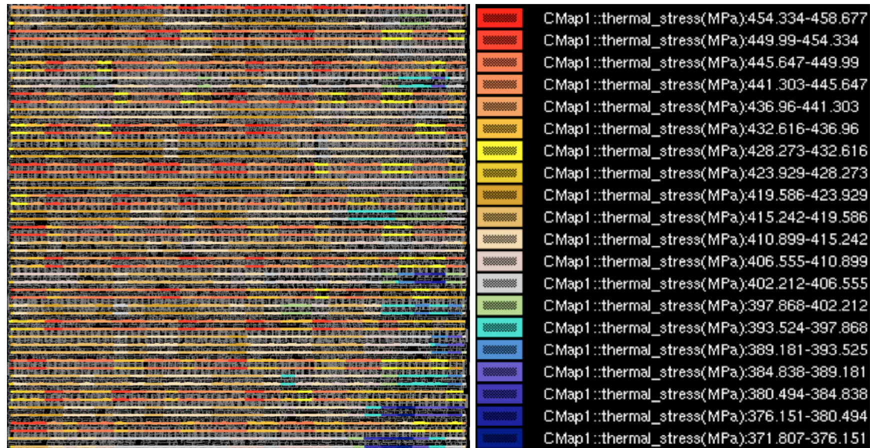


Figure 3.12: Thermal stress (MPa) distribution in M1 layer

9: **while** the largest IR drop $\leq$ threshold or $t < LT_{\text{REQ}}$ **do**

10: Move to next instant in time $t := t + \Delta t$: For branches in the growth phase, update resistance for branches with non-saturated voids.

11: Perform the DC analysis of the P/G nets. Re-compute the hydrostatic stress distribution inside each tree.

12: For each tree, find the minimum void nucleation time $(\min\{t^i_{\text{nuc}})$ for all suspicious branches in the nucleation phase. If $\min\{t^i_{\text{nuc}}\} \leq t$, the corresponding branches steps into the growth phase.

13: **end while**

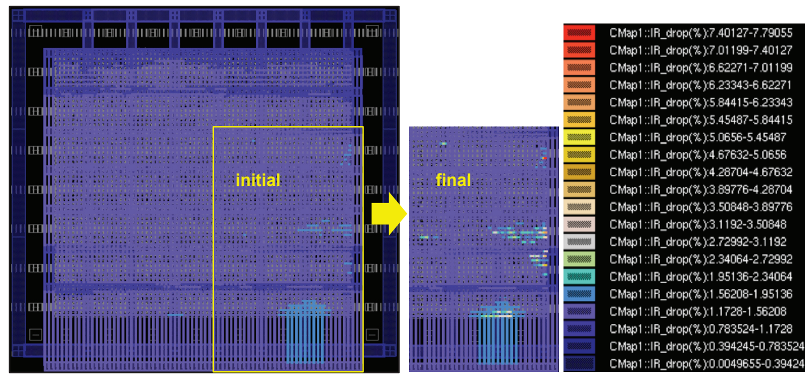
14: Output t, IR drop map and locations of voids

3.5.2 Experimental results and discussion

The proposed full-chip thermal variation aware-EM assessment method is implemented by C++ code on a 2.4GHz Linux server and tested on the 32nm standard-cell IC design. We use Calibre tools for layout extraction and circuit analysis. The EM analysis results can be mapped into the BEOL layout and displayed in Calibre RVE tool. The power net and ground net are symmetrical and independent on each other since the standard cells are modeled as effective DC current sources. In this work, the thermal analysis targets the whole chip and the EM analysis focuses on the power net. We assume the chip fails when the maximum IR drop exceeds $10\% V_{\text{DD}}$.

Fig. 3.13(b) demonstrates the EM-induced IR drop increase in the power net. The results show that the most significant IR drop change happens in the M1 layer, which is

(a)



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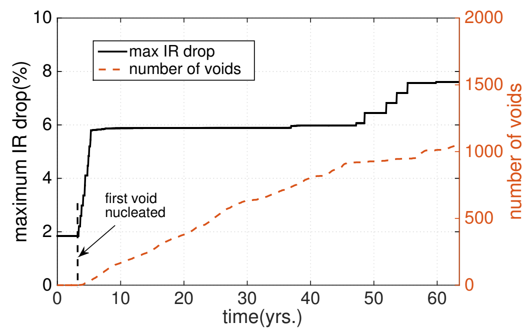


(c)

Figure 3.13: (a)Steady state hydrostatic stress map of M1 layer predicted by initial current densities (the distribution of thermal stress is taken into account), (b) EM-induced IR drops change in the power net, and (c) the increase of the maximum IR drop and number of nucleated voids over time.

the closest layer to devices. Comparing it with the initial steady state hydrostatic stress shown in Fig. 3.13(a), which includes the thermal stress and the steady state EM stress computed by the initial current densities, and with the temperature distribution shown in Fig. 3.11, we can get the conclusion that the EM-induced IR drop degradation is more likely to happen at the locations with both high hydrostatic stress and high local temperature. Fig. 3.13(c) plots the change of the largest IR drop in the power net over time, caused by the increasing number of nucleated voids. It shows that the worst IR drop is smaller than $10\%V_{\mathrm{DD}}$ ($V_{\mathrm{DD}} = 1.1V$) when the simulation stops, which means this chip has a longer lifetime than the requirement.

Effect of cross-layout temperature variation

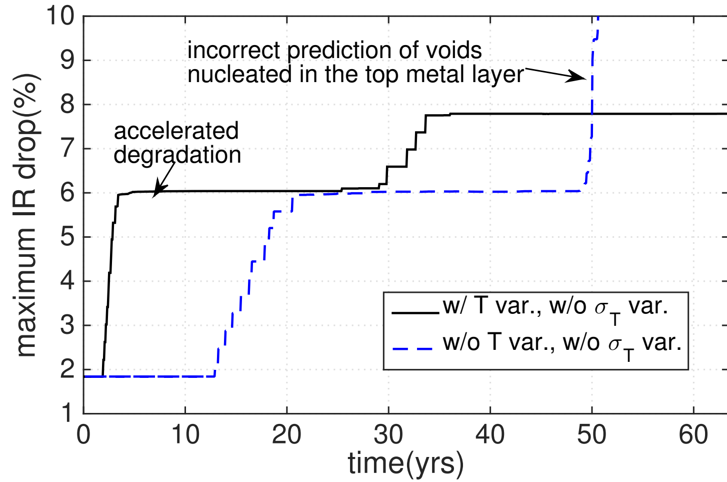
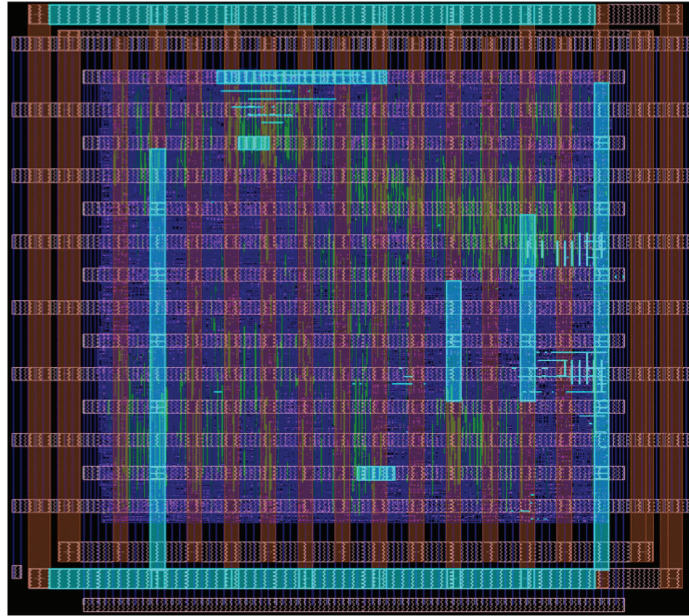
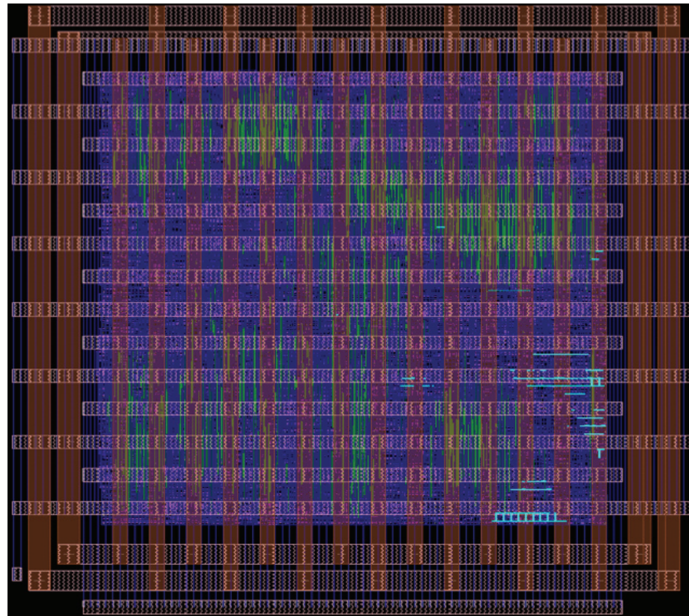


Figure 3.14: Comparison of predicted maximum IR drop increase between w/o and w/ temperature variation conditions. Uniformly distributed thermal stress is considered in both cases.

To evaluate the impact of within-die temperature variation, we performed EM assessment under assumption of uniform temperature (T=367.4K, averaged temperature



(a)



(b)

Figure 3.15: The branches with voids (blue color) at the time when simulation stops in two cases: (a) uniform averaged temperature, and (b) with temperature variation. Uniform thermal stress distribution is considered in both cases.

across the chip) and with the calculated non-uniform temperature distribution. Uniform average thermal stress σ_T =434.55MPa was assumed in both cases. The evolution of IR drop degradation and the locations of branches with voids when the simulation stops, are shown in Fig. 3.14 and Fig. 3.15 respectively.

We have several interesting observations: First, the accelerated voltage degradation caused by high local temperatures at lower layers was observed in the case of non-uniform temperature distribution during the earlier time. Second, as time goes by, the drastic IR drop increase is found under the average temperature assumption. At this time these two assumptions result in totally different analysis results (the average temperature case causes a false-alarm chip failure). This is mainly due to the incorrect prediction of voids nucleated in the top layers where the actual local temperature is much lower than the average value, which can be viewed by comparing Fig. 3.15(a) and Fig. 3.15(b).

Effect of spatial thermal stress variation

Next, we have investigated the impact of thermal stress on EM effects by comparing the IR drop evolution in two cases characterized by non-uniform and uniform (σ_T=434. 55MPa) thermal stress distributions. Fig. 3.16 shows the IR drop evolution taking place in these two cases. Contrary to the impacts of spatial temperature variation, the retarded voltage degradation has been observed when the thermal stress variation was taken into account. The failure prefers to happen at places where both the hydrostatic stress and local temperature are high. Since a higher temperature corresponds to a lower thermal stress, when spatial thermal stress variation is considered, the branches with the high temperature have smaller initial stresses compared with the average value, thus a longer evolution time

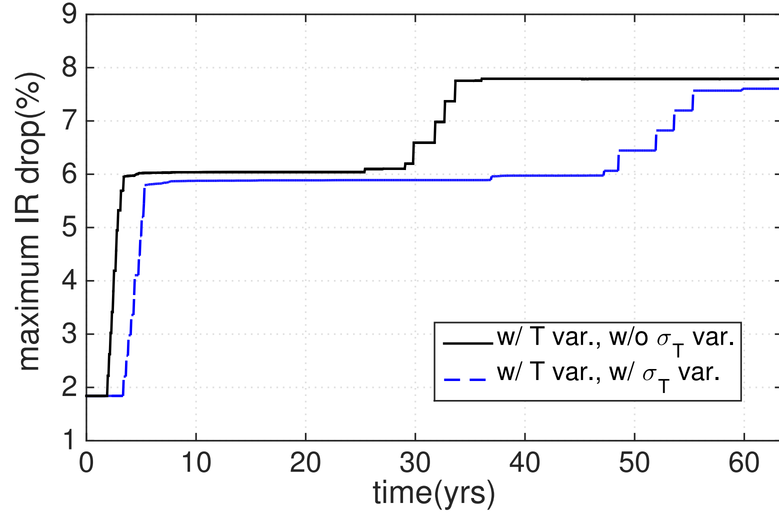


Figure 3.16: Comparison of the IR drop evolutions calculated w/o and w/ thermal variation assessments. Temperature variation is considered in both cases.

is needed for stress to reach the critical value required for void nucleation.

3.6 Summary

In this chapter, we have proposed and implemented a new EM assessment method for power delivery networks of VLSI circuits. In the proposed approach, an increase in the IR-drop above the threshold level, caused by EM-induced increase in resistances of the individual interconnect branches, is considered as a failure criterion. It replaces a currently employed conservative weakest branch criterion, which does not account an essential redundancy for current propagation existing in the P/G networks. EM-induced increase in the resistance of the individual grid branches is described in the approximation of our developed physics-based formalism for void nucleation and growth discussed in Chapter 2. We implement the tree-based analysis approach to calculate the void nucleation times in the group of branches comprising the interconnect tree. As a result, P/G networks become

time-varying linear networks. A developed technique for calculating the hydrostatic stress evolution inside a multi-branch interconnect tree allows to avoid over optimistic prediction of the TTF made with the Blech-Black analysis of individual branches of interconnect tree. Experimental results obtained on a number of IBM benchmark circuits show that the proposed method will lead to less conservative estimation of the lifetime than the existing Black-Blech based methods. It also reveals that the EM-induced failure is more likely to happen at the place where the hydrostatic stress predicted by the initial current density is large and is more likely to happen at longer times when the saturated void volume effect is taken into account.

We next improved the full-chip EM assessment methodology by integrating it with temperature and thermal stress assessment methods. Where, the temperature simulation is realized by characterizing the power dissipation in devices and Joule heating in interconnects, and by building the thermal netlist with the effective thermal properties. Then, the thermal stress variation across the layout is obtained based on the temperature distribution. Experimental results obtained on a 32/28nm test chip show that traditional assumption of the uniform average temperature leads to inaccurate predictions of the time-to-failure. Furthermore, the consideration of thermal stress variation results in a retarded EM-induced degradation.

Chapter 4

Dynamic Electromigration Models for Transient Stress Evolution and Recovery

The transient recovery effect in the EM-induced stress evolution kinetics has never been modeled properly in all the existing analytical EM models. In this chapter, we propose a new physics-based dynamic compact EM model, which for the first time, can accurately predict the transient hydrostatic stress recovery effect in a confined metal wire.

4.1 Introduction

EM-induced degradation of electric resistance in a variety of test structures is traditionally monitored by applying the DC stressing. A majority of proposed physical models describing the EM phenomenon have also assumed the DC load. At the same time

all semiconductor IC chips operate with time-dependent, for example AC or pulse, electric currents. Today's multi/many-core microprocessors are working on different performance states and are the subject for dynamic power/thermal management schemes. At the server and rack and even data center levels, many low power techniques such as the KnightShift architecture for scaling energy proportionality scheme using hybrid performance servers [5] and the big.LITTLE technology from ARM at the chip level can create dynamic power, and, hence, across-die temperature profiles [55]. Such dynamic power/energy scheduling and provisioning could result in large variations in current density and temperature, which can have huge impacts on the EM-induced stress evolution in interconnect wires and, thus, affect the failure development.

One important transient behavior in EM stress evolution is the recovery effect shown in Fig. 4.1. It refers to the stress relaxation or decreasing in the metal line, which occurs when the current is switched-off. It can be considered as the healing process extending the lifetime of interconnects. Manifestation of the recovery of EM-induced stress buildup has been observed and reported in many papers [50, 56–58]. This phenomenon is very visible when the wire is stressed by symmetric bi-directional (bipolar) pulse current waveforms. It becomes less obvious when the current waveforms are unidirectional (unipolar) characterized by the high frequencies (larger than kHz) [50, 58]. However, a lot of experimental works have found that when the frequencies of current waveforms are small enough (its period is about 100 seconds or longer), we can still see significant EM recovery, which extends the lifetime of the stressed wire [57]. Such low frequency power/temperature patterns are typical today due to the proposed low power techniques at chip/server/rack

levels, which can be operated at the time scale of minutes and hours. Emerging dark silicon also requires to keep cores at low power status for sufficient period of time [59]. However the lack of the solid EM transient models hinders the development of optimization techniques for such kind of effects.

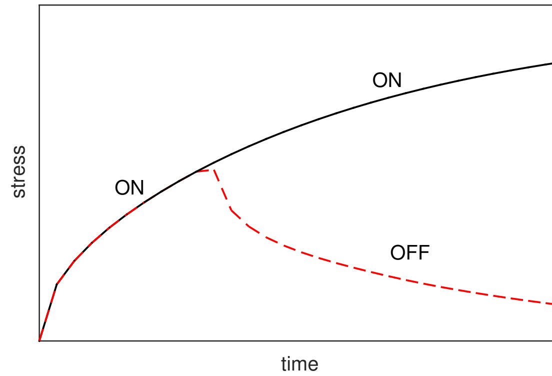


Figure 4.1: Stress relaxation (EM recovery) when current is switched-off.

In this chapter, we propose new physics-based dynamic EM model and assessment technique to deal with the stress recovery effect in interconnect wires stressed by the arbitrary (unipolar or bipolar) time-varying current waveforms and varying temperature. Such dynamic EM model is in contrast to the existing EM models, which assume the wire is stressed under constant current density and temperature. The new model is developed by the analytical solution of the one-dimensional Korhonen's equation with the time-varying electric current and temperature loads [49]. The model can explain many of the experimentally observed transient stress recovery effects caused by various current waveform patterns [50, 57, 58]. More significantly, the new EM model open the new opportunities to manage EM reliability at the circuit, system, and even server/rack/data center levels without additional design costs. A comparison of the predicted analytic stress evolution kinetics

with the results generated by the direct numerical calculation of the continuity equation with the FEA tool has demonstrated an excellent agreement.

The rest of the chapter is organized as follows: Section 4.2 reviews the physics and existing models of electromigration. Section 4.3 introduces the new dynamic EM model considering the time-varying current density and temperature. The EM stress recovery effect and and the limitation of using the effective DC for failure prediction and EM immortal check are discussed in Section 4.4. Section 4.5 presents the potential of the application of the proposed EM model for reliability-aware energy-efficient computing at system level. Section 4.6 concludes this chapter.

4.2 Background and review of existing works

4.2.1 Existing modeling based on effective direct current

Existing EM models such as the semi-empirical Black's equation, which is widely used in industry, are based on the DC load of a single confined metal wire keeping at the constant temperature [9]. In order to consider the stress buildup caused by the transient current waveforms in a typical VLSI chip, which can be unipolar, such as in the power grid networks, or bipolar, such as in the signal nets, the time-dependent current density waveforms are converted to the so called EM effective DC current, Eq. (3.3). However, using the effective current formula in Eq. (3.3) will create several problems [50]. First, the recovery factor depends on the specific current waveforms and is not constant. Second, it ignores important transient effects. For instance, we may have the driving current waveform, which makes the peak stress exceed the critical stress while the average current never leads

to void nucleation (wire is immortal).

To mitigate this problem, a number of *dynamic* EM models, which consider the time-dependent current waveforms, have been proposed [13–15]. However, the EM model in [15] is still based on traditional semi-empirical Black's equation, where the current density exponent is not a constant but a function of residual stress and current density. Especially, the recovery effect is not properly considered and the weighted average current is still used. Recently, a new dynamic EM model was proposed [16]. However, this model is based on Korhonen's continuity equation with constant current density. It fails to predict stress recovery effect as we shown in this work and inappropriately predicts increasing/constant stress when current changes are significant: reducing to a much smaller value or turning off.

4.2.2 EM physics and governing equations

EM is a physical phenomenon caused by current-induced atom diffusion in the direction of the electron flow due to momentum exchange between lattice atoms and charge carriers. This oriented atomic flow results in metal density depletion and accumulation at the ends of the wire, where the atomic migration is blocked by diffusion barriers. When the hydrostatic stress develops, the stress gradient along the wire would lead to the drift of lattice atoms in the direction opposite the direction of the electric current.

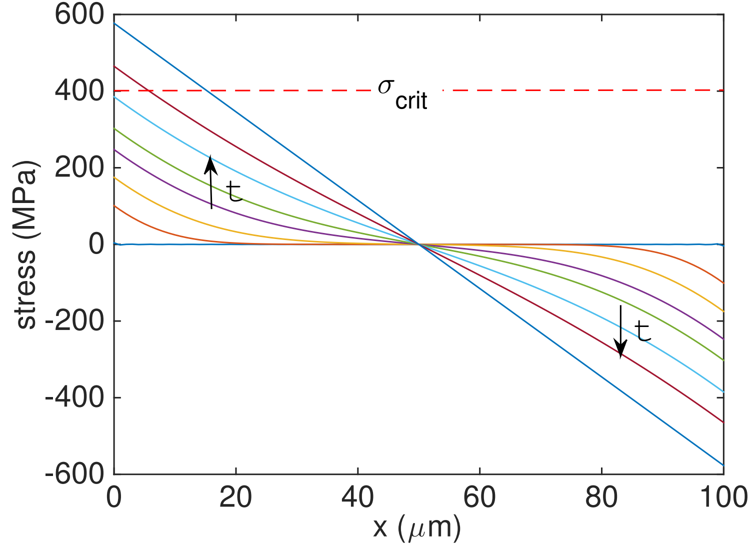
As shown in Fig. 4.2, the steady state will be reached when the backward flux compensates the current-induced flux, and the stress will be linearly distributed along the wire. Fig. 4.2(a) shows the stress evolution along the wire (with the left end as the cathode node and right as the anode node). This is a typical hydrostatic stress evolution pattern

driven by DC current. But if the driving current is time-varying, the stress might not be monotonically increasing with time. For instance, if the current density is reduced at some instance in time, then the current induced flux can be smaller than the stress gradient induced atomic backflow, and the atom migration direction can even be reversed leading to a reduction of the hydrostatic stress as shown in Fig. 4.1. Such transient recovery can make the stress evolution take longer time to reach to the critical stress for void nucleation. As a result, it can help extend the lifetime of the wires.

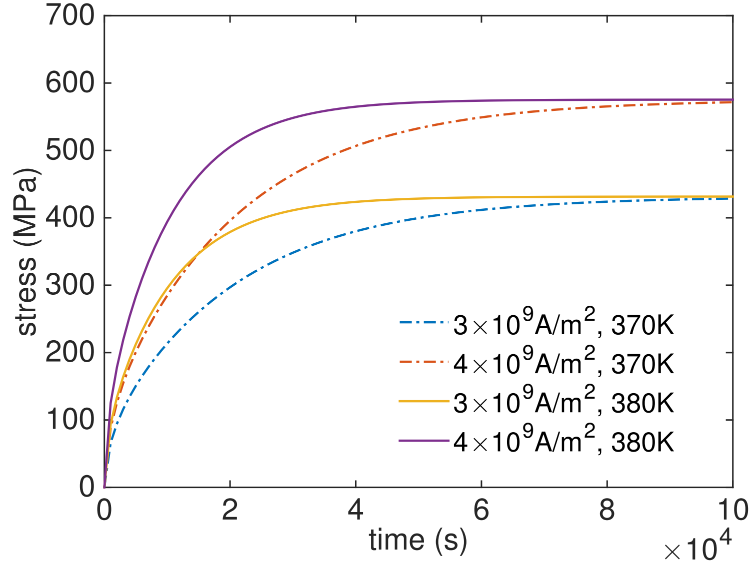
Fig. 4.2(b) shows the evolution of the electric current induced hydrostatic stress at the cathode end of a metal wire (biggest tensile stress) under different DC densities and temperatures. It indicates that both the current density and the temperature affect the stress evolution rate.

4.3 New model for the EM-induced stress evolution caused by time-dependent current density and temperature

In this section, we present the new dynamic EM model considering the time-varying current density and temperature. This model was originally derived from the analytical solution of the continuity equation Eq. (2.25) for a metal wire loaded by the time-varying electric current. We further extended the model to take into account the time-varying temperature. The resulting model can analyze the stress evolution kinetics caused by any time-varying currents and temperatures. To validate the proposed model, detailed numerical simulation of the continuity equation Eq. (2.25) should be employed. Here, we do numerical simulation using the FEA tool COMSOL. Before we proceed, we list



(a)



(b)

Figure 4.2: Evolution of hydrostatic stress (a) along the wire and (b) at the cathode end over time stressed under different current densities and temperatures, in the case of zero initial stress.

values of all employed parameter in the Table I. Also, to simplify our numerical analysis, we keep the thermal (residual) stress (σ_T) equals zero.

Table 4.1: Parameters and typical values

Parameter	Value	Parameter	Value
E_a	$0.86eV$	B	$1 \times 10^{11} Pa$
Z	10	Ω	$1.66 \times 10^{-29} m^3$
σ_{crit}	$400MPa$	ρ	$3 \times 10^{-8} \Omega$
l	$1 \times 10^{-4} m$	D_0	$7.56 \times 10^{-5} m^2/s$

4.3.1 Generalized model with the arbitrary piecewise constant current

We first present the governing stress evolution equation with time-varying current waveforms. The stress evolution takes place in an initially void-less interconnect line. To simplify the analysis, we first assume that only the current density changes over time, i.e. the temperature is constant. Later on, we extend the derived stress evolution expression to consider time-varying temperature.

Dynamic EM model considering arbitrary time-varying currents

In the case of time-dependent current density, one-dimensional continuity equation Eq. (2.25) can be converted into the following nonhomogeneous form [49]:

$$\frac{\partial(\sigma + \frac{eZ\rho j}{\Omega}(x - \frac{L}{2}) - \sigma_T)}{\partial t} - \kappa \frac{\partial^2}{\partial x^2}\left(\sigma + \frac{eZ\rho j}{\Omega}\left(x - \frac{L}{2}\right) - \sigma_T\right) = \frac{eZ\rho j}{\Omega}\left(x - \frac{L}{2}\right)\frac{\partial j}{\partial t} \quad (4.1)$$

with the boundary condition: $\frac{\partial \sigma}{\partial t}|_{x=0,L} = -\frac{eZ\rho j}{\Omega}$ and the initial condition: $\sigma(x, t = 0) = \sigma_T$. Here, $\kappa = DB\Omega/k_BT$ where $D = D_0 exp(-Ea/k_BT)$ is the atomic diffusivity which depends on temperature. As it was shown in [49], the Eq. (4.1) can be solved analytically. The

analytical solution for stress evolution kinetics takes the form:

$$\sigma(x,t) = \sigma_T + \frac{4eZ\rho}{\Omega L}\kappa \sum_{n=0}^{\infty} cos\frac{(2n+1)\pi x}{L} e^{-\frac{(2n+1)^2\pi^2}{L^2}\kappa t} \times \int_0^t j(t) e^{\frac{(2n+1)^2\pi^2}{L^2}\kappa \tau} d\tau \tag{4.2}$$

Solution Eq. (4.2) is valid for any arbitrary time-varying current waveform $j(t)$. It is not difficult to show that Eq. (4.2) converts to the standard stress evolution kinetics Eq. (2.25) if the current density is constant (DC current).

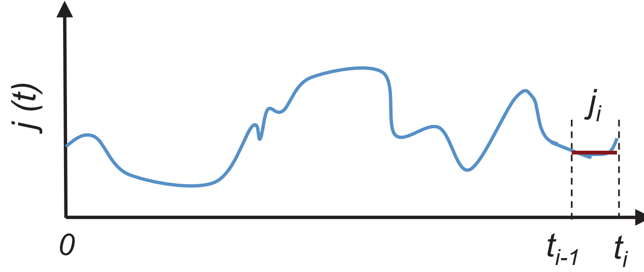


Figure 4.3: A random time-dependent current density waveform where piecewise constant method can be applied.

In practical application, the current or power inputs of a chip are better modeled as time-varying piece-wise constant as the chip may be in different stable performance/power states for a period of time instead of changing all the time. In this work, we divide a given time period $[0, t]$ into i intervals and in each interval Δt_i, we have constant temperature and current density. The time interval can be decided based on the computational complexity and precision requirement. A large interval is chosen at low frequency. Assume that we have computed the stress at t_{i-1} and want to predict the stress at $t_i = t_{i-1} + \Delta t_i$ as shown in Fig. 4.3. Then we have following iterative stress computation formula:

$$\sigma(x,t_i) = \sigma_T + \frac{4eZ\rho}{\Omega L} \sum_{n=0}^{\infty} cos\frac{(2n+1)\pi x}{L} \phi(t_i) \tag{4.3}$$

where,

$$\phi(t_i) = e^{-\frac{(2n+1)^2\pi^2}{L^2}\kappa\Delta t_i}\left[\kappa\int_0^{\Delta t_i} j_i e^{\frac{(2n+1)^2\pi^2}{L^2}\kappa\tau}d\tau + \phi(t_{i-1})\right] \tag{4.4}$$

and

$$\phi(t_1) = e^{-\frac{(2n+1)^2\pi^2}{L^2}\kappa\Delta t_1}\kappa\int_0^{\Delta t_1} j_1 e^{\frac{(2n+1)^2\pi^2}{L^2}\kappa\tau}d\tau \tag{4.5}$$

Here, j_i is the constant current density value during the time interval $[t_{i-1}, t_i]$. Note that $\frac{4eZ\rho}{\Omega L}\sum_0^\infty cos\frac{(2n+1)\pi x}{L}\phi(t_{i-1})$ presents EM stress at t_{i-1}, which is caused by the driving current $j(t)$ from the very beginning ($t = 0$) to the time instant $t = t_{i-1}$. So the accumulated hydrostatic stress at the instant in time $t = t_i$ can be easily calculated based on Eq. (4.3) if $\phi(t_{i-1})$ is provided. Fig. 4.4 shows an example of the stress evolution at the cathode end of the metal wire under time-varying current and constant temperature loads. The solution obtained from Eq. (4.3) agrees well with the result of numerical solution of the Eq. (2.25).

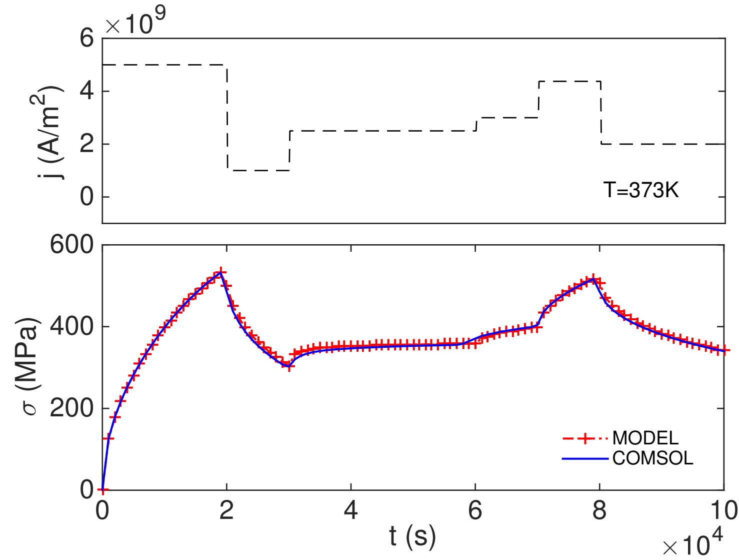


Figure 4.4: Stress evolution under time-varying current load with constant temperature.

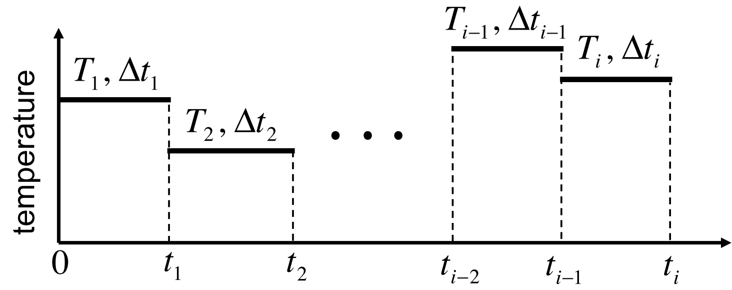
Dynamic EM model considering both time-varying current and temperature

Temperature affects atomic diffusivity and is reported to have huge (exponential) impacts on the lifetime of the wire due to EM effects [20, 60]. The on-chip temperature changes along with the change of chip workloads (power dissipation). Thus it is necessary to consider the effect of time-varying temperature in EM modeling. In this work, we employ the equivalent time scheme to account for the dynamic temperature effect, which uses expressions for stress build-up under constant temperature to describe the stress evolution under time-varying conditions [15, 16].

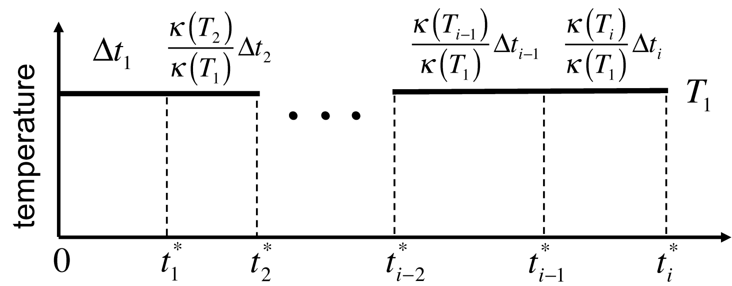
$\kappa(T(t))$ is the term that is affected by temperature:

$$\kappa(T(t)) = \frac{D_0 exp(-Ea/k_B T(t)) B\Omega}{k_B T(t)} \tag{4.6}$$

It has been observed that, if the atomic diffusivity is assumed to be independent of the stress, the temperature impact on the stress $\sigma(T, t)$ through $\kappa(T(t))$ can be translated to the time period change for a metal wire. In other words, as demonstrated in Fig. 4.5, the stress developed on the wire over time interval Δt_i under temperature T_i is equal to the stress developed over time interval $\frac{\kappa(T_i)}{\kappa(T_1)}\Delta t_i$ under temperature T_1. As a result, the problem of analyzing stress evolution considering both time-varying current density and temperature becomes estimating stress evolution under dynamic current stress while temperature is constant ($T = T_1$), which has been discussed in Section 4.3.1. Thus we replace the time intervals Δt_i in Eq. (4.4) and Eq. (4.5) with new time intervals $\Delta t_i^* = \frac{\kappa(T_i)}{\kappa(T_1)}\Delta t_i$ and apply constant temperature $T = T_1$. The stress at t_i considering time-varying current density and



(a)



(b)

Figure 4.5: (a) Original time-dependent temperature waveform and (b) constant temperature with equivalent time intervals.

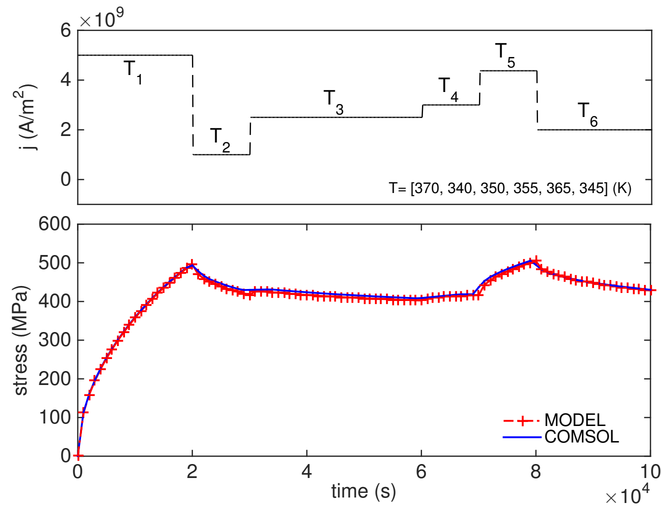


Figure 4.6: Stress evolution under time-varying current and temperature stressing.

temperature can be calculated as:

$$\sigma(x,t_i) = \sigma_T + \frac{4eZ\rho}{\Omega L}\sum_{n=0}^{\infty} cos\frac{(2n+1)\pi x}{L}\phi(t_i) \tag{4.7}$$

where,

$$\begin{aligned}
\phi(t_i) =& e^{-\frac{(2n+1)^2\pi^2}{L^2}\kappa(T_1)\frac{\kappa(T_i)}{\kappa(T_1)}\Delta t_i} \times \\
& \left[\kappa(T_1)\int_0^{\frac{\kappa(T_i)}{\kappa(T_1)}\Delta t_i} j_i e^{\frac{(2n+1)^2\pi^2}{L^2}\kappa(T_1)\tau} d\tau + \phi(t_{i-1})\right] \\
=& e^{-\frac{(2n+1)^2\pi^2}{L^2}\kappa(T_i)\Delta t_i} \times \\
& \left[\kappa(T_1)\int_0^{\Delta t_i} j_i e^{\frac{(2n+1)^2\pi^2}{L^2}\kappa(T_1)\frac{\kappa(T_i)}{\kappa(T_1)}\tau}\frac{\kappa(T_i)}{\kappa(T_1)} d\tau + \phi(t_{i-1})\right] \\
=& e^{-\frac{(2n+1)^2\pi^2}{L^2}\kappa(T_i)\Delta t_i} \times \\
& \left[\kappa(T_i)\int_0^{\Delta t_i} j_i e^{\frac{(2n+1)^2\pi^2}{L^2}\kappa(T_i)\tau} d\tau + \phi(t_{i-1})\right]
\end{aligned} \tag{4.8}$$

and

$$\phi(t_1) = e^{-\frac{(2n+1)^2\pi^2}{L^2}\kappa(T_1)\Delta t_1}\kappa(T_1)\int_0^{\Delta t_1} j_1 e^{\frac{(2n+1)^2\pi^2}{L^2}\kappa(T_1)\tau} d\tau \tag{4.9}$$

Now we are able to predict the EM-induced stress evolution under time-varying current load with time-varying temperature based on Eq. (4.7). Fig. 4.6 shows an example of the stress evolution at the cathode end of the metal wire caused by dynamic current load, which refers for instance, to a core working in different power states. Since the time scale for each state is much longer than thermal time constant, we assume each state corresponds to a constant temperature value. We have compared the obtained analytical solution with the result of numerical solution of the Eq. (2.25) with the known $j(t)$ and $T(t)$ and have gotten an excellent agreement as shown in the Fig. 4.6.

It can be observed from Eq. (4.8) that, different from the expressions in [15, 16] which need to translate the actual time intervals Δt_i to the equivalent time intervals $\frac{\kappa(T_i)}{\kappa(T_1)}\Delta t_i$

during the stress computation, the final expression of our proposed stress evolution model includes only the actual time-inverval Δt_i and the actual temperature T_i during the time interval Δt_i. Besides, Eq. (4.8) differs from Eq. (4.4) only in that it uses a time-dependent temperature T_i instead of a constant temperature. Thus the proposed model naturally considers the temperature change. It also should be noted that the derived general discretization formula Eq. (4.7) can be applied to any time-varying current densities and temperature waveforms, and at the same time correctly predicts stress recovery effect, which is ignored in all existing ad-hoc methods [15, 16].

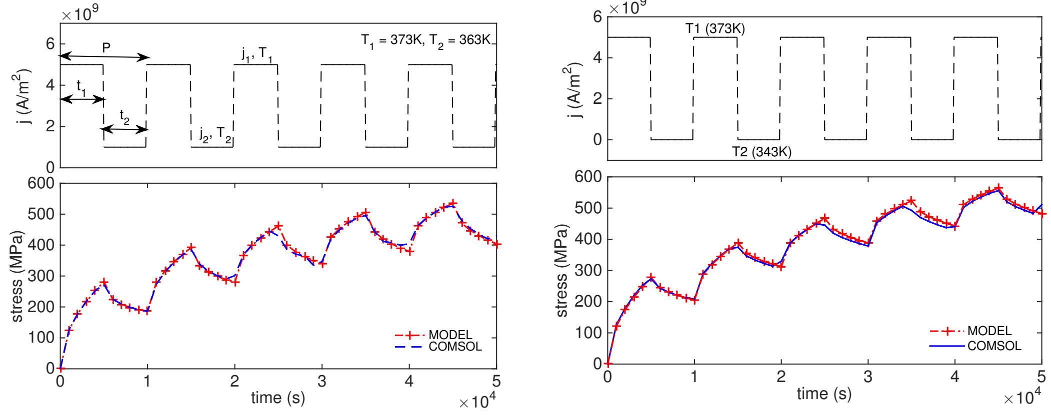
4.3.2 EM modeling for periodic pulse current

Another interesting case is the driving currents are periodic pulse waveforms, which can be found in the typical clock networks and in some signal networks as well. In this case, the computation of the stress evolution can be simplified. Let's consider, for instance, the current density profiles shown in Fig. 4.7, which are good approximations for real power traces in the practical situations. Specifically, we assume that the current density $j(t)$ has the following form:

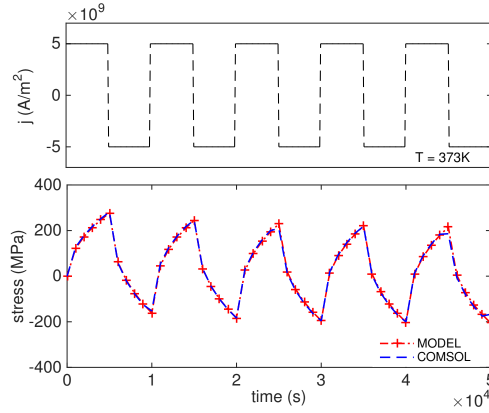
$$j(t) = \begin{cases} j_1, \ mP \le t < mP + t_1, \\ \\ j_2, \ mP + t_1 \le t < (m+1)P, \end{cases} \tag{4.10}$$

We note that j_1 and j_2 can be in the same phase or in opposite phases of the pulse, P is the period of the current waveform. For large time scales, which is longer than thermal time constant, we can assume the temperature profile has similar form:

$$T(t) = \begin{cases} T_1, \ mP \le t < mP + t_1, \\ \\ T_2, \ mP + t_1 \le t < (m+1)P, \end{cases} \tag{4.11}$$



(a) (b)



(c)

Figure 4.7: Stress evolution caused by periodic (a), (b) unipolar and (c) symmetrical bipolar pulse current densities at cathode end of the metal line.

In this case, the stress evolution expression considering periodic pulsed current waveform can be derived based on Eq. (4.7):

- **If** $mP \leq t < mP + t_1$ **(**$\tau = t - mP$**):**

$$\sigma(x,t) = \sigma_T + \frac{4eZ\rho}{\Omega L} \sum_{n=0}^{\infty} cos \frac{(2n+1)\pi x}{L} e^{-\frac{(2n+1)^2\pi^2}{L^2}\kappa_1 \tau} \times \left(\kappa_1 \int_0^{\tau} j_1 e^{\frac{(2n+1)^2\pi^2}{L^2}\kappa_1 \tilde{\tau}} d\tilde{\tau} + M\phi_P \right) \tag{4.12}$$

where,

$$\phi_P = e^{-\frac{(2n+1)^2\pi^2}{L^2}(\kappa_1 t_1+\kappa_2 t_2)}\kappa_1 \int_0^{t_1} j_1 e^{\frac{(2n+1)^2\pi^2}{L^2}\kappa_1\tilde{\tau}} d\tilde{\tau} + e^{-\frac{(2n+1)^2\pi^2}{L^2}\kappa_2 t_2}\kappa_2 \int_0^{t_2} j_2 e^{\frac{(2n+1)^2\pi^2}{L^2}\kappa_2\tilde{\tau}} d\tilde{\tau}$$

- **If** $mP + t_1 \leq t < (m+1)P$ **(**$\tau = t - mP - t_1$**):**

$$\sigma(x,t) = \sigma_T + \frac{4eZ\rho}{\Omega L}\sum_{n=0}^{\infty} cos\frac{(2n+1)\pi x}{L} e^{-\frac{(2n+1)^2\pi^2}{L^2}\kappa_2\tau} \times \left(\kappa_2 \int_0^{\tau} j_2 e^{\frac{(2n+1)^2\pi^2}{L^2}\kappa_2\tilde{\tau}} d\tilde{\tau} + \phi_1 + M\phi_P\right) \tag{4.13}$$

where,

$$\phi_1 = e^{-\frac{(2n+1)^2\pi^2}{L^2}\kappa_1 t_1}\kappa_1 \int_0^{t_1} j_1 e^{\frac{(2n+1)^2\pi^2}{L^2}\kappa_1\tilde{\tau}} d\tilde{\tau}$$

$$\phi_P = e^{-\frac{(2n+1)^2\pi^2}{L^2}(\kappa_1 t_1+\kappa_2 t_2)} \times \left(\phi_1 + \kappa_2 \int_0^{t_2} j_2 e^{\frac{(2n+1)^2\pi^2}{L^2}\kappa_2\tilde{\tau}} d\tilde{\tau}\right)$$

In both cases, we have

$$t_2 = P - t_1 \quad M = \frac{1 - e^{\frac{-(2n+1)^2\pi^2}{L^2}m(\kappa_1 t_1+\kappa_2 t_2)}}{1 - e^{\frac{-(2n+1)^2\pi^2}{L^2}(\kappa_1 t_1+\kappa_2 t_2)}}$$

$$\kappa_1 = \frac{D_0 e^{-\frac{E_a}{k_B T_1}} B\Omega}{k_B T_1} \quad \kappa_2 = \frac{D_0 e^{-\frac{E_a}{k_B T_2}} B\Omega}{k_B T_2}$$

The proposed model for periodic pulse current has been validated by results of numerical simulations as shown in Fig. 4.7. Fig. 4.7(a) and Fig. 4.7(b) correspond to unipolar pulsed current density waveforms, where the former one has two nonzero magnitudes, while Fig. 4.7(c) is the case of symmetrical bipolar pulsed current density. Significant stress variation caused by dynamical current loads is observed. We will discuss this phenomenon in the next section.

4.4 Study of the EM stress recovery

EM process is composed of the void nucleation phase followed by the void growth. As it was mentioned above, the void is generated from the preexisting flaw existing in the metal when the EM-induced hydrostatic tensile stress exceeds the critical one. We now analyze the EM stress recovery process focusing on the first phase where the void has not been nucleated. The recovery effect of hydrostatic stress, which is described in this subsection, is based on the proposed new dynamic EM model.

4.4.1 EM stress recovery effect

As shown in the previous sections, EM recovery happens when the current density goes down temporarily. In Fig. 4.7, the hydrostatic stress is reduced when the current density jumps from j_1 to a much smaller value j_2. As a result, it takes longer time for the stress to reach the critical value, thus results in a longer lifetime. The EM recovery effect is mainly caused by the net atomic backflow, which relaxes the stress. This phenomenon can be easily understood when atoms change their migration direction in the opposing phase of bipolar stressing. On the other hand, even when j_1 and j_2 are in the same direction, it is still possible that the net atom flow can change their direction. The reason is that when current is decreasing, the atomic backward flux caused by an accumulated stress gradient will prevail the electronic current induced flux and we will have a temporal reduction in the stress. Fig. 4.8 shows the analysis of the stress recovery for a single pulse current case. Fig. 4.8(a) refers to the schematics for current density and temperature.

To further study the recovery effects, we first fix the temperature and investigate

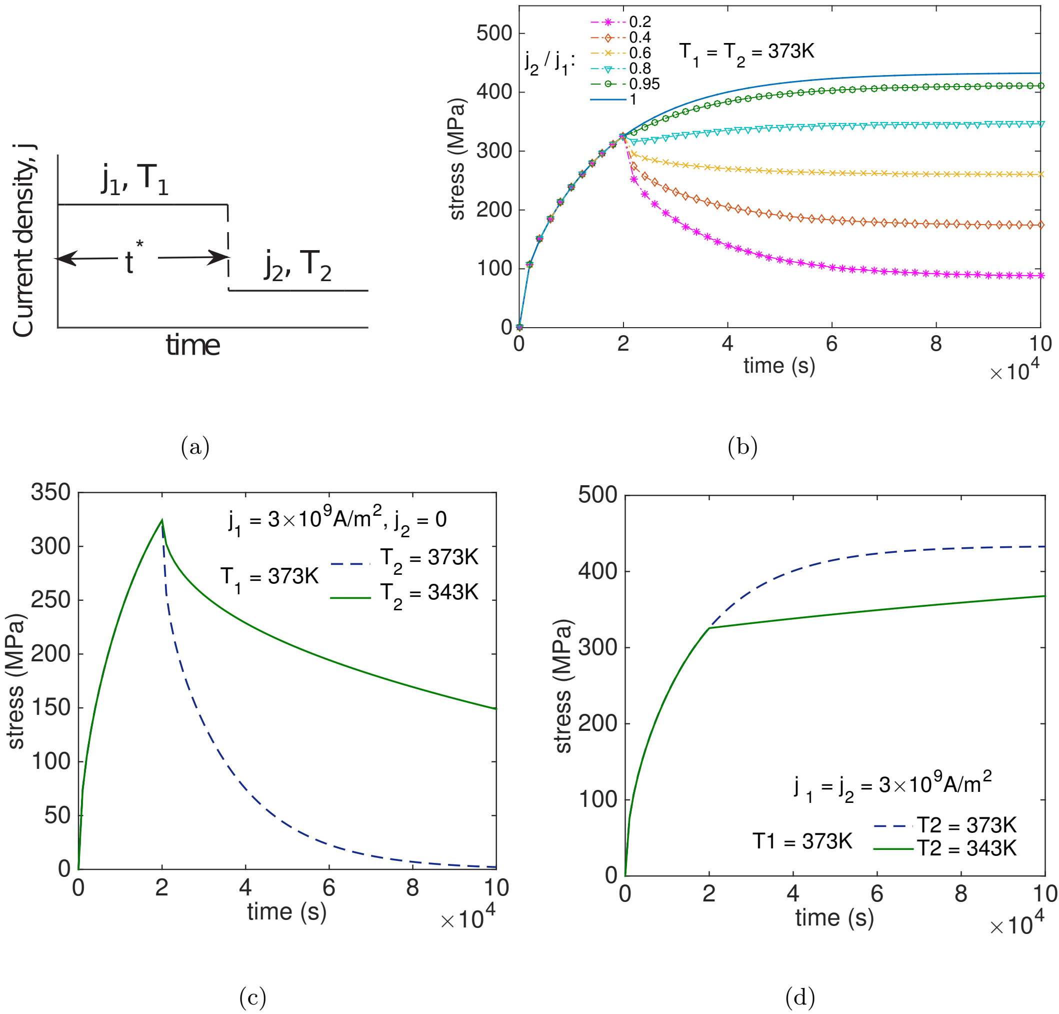


Figure 4.8: (a) Time dependent current density and temperature waveform, (b) EM recovery considering different current density change magnitude at constant temperature, (c) stress relaxation when current is switched off at different temperatures, and (d) stress evolution caused by DC current at different temperatures.

EM recovery under different magnitudes of current density change as shown in Fig. 4.8(b). Then we investigate the impact of temperature on stress evolution considering different current loads. Fig. 4.8(c) describes the stress recovery when current is switched off, while Fig. 4.8(d) corresponds to constant current stressing. The observations are summarized as following:

- There could be no stress recovery when current density difference is small, for example the $j_2/j_1 = 0.95$ curve in Fig. 4.8(b). This is because the electron flow induced forward flux can be still larger than the stress gradient induced backward flux when current density reduces from j_1 to j_2. Thus the atoms keep diffusing from the cathode end to the anode end along the metal line, results in continuous accumulation of the stress. The backward atomic flux caused by stress gradient could be larger than the current induced forward flux if the current density difference is significant, where an extreme case is the current is switched off at an instant in time $t = t^*$. This atomic backflow will be gradually reducing over time and finally the system will reach a new equilibrium state corresponding to the new current density.

- As shown in Fig. 4.8(c), the accumulated stress starts to relax when current is turned off. This process is described by an exponential decay with the time constants $\tau_0^{(2n+1)} = l^2/\kappa\pi^2(2n+1)^2 = \tau_0/(2n+1)^2$, determined by the atomic diffusivity. We observe that higher temperature can speed up atom diffusion towards the cathode end and lead to more recovery. This is contrary to the non-recovery case, for instance the metal wire stressed by constant current as demonstrated in Fig. 4.8(d), where higher temperature results in faster stress accumulation thus a shorter lifetime.

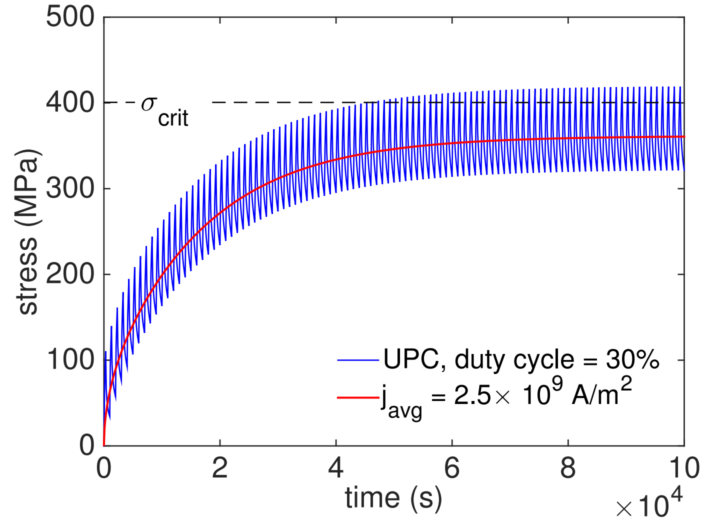
4.4.2 Limitation of using effective DC methods

For unidirectional current, the time-averaged or other weighted averaged currents have been used as the effective DC in existing EM analysis. However, we show in this subsection that using the effective DC for failure predication and immortal wire detection

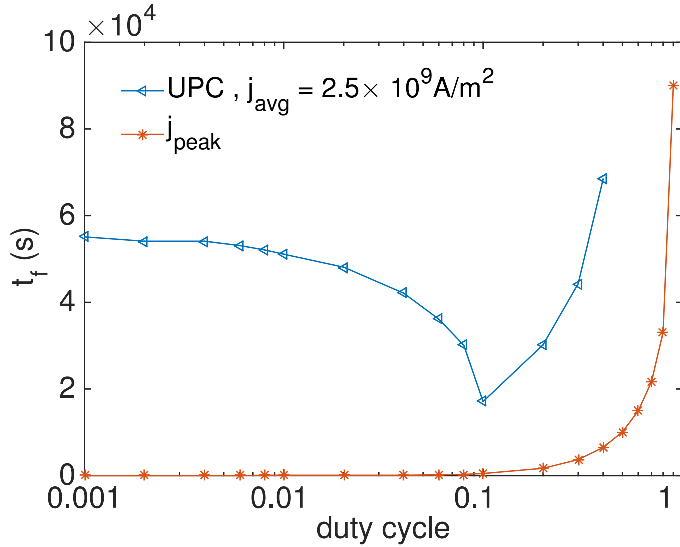
can lead sometime to wrong results.

It is well known that the Blech rule has been employed for the out filtration of immortal wire segments with diffusion blocking boundaries [8]. The interconnect will not fail if the product of $(j \times L)$ is smaller than the critical value, as shown in Eq. (2.3). Now let's look at one particular case. Assuming at a constant temperature, we set the average current density (j_{avg}) to $2.5 \times 10^9 A/m^2$ so that $(j_{avg} \times l) < (j \times l)_{crit}$, which means that the metal line is EM immortal under the average current model using the Blech rule. However, based on the proposed dynamic model, which is also the actual numerical analysis results as shown Fig. 4.9(a), we find that stress can go above the critical stress σ_{crit}, indicating that the void will be nucleated in this case. Note that the kinetics of stress evolution is caused by unipolar pulse current of 30% duty cycle in Fig. 4.9(a).

Fig. 4.9(b) further shows the lifetimes of a wire caused by UPC under different duty cycles (duty cycle = 1 means DC current) with the same average current density using the proposed EM model. We also show the lifetime of a wire caused by the peak current of the UPC. From the figure, we can observe that the wire would fail by UPC stressing when duty cycle $\leq$ 40% (when the curve starts to appear in the figure). However, if we use the average current density for the calculation, as shown in the previous figure, the wire will never fail by EM. So the effective DC method can lead to optimistic EM estimation, which can be dangerous for practical EM signoff. On the other hand, simply applying worst-case current density would lead to too conservative results, limiting the design space for reliability-performance trade-off. Traditionally, the EM failure for a single confined metal line is considered as, for example, 10% line resistance increase. So far, we have discussed a



(a)



(b)

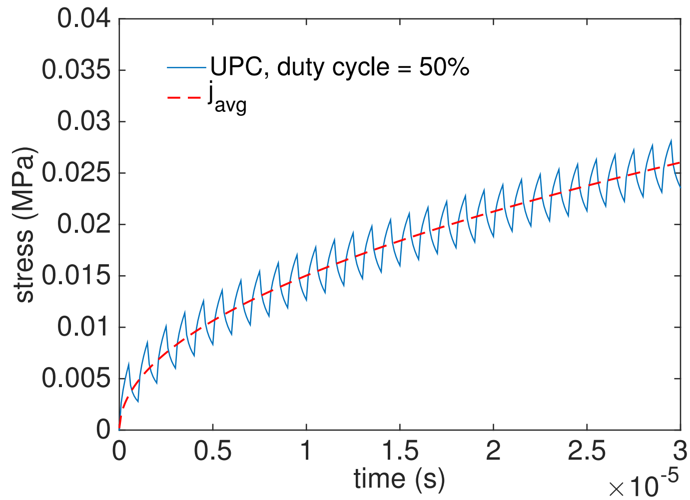
Figure 4.9: (a) Stress evolution at the cathode end of the metal line caused by the unipolar pulse current (UPC) with duty cycle = 30% and averaged DC current, (b) EM lifetimes for UPC load with various duty cycles compared with lifetimes caused by constant peak current load. Here, j_{avg} is fixed to $2.5 \times 10^9 A/m^2$ so that $(j_{avg} \times L) < (j \times L)$, T=373K.

phenomenon of the void nucleation, which by itself cannot increase the line resistance. Void growth following it nucleation is responsible for this increase. As it was shown in [20], it is

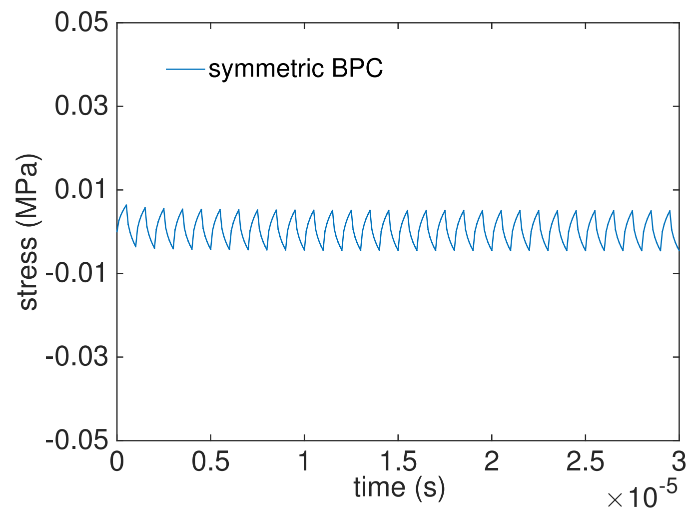
pretty straightforward to account the void volume growth for the accurate estimation of the line lifetime. But, taking into consideration the noticeable redundancy existing in on-chip interconnects, we can conclude that the failure of an individual line of the power/ground grids cannot result in the interconnect failure. New criterion for the EM-induced chip failure was proposed in a number of works, see for example [20, 45]. To be more specific, EM-induced voltage drop degradation above the spec should be considered as the failure criteria for the full-chip EM assessment [20].

All above results were obtained for the low frequency currents with time intervals comparable to time constant τ_0, which is close to minutes or hours. Time-varying current or power profiles in those cases are more likely to be caused by power/energy management at server/rack/data center levels, where the currents under analysis are mainly carried by the power/ground nets. However, the chip level power management and scheduling may operate at millisecond level and chip clocks may operate in the MHz and GHz ranges. Fig. 4.10 analyzes the stress evolution in a metal line caused by UPC and symmetrical BPC at 1MHz frequency, which corresponds to the signal lines in the circuit. We can observe from the figure that, at high frequencies, the averaged DC currents can be good estimations of the unipolar and bipolar pulsed currents.

In this case, the time-dependent current induced stress fluctuates (∼0.01MPa) around the curve, which describes the stress evolution generated by the effective DC current. This is because at high frequencies, the time intervals are much shorter than τ_0 so that the system cannot reach a new equilibrium state corresponding to the new applied current by means of atom diffusion. In Fig. 4.10(b), stress fluctuates around zero for symmetrical



(a)



(b)

Figure 4.10: Stress evolution at the cathode end of the metal line caused by unipolar pulse (UPC) with duty cycle = 50% and symmetrical bipolar pulse current (BPC) loads at T = 400K.

bipolar pulse current. It indicates complete EM recovery during current reversal, and has been experimentally observed in [58]. Thus high frequency symmetrical bipolar current will not cause EM failure in interconnects.

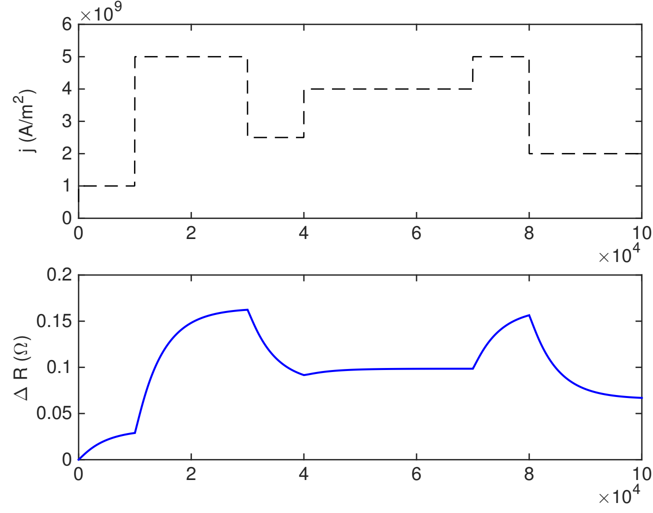
4.4.3 Resistance degradation caused by the symmetrical bidirectional current

Results, that were obtained above, indicate that even long metal lines loaded with the symmetrical bipolar pulse or AC currents will never failed since the EM-induced accumulation of the critical stress required for voiding or hillock formation is never happened. Nevertheless there are a good number of papers providing the experimental proof of failures generated by this type of stressing [13, 50, 61, 62]. One of the possible answers for this paradox can be found in the paper of Moning *et al.* [63], where the identical defects were found in all three lines located in a close proximity to each other in the test structure with two outer lines loaded with the sinusoidal voltages and the middle line was not carrying any current. The temperature oscillations generated by the outer lines have resulted in the identical defects in all three lines. Authors have concluded that the thermal fatigue controlled by diffusive mechanism and interface properties was responsible for these defects. A difference between these fatigue-based defects and the EM-induced voids is a mobility of the later under the action of electric current, which can be observed, for example, by SEM studies [64].

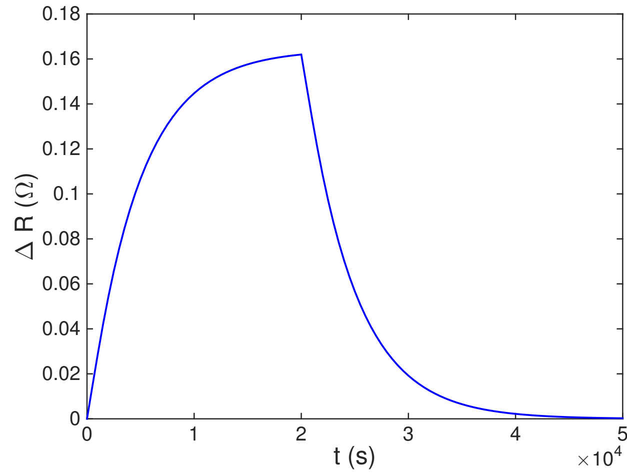
Another possible mechanism of failure caused by symmetrical bidirectional currents is the growth of a void, which was formed in the line as the result of thermal stress relaxation. Very short metal lines with preexisted thermal voids, loaded with such bidirectional currents, can demonstrate a notable resistance increase when a specific temperature oscillation is generated. In order to prove the existence of this mechanism, we need to develop a formalism describing an evolution of the metal line resistance caused by the current

induced evolution of the void volume. As it was discussed in [25], a metal line embedded in the rigid confinement and cooled from the zero stress temperature down to the test temperature can reach two different states of equilibrium. One of them is the state with a uniformly distributed tensile stress, which was generated in the line due to a difference in the coefficients of thermal expansion of the metal and surrounding. Another one is characterized by the presence of a void, which volume is determined by the relaxation of the preexisted tensile strain, and by zero stress everywhere else in the metal. It should be mentioned that generated thermal stress should exceed the critical stress, which is required for void nucleation. The later state is the only stable equilibrium state for the metal line with the large tensile stress. When an electrical stressing is applied to this line, a void, if it is located at the line end, starts changing its volume. In the case of DC stressing, a void located at the cathode end of line will be growing by means of migration of the void surface atoms to the metal bulk.

In the case of time-dependent current densities loaded to the line with the preexisted void, a calculation of the stress evolution is done in the way very similar to that was used for the calculation of stress evolution in the void-less case, considered in Sec. 4.3. Conversion of the stress distribution obtained from the solution of Eq. (4.1), with the zero stress and zero flux BC at the void edge and the anode end of line correspondingly, to the void volume evolution through $V(t) = -\int_0^L \frac{\sigma(x,t)}{B} dx$, and, then, to the kinetics of the resistance change, provides the following results: for the general case time-dependent current



(a)



(b)

Figure 4.11: (a) Short line resistance evolution caused by a random set of current densities, (b) relaxation of the resistance change accumulated during $2 \times 10^4 s$ of $j = 5 \times 10^9 A/m^2$ stressing. $T = 400K$ for both cases.

density j(t): (global time is t)

$$\Delta R = -\frac{4eZ\rho D_a}{\pi k_B T}\left(\frac{\rho_{\text{TaN}}}{H_{Ta}(W+2H)} - \frac{\rho_{Cu}}{WH}\right)\sum_{n=1}^{\infty}\frac{(-1)^n}{(2n+1)e^{-\kappa\frac{(2+1)^2\pi^2}{4L^2}}t}\int_0^t j(t)e^{\kappa\frac{(2+1)^2\pi^2}{4L^2}\tau}d\tau \tag{4.14}$$

and for resistance relaxation after switching off the electric current at t_+: (global time is $t \geq t_+$)

$$\Delta R = -\frac{4eZ\rho D_a}{\pi k_B T}\left(\frac{\rho_{\text{TaN}}}{H_{Ta}(W+2H)} - \frac{\rho_{Cu}}{WH}\right)\sum_{n=1}^{\infty}\frac{(-1)^n}{(2n+1)e^{-\kappa\frac{(2+1)^2\pi^2}{4L^2}t}}\int_0^{t_+} j(t)e^{\kappa\frac{(2+1)^2\pi^2}{4L^2}\tau}d\tau \tag{4.15}$$

Fig. 4.11 shows the kinetics of line resistance change caused by a random time-dependent current, Fig. 4.11(a), and by switching off the applied current, Fig. 4.11(b).

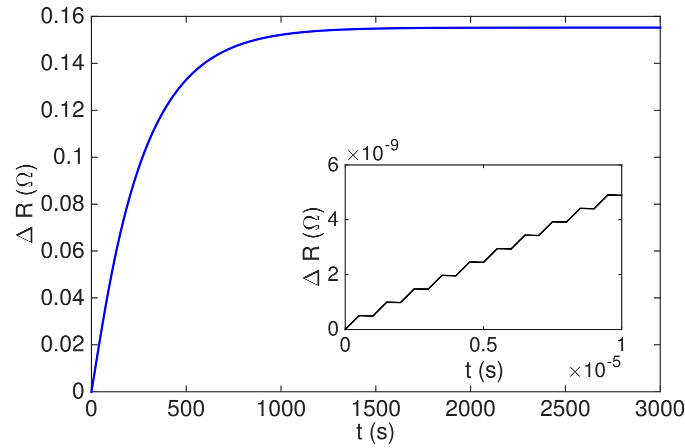


Figure 4.12: 1 MHz symmetrical BPC load with $j_+ = 5 \times 10^9 A/m^2$, $j_- = -5 \times 10^9 A/m^2$, $t_+ = t_- = P/2$, $T_+ = 450K, T_- = 400K$.

Fig. 4.12 shows the resistance increase caused by the high frequency symmetrical BPC, which is synchronized with a specific temperature oscillation: the positive pulse of the current happens at higher temperature than the negative pulse. It destroys the symmetry of the bidirectional change of the void volume caused by a transfer of atoms between the void surface and metal bulk. The resistance increase shown in Fig. 4.12 is happened when the current positive pulses forcing atoms to move from the void surface into the metal in the direction toward the anode end of line occur at $T = 450K$, while the negative pulses pushing

atoms back on the void surface take place at lower temperature of $T = 400K$. We use this ideal but unrealistic synchronized current-temperature dynamics just to illustrate a possible mechanism of resistance degradation in short metal lines loaded with the symmetrical BPC. In reality, we can expect a variety of temperature oscillations inside on-chip interconnect due to a sporadic character of switching of many millions of transistors, which locations are distributed through the chip layout. Such irregular temperature oscillations can cause asymmetry in the void shrinking-advancing and, in some cases, can be responsible for void growth above the critical size, corresponding to the threshold increase of the line resistance

4.5 Application for system level reliability aware computing

Now we present a potential application of the proposed EM model for reliability-aware energy-efficient computing at the server level. We look at the KnightShift architecture [5], which is a server-level heterogeneous server architecture that introduces an active low-power mode using the additional computing node called the Knight. KnightShift enables two energy-efficient operating regions from two different CPUs. Fig. 4.13 shows the power trace a KnightShift architecture will generate, where the Knight is a node with a 1.8Ghz Intel Atom D525, which operates from 15W to 16.7W, and the CPU and memory consumes 9W at idle, while the primary node corresponds to dual 2.13GHz 4-code Intel Xeon L5630 that consumes from 156W to 205W at active mode.

The main benefit of the KnightShit architecture is that the primary node can be powered off to save energy during the light demands and Knight can still operate to take the light loads. If the both power-on and shut-down time can be properly managed and

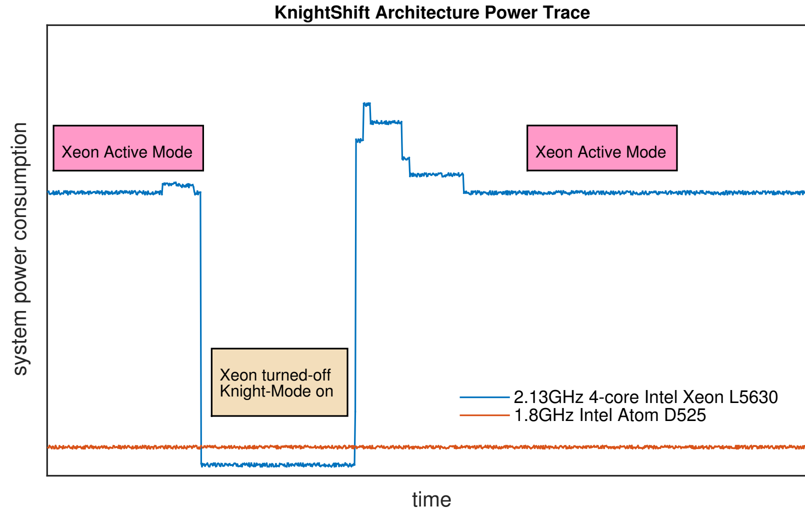


Figure 4.13: Power trace in KnightShift server [5].

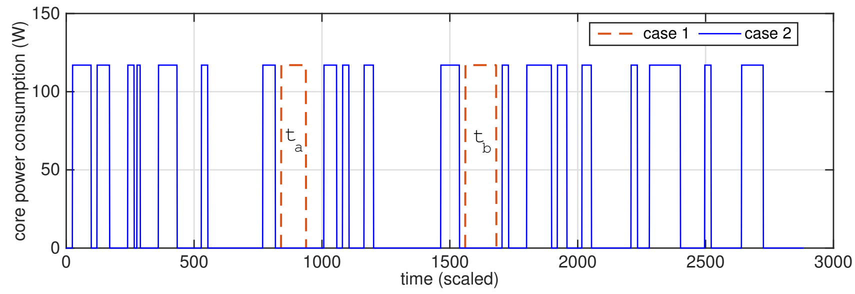
controlled such that performance can still be maintained, then we can significantly extend the server reliability by leveraging the EM recovery effects, predicted by the proposed model. Note that KnightShift can also place the primary server in suspend mode quicker than shutting down, but at the cost of higher idle power. For the sake of illustration, we only consider the shut-down situation in this work.

Specifically, we present two different power traces for the Xeon CPU based on [65] for our analysis. As demonstrated in Fig. 4.14(a), the two trace are different in that the Xeon CPU is working during t_a and t_b in $case1$ and is turned-off in $case2$. The temperature is assumed to be 363K when Xeon node is active and 340K when it is off [66]. During this period (t_a and t_b), the task loads could be taken over by the Knight node when the demand is light, or by other primary node in a server cluster for heavy demands. Such power-off period not only leads to energy saving, it also can be served as the recovery period for EM effect to extend the lifetime of the chip. Indeed, by using the proposed EM model, we

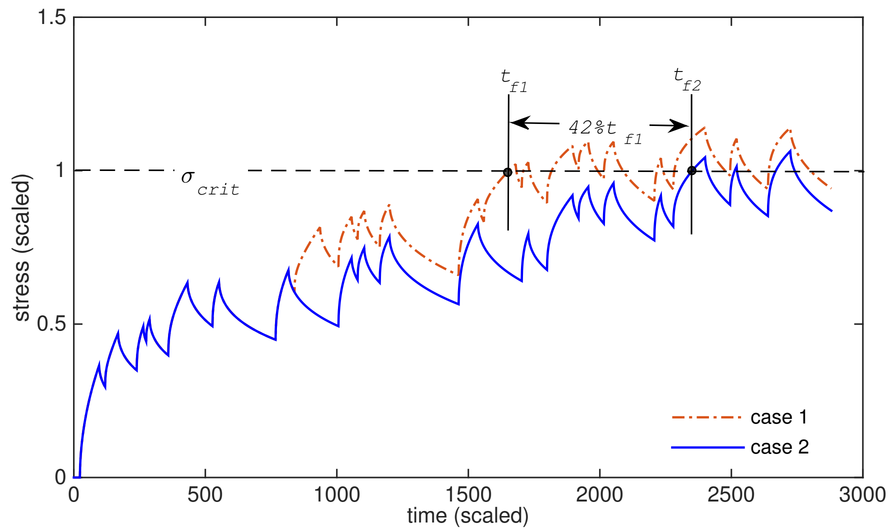
find that the interconnect lifetime in $case2$ can be extended to be 42% longer than that of $case1$ due to EM recovery during t_a and t_b as shown Fig. 4.14(b). For each CPU, if we can extend the power-off periods even longer or reduce the power-on periods while still maintain the performance requirement, we can achieve both energy saving and much longer lifetime (even immortal EM-induced life). As a result, the new EM recovery model can lead to more opportunities for system level reliability optimization or combined energy and reliability management and optimization.

4.6 Summary

In this chapter, we proposed the new model for EM-induced degradation, which for the first time accounts for the transient stress recovery effect. Nowadays the recovery effect becomes more significant and relevant due to available low power and energy optimization and management techniques at multiple system levels. The new dynamic model is based on the direct analytical solution of the Korhonen's equation with arbitrary unipolar or bipolar current loads at varying temperatures. We have demonstrated that the recovery effect can be quite significant even under time-dependent unidirectional current loads. Large difference in current densities and high temperature during the healing process will lead to a more complete recovery. Such effect can be further leveraged to extend the lifetime of the on-chip interconnect if the driving powers will be properly controlled and managed at the run time. Our numerical results show that the results generated by the proposed analytical model agree well with the numerical analysis results under any time-varying current densities and temperature profiles. Potential applications of the proposed model have been demonstrated.



(a)



(b)

Figure 4.14: (a) Two cases of the power trace for Xeon node and (b) the resulting hydrostatic stress evolution kinetics in the interconnect, where current density is assumed to be $4 \times 10^9 A/m^2$.

Chapter 5

Physics-Based Full-Chip TDDB Assessment for BEOL Interconnects

This chapter presents a novel approach, techniques, and flow for the physics-based chip-scale assessment of backend low-k TDDB. Instead of using the widely accepted across-layout electrostatic field based TDDB assessment, we consider the breakdown development as the complementary combination of electric current path generation by means of diffusing metal ions and field-based hoping conductivity of the current carriers.

We use FEA-based simulations for populating the set of lookup tables, which provide a time to breakdown for any interconnect pattern with given geometries and voltages. Besides, we use a pattern-matching technique for extracting from the layout all patterns belonging to different classes of pattern shapes with different geometries, locations and

electric loads.

5.1 Introduction

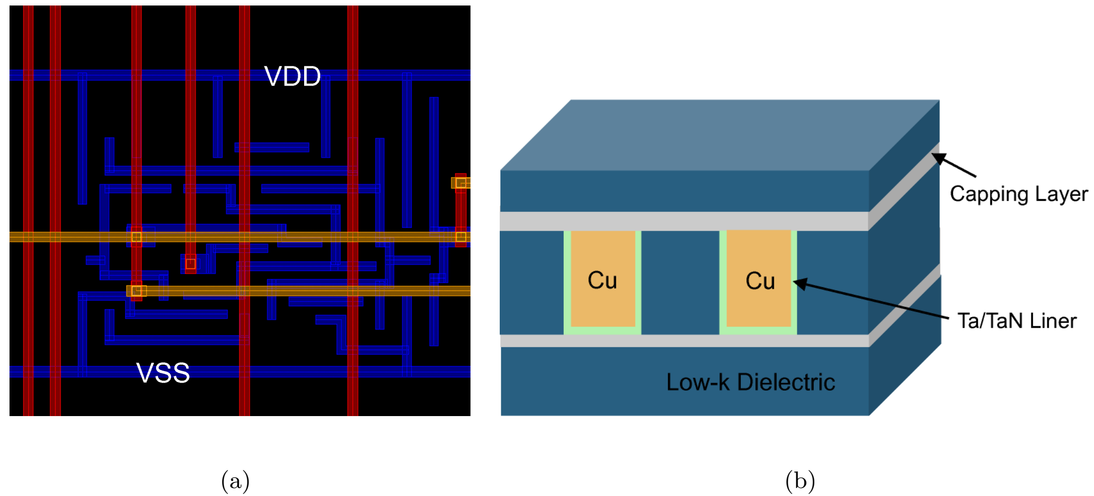
Great efforts have been made to model TDDB degradation, for instance [67–71]:

- E model: $TTF \propto exp(-\gamma E)$
- $1/E$ model: $TTF \propto exp(G/E)$
- power-law model: $TTF \propto E^{-m}$
- $\sqrt{E}$ model: $TTF \propto exp(-\beta sqrt(E))$

Where γ, G, m and β are generally referred as field acceleration parameters. However, there is still no universal agreement between the proposed field acceleration models which are based on different physical breakdown mechanisms [67]. The underlying physics of the dielectric breakdown is still not completely defined. The frequently employed the thermo-chemical E model [68] and $1/E$ model [69] were initially developed for gate oxides, where the E model describes weak bond breakage due to thermo-chemical heating and the $1/E$ model refers to high energy hole injection induced damage. The power-law model refers to hydrogen-induced defects and it was proposed for ultra-thin gate oxides ($< 4nm$). The E model and $1/E$ model were later examined toward extension on the copper/low-k interconnect TDDB. The major difference between TDDB in low-k BEOL dielectrics and gate oxides is the presence of metal ions in the former interior. Accordingly, the $\sqrt{E}$ model was first proposed for metal-SiN-metal capacitors [70], and further employed for the low-k TDDB, assuming that the copper ions play a major role in dielectric breakdown, by Chen

and Suzumura *et al.* [71, 72]. Lately, the experimental data collected at the low fields have demonstrated the overly conservative predictions generated by the E model, and too optimistic predictions with the $1/E$ model [67]. In addition, as it was mentioned in [67], the breakdown event depends on the formation of the conducting path of traps connecting the two electrodes (metal lines). However, all proposed TDDB models fail to describe the kinetics of conduction path generation. Majority of currently employed TDDB assessment approaches are based on calculations of the across-layout electrostatic fields and, thus, cannot provide any kind of the interconnect lifetime assessment. Therefore, the development of the backend low-k interconnect TDDB TTF assessment flow is still not addressed task.

A robust full-chip assessment technique for low-k TDDB is needed for evaluating the amount of the IMD degradation, measured by the leakage current density, and the MTTF during the circuit design. As shown in Fig. 5.1(a), the copper/low-k dielectric structures are characterized by a wide variety of geometries. The architecture of a metal line, which is comprised of the capping (etch stop) layer, and the diffusion barrier coating the copper bulk shown in Fig. 5.1(b), may impact the TDDB-induced interconnect lifetime. Distribution of the electric field in IMD gaps effects both the kinetics of the current conducting path generation and the resulting leakage current density. Bashir *et al.*, [73], have assumed a fixed voltage drop between all neighboring metal segments in the proposed full-chip TDDB simulator. However, interconnects in the chip can be categorized as power/ground lines and signal lines. Patterns with the same geometries but different power/ground/signal line combinations, e.g. with the different electric loads, will be characterized by different TDDB activities. Thus, the method proposed in [73] will induce



(a) (b)

Figure 5.1: Layout of on-chip interconnects (blue line: M1, red line: M2, and yellow lines: M3), (a), and cross section of copper/low-k dielectric structure, (b).

too conservative results. Novel solutions should be developed to mitigate the mentioned problems for full-chip TDDB assessment.

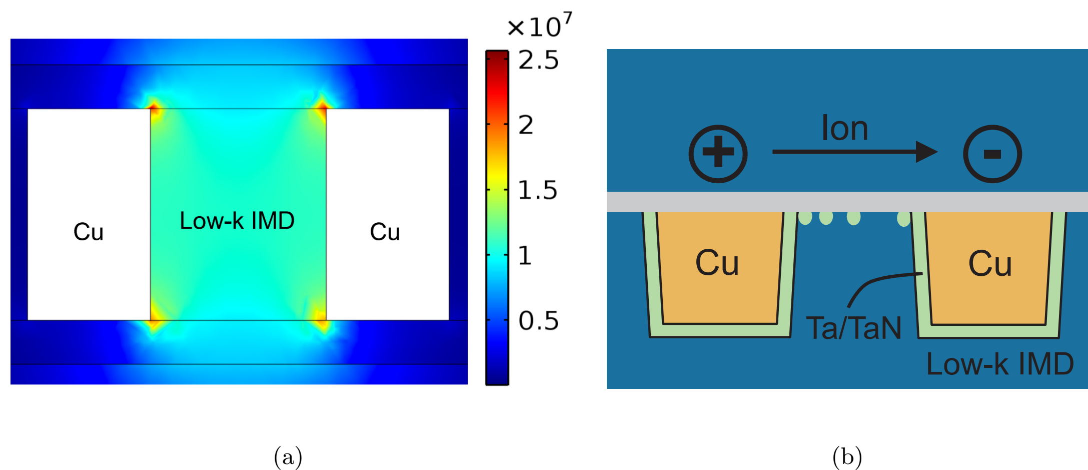
The reminder of the chapter is organized as follows: Section 5.2 introduces the new physics-based TDDB modeling method for low-k BEOL stack, including the model for electric current path generation, the expression for leakage current evolution, and the TDDB lifetime model. Section 5.3 presents the proposed new full-chip backend low-k TDDB analysis method based on the developed electric path generation model. In Section 3.3, a 32/28nm test chip is used as case example to demonstrate the full-chip analysis flow. Section 5.5 concludes this chapter.

5.2 Physics-based TDDB model for low-k BEOL stack

5.2.1 The model for electric path generation

Inter-layer dielectric (ILD) and inter-metal dielectric (IMD) are the two types of low-k dielectrics, which represent, respectively, the isolation between two metal layers and between metal lines in the same layer. Because the thickness of ILD is generally larger than the metal lines space, we focus on the breakdown of dielectrics between metal lines located in the same layer. Fig. 5.1(b) shows a cross section of the typical copper/low-k dielectric structure with two parallel metal lines. The experiments demonstrate that TDDB failures take place mostly at the interface between the capping layer and the low-k dielectrics [74, 75]. The 3-D simulation of the distribution of electrostatic field in the geometry shown in Fig. 5.1(b) with the COMSOL Multiphysics FEA tool, demonstrates the electric field enhancement near the cap/IMD interface, Fig. 5.2(a). Besides, the ions are reported to diffuse much faster at the interface than in the bulk dielectric, as shown in Fig. 5.2(b), which is possibly due to the defects generated at the surface during CMP process, [75]. Based on these findings, in the following analysis we consider 2D diffusion of the metal ions along the cap/IMD interface between the oppositely charged metal lines.

The effect of copper ions on the intra line leakage is debated in the literature. Recently, a number of experimental results have reported that Cu can hardly diffuse out of the Ta/TaN barrier under chip operating conditions [6, 74, 76]. Instead, Ta ion diffusion has been observed in the low-k materials. The diffusion of metal ions can generate defects in the dielectric serving as potential centers for localization of the electrons coming from the metal electrodes. An electric conductivity is represented by electron jumps between neighboring



(a) (b)

Figure 5.2: Cross section of copper/low-k dielectric structure: (a) Result of 3D FEA simulation for the electric field (V/m) distribution in IMD between parallel metal lines with $spacing = 100nm$ and $\Delta V = 1.1V$ and (b) ion migration along the cap/IMD interface.

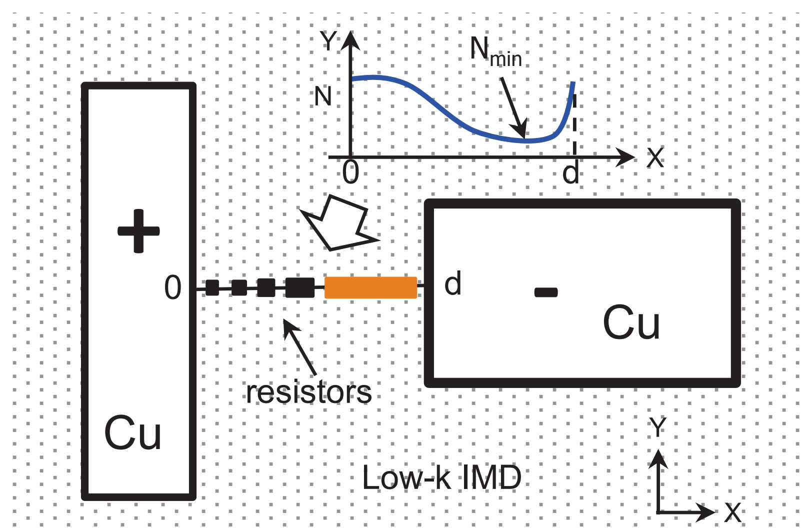


Figure 5.3: Ion concentrations and the corresponding resistors in IMD along $(0, d)$.

centers (hoping conductivity). A local conductivity is proportional to the probability of the electron jumping between the neighbor centers, which exponentially depends on the

distance between the centers [77]:

$$\sigma_{ij} \sim \Gamma_{ij} = \gamma_{ij}^{0} exp \left\{ -\frac{-2r_{ij}}{a} - \frac{\varepsilon_{ij}}{k_B T} \right\} \tag{5.1}$$

Here, r_{ij} is the distance between i and j centers, a is the radius of electron localization at this type of centers (analog of the Bohr's radius), which can reach $100 \mathring{A}$, ε_{ij} is the energy barrier between centers, $k_B T$ is the thermal energy. All connected centers form the resistors network, with the resistor between i and j centers equals to

$$R_{ij} = R_{ij}^{0} exp \left\{ \frac{-2r_{ij}}{a} + \frac{\varepsilon_{ij}}{k_B T} \right\} \tag{5.2}$$

In a 2D system, the distance r_{ij} is determined by:

$$r_{ij} = \sqrt{N(x, y, t)} \tag{5.3}$$

where $N(x, y, t)$ is the ion concentration at the considered interface. Fig. 5.3 shows the schematics of the distribution of ion concentration and corresponding resistor network at an arbitrary instant in time in IMD along a path $(0, d)$ connecting metal electrodes. It is clear that electrons moving from the cathode to anode will meet the biggest resistors at the locations characterized by the largest distances between centers. Since the difference in the distances between centers results an exponentially large difference in the resistors, it is reasonable to conclude that the total resistance of the path $(0, d)$ depends on the largest resistor, i.e. the minimum ion concentration. The distribution of the normalized ion concentration $N_{\text{norm}}(x, y, t) = N(x, y, t)/N_0$ is governed by the diffusion of ions in an electric field [78]:

$$\frac{\partial N_{\text{norm}}}{\partial t} = -\nabla J \tag{5.4}$$

$$J = -D\nabla N_{\text{norm}} + \frac{qDEN_{\text{norm}}}{k_B T} \quad (5.5)$$

with boundary conditions:

$$N_{\text{norm}}(x=0) = N_{\text{norm}}(x=d) = 1 \quad (5.6)$$

Here J is the metal flux, $D = D_0 exp(-Ea/k_B T)$ is the diffusion coefficient, Ea is the activation energy for metal ion diffusion, k_B is the Boltzmann constant, T is the temperature, q is the electric charge and E is the electric field.

Table 5.1: Parameters used in FEA simulation

Parameter	Value	Parameter	Value
D_0	2×10^{-11}m^2/s	E_a	0.9eV
k	2.9	k_B	1.38×10^{-23}J/K
T	333K	V_{DD}	1.1V

Metal line structure shown in Fig. 5.3 is used as an example for simulating the electric path generation. Time-dependent distribution of the metal ions is obtained from the COMSOL-based solution of the coupled electric field and diffusion equations (5.4)-(5.6). The employed parameter values are listed in Table 5.1. Before applying the electric field stressing, the metal atoms are allowed to diffuse into the dielectric for a short period of time at high temperatures (T=400K and t=1e5s in this case). This step should mimic the atomic thermal diffusion, which occurs at the high temperature processing steps including annealing. The simulation results are demonstrated in Fig. 5.4 and Fig. 5.5. Fig. 5.4(a)-Fig. 5.4(c) show the contour lines representing the evolution of the concentration field $N_{\text{norm}}(x, y, t)$ at three instances in time: before a continuous chain of ions characterized

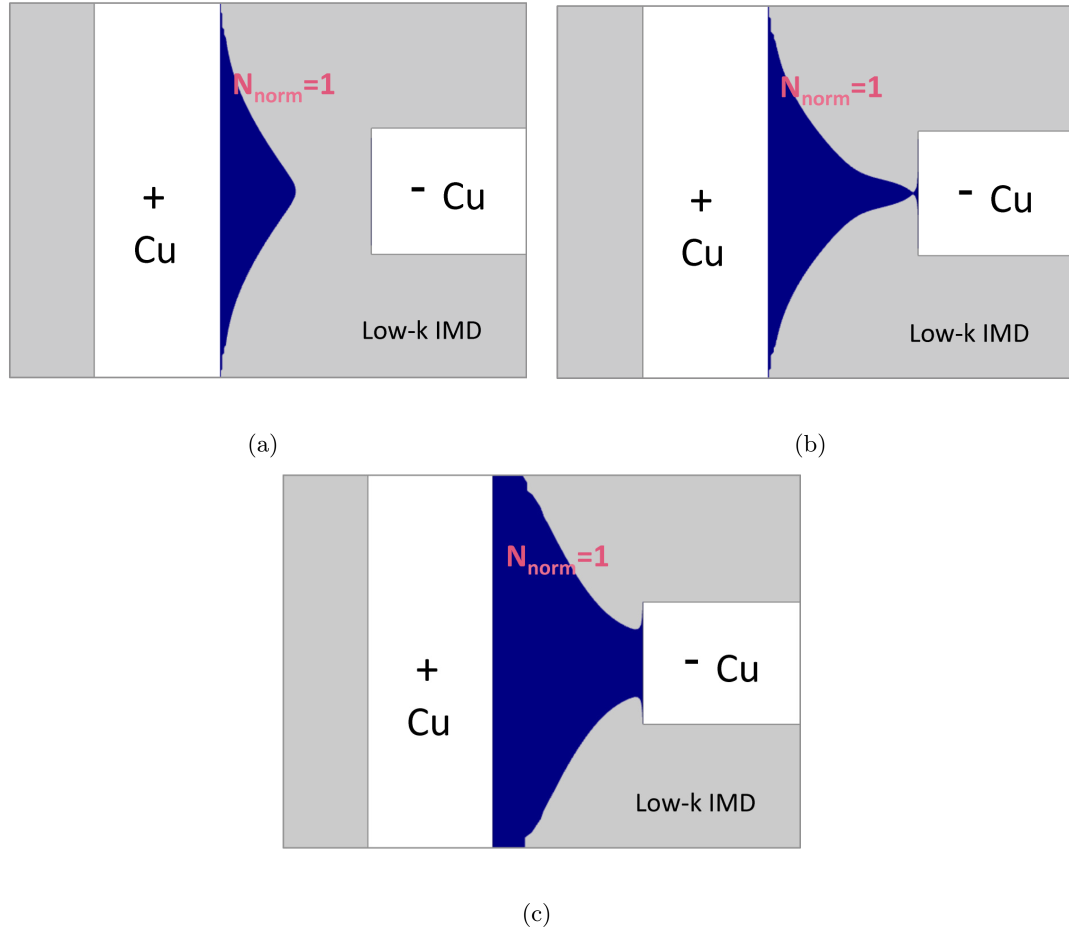
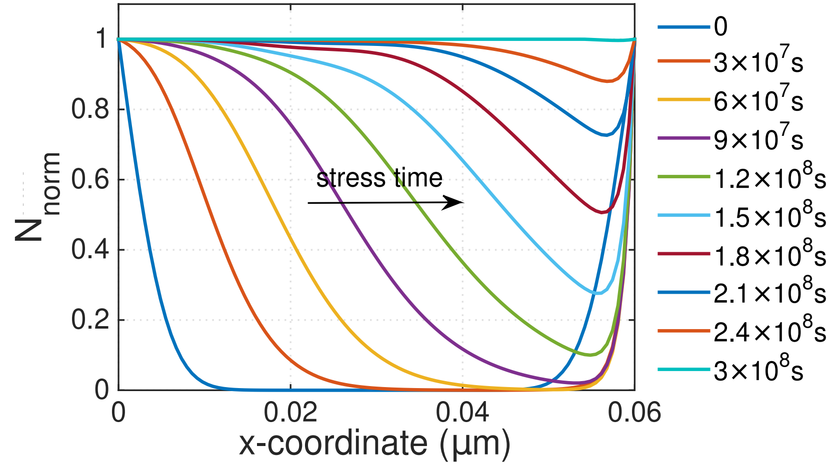
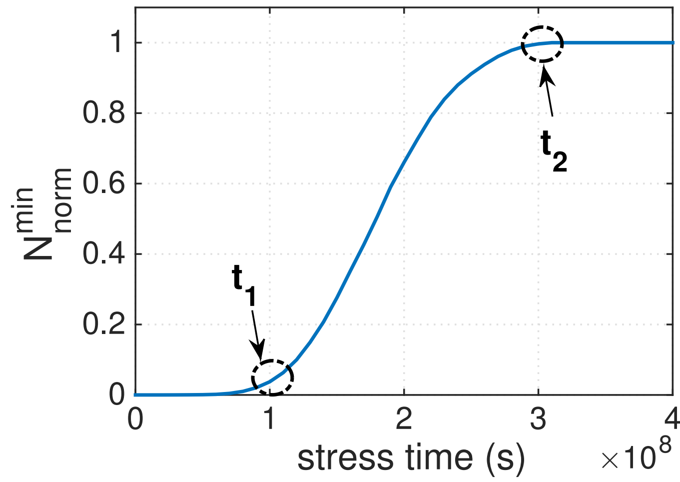


Figure 5.4: FEA simulation results of contour shapes for normalized ion concentration $N_{\mathrm{norm}} = 1$ in IMD between electrodes at different instants in time (a)-(c), with line spacing $d = 60nm$, $V(x=0) = V_{\mathrm{DD}}$, and $V(x=d) = 0$.

by the minimum spacing (N_{norm}=1) is formed between metal lines, at the moment when this chain is formed for the first time, and at longer time when the area with N_{norm}=1 is expanded along the anode edge. Evolution of the ion distribution along the fastest diffusion path, which is the path connecting the centers of the neighboring metal lines, is shown in Fig. 5.5(a). It can be seen that the initial ion distribution, which was resulted by the thermal diffusion, is shifting as a whole with the duration of time toward the anode keeping unchanged the minimum concentration $N_{\mathrm{norm}}^{\mathrm{min}}$, which is determined by the most separated



(a)



(b)

Figure 5.5: FEA simulation results of changes in ion concentration distribution in IMD along the fastest diffusion path with time, (a), and corresponding time dependent minimum ion concentration, (b), with line spacing $d = 60nm$, $V(x = 0) = V_{\mathrm{DD}}$, and $V(x = d) = 0$.

ions. Simultaneously, the increasingly larger area is occupied with the closed packed ions: N_{norm}=1. It lasts until the instance in time when the region with $N_{\mathrm{norm}}^{\mathrm{min}}$=1 reaches the vicinity of anode edge. Starting this moment t_1 the minimum concentration starts to increase drastically. Finally, the ion concentration becomes uniformly distributed with

N_{norm}=1 between the electrodes. Based on this observation, we introduce two important time instances $\boldsymbol{t_1}$ and $\boldsymbol{t_2}$, Fig. 5.5(b):

- $\boldsymbol{t_1}$: The instance in time when $N_{\text{norm}}^{\text{min}}$ starts to increase (drastically).
- $\boldsymbol{t_2}$ (TTF): The instance in time when $N_{\text{norm}}^{\text{min}}$ reached 1 and the resistivity is uniformly distributed between electrodes.

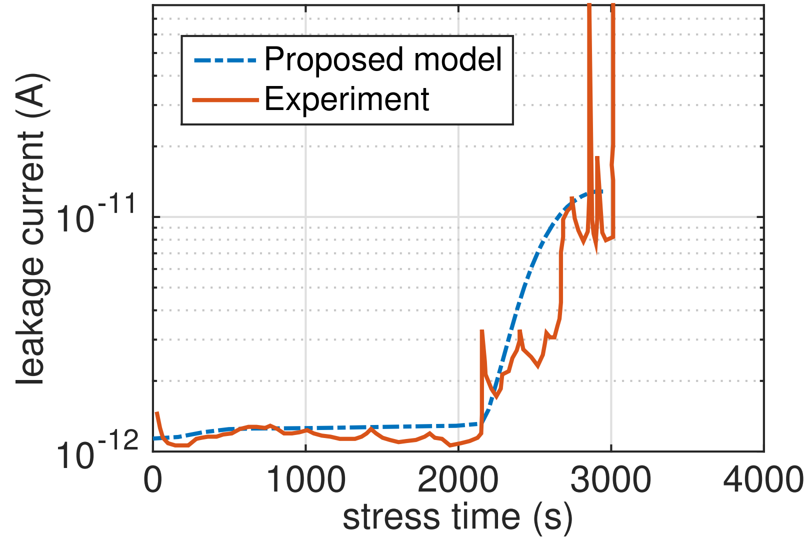
Since the largest resistor, corresponding to $N_{\text{norm}}^{\text{min}}$, dominates the total resistance of the leakage path, the dielectric will start to degrade from t_1, leading to significant increase in leakage current. After the instance in time t_2, other mechanisms governed by excessive Joule heating will generate the catastrophic dielectric failure. Therefore, the instance in time t_2 represents the TTF of the low-k dielectric in this particular metal gap.

5.2.2 Model calibration

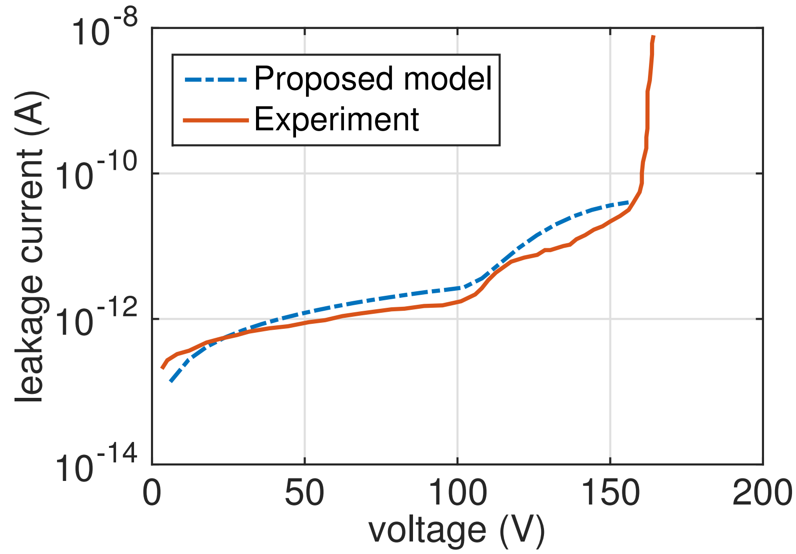
The developed model of the electric path generation and evolution allows to come out with the formalism of the leakage current evolution. As it was mentioned above the neighboring ions characterized by the largest separation provides the largest "resistivity" for the electrons hopping between metal ions. Assuming that the potential barriers between neighboring centers do not depend on the distance between them ($\varepsilon_{ij} = \varepsilon$), and accepting the Poole-Frenkel mechanism of the field-induced barrier lowering, we can derive the expression for the current density evolution:

$$j(t) = j_0 E exp\left\{-\frac{2}{a\sqrt{N_{\text{min}}^{\text{min}}(t)\cdot N_0}} - \frac{\varepsilon - q\sqrt{qE/(\pi\varepsilon_{\text{perm}})}}{k_B T}\right\} \tag{5.7}$$

Here, $\varepsilon_{\text{perm}}$ is the dielectric dynamic permittivity.



(a)



(b)

Figure 5.6: Current-voltage leakage characteristics for constant voltage (TDDB) stress, (a), and ramped voltage stress, (b), with experimental data from [6].

The total leakage current can be obtained by integration of leakage current density over the whole shape contour. Due to the limited space of the conference paper, the details

of the leakage analysis and corresponding calibration of the model will be discussed in the journal version of this paper. For now we just mention that the leakage currents calculated with the calibrated model demonstrate good agreement with experimental results, Fig. 5.6. It should be mentioned that the model should be calibrated with a set of test structures just once per the technology node and foundry.

5.2.3 TDDB lifetime model

We next extract the dependence of TDDB lifetime on electric field based on the numerical results. As shown in Fig. 5.7 a power-law trend shows the best fit:

$$TTF = \alpha(T) \cdot E^{-\beta(T)} \tag{5.8}$$

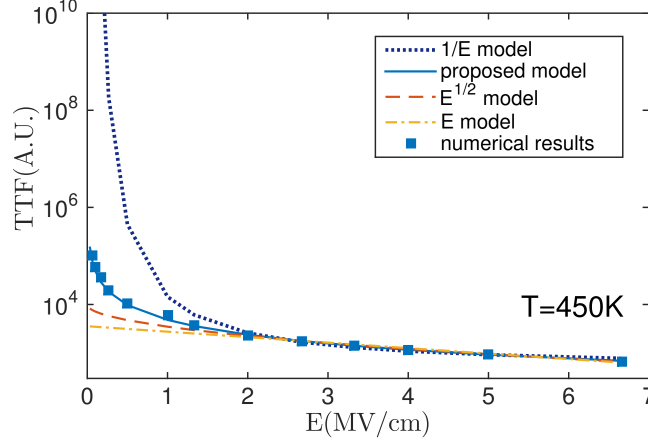


Figure 5.7: Layout of *ChipTop* architecture.

The values of α and β at different temperatures are listed in Table 5.2, indicating that both α and the field acceleration parameter β are functions of temperature. Higher temperature leads to a shorter TTF. This can be explained by faster metal ion migration at higher temperatures. It should be noted that the power-law model proposed for ultra

thin gate oxide is based on a different dielectric breakdown mechanism, where the field acceleration parameter is independent on temperature. The extracted power-law model for low-k TDDB agrees with the conclusion obtained from a number of experimental results [79].

Table 5.2: Parameters used in TDDB lifetime model

Temperature (K)	α	β
350	$1e^{3}4.36$	1.096
400	$1e^{3}1.62$	1.118
450	$1e^{2}9.57$	1.139

5.3 New full-chip backend low-k TDDB analysis

In this section, we present the proposed new full-chip backend low-k TDDB analysis method based on the developed electric path generation model. Fig. 5.8 illustrates the analysis flow, which can be achieved through two major steps: one is the generation of lookup tables that provide TTF for any interconnect pattern with given geometries and voltages; another is the pattern matching step that extracts all patterns of interest from the layout along with their geometrical and electrical characteristics. The TDDB induced chip lifetime is then determined by the minimum TTF of all analyzed matched patterns. The details are discussed in the following subsections.

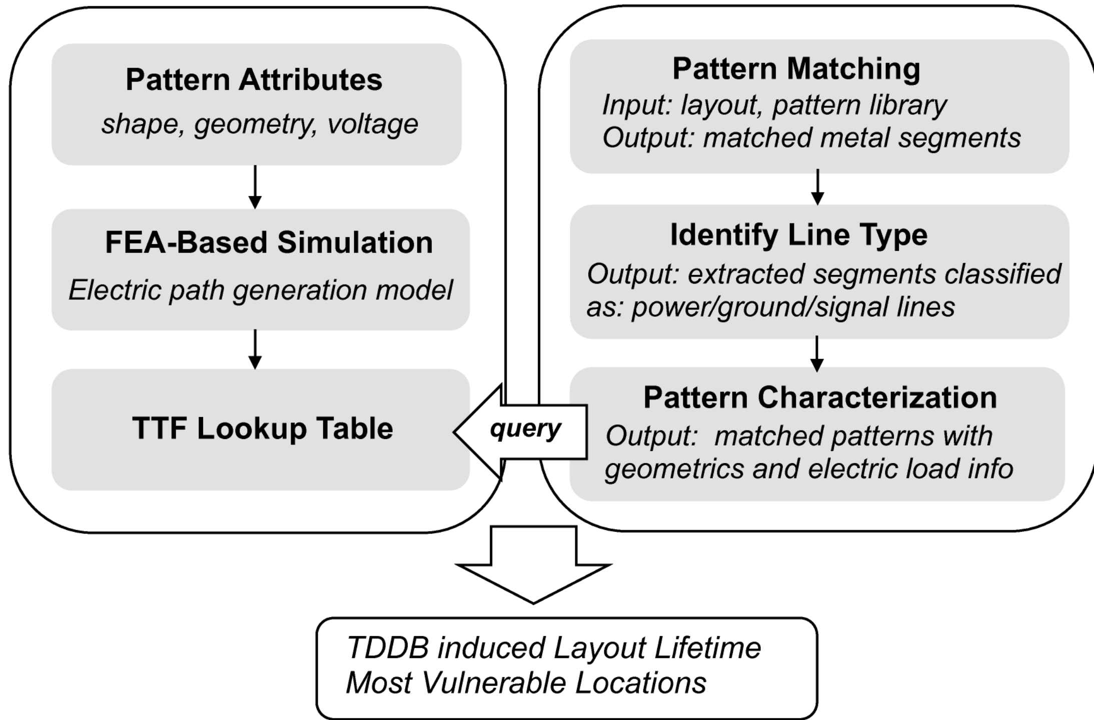


Figure 5.8: Chip-scale TDDB analysis flow for backend low-k dielectrics.

5.3.1 Impact of electric load

In this subsection, we discuss the impact of electric loads on low-k dielectric reliability. Interconnects in the integrated circuits are serving as power/ground lines or signal lines. As a result, the interconnect patterns can be characterized by different kind of electric loads according to the following three combinations:

1. **Power, Ground**: As shown in Fig. 5.9(a) and Fig. 5.9(e), the dielectric will be stressed with a constant electric field.

2. **Power/Ground, Signal**: Fig. 5.9(b) and Fig. 5.9(c) are the schematics of the corresponding voltage waveforms, resulting in a time-dependent electric field in IMD, Fig.5.9(f).

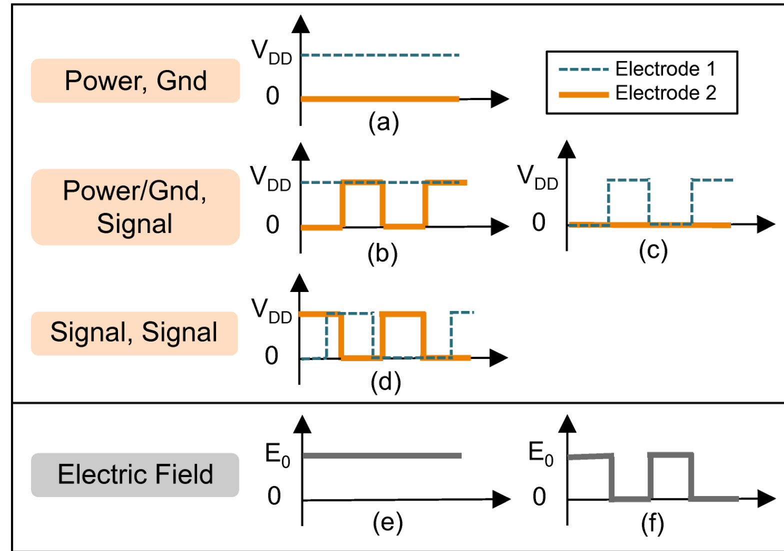


Figure 5.9: Schematics of different voltage waveforms on two electrodes and the corresponding electric field (assume a uniform field).

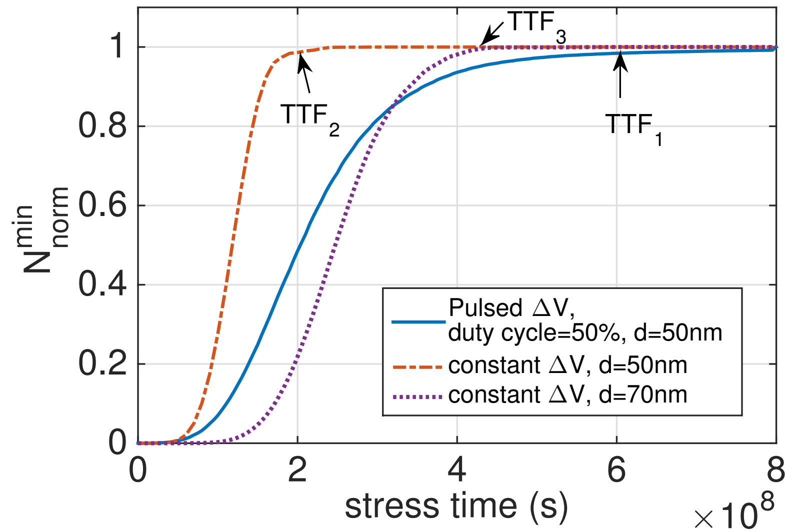


Figure 5.10: Comparisons of kinetics of $N^{\mathrm{min}}_{\mathrm{norm}}$ evolution in IMD between: 1: line spacing $d = 50nm$, pulsed ΔV with duty cycle $= 50\%$ and amplitudes=V_{DD}, 2: $d = 50nm$ and constant $\Delta V = V_{DD}$, 3: $d = 70nm$ and constant $\Delta V = V_{\mathrm{DD}}$

3. **Signal, Signal**: According to Fig. 5.9(d), in general cases, the electric fields between neighboring signal lines are time-dependent waveforms similar to Fig. 5.9(f). A special

case that much less likely to happen is the voltage waveforms in Fig. 5.9(d) are totally opposite, leading to a constant electric field.

Taking, for example, the structure shown in Fig. 5.3, and selecting line spacing as d=50nm and d=70nm we will analyze the kinetics of $N_{\rm norm}^{\rm min}$ evolution in the IMD gap, loaded with a constant voltage drop or a pulsed voltage drop with a duty cycle=50%. We can observe from Fig. 5.10 that when the patterns have the same geometries, the flux of metal ions, Eq. (2.24), is larger in the case of the constant electric stress, which leads to faster $N_{\rm norm}^{\rm min}$ evolution, and thus to a shorter TTF ($TTF_1 \approx 3 \times TTF_2$). Besides, when the patterns are stressed with the same voltages, a smaller line spacing results in a shorter TTF ($TTF_3 \approx 2 \times TTF_2$). However, under some circumstances, a pattern with a larger spacing and constant electric stress may have a shorter TTF than the pattern with a smaller spacing but loaded with the time-dependent voltage ($TTF_1 \approx 1.5 \times TTF_3$). Hence, when analyzing dielectric reliability of IC chips, we need to pay attention to the patterns characterizing by both: the relatively small metal line spacing and constant voltage electric stressing. Note, that the patterns carrying the same voltages, for example $V_{\rm DD}$, should be excluded from the analysis. Therefore in the chip-scale low-k TDDB analysis, an attribute of electric loads, in addition to geometries, needs to be added to the extracted patterns. In contrast, existing method assuming a fixed voltage drop between all neighboring metal segments in the layout will generate very conservative results and can probably incorrectly detect the most vulnerable locations.

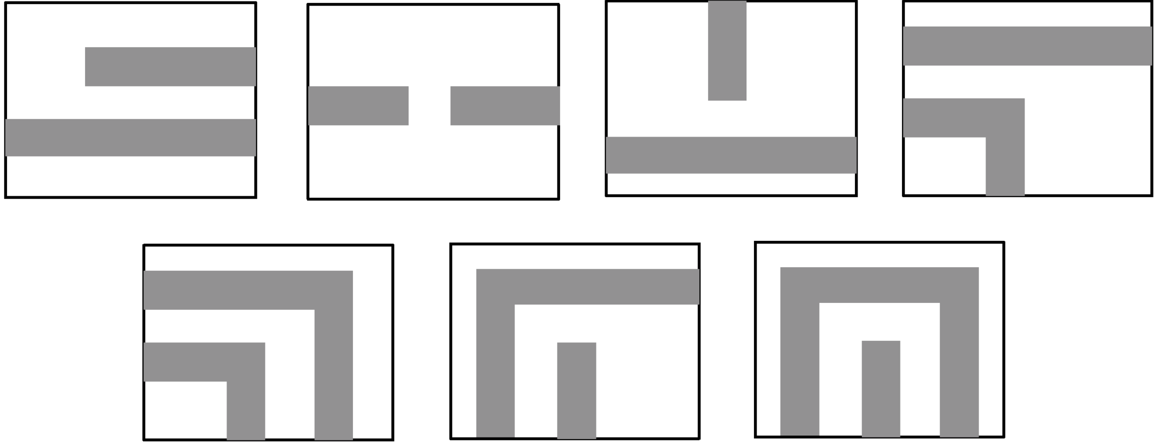


Figure 5.11: Example of different pattern shapes.

5.3.2 Time-to-failure lookup table

As demonstrated in the Fig. 5.1(a), the backend interconnects are characterized by a variety of shapes and sizes. In this work, we consider interconnects as groups of patterns belonging to different classes of frequently used layout pattern shapes. Thus, the full-chip reliability analysis can be carried out by independently evaluating the dielectric breakdown of interconnect patterns existed in the layout. The minimum pattern failure time provides the lifetime of the chip due to TDDB, as a short-circuit is generated after the dielectric breakdown. In this case, lookup tables need to be generated, in advance for each technology node, for the TTF of a large number of interconnect patterns with given geometries and voltages, so that a corresponding TTF can be linked to each pattern. Fig 5.11 shows the example of pattern shapes considered in this work. As it was discussed above, each type of the topologically similar patterns but characterizing by different inter-metal spacing is a subject of the FEA-based extraction of t_1 and t_2 instances in time. The calculated TTF

are used for populating the set of corresponding lookup tables.

5.3.3 Pattern-matching method

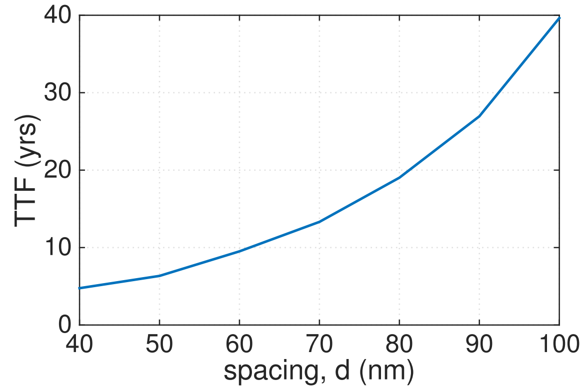


Figure 5.12: TTF of low-k dielectrics for different line spacing under $\Delta V = V_{\mathrm{DD}}$

This subsection describes the pattern-matching technique followed by the extraction of geometrical and electrical information for each pattern. This process includes following four steps, where the first three steps are carried out by the *Calibre Pattern Matching* integrated with the *Calibre nmDRC*:

1. **Build pattern library:** The pattern library is generated as an input of pattern matching for the frequently used classes of patterns demonstrated in Fig. 5.11. For each kind of pattern, we vary wire width, length, and spacing within the designed ranges, so that all patterns of interest can be extracted from the layout. Fig. 5.12 shows the exponential dependence of TTF on spacing when the constant electric stressing is applied, which indicates that the patterns having negligible impact on the chip lifetime can be excluded from analysis in order to reduce database size, as the patterns with the spacing $d>90nm$ in this case.

2. **Pattern matching:** The *Calibre Pattern Matching* tool is employed to recognize the layout patterns defined in the library. The output is sets of metal segments for matched patterns. Each segment is a group of edges described by pairs of vertices that can reflect the shape and location of the pattern.

3. **Identify line type**: The extracted metal segments are then identified based on their electric functions as *power lines*, *ground lines*, and *signal lines* using the *nmDRC* platform.

4. **Pattern characterization:** As the pattern-matching step generates sets of segments that belong to all recognized patterns, in order to get the information of each pattern, we need to figure out which segments build a pattern. It can be realized by generating the polygons that represent the tightest boundary of each matched pattern during the pattern recognition, so that the interconnect segments locate in the same boundary form a pattern and determine the geometry, location, and voltage load of the pattern.

5.4 Experimental results

In our experiments, we use a low power design named *ChipTop* as the test case. *ChipTop* is a processor architecture, which contains cache blocks, I/O standard cells and digital standard cells. It is synthesized using *Synopsys Design Compiler*, and is placed and routed with *Synopsys* 32/28*nm Generic Library* [80] using *Synopsys IC Compiler*. The layout of the chip is shown in Fig. 5.13.

Table 5.3 lists the minimum spacing for interconnect patterns on M1, M2 and M3 layers and the corresponding electric function of the lines belonging to these minimum

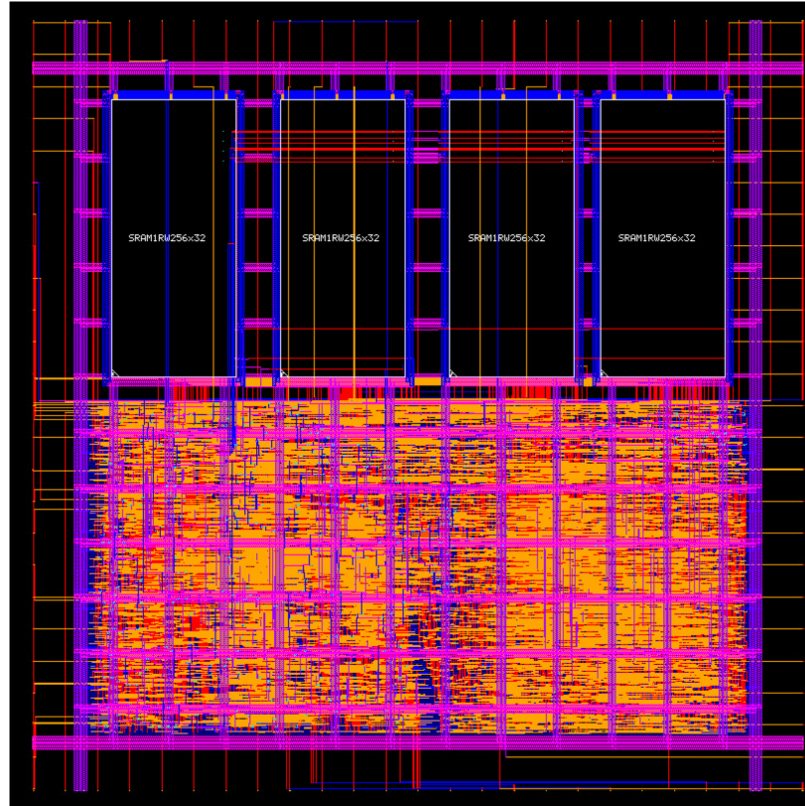
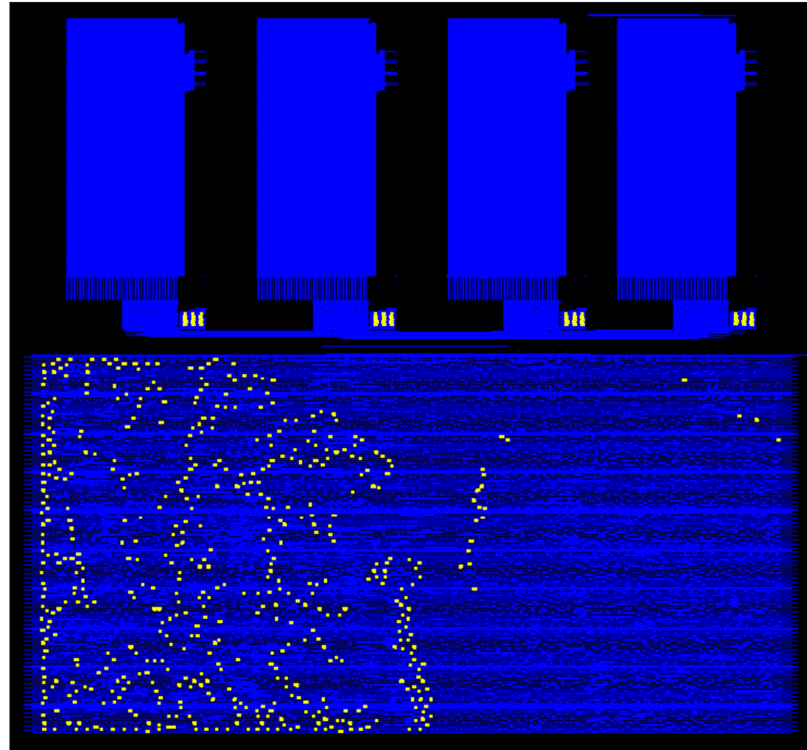


Figure 5.13: Layout of *ChipTop* architecture.

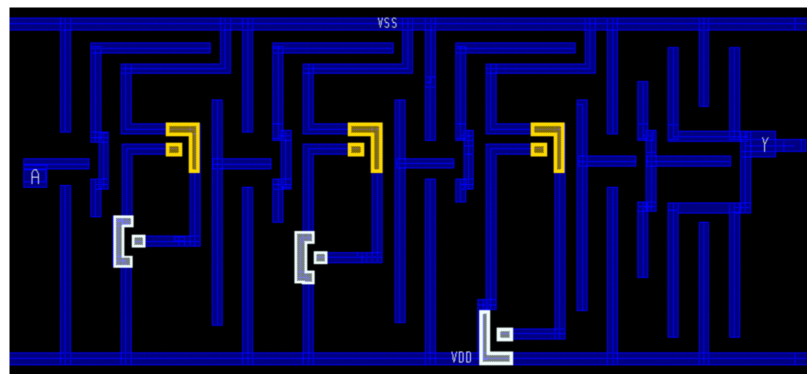
Table 5.3: Minimum spacing and line types of corresponding interconnect patterns

Metal layer	Spacing	Line type
$M1$	50nm	power/ground/signal
$M2$	64nm	signal
$M3$	67nm	signal

spacing patterns. The spacing between interconnects in higher metal layers are much larger than $100nm$, thus according to Fig. 5.12, these layers can be removed from the TDDB assessment. It can be seen from Table 5.3 that the M1 metal patterns characterized by the minimum spacing are composed of the power lines, ground lines and signal lines, while



(a)



(b)

Figure 5.14: (a) The most vulnerable (yellow dots) locations in M1 layer (blue); (b) zoom in image of the critical shapes in a delay cell (yellow: worst case; white: TTF comparable to the worst case).

the M2 and M3 patterns are composed of signal lines only. We specify the geometries and electric loads of the extracted interconnect patterns and rank their TTFs according to

the TTF lookup table. The minimum TTF of these patterns is around 6.5 years, which determines the low-k TDDB induced lifetime of the chip.

The most vulnerable pattern consists of a power line and a ground line, thus, it is stressed by the constant voltage, and has the minimum allowed line spacing of d=50nm. Other patterns with minimum line spacing but stressed with the pulsed voltage have the much longer TTFs. All these most critical patterns are located in M1 layer and their distribution is demonstrated in Fig. 5.14(a). Specifically, we have found that all these shapes come from the delay cells: $DELLN1X2_RVT$, $DELLN2X2_RVT$, and $DELLN3X2_RVT$ in the standard cell library, [80]. Fig. 5.14(b) shows a zoom-in image of the critical M1 patterns in the $DELLN2X2_RVT$ cell. These detected most leaking paths in the cell indicate the places where one can do optimization, by, for instance, increasing spacing between electrodes.

5.5 Summary

In this chapter, we have proposed a new physics-based TDDB modeling and assessment method and implemented it for the copper/low-k interconnects of VLSI chips. The new TDDB model accounts for the kinetics of electric current path generation and evolution in the IMD gap where the evolution of minimum metal ion concentration determines the TTF of the low-k dielectric. The proposed conduction path generation model along with the assumption of the field-based hoping conductivity of the current carriers results in a formalism of the leakage current evolution that can be calibrated with experimental results. A power-law model can best describe the dependence of TDDB lifetime on electric field.

For the chip-scale low-k TDDB assessment the FEA-based simulation of the TTF for any layout pattern with different geometries and voltages are employed in order to generate the lookup tables. All patterns of interest are extracted from the layout using pattern-matching technique. Obtained experimental results demonstrate capability of the proposed method to predict the TDDB induced chip lifetime and detect the locations in the layout that are most vulnerable to TDDB failure. The proposed assessment flow can be employed in the reliability-aware circuit design.

Chapter 6

Conclusion

With the continuous technology scaling, Electromigration (EM) has become a major design constraint in nanometer VLSI circuits and the time-dependent-dielectric-breakdown (TDDB) effect, after EM, is playing a more important role in interconnect reliability. Reliability signoff based on traditional assessment techniques is becoming more difficult due to the increasing complexity of modern VLSI designs, which demands new, physics-based models and analysis methodologies for designers to alleviate the reliability threats. In this dissertation, we propose the new physical modeling method and on the basis of it we develop new methodologies for chip-scale EM and TDDB assessment. In this chapter, the main contributions of the thesis are summarized.

6.1 Summary of research contributions

6.1.1 Physics-based EM modeling

Chapter 2 reviews the EM fundamentals and shows the the development of physics-based EM models for void nucleation and growth. The FEA analysis of EM-induced failure of confined metal lines, which models redistribution of metal lattice vacancies taking place under electric stressing with accounted equilibration of local vacancy concentration with stress, is performed to show additional support to the developed anaytical models. The proposed models account the statistical nature of the EM phenomenon due to a random grain size distribution. Also, the thermal and other process-induced residual stresses which have been ignored by the Black's equation based EM assessment, are considered in the models. We derive the analytical solution to the continuity equation describing both the pre-voiding and the post-voiding stress evolution kinetics in the confined metal line. And we further extract the nucleation time from the obtained pre-voiding stress evolution equation. We compare the growth kinetics of the current nucleated void with the kinetics of the void growth caused by the electric current-induced evolution of the preexisted void. The results show that the initial void growth in the former case does not depend on the current density. For the application in nanometer VLSI circuits, we developed a technique that allows to assess the hydrostatic stress evolution inside a multi-branch interconnect tree for more accurate prediction of the TTF.

6.1.2 Full-chip EM assessment

In Chapter 3, we have proposed a new EM assessment approach for power delivery networks of VLSI systems. Instead of considering the failure of a single interconnect branch, we consider the failure criterion as the increase in the voltage drop above the threshold level, caused by the EM-induced resistance increase of the individual branches. The new approach takes full account of essential redundancy for current delivery existing in the P/G networks. The new method calculates the EM-induced resistance increase of the individual branches in terms of the developed physics-based formalism for void nucleation and growth, where the hydrostatic stress and void nucleation time are calculated on the basis of multi-branch interconnect trees, which allows to avoid over optimistic prediction of the TTF made with the Black-Blech based methods for individual branches of an interconnect tree. The P/G networks are modeled as time-varying linear networks, which is solved in the EM-time scale to estimate the time-varying voltage drops of P/G networks due to the EM effects over time and the resulting full-chip EM failure time. Experimental results show that the proposed method will lead to less conservative estimation of the lifetime than the existing Black-Blech based methods. The EM-induced failure is more likely to happen at the place where the hydrostatic stress and local temperature are large and is more likely to happen at longer times when the saturated void volume effect is taken into account. It also reveals that traditional assumption of the uniform average temperature leads to inaccurate predictions of the time-to-failure, while the consideration of thermal stress variation results in a retarded EM-induced degradation.

6.1.3 Dynamic EM modeling and recovery effect

Chapter 4 presents a new physics-based dynamic compact EM model for transient stress evolution under time-dependent current density and time-dependent temperature stressing, which is the first one that can correctly model the EM recovery effect. The new dynamic EM model is based on the direct analytical solution of one-dimensional Korhonen's equation with load driven by any unipolar or bipolar current waveforms under varying temperature. We show that the EM recovery effect can be quite significant even under unidirectional current loads. This recovery/healing process is sensitive to temperature, and higher temperatures lead to faster and more complete recovery. Such effect can be further exploited to extend the lifetime of the interconnect wires if the chip current or power can be properly regulated and managed. As a result, the new dynamic EM model can be incorporated with existing dynamic thermal/power/reliability management and optimization approaches, devoted to reliability-aware optimization at multiple system levels (chip/server/rack/data centers). Presented results show that the proposed EM model agrees very well with the numerical analysis results under any time-varying current density and temperature profiles.

6.1.4 Low k TDDB modeling and full-chip assessment

In Chapter 5, we have proposed a novel approach for physics-based chip-scale assessment of backend low-k TDDB. We consider the breakdown development as the complementary combination of electric current path generation by means of diffusing metal ions and field-based hoping conductivity of the current carriers. It replaces the widely accepted

TDDB assessment which only considers the across-layout electrostatic field. As a result, the model generated TTF is governed by kinetics of the electric current path generation, which is controlled by a time-dependent minimum metal ion concentration in the IMD gap-fill. We perform FEA-based simulations to populate the set of lookup tables, which provide a time to breakdown for any interconnect pattern with given geometries and voltages. The pattern-matching technique is used for extracting from the layout all patterns belonging to different classes of pattern shapes with different geometries, locations and electric loads. The power-law TDDB lifetime model is extracted first time based on the based on proposed model, which agrees with the conclusion drawn from a number of experimental results. Experimental results obtained on a $32/28nm$ test chip show that upon the calibration the proposed flow provides a capability to evaluate chip-scale low-k TDDB reliability based on the calculated TTF and detect most leaking shapes in the layout.

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