Title
Doping Profile Engineering for Advanced Transistors

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Publication Date
2020

Peer reviewed|Thesis/dissertation

UNIVERSITY OF CALIFORNIA

Los Angeles

Doping Profile Engineering for Advanced Transistors

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in Electrical and Computer Engineering

by

Peng Lu

2020

ABSTRACT OF THE DISSERTATION

Doping Profile Engineering for Advanced Transistors

by

Peng Lu

Doctor of Philosophy in Electrical and Computer Engineering

University of California, Los Angeles, 2020

Professor Jason C. S. Woo, Chair

Over the last decades, conventional scaling (Moore's law) has provided continuous improvement in semiconductor device/circuit technology. FinFETs, featuring superior electrostatic control compared to planer FETs, have been the mainstream technology for the front-end-of-line (FEoL) application since the 22-nm node. Process-induced performance variation, which is already a key limit in 7/10-nm node FinFETs, is becoming even more severe in beyond 5-nm node. Furthermore, FinFETs' analog/RF performances are inferior to those in bulk and SOI transistors, preventing their applications in the system on chip (SoC) designs. In this work, 3D source/drain extension (SDE) doping profile control technique, developed for I_{ON}/I_{OFF} enhancement in 7/10-nm node FinFET, is proposed as an effective method for variability

suppression and digital/analog performance enhancement in the 3-nm node. The methodology of 3D doping profile optimization and governing physics are systematically analyzed.

In addition to transistor scaling, wafer-level packaging (WLP) has also been widely accepted as a pathway to further increase the device density. Active device integration in the back-end-of-line (BEoL) has been proposed to enhance the interconnect bandwidth, design flexibility, and reduce power consumption. Multi-layered molybdenum disulfide (MoS_2), featuring a finite bandgap, high mobility, and possible CMOS BEoL compatible (<400 °C) synthesis process, is a promising candidate for such an application. One of the major roadblocks in MoS_2 FET's fabrication is the lack of the controllable doping process for S/D formation. This work demonstrates a carrier control technique in MoS_2 by introducing substitutional Nb. The impact of high concentration Nb is quantified to precisely modulate the carrier density. Electrical characterizations show that a high carrier density ($>2\times10^{20}$ cm^{-3}) can be achieved, favorable for S/D formation with low access resistance. The relations between high concentration Nb and mobility, contact resistivity, and bandgap are also analyzed to guide MoS_2 transistor design.

The dissertation of Peng Lu is approved.

Robert N. Candler

Mark S. Goorsky

Subramanian Srikantes Iyer

Jason C. S. Woo, Committee Chair

University of California, Los Angeles

2020

To my parents.

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Acknowledgments

First and foremost, I would like to express my sincere gratitude to my advisor Prof. Jason Woo for his guidance and patience to help me navigate through my journey in graduate school. Also, I would like to thank Professor Robert Candler, Professor Mark Goorsky, and Professor Subramanian Iyer for the time to be in my committee

I would like to thank China Scholarship Council (CSC) for their funding from September 2016 to August 2019.

Many thanks to the staff in the UCLA Nanoelectronics Research Facility for their technical support and professional discussion of the process. And special thanks to Dr. You-Sheng Lin, Dr. Max Ho, and Hoc Ngo for the professional discussions of ALD dielectric deposition and 2D TMD's CVD system setup.

Additionally, I would like to thank all my lab mates, Ming, Po-Yen, Esther, Bo-Chao, Weicong, Xicheng, Allen, Scott, Emily, and Rabi, for their valuable discussions and inputs in my research.

Especially, I would like to express the ultimate gratitude to my parents for their unwavering faith in me, which make this thesis possible.

Finally, I would like to thank all the people who have helped me along the way.

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Chapter 1

Introduction

1.1 Overview and motivations

In the past decades, aggressive transistor scaling has been the driving force for the integrated circuit (IC) industry, enabling powerful computers, portable electronics, high-speed wireless communication, and recently IoTs. However, as device geometries are scaled-down, challenges such as short channel effects, variabilities, and power/thermal issues have become major roadblocks. The industry has invested heavily to mitigate these issues and maintain the scaling trend.

FinFETs have been the mainstream technology for the front-end-of-line (FEoL) application since the 22-nm node [1]. The 3D device structure provides a superior electrostatic control compared to planer FETs and features improved short channel effects such as drain-induced barrier lowering (DIBL) and sub-threshold swing (*SS*) degradation. The larger current drive per footprint compared with planar devices is preferable for high-speed logic circuits. FinFET technology has enabled further scaling down to 5nm node [2-5]. In addition to transistor scaling, 3D wafer-level packaging (WLP) and 3D integration [6-9] have also been widely accepted as a pathway to further increase the device density. Active device integration [10,11] in the back-end-of-line (BEoL) can be utilized to enhance the interconnect bandwidth, design flexibility, and reduce power consumption.

However, challenges arise in both FEoL and BEoL devices. For FEoL applications, process-induced performance variation, which is already a key limit in 10/14-nm node FinFETs (Fig. 1.1) [2,3], is becoming even more severe in beyond 5-nm node [12-15]. Although advanced

module process technologies have been developed to reduce the geometry parameters' variation in absolute value, their variation in percentage increases in ultra-scaled transistors. Consequently, it is crucial to identify the variability sources in FinFETs with realistic physical parameters and suppress process-induced performance variation in the future 3-nm node FinFETs. Furthermore, FinFET's analog/RF performances are inferior to those in bulk and SOI transistors [16], preventing its applications in the system on chip (SoC) designs. Advanced S/D formation technologies have been developed to precisely control the 3D doping profile in the source/drain extension (SDE) module [17], enabling new dimensions of freedom for design optimizations. In this work, both variability suppression and digital/analog performance enhancement through SDE doping profile optimization are investigated for 3-nm node FinFETs.

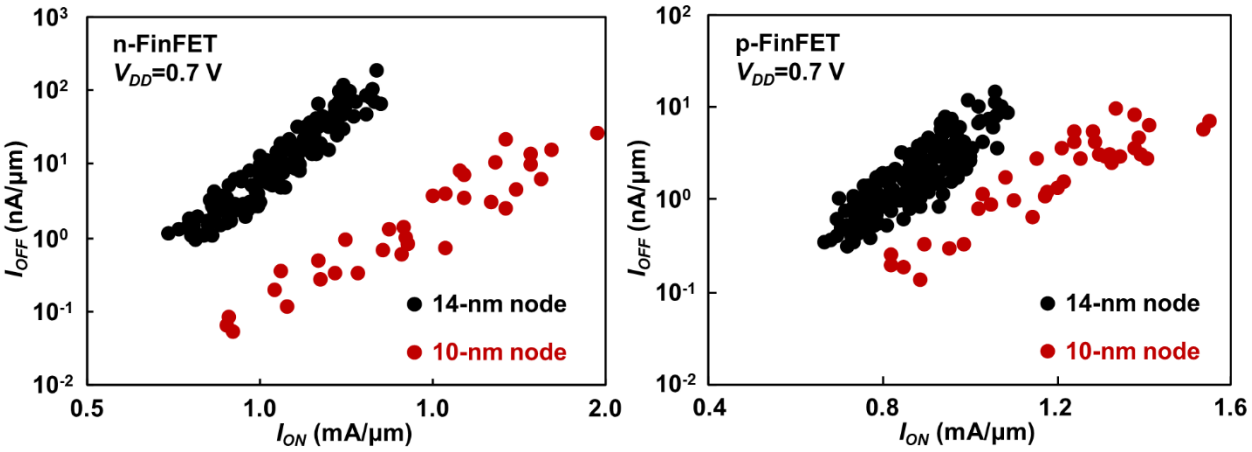

Fig. 1.1 Performance variability in Intel's 14 and 10-nm node FinFETs [2]-[3]. Although advanced process control techniques have been developed, variability degrades as geometry parameters are scaled down.

Multi-layered molybdenum disulfide (MoS_2), featuring a finite bandgap, high mobility, and possible CMOS BEoL compatible (<400 °C) synthesis process [18-20], is a promising

candidate for the active device integration in the BEoL. For such an application, a low access resistance is crucial to reducing the power consumption and increasing the signal bandwidth. Although tremendous effort has been made improve the contact resistivity [21-23] and mobility for access resistance reduction, it is necessary to have the TMD films below the contact to have a carrier concentration in the order of 10^{15} cm^{-2} (10^{20}~10^{21} cm^{-3}). Consequently, a selective-area carrier control technique is required for MoS_2 be useful for semiconductor industry. It would be helpful and interesting to investigate a MoS_2's controllable doping technique for access resistance reduction in MoS_2 channel FETs.

1.1.1 Variability suppression and performance enhancement through 3D SDE doping profile engineering in 3-nm node FinFETs

Process-induced variability is predicted to be exceedingly severe in ultra-scaled FinFETs beyond the 5-nm node. To guide process optimizations, the variabilities induced by different modules, including the fin, gate stack, ploy pitch, and source/drain (S/D), need to be quantified. In previous works, FinFETs are modeled with idealized fin structures [24-26], and the device performances are analyzed to resemble those in a double-gate (DG) FET [27,28]. However, experimental analysis shows that device performances have become increasingly sensitive to detailed geometry parameters such as the fin taper angle and the bending effect [29-31]. Therefore, realistic module parameters instead of idealized geometries are required for variability analysis. In this work, the FinFET performance's dependency on the non-ideal factors, including the coupling between the intrinsic active fin and the heavily doped sub-fin, the fin taper angle, and the dopant diffusion profile in the SDE region, are systematically analyzed for 3-nm node FinFETs.

In sub-14-nm node FinFETs, the gate underlap design is adopted to suppress the short channel effect (SCE). As the FinFET's poly pitch is continuously scaled-down, the device performances are exceedingly sensitive to the dopant encroachment from the heavily doped S/D towards the intrinsic channel [16,17,26,32,33]. However, to the best of the author's knowledge, the SDE doping profile induced variability has not been systematically analyzed. Although the SDE doping profile's impact on the sub-threshold performance has been analyzed [17,32], the relation between the SDE doping profile and the on-state parasitic resistance ($R_{S/D}$) has not been studied. In this work, FinFETs with realistic doping diffusion gradient is simulated to quantify the SDE doping's impact on the SDE parasitic resistance (R_{SDE}) and performance variations. The governing physics is interpreted to guide the design optimization for future generation FinFETs and gate-all-around FETs (GAAFETs).

More importantly, SDE doping profile engineering is proposed as an effective method to suppress the coupling between the channel and the drain fringing field, and thus reduce the FinFET performance's sensitivity to the physical parameter's variation. Advanced S/D formation technologies have been developed to precisely control the fin top recess length (LR) and the vertical profile (in the fin height direction), enabling new dimensions of freedom for design optimizations. The 3D SDE doping profile, previously developed to improve device performance in 7/10-nm node, is shown to be an effective method for variability suppression with minimal modification in the FinFET's process flow. Inspired by the physical interpretations, a 3D SDE doping profile's optimization methodology is also proposed to achieve variability suppression together with I_{ON}/I_{OFF} enhancement in 3-nm node FinFETs. To improve the trade-off between *SS* and the parasitic resistance ($R_{S/D}$), it is crucial to optimize the SDE doping profile concerning the physical parameters in the channel and gate module in future generation transistors.

The 3D SDE doping profile optimization also provides pathways for 3-nm node FinFET's analog performance enhancement. The relatively low cut-off frequency (f_T) in FinFETs is known to be limited by the $R_{S/D}$ and the parasitic capacitance ($C_{parasitics}$) [34,35]. 3D SDE doping profile engineering can be utilized to increase the SDE doping concentration and reduce the $R_{S/D}$. Enabled by the advanced S/D formation technologies, a reduction in $C_{parasitic}$ can also be achieved by spacer and SDE module co-optimization and further enhance f_T. In this work, an SDE doping and spacer length co-optimization process is demonstrated, resulting in ~80 GHz (~16%) f_T improvement. The contributions of parasitic resistance and capacitance reduction on f_T enhancement are quantified, guiding the analog performance optimization in ultra-scaled transistors.

1.1.2 Carrier control technique in multi-layered MoS_2

Both theoretical and experimental studies show that substitutional Nb can be utilized to introduce holes in the 2D MoS_2. Density function theory calculations have suggested that substitutional Nb in MoS_2 (native n-type) with mole fractions lower than a few percent is a p-type dopant and has little impact on band-structure [36,37]. Experimentally, MoS_2 with Nb demonstrates a p-type behavior [38-42]. MoS_2 with hole concentration as high as 10^{21} cm^{-3}, corresponding to >10% Nb mole fraction, has been synthesized [40]. However, several challenges remain before achieving a fully controllable doping process. A selective-area precise Nb dose control technique has not been demonstrated. More importantly, for a >10% Nb concentration, the material would be considered as a compound semiconductor, as in the case of bulk semiconductors like SiGe or III/V materials. The impact of high concentration Nb on carrier density needs to be quantified. In this work, a precise Nb mole fraction control technique in the 2D MoS_2 is demonstrated. Multi-layered $Mo_{1-x}Nb_xS_2$ samples with various Nb concentrations from 3.5% to

11% are synthesized to quantify the role of Nb. TLM structures and MOSFETs are fabricated on the wafer-scale uniform 2D films for electrical characterizations. Highly non-linear relations between Nb mole fraction and hole density, mobility, and contact resistivity are observed, strongly suggesting that the high concentration Nb does not act as an active dopant. The relationships between hole density and Nb mole fraction can be utilized to guide carrier concentration modulation. Increasing the Nb mole fraction from 3.5% to 11% also results in $>10^4\times$ mobility improvement and contact resistivity reduction, both are favorable for achieving S/D regions with low access resistances.

1.2 Organization

This dissertation is organized into the following chapters.

In Chapter 2, the device performances in FinFETs with realistic geometry parameters are analyzed using TCAD simulation, and the governing physics is investigated to guide variability quantification and suppression. The setup of the TCAD tools and the calibration process are discussed in detail. In this work, the impact caused by the non-ideal factors are systematically analyzed. In the 3-nm node FinFET with realistic module, the fin and the SDE doping are identified as major sources of the process-induced variability. Guided by the physics interpretation, 3D SDE doping profile engineering is demonstrated to be an effective method to suppress process-induced variability in 3-nm node FinFETs.

In Chapter 3, the 3D SDE doping profile's optimization methodology is proposed to improve the digital and analog performance in 3-nm node FinFETs. By optimizing the LR together with the vertical doping profile along the fin height direction, better *SS* and $R_{S/D}$ trade-off can be

achieved, benefiting both digital and analog performances. A co-optimization of the spacer thickness and the SDE doping is also investigated for parasitic capacitance reduction, further enhancing 3-nm node FinFET's analog performance.

In Chapter 4, the high mole fraction (>3.5%) Nb's impact in MoS_2 is quantified to guide precise carrier control in MoS_2. The synthesis process and material characterization of wafer-scale $Mo_{1-x}Nb_xS_2$ films with various Nb mole fractions are discussed. The material and electrical characterization process are demonstrated. The impact of high mole fraction Nb (>3%) on carrier concentration, mobility, and contact resistivity is quantified, and the role of Nb in $Mo_{1-x}Nb_xS_2$ is analyzed. This chapter is a modified version of "Peng Lu, Yen Teng Ho, Yung-Ching Chu, Ming Zhang, Po-Yen Chien, Tien-Tung Luong, Edward Yi Chang, Jason C.S. Woo, "Electrical Properties of Compound 2D Semiconductor $Mo_{1-x}Nb_xS_2$", *14th IEEE International Conference on Solid-State and Integrated Circuit Technology* (ICSICT), pp. 1-4, Oct. 2018, DOI: 10.1109/ICSICT.2018.8564953".

Finally, Chapter 5 summarizes the major contributions of this work and suggests future research directions.

Chapter 2

3-nm node FinFET's variability quantification and suppression

2.1 Introduction

Process-induced variability is predicted to be exceedingly severe in ultra-scaled FinFETs beyond the 5-nm node. In this work, Sentaurus [43] TCAD simulations are used to quantify the 3-nm node FinFET's performance variation induced by different modules. Realistic geometry parameters and their variation ranges are characterized by advanced module process results, and the impact of the non-ideal factors are discussed. Rather than semi-classical models [27,44], calibrated quantum mechanical models are used to capture the physics in the ultra-scaled device. To identify the physical mechanisms, Si-channel n-FinFETs' various geometry parameters are studied in detail, and the differences between Si n- and s-SiGe p-FinFETs are discussed.

The gate underlap design has been adopted to suppress the SCE in sub-14-nm node FinFETs. As the FinFET's poly pitch is continuously scaled-down, the device performances are exceedingly sensitive to the dopant encroachment towards the intrinsic channel. In this work, the performance variation induced by the SDE formation process is analyzed. The governing physics, especially the SDE doping profile's impact on the parasitic resistance, is interpreted to guide the design of future generation transistors. More importantly, Advanced source/drain (S/D) formation technologies have been developed to precisely control the fin top recess length (LR) and the vertical profile (in the fin height direction), enabling new dimensions of freedom for design optimizations. The SDE doping profile engineering can be utilized as an effective method to suppress the coupling between the channel and the drain fringing field, and thus reduce the FinFET

performance's sensitivity to the physical parameter's variation. The physical mechanism and limitations are demonstrated.

2.2 Simulation setup and calibration

2.2.1 3D FinFET structure setup

In this study, 3nm node FinFET structures featuring tapered fin, double-layered gate stack, and experimentally extracted channel and source/drain junction profile are simulated (Fig. 2.1). The geometry parameters, and the realistic variations ranges (Table I) are extracted from the characterizations of advanced module process results. Advanced de-footing and fin trimming technology (Fig. 2.2(a)) can be employed to realize well-controlled fin width (W_{fin}, defined as the Si thickness T_{Si} at the fin top) and fin taper angle (θ). A double-layered gate stack module consisting of a Silicon Oxynitride (SiON) interfacial layer (IL, ε_r=6) and a Hafnium Oxide (HfO_2) high-k (HK, ε_r=22.5) layer is simulated. The fluctuation of nitrogen composition in the IL results in a permittivity (ε_r) variation, and consequently causes a variation in the gate stack's Effective Oxide Thickness (*EOT*). The SDE doping is induced by the diffusion from the heavily doped (3.5×10^{20}/1×10^{20} cm^{-3} for n-/p-FinFET) S/D region to the lightly doped channel. The S/D and channel junction profile can be characterized by TEM images (Fig. 2.2(b)). Secondary Ion Mass Spectroscopy (SIMS) measurement shows a steep dopant gradient (~2 nm/dec) at the SDE/channel interface (Fig. 2.2(c)). FinFETs with both vertically uniform (no 3D SDE doping profile engineering, Fig. 2.1(c)) and non-uniform SDE doping profiles (Fig. 2.1(d)) are analyzed in this study. By employing an isotropic S/D recess etch technology with lateral recess length (LR) followed by bi-layer Si:As/Si:P epitaxy regrowth [17], a vertically non-uniform S/D junction

profile (Fig. 2.2(b), referred to as the V-shape profile in this work) featuring reduced dopant encroachment near the sub-fin can be achieved. The fin recess etching process is identified as a variation source, and ±1 nm ΔLR is observed. The S/D contact resistivity (ρ_C) is assumed to be 1×10^{-9} Ω·cm^2 [45].

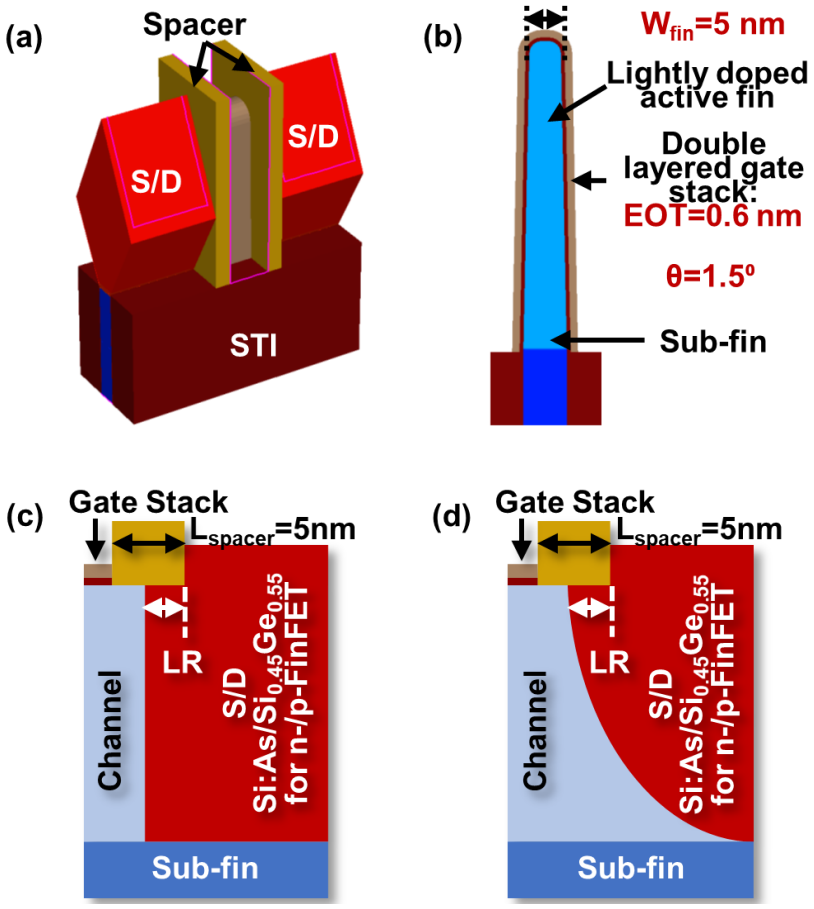

Fig. 2.1 Schematic of simulated 3-nm node FinFETs (a) the 3D structure, (b) the fin geometry and the gate stack parameters, (c) (d) schematic of the vertically uniform and non-uniform SDE doping profile, respectively (not to scale).

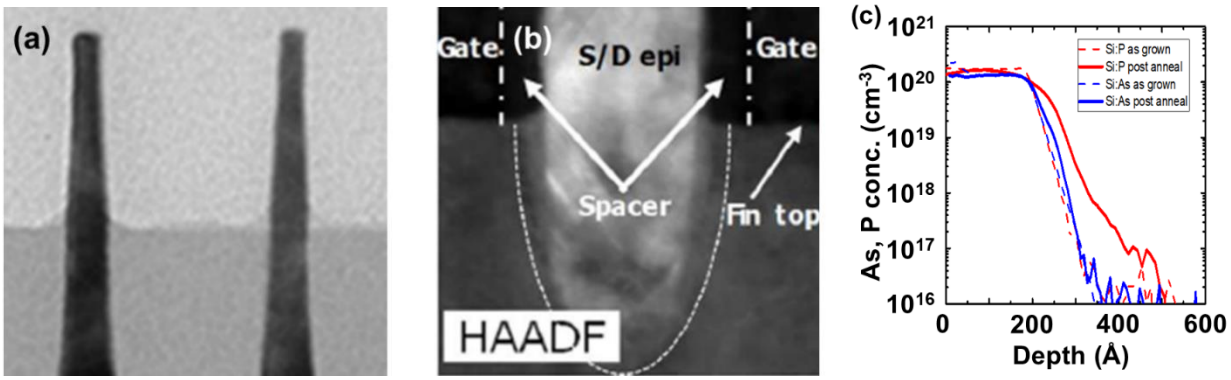

Fig. 2.2 Geometries and variation ranges extracted from advanced module process characterizations. (a) Fin geometry, (b) SDE junction profile [17], and (c) the SIMS of the doping diffusion gradient from the heavily doped S/D to the intrinsic channel.

Table 2.1 Geometry parameters and their variation ranges in 3-nm node FinFETs

Geometry parameter	Nominal Value	Variation range
Fin height (H_{fin})	50 nm	
Fin pitch	26 nm	
Spacer length (L_{spacer})	5 nm	
Contact resistivity (ρ_C)	10^{-9} Ω·cm^2	N/A
Channel material	Si ($Si_{0.75}Ge_{0.25}$) in n-(p)FET	
S/D doping	3.5(1) ×10^{20} cm^{-3} in n-(p)FET	
Junction doping gradient	2 nm/dec	
Poly pitch (L_G)	14 nm	±1.5 nm
Fin top width (W_{fin})	26 nm	±1 nm
Taper angle (θ)	1.5º	±1.5º
Gate dielectric EOT	0.6 nm	±0.05 nm
S/D material	Si:As ($Si_{0.45}Ge_{0.55}$) in n-(p-)FET	±5% Ge in p-FET
LR in vertical uniform SDE profiles	0 nm	±1 nm
LR in V-shape SDE profiles	2 nm	±1 nm

2.2.2 Physical models setup and calibration

Fig. 2.3 shows the simulation setup in this study. A self-consistent 2D Schrodinger equation and Poisson's equation solver accurately captures the carrier quantum confinement. For both n- and p-FinFET, the channel materials are grown on a <100> surface, and the channel length (carrier transport direction) is along the <110> direction. When the film thickness is scaled down, the density of available state per area reduces in the case of 2D materials, leading to a reduction in quantum capacitance. Since the $G_G=(C_{Si}^{-1}+C_{OX}^{-1})^{-1}$, (where the C_G, C_{Si}, and C_{OX} are the gate capacitance, Si film's quantum capacitance and the gate dielectric's capacitance, respectively,) a smaller C_G is expected. However, this study shows a trend contrary to expectations (Fig. 2.4(a)). When T_{Si} reduces from 8 to 5 nm, the gate-channel coupling is enhanced because the inversion charge peak gets closer to the interface, increasing the C_{Si} and C_G (~5%). The simulation results match the reported experimental data C_G vs. T_{Si} in the latest nanosheet device results [46], adding credibility to the physical interpretation. In the nominal Si fin in n-FinFET, the on-state C_{Si} is calculated to be 6.68 μF/cm^2, equivalent to 0.52 nm of *EOT*. In s-SiGe p-FinFET, the compressive uniaxial stress induced by the S/D stressor is extracted from process simulations. The deformation potential model is included to capture the channel stress's impact on carrier quantum confinement [47]. Since the effective mass of the hole is much larger than that of the electron, the holes distribute closer to the channel/dielectric interface. As a result, the gate-channel coupling is stronger in p-FinFET, and the quantum capacitance (C_{SiGe}) is extracted to be 7.34 μF/cm^2, equivalent to 0.47 nm of *EOT*.

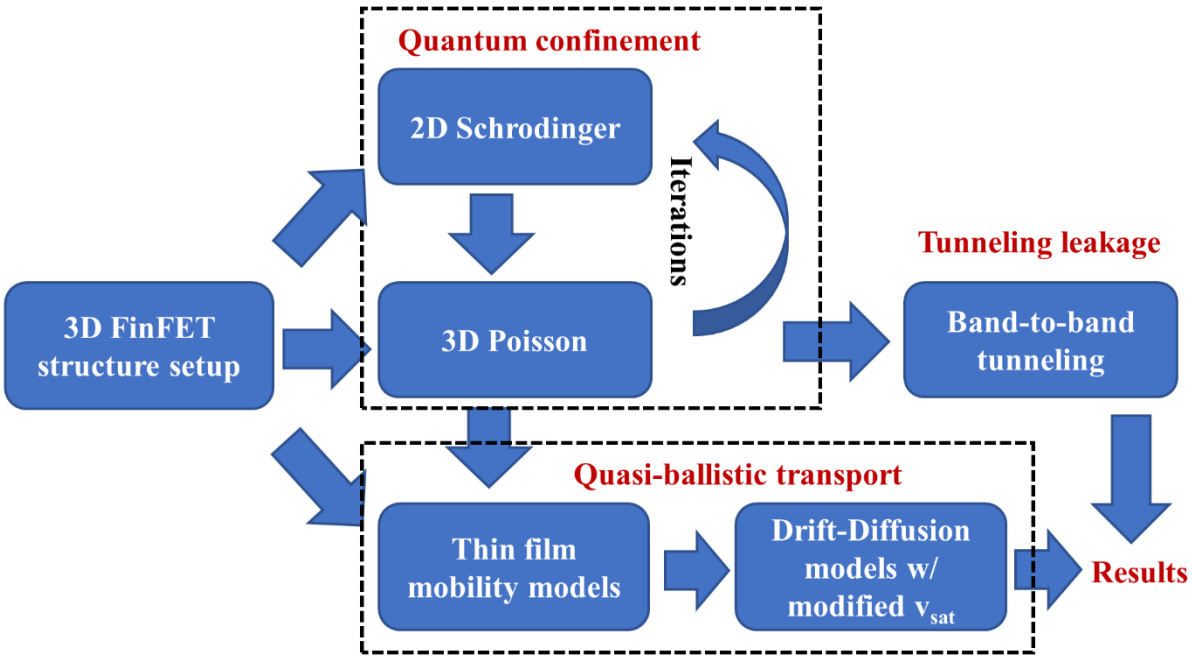

Fig. 2.3 Simulation setup for the 3-nm node FinFET's variability analysis.

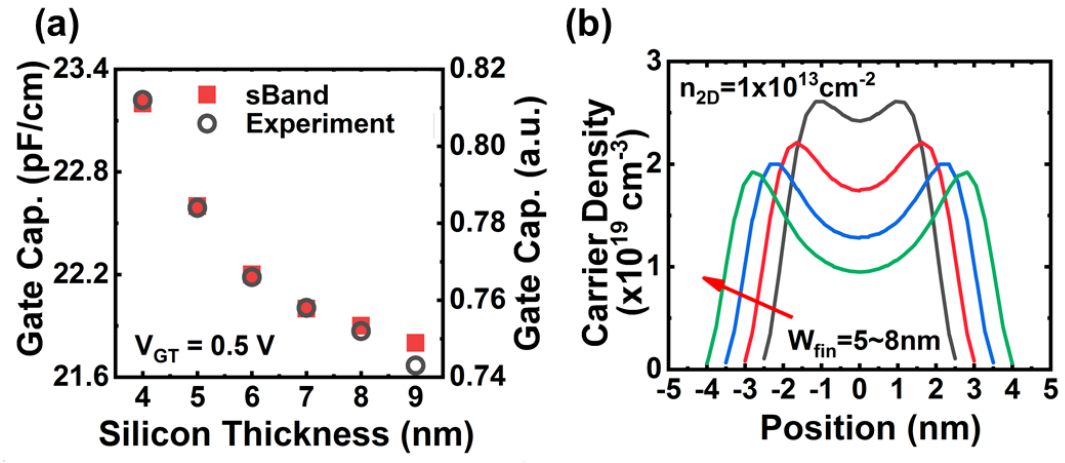

Fig. 2.4 The trend of simulated gate capacitance vs. Si thickness agrees with the experimental data in nano-sheet devices [46]. The quantum capacitance increases.

To capture the carrier quasi-ballistic transport in devices with sub-20-nm channel lengths, schemes for the simulation, including Monte Carlo (MC) method, Hydrodynamic (HD) model, and Drift-Diffusion (DD) model with modified saturation velocity (v_{sat}), have been proposed. The MC method [48,49], which is based on an indirect solution of the Boltzmann transport equation, has the strongest conceptual basis among all the models discussed and is frequently considered the most accurate approach. However, the computational efforts of the three approaches mentioned above in terms of CPU time yields are estimated to be 1:6:140 for DD, HD, and MC, respectively [48]. Therefore, the MC model is not suitable for a variability study due to the expense of computational cost. Modified HD models with adjusted energy relaxation times have been used to simulate transistors with down to sub-20-nm [50]. However, an over-estimate of the carrier velocity is observed [51]. In this study, a drift-diffusion model with a modified saturation velocity is used to emulate the carrier quasi-ballistic transport [51]. This method is capable of reproducing the velocity profile of the MC method down to <10 nm L_G (Fig. 2.5). For s-SiGe channel p-FinFET, the effective v_{sat} is calculated by $v_{sat}=v_{ballistic}\times$*ballistic ratio*, where $v_{ballistic}$ is the ballistic transport velocity, and *ballistic ratio* is a fitting parameter as a function of L_G. The dependency of $v_{ballistic}$ and *ballistic ratio* on the Ge composition, stress and poly pitch are reported in publication [52,53], enabling variability analysis for p-FinFET.

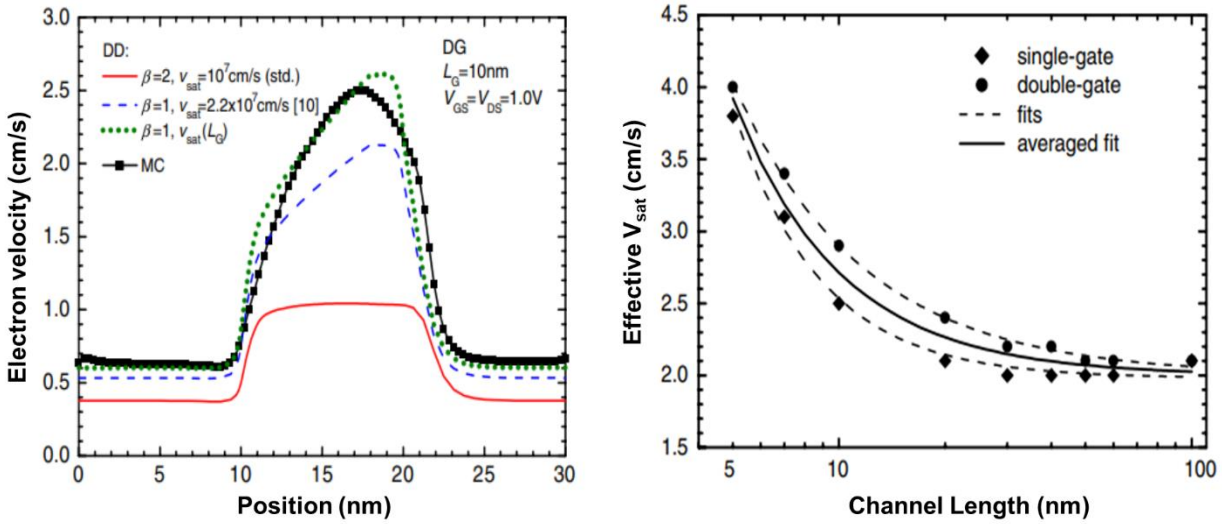

Fig. 2.5 Drift-diffusion model with modified v_{sat} can be used to emulate the quasi-ballistic transport for L_G<20nm [51].

In this study, the high-field dependence, vertical field degradation (Enormal), and doping dependence model are used to simulate mobilities in ultra-scaled transistors. The high field dependence model with modified v_{sat} is used to emulate quasi-ballistic transport. A calibrated Enormal model is adopted to capture surface roughness degradation. For n-FET, the simulated mobility agrees with the thin-film FET's experimental data [54] (Fig. 2.6). For p-FET, the models are calibrated against SOI s-$Si_{0.73}Ge_{0.27}$ FinFET's I-V curve [55] (2.7(a)). The experimentally measure mobility enhancement factor as a function of Ge composition and stress [56] is utilized to simulate stress-induced mobility variation in 3-nm node p-FinFETs with s-$Si_{0.75}Ge_{0.25}$ channel.

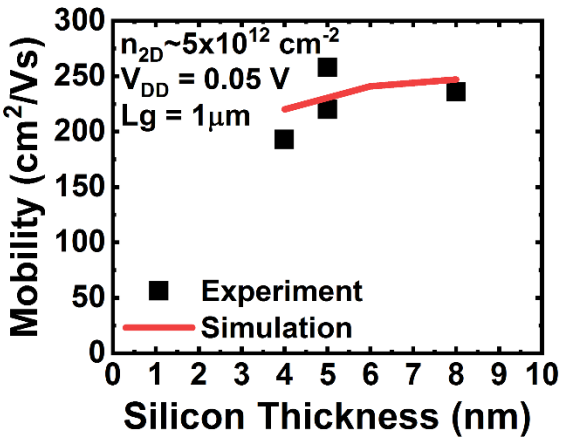

Fig. 2.6 Calibrated electron mobility in the thin film agrees with experimental data [54].

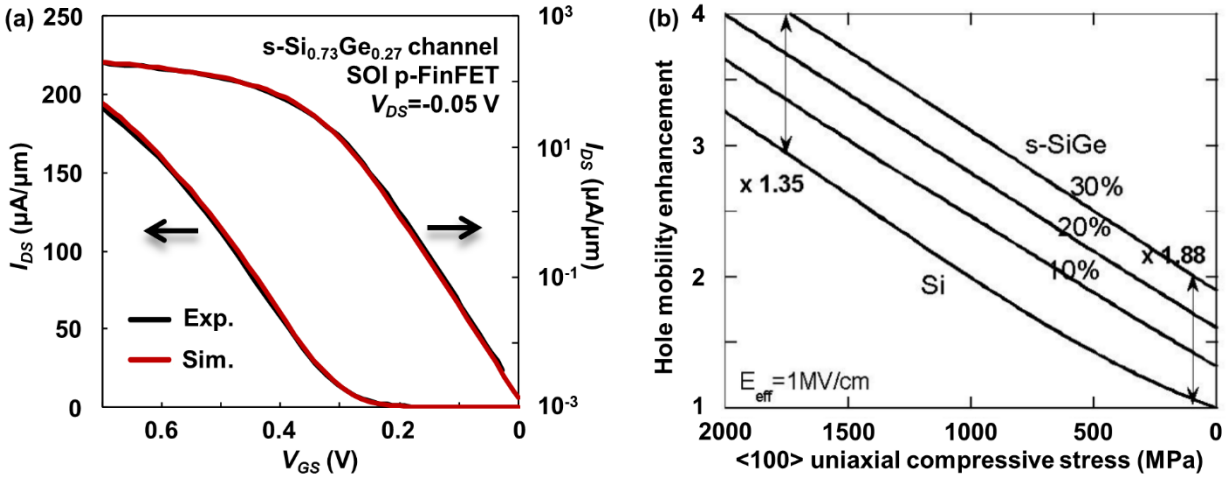

Fig. 2.7 (a) Hole mobility models in s-$Si_{0.73}Ge_{0.27}$ are calibrated to SOI FinFET I-V characteristics (<2% error) [55], and (b) the mobility enhancement factor is utilized for stress induced variability [56].

To check the accuracy of the above-mentioned platform, simulation results are compared against FinFETs' experimental I-V characteristics. FinFETs with various geometry parameters, including Intel's 14-nm node bulk n- and p-FinFET [2], 10-nm node bulk n-FinFET [3], and Globalfoundries' 10-nm node SOI p-FinFET [55], are tested. For etch transistor, detailed fin geometry and gate stack parameters (Fig. 2.8) are properly modeled, and the SDE doping gradient

is calibrated to fit the sub-threshold slope (*SS*) and drain induced barrier lowering (DIBL). The simulation results agree with n-/p-FinFETs' experimental data (Fig. 2.9), adding credibility to this variability analysis.

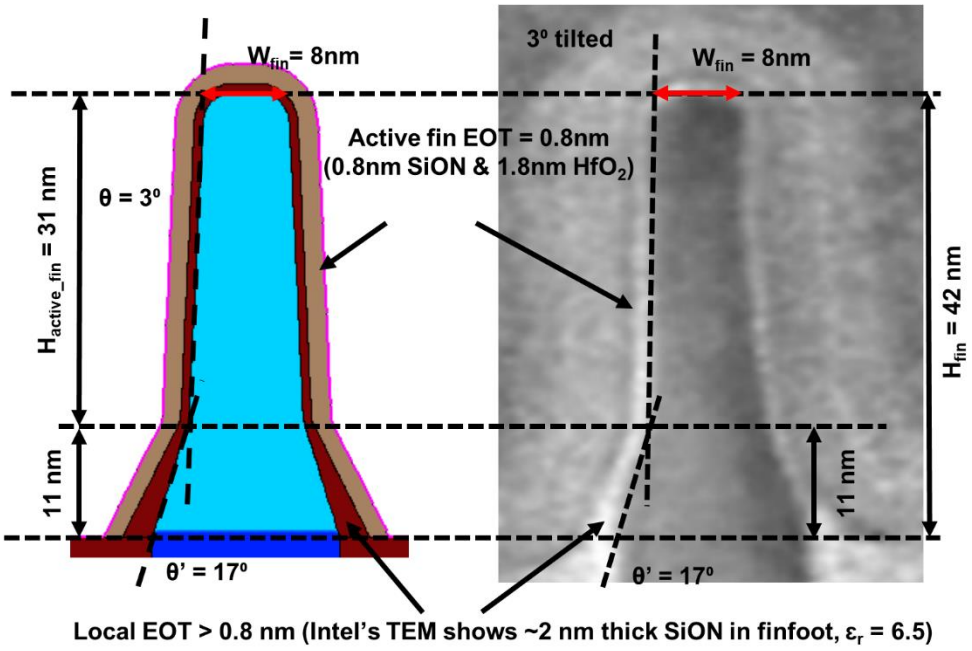

Fig 2.8 Fin structure setup for Intel's 14-nm node n-FinFET [2].

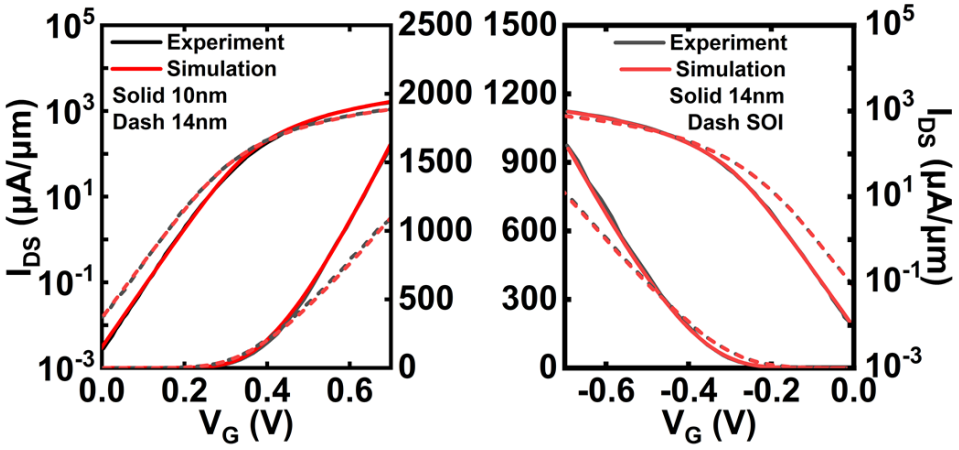

Fig. 2.9 Simulation results match the experimental data of (a) Intel's 10/14-nm node bulk n-FinFET [2]-[3], (b) Intel's 14-nm node bulk p-FinFET [2], and Globalfoundries' SOI p-FinFET [55].

2.3 Device performance of realistic FinFETs

To improve the accuracy of the variability analysis, the device performances in FinFETs with realistic module parameters are quantitatively investigated. In ultra-scaled FinFETs, the device performances are extensively sensitive to non-ideal factors. In an n-FinFET with an idealized fin (taper angle θ=0º), both the sub-threshold and on-state currents flow approximately uniformly along the fin height (H_{fin}) direction (Fig. 2.10), resembling those in a DG MOSFET. However, a tapered fin is designed in the 3-nm node FinFETs to enhance the robustness of the device, resulting in a ~2.5nm larger fin bottom T_{Si} than the W_{fin}. The non-uniform T_{Si} results in a unique evolution of the current density (Fig. 2.11), featuring a localized leakage path near the sub-fin and a relatively uniform on-state current distribution in the fin cross-section. The difference in current distribution can substantially affect the device performances including I_{ON}, I_{OFF}, constant current threshold voltage (V_{TS}, defined as the V_{GS} at I_{DS}=10μA/μm and V_{DS}=0.7V), sub-threshold swing (SS), and Drain Induced Barrier Lowering (DIBL). To isolate the impact caused by various non-ideal factors, n-FinFETs with both idealized and realistic geometry parameters are analyzed and compared. The device performances' dependency on the realistic physical parameters are quantified, and the governing physics are interpreted.

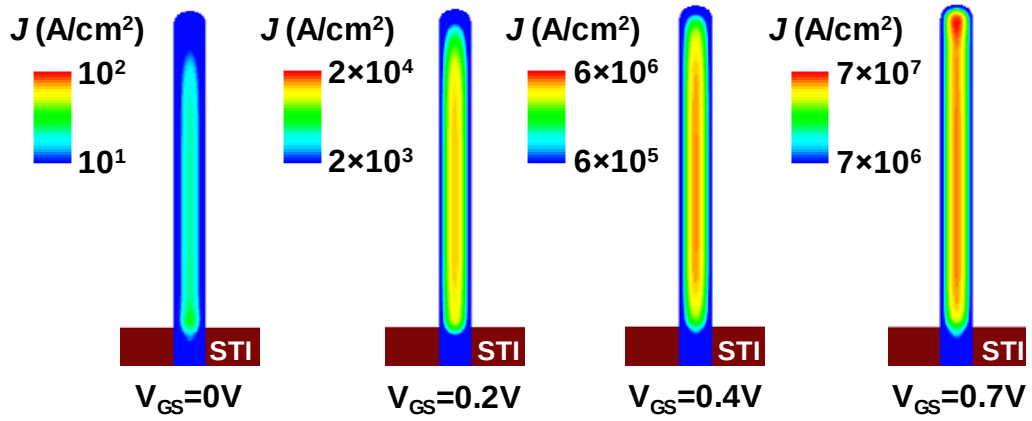

Fig. 2.10 Current density distribution's evolution in an n-FinFET with an idealized fin (θ=0º), a vertically uniform SDE junction profile, and V_{DS}=0.7V.

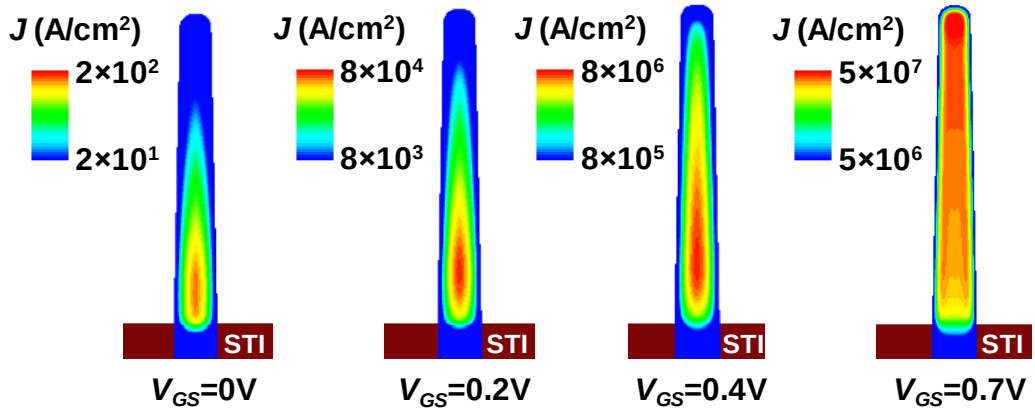

Fig. 2.11 Current density distribution's evolution in the nominal 3-nm node n-FinFET without 3D SDE doping profile engineering and V_{DS}=0.7V. The geometry of the fin is predicted based on advanced module process results.

2.3.1 Sub-threshold performance

The sub-threshold current is controlled by the diffusion across the virtual cathode (the location where minimum energy barrier occurred) and is governed by the gate electrostatic control competing with the drain fringing field. For an n-FinFET with an idealized fin, the electric field along the H_{fin} direction (E_X) is negligible in the middle of H_{fin}, and the sub-threshold performance resembles that in a short channel DG MOSFET. Analytical models of the short channel DG

MOSFET have been widely studied [38,57,58]. However, they are insufficient for FinFET's sub-threshold performance quantification. Since the gate underlap design has been adopted to suppress the SCE since the 14-nm node, it is crucial to properly model the potential or electric field distribution in the relatively lightly doped SDE region. To the best of the author's knowledge, no analytical model has been proposed to accurately capture the impact of the gate underlap design. Therefore, TCAD simulations are required for the 3-nm node FinFET's sub-threshold performance analysis.

The electric field profile in a cut-plane perpendicular to the H_{Fin} direction (H=25 nm, where H is defined as the distance from the fin top) is shown in Fig. 2.12. The space charge density is relatively small in the lightly doped channel, and the electric field induced by the S/D regions (caused by V_{DS} combined with the S/D and channel built-in potential [38]) terminates at the gate metal. The drain induced fringing field is known to degrade the coupling between gate bias and the virtual cathode. With a fixed physical channel length and gate stack EOT, increasing the T_{Si} can lead to a larger electric field along the T_{Si} direction (E_Y, Fig. 2.13(a)). As a result, the voltage drops in the gate dielectric and the semiconductor increase (Fig. 2.13(b)), reducing the E_C and the virtual cathode barrier height (E_C-E_{fn}) in the channel (Fig. 2.13(c)). This is analogous to the threshold voltage roll-off effect in SOI and DG MOSFETs. Increasing the T_{Si} also reduces the ground state energy (E_0, proportional to T_{Si}^{-2}) of the quantum confinement, further increasing the I_{OFF}. At a fixed gate bias and work function, the I_{OFF} is observed to be approximately exponentially related to the T_{Si} (Fig. 2.13(c)). Meanwhile, the larger drain fringing field degrades the coupling between the virtual cathode and the gate bias (Fig. 2.13(d)) and consequently enlarges the *SS* and DIBL.

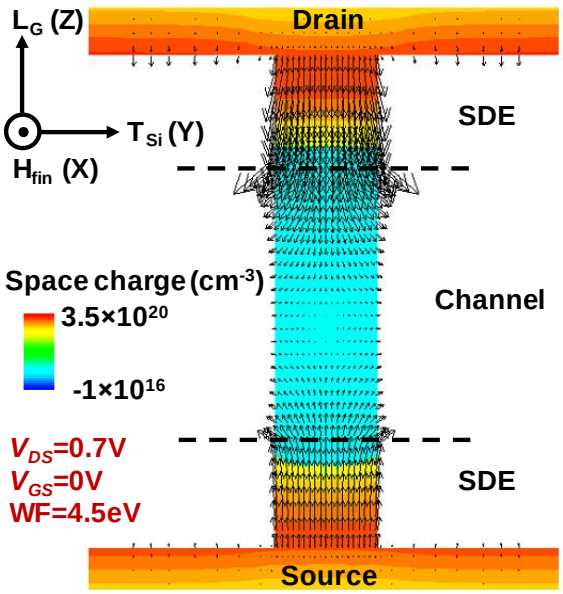

Fig. 2.12 The electric field and space charge profile in a cut-plane perpendicular to the H_{Fin} direction (25 nm from the fin top). The n-FinFET has an idealized fin.

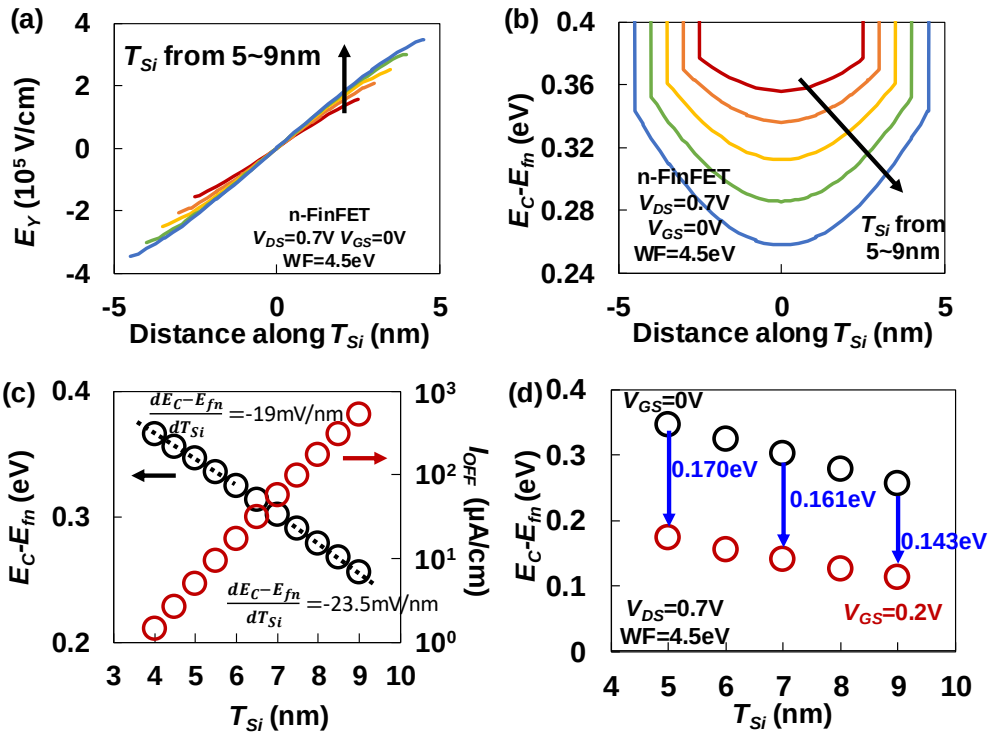

Fig. 2.13 (a) The E_Y and (b) the barrier profile along the cutline across the virtual cathode as a function of the T_{Si}, (c) the virtual cathode barrier height, off-state current density normalized to effective conduction width, and (d) the coupling between the virtual cathode barrier height and the gate bias as a function of the T_{Si}.

Close to the active fin and sub-fin interface, the virtual cathode barrier is modulated by the drain induced fringing field as well as the built-in potential induced by the relatively heavily doped sub-fin (Fig. 2.14(a)). Because of the absence of gate modulation in the sub-fin, the drain fringing field results in a larger E_Y at H>40 nm (Fig. 2.14(b)). Consequently, the larger potential drops in the gate dielectric and the semiconductor reduce the virtual cathode barrier height (Fig. 2.14(c)). Meanwhile, the barrier profile in the sub-fin is increased by the sub-fin built-in potential, counter-balancing the effect of the larger E_Y. A combination of the above-mentioned factors results in the lowest barrier energy at H=48.5 nm (Fig. 2.14(d)), leading to a ~2.5× leakage current density compared to that at H=25 nm. The bottom 10 nm of the active fin has an ~1.6× average current density compared to that at H=25 nm and contributes to 35% of the total I_{OFF}.

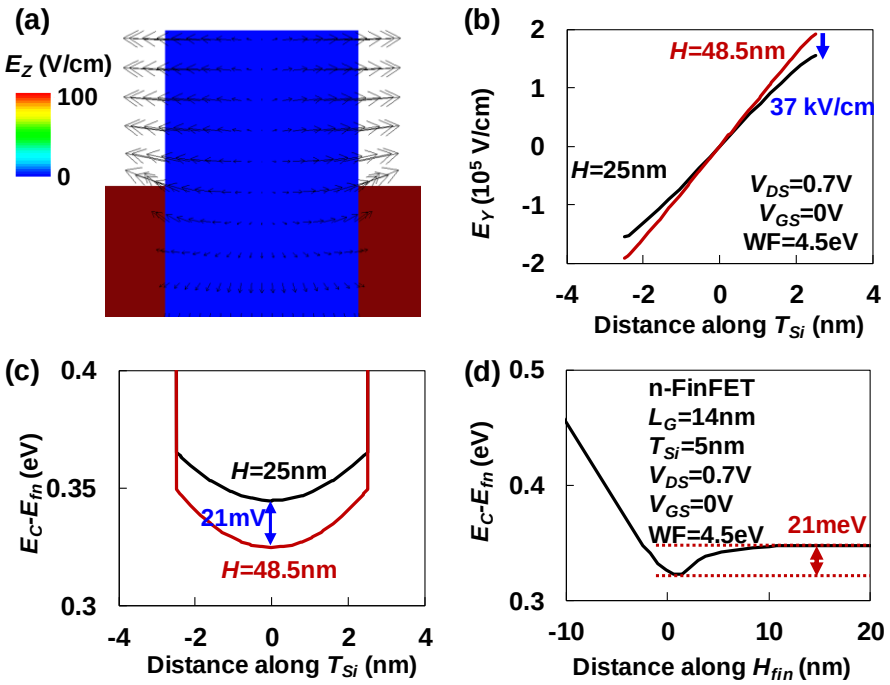

Fig. 2.14 Electric field and the barrier profile close to the sub-fin. (a) The electric field distribution in the fin cross-section near the virtual cathode, (b) and (c) the comparison between the E_Y and the barrier profile at the middle of the H_{fin} (H=25 nm) and near the fin bottom (H=48.5 nm), respectively, and (d) the barrier height along the H_{fin} direction in the middle of the T_{Si}.

More importantly, the realistic 1.5º tapered fin shows a substantial impact on the n-FinFET's sub-threshold performance. In a tapered fin, $T_{Si}=W_{fin}+2\times H\times tan(\theta)$. In the middle of the H_{fin} (H=10~40 nm), E_X is observed to be much smaller (<10^{-2}×) than E_Y, and the local barrier height is mainly modulated by the local E_Y (Fig. 2.15). As shown in Fig. 2.13, the increase in T_{Si} leads to a larger drain induced fringing field and a reduced diffusion barrier height. Consequently, the diffusion barrier height reduces approximately linearly as H increases (Fig. 2.15 (b)). The active fin and sub-fin coupling further reduces the barrier height close to the fin bottom, forming a localized virtual cathode (Fig. 2.15(b)) and leakage path (Fig. 2.15(c)). In the 3-nm node FinFET, the T_{Si} is increased by ~50% (from 5 to ~7.5 nm) from the fin top to the fin bottom, resulting in a 63meV lower virtual cathode barrier height (Fig. 2.15(b)) and a ~10× larger I_{OFF} than those in an idealized FinFET. In summary, properly modeling the non-ideal factors is of substantial significance for 3-nm node FinFET's sub-threshold performance analysis.

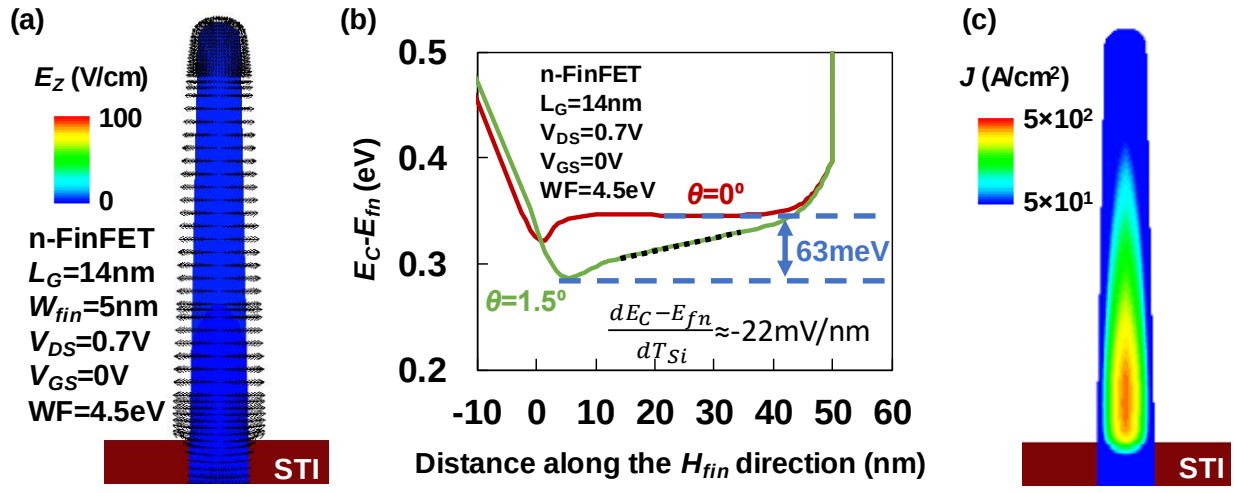

Fig. 2.15 The sub-threshold performance in an n-FinFET with a tapered Fin. (a) The electric field profile in the cross section at the virtual cathode, (b) a comparison of the barrier profiles along the H_{fin} direction between FinFETs with idealized and realistic fins, and (c) the off-state current distribution in the fin.

2.3.2 On-state performance

The FinFET's on-state performance is determined by the total carriers and average carrier velocity across the fin near the source. Therefore, it depends on the gate modulation, carriers' drift transport, $R_{S/D}$, and gate overdrive. Gate modulation to the first order is determined by $C_G=(C_{OX}^{-1}+C_{Si}^{-1})^{-1}$. In an n-FinFET with an idealized fin, the on-state current distributes approximately uniformly in the fin cross-section. This is similar to that in a DG FET, except in the regions close to the fin top and the fin bottom (Fig. 2.16). In section A, the effective conduction width enlarged by the top gate, resulting in a ~24% higher average carrier density and a larger I_{ON} compared to those near the middle of the H_{fin}. However, the higher gate electric field degrades the local mobility and the quasi-ballistic velocity, counter-balancing the effect of the increased carrier density. The average current density in section A is observed to be ~15% higher compared to that in the middle of the H_{fin}. Near the fin bottom (section E), both the absence of gate stack in the sub-fin and the built-in potential between the active fin and the sub-fin reduce the gate modulation, resulting in a ~15% smaller carrier density and I_{ON}.

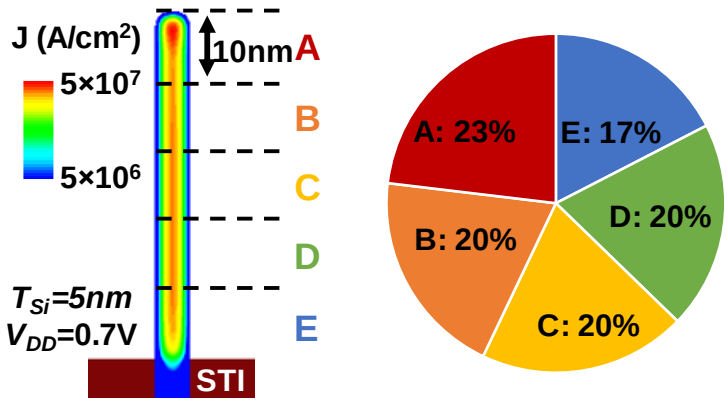

Fig. 2.16 The on-state current distribution in an n-FinFET with an idealized fin.

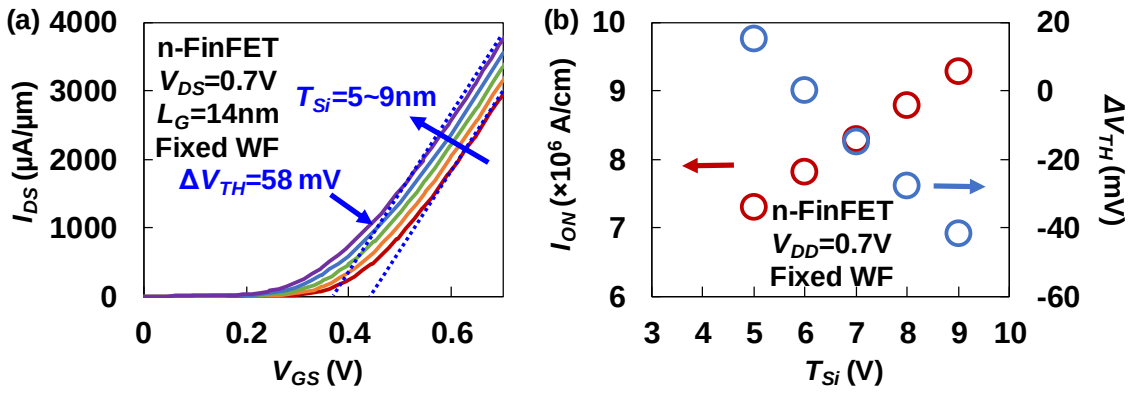

Fig. 2.17 The on-state performance as a function of the T_{Si} in n-FinFETs with idealized fins. (a) The transfer characteristics, and (b) the I_{ON} normalized to the effective conduction width, and the linearly extracted V_{TH} shift.

To quantify the impact of the T_{Si} on FinFETs' on-state performance, idealized FinFETs with various T_{Si} from 5 to 9 nm are compared (Fig. 2.17). Within the studied T_{Si} range, reducing the T_{Si} by 1 nm leads to a ~2% higher C_{Si} (Fig. 2.4) [46] and an improvement in the transconductance (g_m). However, the higher gate electric field results in a ~5% lower mobility [54], counter-balancing the effect of the C_{Si} increase. The reduced SDE conduction area also increases the parasitic resistance, further reducing the g_m. Consequently, a relatively small change (~3%) in g_m is observed. More importantly, the scaling of the T_{Si} causes an approximately linear reduction in the V_{TH} (defined as the linearly extrapolated threshold voltage in the on-state, Fig. 2.17(b)). This is contributed by the lowered E_0 and the reduced density of states in fin cross-section area. Numerically, the ΔV_{TH} has a dominating impact on the on-state performance, and the I_{ON} is approximately linearly related to the T_{Si} (Fig. 2.17(b)). Reducing the T_{Si} by 1 nm leads to a ~5% reduction in the I_{ON}.

In FinFETs with realistic tapered fins, the on-state current density is affected by the change in local T_{Si} ($T_{Si}=W_{fin}+2\times H\times tan(\theta)$), top gate modulation, and the degradation of gate modulation near the fin bottom. In section B, C, and D, the increase in the T_{Si} leads to an enlarged on-state

current density (Fig. 2.18). In addition, the local current density is enhanced (suppressed) near the fin top (bottom). Since a FinFET with a tapered fin analogous to DG MOSFETs with different T_{Si} values in parallel, the I_{ON} is approximately linearly related to the average T_{Si} ($T_{average}$).

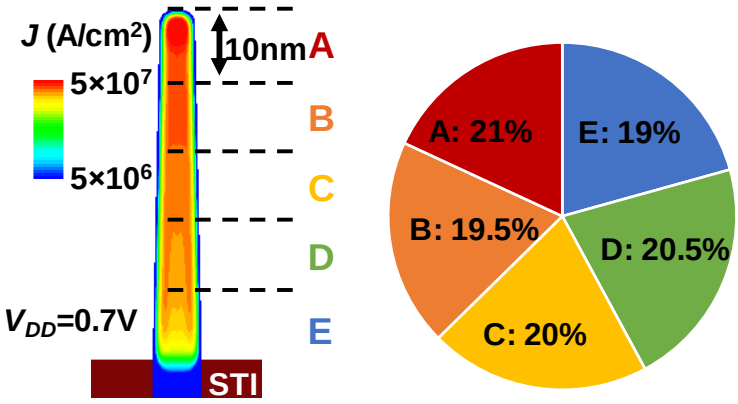

Fig. 2.18. The on-state current distribution in an n-FinFET with a realistic tapered fin (θ=1.5º).

The on-state performance of FinFETs has been reported to be strongly affected by the parasitic resistance [16,17]. Although the SDE parasitic resistance (R_{SDE}) is shown to be a significant parasitic component, the relation between the SDE doping profile and the on-state R_{SDE} has not been systematically analyzed in FinFETs with a gate underlap design. In this work, FinFETs with realistic doping diffusion gradient (Fig. 2.2(c)) are simulated to quantify the SDE doping's impact on the R_{SDE}.

The FinFET's $R_{S/D}$ consists of three components: the contact resistance (R_C), the epitaxial S/D region's resistance (R_{Epi}), and R_{SDE} (Fig. 2.19). The contact resistivity has been reduced to 10^{-9} Ω·cm^2, and the R_C is extracted to be 180 Ω per fin per side. The epitaxial S/D region has a relatively low resistance (45 Ω per fin per side) due to its high doping concentration and the large

conduction area. The R_{SDE} is extracted to be 345 Ω per fin per side in an n-FinFET with 0nm LR, and is identified as the largest component in the $R_{S/D}$.

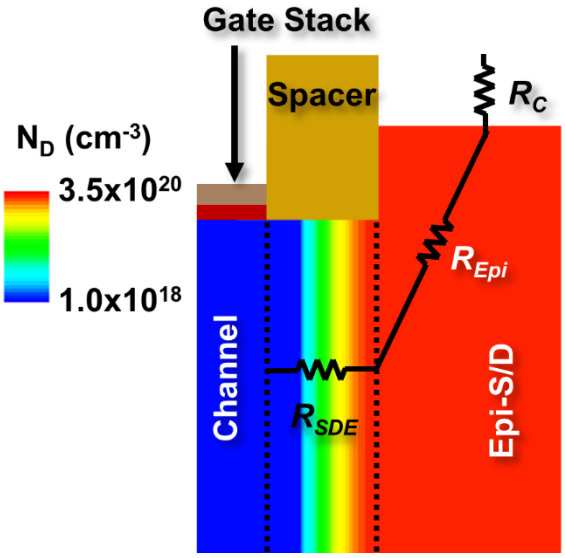

Fig. 2.19 Schematics of the parasitic resistance's component in 3-nm node n-FinFET.

In the SDE junction, the local resistivity can be calculated by $\rho=1/(q\cdot n\cdot\mu)$, where n is the on-state carrier density (Fig. 2.20(a)). Near the S/D and SDE junction, the n is dominated by the dopant diffusion from the heavily doped S/D. Although the high doping concentration degrades the mobility, the local resistivity is relatively low. Near the SDE and channel junction, the on-state carrier density is much higher (>100×) than the doping concentration. The local n is mainly modulated by the gate bias (through both fringing field in the spacer and carrier spill-over) and is <0.1× lower than that near the S/D and SDE junction. As a result, the R_{SDE} is dominated by the SDE and channel junction resistance (Fig. 2.20(b)). Increasing the LR by 1 nm can largely increase the n at 3 nm from the S/D and SDE junction (Fig. 2.21), leading to a R_{SDE} reduction. Meanwhile, the reduced voltage drop on the $R_{S/D}$ increases the intrinsic V_{GS} and the carrier concentration close to the SDE/channel interface, and thus forms a positive feedback to further reduce the R_{SDE}.

However, the R_{SDE} reduction effect saturates when LR>2.5 nm. Since the entire SDE region is relatively heavily doped, further increasing the dopant encroachment has little impact on the R_{SDE}.

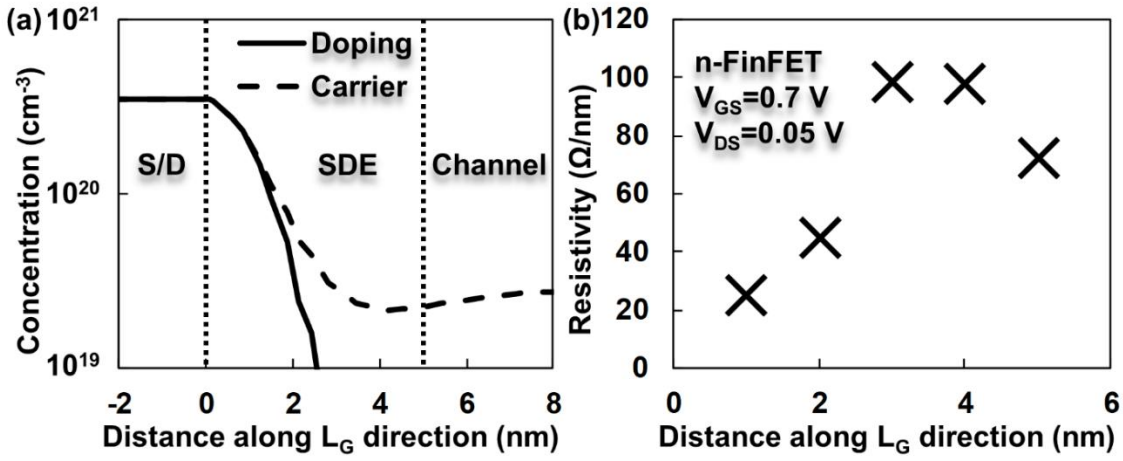

Fig. 2.20 (a) The doping and on-state carrier profile along the L_G direction in the SDE region of an n-FinFET without 3D SDE doping profile engineering, and (b) the corresponding resistivity. The carrier profile is extracted at 1 nm from the channel/gate stack interface, 25 nm from the fin top.

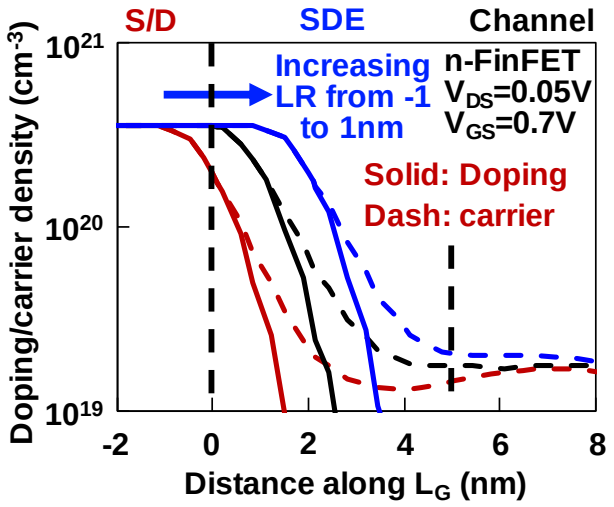

Fig. 2.21 The SDE doping profiles in FinFETs with various LRs and the corresponding carrier profiles near the SDE/channel junction.

2.4 Quantification of process-induced variabilities in 3-nm node FinFET

The FinFET performance variations induced by the examined sources are summarized in Fig. 2.22. The fin geometry's variation (taper angle θ and top fin width W_{fin} co-variation) is the dominating contributor for ΔI_{OFF}. Both the fin and the SDE (LR) are major sources for ΔI_{ON}. 3-nm node n-FinFETs with various geometry parameters are studied in detail to identify the physical mechanisms. Since the ΔI_{ON} and ΔI_{OFF} are governed by different physics, their sensitivities to the examined geometry parameters are different. The process-induced variabilities contributed by the studied models are analyzed individually.

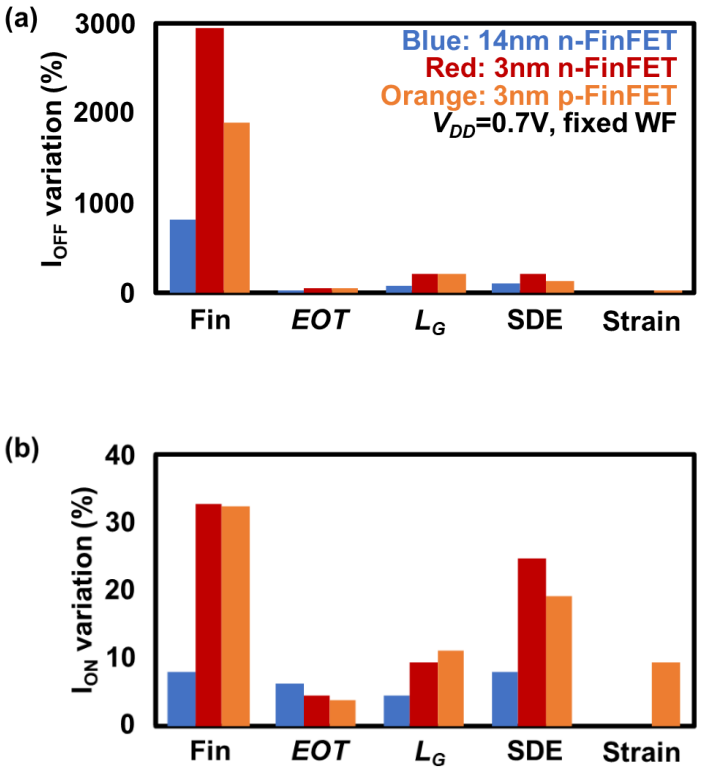

Fig. 2.22 (a) ΔI_{OFF} and (b) ΔI_{ON} induced by various sources in n- and p-FinFET without 3D SDE doping profile engineering.

2.4.1 Fin module induced variability

The fin geometry can be characterized by three parameters: fin height (H_{fin}), W_{fin}, and θ (Fig. 2.1(b)). ΔH_{fin} is tightly controlled by an advanced chemical-mechanical polish (CMP) process. Therefore, H_{fin} is fixed to be 50 nm. The fin module induced variability is caused by the θ and W_{fin} co-variation (Fig. 2.23).

In FinFETs with realistic tapered fins and a vertically uniform SDE doping profile, the leakage path is localized close to the sub-fin. This is caused by the relatively strong coupling between the drain fringing field and the virtual cathode (contributed by the relatively large local T_{Si} and the degraded gate modulation). The sub-threshold current is modulated by the change in the barrier height and the E_0 of the quantum confinement and demonstrates an exponential relation to the local T_{Si} close to the leakage path ($T_{leakage}$). Increasing the leakage path thickness ($T_{leakage}$) by 1 nm (from 7 to 8 nm) can lead to a 22 meV reduction in the barrier height in the off state. Meanwhile, the E_0 is also reduced by 7meV, further reducing the I_{OFF}. The θ and W_{fin} co-variation can lead to ±3 nm $\Delta T_{leakage}$, and consequently, cause ~630× ΔI_{OFF} (Fig. 2.23(b)). Therefore, the fin module's variation is identified as the dominating contributor of ΔI_{OFF}.

Since I_{ON} flow through the entire fin (Fig. 2.12(c)), it is sensitive to the $T_{average}$. Although the $\Delta T_{average}$ can lead to changes in the mobility [54], C_{Si} [46], and $R_{S/D}$, their impact counterbalance to each other, and result in a relatively small Δg_m (<5%). Consequently, $\Delta I_{ON} \approx \Delta V_{TH} \times g_m$. Since the V_{TH} is approximately linearly related to the T_{Si} (Fig. 2.17), the ΔI_{ON} shows a linear relation to the $\Delta T_{average}$ induced by the W_{fin} and θ co-variation (Fig. 2.23(c)).

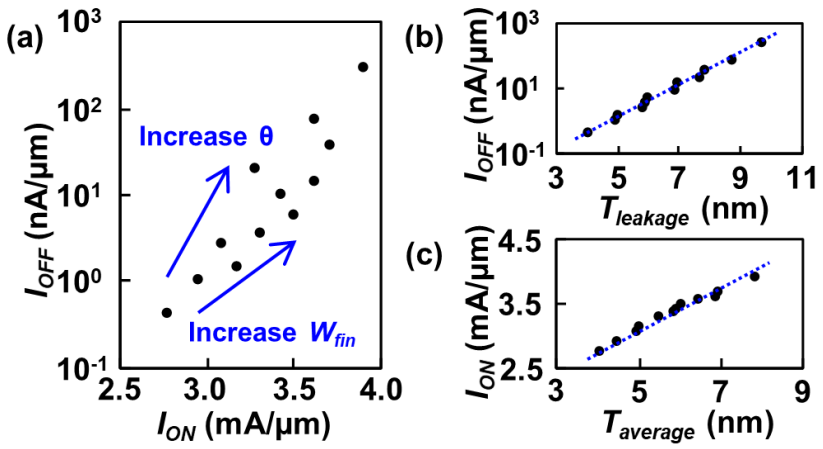

Fig. 2.23 Fin module induced variability in n-FinFETs without 3D SDE doping profile engineering. (a) The I_{OFF}-I_{ON} distribution, (b) and (c) I_{OFF} and I_{ON} as a function of $T_{leakage}$ and $T_{average}$, respectively.

As the FinFETs are scaled down, the H_{fin} has been continuously increased to improve the effective conduction width and current density per footprint. In a tapered fin, $T_{Si}=W_{fin}+2\times H\times tan(\theta)$. Although advanced fin etching technologies have been developed to reduce θ from 2.5º in 10-nm node to 1.5º in 3-nm node, the $\Delta\theta$-induced $\Delta T_{leakage}$ and $\Delta T_{average}$ are similar in absolute value. Since the overall fin thickness is reduced to improve the electrostatic control, the $\Delta T_{leakage}$ and $\Delta T_{average}$ become larger in percentage. Consequently, the ΔI_{ON} (ΔI_{OFF}) induced by the fin module increases by 4.1× (3.6×) from the 14-nm node to 3-nm node. More importantly, the relatively large $T_{leakage}$ (~7 nm, close to the sub-fin) degrades the leakage path electrostatic control, increasing the SS and reducing the I_{ON}/I_{OFF} at a fixed V_{DD}. Therefore, reducing the θ without degrading the fin's robustness is crucial for digital performance enhancement in future generation FinFETs.

2.4.2 Gate stack module induced variability

The gate module has a substantial impact on both FinFET and planner FETs' performances in previous generations. However, the Δ*EOT* induced variability is predicted to be not as significant in 3-nm node FinFETs. This study assumed that carrier mobility does not degrade when EOT is reduced, which can be achieved by advanced gate stack processing. In the nominal fin architecture (Fig 2.1(b)), the C_{Si} is extracted to be 6.68 μF/cm^2, equivalent to 0.52 nm of *EOT*, and is comparable to C_{OX} (0.6 nm *EOT*). Consequently, an *EOT* reduction from 6.5 Å to 5.5 Å leads to only a 9% increase in C_G (Fig. 2.24). In addition, the high electric-field induced mobility degradation counterbalances the increase in carrier density, and the 3-nm node has a small ΔI_{ON} caused by *EOT* variation. The ΔI_{OFF} results from the change in both V_{TS} and *SS*. When *EOT* varies from 6.5Å to 5.5Å, the electrostatic control improves. Therefore, V_{TS} increases by ~7mV (less DIBL), and *SS* reduces by ~3mV/dec (Fig. 2.13(b)). The ΔI_{OFF} caused by ΔEOT (~50%) is relatively small compared to that induced by fin geometry variation (over 100× as shown in Fig. 2.23).

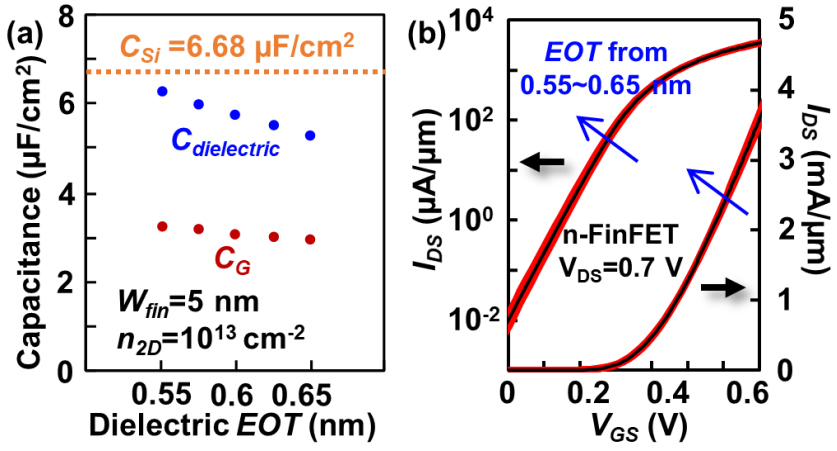

Fig. 2.24 (a) $C_{dielectric}$ and C_G vs. gate dielectric *EOT*, and (b) gate stack induced performance variation in 3-nm node n-FinFET.

2.4.3 SDE module induced variability

The SDE doping has a substantial impact on both the R_{SDE} and the virtual cathode and drain fringing field coupling, and consequently results in ΔI_{ON} and ΔI_{OFF} [17]. Increasing the LR from -1 nm (under-etch in the fin recess) to 1 nm (over-etch in the fin recess) can increase the dopant in the relatively lightly doped SDE region (Fig 2.21) and reduce R_{SDE} by ~40% (Fig. 2.25). The dopant encroachment also results in a stronger coupling between the virtual cathode and the drain fringing field. Therefore, the degraded DIBL increases the gate over-drive, further increasing the I_{ON}. Combined with the R_{SDE} reduction, a ~30% higher I_{ON} is observed. However, the degraded SCE enlarges the *SS* and I_{OFF}. Although a tight LR control can be achieved through advanced recess etch process, ±1 nm ΔLR can lead to ~31mV ΔV_{TS}. It is comparable to ΔV_{TS} induced by metal gate granularity (MGG), which is reported to be a significant variability source. Consequently, it is critical to suppress the device performances' sensitivity to the ΔLR. This can be achieved by improving the electrostatic control through both fin trimming and 3D SDE doping profile engineering.

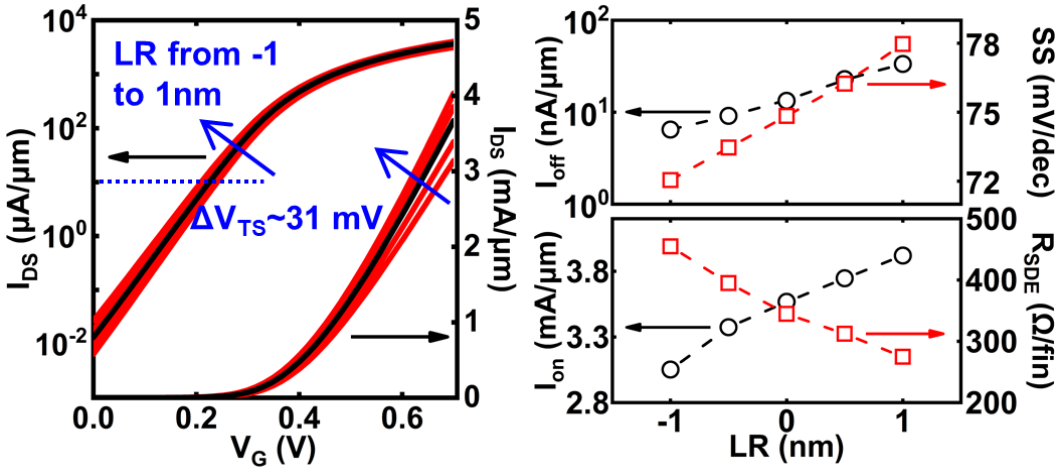

Fig. 2.25 ±1 nm ΔLR induced performance variation in 3-nm node n-FinFETs without 3D SDE doping profile engineering.

2.4.4 Comparison between n- and p-FinFET

In 3-nm node p-FinFET with s-$Si_{0.75}Ge_{0.25}$ channel, the relatively small bandgap leads to a much larger tunneling leakage than that in n-FinFET. In this work, the tunneling leakage is simulated by a calibrated band-to-band tunneling model [59]. A ~3nA/μm tunneling leakage current is observed (Fig. 2.26) and agrees with experimental data [60]. Since the tunneling leakage is less sensitive to the fin geometry, the fin module induced ΔI_{OFF} in percentage is smaller than that in n-FinFET (Fig. 2.22(a)).

The gate stack module induced variabilities in p-FinFET are similar to those in n-FinFET (Fig. 2.22). Although the hole has a larger effective mass, the quantum capacitance (equivalent to 0.47 nm of *EOT*) is comparable to that in n-FinFET (equivalent to 0.52 nm of *EOT*). As a result, the ±0.05 nm ΔEOT has similar impact on C_G and device performances.

The S/D Ge composition's variation acts as a source of ΔI_{ON} in p-FinFET. Since the epitaxial S/D regions are utilized as stressors for channel mobility improvement, the ±5% Ge composition variation in the S/D formation can lead to a ±0.27 GPa change in the channel stress. The stress-variation-induced change in mobility and quasi-ballistic velocity results in a 9% ΔI_{ON}.

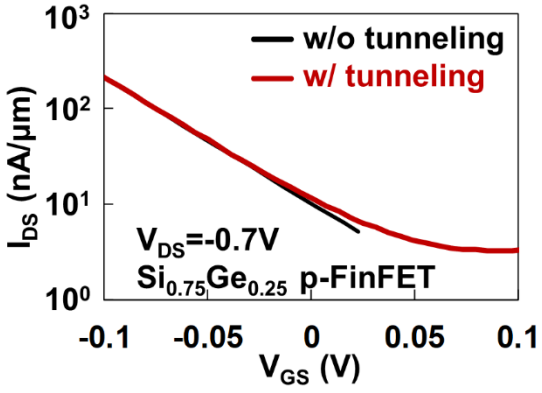

Fig. 2.26 Tunneling leakage current in the nominal s-$Si_{0.75}Ge_{0.25}$ p-FinFET

2.5 Variability suppression by 3D SDE doping profile engineering

2.5.1 Physical interpretation and quantification

The variability quantification shows that the ΔV_{TS}, induced by both the fin and SDE module, is a significant contributor for both ΔI_{ON} and ΔI_{OFF}. In 3-nm node FinFETs with a tapered fin, the localized leakage path indicates that the sub-threshold performance's variation, including ΔV_{TS} and ΔSS, can be reduced by improving the electrostatic control around the leakage path. This can be effectively achieved by 3D SDE doping profile engineering.

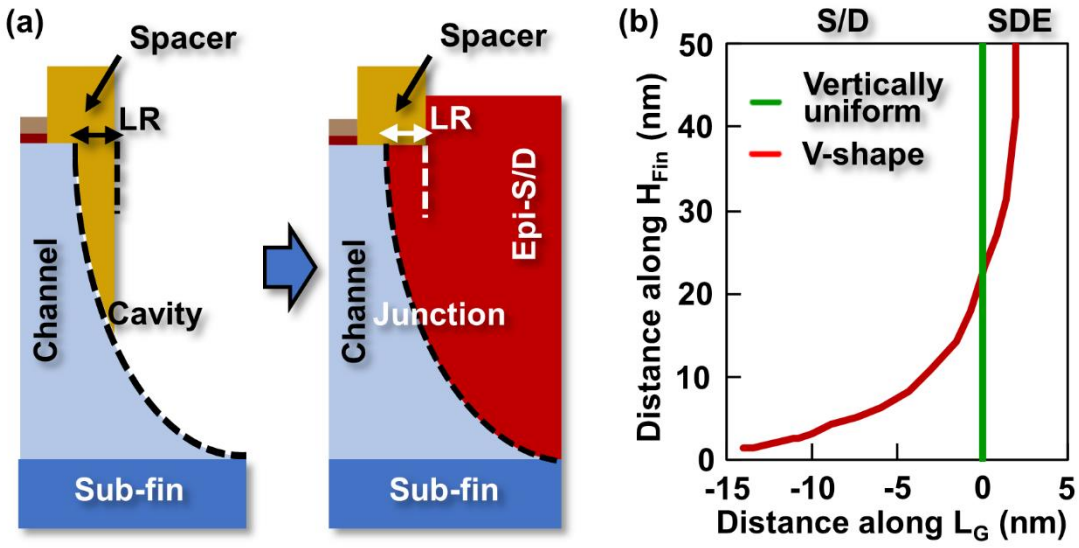

Fig. 2.27 Schematics of 3D SDE doping profile engineering. (a) The formation process (not to scale), and (b) the resulting doping profile extracted from TEM.

The 3D SDE doping profile engineering can be achieved with minimal modification in the FinFET's process flow (Fig. 2.27). By employing an isotropic S/D recess etch technology followed by bi-layer Si:As/Si:P epitaxy regrowth, a V-shape S/D and SDE profile (Fig. 2.27(b)) can be achieved (extracted from TEM, Fig. 2.2(b)). The V-shape profile features reduced dopant

encroachment near the sub-fin, resulting in a weaker local virtual cathode and drain fringing field coupling. Therefore, the virtual cathode and the leakage path is sifted towards the fin top (Fig. 2.28), and the local electrostatic control is significantly improved by the reduced $T_{leakage}$ (from ~7 nm to ~5.5 nm) combined with the top gate electric field. Consequently, the device performances' sensitivities to geometry parameters are suppressed. In addition, since $\Delta T_{leakage}=\Delta W_{fin}+2\times H\times tan(\Delta\theta)$, the leakage path shift also reduces $\Delta\theta$ induced $\Delta T_{leakage}$, further reducing the fin module induced variability. For the on-state performance, the reduction in SDE doping near the sub-fin leads to a larger local R_{SDE} and smaller I_{ON}. However, the increased fin top SDE doping reduces the local R_{SDE}, counter-balancing the overall R_{SDE} reduction. More importantly, the improved electrostatic control reduces SS and increases gate over-drive at a fixed I_{OFF}, further improving the I_{ON}. As a result, the I_{ON} values are comparable (Δ<0.5%) in the nominal FinFETs with different SDE doping profiles.

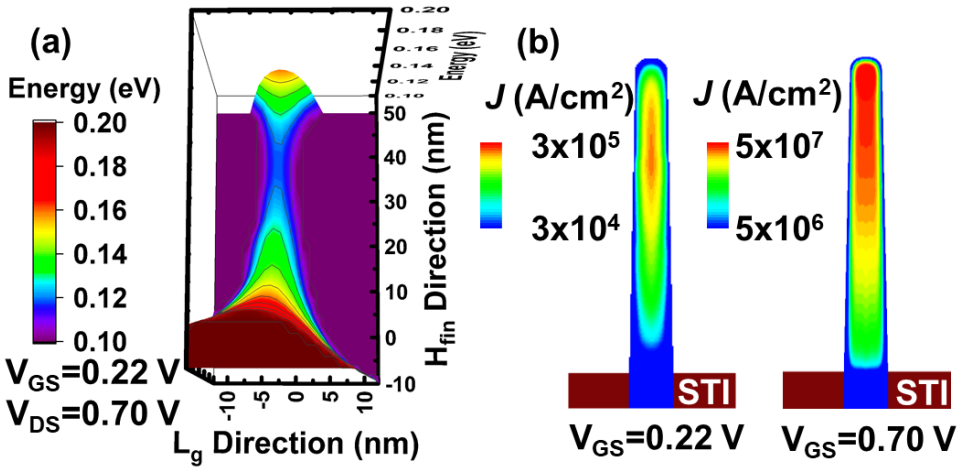

Fig. 2.28 Impact of V-shape SDE on device performance. (a) The sub-threshold energy barrier profile, and (b) the sub-threshold and on-state current density distribution in the fin cross-section.

Fig. 2.29 and Fig. 2.30 show the fin and SDE module induced variability in FinFETs with various SDE doping profiles, respectively. Compared to the vertically uniform SDE, the V-shape SDE suppresses the fin module induced ΔI_{ON} and ΔI_{OFF} by 1.6× (1.3×) and 4.0× (2.7×) in n-(p-)FinFET, respectively. In addition, the ±1 nm ΔLR induced I_{ON} variation is reduced by 1.8× (2.1×) in n-(p-)FinFET.

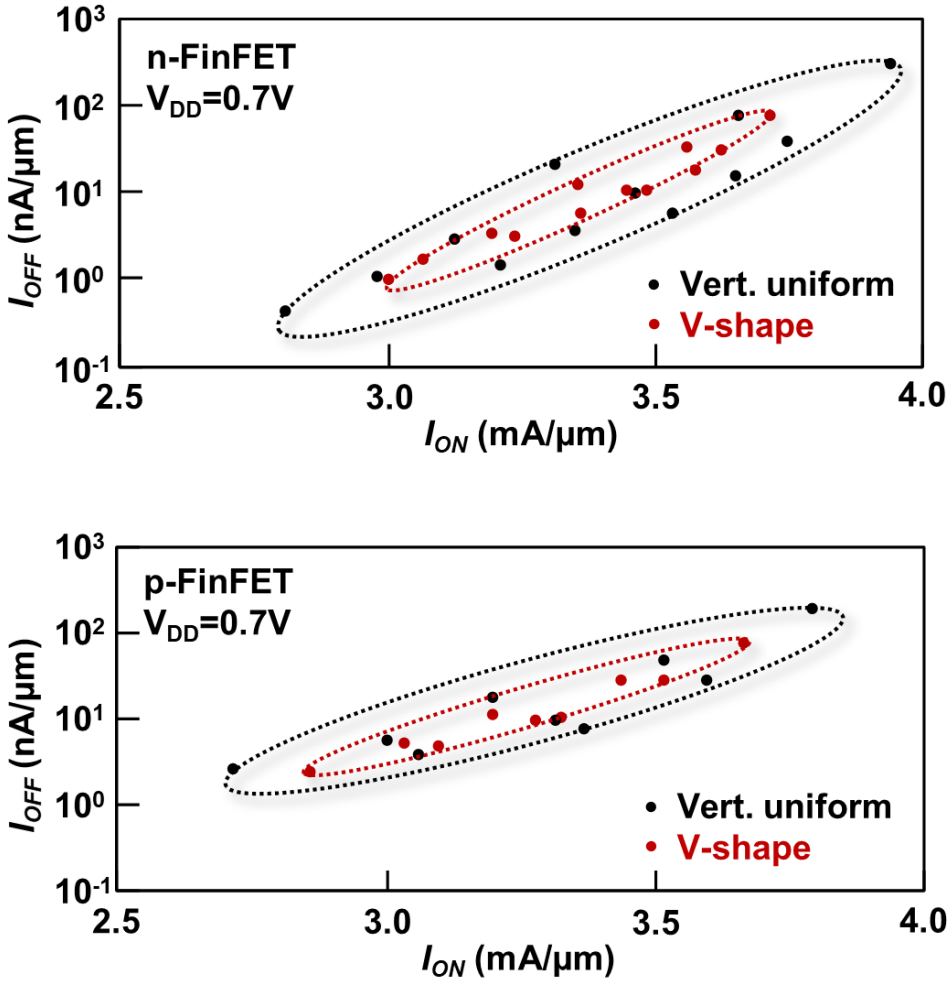

Fig. 2.29 Fin module induced I_{ON}-I_{OFF} variation in 3-nm FinFETs with various SDE doping profiles.

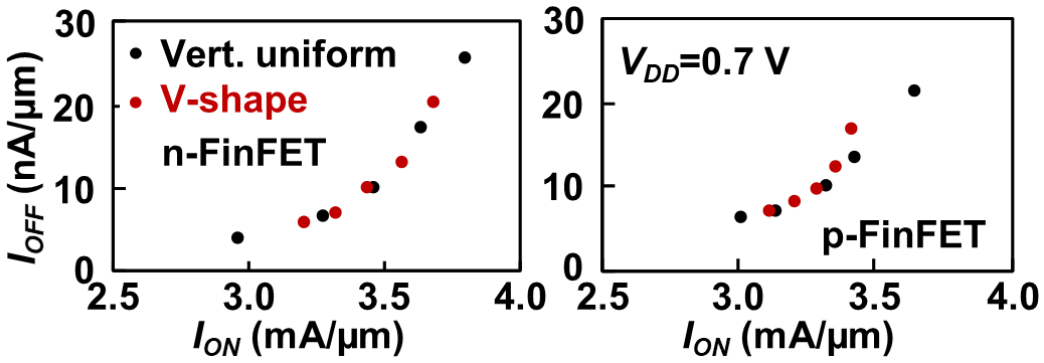

Fig. 2.30 SDE module induced I_{ON}-I_{OFF} variation in 3-nm FinFETs with various SDE doping profiles.

2.5.2 Limitations of the V-shape SDE doping profile

Although the V-shape SDE doping profile with LR=2 nm can lead to performance enhancement in the 7/10-nm node FinFETs [17], no increase in I_{ON}/I_{OFF} is observed in the 3-nm node (Fig. 2.29). As discussed before, the trade-off between electrostatic control and the on-state R_{SDE} is the key for the I_{ON}/I_{OFF} enhancement. Fig. 2.31 shows the device performance as a function of LR to find out the optimal dopant encroachment. For all the transistors, I_{OFF} is fixed at 10nA/μm for high power (HP) application, as indicated in ITRS. Maximized I_{ON}/I_{OFF} can be achieved at LR=2 nm and 2.5 nm in n- and p-FinFET with the V-shape SDE doping profile, respectively. This result is consistent with the experimental data in 10-nm node FinFETs [17]. However, the optimal I_{ON}/I_{OFF} values are close to (Δ<1%) the value in FinFETs without 3D SDE doping engineering. The performance enhancement effect is limited by the relatively low SDE doping and on-state current density close to the sub-fin (Fig. 2.28). A novel strategy of the 3D SDE doping profile's optimization needs to be investigated for performance enhancement in the 3-nm node.

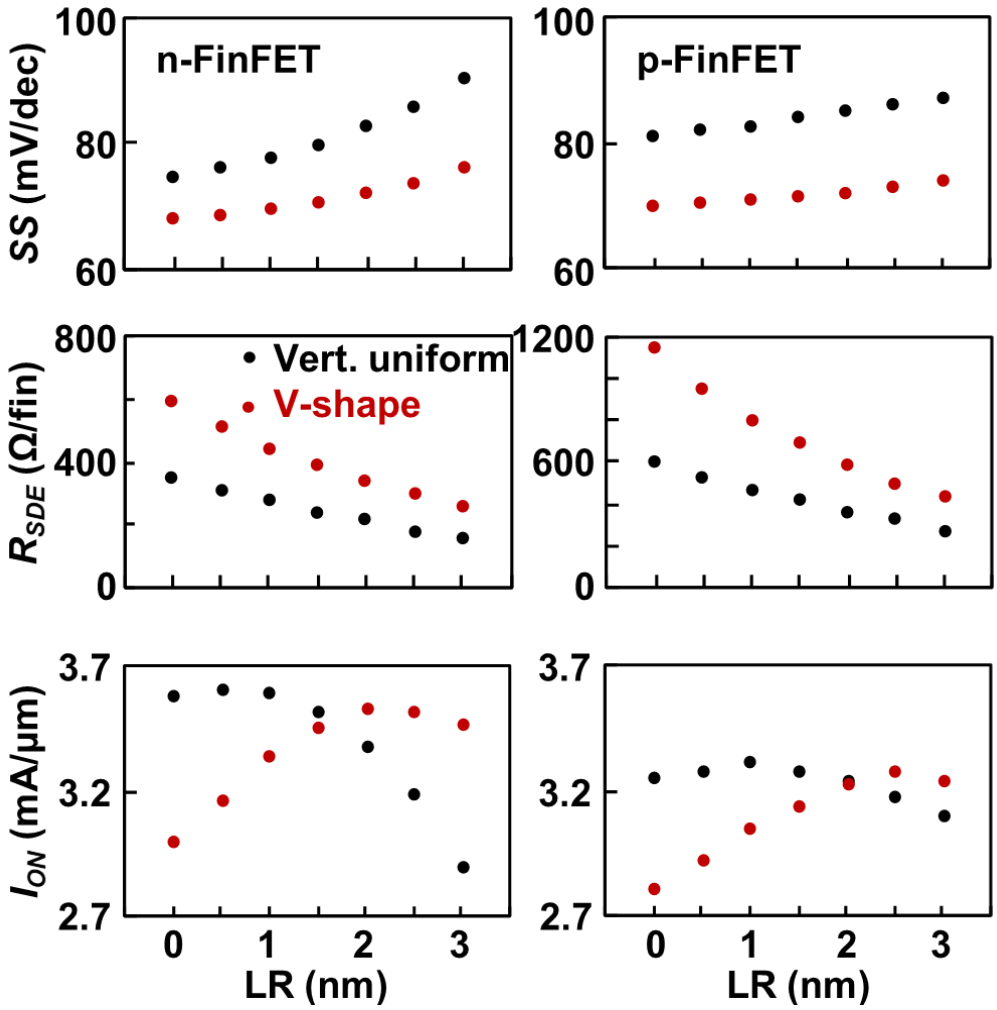

Fig. 2.31 Device performances vs. LR in 3-nm node n-/p-FinFETs with vertically uniform and V-shape SDE doping profiles. All transistors have fixed I_{OFF}=10 nA/μm.

2.6 Summary

In this section, the process variabilities induced by different modules are quantified in 3-nm node FinFETs, and the governing physical mechanisms are systematically analyzed. In FinFETs with tapered fins and vertically uniform SDE doping profiles, the leakage path is localized close to the fin bottom, while the I_{ON} flows relatively uniformly in the fin cross-section. Consequently, the ΔI_{ON} and ΔI_{OFF} show different sensitivities to the geometry parameter's variation. The fin geometry's variation (taper angle θ and top fin width W_{fin} co-variation) is the

dominating source for ΔI_{OFF}. Both the fin etching and the SDE recess etch process are major contributors for ΔI_{ON}. The localized leakage path indicates that the variabilities can be suppressed by enhancing the local electrostatic control, which can be effectively achieved through 3D SDE doping profile engineering. A V-shape SDE doping profile can enhance the electrostatic control by shifting the leakage path towards the fin top, suppressing the device performances' sensitivities to the geometry parameters.

Although the V-shape SDE doping profile is developed to improve the I_{ON}/I_{OFF} in 7/10-nm node FinFETs, no I_{ON}/I_{OFF} improvement is observed in the 3-nm node FinFET. In SDE doping profile engineering, the trade-off between *SS* (sensitive to the SDE doping, poly pitch, *EOT*, and fin's geometry) and the on-state R_{SDE} (mainly sensitive to the SDE doping) has been identified as the key for the I_{ON}/I_{OFF} enhancement. Consequently, the 3D SDE doping profile needs to be optimized based on the channel and gate stack's physical parameters in future generation transistors to maximize the I_{ON}/I_{OFF}.

Chapter 3

3-nm node FinFET's Performance Enhancement through 3D SDE Doping Profile Engineering

3.1 Introduction

Compared to planner FETs, FinFET provides increased conduction width per footprint and enhanced current drive, which are preferred for digital applications. Advanced S/D formation technologies have been developed to precisely control the fin top LR and the vertical profile (in the fin height direction), enabling new dimensions of freedom for design optimizations to further improve the I_{ON}/I_{OFF}. Although the experimental V-shape doping profile can be utilized to improve the I_{ON}/I_{OFF} in the 7/10-nm node FinFETs, it cannot improve the I_{ON}/I_{OFF} in the 3-nm node. To the best of the author's knowledge, no optimization methodology has been proposed for the vertically non-uniform SDE module. In this chapter, an optimization strategy of the 3D SDE doping profile is proposed for 3-nm node FinFETs with realistic physical parameters, improving I_{ON}/I_{OFF} while maintaining the variability suppression effect.

Although FinFETs can achieve superior digital performance compared to bulk an SOI FETs, their analog performance, especially the f_T, is inferior compared to bulk and SOI transistors (Fig. 3.1) [16], posting major challenges for their SoC applications. In FinFETs, the analog performance is largely degradation by the parasitic components. Since the 3D SDE doping profile engineering can effectively reduce the R_{SDE} and $R_{S/D}$, it is proposed as an analog performance enhancement method in 3-nm node FinFETs. In addition, enabled by the advanced S/D formation technologies, a reduction in $C_{parasitic}$ can be achieved by spacer and SDE module co-optimization and further enhance f_T. In this work, an SDE doping and spacer length co-optimization process is

demonstrated. The contributions of parasitic resistance and capacitance reduction on f_T enhancement are quantified, guiding analog performance optimization in future generation FinFETs and GAAFETs.

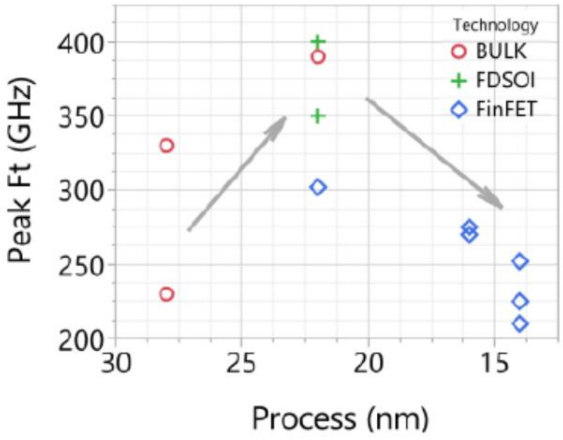

Fig. 3.1 f_T trends by process node [16]. f_T in FinFETs are lower than that in bulk and SOI transistors.

3.2 Digital performance optimization

3.2.1 Optimization methodology

As discussed before, the performance enhancement effect in a V-shape SDE doping profile is limited by the relatively low on-state current density close to the sub-fin. To further understand the physical insight, the on-state current distribution in an n-FinFET with the nominal fin shape, a V-shape SDE doping profile, and 2 nm LR is investigated in detail. The fin is uniformly separated into five sections along the fin height direction, and the on-state current contributed by each section is summarized in Fig. 3.2. Section E has the smallest I_{ON} due to its least SDE dopant encroachment.

The *SS* is limited by the coupling between the gate and virtual cathode, which is located at ~15 nm from the fin top (in section B, Fig. 2.19). This is confirmed by the fact that the local value

in section B limits the overall *SS* (72.0 mV/dec) (Fig. 3.3). Since the local *SS* values in other sections, especially sections D and E close to the sub-fin, are smaller than the overall *SS*, the local SDE doping concentration can be increased, trading electrostatic control for R_{SDE} reduction. As a result, the overall R_{SDE} can be reduced without degrading the sub-threshold performances and the gate overdrive, and the I_{ON}/I_{OFF} can be improved. The localized leakage path near the fin top also maintains the variability suppression effect, especially the reduction of $\Delta\theta$ induced performance variation. The gate to virtual cathode coupling is sensitive to both the fin module and the SDE doping. Therefore, the 3D SDE doping profile needs to be optimized with respect to geometry parameters in the fin.

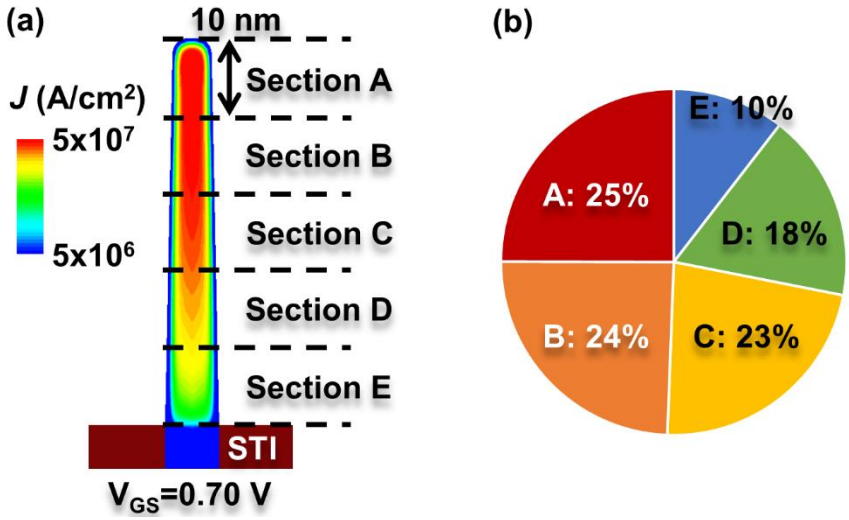

Fig. 3.2 On-state current in an n-FinFET with the nominal fin shape, a V-shape SDE doping profile, and 2 nm LR. (a) The current distribution and the illustration of five sections, and (b) on-state current contribution from each section.

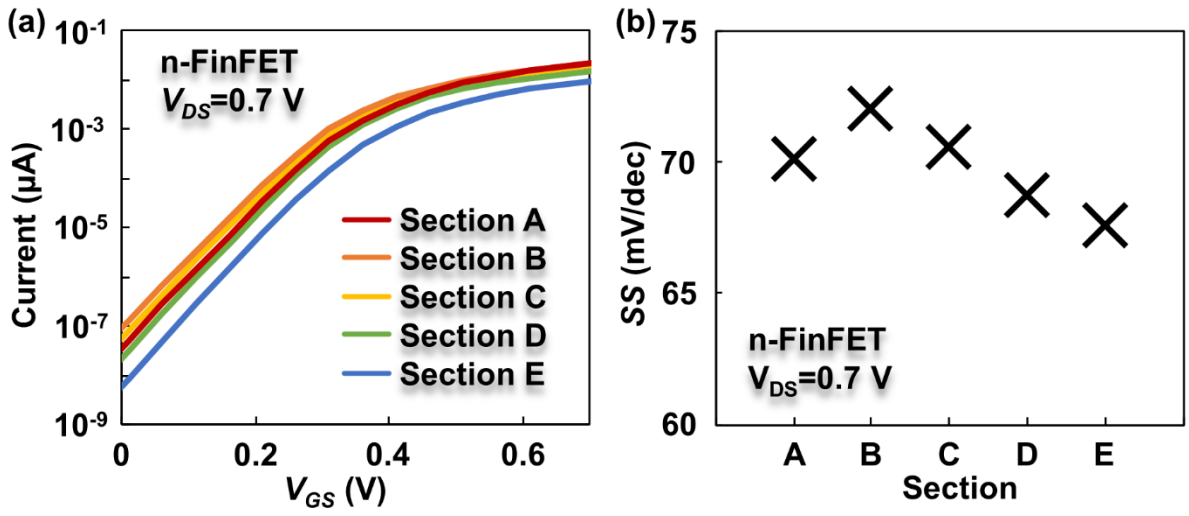

Fig. 3.3 (a) I_{DS}-V_{GS} characteristics and (b) *SS* in each section in an n-FinFET with the nominal fin shape, a V-shape SDE doping profile, and 2 nm LR.

3.2.2 Optimization result

LR from 0 to 3 nm (by a step of 0.5 nm) is tested to find the optimum SDE doping profile. For each LR value, the vertical profile is fine-tuned so that the local dJ_{DS}/dV_{GS} at different locations along the H_{fin} direction matches the value at the virtual cathode (overall *SS*). Fig. 3.4 shows the optimized SDE doping profile. The resulting sub-threshold and on-state current distribution in 3-nm node n-FinFETs are demonstrated and compared in Fig. 3.5. A similar trend is observed in p-FinFETs. Since p-FET has a lower peak doping concentration (1×10^{20} cm^{-3}) than n-FET (3.5×10^{20} cm^{-3}), the optimum dopant encroachment is larger than that in the n-FinFET. The optimized profiles in both n- and p-FinFET feature larger dopant encroachment close to the sub-fin compared to the V-shape profile, reducing the overall R_{SDE} without degrading the *SS* (Fig. 3.6). This is consistent with the theoretical analysis. As a result, 7% (10%) I_{ON}/I_{OFF} enhancement can be achieved (Fig 3.7) by increasing the current density close to the sub-fin in n-(p-)FinFETs.

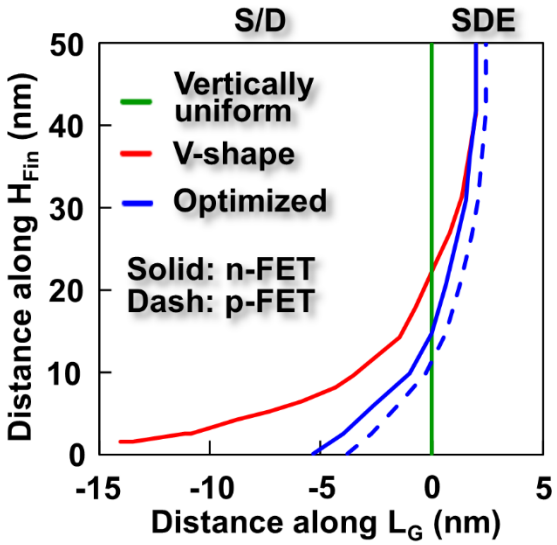

Fig. 3.4 The optimized 3D SDE doping profile in 3-nm node n- and p-FinFET.

Since the leakage path in a FinFET with the optimized SDE doping profile is localized near the fin top, suppressed fin (Fig 3.6) and SDE module (Fig. 3.8) induced variabilities are observed. Compared to the V-shape profile, the optimized profile trades local electrostatic control for R_{SDE} reduction close to the sub-fin. Consequently, the device performances become more sensitive to geometry variations. However, numerical analysis shows the increases in fin and SDE process-induced ΔI_{ON} and ΔI_{OFF} are relatively small. The optimized SDE profile suppresses the fin module induced ΔI_{ON} and ΔI_{OFF} by 1.6× (1.3×) and 3.9× (2.6×) in n-(p-)FinFET, respectively. In addition, the ±1 nm ΔLR induced I_{ON} variation is reduced by 1.8× (2.1×) in n-(p-)FinFET.

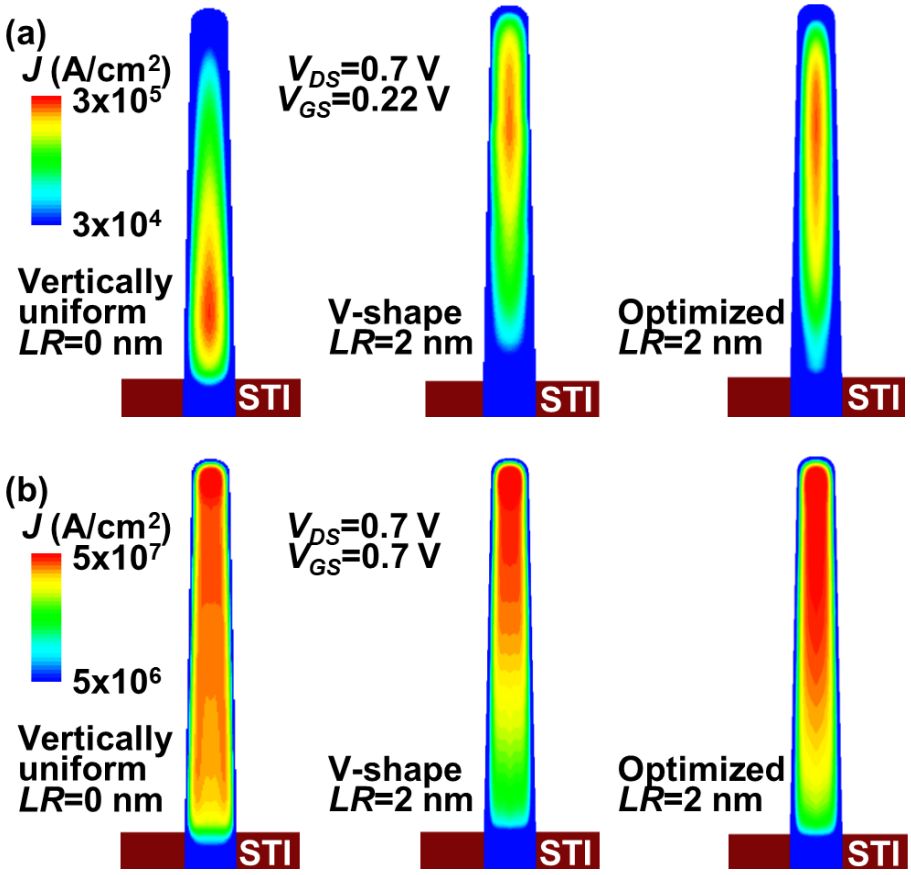

Fig 3.5. Current density distribution in 3-nm node n-FinFETs with different SDE doping profiles.

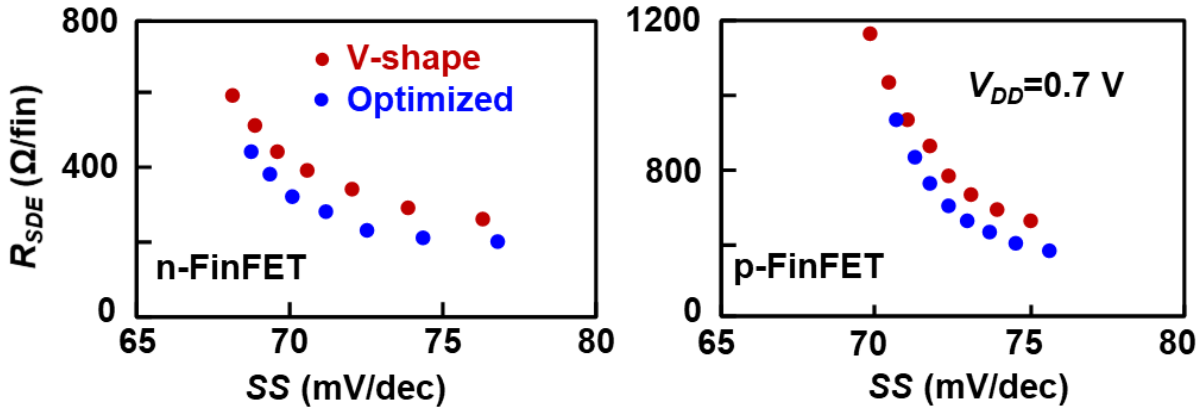

Fig. 3.6 The R_{SDE}-*SS* trade-off in 3-nm node n- and p-FinFETs with the V-shape and the optimized SDE profiles.

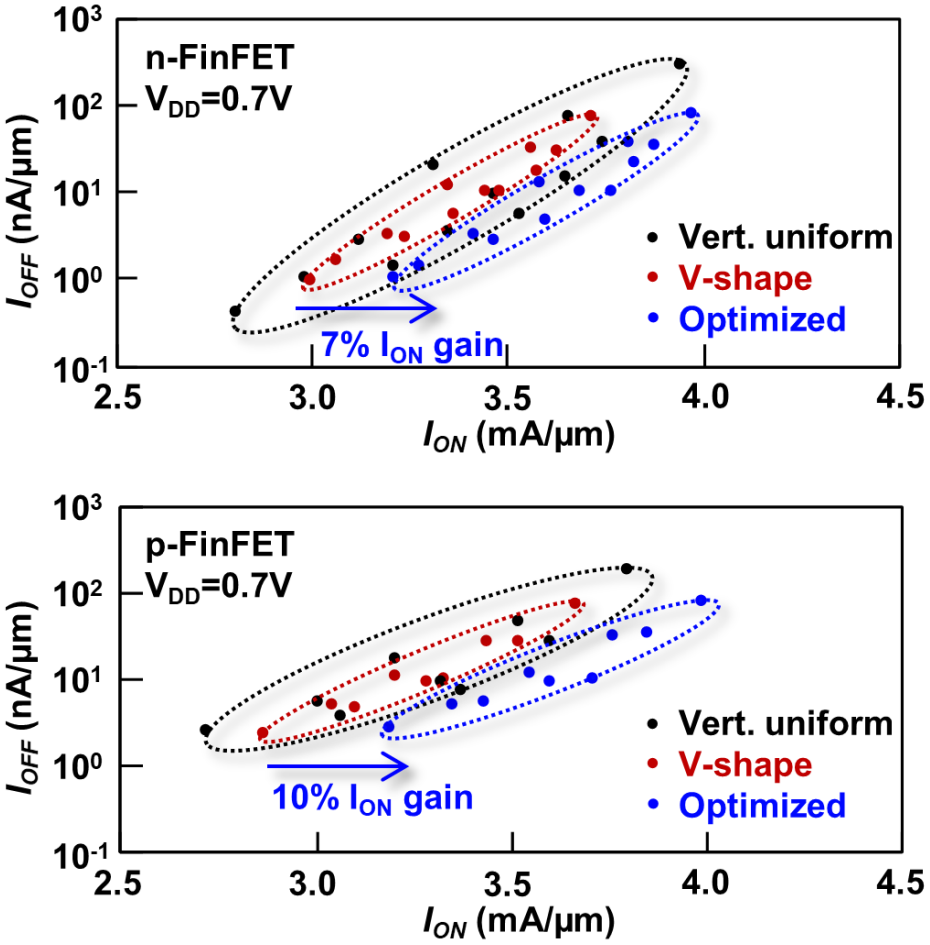

Fig. 3.7 Fin module induced variability in 3-nm node n- and p-FinFETs with various SDE doping profiles.

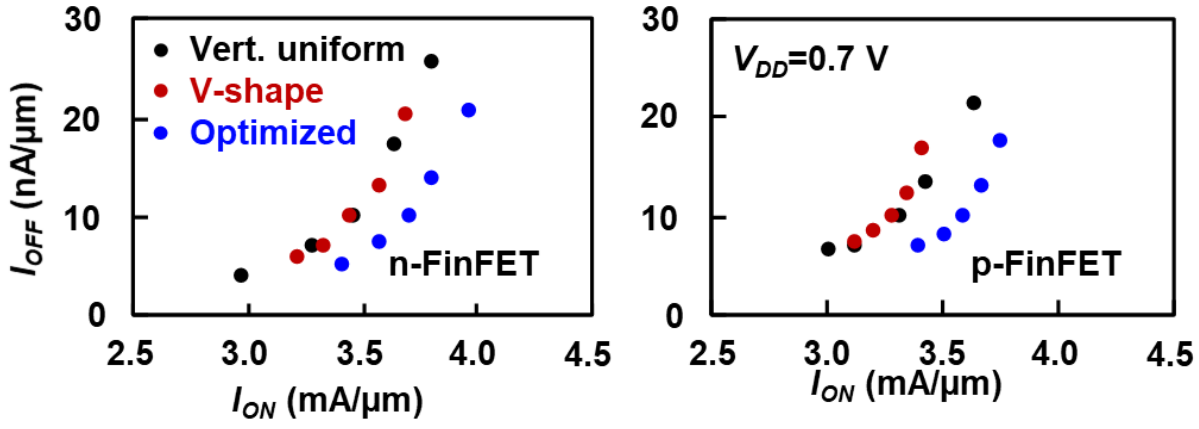

Fig. 3.8 SDE module induced variability in 3-nm node n- and p-FinFETs with various SDE doping profiles.

3.3 Analog performance analysis and optimization

3.3.1 Benchmark of 3-nm node FinFET's analog performance

FinFETs have improved electrostatic control, resulting in relatively high output resistance (R_{out}), favorable for analog applications. However, the f_T values in the 14/22-nm node FinFETs are relatively low compared to SOI and bulk transistors, limiting their SoC applications. To the first order, f_T can be predicted by the equation:

$$f_T = \frac{g_{mext}}{2\pi \cdot C_{total}}$$

where g_{mext} is the extrinsic transconductance and C_{total} is total capacitance up to Metal 2 routing. g_{m_ext} can be calculated by

$$g_{mext} = \frac{g_{m\mathrm{int}}}{1 + g_{m\mathrm{int}} \cdot R_{S/D}}$$

where g_{mint} is the intrinsic transconductance and is proportional to the carrier transport velocity. FinFETs have relatively low f_T mainly because of three reasons: the surface roughness and interface defect induced mobility degradation, the relatively large parasitic resistance, and the increasing parasitic capacitance as the poly pitch is scaled down. The former two factors contribute to the reduction of g_{mext}, and the latter factor substantially increases C_{total}.

Fig. 3.9 shows a comparison between the 3-nm node FinFETs without 3D SDE engineering and the extensively studied 14-nm node FinFET. 3-nm FinFET has a much larger g_{mext} because of the increased effective conduction width (taller fin), reduced $R_{S/D}$, and improved quasi-ballistic transport velocity caused by the shorter L_G. Meanwhile, the reduced $R_{S/D}$ also leads to higher gain-power efficiency (g_{mext}/I_{DS}) (reduced $I_{DS}^2 \cdot \mathrm{R_{S/D}}$). Both the improvements are favorable for analog applications.

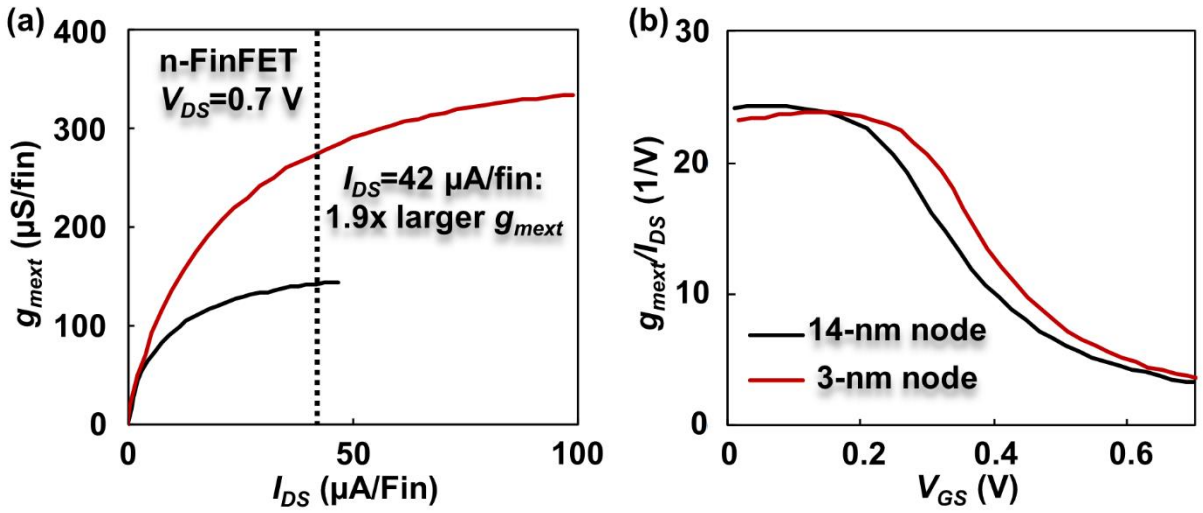

Fig. 3.9 Comparison of (a) transconductance and (b) gain-power efficiency between 3nm-node and 14-nm node.

Fig. 3.10 demonstrates the schematics of capacitor components. C_{total} has four components: C_G, the spacer capacitance (C_{spacer}) due to the coupling between the gate metal and the heavily doped S/D regions, the MoL capacitance (C_{MoL}) due to the coupling between the gate and source/drain contact metal, and BEoL capacitance (C_{BEoL}) due to the coupling between the metal wiring up to Metal 2 routing. This study assumes that BEoL metal routing is scaled ideally, and consequently, the C_{BEoL} does not change between generations. The C_{BEoL} value is extracted from Intel's 14-nm node experimental data. AC simulations are performed to analyze the C_G, C_{spacer}, and C_{MoL} in the 3-nm node FinFETs. The contact metal's geometries are estimated based on the parameters in the TSMC's 7-nm node technology. The capacitor components are summarized in Table II. The spacer length (L_{spacer}) is scaled from 10 nm (14-nm node) to 5 nm (3-nm node), leading to a stronger coupling between the gate metal and the S/D increases C_{spacer} and C_{MoL}. However, the reduction in fin pitch from 42 nm to 26 nm reduces the coupling area, counter-balancing the increase in C_{spacer} and C_{MoL}. In addition, the ε_r of the spacer is reduced from

6.5 to 4.5 through material engineering, further reducing the parasitic capacitances. As a result, the C_{spacer} and C_{MoL} increase by ~10%, contributing to ~19% of the C_{total}.

AC simulations show that the 3-nm node n-FinFET has a peak f_T=490 GHz, much higher than the values (~400 GHz) in previous generation bulk and SOI transistors. This is mainly caused by the improvement in conduction width per fin and the resulting g_{mext} increase. The number serves as an upper limit of f_T in the 3-nm node.

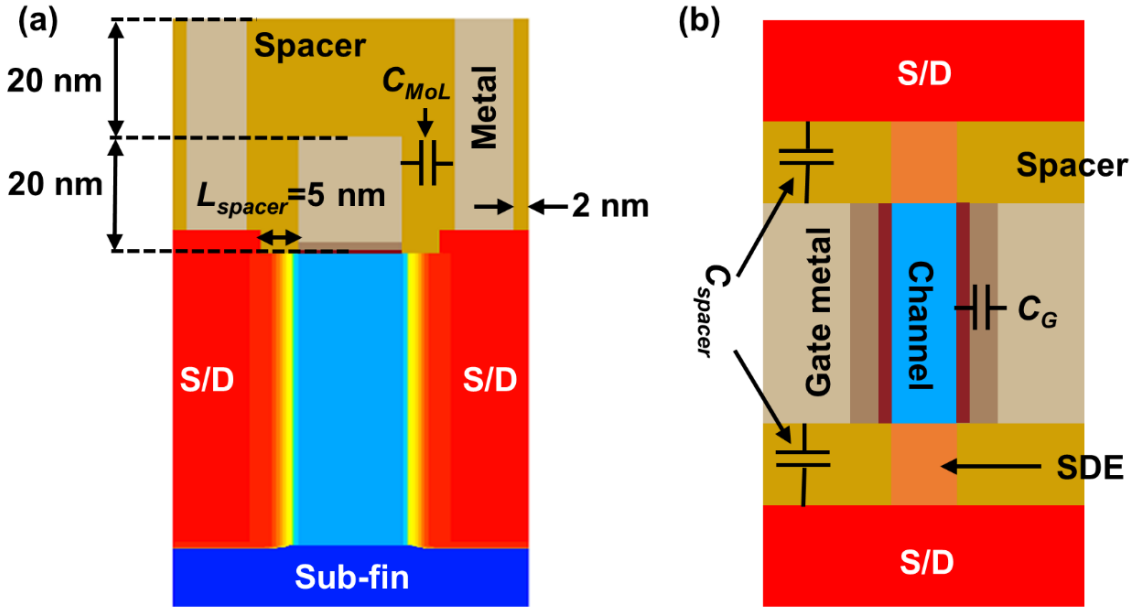

Fig. 3.10 Schematics of 3-nm node FinFET's capacitor components in FEoL and MoL (not to scale). (a) Cross-section along the L_G direction in the middle of the fin, and (b) perpendicular to the H_{fin} direction.

Table 3.1 Capacitor components in simulated 3-nm node and Intel's 14-nm node n-FinFETs

Component	3-nm node n-FinFET	14-nm node n-FinFETs
Gate capacitance (C_G)	4.36×10^{-17} F/fin	4.70×10^{-17} F/fin
Spacer capacitance (C_{spacer})	0.80×10^{-17} F/fin	0.75×10^{-17} F/fin

MoL capacitance (C_{MoL})	1.02×10^{-17} F/fin	0.92×10^{-17} F/fin
BEoL capacitance (C_{BEoL})	3.60×10^{-17} F/fin	3.60×10^{-17} F/fin
Total capacitance (C_{total})	9.78×10^{-17} F/fin	9.97×10^{-17} F/fin

3.3.2 Analog performance optimization

Although the 3-nm node FinFET is predicted to have an improved f_T compared to the previous generation transistors, the f_T may be degraded by the C_{BEoL} increase caused by the non-ideal routing metal scaling. In addition, the coupling between the gate metal and the adjacent fin's gate contacts becomes increasingly crucial as the fin pitch scales down, introducing additional parasitic capacitances for sub-10-nm node FinFETs [16]. The reduction in the gate contact metal's thickness also leads to an increase in gate resistance, degrading the quality factor and stabilization. Therefore, an intrinsic f_T enhancement in 3-nm node is not only desired to compensate for worsening parasitic components, but also to increase the power efficiency in high-speed operations. An improved g_{mext}-R_{out} trade-off is also preferred in the feedback systems.

As discussed before, g_{mext} is limited by the $R_{S/D}$, while R_{out} is sensitive to DIBL and electrostatic control. Since the 3D SDE doping profile engineering can effectively improve $R_{S/D}$ without degrading electrostatic control, it can be adopted for FinFET's analog performance enhancement. Fig. 3.11(a) shows the g_{mext}-I_{DS} curves as a function of LR in FinFETs with the optimized SDE profile for digital application. Increasing the LR from 0 to 2 nm can lead to a 220 Ω/fin reduction in R_{SDE} (from 450 to 230 Ω/fin), resulting in a 13% improved peak g_{mext} to 356 μS/fin. Further increasing the LR has relatively small impact on R_{SDE} and g_{mext} since the SDE region is relatively heavily doped. Compared to a vertically uniform SDE profile (without 3D engineering), the optimized SDE doping profile for digital application (LR=2 nm) can improve the

g_{mext} by 8%. An enhanced g_{mext}-R_{out} is also observed (Fig. 3.11(b)). A peak f_T of 540 GHz can be achieved.

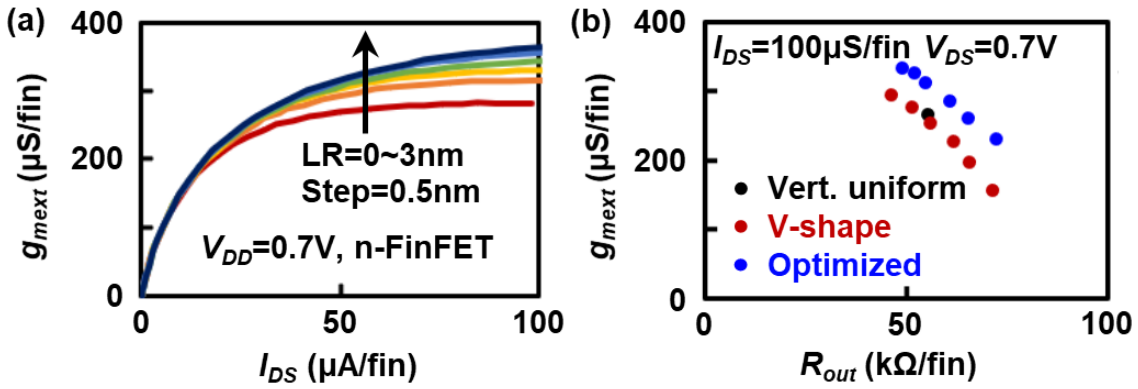

Fig. 3.11 g_{mext} enhancement through 3D SDE doping profile engineering. (a) g_{mext}-I_{DS} curve vs. LR, and (b) the resulting peak g_{mext} and R_{out} trade-off.

In addition to g_{mext} improvement, parasitic capacitance ($C_{parasitics}$) reduction can be achieved by spacer and SDE module co-optimization and further enhance f_T. Experimental results show that an LR up to 8 nm can be fabricated [17]. By increasing the LR from 2 nm to 8 nm and meanwhile increasing the L_{spacer} from 5 nm to 11nm, the C_{spacer} (C_{MoL}) can be reduced by 0.44×10^{-17} (0.55×10^{-17}) F/fin at the cost of ~90 Ω/Fin increase in R_{SDE}. Although the g_{mext} is reduced to 340 μS/Fin (by 4.5%), AC simulation suggests that the f_T can be further improved by ~5% to 570 GHz.

3.4 Summary

In this chapter, an optimization strategy of the 3D SDE doping profile is proposed for 3-nm node FinFETs. To improve the I_{ON}/I_{OFF} in future generation transistors, it is crucial to optimize the SDE module based on the physical parameters in the channel and gate modules.

TCAD simulations show that the optimized SDE doping profile can reduce R_{SDE} without degrading the electrostatic control. As a result, a 7% (10%) I_{ON}/I_{OFF} enhancement can be achieved in n-(p-)FinFETs while maintaining the variability suppression effect. 3D SDE engineering can also be adopted as an effective method for analog performance enhancement. The optimized 3D SDE profile for the digital application can improve the g_{mext}-R_{out} trade-off, which is favorable for analog applications. Enabled by the advanced S/D formation technologies, an SDE doping and spacer length co-optimization can be performed to reduce both the $R_{S/D}$ and $C_{parasitic}$ in 3-nm node n-FinFETs, resulting in a ~80 GHz (~16%) f_T improvement.

Chapter 4

Carrier Density Modulation in Multi-layered MoS_2

4.1 Introduction

TMDs such as MoS_2, WS_2, and WSe_2 have attracted much attention for future electrical device applications [61]-[69]. Due to its ultra-thin nature and CMOS BEoL compatible low temperature (<400 °C) synthesis, multi-layered MoS_2 can be used to realize active devices in the area not used as interconnect (Fig. 4.1). However, challenges need to be addressed before 2D MoS_2 can become production viable. One of the key requirements is a controllable doping process in MoS_2 for S/D formation in transistor fabrication. Density function theory calculations suggest that substitutional Nb in MoS_2 (native n-type) with mole fractions lower than a few percent is a p-type dopant and has little impact on band-structure [36,37]. Experimentally, MoS_2 with Nb demonstrates a p-type behavior [38-42]. MoS_2 with hole concentration as high as 10^{21} cm^{-3}, corresponding to >10% Nb mole fraction, has been synthesized [40]. However, a selective-area and precise Nb concentration's control technique has not been demonstrated. More importantly, for a >10% Nb concentration, the material would be considered to be a compound semiconductor, as in the case of bulk semiconductors like SiGe or III/V materials. Instead of only modulating the hole concentration, Nb with a high mole fraction can possibly affect other parameters such as mobility and bandgap. The impact of high dose Nb needs to be quantified.

In this chapter, a precise Nb mole fraction control technique in the 2D $Mo_{1-x}Nb_xS_2$ is demonstrated, and 2D films with various Nb concentration are synthesized and tested to identify the role of high concentration Nb. TLM structures and MOSFETs are fabricated on wafer-scale uniform $Mo_{1-x}Nb_xS_2$ samples for electrical characterization. The relation between hole

concentration and Nb mole fraction is extracted to precisely control the carrier concentration. In addition, Nb mole fraction's impact on the effective mobility (μ_{eff}, defined as the average mobility of carriers in the 2D films), contact resistivity (ρ_C), and the bandgap are analyzed to guide transistor design.

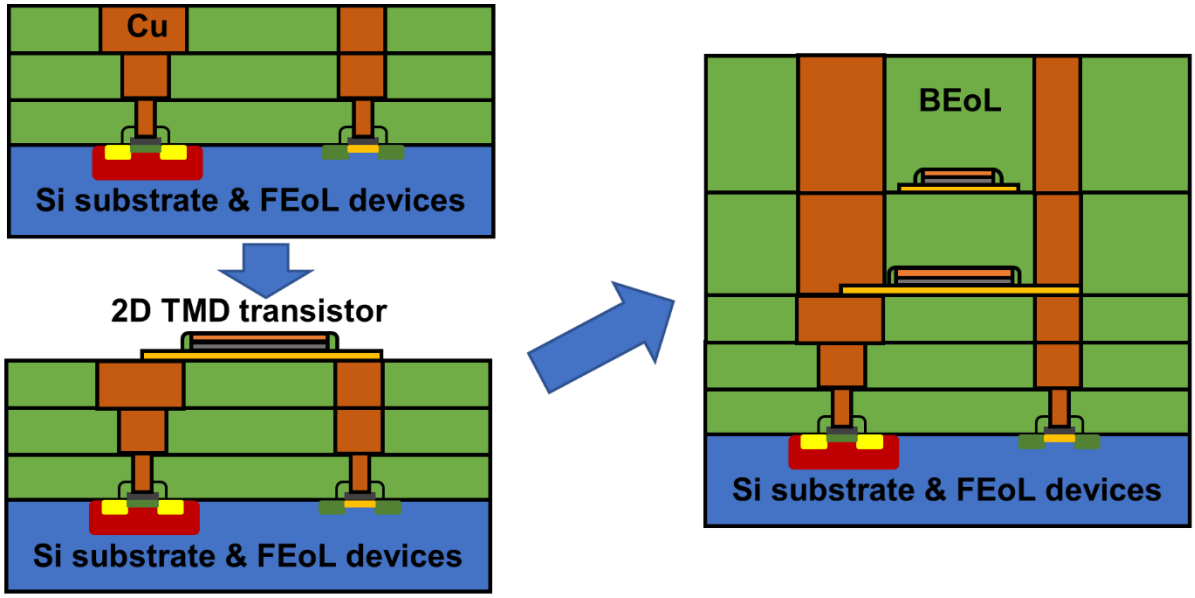

Fig. 4.1 Schematics of 2D TMD active device integration in the BEoL process.

4.2 Multi-layered $Mo_{1-x}Nb_xS_2$ synthesis and material characterization

Tremendous effort has been made to the synthesis of 2D MoS_2, including mechanical exfoliation [70], chemical liquid exfoliation [71], chemical vapor deposition (CVD) [72], etc. Among these methods, the sulfidation of the transition metal oxide is a common process to achieve high quality, wafer-scale uniform MoS_2 material. In this work, the multi-layered $Mo_{1-x}Nb_xS_2$ is synthesized by $Mo_{1-x}Nb_xO_y$ sulfidation in a closed CVD system (Fig. 4.2). Mo and Nb are deposited by co-sputtering on two-inch c-face sapphire wafers in Ar and O_2 ambient at

room temperature and a ~5nm thin layer of $Mo_{1-x}Nb_xO_y$ with high uniformity is achieved. The ratio between Mo and Nb can be tuned by the sputtering gun power as well as the shutter opening time. The sulfidation of $Mo_{1-x}Nb_xO_y$ is carried out in a closed system furnace with H_2S (10% mixed with Ar) reactive gas under a partial pressure of 200 Torr with a temperature profile ramped up by +20˚C/min to 650˚C for 30min then raised to 750˚C for 60min. After the sulfurization process, the samples were cooled down to room temperature. Seven samples with various Nb mole factions are synthesized to quantify the impact of high concentration Nb, and the synthesis parameters are summarized in table 4.1. It is worthwhile noting that the Nb mole fraction in the $Mo_{1-x}Nb_xO_y$ and the $Mo_{1-x}Nb_xS_2$ are different. Since MoO_x sublimates in the >650 ºC heat treatment, while NbO_x does not sublimate, the Nb mole fraction in $Mo_{1-x}Nb_xS_2$ is higher than that in $Mo_{1-x}Nb_xO_y$. In addition, the Nb sputtering deposition rate is not constant in the process, and the Nb dose is not linearly related to the Nb deposition time.

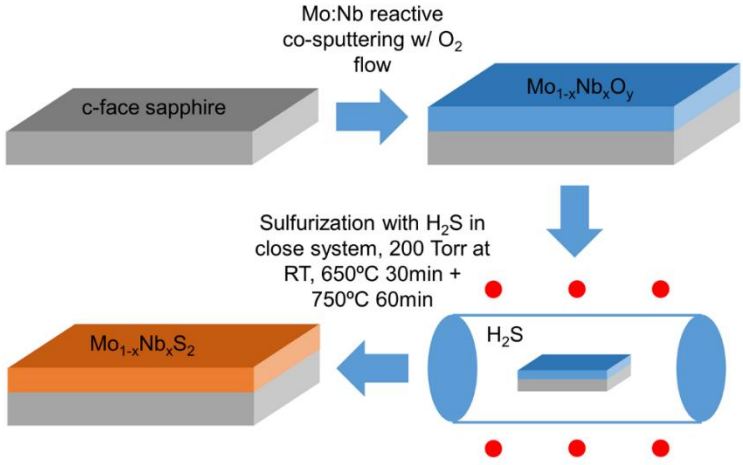

Fig.4.2 Schematics of the two-step CVD technique for wafer scale multi-layered $Mo_{1-x}Nb_xS_2$ synthesis.

Table 4.1 Synthesis condition and the resulting Nb mole fraction of $Mo_{1-x}Nb_xS_2$ samples

Sample	A	B	C	D	E	F	G
Mo DC sputtering condition	300 W for 30 sec						
Nb AC sputtering power (W)	20	30	30	20	30	40	50
Nb AC sputtering time (sec)	15	10	30	300	300	300	300
Gas flow in sputtering	15 sccm Ar + 15 sccm O_2 for 300 sec						
Sulfidation condition	Closed system, 200 torr 10% H_2S, 650°C for 30min + 750°C for 60min						
Nb mole fraction by SIMS	3.5%	5.5%	7.0%	7.5%	8.0%	10.0%	11.0%

Transmission electron microscopy (TEM) shows that the samples have 10~12 well order layers (Fig. 4.3). Nb mole fractions of the samples are extracted by SIMS measurements. The uncertainty of the SIMS measurement is <0.5%. The SIMS result of $Mo_{0.92}Nb_{0.08}S_2$ (sample E) is shown in Fig. 4.4 as an example. Mo and Nb doses are estimated with *Dose = Atomic count / Yield of SIMS*. Atomic counts of Mo and Nb are calculated by integrating atomic counts from 20 sec to the 2D/Sapphire interface. $Yield_{Mo} / Yield_{Nb}$ is calibrated to be 1.05. The first 20 sec (corresponding to the top ~2 nm of the films) in the SIMS reading is ignored due to surface memory effect. The Mo:Nb count ratio varies by <15% from 20 sec to the 2D/sapphire interface, suggesting Nb atoms are relatively uniformly distributed in the film. This uniform distribution of Nb is verified by X-ray photoelectron spectroscopy **(**XPS) and scanning tunneling microscope (STM). No Nb-O bond is detected in XPS measurements, suggesting no presence of NbO_x. STM shows a bandgap of ~0.68 eV (Fig. 4.5), implying there is no clustered Nb or clustered NbS_2 semi-metal. In addition, no interstitial defects are observed under TEM. Consequently, most of the Nb atoms are incorporated in the $Mo_{1-x}Nb_xS_2$ lattice and distribute uniformly in the 2D film. This phenomenon is observed in all the tested samples.

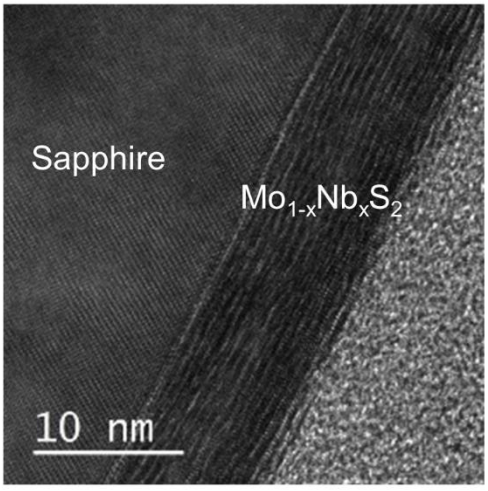

Fig. 4.3 TEM image of the multi-layered $Mo_{0.92}Nb_{0.08}S_2$. All samples are observed to have 10~12 layers.

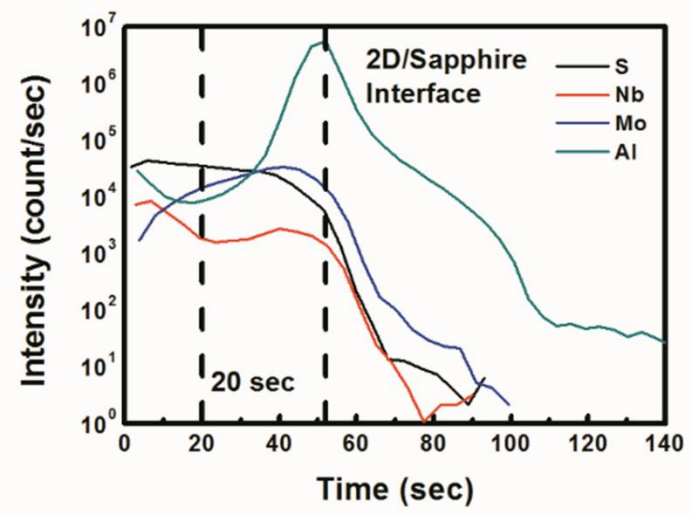

Fig. 4.4 SIMS measurement for Nb mole fraction extraction. Data of $Mo_{0.92}Nb_{0.08}S_2$ is shown as an example.

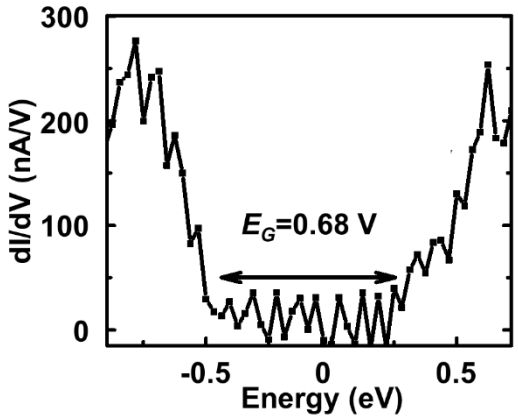

Fig. 4.5 STM result of $Mo_{0.92}Nb_{0.08}S_2$. A 0.68 eV bandgap is observed.

The selective-area capability of the $Mo_{1-x}Nb_xS_2$ CVD process is also investigated. Fig. 4.6 shows a preliminary result. By patterning the $Mo_{1-x}Nb_xO_y$ by lithography followed by sulfidation, a selective-area synthesis can be achieved. With this method, the $Mo_{1-x}Nb_xS_2$ can be patterned as S/D regions with high hole concentration in an enhancement mode MoS_2 channel p-MOSFET. Since the MoS_2 is formed by a sublimation-redeposition process, the film's thickness is sensitive to the pattern's shape of the $Mo_{1-x}Nb_xO_y$, and 2D film is observed outside of the patterned area (because of the gas phase reaction and redeposition of the $Mo_{1-x}Nb_xS_2$). Therefore, an etching process is required to remove the $Mo_{1-x}Nb_xS_2$ out of S/D areas in enhancement mode MOSFET's.

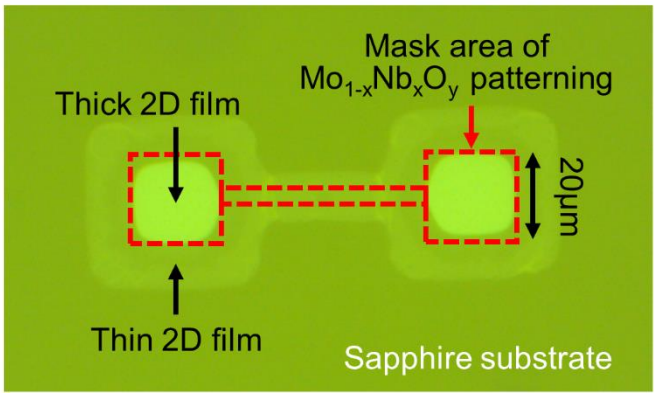

Fig. 4.6 Selective area synthesis of $Mo_{1-x}Nb_xS_2$ by pattering $Mo_{1-x}Nb_xO_y$ before sulfidation.

4.3 Device fabrication and electrical characterization

TLM structures and MOSFETs are fabricated on the wafer-scale uniform 2D films to quantify the impact of Nb mole fraction on electrical characteristics. Table 4.2 shows the fabrication process flow. Since $Mo_{1-x}Nb_xS_2$ films are p-type, 40 nm of palladium (Pd), which has a large work function (~5.12 eV), is used as contact metal to achieve low contact resistivity. Al_2O_3 is deposited by ALD as the gate dielectric with a relatively large EOT of 12 nm. For every Al_2O_3 deposition, a bare Si wafer, processed by a buffered oxide etch (BOE) for native oxide removal, is placed in the ALD chamber to monitor the quality of the dielectric. The MOSCAP measurements confirm the 12 nm EOT. Fig. 4.7 and Fig. 4.8 show the schematics of the $Mo_{1-x}Nb_xS_2$ TLM structures and MOSFET, respectively.

Table 4.2 TLM and MOSFET fabrication process flow

Step	Process	Condition and comments
0	$Mo_{1-x}Nb_xS_2$ on sapphire	
1	Active area mask	Lithography with PR AZ5214-E
2	Active area patterning	CF_4 plasma etching 30 sec at 100W
3	Mask removal	PR strip with acetone
4	S/D and TLM contact area mask	Image reverse lithography with PR AZ5214-E
5	S/D and TLM contact metal deposition	40 nm Pd and 80 nm Au e-beam evaporation
6	Metal contact formation using lift-off	PR strip with acetone
7	TLM measurement	
8	Gate dielectric deposition	Al_2O_3 by thermal ALD at 200 ºC, 200 cycles
9	Gate contact mask	Image reverse lithography with PR AZ5214-E
10	Gate metal deposition	80 nm Al e-beam deposition

11	Gate contact formation using lift-off	PR strip with acetone
12	S/D opening mask	Image reverse lithography with PR AZ5214-E
13	Oxide removal	Buffered Oxide Etcher 15-30 sec
14	Mask removal	PR strip with acetone
15	MOSFET measurement	

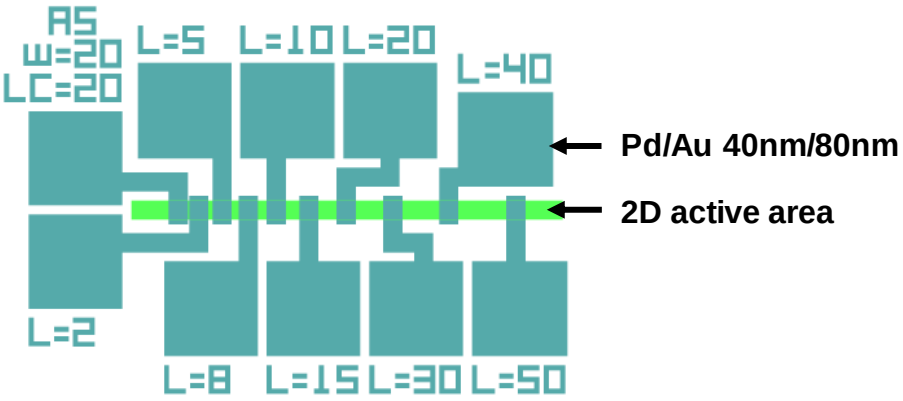

Fig. 4.7 Layout of the TLM structure.

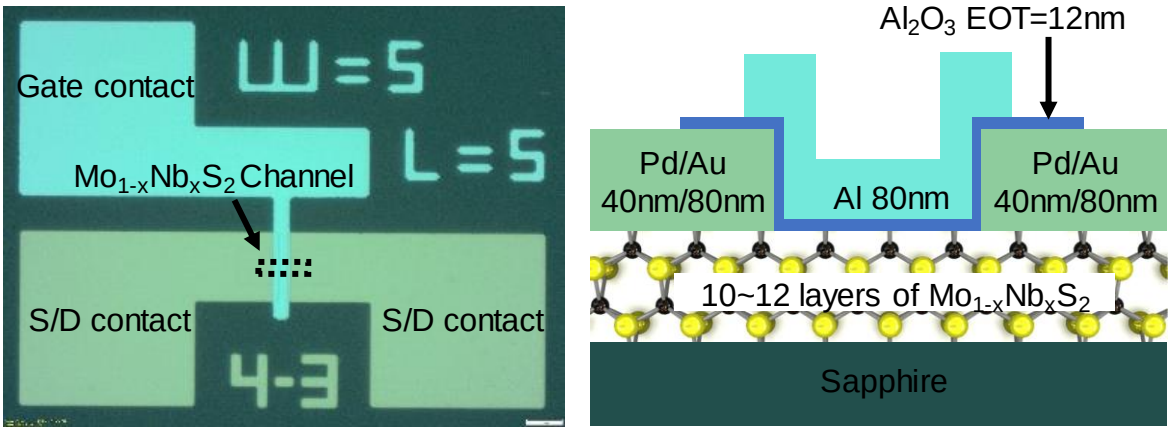

Fig. 4.8 Layout and channel cross-section schematics (not to scale) of $Mo_{1-x}Nb_xS_2$ MOSFETs.

4.3.1 TLM results and analysis

TLM results (Fig. 4.9) are used to extract sheet resistivity (ρ_s) and R_C in each sample. For each sample, multiple TLMs are measured, and the variation between devices is found to be <5%. This confirms the high uniformity of the 2D films. The average values of electrical properties are used in the analysis. Transmission line model (Fig. 4.10) is used to calculate the contact resistivity (ρ_c). The resistance of the contact metal is assumed to be much smaller than ρ_s and ρ_c and is ignored in the extractions. The total contact resistance (under the width of W) can be derived [73] as

$$R_C \times W = \sqrt{\rho_c \rho_s}\coth\left(L_{con}\sqrt{\frac{\rho_s}{\rho_c}}\right)$$

where L_{con} is the contact length. Furthermore, the transfer length (L_T) can be defined as $L_T=(\rho_c/\rho_s)^{0.5}$. With the long overlapping region of the 2D layers and metal contact (20 μm), $L_{con} >> L_T$ can be assumed. The contact resistance can be approximated as

$$R_C \times W = \frac{\rho_c}{L_T}$$

The ρ_s and ρ_c extracted from the tested samples are summarized in Fig. 4.11 and will be used in the p and μ extraction process from MOSFETs' data.

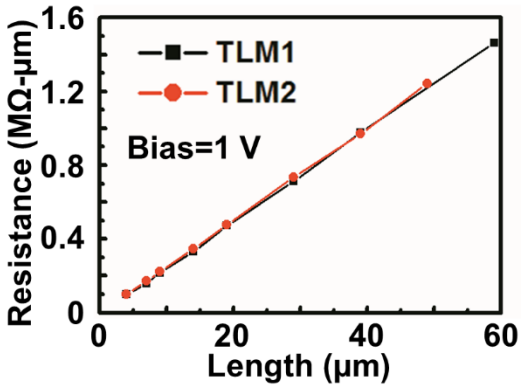

Fig. 4.9 TLM results of $Mo_{0.92}Nb_{0.08}S_2$.

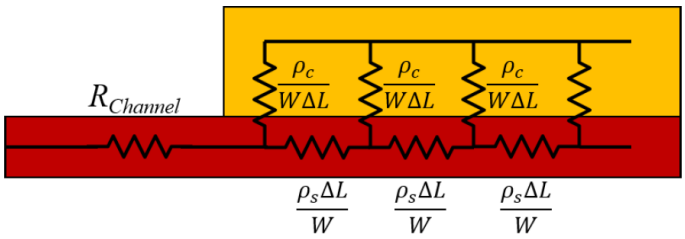

Fig. 4.10 Transmission line model for contact resistivity extraction.

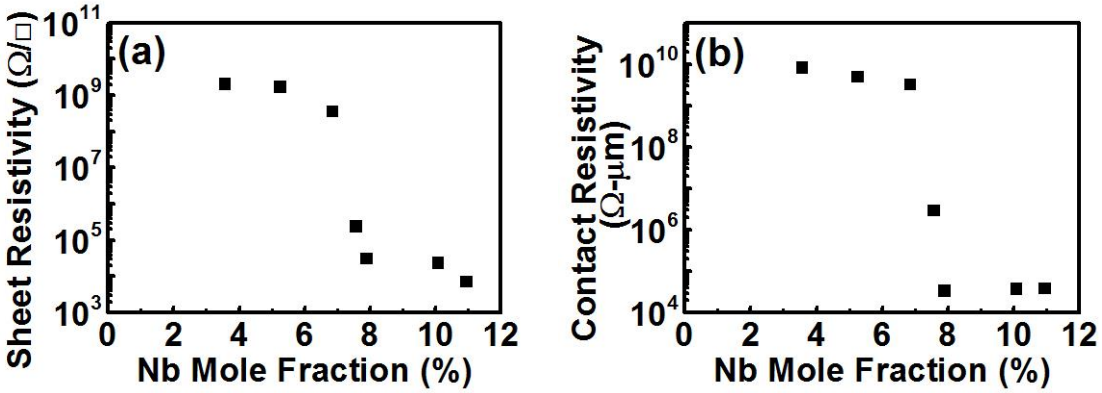

Fig. 4. 11 (a) ρ_s and (b) ρ_c as a function of Nb mole fraction extracted by TLM results.

4.3.2 MOSFET results and analysis

To further understand the Nb concentration's impact on electrical parameters, effective carrier concentration (p) and μ_{eff} are extracted from transfer characteristics in $Mo_{1-x}Nb_xS_2$ MOSFET with various Nb mole fractions. In this study, p is defined as the average sheet carrier concentration of 10~12 layers of 2D TMD with V_{GS}=0 V. Fig. 4.12(a) shows the transfer characteristics of MOSFET with $Mo_{0.92}Nb_{0.08}S_2$ channel as an example. An average extrinsic transconductance (g_{mext}) of -3.27x10^{-2} mS/mm is measured at V_{DS} =1 V. The negative g_{mext} displays a p-type behavior, which is shared by all tested samples. The $Mo_{1-x}Nb_xS_2$ transistors are modeled

as long channel MOSFETs with the parasitic resistances and gate interface traps. The μ_{eff} can be extracted using

$$\mu_{eff} = g_{mint} / \left(\frac{W}{L_G} \times C_G \times V_{DS} \times \frac{R_{CH}}{R_{CH} + 2 \times R_{S/D}} \times \frac{\Delta Q_{mobile}}{\Delta Q_{total}} \right)$$

where g_{mint} is the intrinsic transconductance, C_G is the gate capacitance, R_{CH} is the channel resistance, and ΔQ_{mobile} and ΔQ_{total} are the mobile and total charge density modulated by the gate respectively. g_{mint} can be calculated as

$$g_{mint} = g_{mext} / \left(1 - g_{mext} \times R_{S/D}\right)$$

and C_G can be extracted as

$$C_G = \left({C_{OX}}^{-1} + \left(C_{IT} + C_Q \right)^{-1} \right)^{-1}$$

where C_{OX}, C_{IT} and C_Q are the dielectric capacitance, interface trap capacitance and quantum capacitance respectively.

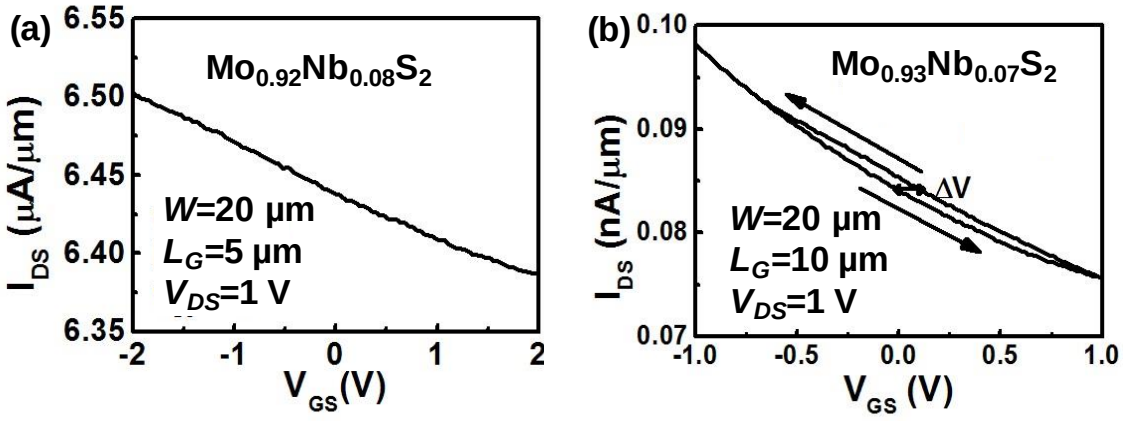

Fig. 4.12 Transfer characteristics of (a) $Mo_{0.92}Nb_{0.08}S_2$, and (b) $Mo_{0.93}Nb_{0.07}S_2$ MOSFETs.

In the extraction, $V_{DS} \times R_{CH}/(R_{CH} + 2 \times R_{S/D})$ represents the impact of parasitic resistance on voltage drop in the channel region. Based on the model and assumptions, $\Delta Q_{total} = \Delta Q_{mobile} + \Delta Q_{IT}$, where ΔQ_{IT} is the interface trap density. The $\Delta Q_{mobile}/\Delta Q_{total}$ term in the μ_{eff} extraction counts for the impact of dielectric interface traps. ΔQ_{IT} can be estimated by the hysteresis in I_{DS}-V_{GS} curves. The FET transfer characteristic with the largest hysteresis is shown in Fig. 4.12(b). ΔQ_{IT} is found to be non-uniform across all devices, and the highest ΔQ_{IT} is measured to be <7% of ΔQ_{total}. Consequently, it is reasonable to assume $\Delta Q_{mobile}/\Delta Q_{total} = 1$. Therefore, $C_Q + C_{IT} \approx C_Q$. C_Q of the $Mo_{1-x}Nb_xS_2$ is assumed to be similar to that in multi-layered MoS_2 [74,75], and $C_Q \sim 10^{-5}$ F/cm^2 (equivalent to 0.35 nm EOT). With the relatively thick gate dielectric (EOT=12 nm) used, C_{OX} is much smaller than C_Q, and therefore $C_G \approx C_{OX}$. All transistors tested have negligible gate leakage currents (I_G) below 2 pA/μm within the applied gate bias range. With $\Delta Q_{mobile}/\Delta Q_{total}$ under-estimated, the μ_{eff} is slightly under-estimated (<8%). p is calculated using $p = L/\left(q \times R_{CH} \times \mu_{eff} \times W\right)$ at V_G =0 V. Since μ_{eff} is slightly under-estimated, p is slightly over-estimated. Fig. 4.13 shows the impact of Nb mole fraction on μ_{eff} and p.

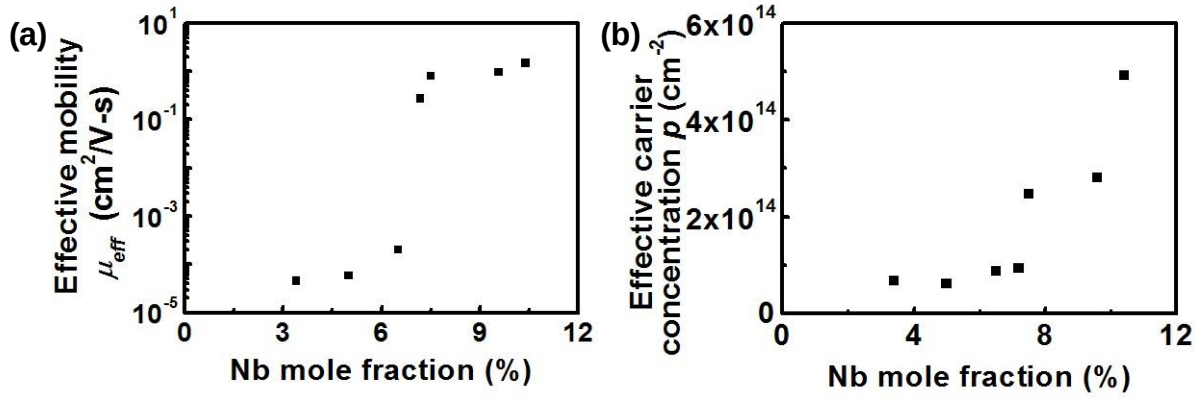

Fig. 4.13 Impact of Nb mole fraction on (a) effective mobility and (b) effective carrier concentration.

4.4 Role of high concentration Nb in $Mo_{1-x}Nb_xS_2$

Theoretical analysis suggests that substitutional low mole fraction Nb acts as a p-type dopant in MoS_2 [28]-[29]. However, the highly non-linear relation between *p* and Nb mole fraction observed in this work strongly suggests otherwise. One hypothesis of this non-linear relation is that the change in *p* is caused by the difference in density of sulfur vacancies instead of the Nb dose. Although sulfur vacancies can act as donors in MoS_2 [76], SIMS results suggest that its density is much smaller than the *p* in all samples. Therefore, the influence of sulfur vacancy is negligible. The Nb's role can be verified by comparing Nb density and *p* (Fig. 4.14) in the tested samples. The Nb density is estimated by assuming $Mo_{1-x}Nb_xS_2$ has a similar lattice constant as compared to MoS_2 (10^{15} cm^{-2} Mo/Nb atoms per layer). Fig. 4.14 shows that *p* is less than 50% of Nb density for all samples. If the Nb atoms act as substitutional impurities (~100% activation rate according to material characterization), the ionization rate is less than 50% at room temperature for all the tested samples and is significantly smaller than the ~100% ionization rate for conventional dopants.

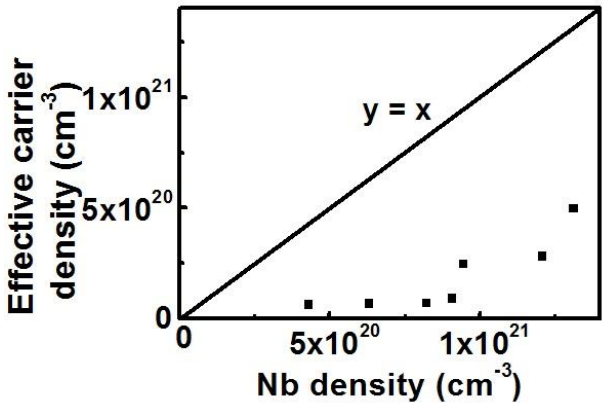

Fig. 4.14 Comparison between effective carrier densities and Nb densities in all tested samples

The high concentration Nb's impact on μ_{eff} and bandgap also indicate that Nb does not act as an active dopant. A non-linear relation between μ_{eff} and Nb mole fraction is also observed (Fig. 4.13(s)). μ_{eff} improves dramatically (by >4000×) when Nb mole fraction increases from 7% to 8%, while μ_{eff} stays within an order of magnitude for Nb mole fraction from 3.5% to 7% and from 8% to 11%. This non-linear μ_{eff} variation is not caused by the difference in films' grain size, which can be a limiting factor in 2D's mobility. TEM shows an average distance between lattice disorders of ~50 nm for all samples, so the impact of grain size on μ_{eff} is not significant. Therefore, the change in μ_{eff} is believed to be caused by the difference in Nb mole fraction. If Nb acts only as an active dopant, μ_{eff} has been suggested to be limited by impurity scattering [40], and mobility decreases with increasing Nb density. However, the increase in μ_{eff} observed in this work contrasts with the trend of mobility degradation. More importantly, a bandgap of ~0.68eV is observed by STM in $Mo_{0.92}Nb_{0.08}S_2$, which is much smaller than the ~1.3eV bandgap of multi-layered MoS_2 [28]. Nb with >3.5% mole fraction not only modulates carrier density but also reduces the bandgap of the 2D TMD. In conclusion, $Mo_{1-x}Nb_xS_2$ with >3.5% Nb concentration can be viewed as a compound 2D TMD semiconductor.

4.5 Summary

In this study, a precise Nb mole fraction control technique in the 2D $Mo_{1-x}Nb_xS_2$ is demonstrated, and the impact of the high mole fraction (>3.5%) Nb in MoS_2 is quantified. Multi-layered $Mo_{1-x}Nb_xS_2$ are synthesized by a Mo/Nb co-sputtering process followed by a closed-system sulfidation. The Nb mole fraction can be well controlled by modulating the Nb sputtering condition, resulting in carrier concentration from 8×10^{13} to 5×10^{14} cm^{-2} (9×10^{19} to 5×10^{20} cm^{-3}) in the 2D film. Electrical characterizations show that a high carrier density (>2×10^{20}

cm^{-3}) can be achieved by introducing a substitutional Nb of >8%, suitable for S/D formation in MoS_2 MOSFETs. The Nb mole fraction from 3.5% to 11% demonstrates highly non-linear impact on the carrier density, mobility, and contact resistance, suggesting that Nb does not act as an active dopant, as reported in previous publications. Instead, $Mo_{1-x}Nb_xS_2$ can be viewed as a compound 2D TMD semiconductor. The extracted relation between the Nb mole fraction and the carrier density can guide precise carrier density control. Increasing the Nb mole fraction from 3.5% to 11% also results in $>10^4\times$ mobility improvement and contact resistivity reduction, both are favorable for achieving S/D regions with low access resistances.

Chapter 5

Conclusions

5.1 Summary

5.1.1 3D SDE doping profile engineering in 3-nm node FinFETs

Advanced S/D formation technologies have been developed to precisely control the 3D doping profile in the SDE region, enabling new dimensions of freedom for design optimizations. In this work, 3D SDE doping profile engineering is demonstrated as an effective method to suppress process-induced variability in FinFETs, which is extensively crucial for the future 3-nm node. In FinFETs with realistic tapered fin, the sub-threshold current is localized, while the I_{ON} distributes almost uniformly in the fin. I_{ON} and I_{OFF}'s sensitivity to different geometry parameters are systematically analyzed using TCAD simulations, and the governing physics are investigated. The localized leakage path indicates that the variabilities can be suppressed by enhancing the local electrostatic control, which can be achieved through 3D SDE doping profile engineering. By using a V-shape SDE doping profile, which is previously developed for I_{ON}/I_{OFF} enhancement in 7/10-nm node FinFETs, the leakage path can be shifted towards the fin top. The electrostatic control enhancement caused by T_{Si} reduction and top gate modulation suppresses the device performances' sensitivities to the physical parameter variations.

A 3D SDE doping profile's optimization strategy is also proposed for the 3-nm node FinFETs. In the SDE doping profile engineering, the trade-off between electrostatic control and the on-state R_{SDE} has been identified as the key for the I_{ON}/I_{OFF} enhancement. The relation between the SDE doping and the R_{SDE} is systematically analyzed to guide the design optimization. To maximize the I_{ON}/I_{OFF}, it is crucial to optimize the SDE doping profile based on the physical

parameters in the channel and gate module. Compared to the experimental V-shape profile, the optimized SDE doping profile can reduce R_{SDE} without degrading the electrostatic control, resulting in a 7% (10%) I_{ON}/I_{OFF} enhancement in n- (p-)FinFETs while maintaining the variability suppression effect. The 3D SDE doping profile optimization can be also be utilized as an effective method for analog performance enhancement. The optimized 3D SDE profile for the digital application can be used to improve the g_{mext}-R_{out} trade-off, which is favorable for analog applications. Enabled by the advanced S/D formation technologies, an SDE doping and spacer length co-optimization can be performed to reduce both the $R_{S/D}$ and $C_{parasitic}$ in 3-nm node n-FinFETs, resulting in a ~80 GHz f_T improvement.

5.1.2 Carrier density modulation in multi-layered MoS_2

In this study, a precise Nb mole fraction control technique in the 2D $Mo_{1-x}Nb_xS_2$ is developed to module the carrier density in the 2D film. $Mo_{1-x}Nb_xS_2$ films with various Nb concentration are synthesized and tested to identify the role of high concentration (>3.5%) Nb. The Nb mole fraction from 3.5% to 11% demonstrates highly non-linear impact on carrier density, mobility, and contact resistance. This strongly suggests that Nb does not act as an active dopant, as reported in previous publications. Instead, $Mo_{1-x}Nb_xS_2$ can be viewed as a compound 2D TMD semiconductor. The extracted relation between Nb mole fraction and carrier density provides guidance for precise carrier density control. Increasing the Nb mole fraction from 3.5% to 11% also results in $>10^4\times$ mobility improvement and contact resistivity reduction, both are favorable for achieving S/D regions with low access resistances.

5.2 Suggestions for Future Research

The followings are some possible directions for further investigations:

- Quantification and suppression of 3-nm node FinFET's analog performance variation: 3-nm node FinFET demonstrates improved analog performances compared to previous generation transistors. However, process-induced and statistical analog performance variation needs to be systematically analyzed. This study shows that both g_{mext} and R_{out} are sensitive to the dopant encroachment in the SDE module. g_{mext}, f_T, and f_{max} are known to be sensitive to the gate overdrive, which has a strong dependency on the fin's geometry and the gate stack. In addition, variations in linearity and noise need to be analyzed. A device-circuit co-optimization is proposed to investigate the trade-off between different parameters and guide FinFET's design optimization for analog applications.
- Process induced variability in nanosheet FET (NSFET) and nanowire FET (NWFET): For future generation transistors with a sub-10-nm physical channel length, new technologies such as NSFET and NWFET have been proposed. With further scaled device dimensions, these transistors are predicted to be extensively sensitive to process-induced geometry variations. The reduced physical channel length also enhances the coupling between the virtual cathode to the drain fringing field, increasing the device performances' sensitivity to the SDE doping profile. Since the 3D SDE doping profile needs to be co-optimized with the channel's geometry, the strategy of SDE optimization need to be re-analyzed. More importantly, new variation sources, such as the spacing between nanosheet and the gate stack's non-uniformity, need to be investigated to guide design and process optimization.
- Low-temperature synthesis of high-quality 2D MoS_2: In order to build 2D TMD based BEoL active devices, one of the main challenges is to synthesize 2D material with high

mobility at a low-temperature compatible to CMOS BEoL process (< 400°C). CVD related synthesis processes, being able to form wafer-scale uniform 2D films, are most suitable for VLSI fabrication. However, a relatively high temperature is required to achieve full conversion of metal or metal oxide precursors. Even in H_2-assisted [77] and Te-assisted CVD [78], the reaction temperature is still not compatible with the BEoL process (> 500°C for MoS_2). Large area multi-layered MoS_2 growth can be achieved at 400°C by magnetron sputtering MoS_2 target [79] and MOCVD [80]. However, a post-deposition annealing process is required to enhance the 2D TMD's crystallinity, making it unsuitable for electronic applications. A 2-step CVD with remote plasma-enhanced sulfurization can possibly solve the drawbacks mentioned above in existing 2D TMD synthesis processes. Low temperature (< 300°C) sulfidation has been demonstrated by a direct plasma PECVD [81]. In order to avoid the plasma charging effect to the low-k material in CMOS BEoL, a remote plasma enhanced sulfidation process needs to be investigated to achieve < 400°C reaction temperature.

- Contact resistance reduction of multi-layered $Mo_{1-x}Nb_xS_2$: In this work, a relatively low contact resistivity of 10^{-3} Ω-cm is demonstrated on multi-layered $Mo_{0.89}Nb_{0.11}S_2$. However, the contact resistance is measured to be 3×10^4 Ω/μm and needs to be reduced by a factor of >100 to meet the requirement of BEoL electronics. The large contact resistance is partially caused by the low mobility (~1.5 $cm^2/V\cdot sec$) and the resulting high sheet resistivity. For BEoL active devices, the contact's dimension is assumed to be in the 0.1 μm level (dimension of metal routing), and the contact resistance can be approximated by $R_C \times W = \sqrt{\rho_c \rho_s}$. By improving the 2D film's crystallinity combined with substrate/encapsulation engineering, a μ≈100 $cm^2/V\cdot sec$ (approximately the value in mechanically exfoliated MoS_2) is expected, resulting in a ~10×reduction in contact resistance. Advanced stack contact, such as metal/semiconductor and

metal/semiconductor/nm-insulator stacks, and low-temperature post-deposition annealing need to be investigated to further reduce the contact resistivity.

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