Title

Dynamic Level Changing for Full Range ZVS in Flying Capacitor Multi-Level Converters

Authors

Blackwell, Margaret E
Stillwell, Andrew
Pilawa-Podgurski, Robert CN

Publication Date

2022

DOI

10.1109/ojpel.2022.3200371

IEEE Open Journal of Power Electronics, Volume 3, August 2022

Dynamic Level Changing for Full Range ZVS in Flying Capacitor Multi-Level Converters

M. E. Blackwell
A. Stillwell
R. C. N. Pilawa-Podgurski

Dynamic Level Changing for Full Range ZVS in Flying Capacitor Multi-Level Converters

Margaret E. Blackwell, *Student Member, IEEE*, Andrew Stillwell, *Member, IEEE*,
and Robert C. N. Pilawa-Podgurski, *Member, IEEE*

***Abstract*—This paper presents a control technique for flying capacitor multi-level (FCML) converters to achieve zero-voltage switching (ZVS) across the full range of duty cycles, with application in high power density and high efficiency power converters. Previous works have used variable frequency control to enable ZVS at specific duty cycles in FCML converters, but have not been able to use these methods to enable ZVS across the full range. This work uses dynamic level selection and variable frequency control to increase inductor current ripple at duty cycle ranges for which ZVS was previously unattainable. An experimental 5-level FCML prototype has been built using GaN devices on a single-sided PCB to demonstrate this control technique. We demonstrate 4-level and 5-level operation with ZVS at duty cycles that are not possible with 5-level operation alone, as well as a dynamic level transition with active capacitor voltage balancing.**

I. Introduction

Flying capacitor multi-level (FCML) converters utilize one or more flying capacitors as energy storage elements to reduce the switch voltage stress of each transistor and to reduce the volt-second on the inductor [1]–[6]. These benefits allow the use of lower voltage rated switches, which permits higher switching frequencies as a result of lower switching losses. The increase in switching frequency, in conjunction with the reduction in inductor volt-second, due to inherent qualities of the FCML topology, leads to a reduction in the volume of the inductor and the total volume of the converter [7]. However, with this decrease in volume comes a necessity to increase efficiency because the surface area for heat transfer is reduced. Further reduction in volume can be achieved through higher frequency switching at the cost of higher switching losses. To mitigate these switching losses, zero-voltage switching (ZVS) can be employed at selected duty cycles as shown in [8], [9] through variable frequency control. However, both works noted the challenges of obtaining ZVS at specific duty cycles inherent to FCML operation. For DC/AC or AC/DC converter applications, or for applications with wide input voltage ranges, the duty cycle of the switches must vary across a wide range. However, due to the nature of FCML operation detailed in this paper, maintaining ZVS across the full range is a challenge. In [10], the current ripple is *minimized* by dynamically varying the number of levels of the FCML, which is suitable for hard-switched operation. Here, we propose to dynamically vary the number of levels to *increase* the inductor current ripple and, in conjunction with variable frequency control, maintain the necessary conditions for ZVS across the full duty cycle range.

Shortened portions of this manuscript were presented at the 2018 IEEE Workshop on Control and Modeling for Power Electronics (COMPEL), Padova, Italy.

We derive the underlying mechanisms in FCML converters which make ZVS a challenge at specific duty cycle ranges, and show how dynamic level selection overcomes this challenge. Additionally, we detail the considerations of capacitor voltages necessary to decide the number of converter levels and switch implementation. Our control strategy is validated in hardware through a 5-level experimental prototype, which demonstrates ZVS at duty cycles previously unattainable. Level transitioning is demonstrated with active balancing through the use of duty cycle adjustment. This paper presents a method of ensuring ZVS operation across a full range of conversion ratios for an FCML converter and demonstrates this method in a compact and flat hardware prototype.

This work extends our previous conference publication [11], with key additions, including the consideration of resonant operation in determining frequency limits, a method for determining the parameters for active balancing during a level transition, and additional experimental results. The remainder of this manuscript is organized as follows: Section II reviews the basics of FCML operation; Section III derives the fundamental characteristics of FCML converters that prevent ZVS operation at specific duty cycles and proposes dynamic level selection to overcome these challenges; Section IV describes the active balancing method for level transitions and presents a method to determine parameters for active balancing for shortest settling time; Section V demonstrates the method of dynamic level selection for a wide duty cycle range in hardware; and Section VI summarizes the contribution of the paper.

II. Flying Capacitor Multi-level Converter

Fig. 1 shows a schematic drawing of the 5-level FCML converter used in this work with flying capacitors labeled C_1, C_2, and C_3. Phase-shifted PWM (PS-PWM) [1], [5] is typically used for FCML converters of N levels with each switch pair (labeled S_{iA} and S_{iB}) operated complementary to each other at duty cycle, D, and phase shifted by $360°/(N-1)$. The voltage conversion ratio of the buck FCML is equivalent to that of the traditional two-level buck converter, given by (1). One advantage of the FCML converter with PS-PWM control

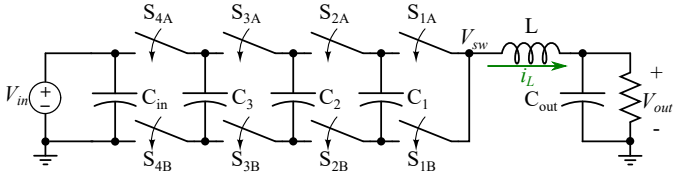


Fig. 1: 5-Level FCML Converter Schematic.

is the reduced switch voltage stress, $V_{in}/(N-1)$, because the flying capacitors, C_k, are held at a steady-state voltage, (2).

$$V_{out} = D \cdot V_{in} \tag{1}$$

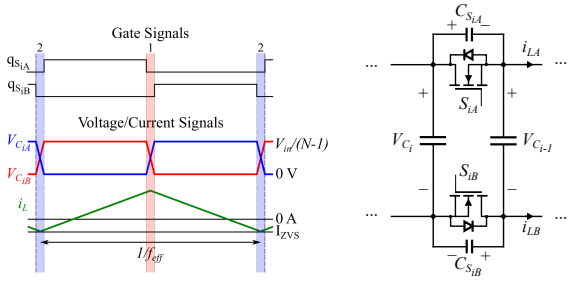
$$V_{C_k} = \frac{k \cdot V_{in}}{(N-1)}, k = 1, 2...(N-2) \tag{2}$$

Additionally, the FCML topology has an inherent frequency multiplication at the switch node, V_{sw} in Fig. 1, that allows for a reduction in inductance. For a given switching frequency, f_{sw}, the effective switching frequency, f_{eff}, seen at the inductor is $(N-1) \cdot f_{sw}$ and the voltage across the inductor swings by $V_{in}/(N-1)$. Both the frequency multiplication and voltage reduction lead to a required inductance decrease by $(N-1)^2$.

III. Zero-Voltage Switching

In addition to the frequency multiplication property and inductance reduction inherent to the FCML topology, the switching frequency can be increased to further improve power density. However, the switching losses also increase with frequency. One method to reduce these switching losses is to operate with sufficient inductor ripple such that the momentarily negative inductor current can be used to discharge the parasitic capacitance of the power transistor, enabling ZVS operation [12]. Only the basics of ZVS for FCMLs are described here and a more detailed explanation is available in [8]. In buck-mode operation, because the inductor current is naturally positive during the deadtime of Region 1 in Fig. 2a, ZVS is easily attainable for the low-side switches. The small parasitic capacitance of the low-side transistor, $C_{S_{iB}}$ in Fig. 2b, can discharge quickly from $V_{C_{SiB}} = V_{in}/(N-1)$ to 0 V with this positive current, i_L, thus enabling a zero-voltage at the time of switching. Conversely, ZVS for the high-side switches is more difficult because a negative current during the deadtime of Region 2 is required to discharge the parasitic capacitance, $C_{S_{iA}}$ to 0 V before switching.

Previous works, [12] and [13], have shown that a sufficiently large inductor current ripple is required to provide a negative current, i_L, during a specified deadtime which discharges the transistor parasitic capacitance and allows ZVS operation. However, due to the multi-level operation of the FCML, certain



(a) Converter waveforms for ZVS conditions.

(b) Arbitrary switch pair with parasitic capacitances.

Fig. 2: Inductor current must have enough ripple to reach a peak negative value, I_{ZVS} which can discharge the parasitic capacitance $C_{S_{iA}}$ of an arbitrary switch pair and allow for ZVS.

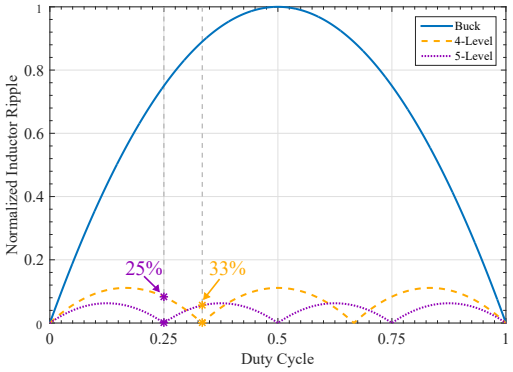


Fig. 3: Higher-level FCML converters inherently exhibit lower inductor current than two-level buck converters, but introduce inductor ripple valleys at certain duty cycles.

duty cycles inherently exhibit low or no current ripple, inhibiting the ability to achieve ZVS without going to extremely low switching frequencies. In this work, a constant negative inductor current peak, I_{ZVS}, is chosen along with a constant deadtime. The process for determining these parameters is detailed in [14], [15]. One potential shortcoming of this ZVS technique is the increase in peak-to-peak inductor current, which is needed to maintain the negative current required for ZVS. Due to this increased ripple, inductor core losses increase and may offset any benefit seen from reducing the switching losses. Furthermore, there is a limit at which the load current is no longer sufficient to allow for ZVS, Eqn. 3. When the required negative inductor current for ZVS is larger (i.e. more negative) than the average current minus half of the peak-to-peak current ripple, the technique detailed here of discharging the switch output capacitance cannot be used to achieve ZVS. At very light-load, another method, such as, burst-mode operation [16], discontinuous conduction mode operation [17], [18], or frequency/duty modulation [19]–[21], is recommended to avoid increasing non-switching losses during ZVS.

$$I_{ZVS} < I_{out} - \frac{\Delta i_L}{2} \tag{3}$$

$$D_{eff} = D \cdot (N-1) - floor(D \cdot (N-1)) \tag{4}$$

$$\Delta i_{pp} = \frac{V_{in} \cdot (D_{eff} \cdot (1 - D_{eff}))}{L \cdot f_{sw} \cdot (N-1)^2} \tag{5}$$

Inherent to the FCML operation are both the converter duty cycle, D, and an effective duty cycle, D_{eff}, (given by (4)) at the switching node, V_{sw}, which affects the inductor current ripple, Δi_{pp}, (given by (5)). It is apparent that D_{eff} is zero for certain values of D (when $D \cdot (N-1)$ is an integer value) and therefore, the inductor current ripple approaches zero as well. Fig. 3 shows the inductor current ripple at a fixed switching frequency, f_{sw}, and fixed inductor, L, for a 4- and 5-level FCML normalized to the conventional two-level buck converter, with current ripple valleys at duty cycles of 0.33 and 0.66 for the 4-level FCML, and 0.25, 0.5, and 0.75 for the 5-level FCML. Previous works [8], [9] have shown that by varying the switching frequency along the duty cycle range, the inductor current ripple can be changed to maintain ZVS operation. However, the switching frequency can only

be decreased to limits imposed by the flying capacitor ripple, inductor saturation, or practical limitations [9]. These switching frequency limitations are summarized in Subsection III-C along with an evaluation of how the resonant frequency should be factored in to the ZVS frequency limitation. Moreover, the valleys of the inductor current ripple plot in Fig. 3, cannot be avoided by decreasing the switching frequency and consequently, ZVS cannot be maintained at these operating points.

A. Dynamic Level Selection

Here, we propose to use dynamic level selection to maintain a minimally sufficient inductor current ripple required for ZVS operation. Fig. 4 illustrates the proposed method for selecting the number of levels to operate across all duty cycles. Over the full range of duty cycles, we plot the switching frequency required to achieve ZVS for 4- and 5-level operation and a minimum switching frequency, f_{lim}, for which the converter is not designed to operate below. This plot is for a constant peak negative inductor current which can be controlled to maintain ZVS [22]. At each duty cycle, we prioritize 5-level operation because the switch voltage stress and therefore, the switching losses, is reduced in the case of a higher number of levels. Moreover, as shown in [23], lower device operating voltage also reduces dynamic $R_{ds,on}$ effects in GaN transistors, another important design consideration. The voltage swing of the inductor is also reduced for the case of a higher number of levels, consequently reducing inductor core losses. If the 5-level switching frequency must be below f_{lim} to maintain ZVS, the converter transitions to 4-level operation at a new switching frequency to maintain ZVS. However, there are some duty cycles for which both the 4- and 5-level converter have ZVS frequencies below their respective f_{lim} values; in these cases, we operate as a 5-level converter because efficiency benefits of a higher level count as described above, even without maintaining full ZVS conditions. Operating maps for varied input voltages and output load currents are shown in Fig. 5. As the input voltage changes, the duty cycles for which 4-level or 5-level operation is preferred varies slightly. Here, as input voltage changes, the load current and deadtime are kept constant, but the negative inductor current valley is updated to provide the necessary energy for ZVS as the blocking voltage of the switch changes with the input voltage. For the load range operating map, the input voltage, deadtime, and inductor current valley are all kept constant. Fig. 5 shows the prioritization of 5-level operation across a range of operating conditions.

B. Dynamic Level Operation

While dynamically changing the number of levels of the FCML converter yields ZVS benefits, there are numerous practical challenges to enable seamless transition between these distinct operating points. As there are various ways in which to reconfigure the circuit topology to alter the level-count, there are practical concerns in terms of transient response, voltage stress, and active balancing that must be considered. Moreover, the impact of each flying capacitor voltage during transitions is complex, owing to the number of charge/discharge paths of

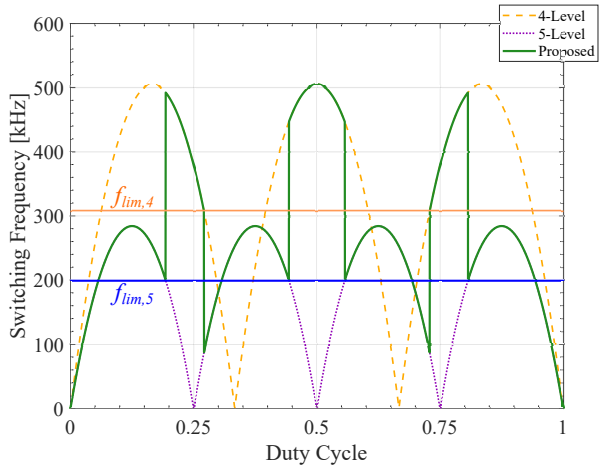
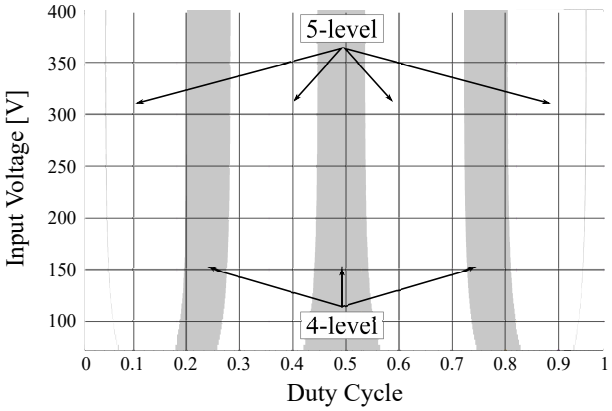
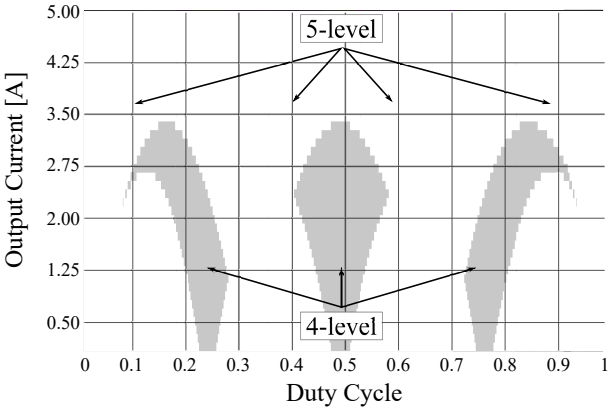


Fig. 4: The proposed method implements dynamic level changing to avoid operation at the inductor current ripple valleys and to maintain ZVS across the entire duty cycle range.



(a) Operating mode for varied input voltages at a 1.75 A output load current.



(b) Operating mode for varied load currents at a 100 V input voltage.

Fig. 5: Operating map for mode determination across the duty cycle range for varied input voltages (Fig. 5a) and output currents (Fig. 5b).

the FCML converter. Here, we outline some of these practical challenges, and motivate our choice of operating transitions.

An analysis of the steady-state capacitor voltages for different number of FCML levels informs the selection of the number of levels in the converter and the ideal switch control method. Configurable level operation in this work utilizes switches controlled similarly in phase so that the effective

TABLE I: 4/5 Level Switch Pair Configurations and Flying Capacitor Impact

Level	Pair	S_4	S_3	S_2	S_1	V_{C3}	V_{C2}	V_{C1}	ΔV_C		
									C_3	C_2	C_1
5		$\frac{1}{4}V_{in}$	$\frac{1}{4}V_{in}$	$\frac{1}{4}V_{in}$	$\frac{1}{4}V_{in}$	$\frac{3}{4}V_{in}$	$\frac{1}{2}V_{in}$	$\frac{1}{4}V_{in}$	0	0	0
4a	S_4, S_3	$\frac{1}{4}V_{in}$	$\frac{1}{12}V_{in}$	$\frac{1}{3}V_{in}$	$\frac{1}{3}V_{in}$	$\frac{3}{4}V_{in}$	$\frac{2}{3}V_{in}$	$\frac{1}{3}V_{in}$	0	$+\frac{1}{6}V_{in}$	$+\frac{1}{12}V_{in}$
4b	S_3, S_2	$\frac{1}{3}V_{in}$	$\frac{1}{6}V_{in}$	$\frac{1}{6}V_{in}$	$\frac{1}{3}V_{in}$	$\frac{2}{3}V_{in}$	$\frac{1}{2}V_{in}$	$\frac{1}{3}V_{in}$	$-\frac{1}{12}V_{in}$	0	$+\frac{1}{12}V_{in}$
4c	S_2, S_1	$\frac{1}{3}V_{in}$	$\frac{1}{3}V_{in}$	$\frac{1}{12}V_{in}$	$\frac{1}{4}V_{in}$	$\frac{2}{3}V_{in}$	$\frac{1}{3}V_{in}$	$\frac{1}{4}V_{in}$	$-\frac{1}{12}V_{in}$	$-\frac{1}{6}V_{in}$	0

number of switches coincides with the desired level operation. The steady-state capacitor voltages for 5-level operation, as well as for 4-level operation with different switches operated as a pair are shown in Table I. Additionally, the magnitude of capacitor voltage change required to transition from 5-level to 4-level operation is also shown. To elucidate the design considerations, this analysis was performed for 5/4, 6/5, and 7/6 level converters. Transitioning from a higher odd number of levels down to an even number of levels reduces the capacitor voltage change required. For the 5/4 converter and the 7/6 converter, the minimum voltage change required is $\frac{1}{12}V_{in}$ and $\frac{1}{15}V_{in}$, respectively compared to the 6/5 level converter which requires $\frac{1}{10}V_{in}$. For the 7/6 level converter, two flying capacitors would need to change by $\frac{1}{30}V_{in}$ and two by $\frac{1}{15}V_{in}$, with one remaining unchanged. However, for the 5/4 level converter, the capacitors which need re-balancing all require the same change in voltage, therefore simplifying the active balancing technique used to re-balance the flying capacitors.

Furthermore, this evaluation of the steady-state flying capacitor voltages is used to select which switch pair to operate in phase when in the 4-level mode [10]. When the two middle switch pairs, S_3 and S_2 in Fig. 6, are operated as one switch pair, configuration $4b$, the blocking voltage of the transistors is more evenly distributed, therefore distributing the voltage stress on each of the transistors. Considering the amount of capacitor voltage change required to re-balance on a new number of levels, the configuration with the middle pairs acting as one yields the smallest ΔV in flying capacitor voltage, $\frac{1}{12}V_{in}$.

In 4-level operation, the two middle pairs of switches (labeled S_2 and S_3 in Fig. 6) are controlled in phase as shown by control signals q_{2A} and q_{3A} in Fig. 7a. This switch pair is chosen so that the amount the flying capacitor voltages need to adjust by is minimized. The remaining switch pairs are operated as a 4-level FCML with a phase shift of 120°, shown in Fig. 7a. Consequently, the voltage on the middle flying capacitor (labeled C_2 in Fig. 6) remains constant at $V_{in}/2$ from the 5-level operation, while the remaining flying capacitors, C_1 and C_3 are actively re-balanced to $V_{in}/3$ and $2 \cdot V_{in}/3$, respectively, in accordance with 4-level FCML operation, as shown in Table I.

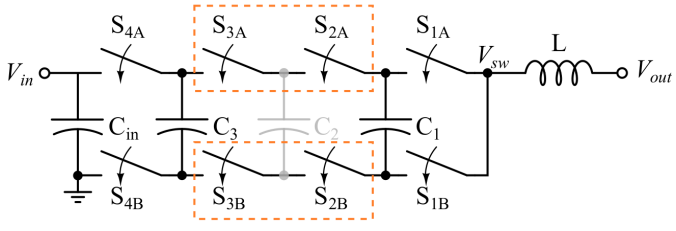
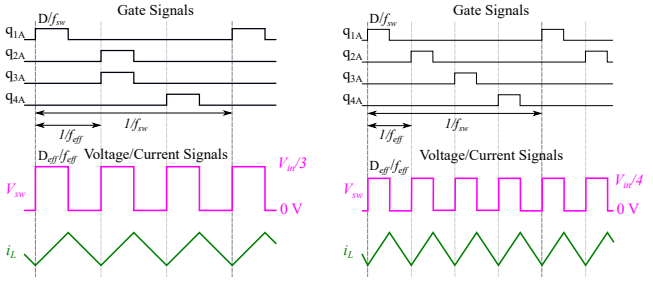


Fig. 6: The 5-level FCML operated as a 4-level with C_2 voltage maintained at the 5-level value while C_1 and C_3 re-balance to 4-level operation.



(a) Four-level operation. (b) Five-level operation.

Fig. 7: Simulated converter waveforms for the proposed method.

Similarly, when the converter needs to transition from 4-level to 5-level operation, the capacitors are re-balanced to 5-level voltages by natural or active balancing techniques. The middle switch pairs are no longer controlled by similar PWM signals and the control scheme returns to that of the 5-level FCML, shown in Fig. 7b. When sizing the switches and capacitors [4], the voltage ratings of the 4-level operation should be used since they are of greater magnitude, as shown in Table I. Over-sizing components for a portion of operating conditions, when the 5-level converter acts as a 4-level converter, or alternatively increasing the number of components to add the ability for a 4-level FCML to operate as a 5-level FCML are potential drawbacks to implementing dynamic level selection. The designer should weigh the benefits of achieving ZVS versus a lower component count as well as against component rating requirements.

C. Frequency Limitations

As mentioned above, there are limitations placed on the lower limits of the converter switching frequency, which prevent zero-voltage switching conditions. These limits, summarized in Table II for 5-level operation, are due to converter components [9], such as inductor current saturation or flying capacitor voltage ripple, and due to converter operation (i.e. resonance) [24]. In [9], the component frequency limitations are derived for 4-level operation. Moreover, the resonant frequency of the converter must also be accounted for when determining the lower limit on switching frequency. As shown in Fig. 8, when operating near resonant frequency, the inductor current is no longer linear which causes the negative peaks of the inductor current to vary throughout the switching period.

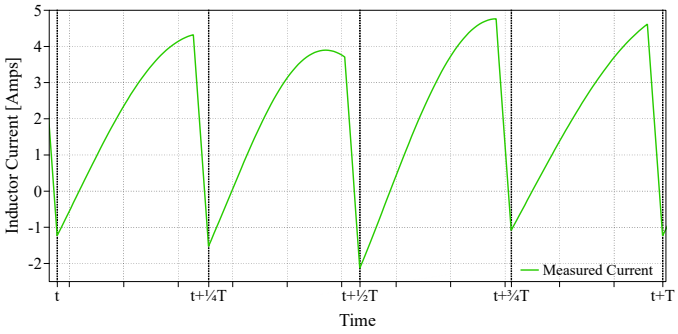
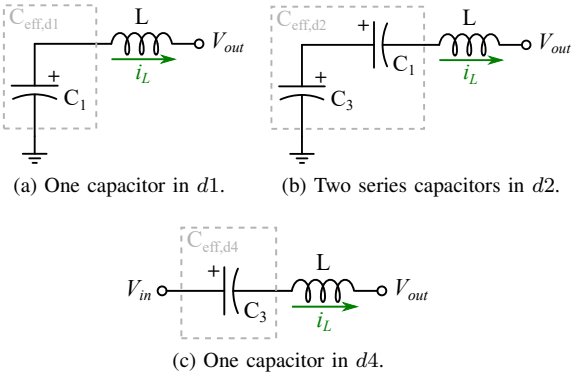


Fig. 8: When operating near resonant frequency, the inductor current is not linear, and therefore, only quasi-ZVS may be possible.



(a) One capacitor in $d1$. (b) Two series capacitors in $d2$.

(c) One capacitor in $d4$.

Fig. 9: Effective capacitances for each of the sub-periods in a switching cycle.

Because of this variation, the converter is unable to maintain ZVS in quasi-resonant operation without additional implementation complexity such as valley current detection and setting specific deadtimes for each current valley [22]. As detailed in [24], there are two resonant frequencies for the FCML converter based on the switching configuration when current flows through either one or two flying capacitors. The resonant frequency, f_{swRes}, is given by the equation in Table II, where C_{eff} is given by either one or two series-connected flying capacitors, depending on the switch configuration. Fig. 9 shows the effective capacitance during each sub-period, $d1$, $d2$, and $d4$, in Table III. To avoid quasi-resonant operation and maintain linear inductor current, a switching frequency limit is chosen to be sufficiently larger than the resonant frequency of the two flying capacitors in series (1.5 to 2.5 times higher).

IV. Active Balancing

Level transitioning requires flying capacitor re-balancing because the steady-state voltages on flying capacitors, C_1 and C_3, are at different values based on the number of levels, as shown in Table I. The FCML topology has natural balancing qualities [25]–[29], which will re-align the capacitor voltages with steady-state operation after time. However, more switching cycles spent in an unbalanced condition, leads to more uneven voltage stress on the transistors. To reduce the amount of re-balancing time necessary, active balancing techniques can be used. Previous work [10] on level transitioning in FCML converters has used repeated switch states within each cycle in order to increase/decrease the charge on the capacitors. However, here we utilize a technique of duty cycle adjustment [6], [22], [30] to increase or decrease the charge/discharge time of the flying capacitors that require re-balancing.

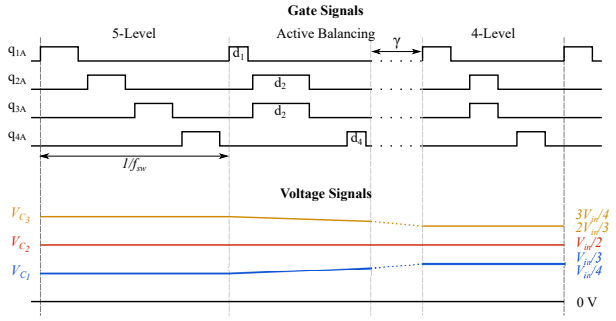


Fig. 10: Active balancing through duty cycle adjustment is implemented at transitions between different numbers of levels.

Active balancing of the converter is done in 4-level operation because FCML converters have been shown to have more balanced performance on even-numbered levels [29]. When transitioning from 4- to 5-level operation, the flying capacitors are re-balanced to 5-level voltages before the control signals are changed to the 5-level configuration. Table III shows the charge/discharge behavior of the flying capacitors for sub-periods in the lowest duty cycle range of 4-level operation (0 - 33%). For the transition from 5- to 4-level operation, the voltage on capacitor C_1 needs to increase and the voltage on capacitor C_3 needs to decrease, while capacitor C_2 is maintained. To achieve this voltage differential, the sub-period where C_1 charges (indicated by a '+'), $d2$, when the middle switch pairs (S_2/S_3) are on (indicated by '1' in Table III), should be increased, while the sub-period where C_1 discharges (indicated by a '$-$'), $d1$, when switch S_1 is on, should be decreased. Similarly, to decrease the voltage on C_3, sub-periods $d2$ and $d4$ should be increased and decreased, respectively.

In contrast, active re-balancing for the transition from 4- to 5-level operation is accomplished by decreasing $d2$ while increasing $d1$ and $d4$. The sub-periods $d1$ and $d4$ are adjusted equivalently and are changed with respect to $d2$ so that the effective duty cycle at the switch node remains equivalent to that of normal 4-level operation [6], [22]. Equation 6 shows the relationship between the switching sub-periods in 4-level operation for the case of duty cycles less than 33%. Equations for the sub-periods in the remaining duty cycle ranges are provided in Table IV in [22]. Applying this duty cycle adjustment technique across multiple switching cycles can re-balance the voltages to the new steady-state operation values as shown in Fig. 10.

$$D_{eff} = d_2 + d_1 + d_4 = d_2 + 2 \cdot d_1 \tag{6}$$

The two parameters governing the speed at which the converter balances, using constant effective duty cycle (CEDC) active balancing [22], are the duty cycle adjustment, α, and the number of cycles of active balancing, γ. The shortest settling time of the flying capacitor voltages can be achieved by applying the correct combination of α and γ. Appendix A discusses the Monte Carlo method used to determine the best combination for a specific input voltage and a range of output current values. The number of active balancing cycles, γ, and the corresponding α values for the shortest settling

TABLE II: Frequency Limits

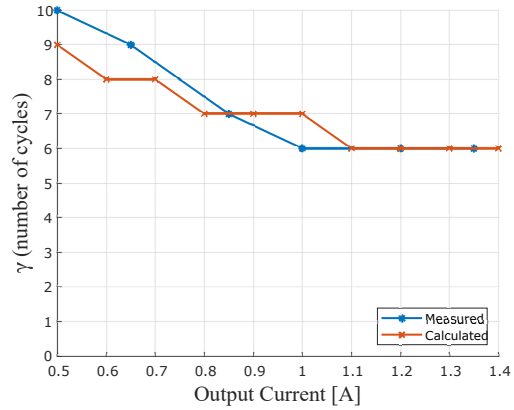
	$0 < D < \frac{1}{4}$	$\frac{1}{4} < D < \frac{3}{4}$	$\frac{3}{4} < D < 1$
f_{swCfly}	$\frac{I_L \cdot D_{eff}}{2 \cdot C_{fly} \cdot \%V_r \cdot V_{in,pk}}$	$\frac{I_L}{2 \cdot C_{fly} \cdot \%V_r \cdot V_{in,pk}}$	$\frac{I_L \cdot (1-D_{eff})}{2 \cdot C_{fly} \cdot \%V_r \cdot V_{in,pk}}$
f_{swIsat}	$\frac{V_{in,pk} \cdot (D_{eff} \cdot (1-D_{eff}))}{2 \cdot L \cdot (N-1)^2 \cdot (I_{sat}-I_L)}$	$\frac{V_{in,pk} \cdot (D_{eff} \cdot (1-D_{eff}))}{2 \cdot L \cdot (N-1)^2 \cdot (I_{sat}-I_L)}$	$\frac{V_{in,pk} \cdot (D_{eff} \cdot (1-D_{eff}))}{2 \cdot L \cdot (N-1)^2 \cdot (I_{sat}-I_L)}$
f_{swRes}	$\frac{1}{2\pi\sqrt{L \cdot C_{eff}}}$	$\frac{1}{2\pi\sqrt{L \cdot C_{eff}}}$	$\frac{1}{2\pi\sqrt{L \cdot C_{eff}}}$
f_{swZVS}	$\frac{V_{in,pk} \cdot (D_{eff} \cdot (1-D_{eff}))}{2 \cdot L \cdot (N-1) \cdot (I_L - I_{ZVS})}$	$\frac{V_{in,pk} \cdot (D_{eff} \cdot (1-D_{eff}))}{2 \cdot L \cdot (N-1) \cdot (I_L - I_{ZVS})}$	$\frac{V_{in,pk} \cdot (D_{eff} \cdot (1-D_{eff}))}{2 \cdot L \cdot (N-1) \cdot (I_L - I_{ZVS})}$

TABLE III: Flying Capacitor Charge and Discharge Sub-periods

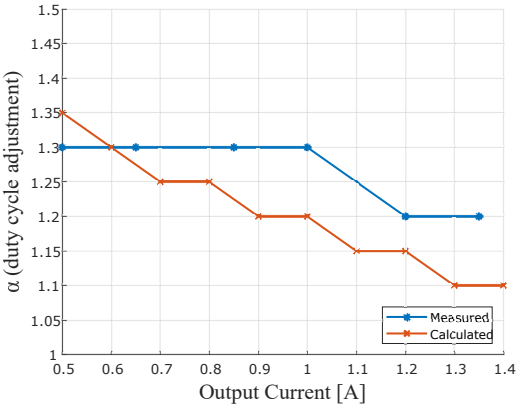
Sub-period	S_{4A}	S_{3A}/S_{2A}	S_{1A}	V_{C3}	V_{C2}	V_{C1}
d1	0	0	1			−
d2	0	1	0	−		+
d4	1	0	0	+		

time, shown in Fig. 11 decrease as the average output current, increases.

The shortest settling time is achieved by allowing the maximum amount of energy transfer between the flying capacitors and the output, while maintaining any constraints placed on the peak inductor current and output voltage ripple. A larger transfer of energy per cycle occurs when α is larger because the inductor current increases for a longer amount of time (during sub-period $d2$). Therefore, at lower current, larger duty cycle adjustments are required. Furthermore, at lower currents, more active balancing cycles are needed because the duty cycle adjustment, α, is limited by the output voltage ripple. As the output current increases, α is also limited by the saturation current of the inductor. However, with higher average output current, more energy can be transferred in each sub-period between the capacitors, thereby necessitating both lower duty cycle adjustment and fewer active balancing cycles. At low output current, the drawback of using this active re-balancing method is that, the current ripple needs to be increased. During this relatively short time of re-balancing, a large current ripple to average current ratio may be required, therefore, incurring more losses. Moreover, for low duty cycles and low input voltage, it may not be possible to have enough current ripple to re-balance in a reasonable amount of time. Another interesting operating condition is circuit response to a load step or change in input voltage. Without current peak/valley detection and control [6], [22], [31], the modeled active balancing parameters may be sub-optimal for active re-balancing of the flying capacitors during a level transition.



(a) Values of γ (number of switching cycles) in combination with the α (duty cycle adjustment ratio) value in Fig. 11b.



(b) Values of α (duty cycle adjustment ratio) in combination with the γ (number of switching cycles) value in Fig. 11a.

Fig. 11: Comparison of measured and calculated balancing parameters for an input voltage of 50 V and a range of output voltages.

V. Experimental Results

A 5-level FCML converter, Figs. 12 and 13, was designed and constructed to demonstrate this control technique that maintains ZVS across the full duty cycle range. The prototype was built using 100 V GaN devices from GaN Systems due to their low conduction and switching losses. Because these GaN devices are bottom-side cooled, the FCML was constructed on a single-sided PCB to facilitate a heat sink across the bottom side. Assembling the FCML on a single side increases the commutation loop and introduces more parasitic inductance into the conduction path. To decrease the commutation loop area and absorb the excess parasitic energy, local decoupling capacitors are used for each switch pair [9]. Additionally, previous work [32] has proven the merit of using a cascaded bootstrap technique to power the isolated gate drivers for each switch of the FCML. The cascaded bootstrap technique has a reduced area and better efficiency when compared to the conventional single IC isolated gate driver [32], [33]. Table IV

TABLE IV: Component Listing of the Hardware Prototype

Function Block	Component	Mfr. & Part Number	Parameters
FCML	GaN FETs	GaN Systems GS61008P	100 V, 7mΩ
	Capacitors (C_1, C_2, C_3)	TDK C5750X6S2W225K250KA × 3	450 V, 2.2μF
	Capacitors (C_{in})	TDK C5750X6S2W225K250KA × 8	450 V, 2.2μF
	Capacitors (C_{out})	TDK C5750X6S2W225K250KA × 4	450 V, 2.2μF
	Inductor (L)	Vishay IHLP4040DZ-01	26 A, 2.2μH
Cascaded Bootstrap	Isolated gate drivers	Silicon Labs SI8271GB-IS	
	Bootstrap Diodes	Vishay VS-2EFH02HM3	400 V
	LDO	Texas Instruments LP2985IM5-6.1/NOPB	
Controller Board	Logic level shifters	Texas Instruments SN74LV4T125PWR	
	Microcontroller	Texas Instruments TMX320F28377D	

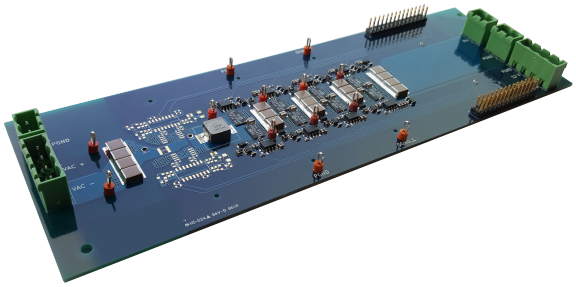


Fig. 12: ZVS is achieved across the full conversion range on a 5-level FCML hardware prototype.

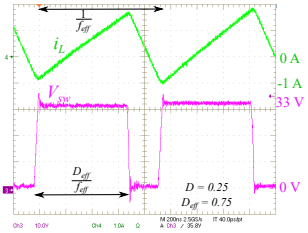


Fig. 14: ZVS is achieved for 4-level operation at a duty cycle for which 5-level operation cannot achieve ZVS.

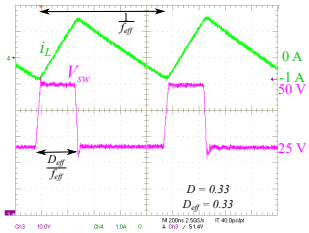


Fig. 15: ZVS is achieved for 5-level operation at a duty cycle for which 4-level operation cannot achieve ZVS.

shows the full component listing of the hardware prototype. While the 100 V GaN devices used here could be implemented with a larger input voltage due to the reduction in voltage stress as a characteristic of the FCML converter, we chose devices with a conservative voltage rating for this application, solely for reducing the risk of damage during testing of this dynamic level shifting operation.

To demonstrate the proposed method, the experimental prototype was tested in multiple operating conditions. Fig. 14 shows measured oscilloscope waveforms with the converter operating as a 4-level FCML at an input voltage of 100 V, 10 W, a switching frequency of 350 kHz, and a duty ratio of 25%, which, as shown in Fig. 3, is an operation point where the 5-level FCML has no current ripple and cannot maintain ZVS. The inductor current ripple is shown to go negative which discharges the parasitic capacitances of the high-side transistors and allows ZVS, which is evident by the minimal overshoot on the rising edge of the switch-node voltage, V_{sw}.

Likewise, Fig. 15 shows the converter operating in ZVS as a 5-level FCML at the same voltage and loading condition, a 255 kHz switching frequency and a 33% duty ratio, which is a current ripple valley of the 4-level converter. These results show that ZVS is possible at two different duty cycles for which ZVS is not possible with a fixed number of levels.

A dynamic transition between levels is demonstrated in Fig. 16. In this case, the converter transitions from 5-level to 4-level operation (Fig. 16a) and vice-versa (Fig. 16b) with only natural balancing. The measured settling time of the capacitor voltages, V_{C1} and V_{C3} for the 5- to 4-level transition is about 2.8 ms and from 4- to 5-levels is about 0.89 ms. Fig. 17 shows the transition from 5- to 4-level operation with a region of active balancing by duty cycle adjustment to charge C_1 and discharge C_3 from 5-level steady-state voltages to 4-level voltages. The capacitor voltages balance to steady-state in 88 μs, which is over 30 times faster than the settling time using natural balancing. Fig. 18 shows the transition from 4- to 5-level operation with active balancing, which takes 0.66 ms,

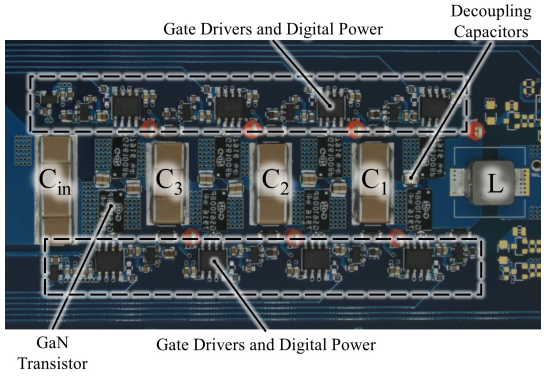
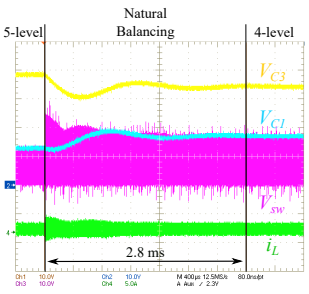
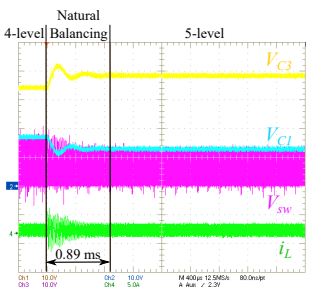


Fig. 13: Annotated photograph of the experimental prototype.



(a) Five to four level transition.



(b) Four to five level transition.

Fig. 16: Level transitioning with natural balancing.

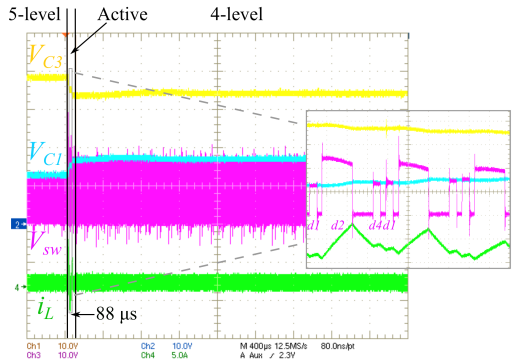


Fig. 17: Active balancing decreases the settling time of capacitors C_1 and C_3 during a transition from 5- to 4-level operation.

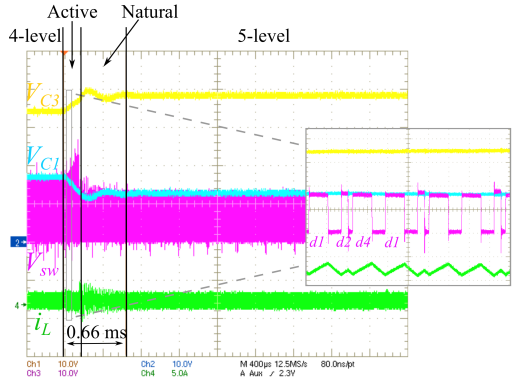


Fig. 18: Active balancing decreases the settling time of capacitors C_1 and C_3 during a transition from 4- to 5-level operation.

which is about 1.3 times faster than natural balancing alone.

When performing active balancing, two parameters can be tuned for different balancing characteristics — the magnitude of duty cycle adjustment, α, and the number of active balancing cycles, γ. If rapid balancing is desired, the percent change of duty cycles, α is set high, with a corresponding low number of active balancing cycles, γ. Alternatively, slower, but with less inductor current ripple induced, balancing operation can be achieved with low percent change of duty cycles, and a higher number of active balancing cycles. In the case of the 5- to 4-level transition, shown in Fig. 17, seven cycles of active balancing were used and the sub-periods were adjusted: d_2 was 40%, or twice the width of the baseline duty cycle of 20%, and d_1 and d_4 where each 10%, maintaining a constant effective duty cycle at the switch node of 60%. This approach demonstrates a more aggressive duty cycle adjustment with a smaller number of active balancing cycles, which leads to a shorter settling time, with the trade-off of a brief time period with increased current ripple and larger output voltage ripple. However, if a more moderate adjustment to duty cycle and more cycles of active balancing can be permitted, then the magnitude of the increased current ripple can be lower as shown in Fig. 19 (d_2 at 25% for 25 cycles) as compared to aggressive re-balancing in Fig. 17. Both moderate and aggressive implementations of active balancing still reduce the settling time when compared to natural balancing.

The output voltage is also disturbed during this mode transition. Fig. 20 compares the output voltage ripple for

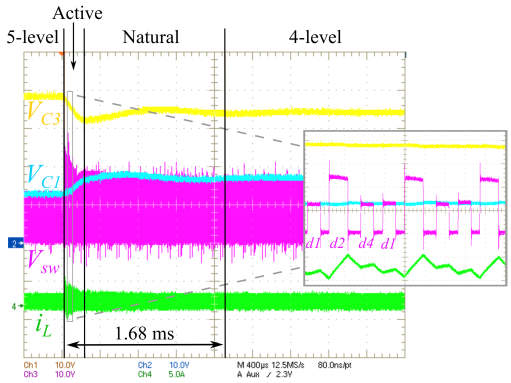


Fig. 19: Level transitioning with less aggressive active balancing has a longer settling time, but a lower magnitude of increased inductor current ripple.

the aggressive and moderate re-balancing cases shown in Fig. 17 and 19. Furthermore, the output capacitance can be increased to allow for more aggressive, and therefore quicker, active balancing transition. The output voltage deviation with an output capacitance ∼4x larger than the already exhibited transition is reduced by 9%, shown in Fig. 20. The designer can size the output capacitance appropriately with the desired transition speed, as detailed in the Appendix.

To demonstrate the efficiency benefits of the proposed control method, we tested 4- and 5-level operation over a wide range of duty cycles. The efficiency at each duty cycle was measured in 4- and 5-level operation at 100 V_{in} and 0.5 A load with constant negative inductor current peak, I_{ZVS}, with a high precision power analyzer (Keysight PA2201A). The frequency was adjusted to achieve ZVS conditions, if possible, without violating the converter frequency limitation. The switching frequency limitations, as well as the required frequency for ZVS, from Table II are shown for each 4- and 5-level operation at a specific duty ratio, 28%, in Fig. 21a and 21b, respectively. This duty ratio was selected to highlight as it is near a transition point between the two modes. In regions where both the 4- and 5-level ZVS switching frequency violates the limit, the converter operates in the 5-level mode, with a relaxed switching frequency limit. In the tested operating conditions, because the resonant frequency is the critical frequency for choosing the limit, operating slightly below this limit does not violate the f_{swCfly} or f_{swIsat} limits. However, operating below the switching frequency limit means

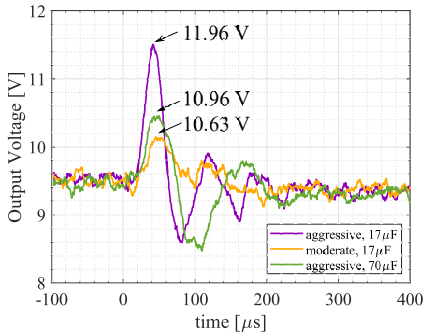
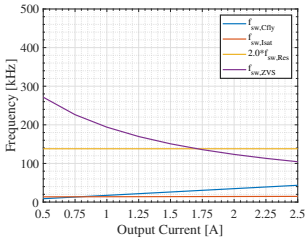
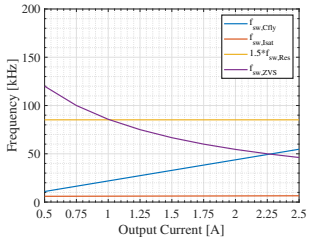


Fig. 20: The output voltage ripple disturbance caused by the active re-balancing transition can be reduced by either choosing more moderate transition parameters or by increasing the output capacitance.

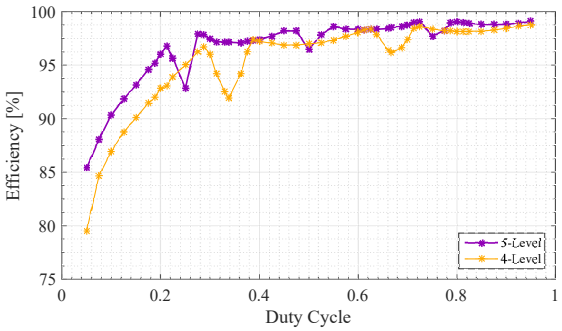


(a) 4-level FCML switching frequency limitations.

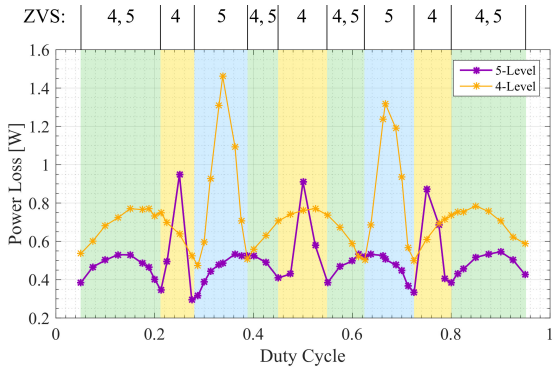


(b) 5-level FCML switching frequency limitations.

Fig. 21: Switching frequency limitations for the 4-level and 5-level FCML, near a transition point, at 28% duty cycle, as well as the required switching frequency to achieve ZVS.



(a) Efficiency measurements of 4- and 5-level operation, maintaining ZVS where possible without violating converter switching frequency limitations.



(b) Corresponding power loss for 4- and 5-level operation.

Fig. 22: Higher efficiency points closely correspond with the proposed method in Fig. 4.

that the converter is in a quasi-resonant mode, and as described above, ZVS may only occur on some switching edges instead of all edges. This quasi-resonant operation is allowed until either level mode has a ZVS frequency above its corresponding limit.

Fig. 22 shows the efficiency of 5- and 4-level operation at each duty cycle, which aligns with the proposed level transitioning technique in Fig. 4. Operation as in 4-level mode is more efficient than the 5-level mode for duty cycle ranges around 25%, 50%, and 75%, shaded yellow in Fig. 22, when the 5-level converter exhibits a current ripple minimum and cannot maintain ZVS, but where the 4-level can. In this case, the switching losses and core losses in non-ZVS 5-level operation are greater than the core losses on the 4-level converter. Furthermore, operation as a 5-level converter is more efficient for regions surrounding 33% and 66%, shaded blue in Fig. 22, which are the regions where the 4-level converter cannot achieve ZVS. In the green-shaded regions, both the 4- and 5-level converters achieve ZVS. In these regions, the 5-level is more efficient because, as shown in Fig. 4, in these duty cycle ranges, the switching frequency needed to maintain ZVS for the 5-level converter is lower than for 4-level operation. Due to the higher level count and lower switching frequency, the 5-level converter has lower switching losses and lower core loss. For both the 4- and 5-level converters, when ZVS can be maintained, the losses display a nearly sinusoidal characteristic similar to that of the proposed method and equations of [9]. Despite the 4-level converter operating at a much higher switching frequency, the switching losses can be reduced by maintaining ZVS, therefore demonstrating the benefit of dynamic level transitioning in order to maintain ZVS across duty cycles. For this experimental prototype, the regions where 4-level operation has higher efficiency represent a small percentage of the total duty cycle range; however, there are several simple circuit optimizations that can lead to overall higher efficiency as well as an increase in the duty cycle ranges with higher 4-level efficiency. Some of these design adjustments that this work has not incorporated include: optimal inductor selection for a better balance of conduction and switching losses, as well as dynamic deadtime/current valley adjustment across the load range.

Furthermore, this converter was tested at the same input voltage, 100 V, across a range of loads, 0.5 A to 2.5 A, maintaining a constant negative inductor current value for ZVS, I_{ZVS}. Fig. 23 shows the efficiency for a duty cycle near a transition point, 28%. Additionally, a loss estimation for the tested conditions is shown in Fig. 24. The switching frequency was again chosen to allow for ZVS if possible without violating any of the converter limitations. These limits for this operating point are shown in Fig. 21a and 21b. At lighter load, the 5-level converter can achieve ZVS and has a greater efficiency than the 4-level converter which is also achieving ZVS. However, as the load increases, the switching frequency of the 5-level converter is limited by the resonant frequency and can no longer maintain ZVS. On the other hand, the 4-level converter is not yet frequency limited and still exhibits ZVS. However, as demonstrated by the loss breakdown in Fig. 24, even though the 4-level converter has reduced switching losses, the inductor AC losses increase as more current ripple is required to maintain ZVS. Additionally, due to the reduced number of levels, the core losses of the 4-level converter are naturally higher than of the 5-level converter. The difference in inductor losses show that at a specific duty cycle and across a load range, maintaining ZVS, and using this dynamic level transitioning method, may not be a priority for loss reduction. Moreover, further increasing the load, forces the 4-level converter into frequency limitations and ZVS is no longer maintained. For these scenarios, the 5-level mode should be prioritized as described by the proposed dynamic level transitioning method. The efficiency of the 5-level mode is higher than the 4-level mode when neither can keep ZVS conditions. The additional measured losses are shown in Fig. 24. The discrepancy in the model and the measured efficiency is in part due to various circuit non-

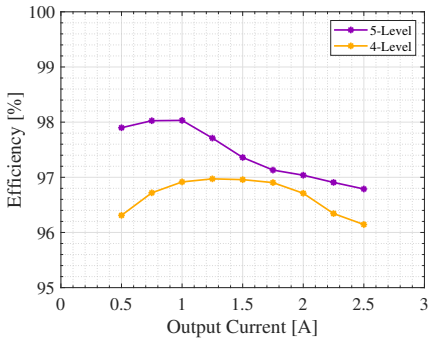


Fig. 23: Efficiency measurements of 4- and 5-level operation across a load range near a transition point, maintaining ZVS where possible without violating converter switching frequency limitations.

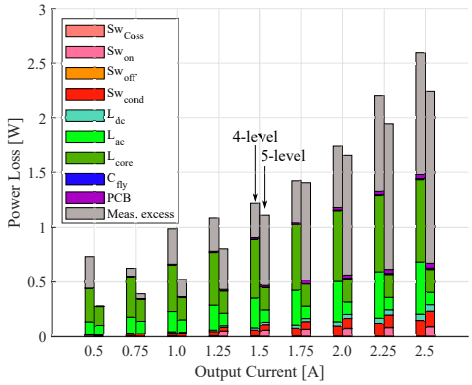


Fig. 24: Estimated loss breakdown for the tested conditions in Fig. 23.

idealities that are not modeled in the loss estimation, such as: mismatched flying capacitance values. As load increases, the mismatch between flying capacitance values could lead to the loss of ZVS on some of the switches due to unequal inductor current valleys.

VI. Conclusion

This paper presented a method for maintaining ZVS across the full range of duty cycles for an FCML converter by both controlling the switching frequency and dynamically changing the number of levels. An analysis of flying capacitor voltages and switch configurations was used to determine the number of levels and the switching scheme to achieve dynamic level transitioning. Additionally, a method of dynamic level transitioning with active capacitor balancing through duty cycle adjustment was detailed. A hardware prototype was constructed using bottom-side cooled GaN Systems devices, a single-sided PCB for improved cooling methods, and a cascaded bootstrap to supply the isolated gate drivers. The prototype achieved ZVS operation under 4-level and 5-level conditions at duty cycles not possible for a fixed number of levels. Dynamic level transitioning with active re-balancing of the flying capacitors was demonstrated in hardware. A method for determining the active balancing parameters was derived including a curve-fit for simple implementation in a controller. Transitioning between numbers of levels to avoid inductor current ripple valleys and maintain ZVS improves converter efficiency by reducing switching losses, which allows for more power dense designs.

Appendix A
Active Balancing Parameter Calculation

A Monte Carlo analysis of the converter design space and active balancing parameters was performed to determine the combination which would lead to the shortest settling time of the flying capacitor voltages during a level transition. Converter parameters are defined, such as input voltage, V_{in}, average output current, I_{out}, inductance, L, flying capacitance, $C_{fly,k}$, output capacitance, C_{out}, and the levels for transitioning, starting level, N_0, ending level, N_1. The valley current, I_{ZVS}, is defined for calculating the ZVS frequencies. Furthermore, the design space is set up to limit the duty cycle adjustment parameter, α, and the number of active balancing cycles, γ. The parameter, α is constrained by not allowing any of the sub-periods, T_1, T_2, T_4 in Fig. 25 to be greater than 1 (where 1 corresponds to a full switching period). This limitation is also equivalent to maintaining sub-period duty cycles, d_1, d_2, d_4, below D_{eff}. Equations (7a-d) show the calculation of this limit for the lowest duty cycle range. The maximum number of cycles, Γ is decided by the designer.

$$[d_2 = \alpha D] \leq [D_{eff} = (N-1)D], \tag{7a}$$

$$\alpha \leq (N-1) \tag{7b}$$

With all of the parameters specified, the switching frequency limitation for the converter is calculated based on operating conditions (V_{in}, I_{out}) and component parameters (L, C_{fly}). A switching frequency limitation is chosen for both 4- and 5-level operation by choosing the maximum switching frequency of the calculated switching frequencies (f_{swCfly}, f_{swIsat}, and f_{swRes} in Table II) across all duty cycles. If the converter operates above the maximum of these limits, none of the limits will be violated at any duty cycle. Then, based on these switching frequency limits, the duty cycle, D_{tran}, when the ZVS frequency crosses the limit, $f_{lim,N}$, is calculated. At this duty cycle the converter will dynamically transition levels to maintain ZVS. Because 5-level operation is prioritized, if the ZVS switching frequency falls below the 5-level limit, the converter transitions from 5- to 4-level only until the 5-level ZVS frequency is above the 5-level limit, at which point the converter transitions back to 5-level operation. If both the 4- and 5-level ZVS frequencies violate their respective limits, 5-level operation is used as discussed previously.

The maximum inductor current ripple allowed, $i_{pp,max}$, is calculated based on the output capacitance allowable ripple (8) [24], which as mentioned in Section IV is an important limiting factor.

$$\Delta V_{out} = \frac{1}{N} \frac{\Delta i_{pp,max}}{8 f_{sw} \cdot C_{out}} \tag{8}$$

The N_0 voltages and currents are calculated for the starting point of the level transitioning and active re-balancing. Then the converter voltages and currents are calculated for a randomly selected (from the predetermined range of γ) number active balancing and a randomly selected duty cycle adjustment value, α. Fig. 25 shows an example active balancing switching cycle with sub-periods used in calculating

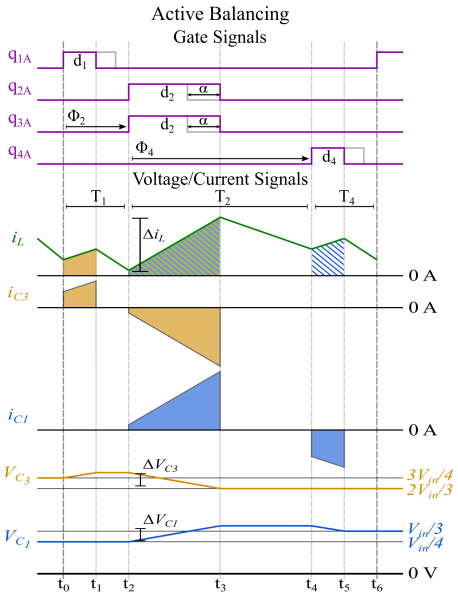


Fig. 25: Sub-periods for the lowest duty-cycle range for calculating active balancing capacitor voltages.

the voltages and currents. For an N-level converter, there are $2 \cdot (N-1)$ sub periods within a switching cycle. For each sub-period, the following are calculated:

1) Inductor voltage, $V_L(t)$, from $V_{sw}(t-1)$ and $V_{out}(t-1)$
2) Change in inductor current, $\Delta i_L(t)$, from (9), where d_x is the ratio of the sub-period to the full switching period

$$\Delta i_L(t) = \frac{V_L \cdot d_x \cdot T}{L} \tag{9}$$

3) Updated inductor current:

$$i_L(t) = i_L(t-1) + \Delta i_L(t) \tag{10}$$

4) Capacitor de-rating for $C_{fly,k}(t)$ and $C_{out}(t)$, based on $V_{C,k}(t-1)$ and $V_{Cout}(t-1)$
5) Capacitor current, $\pm\Delta i_L(t)$, depending on the sub-period
6) Change in flying capacitor voltage, (11), where dt is the length of time of the sub-period (area under the capacitor current curve)

$$\Delta V_{C,k}(t) = \frac{1}{C_{fly,k}} \int i_{C,k} dt \tag{11}$$

7) Change in output capacitor voltage, (12), where dt is the length of time of the sub-period (area under the capacitor current curve)

$$\Delta V_{Cout}(t) = \frac{1}{C_{out}} \int (i_L - I_{out}) dt \tag{12}$$

8) Updated capacitor voltages:

$$V_{C,k}(t) = V_{C,k}(t-1) + \Delta V_{C,k}(t) \tag{13}$$

$$V_{Cout}(t) = V_{Cout}(t-1) + \Delta V_{Cout}(t) \tag{14}$$

Once a complete switching cycle has been calculated, the differences between the calculated voltages on the flying capacitors and the goal voltages (of N_1 level) are calculated and this process is repeated for the number of cycles determined by γ. The peak current during active balancing is then checked against the maximum allowed current based on the output capacitor voltage ripple. If the peak current that occurs during active balancing violates the maximum current limit or the maximum current ripple limit, then the $\alpha - \gamma$ pair is deemed invalid and no further calculations are done with this pair. Next, for any valid combination, the Euclidean norm for the flying capacitor voltage differences is calculated based on (15). The α-γ value-pair with the minimum deviation, or minimum Euclidean norm, is the combination that will correspond to the shortest settling time since the flying capacitor voltages are the closest to the goal at the end of the active balancing stage. This process is repeated for several randomly selected α-γ value pairs as part of the Monte Carlo analysis and then for a specific load current, the value-pair corresponding to the lowest norm is selected.

$$||V_c||_2 = \sqrt{\Delta V_{c1}^2 + \Delta V_{c3}^2} \tag{15}$$

REFERENCES

[1] T. Meynard and H. Foch, "Multi-Level Conversion: High Voltage Choppers and Voltage-Source Inverters," in *Power Electronics Specialists Conference, 1992. PESC '92 Record., 23rd Annual IEEE*, Jun 1992, pp. 397–403 vol.1.

[2] J.-S. Lai and F. Z. Peng, "Multilevel Converters-A New Breed of Power Converters," in *Industry Applications Conference, 1995. Thirtieth IAS Annual Meeting, IAS '95., Conference Record of the 1995 IEEE*, vol. 3, Oct 1995, pp. 2348–2356 vol.3.

[3] F. Z. Peng, "A Generalized Multilevel Inverter Topology with Self Voltage Balancing," *Industry Applications, IEEE Transactions on*, vol. 37, no. 2, pp. 611–618, Mar 2001.

[4] T. Modeer, Y. Lei, and R. C. N. Pilawa-Podgurski, "An analytical method for evaluating the power density of multilevel converters," in *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2016.

[5] Y. Lei, C. Barth, S. Qin, W. c. Liu, I. Moon, A. Stillwell, D. Chou, T. Foulkes, Z. Ye, Z. Liao, and R. C. N. Pilawa-Podgurski, "A 2 kW, Single-Phase, 7-Level, GaN Inverter with an Active Energy Buffer Achieving 216 W/in3 Power Density and 97.6% Peak Efficiency," *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8570–8581, 2017.

[6] J. S. Rentmeister and J. T. Stauth, "A 48V:2V Flying Capacitor Multilevel Converter Using Current-Limit Control for Flying Capacitor Balance," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2017, pp. 367–372.

[7] Y. Lei, W. Liu, and R. C. N. Pilawa-Podgurski, "An Analytical Method to Evaluate Flying Capacitor Multilevel Converters and Hybrid Switched-Capacitor Converters for Large Voltage Conversion Ratios," in *2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2015, pp. 1–7.

[8] D. Chou, Y. Lei, and R. C. N. Pilawa-Podgurski, "A Zero-Voltage Switching, Physically Flexible Multilevel GaN DC-DC Converter," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct 2017, pp. 3433–3439.

[9] A. Stillwell, M. E. Blackwell, and R. C. N. Pilawa-Podgurski, "Design of a 1 kV Bidirectional DC-DC Converter with 650 V GaN Transistor," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2018, pp. 1155–1162.

[10] N. Vukadinović, A. Prodić, B. A. Miwa, C. B. Arnold, and M. W. Baker, "Ripple Minimizing Digital Controller for Flying Capacitor dc-dc Converters Based on Dynamic Mode Levels Switching," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar 2017, pp. 1090–1096.

[11] M. E. Blackwell, A. Stillwell, and R. C. N. Pilawa-Podgurski, "Dynamic Level Selection for Full Range ZVS in Flying Capacitor Multi-Level Converters," in *2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL)*, June 2018, pp. 1–8.

[12] C. P. Henze, H. C. Martin, and D. W. Parsley, "Zero-Voltage Switching in High Frequency Power Converters Using Pulse Width Modulation," in *Proc. 1988. Third Annual IEEE Applied Power Electronics Conf and Exposition APEC '88*, 1988, pp. 33–40.

[13] Y. Naeimi and A. Huang, "Design and Optimization of High Conversion Ratio Quasi Square Wave Buck Converters," in *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Oct. 2017, pp. 148–152.

[14] M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar, "ZVS of Power MOSFETs Revisited," *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8063–8067, 2016.

[15] Z. Ye, Y. Lei, and R. C. N. Pilawa-Podgurski, "A 48-to-12 V Cascaded Resonant Switched-Capacitor Converter for Data Centers with 99% Peak Efficiency and 2500 W/in3 Power Density," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 13–18.

[16] B.-Y. Chen and Y.-S. Lai, "Switching Control Technique of Phase-Shift-Controlled Full-Bridge Converter to Improve Efficiency Under Light-Load and Standby Conditions Without Additional Auxiliary Components," *IEEE Transactions on Power Electronics*, vol. 25, no. 4, pp. 1001–1012, 2010.

[17] J.-W. Kim, D.-Y. Kim, C.-E. Kim, and G.-W. Moon, "A Simple Switching Control Technique for Improving Light Load Efficiency in a Phase-Shifted Full-Bridge Converter with a Server Power System," *IEEE Transactions on Power Electronics*, vol. 29, no. 4, pp. 1562–1566, 2014.

[18] N. Vukadinovic, A. Prodic, B. A. Miwa, C. B. Arnold, and M. W. Baker, "Discontinuous Conduction Mode of Multi-Level Flying Capacitor DC-DC Converters and Light-Load Digital Controller," in *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2017, pp. 1–7.

[19] X. Zhou, M. Donati, L. Amoroso, and F. Lee, "Improved Light-Load Efficiency for Synchronous Rectifier Voltage Regulator Module," *IEEE Transactions on Power Electronics*, vol. 15, no. 5, pp. 826–834, 2000.

[20] H.-W. Huang, K.-H. Chen, and S.-Y. Kuo, "Dithering Skip Modulation, Width and Dead Time Controllers in Highly Efficient DC-DC Converters for System-On-Chip Applications," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 11, pp. 2451–2465, 2007.

[21] H.-W. Seong, H.-S. Kim, K.-B. Park, G.-W. Moon, and M.-J. Youn, "High Step-Up DC-DC Converters Using Zero-Voltage Switching Boost Integration Technique and Light-Load Frequency Modulation Control," *IEEE Transactions on Power Electronics*, vol. 27, no. 3, pp. 1383–1400, 2012.

[22] A. Stillwell, E. Candan, and R. C. N. Pilawa-Podgurski, "Active Voltage Balancing in Flying Capacitor Multi-Level Converters with Valley Current Detection and Constant Effective Duty Cycle Control," in *IEEE Transactions on Power Electronics*, 2019.

[23] T. Foulkes, T. Modeer, and R. C. N. Pilawa-Podgurski, "Developing a Standardized Method for Measuring and Quantifying Dynamic On-State Resistance Via a Survey of Low Voltage GaN HEMTs," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2018, pp. 2717–2724.

[24] K. Kesarwani and J. T. Stauth, "Resonant and Multi-Mode Operation of Flying Capacitor Multi-Level DC-DC Converters," in *2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL)*, July 2015, pp. 1–8.

[25] R. Wilkinson, T. Meynard, and H. du Toit Mouton, "Natural Balance of Multicell Converters: The General Case," *Power Electronics, IEEE Transactions on*, vol. 21, no. 6, pp. 1658–1666, Nov 2006.

[26] X. Yuan, H. Stemmler, and I. Barbi, "Self-Balancing of the Clamping-Capacitor-Voltages in the Multilevel Capacitor-Clamping-Inverter under Sub-Harmonic PWM Modulation," *Power Electronics, IEEE Transactions on*, vol. 16, no. 2, pp. 256–263, Mar 2001.

[27] A. Ruderman and B. Reznikov, "Five-Level Single-Leg Flying Capacitor Converter Voltage Balance Dynamics Analysis," in *Industrial Electronics, 2009. IECON '09. 35th Annual Conference of IEEE*, Nov 2009, pp. 486–491.

[28] S. Thielemans, A. Ruderman, B. Reznikov, and J. Melkebeek, "Improved Natural Balancing With Modified Phase-Shifted PWM for Single-Leg Five-Level Flying-Capacitor Converters," *IEEE Transactions on Power Electronics*, vol. 27, no. 4, pp. 1658–1667, April 2012.

[29] Z. Ye, Y. Lei, Z. Liao, and R. C. N. Pilawa-Podgurski, "Investigation of Capacitor Voltage Balancing in Practical Implementations of Flying Capacitor Multilevel Converters," in *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, July 2017, pp. 1–7.

[30] G. Gateau, M. Fadel, P. Maussion, R. Bensaid, and T. Meynard, "Multicell Converters: Active Control and Observation of Flying-Capacitor Voltages," *Industrial Electronics, IEEE Transactions on*, vol. 49, no. 5, pp. 998–1008, Oct 2002.

[31] L. Lu, S. M. Ahsanuzzaman, A. Prodic, G. Calabrese, G. Frattini, and M. Granato, "Peak Offsetting Based CPM Controller for Multi-Level Flying Capacitor Converters," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 3102–3107.

[32] Z. Ye, Y. Lei, W. Liu, P. S. Shenoy, and R. . Pilawa-Podgurski, "Improved Bootstrap Methods for Powering Floating Gate Drivers of Flying Capacitor Multilevel Converters and Hybrid Switched-Capacitor Converters," *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 5965–5977, 2020.

[33] K. Abe, K. Nishijima, K. Harada, T. Nakano, T. Nabeshima, and T. Sato, "A Novel Three-Phase Buck Converter with Bootstrap Driver Circuit," in *Power Electronics Specialists Conference*, Jun. 2007, pp. 1864–1871.

Margaret E. Blackwell (Student Member, IEEE) received the B.S. degree in electrical engineering from Texas A&M University, College Station, TX, USA in 2017 and the M.S. degree in electrical engineering and computer sciences in 2019 from the University of California, Berkeley, CA, USA, where she is currently working toward the Ph.D. degree in electrical engineering. Her current research interests include hybrid switched-capacitor circuits focusing on the modeling and implementation of resonance operation, soft-switching techniques, and EMI mitigation strategies. Ms. Blackwell was the recipient of the IEEE Workshop on Control and Modeling of Power Electronics Best Paper Award, in 2018 and is a 2019 NSF Graduate Research Fellow.

Andrew Stillwell (Member, IEEE) received dual B.S. degrees in Electrical Engineering and Computer Engineering from University of Missouri, Columbia, MO in 2005. He spent seven years at National Instruments before arriving at the University of Illinois at Urbana-Champaign where he received M.S. and Ph.D degrees in electrical and computer engineering in 2015 and 2019 respectively. He is currently an Assistant Professor in the Electrical and Computer Engineering Department with the University of Illinois at Urbana-Champaign. His research interests include renewable energy applications, hybrid switched-capacitor converters, power electronics design optimization, high-density and high-efficiency power converters, and advanced control techniques for multilevel converters.

Robert C. N. Pilawa-Podgurski (S'06M'11SM'19) was born in Hedemora, Sweden. He is currently an Associate Professor in the Electrical Engineering and Computer Sciences Department at the University of California, Berkeley. Previously, he was an Associate Professor in Electrical and Computer Engineering at the University of Illinois Urbana-Champaign. He received his B.S., M.Eng., and Ph.D. degrees from MIT in 2005, 2007, and 2012, respectively. He performs research in the area of power electronics, and enjoys chocolate. His research interests include renewable energy applications, electric vehicles, CMOS power management, high density and high efficiency power converters, datacenter power delivery, and advanced control of power converters.

Dr. Pilawa-Podgurski served as the Student Activities Chair for IEEE Energy Conversion Congress and Exposition 2016 and 2017, and as the Technical Co-Chair for the 4th IEEE Workshop on Wide Bandgap Power Devices and Applications, 2016. Since 2014, he has served the PELS Technical Committee 6Emerging Power Electronics Technologies as Awards Chair, Secretary, Vice Chair, and (presently) Chair. From 2016-2019 he served as Chair of PELS Technical Committee 2Power Conversion Systems and Components. From 2014-2019, he served as Associate Editor for IEEE Transactions on Power Electronics, and for IEEE Journal of Emerging and Selected Topics in Power Electronics. Since 2018, he has been a member of the ISSCC Power Management Committee.

Dr. Pilawa-Podgurski received the Chorafas Award for outstanding MIT EECS Masters thesis, the Google Faculty Research Award in 2013, and the 2014 Richard M. Bass Outstanding Young Power Electronics Engineer Award of the IEEE Power Electronics Society, given annually to one individual for outstanding contributions to the field of power electronics before the age of 35. In 2015, he received the Air Force Office of Scientific Research Young Investigator Award, the UIUC Deans Award for Excellence in Research in 2016, the UIUC Campus Distinguished Promotion Award in 2017, and the UIUC ECE Ronald W. Pratt Faculty Outstanding Teaching Award in 2017. He was the 2018 recipient of the IEEE Education Society Mac E. Van Valkenburg Award given for outstanding contributions to teaching unusually early in ones career. He is co-author of twelve IEEE prize papers.