UNIVERSITY OF CALIFORNIA SAN DIEGO

Active Load Modulation for High Efficiency RF Transmitters

A dissertation submitted in partial satisfaction of the
requirements for the degree Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Voravit Vorapipat

Committee in charge:

Professor Peter M. Asbeck, Chair
Professor Gert Cauwenberghs
Professor William S. Hodgkiss
Professor Patrick P. Mercier
Professor Gabriel M. Rebeiz

2018

The Dissertation of Voravit Vorapipat is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

_____

_____

_____

_____

_____

Chair

University of California San Diego

2018

DEDICATION

To my family.

EPIGRAPH

"If I have seen further it is by standing on the shoulders of giants."

— Isaac Newton

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ACKNOWLEDGEMENTS

I would like to thank my advisor Professor Peter Asbeck for his invaluable guidance and support throughout my graduate studies. His exceptional work ethic and dedication make him the ideal role model for any researcher, and his patience and commitment have been greatly encouraging.

I would also like to thank my thesis committee: Professor Gabriel Rebeiz, Professor Patrick Mercier, Professor Gert Cauwenberghs, and Professor William Hodgkiss for providing valuable feedback and suggestions.

I am very grateful to work with exceptional colleagues and would like to thank them for their invaluable advice and friendship. Special thanks go to my co-author Cooper Levy who always has ingenious ideas and insightful thoughts on circuit design. I would like to thank Jefy Jayamon, Varish Diddi, Narek Rostomyan, Alex Sun and the HSDG group for their support throughout my PhD.

Chapter 2, in full, is a reprint of the material as it appears in Voltage Mode Doherty Power Amplifier in IEEE Journal of Solid-State Circuits, vol. 52, no. 5, pp. 1295-1304, May 2017. V. Vorapipat, C. S. Levy and P. M. Asbeck. The dissertation author was the primary investigator and author of this paper.

Chapter 3, in full, is a reprint of the material as it appears in A Class-G Voltage-Mode Doherty Power Amplifier in IEEE Journal of Solid-State Circuits, vol. 52, no. 12, pp. 3348-3360, Dec. 2017. V. Vorapipat, C. S. Levy and P. M. Asbeck. The dissertation author was the primary investigator and author of this paper.

Voravit Vorapipat

La Jolla, CA

May 2018

VITA

EDUCATION

2012	Bachelor of Science, Physics, University of Virginia, Charlottesville, Virginia
2014	Master of Science, Electrical and Computer Engineering, University of California San Diego
2018	Doctor of Philosophy, Electrical Engineering (Electronic Circuits and Systems), University of California San Diego

PUBLICATIONS

V. Vorapipat, C. Levy and P. Asbeck, "A wideband voltage mode Doherty power amplifier," 2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), San Francisco, CA, 2016, pp. 266-269.

C. S. Levy, **V. Vorapipat** and J. F. Buckwalter, "A 14-GHz, 22-dBm Series Doherty Power Amplifier in 45-nm CMOS SOI," 2016 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), Austin, TX, 2016, pp. 1-4.

V. Vorapipat, C. S. Levy and P. M. Asbeck, "Voltage Mode Doherty Power Amplifier," in IEEE Journal of Solid-State Circuits, vol. 52, no. 5, pp. 1295-1304, May 2017.

V. Vorapipat, C. Levy and P. Asbeck, "2.8 A Class-G voltage-mode Doherty power amplifier," 2017 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, 2017, pp. 46-47.

V. Vorapipat, C. S. Levy and P. M. Asbeck, "A Class-G Voltage-Mode Doherty Power Amplifier," in IEEE Journal of Solid-State Circuits, vol. 52, no. 12, pp. 3348-3360, Dec. 2017.

ABSTRACT OF THE DISSERTATION

Active Load Modulation for High Efficiency RF Transmitters

by

Voravit Vorapipat

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California San Diego, 2018

Professor Peter M. Asbeck, Chair

This dissertation focuses on the development of active load-modulation techniques to improve back-off efficiency of power amplifiers (PAs) while maintaining wide bandwidth and high linearity suitable for modern wireless handsets. High back-off efficiency is required because of the use of high spectral efficiency modulation with high peak-to-average power ratio (PAPR), which causes the PA to operate in a back-off condition most of the time, typically reducing the efficiency. The Doherty architecture is a widespread active load modulation technique. A well-known issue for Doherty PAs, however, is limited bandwidth due to the use of frequency-sensitive quarter-wave transmission line or its equivalent as impedance inverter. In this work, the impedance inverter is eliminated by using voltage-source PA building blocks, rather than current-

source PAs used in conventional Doherty PAs. Such idea was shown in Doherty's original paper (1936), however it was long forgotten due to the unavailability of voltage-source PAs. Mainstream Doherty amplifiers are implemented using two current source PAs and an impedance inverter. Recently, advances in CMOS devices and PA architecture have led to a high efficiency, high linearity voltage source PA, a switched capacitor power amplifier (SCPA). In this dissertation, a Doherty PA without impedance inverter, the Voltage-Mode Doherty (VMD), is realized by using SCPA building blocks. The VMD is fabricated in 65nm CMOS and achieves 24dBm saturated power (Psat) with power-added efficiency (PAE) of 45%/34% at 0dB/5.6dB back-off, comparable to the state of the art however with much wider 1dB fractional bandwidth from 750MHz to 1050MHz. With memoryless linearization, the VMD transmits 40MHz 256-QAM 802.11ac modulation with -34.8dB EVM and 22% PAE. Compared to the state of the art, the VMD achieves much better modulation accuracy with similar PAE. The wide bandwidth, high back-off efficiency, and excellent linearity of VMD architecture enable high efficiency RF transmitters for future wideband and high spectral efficiency modulation.

Another issue of commonly used active load modulation techniques is a rather "shallow" back-off efficiency enhancement of about 6dB. Since modern modulation signals have PAPR of about 10dB, achieving deeper back-off enhancement can further improve the overall efficiency. Several hybrid architectures have been demonstrated to have efficiency enhancement beyond 6dB back-off. However, they come at the cost of a mode-switching glitch which occurs when the PA changes configuration. The mode-switching glitch causes increased distortion in the transmitted signal proportional to the modulation bandwidth, thus preventing these PAs to be used with future wideband modulation. The second part of the dissertation combined the class-G SCPA and VMD used in the first part of the dissertation to implement a PA with efficiency enhancement up to 12dB

back-off without mode-switching glitch. The CG-VMD PA is fabricated in 45nm CMOS SOI with integrated balun. At 3.5GHz, it achieved 25.3dBm Psat and 30.4%/25.3%/17.4% PAE at 0/6/12 dB back-off, comparable to the state of the art with much wider bandwidth of 1GHz. With memoryless linearization, the PA achieved 19.2% PAE with −35.8dB EVM while transmitting a 40MHz 256QAM 10.1dB PAPR 802.11ac modulation. The excellent achieved EVM is superior to what is achieved in current state of the art hybrid architecture due to the absence of mode-switching glitch.

The third part of the dissertation investigates the distortion caused by the mode-switching glitch in dynamic reconfiguration PAs, and compares it to the glitch-free technique developed in this dissertation. The PA described above provides sufficient flexibility that with software control it can be used to create a mode-switching discontinuity in the same way as the power-combined transformer reconfiguration architecture used in several recent high efficiency PA reports. The measured results show a significant glitch in the signal envelope when the mode-switching occurs, causing both in-band and out-of-band distortion. A correction technique was developed to partially correct the distortion caused by the glitch. It is shown, however, that the in-band distortion can be corrected at the cost of increased out-of-band distortion. With optimal operation of the PA demonstrated in the dissertation, no glitch is observed in the signal envelope, and in-band and out-of-band distortion are much improved. This result quantitatively demonstrates the benefits of the VMD and CG-VMD glitch-free architectures for future wideband high spectral efficiency modulation.

Chapter 1
Introduction

The growing popularity of smartphones in the last decade has caused an explosion of demands on mobile data traffic. In 2016, the yearly data traffic was over 100 Exabytes, and is expected to grow by more than 40% annually [1]. To keep up with the high data rate demands, high spectral efficiency modulations are now widely used [2]. Such modulations have high peak-to-average power ratio (PAPR) which causes the PA to operate mostly in its back-off region. This leads to poor overall efficiency of the RF transmitter, as the traditional PA has low efficiency at back-off.

In high-efficiency, linear PAs such as class-B amplifiers, the efficiency goes down by half for every 6dB back-off in output power. When transmitting a signal with high PAPR, for example 12dB, an ideal class-B PA with 78% peak efficiency would have average efficiency of only about 20% (and in practice it is significantly lower for real class-B amplifiers). Several techniques have been developed [3-5] to improved peak efficiency of the PA and ideally can make the peak efficiency reach 100%. Even in such case, the overall PA efficiency would have been only 25% when transmitting 12dB PAPR modulation which is quite disappointing even in theory.

1.1 Back-Off Efficiency Degradation

The PA efficiency degradation at back-off power is due to "excess" supply voltage when the PA is transmitting at back-off. When the PA operates at saturation, the supply voltage is just enough for the PA to operate without clipping. As the power is backed-off, the voltage swing at the drain of the transistor reduced, and it is possible to reduce the power supply voltage without clipping the output signal. In a class-B PA at a given output power, the DC current is independent of the supply voltage as long as we do not clip the signal. This implies that we can reduce the PA power consumption at back-off by reducing the power supply by up to the excess voltage. Conversely, we can conclude that the degradation in PA efficiency in back-off is due to the excess voltage headroom of the PA. This leads to development of several efficiency enhancement techniques which try to minimize the excess voltage headroom of the PA when operating at back-off. Several efficiency enhancement techniques such as power supply modulation and load impedance modulation will be discussed in this introduction as the background for the dissertation.

1.2 Previous Works

1.2.1 Power Supply Modulation

The most straightforward way to minimize the excess voltage headroom at back-off and thus improve back-off efficiency is to continuously decrease power supply voltage as the power is backed-off. This technique is known as envelope tracking (ET) [6] since the power supply tracks the instantaneous power of the envelope of the transmit signal. In ET, the power supply of the PA is modulated by a high efficiency power supply modulator as the instantaneous output power

changes; several works [6-8] have shown significant efficiency enhancements. The challenge of ET is the design of high efficiency, wideband power supply modulators, which limits overall modulation bandwidth [8].

A simpler way to implement supply modulation is to use a few discrete power supplies and switch the levels using switches (class-G). Due to the glitch incurred at supply voltage transitions, most implementations are only used for average power tracking (APT) [9] which does not improve PA efficiency when transmitting high PAPR modulation. Recently, however, several works [12, 24] have used this technique for dynamic discrete supply voltage modulation which dynamically switches the power supply following the modulation envelope of the transmit signal, achieving efficiency enhancement similar to ET for modulated signals. However, the increased distortion due to the power supply switching glitch which has been reported in [28] warrants a further study of the feasibility of this architecture for wide modulation bandwidth signals.

1.2.2 Load Modulation

Another approach for improving back-off efficiency is to increase the load impedance of the PA at back-off power. By increasing the load impedance of the PA, the voltage swing at the drain of the transistor increases, reducing the excess voltage headroom and thereby improving the efficiency. One of the simplest ideas, referred to as Dynamic Load Modulation, is to reconfigure the matching network to present higher impedance load as the PA is backed-off. In [10], a varactor is used to modulate the load impedance as the PA is backed-off, and significant efficiency improvement is achieved. The limitation of this approach is the limited modulation bandwidth of matching network reconfiguration; significant research for improving the speed is needed for this method to become feasible.

A practical way to achieve load modulation is to have two or more PAs modulate each other's load impedance through a power combiner network, the Active Load Modulation; two well-known techniques are Outphasing and Doherty.

1.2.2.1 Outphasing PA

The idea of Outphasing PA [11] is to create amplitude modulation using two saturated constant envelope PAs and a combiner. The output amplitude of the Outphasing PA depends on the relative angle between the two PA signals, which follows $\cos(\varphi/2)$, where φ is the phase angle between the two signals. Since the two PAs always operate in saturation with no excess voltage headroom regardless of output power, high back-off efficiency can be achieved. The efficiency of the Outphasing PA is highly dependent on the type of combiner used. For high accuracy applications, the isolated combiner is used. In this architecture, the PAs see constant load impedance and thus consume constant power, and efficiency is class-A like. This type of combiner must be used in combination with another technique to realize efficiency enhancement. For example, in the asymmetric multi-level outphasing PA [12], the outphasing PAs with an isolated combiner are used in conjunction with multi-level discrete supply modulation to realize back-off efficiency enhancement.

For better back-off efficiency, a lossless non-isolated combiner can be used. It can be shown that with a non-isolated combiner, an efficiency roll-off like that of a class-B PA due to non-unity power factor of load impedance at back-off [2] can be achieved. To achieve higher efficiency than class-B back-off, the combiner has to compensated, a so-called Chireix combiner [29]. This compensation maintains high power factor of the load presented to the PA resulting in high back-off efficiency. Several works [14-15] have demonstrated Outphasing with a Chireix

combiner. The main limitation of Outphasing is its limited dynamic range [15], since the output power is very sensitive to the relative phase of the two signals at low output power (since they must accurately cancel one another). Moreover, the Chireix combiner is inherently narrowband as it relies on matched positive and negative reactance compensation at each PA.

1.2.2.2 Doherty PA

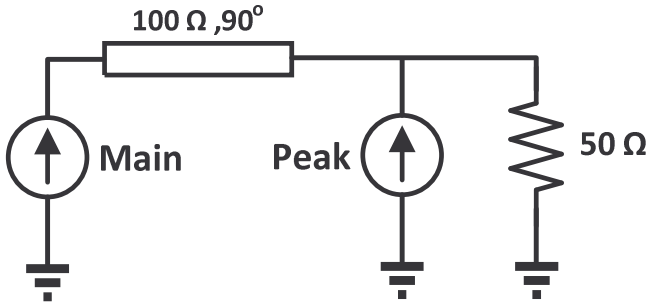


Figure 1.1 : Doherty Power Amplifier

The Doherty amplifier [16] is shown in figure 1.1. It is composed of main PA, peaking PA and an impedance inverter. The key element in its operation is the impedance inverter, which increases the impedance presented to the main PA as the peaking PA is backed-off. In the Doherty design, higher impedance is presented to the main PA keeping it in saturation as the output power of the Doherty PA decreases from its peak to 6dB back-off. Since the main PA is kept in saturation while providing majority of the output power, the efficiency remains high up to about 6dB back-off. The load impedance and voltage swing of the main PA and the overall efficiency of Doherty PA are shown in figure 2.2 as a function of output voltage amplitude. A well-known issue for Doherty PA is its limited bandwidth due to the use of frequency sensitive quarter-wave transmission line or its equivalent as an impedance inverter.

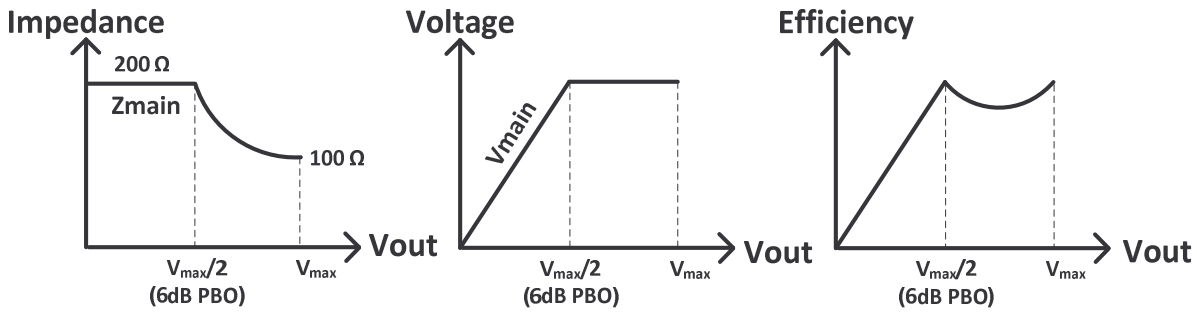


Figure 1.2 : Load Impedance and Voltage Swing of Main PA and Efficiency of Doherty PA

Several works have tried to eliminate the impedance inverter from Doherty amplifier to improve bandwidth. Most of these ended up implementing a lumped element version of the quarter wavelength transmission line [17], others ended up implementing a matching network with 90 degree phase delay [18]. All these works have the same problem; they did not truly eliminate the impedance inverter, and only hide it in other form. This is apparent from the measured results which show wideband peak power and efficiency but very narrowband 6dB efficiency enhancement peaking [19]. A breakthrough in improving the bandwidth [20] of the Doherty amplifier came when an impedance compensation technique similar to that used in the Marchand balun [21] is used to compensate the impedance of the impedance inverter at frequency offsets. Figure 1.3 shows one variant of the impedance compensated Doherty amplifier. The addition of the half-wavelength transmission line at the peaking PA output compensates the load impedance presented to the main PA when the peaking PA is off resulting in a true wideband efficiency enhancement. After extensive research into previous works, the author has become convinced that with main and peaking PA implemented as current source, it is impossible to implement Doherty PA without an impedance inverter.

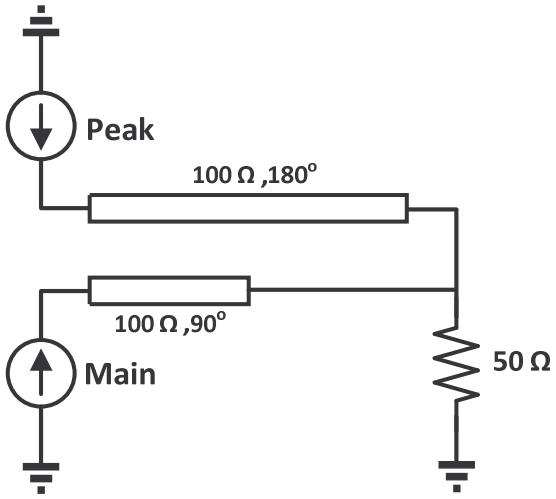


Figure 1.3 : Doherty PA with Impedance Compensation

1.3 Thesis Objective

This dissertation investigates PA design techniques to achieve enhanced efficiency in backoff, and addresses the well-known issues with conventional techniques, as described above, which include bandwidth, back-off efficiency enhancement range and potential mode-switching glitch. This work is a continuation of the improvements of the Doherty PA which has been widely applied in basestations [30] and is a likely candidate for handset PA implementation in the near future. The dissertation first addresses the issue of limited bandwidth of the Doherty PA by fundamentally changing the architecture used to implement the PA. This results in a Voltage Mode Doherty [22] which fundamentally does not require an impedance inverter, resulting in a very wide bandwidth. The dissertation then focuses on the issue of the limited back-off efficiency enhancement range by combining Voltage Mode Doherty [22] and Class-G Switched Capacitor PA [25] in Class-G Voltage Mode Doherty [26], which results in a PA with high back-

off efficiency enhancement range without introducing the mode-switching glitch present in most hybrid architectures [12-13][24]. Lastly, this dissertation discusses the often overlook aspect of efficiency enhancement PA architectures, the mode-switching glitch [28]. The same PA can be used with and without mode switching glitch by exploiting the programmability of the Class-G Voltage Mode Doherty PA, and the results are compared. A brief discussion of each topic is presented in the following.

1.3.1 Voltage Mode Doherty

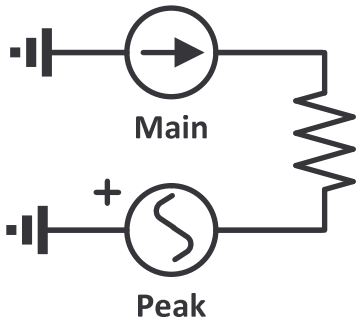


Figure 1.4 : The "forgotten" schematic, Current-Voltage Doherty PA

The first work that showed the concept of a Doherty PA without impedance inverter is, surprisingly, Doherty's own original paper [16], though no real amplifier was implemented that way because there was no high efficiency voltage-source RF PA at that time. This "forgotten" schematic is shown in figure 1.4. The idea is to use a voltage source (peaking PA) to modulate the load of the current source (main PA). The architecture developed in this thesis can be seen to be closely related to this idea. Let us assume for now that we somehow have a voltage source; figure 1.4 will need a little modification for it to work. First, the floating load can be realistically

implemented with a balun driving a single ended load. Second, the implementation of both voltage and current sources makes the design complicated; it turns out that replacing the main PA with a voltage source does not change the effect of active load modulation and thus both main and peaking PA can be implemented as voltage sources. The two changes result in an architecture shown in figure 1.5, the Voltage Mode Doherty discussed in Chapter 2 [22]. The voltage source PA is difficult to implement because traditional PAs are current sources except when they are driven into saturation and the output is heavily clipped. Thanks to advances in CMOS technology and RF digital-to-analog converter (RFDAC) architectures, a high efficiency voltage source PA called the Switched Capacitor Power Amplifier (SCPA) [23] was developed in 2011. Using a modified "forgotten" schematic and SCPA, the Doherty PA without impedance inverter is developed in this work. Implemented in 65nm CMOS, this PA achieved 24dBm saturated power with PAE of 45% at peak power and 34% at 5.6dB back-off over a 750MHz to 1050MHz 1dB bandwidth. To date, this design is the widest fractional bandwidth Doherty PA achieved in CMOS technology. This work was well received at the 2016 RFIC conference where it won the best student paper award.

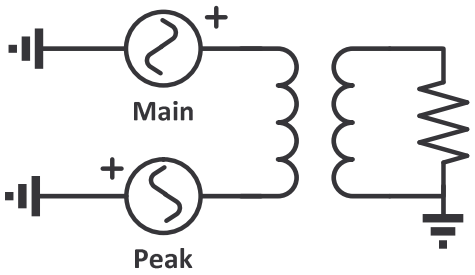


Figure 1.5 : Voltage Mode Doherty PA

1.3.2 Class-G Voltage Mode Doherty

Most modern modulations have PAPR close to 10dB while conventional Doherty and other load modulation techniques have efficiency improvement up to about 6dB, therefore several works [12-13][24] have combined different efficiency techniques to achieve efficiency improvement beyond 6dB back-off. So far, however, all the combined techniques also introduce undesirable "mode-switching" glitches which increase the distortion of the PA. The mode-switching glitch is due to the discontinuous change of PA configuration, such as power supply and load impedance, at critical power levels. In [13] the "skipping window" technique is used to reduce the distortion by skipping some efficiency enhancement mode-transition trading efficiency for lower distortion. It is desirable to have a combined efficiency enhancement technique without introducing mode-switching glitch altogether. The combination of Voltage Mode Doherty [22] and Class-G Switched Capacitor PA [25], is one such combination that provides efficiency improvement up to 12dB back-off and does not have mode-switching glitch. Implemented in 45nm CMOS SOI with an integrated output transformer, this PA achieves 25.3dBm saturated power with 30.4%, 25.3%, and 17.4% PAE at 0, 6, and 12dB back-off at 3.5 GHz, respectively. Due to the absence of the mode-switching glitch, an excellent EVM of -35.8 dB is achieved when transmitting 40 MHz 256-QAM 10.1dB PAPR 802.11ac modulation with 19.2% PAE. The output power and efficiency enhancement are maintained over a 1 GHz bandwidth, which is the widest bandwidth among PAs with efficiency peaking over 10dB back-off.

1.3.3 Mode-Switching Glitch

Techniques such as class-G [9] and power combined transformer-switch [27] have long been effectively used for average power tracking (APT) which makes the glitch at its transition irrelevant. Recently such techniques have been used for real time modulation [12-13][24], though the efficiency enhancement is similar to the well-established technique such as ET, Doherty and Outphasing, one often overlooked issue is the distortion caused by mode-transition glitch. In [28], the glitch in class-G PA is investigated and is shown to increase the distortion both in-band (EVM) and out of band spectrum. However, no direct comparison between glitch and glitch-free configuration with similar efficiency enhancement has been performed. This dissertation compares the same PA configured as glitch and glitch-free configuration with similar efficiency enhancement by exploiting the programmability of the Class-G Voltage Mode Doherty [26]. The measurement result demonstrates the advantage of the glitch-free architectures of Voltage Mode Doherty [22] and Class-G Voltage Mode Doherty [26] implemented in this dissertation.

1.4 Thesis Organization

This dissertation consists of five chapters. The background and fundamental of back-off efficiency enhancement techniques is introduced in this chapter as well as a brief introduction to the topics that will be discuss in subsequent chapters. Chapter 2 will focus on Voltage Mode Doherty PA. Chapter 3 will focus on Class-G Voltage Mode Doherty PA. Chapter 4 will focus on the mode-switching glitch in efficiency enhancement techniques. Chapter 5 concludes the dissertation.

1.5 References

[1] Cerwall, Patrik. Ericsson. Ericsson Mobility Report. Stockholm, Sweden: Ericsson, June 2017.

[2] S. C. Cripps, RF Power Amplifiers for Wireless Communications, 2nd ed. Norwood, MA, USA: Artech House, 2006.

[3] N. O. Sokal and A. D. Sokal, "Class E-A new class of high-efficiency tuned single-ended switching power amplifiers," in IEEE Journal of Solid-State Circuits, vol. 10, no. 3, pp. 168-176, Jun 1975.

[4] F. H. Raab, "Class-F power amplifiers with maximally flat waveforms," in IEEE Transactions on Microwave Theory and Techniques, vol. 45, no. 11, pp. 2007-2012, Nov 1997.

[5] P. Wright, J. Lees, J. Benedikt, P. J. Tasker and S. C. Cripps, "A Methodology for Realizing High Efficiency Class-J in a Linear and Broadband PA," in IEEE Transactions on Microwave Theory and Techniques, vol. 57, no. 12, pp. 3196-3204, Dec. 2009.

[6] Feipeng Wang, A. H. Yang, D. F. Kimball, L. E. Larson and P. M. Asbeck, "Design of wide-bandwidth envelope-tracking power amplifiers for OFDM applications," in IEEE Transactions on Microwave Theory and Techniques, vol. 53, no. 4, pp. 1244-1255, April 2005.

[7] D.F. Kimball, J. Jeong, C. Hsia, P. Draxler, S. Lanfranco, W. Nagy, K. Linthicum, L.E. Larson and P.M. Asbeck, "High-Efficiency Envelope-Tracking W-CDMA Base-Station Amplifier Using GaN HFETs," in IEEE Transactions on Microwave Theory and Techniques, vol. 54, no. 11, pp. 3848-3856, Nov. 2006.

[8] D. Chowdhury, S. R. Mundlapudi and A. Afsahi, "2.2 A fully integrated reconfigurable wideband envelope-tracking SoC for high-bandwidth WLAN applications in a 28nm CMOS technology," 2017 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, 2017, pp. 34-35.

[9] E. Kaymaksut and P. Reynaert, "Dual-Mode CMOS Doherty LTE Power Amplifier With Symmetric Hybrid Transformer," in IEEE Journal of Solid-State Circuits, vol. 50, no. 9, pp. 1974-1987, Sept. 2015.

[10] H. M. Nemati, C. Fager, U. Gustavsson, R. Jos and H. Zirath, "Design of Varactor-Based Tunable Matching Networks for Dynamic Load Modulation of High Power Amplifiers," in IEEE Transactions on Microwave Theory and Techniques, vol. 57, no. 5, pp. 1110-1118, May 2009.

[11] H. Chireix, "High Power Outphasing Modulation," in Proceedings of the Institute of Radio Engineers, vol. 23, no. 11, pp. 1370-1392, Nov. 1935.

[12] P. A. Godoy, S. Chung, T. W. Barton, D. J. Perreault and J. L. Dawson, "A 2.4-GHz, 27-dBm Asymmetric Multilevel Outphasing Power Amplifier in 65-nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 47, no. 10, pp. 2372-2384, Oct. 2012.

[13] Wei Tai, Hongtao Xu, Ashoke Ravi, Hasnain Lakdawala, Ofir Bochobza-Degani, L. Richard Carley and Yorgos Palaskas, "A Transformer-Combined 31.5 dBm Outphasing Power Amplifier in 45 nm LP CMOS With Dynamic Power Control for Back-Off Power Efficiency Enhancement," in IEEE Journal of Solid-State Circuits, vol. 47, no. 7, pp. 1646-1658, July 2012.

[14] I. Hakala, D. K. Choi, L. Gharavi, N. Kajakine, J. Koskela and R. Kaunisto, "A 2.14-GHz Chireix outphasing transmitter," in IEEE Transactions on Microwave Theory and Techniques, vol. 53, no. 6, pp. 2129-2138, June 2005.

[15] Jawad H. Qureshi, Marco J. Pelk, Mauro Marchetti, W. C. Edmund Neo, John R. Gajadharsing, Mark P. van der Heijden and L. C. N. de Vreede, "A 90-W Peak Power GaN Outphasing Amplifier With Optimum Input Signal Conditioning," in IEEE Transactions on Microwave Theory and Techniques, vol. 57, no. 8, pp. 1925-1935, Aug. 2009.

[16] W. H. Doherty, "A New High Efficiency Power Amplifier for Modulated Waves," in Proceedings of the Institute of Radio Engineers, vol. 24, no. 9, pp. 1163-1182, Sept. 1936.

[17] S. Hu, S. Kousai, J. S. Park, O. L. Chlieh and H. Wang, "Design of A Transformer-Based Reconfigurable Digital Polar Doherty Power Amplifier Fully Integrated in Bulk CMOS," in IEEE Journal of Solid-State Circuits, vol. 50, no. 5, pp. 1094-1106, May 2015.

[18] D. Kang, D. Kim, Y. Cho, B. Park, J. Kim and B. Kim, "Design of Bandwidth-Enhanced Doherty Power Amplifiers for Handset Applications," in IEEE Transactions on Microwave Theory and Techniques, vol. 59, no. 12, pp. 3474-3483, Dec. 2011.

[19] A. Cidronali, S. Maddio, N. Giovannelli and G. Collodi, "Frequency Analysis and Multiline Implementation of Compensated Impedance Inverter for Wideband Doherty High-Power Amplifier Design," in IEEE Transactions on Microwave Theory and Techniques, vol. 64, no. 5, pp. 1359-1372, May 2016.

[20] A. Grebennikov and S. Bulja, "High-Efficiency Doherty Power Amplifiers: Historical Aspect and Modern Trends," in Proceedings of the IEEE, vol. 100, no. 12, pp. 3190-3219, Dec. 2012.

[21] G. Oltman, "The Compensated Balun," in IEEE Transactions on Microwave Theory and Techniques, vol. 14, no. 3, pp. 112-119, Mar 1966.

[22] V. Vorapipat, C. S. Levy and P. M. Asbeck, "Voltage Mode Doherty Power Amplifier," in IEEE Journal of Solid-State Circuits, vol. 52, no. 5, pp. 1295-1304, May 2017.

[23] S. M. Yoo, J. S. Walling, E. C. Woo, B. Jann and D. J. Allstot, "A Switched-Capacitor RF Power Amplifier," in IEEE Journal of Solid-State Circuits, vol. 46, no. 12, pp. 2977-2987, Dec. 2011.

[24] S. Hu, S. Kousai and H. Wang, "A Broadband Mixed-Signal CMOS Power Amplifier With a Hybrid Class-G Doherty Efficiency Enhancement Technique," in IEEE Journal of Solid-State Circuits, vol. 51, no. 3, pp. 598-613, March 2016.

[25] Sang-Min Yoo, Jeffrey S. Walling, Ofir Degani, Benjamin Jann, Ram Sadhwani, Jacques C. Rudell and David J. Allstot, "A Class-G Switched-Capacitor RF Power Amplifier," in IEEE Journal of Solid-State Circuits, vol. 48, no. 5, pp. 1212-1224, May 2013.

[26] V. Vorapipat, C. S. Levy and P. M. Asbeck, "A Class-G Voltage-Mode Doherty Power Amplifier," in IEEE Journal of Solid-State Circuits, vol. 52, no. 12, pp. 3348-3360, Dec. 2017.

[27] G. Liu, P. Haldi, T. J. K. Liu and A. M. Niknejad, "Fully Integrated CMOS Power Amplifier With Efficiency Enhancement at Power Back-Off," in IEEE Journal of Solid-State Circuits, vol. 43, no. 3, pp. 600-609, March 2008.

[28] S. Sehajpal, S. S. Taylor, D. J. Allstot and J. S. Walling, "Impact of Switching Glitches in Class-G Power Amplifiers," in IEEE Microwave and Wireless Components Letters, vol. 22, no. 6, pp. 282-284, June 2012.

[29] H. Chireix, "High Power Outphasing Modulation," in Proceedings of the Institute of Radio Engineers, vol. 23, no. 11, pp. 1370-1392, Nov. 1935.

[30] R. Pengelly, C. Fager and M. Ozen, "Doherty's Legacy: A History of the Doherty Power Amplifier from 1936 to the Present Day," in IEEE Microwave Magazine, vol. 17, no. 2, pp. 41-58, Feb. 2016.

Chapter 2

Voltage Mode Doherty Power Amplifier

2.1 Introduction

In modern communication systems, the need for high spectral efficiency and wide bandwidth has led to the use of high peak to average power ratio (PAPR) modulation approaches. With these signals, conventional PAs, having only high efficiency at peak power level, are no longer sufficient to maintain high overall efficiency [1]. Moreover, achieving an acceptable bit-error rate for spectrally efficient modulation puts a stringent linearity requirement on the PA. For example, the 802.11ac standard requires overall transmitter error-vector magnitude of better than -32dB when transmitting 256-QAM symbols [2].

Efficiency enhancement techniques such as Envelope Tracking [3], Outphasing [4], and Doherty [5] have been developed to address the back-off efficiency problem. All of these techniques typically require significant memory-based polynomial correction [6] for use with modern wideband standards, limiting up to now their practical use to base stations.

The goal of this work is to achieve wideband high back-off efficiency while maintaining excellent linearity, suitable for modern modulations, using only simple memoryless correction. This work describes a CMOS PA implemented as a Voltage Mode Doherty (VMD) to address the

issues of back-off efficiency enhancement. To meet these goals in CMOS technology, the architecture eliminates the narrowband impedance inverter used in a conventional Doherty PA. In the following, prior work in high efficiency PA architectures is briefly described, followed by a description of the VMD architecture proposed here and its detailed analysis. Experimental implementation and measurement results are then presented.

2.2 Previous Architectures

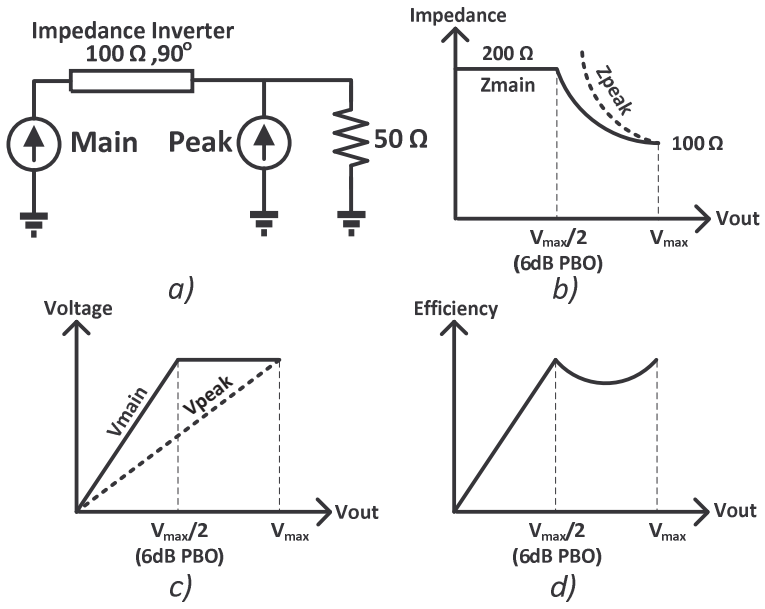


Figure 2.1 : (a) Classical Doherty PA. (b) Impedance seen by main and peaking PAs. (c) Voltage swing at main and peaking PAs. (d) Overall efficiency versus voltage swing at the load.

The classical Doherty PA [5] is composed of main PA, peaking PA and impedance inverter as shown in Fig. 2.1a. At low power, the peaking PA is off, and the impedance inverter presents a high impedance (Fig. 2.1b) to the main PA. This causes it to saturate "early" resulting in an efficiency peak at 6dB back-off (Fig. 2.1c, 2.1d). From 6dB back-off to full power, the peaking PA starts to turn on, and the active load modulation of the peaking PA and impedance inverter

causes the impedance presented to the main PA to decrease (Fig. 2.1b). This allows the main PA to provide more power to the load while it remains in saturation, thus high efficiency is maintained from 6dB PBO to peak power as shown in Fig. 2.1d.

A well-known problem in the classical Doherty PA is its relatively narrow bandwidth. At peak power, the impedance inverter behaves like a through-transmission line and thus does not limit the overall bandwidth of the PA [7]. At 6dB back-off, however, the impedance inverter inverts the impedance from 50 Ohm to 200 Ohm. This significantly limits the bandwidth of the 6dB efficiency peaking [7]. Several techniques [7]-[9] have been shown to improve the bandwidth of impedance inverter. A different approach is taken in this work, eliminating the impedance inverter to improve the overall bandwidth.

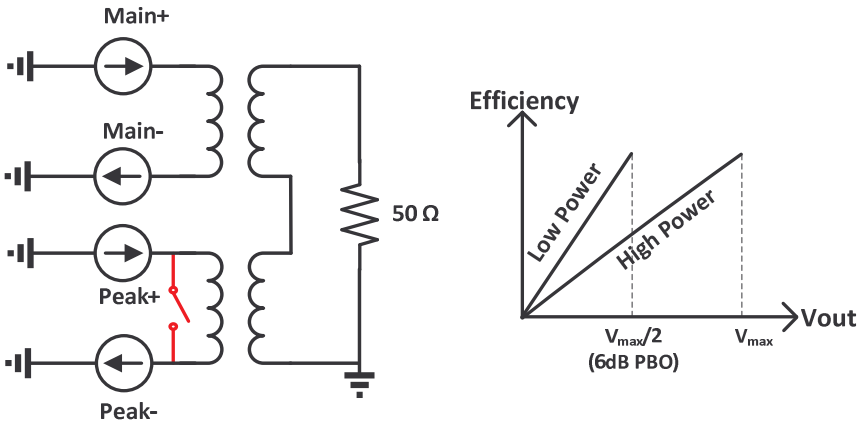


Figure 2.2 : Doherty-like efficiency enhancement using transformers and switch and schematic view of its efficiency enhancement.

A number of alternative Doherty-related PA architectures have been proposed in CMOS to improve back-off efficiency utilizing baluns to perform power combining as well as load modulation. These techniques typically require the use of a large switch (Fig. 2.2) to move from low power to high power [10,19], or a small core inductance in one of the balun transformer's

primaries [11]. A large switch can limit bandwidth and also introduces discontinuities in the DC current of both amplifiers leading to memory effects. A small core inductance will work in place of a switch at low power levels, but forms a low impedance shunt element for the peaking PA, limiting the peak power bandwidth [12].

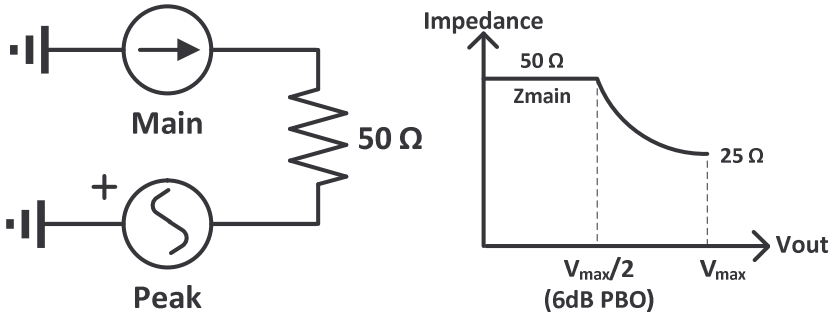


Figure 2.3 : The "forgotten" schematic (Current-Voltage Doherty) and its corresponding load modulation for the main PA

In Doherty's seminal paper [5], he begins by showing that active load modulation between a current source (main PA) and voltage source (peaking PA), in series with a load (Fig. 2.3) can provide back-off efficiency enhancement. We term this architecture the Current-Voltage Doherty. At low power, the voltage source is fixed at 0V, and the current source sees the load impedance directly. When the voltage swing of the current source saturates, the voltage source begins to produce an antiphase voltage with increasing magnitude. This voltage swing on the opposite side of the load allows the current, and hence power, of the current source to continue to increase while its output voltage remains at the saturation level, maintaining high efficiency. This architecture offers two potential benefits over the conventional Doherty PA, particularly in CMOS. Namely, there is no bandwidth-limiting impedance inverter, and the voltages of the two amplifiers are added

in series, allowing for increased output power in scaled technologies without additional impedance matching.

While this architecture achieves the same active load modulation as the classical Doherty PA, a high efficiency RF voltage source was not realizable at the time. Doherty then proceeded to introduce an impedance inverter to allow implementation with only current sources. His initial architecture, however, inspires the VMD architecture which only contains voltage sources as described here.

2.3 Proposed Architecture

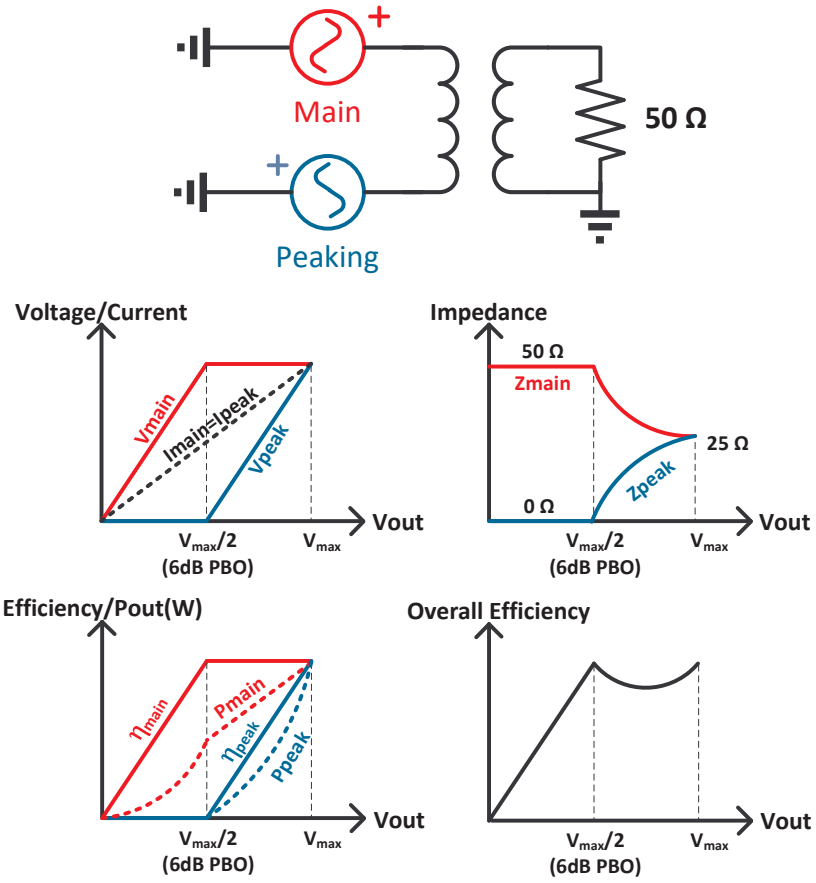


Figure 2.4 : Voltage mode Doherty (VMD) and its corresponding voltage and current trajectories, load impedances and individual efficiencies, and overall efficiency, vs output power.

By replacing the main PA in the Current-Voltage Doherty with another voltage source, we arrive at the VMD architecture which contains only voltage sources. This is shown in Fig. 2.4, where the series load is replaced by a transformer balun driving a single ended load. The principle of operation is as follows: at low power, the peaking PA is off providing a short circuit at the bottom side of the primary of the balun. Under this condition the main PA sees the load impedance, R_L and saturates at 6 dB back-off. The peaking PA is then turned on, driving the balun in antiphase

relative to the main PA and giving $V_{load} = V_m + V_p$ (where V_{load}, V_m and V_p are voltage amplitudes at the fundamental for load, main and peaking PAs), as well as increasing the current through the main PA. While the current provided by the main PA increases due to the peaking PA, the voltage the main PA presents to the balun does not increase, so the impedance seen by the main PA decreases as $R_m = \frac{R_L}{1+\frac{V_p}{V_m}}$. This allows the main PA to provide more power to the load while remaining in saturation, and maintains overall high efficiency from 6dB back-off to peak power. The efficiency vs output power is similar to the classical Doherty PA when Class B back-off is assumed for the voltage-mode PAs.

Since this architecture does not rely on frequency-dependent components to provide active load modulation, the Voltage Mode Doherty has the potential to achieve wide bandwidth, limited by the voltage mode PA and transformer implementation. Moreover, since the output voltage of the voltage mode PA can be precisely controlled all the way to saturation, the turn-on point of the peaking PA for efficiency peaking is well-defined and unchanged across frequency. This is unlike a typical current-mode PA which exhibits compression near saturation of the main amplifier at 6 dB back-off, and at peak power. Additionally, in the classical Doherty, the saturation level is indirectly controlled by current, thus as the impedance seen by main PA changes across frequency, the optimal peaking PA turn-on point and gain also change [13].

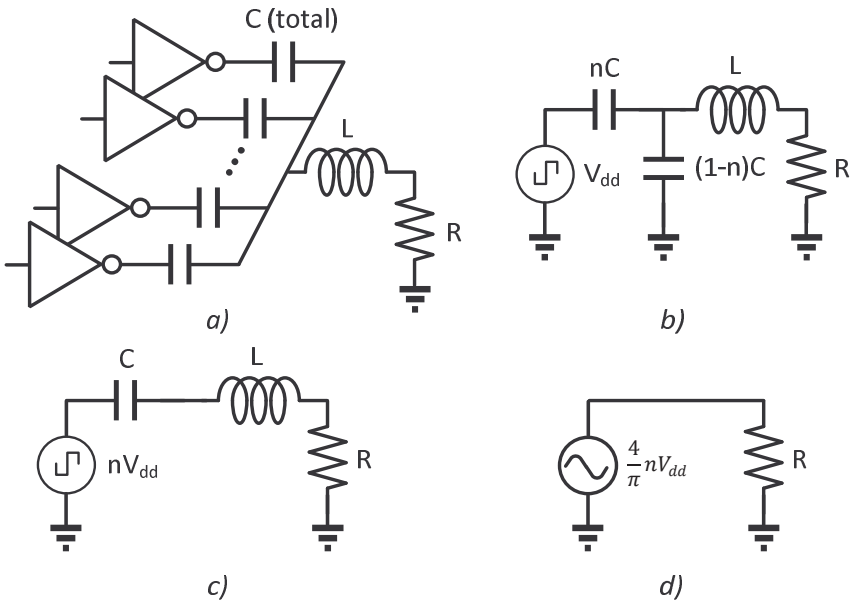


Figure 2.5 : Switched capacitor power amplifier (SCPA) and its equivalent circuit.

The voltage-mode amplifier can be efficiently realized at GHz frequencies with a switched capacitor PA (SCPA) [14]. In a SCPA, the voltage-mode class-D PA (VMCD) is segmented into smaller unit cells, and the output voltage is digitally controlled by turning on a sub-set of the unit cells as shown in Fig. 2.5a.When a unit cell is on, its voltage switches between ground and supply via the low impedance paths of a CMOS inverter. When the unit cell is off, the capacitor is tied to ground via the NMOS transistor of the inverter. If n is the fraction of "on" unit cells, the SCPA circuit can be simplified to a capacitive divider as shown in Fig. 2.5b. The circuit can be further simplified to Fig. 2.5c, which reveals that the impedance looking into the capacitor bank is constant regardless of the state of the SCPA. Resonating out this capacitor bank with a series inductor gives an ideal voltage mode PA at center frequency as shown in Fig. 2.5d.

The loaded quality factor of the series resonator $Q_L = \frac{1}{\omega CR}$ (with C and R defined in Fig. 2.5a) can be designed to be about unity, which provides wide bandwidth, and slightly better than

class B PAE at back-off [14]. Excellent capacitor matching in CMOS technology provides the SCPA architecture with superior linearity [14], making it an ideal choice for voltage sources in a VMD implementation.

2.4 Detailed Analysis

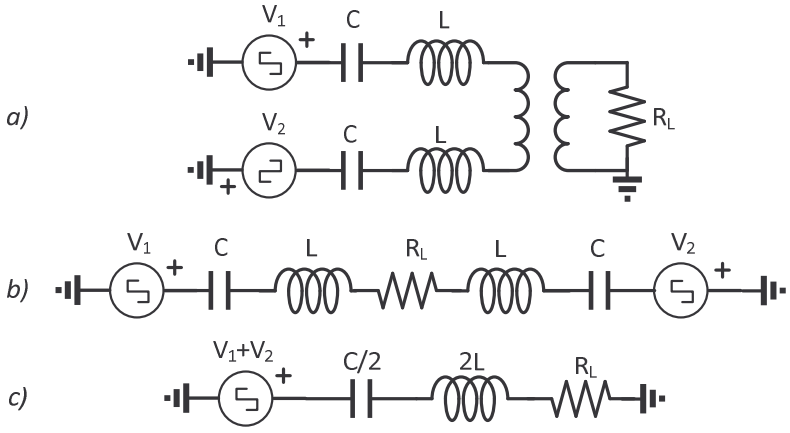


Figure 2.6 : Equivalent circuits of two SCPAs connected across a transformer.

We first present generalized equations for efficiency and output power with arbitrary amplitude for each of the two SCPAs in the structure of Fig. 2.6a. From this, we examine the specific cases of a differential SCPA and a VMD, to demonstrate the back-off efficiency enhancement realized with the VMD.

2.4.1 Generalized Efficiency

We will assume that regardless of amplitude, SCPA1 and SCPA2 operate in anti-phase. The loss due to on-resistance, switching loss of the capacitor bank driver, and matching network insertion loss will be ignored in this section. The output voltage and power can be written as

$$V_{out} = \frac{2}{\pi} V_{dd}(n_1 + n_2)$$

$$P_{out}^{0} = \frac{V_{out}^2}{2R_L} = \frac{2}{\pi^2}\frac{V_{dd}^2}{R_L}(n_1 + n_2)^2$$

where n_1 and n_2 are the fraction of "on" unit cells in SCPA1 and SCPA2 respectively. At the voltage transitions, the inductor in Fig. 2.5b appears as an open circuit due to the fast rising/falling edges of the driver. Thus the capacitance being charge/discharged by each SCPA is $n(1-n)C$ [14]. This gives a capacitive divider loss of $n(1-n)CV_{dd}^2 f$.

Then the overall loss can be written as

$$P_{cd} = P_{cd,1} + P_{cd,2} = [n_1(1-n_1) + n_2(1-n_2)]CV_{dd}^2 f\ ,$$

and the efficiency is

$$\eta = \frac{P_{out}^{0}}{P_{out}^{0} + P_{cd}} = \frac{1}{1 + \frac{P_{cd}}{P_{out}^{0}}} = \frac{1}{1 + \frac{\pi}{2}\frac{1}{Q_L}\frac{n_1(1-n_1) + n_2(1-n_2)}{(n_1+n_2)^2}}\ .$$

Here the term $\omega R_L C$ is replaced by loaded quality factor $Q_L = \frac{1}{\omega R_L \frac{C}{2}}$ of the overall structure as shown in Fig. 2.6c, which is independent of the state (n_1, n_2). Note that the capacitive divider loss relative to the output power is independent of process technology and operating frequency.

The efficiency equation indicates that increasing Q_L reduces the capacitive divider loss in SCPAs resulting in reduced efficiency droop between peak power and 6dB back-off, and better efficiency roll-off beyond 6dB back-off. However, increasing Q_L reduces bandwidth, increases voltage swing in the capacitor bank, and produces higher insertion loss due to finite inductor quality factor. To maintain wideband operation and low insertion loss (if on-chip transformer were to be used) and to reduce voltage stress in the MIM capacitor bank, a low value of Q_L is favored; Q_L is held near 1 in this design.

2.4.2 Back-off Efficiency Enhancement of VMD

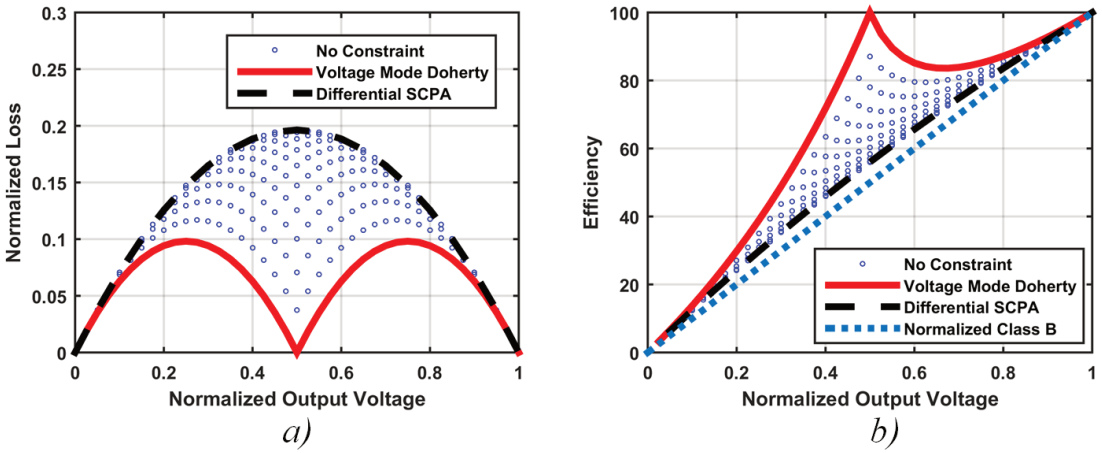


Figure 2.7 : a) Capacitive divider loss normalized to peak output power and b) corresponding efficiency vs normalized output voltage for different choices of amplitude control words (ACW) n_1, n_2 with $Q_L = 1$. Choices corresponding to the differential SCPA and the VMD are shown in bold; additional choices are shown with open circles.

For simple differential operation of the SCPA pair, both SCPAs present the same voltage to the load, and $n_1 = n_2 = n$. The equation above can be readily simplified to yield the efficiency vs output power.

For VMD, the choices of n_1 and n_2 are made to ensure SCPA1 reaches saturation first, at which point SCPA2 turns on (Fig. 2.4). More precisely:

$$n_1 = \begin{cases} 2n & \text{for } n \le 0.5 \\ 1 & \text{for } 0.5 < n < 1 \end{cases} \quad \text{and} \quad n_2 = \begin{cases} 0 & \text{for } n \le 0.5 \\ 2(n-0.5) & \text{for } 0.5 < n < 1 \end{cases}$$

As shown in Fig. 2.7a, the choice of (n_1, n_2) affects the loss in the capacitive dividers. The VMD reduces the peak loss in the capacitive divider by half. We can see that the loss in capacitive divider vanishes at half output voltage, and as shown in Fig. 2.7b, this results in efficiency peaking at 6dB back off, similar to the class-G SCPA architecture [15]. As indicated by the circles of Fig.

2.7, amongst all arbitrary combinations of (n_1, n_2), the VMD provides the lowest capacitive divider loss, and thus the optimum choice of (n_1, n_2) for two SCPAs across a transformer.

2.4.3 Voltage Mode Doherty with Non-ideal Components

At gigahertz frequencies, in addition to the capacitive divider loss of the SCPAs, it is important to consider matching network insertion loss, conduction loss, and switching loss.

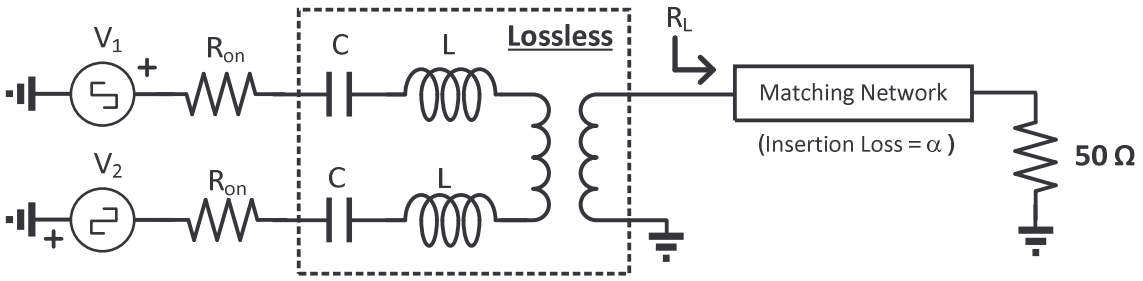


Figure 2.8 : Equivalent circuit used in efficiency analysis. Here the losses of SCPA capacitor bank, inductor and transformer are lumped into the matching network.

The conduction loss can be modelled as the on-resistance of the SCPA drivers, R_{on} (Fig. 2.8). The added resistance reduces the voltage amplitude seen at the input to the matching network by a factor of $\frac{1}{1+\frac{2R_{on}}{R_L}}$, which reduces the power presented to the matching network, relative to ideal driver with $R_{on} = 0\Omega$, to $P'_{out} = \frac{P^0_{out}}{\left(1+\frac{2R_{on}}{R_L}\right)^2}$. However, the conduction loss in the switch is less than the output power reduction, as the addition of R_{on} reduces the current through the switching transistors. Since R_{on} is in series with the load, the power loss in the on-resistance of the SCPA drivers relative to the power delivered to the matching network is $\frac{P_{cond}}{P'_{out}} = \frac{2R_{on}}{R_L}$.

Insertion loss will attenuate the power delivered to the load and can be written as $P_{out} = \alpha P'_{out}$, where α is the insertion loss factor.

The switching loss is due to the charging/discharging of capacitors and crowbar current in SCPA unit cells. This loss can be represented by an equivalent loss capacitance $C_{sw} \equiv \frac{P}{V_{dd}^2 f}$ where P is the power dissipated by the SCPA unit cells including their pre-drivers, when all cells are switching, driving no load, and switching at frequency f. The switching loss can be written as $P_{sw} = C_{sw} V_{dd}^2 f(n_1 + n_2)$, which is proportional to the number of drivers switching, and decreases linearly with output voltage. This allows the VMD to achieve high efficiency at back off.

The conduction loss and switching loss represent a trade-off in the SCPA unit cell design. Since $R_{on} \propto \frac{1}{W}$, and $C_{sw} \propto W$, where W is the effective width of the switching transistors, the product $R_{on} C_{sw}$ is constant. Therefore, we can define the totem pole driver figure of merit $f_{SW} = \frac{1}{2\pi R_{on} C_{sw}}$. Advanced process technologies such as scaled CMOS, circuit topologies (eg. anti-shoot through current) and good layout practice, can all help to improve f_{SW}. With this, we can relate the switching loss to the power delivered to the matching network as $\frac{P_{sw}}{P'_{out}} = \frac{\pi}{2} \frac{f}{f_{sw}} \frac{1}{n_1+n_2} \frac{R_L}{2R_{on}} \left(1 + \frac{2R_{on}}{R_L}\right)^2$. It should be noted that as the output voltage decreases, the relative switching loss increases. This is because even though the switching loss reduces linearly with output voltage $(n_1 + n_2)$, the output power is proportional to the square of output voltage $(n_1 + n_2)^2$. This implies that the efficiency at 6dB back off will always be lower than the efficiency at peak power in this architecture due to a doubling of the relative switching loss. A similar problem (but more pronounced) occurs in Outphasing PAs where the switching loss is constant regardless of output power [16]. In Outphasing, the two switch-mode PAs are fully on regardless of output voltage, resulting in a four-fold increase in relative switching loss at 6dB back-off. In the conventional Doherty PA, the doubling of the main PA load impedance at 6dB back-off and the soft turn-on characteristic of the transistor cause the efficiency to be lower at the 6dB back-off point [21].

We can now write the overall output power and efficiency as

$$P_{out} = \alpha P'_{out} = \frac{\alpha P^0_{out}}{\left(1+\frac{2R_{on}}{R_L}\right)^2} = \frac{\frac{2\alpha V_{dd}^2}{\pi^2 R_L}(n_1+n_2)^2}{\left(1+\frac{2R_{on}}{R_L}\right)^2}$$

$$\eta = \frac{\alpha P'_{out}}{P'_{out}+P_{cond}+P_{sw}+P_{cd}} = \frac{\alpha}{1+\frac{P_{cond}}{P'_{out}}+\frac{P_{sw}}{P'_{out}}+\frac{P_{cd}}{P'_{out}}}$$

where

$$\frac{P_{cd}}{P'_{out}} = \frac{\pi}{2}\frac{1}{Q_{SCPA}}\left(1+\frac{2R_{on}}{R_L}\right)^2 \frac{n_1(1-n_1)+n_2(1-n_2)}{(n_1+n_2)^2}$$

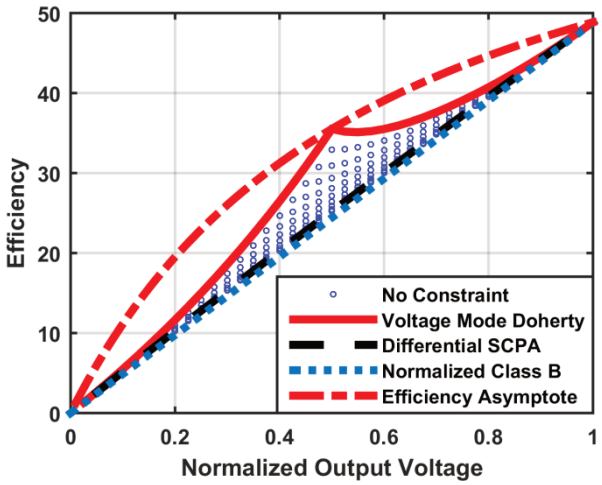


Figure 2.9 : Efficiency vs output voltage for voltage mode Doherty and differential SCPA including non-ideal components ($Q_L = 1, \alpha = 0.9, \frac{2R_{on}}{R_L} = 0.15, f_{SW} = 10$ GHz, $f = 1$ GHz)

Fig. 2.9 illustrates the efficiency versus output voltage of VMD including the non-idealities for a specific set of design parameters. Here we can see that insertion loss, conduction loss, and switching loss form an asymptote of efficiency (dash-dot line), which limits the achievable efficiency at any back-off point. When the capacitive divider loss is included, the efficiency drops

from the asymptote. In the case of VMD, the capacitive divider loss vanishes at 6dB back off causing the efficiency line to touch the asymptote and resulting in back-off efficiency peaking.

2.5 Implementation

2.5.1 Load Modulation Network

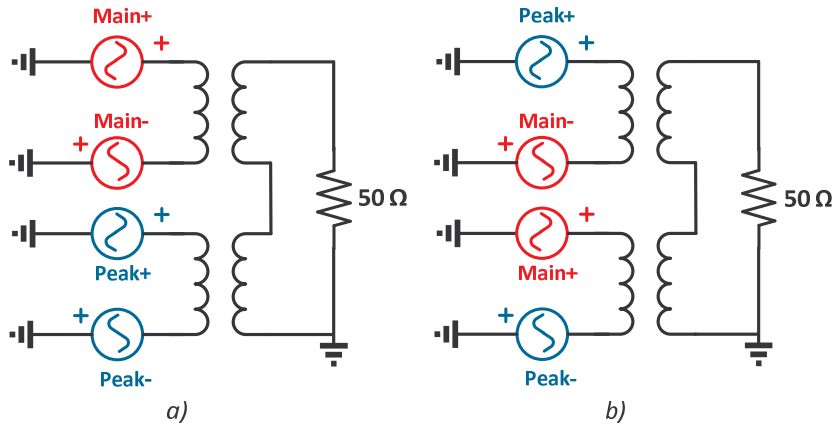


Figure 2.10 : a) Secondary and b) Primary load modulated pseudo-differential voltage mode Doherty

A pseudo-differential architecture is used in this design to mitigate the effect of wirebond inductance on the supply and ground. The virtual ground provides the large fundamental current component, and the remaining even-harmonic ripple is filtered by on-chip decoupling capacitors. Since the VMD architecture needs low impedance looking into the supply network at both baseband and RF, wide RF bandwidth as well as wide modulation bandwidth can be achieved simultaneously with the VMD. This is unlike a conventional current-mode PA where the size of the RF choke presents a trade-off between RF and modulation bandwidth [1].

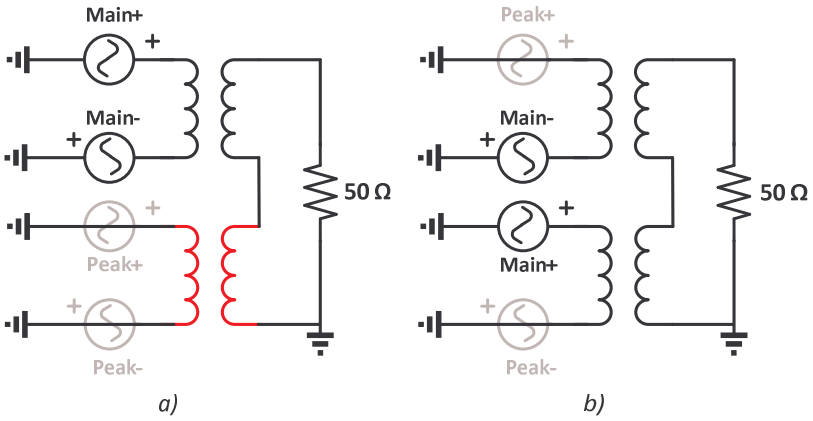


Figure 2.11 : a) Secondary and b) Primary load modulated pseudo-differential voltage mode Doherty operation at 6dB back-off (The parasitic transformer is indicated in red)

Two possible implementations of the VMD utilizing two pseudo-differential SCPAs are shown in Fig. 2.10. The two structures are identical at peak power. However, at 6dB back-off the secondary load modulation architecture (Fig. 2.11a) utilizes only half of the transformer structure (the other half merely provides a short circuit shown in red), while the primary load modulation architecture (Fig. 2.11b) still utilizes the whole structure. Since the primary load modulation architecture fully utilizes the transformer structure at 6dB back-off, it provides low passive loss at any power level [17]. An additional benefit of primary load modulation is that the secondary only provides power combining. This allows flexibility between the choice of series and parallel combining as shown in Fig. 2.12. For ease of experimentation, a lumped-element balun implementation of Fig. 2.12b is used in this design.

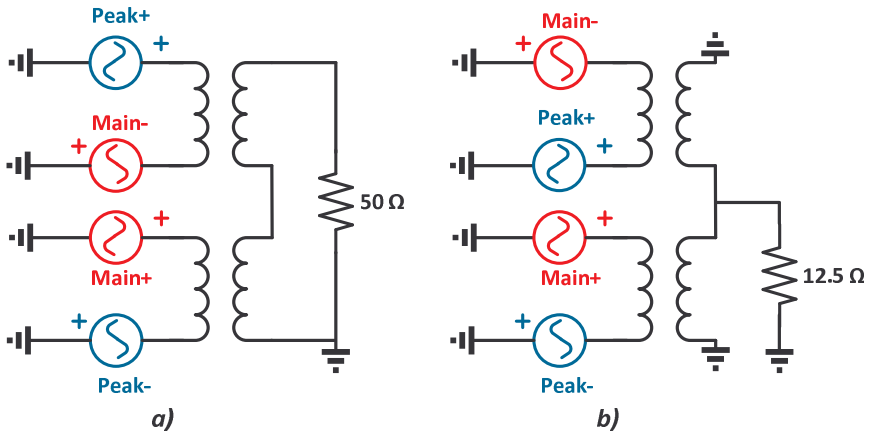


Figure 2.12 : a) Series combined and b) Parallel combined load modulated pseudo-differential voltage mode Doherty (Load is adjusted to provide the same output power)

The lumped-element balun [1] is shown in Fig. 2.13a. It can be shown by superposition (Fig. 2.13b,c) that the voltage at the load is the difference between the two input voltages with 90 degree phase delay, $V_L = -j(V_m + V_p)$, and the load impedance seen by the main PA is $Z_m = \frac{V_m}{I_m} = \frac{V_m}{\frac{V_m}{Z_0}+\frac{V_p}{Z_0}} = \frac{Z_0}{1+\frac{V_p}{V_m}}$. An equivalent representation for the balun, which holds for any load impedance R_L, is shown in Fig. 2.13d.

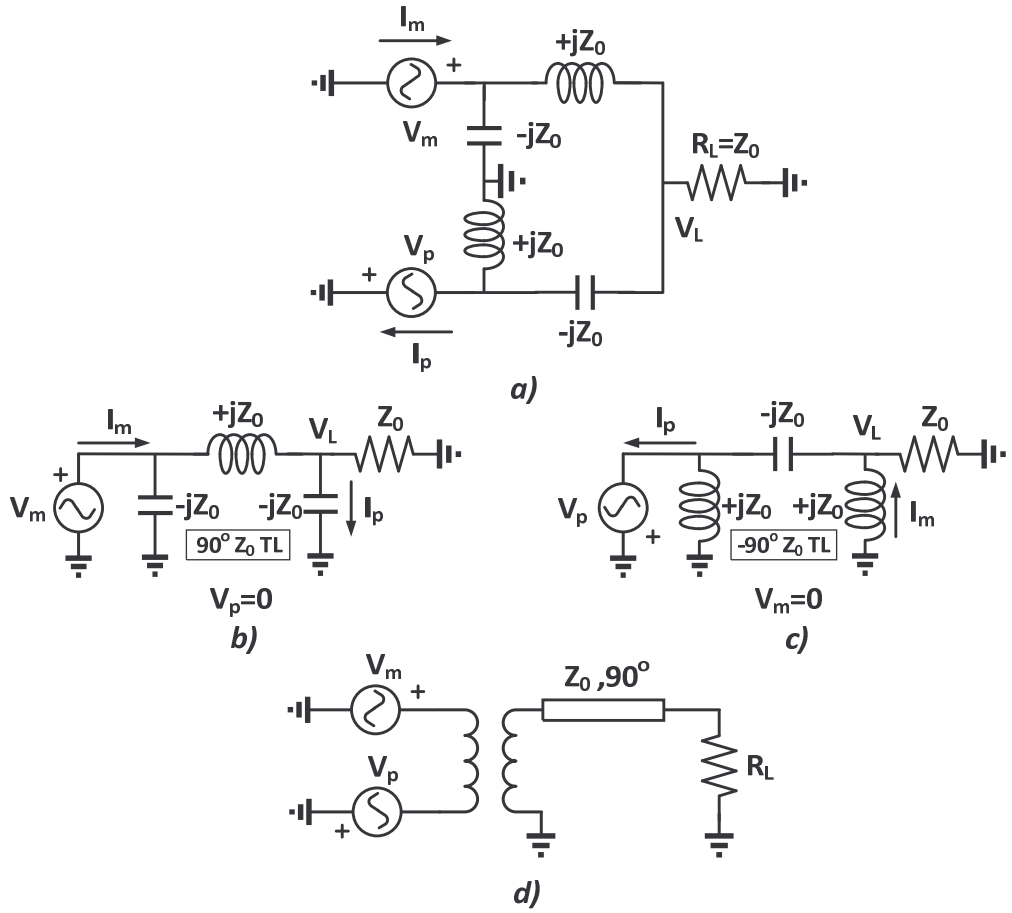


Figure 2.13 : a) Lumped-element balun circuit b) Equivalent circuit when Vp=0 c) Equivalent circuit when Vm=0 d) Overall equivalent circuit

The implemented load modulation network operating at peak power and 6dB back-off is shown in Fig. 2.14. Since the impedance inverter embedded in the balun design can severely limit the bandwidth, the characteristic impedance of each lumped-element balun is designed to be equal to its load impedance (Fig. 2.14) such that the impedance inverter behaves like a through, providing wide bandwidth. In addition to transforming 50Ω to 12.5Ω, the T-network following the baluns also compensates the impedance at frequency offsets from the balun center frequency, further extending the bandwidth.

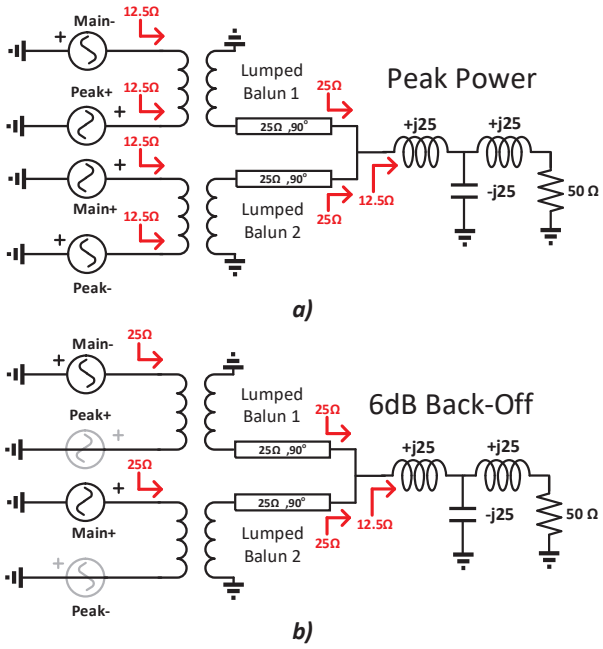


Figure 2.14 : The implemented load modulation network with annotated impedance for operation at a) Peak power and b) 6dB back-off.

2.5.2 Dual Pseudo-Differential SCPA

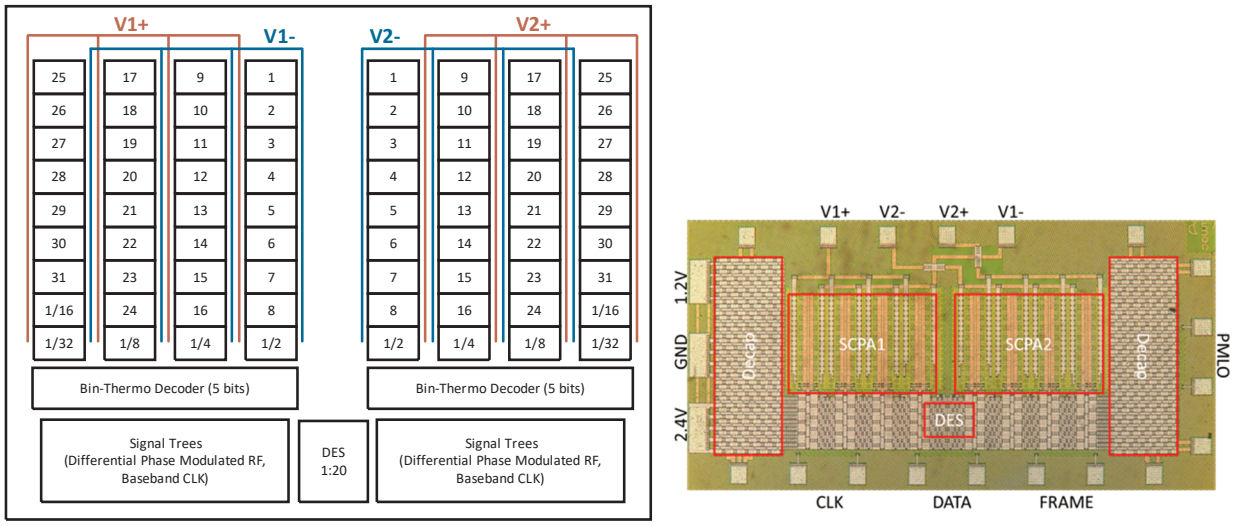


Figure 2.15 : The floor plan and chip micrograph (1.8mm x 0.9mm) for dual pseudo-differential SCPA used in VMD. Integer indicated unary cell turn-on sequence, fraction represent binary cells.

The dual pseudo-differential polar SCPA is implemented in 65 nm bulk CMOS, and the overall floorplan and chip micrograph is shown in Fig. 2.15. The drivers in each side of pseudo-differential SCPA are designed such that at peak power, the drain-source voltage drop over the cascode structure when the transistor is on is about 10% of the supply voltage, keeping the SCPA linear. This gives $R_{on} = 0.1\frac{\pi}{2}12.5\Omega = 1.9\Omega$ for each SCPA. The capacitor bank is designed for $Q_L = 1$, which gives $C = 12.8\text{pF}$ at 1GHz in each side of each pseudo-differential PA. Each SCPA uses a 5-bit unary, 5-bit binary segmented DAC architecture. The unit cell is designed to be pseudo-differential, providing virtual ground locally within the unit cell and minimizing lossy fundamental current flow. The turn-on sequence is as shown in Fig. 2.15, where cells are enabled in increasing numbering as the output voltage increases. The relatively large difference in location between some cells with adjacent numbers, e.g. cells 8 and 9, leads to kinks in the AM-PM characteristic (to be described below, Fig. 2.19), and can be improved with a modified layout in future implementations. The signal distribution trees provide balanced timing for phase-modulated RF and baseband CLK to each column of unit cells.

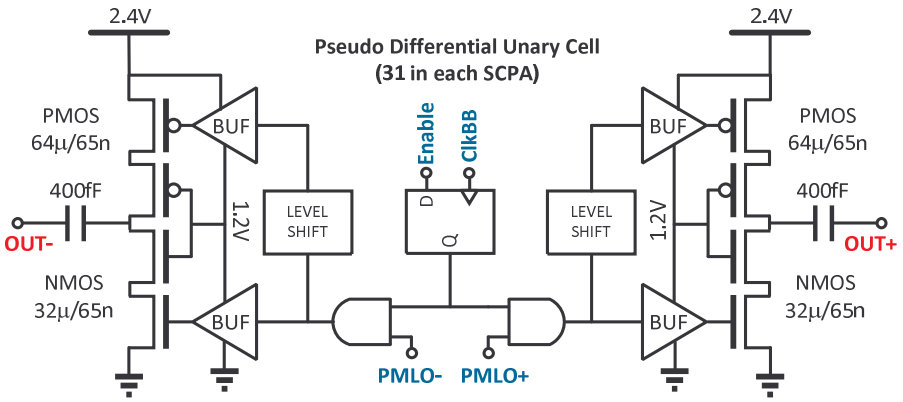


Figure 2.16 : The pseudo-differential SCPA unit cell.

The unit cell is designed with a cascoded switch final stage (Fig. 2.16) to double voltage swing, delivering 6dB higher power to the load. The buffers are designed to have a fan-out of about 4, providing sharp transitions and helping to minimize the crowbar current. The level shift which drives the high side transistor is based on the architecture presented in [18]. The D-Flip-Flop at the unit cell synchronizes the enable signal with the baseband clock providing excellent AM-PM characteristics. The MIM capacitor size is $\frac{12.8\text{pF}}{32} = 400\text{fF}$ for each unary cell, and is scaled down accordingly for binary cells.

2.6 Measurement Setup and Result

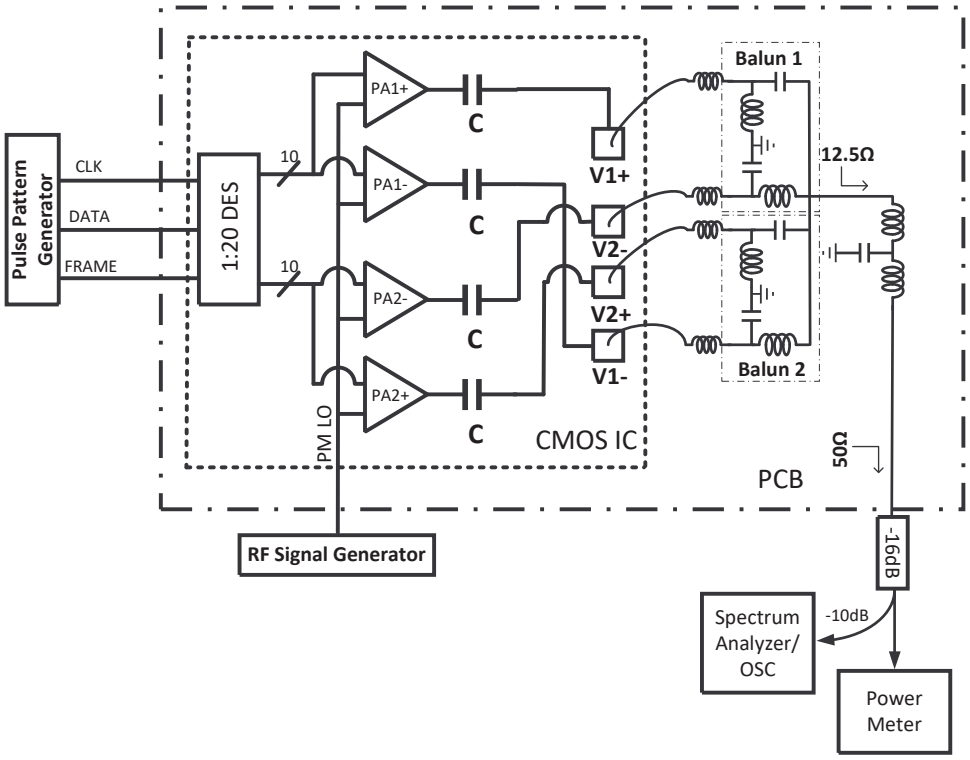


Figure 2.17 : The overall implementation and measurement setup

The measurement setup is shown in Fig. 2.17. It is composed of RF vector signal generator to provide the PM-LO, high-speed serial pulse pattern generator to provide amplitude control word (ACW), spectrum analyzer for spectrum and narrowband EVM measurement (VSA Mode), high speed oscilloscope for wideband EVM measurement, and RF power meter for accurate power measurement. PAE includes all power consumption on-chip, as well as insertion loss of the output load modulation network to the edge of the PCB (50Ω). The external PM-LO and Serial Data/Clk/Frame power is excluded because most of the power is consumed in termination resistors. In an integrated implementation, these will be about the power needed to drive a few minimum size CMOS inverters, which is negligible.

The baseband signal generation and linearization is performed in Matlab with baseband sampling frequency of 360 MHz. Since there is no on-chip interpolation filter [19], digital replicas are expected at multiples of 360 MHz offset.

2.6.1 CW Measurement Result

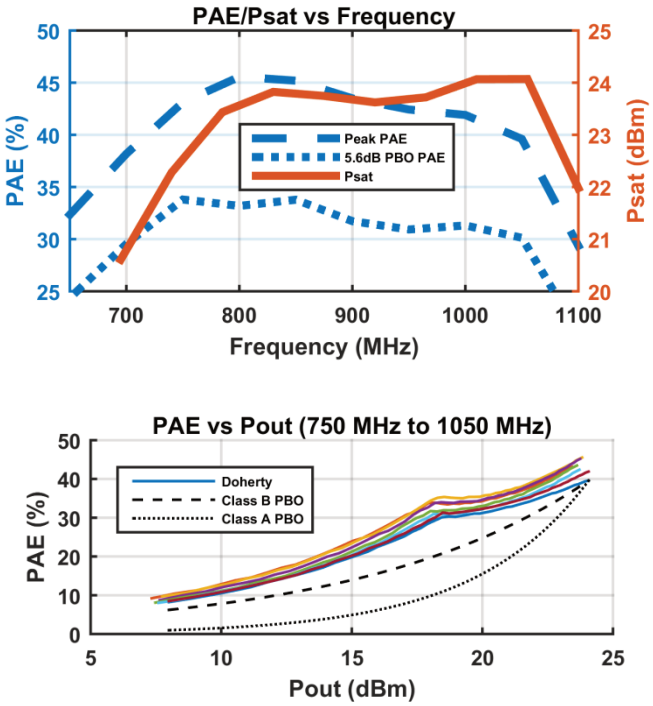


Figure 2.18 : Top: PAE and Psat vs Frequency. Bottom: PAE vs Pout from 750 MHz to 1050 MHz in 50 MHz step.

The CW measurement with standard power supply (1.2/2.4V) is shown in Fig. 2.18, the peak power, peak PAE and 6dB back-off PAE are 24 dBm, 45%, and 34% respectively. With a boosted power supply of 1.5/3V, the measured peak power is 26 dBm with the same PAE; no degradation was observed over laboratory testing time scales. The 1dB Psat bandwidth ranges from 750 MHz to 1050 MHz, a fractional bandwidth over 33%. The efficiency peaking point located around 5.6dB back-off rather than 6dB back-off due to slight increase in the passive network loss.

The efficiency at 6dB back-off is lower than the peak efficiency as expected from efficiency asymptote analysis. At 6dB back-off the relative switching loss $\frac{P_{sw}}{P_{out}}$ doubles similar to the class-G SCPA case [15].

2.6.2 Modulation Measurement

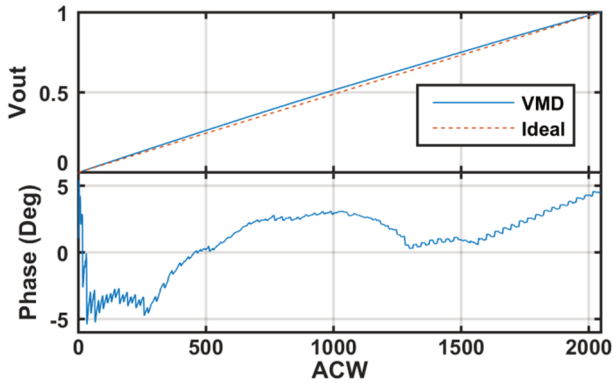
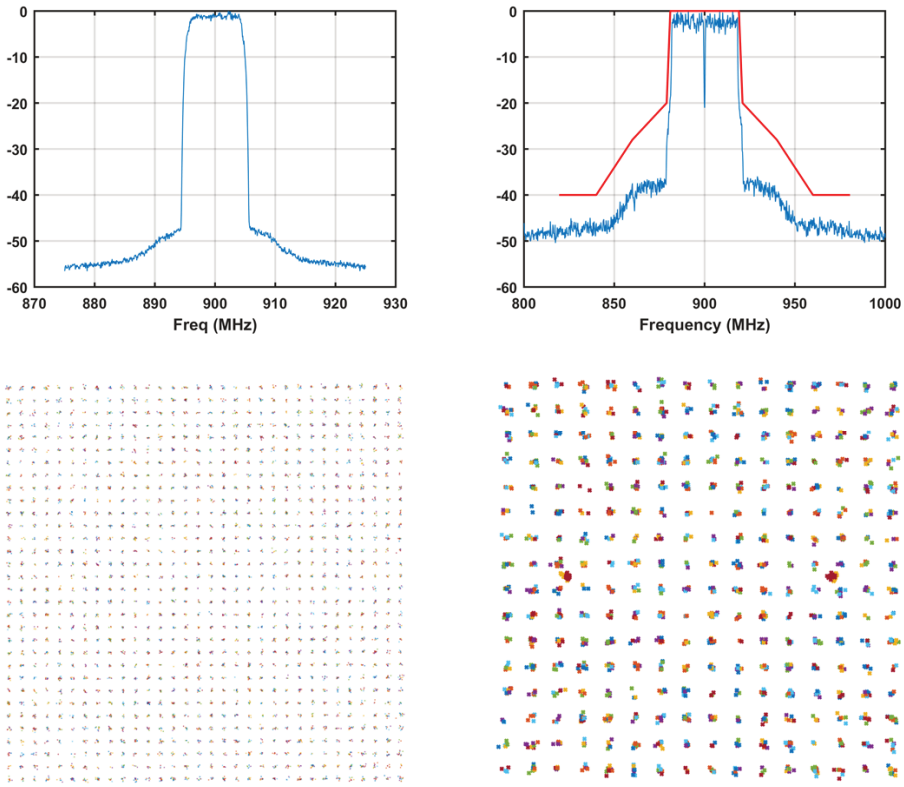


Figure 2.19 : Measured ACW-AM and ACW-PM at 900 MHz

In this measurement, the PA is linearized with a memory-less look-up table (LUT). The LUT was generated using an input signal at 10 kHz, amplitude modulated with 100% modulation index. As shown in Fig. 2.19, the ACW-AM relationship is highly linear even before correction; minor imperfection results from small non-linear on resistance. The ACW-PM relationship appears as a weighted average of ACW-PM behaviors of each SCPA. Its peak-to-peak deviation is comparable to that of a single SCPA, which could be improved with better layout as noted above.

2.6.2.1 Narrowband Modulation

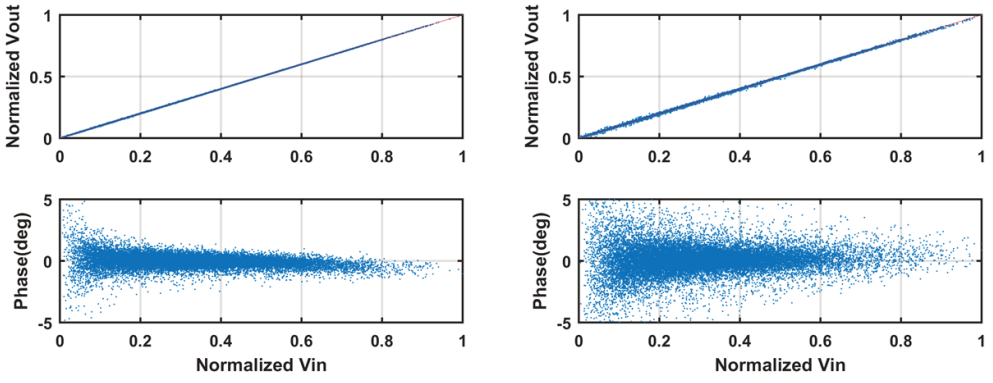


a) *b)*

Figure 2.20 : a) Measured spectrum and constellation of 9 MHz 1024-QAM OFDM modulation. b) Measured spectrum and constellation of 40 MHz 256-QAM 802.11ac modulation.

A 9 MHz 1024-QAM, 32 Carrier OFDM signal hard-clipped to 8.6dB PAPR and centered at 900 MHz is used. The result shows 15.1dBm Pout, 22.9% PAE, -41.2dB EVM and better than 45dBc ACPR (Fig. 2.20a). This demonstrates excellent linearity without the need to back-off the output power (Psat-Pout=PAPR). The dynamic AM-AM and AM-PM (Fig. 2.21a) show minimal memory effects.

2.6.2.2 Wideband Modulation



a) *b)*

Figure 2.21 : The dynamic AM-AM and AM-PM for a) 9 MHz modulation and b) 40 MHz modulation

A 40 MHz 256-QAM 802.11ac modulation (108 Data, 6 Pilot OFDM) hard-clipped to 9dB PAPR is used. The result shows 14.7dBm Pout with 22.0% PAE and -34.8dB EVM, meeting the EVM spec and Tx mask (Fig. 2.20b). No equalization or back-off is required. The dynamic AM-AM and AM-PM (Fig. 2.21b) show moderate amounts of memory effect. This is mainly due to passband P_{sat} ripple and non-ideal baseband supply decoupling. After equalization, the EVM is -36.5dB, very close to the measurement noise floor of -38dB (limited by the oscilloscope).

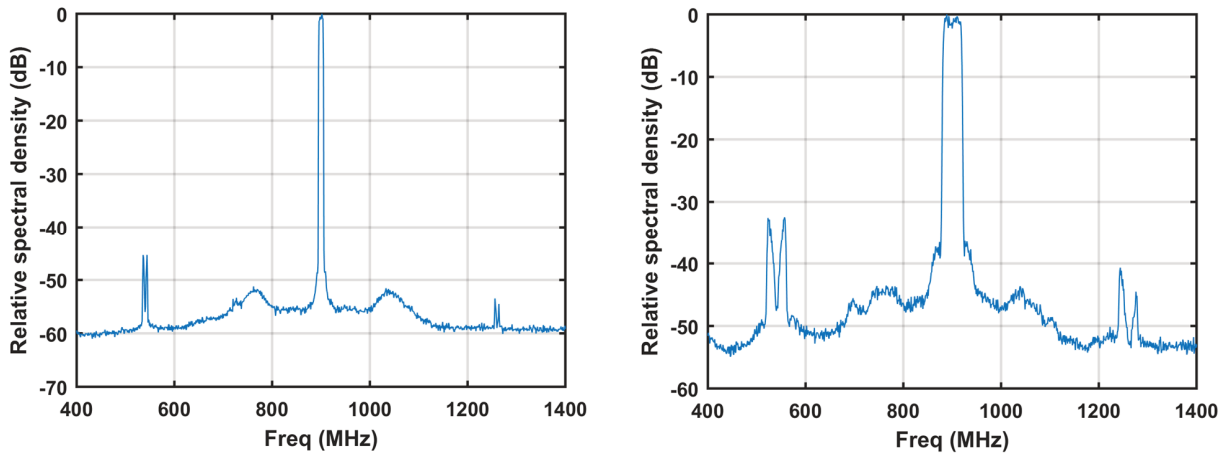


Figure 2.22 : The out-of-band spectrum for 9MHz modulation (left) and 40 MHz modulation (right)

The out-of-band spectra for the 9 MHz and 40 MHz modulations are shown in Fig. 2.22. The digital replicas due to zero-order hold operation of the digital inputs are located at 360 MHz offset as expected; the higher frequency replica is smaller due to matching network attenuation. An on-chip interpolation filter [19] can increase the offset frequency and greatly attenuate the digital replicas. A ground bounce-related spurious output is observed at 120MHz offset in both cases due to bondwire inductance on supply/ground.

Table 2.1 : Comparison with CMOS PA with back-off efficiency enhancement

	This Work	**[15]**	**[20]**	**[19]**	**[13]**	**[17]**
Freq(MHz)	900	2000	2000	2200	3500	1900
1dB Psat BW(%)	**33**	15	10	29	25	17
Psat (dBm)	24	24.3	20	23.3	27.3	28
Technology	65(LP)	65(LP)	65	65	65	40
Vdd	1.2/2.4	1.4/2.8	-	1.2	1.2/3	1.5
Peak/6dB Eff(%)	45/34 (PAE)	44/37[6] (PAE)	22/17 (PAE)	43/33 (DE)	33/34 (DE)	34/26 (PAE)
Topology	VMD	ClassG	ClassG	XFMR	Doherty	Doherty
Modulation	**40MHz 802.11ac 256QAM**	20MHz 802.11g 64QAM	5MHz LTE 64QAM	20MHz 802.11g 64QAM	0.5MHz 16QAM	20MHz LTE 16QAM
PAPR(dB)[4]	**9.0**	7.5	5.8	6.5	5.5	4.6
EVM (dB)	**-34.8**[1]	-30.8[3]	-28[1]	-28[1]	-25[2]	-23[3]
Avg Eff(%)	22	33[6]	12	21.8	22.1	23.3
Equivalent Eff (%)[5]	**62**	78[6]	24	46	42	40
Matching Network	Off-Chip	Off-Chip	On-Chip	On-Chip	On-Chip	On-Chip

[1]With LUT [2]Partial LUT [3]No LUT [4]Output PAPR=Psat-Pout
[5]Efficiency of ideal Class-B PA that achieve the same Avg Eff
[6]Output balun loss is not included

The measurement showed that this PA achieves superior linearity suitable for modern and future modulation standards while maintaining similar efficiency as the current state-of-the-art (Table I). To account for PAPR differences in the comparison of average efficiency for different modulations, we have introduced "equivalent efficiency", defined as the peak efficiency of an ideal class-B amplifier that gives the same average efficiency. This equivalent efficiency can be approximated by $\eta_{eff} = \eta_{avg}\sqrt{PAPR}$ with reasonable accuracy. An amplifier with class-B back-off characteristics would have $\eta_{eff} \approx \eta_{peak}$ regardless of the PAPR of the modulation and the PA with back-off efficiency enhancement would have $\eta_{eff} > \eta_{peak}$. The equivalent efficiency metric illustrates the fact that maintaining high efficiency is increasingly difficult for high back-off, although the detailed relationship between efficiency and back-off does not correspond to the Class

B case for all architectures. In Table I it is also important to note that on-chip matching generally leads to higher insertion loss, resulting in lower output power and efficiency.

2.7 Conclusion

This paper demonstrates a new Doherty technique that eliminates the impedance inverter, thus enabling wide bandwidth. To the authors' knowledge, this is the widest fractional bandwidth (at both peak and 6dB PBO) Doherty amplifier demonstrated in CMOS technology. With only simple look-up table linearization, this amplifier can transmit a 256-QAM 40 MHz 802.11ac modulation meeting the specification without back-off, while also maintaining excellent efficiency. Since this PA uses CMOS transistors as switches, its performance improves with CMOS technology scaling, especially with recent advances in PMOS transistor performance. This should make it possible to use this technique for even higher carrier frequencies, for example, for a 6 GHz carrier with integrated transformer, amplifying up to 160 MHz modulation (similar fractional bandwidth) with reasonable efficiency.

2.8 Acknowledgement

The authors are grateful to the DARPA RF-FPGA program (Dr. W. Chappell and Dr. R. Olsson) and U.S. Air Force Research Laboratory (Dr. P. Watson) for partial support.

Chapter 2, in full, is a reprint of the material as it appears in Voltage Mode Doherty Power Amplifier in IEEE Journal of Solid-State Circuits, vol. 52, no. 5, pp. 1295-1304, May 2017. V. Vorapipat, C. S. Levy and P. M. Asbeck. The dissertation author was the primary investigator and author of this paper.

2.9 References

[1] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*, 2nd ed. Norwood, MA, USA: Artech House, 2006.

[2] Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications: Enhancements for Very High Throughput for Operation in Bands below 6GHz, 2013

[3] Feipeng Wang, A. H. Yang, D. F. Kimball, L. E. Larson and P. M. Asbeck, "Design of wide-bandwidth envelope-tracking power amplifiers for OFDM applications," IEEE Transactions on Microwave Theory and Techniques, vol. 53, no. 4, pp. 1244-1255, April 2005.

[4] H. Chireix, “High power outphasing modulation,” Proc. IRE, Nov. 1935, vol. 23, no. 11, pp. 1370–1392.

[5] Doherty, W.H., "A New High Efficiency Power Amplifier for Modulated Waves," Radio Engineers, Proceedings of the Institute of , vol.24, no.9, pp.1163-1182, Sept. 1936

[6] P. Draxler, J. Deng, D. Kimball, I. Langmore and P. M. Asbeck, "Memory effect evaluation and predistortion of power amplifiers," IEEE MTT-S International Microwave Symposium Digest, 2005., 2005, pp. 4 pp.-.

[7] J. H. Qureshi, W. Sneijers, R. Keenan, L. C. N. deVreede and F. van Rijs, "A 700-W peak ultra-wideband broadcast Doherty amplifier," 2014 IEEE MTT-S International Microwave Symposium (IMS2014), Tampa, FL, 2014, pp. 1-4.

[8] R. Giofre, L. Piazzon, P. Colantonio, and F. Giannini, “A distributed matching/combining network suitable for Doherty power amplifiers covering more than an octave frequency band,” Proc. IEEE MTT-S Int. Microwave Symp., 2014, pp. 1–3.

[9] M. N. A. Abadi, H. Golestaneh, H. Sarbishaei, and S. Boumaiza, “An extended bandwidth Doherty power amplifier using a novel output combiner,” Proc. IEEE MTT-S Int. Microwave Symp., 2014, pp. 1–4.

[10] G. Liu, P. Haldi, T. J. K. Liu and A. M. Niknejad, "Fully Integrated CMOS Power Amplifier With Efficiency Enhancement at Power Back-Off," IEEE J. of Solid-State Circuits, vol. 43, no. 3, pp. 600-609, March 2008.

[11] E. Kaymaksut and P. Reynaert, "CMOS transformer-based uneven Doherty power amplifier for WLAN applications," ESSCIRC (ESSCIRC), 2011 Proceedings of the, Helsinki, 2011, pp. 135-138.

[12] R. M. Fano, “Theoretical Limitations on the Broadband Matching of Arbitrary Impedances,” J. Franklin Institute, vol. 249, pp. 57-83, Jan. 1950, and pp. 139-155, Feb. 1960.

[13] S. Hu, S. Kousai, J. S. Park, O. L. Chlieh and H. Wang, "Design of A Transformer-Based Reconfigurable Digital Polar Doherty Power Amplifier Fully Integrated in Bulk CMOS," IEEE Journal of Solid-State Circuits, vol. 50, no. 5, pp. 1094-1106, May 2015.

[14] S. M. Yoo, J. S. Walling, E. C. Woo, B. Jann and D. J. Allstot, "A Switched-Capacitor RF Power Amplifier," IEEE J. of Solid-State Circuits, vol. 46, no. 12, pp. 2977-2987, Dec. 2011.

[15] S. M. Yoo, J. S. Walling, O. Degani, B. Jann, R. Sadhwani, J. C. Rudell and D. J. Allstot, "A Class-G Switched-Capacitor RF Power Amplifier," IEEE J. of Solid-State Circuits, vol. 48, no. 5, pp. 1212-1224, May 2013.

[16] W. Tai, H. Xu, A. Ravi, H. Lakdawala, O. Degani, L. R. Carley and Y. Palaskas, "A Transformer-Combined 31.5 dBm Outphasing Power Amplifier in 45 nm LP CMOS With Dynamic Power Control for Back-Off Power Efficiency Enhancement," IEEE J. of Solid-State Circuits, vol. 47, no. 7, pp. 1646-1658, July 2012.

[17] E. Kaymaksut and P. Reynaert, "Dual-Mode CMOS Doherty LTE Power Amplifier With Symmetric Hybrid Transformer," IEEE J. of Solid-State Circuits, vol. 50, no. 9, pp. 1974-1987, Sept. 2015.

[18] B. Serneels, M. Steyaert and W. Dehaene, "A High speed, Low Voltage to High Voltage Level Shifter in Standard 1.2V 0.13µm CMOS," 2006 13th IEEE International Conference on Electronics, Circuits and Systems, Nice, 2006, pp. 668-671.

[19] L. Ye, J. Chen, L. Kong, E. Alon and A. M. Niknejad, "Design Considerations for a Direct Digitally Modulated WLAN Transmitter With Integrated Phase Path and Dynamic Impedance Modulation," IEEE J. of Solid-State Circuits, vol. 48, no. 12, pp. 3160-3177, Dec. 2013.

[20] W. Yuan, V. Aparin, J. Dunworth, L. Seward and J. S. Walling, "A Quadrature Switched Capacitor Power Amplifier," IEEE J. of Solid-State Circuits, vol. 51, no. 5, pp. 1200-1209, May 2016.

[21] J. C. Pedro, L. C. Nunes and P. M. Cabral, "A Simple Method to Estimate the Output Power and Efficiency Load–Pull Contours of Class-B Power Amplifiers," in IEEE Transactions on Microwave Theory and Techniques, vol. 63, no. 4, pp. 1239-1249, April 2015.

Chapter 3
A Class-G Voltage Mode Doherty Power Amplifier

3.1 Introduction

Since its invention in 1936, the Doherty power amplifier has seen widespread use to enhance efficiency in broadcast and communication systems transmitting signals with time-varying amplitude [1]. To achieve high spectral efficiency, many recent communications standards have adopted signals with high peak-to-average-power ratio (PAPR) modulation [2]. These high PAPR signals have again brought Doherty and other high back-off efficiency power amplifier (PA) architectures to the forefront [1]. At the same time, these modern digital modulation formats bring the additional demand of high linearity due to their tightly packed symbols. For example, an error vector magnitude (EVM) better than -35dB is required for 1024-QAM OFDM modulation, a format that will be used in the upcoming 802.11ax standard.

A variety of techniques, such as Doherty[3], Outphasing[4], and Class-G [5][6] (discrete supply switching), have been shown to greatly improve PA back-off efficiency to about 6 dB backoff (Fig. 3.1a). However, as PAPR continues to increase beyond 6 dB, this hard-earned

efficiency enhancement gives only a minor improvement in average power added efficiency (PAE). To address this issue, a wide variety of extensions to the aforementioned techniques have been proposed, yet most suffer from a significant performance tradeoff. One such example, often referred to as extended Doherty[7], increases the impedance inverter characteristic impedance, as well as the size of the peaking amplifier, to realize an efficiency peak at deeper back-off. Unfortunately the increased characteristic impedance leads to a higher impedance transformation ratio, increasing loss and limiting bandwidth. Extensions of other techniques [8][9] giving efficiency peaks at 9-12 dB back-off typically share similar trade-offs between efficiency, bandwidth, linearity, and design complexity. Alternatively, combinations of different efficiency-enhancement techniques can be applied to overcome the tradeoffs inherent to a single architecture at deep back-off and achieve high efficiency, bandwidth, and linearity in a low-complexity design. In this work we combine the recently-developed Voltage-Mode Doherty (VMD)[10] with the Class-G switched-capacitor power amplifier (CG-SCPA)[6] for efficiency peaking at both 6 dB and 12 dB back-off (Fig. 3.1b).

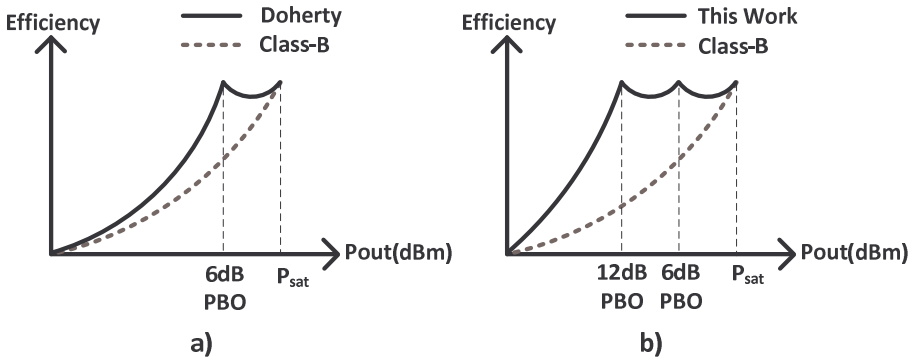


Figure 3.1 : The ideal efficiency of a) Conventional Doherty PA and b) this work, vs ouput power.

3.2 Previous Architectures

Combinations of efficiency enhancement techniques from Doherty with class-G [11], Outphasing with multi-level class-G [12], and Outphasing with power combined transformer [13], have been demonstrated to achieve efficiency enhancement beyond 6dB back-off. However these techniques often suffer from a mode-switching glitch which can be characterized as a sudden change in system configuration such as power supply voltage, impedance level, or discontinuity of the input signal amplitude/phase at critical power levels, usually where efficiency peaks.

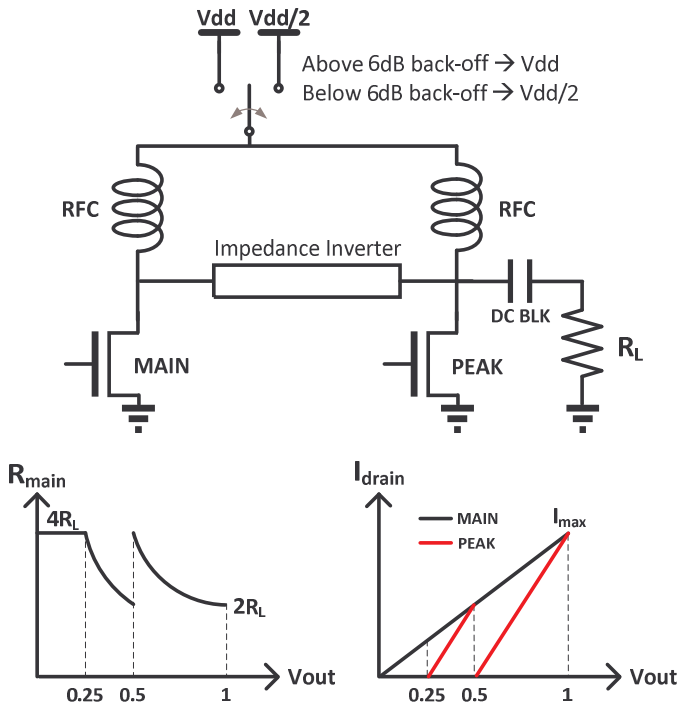


Figure 3.2 : Class-G conventional Doherty with a power switch added in the power supply path allowing switching between Vdd and Vdd/2 at 6dB back-off. A discontinuity in main PA impedance and peak PA current is seen at 6dB back-off.

As a representative example of a combined architecture, the classical Doherty PA can be used with discrete power supply switching (Class-G) [11] as shown in Fig. 3.2. From 0 dB to 6 dB back-off, the PA operates like the classical Doherty PA [3] providing efficiency peaking at 6dB back-off. To achieve additional efficiency peaking at 12dB back-off, mode switching is used. The power supply is switched from Vdd to Vdd/2, and the input drive is also changed such that both the main and peaking PAs deliver the same power to the load. After the mode-switch, the PA operate as classical Doherty PA but at half supply, resulting in a second efficiency peak at 12 dB back-off, 6 dB from halving the supply, 6 dB from Doherty operation.

Though this technique achieves high efficiency at 12 dB back-off, it has several drawbacks. First, the power supply switching at 6 dB back-off causes the glitch in the signal envelope [14] and significant power supply ringing [12] which distorts the PA output. Moreover, the step change in power supply also introduces a large jump in the AM-PM characteristics [11] due to non-linear drain capacitance. This effect is difficult to correct with pre-distortion as it significantly increases the bandwidth requirement of the pre-distorted signal. Second, the transistor used to implement the power supply switch must be very large in order to achieve the low on-resistance required to maintain high efficiency. This makes it difficult to precisely control the timing of power supply switching and usually limited its use to power control application [15]. In dynamic power supply modulation [11], the timing must be synchronized with the PA input signal. This restricts the maximum modulation bandwidth of the technique and significantly increases design complexity.

Several techniques have been proposed to mitigate the mode-switching glitch. One notable technique, shown in [13], skips a transition to the low power mode if two or more mode transitions would be required within a predefined time interval. It is shown in [13] that increasing

the skipping time interval reduces distortion (ACPR) of the transmitted signal. Unfortunately, the loss of efficiency enhancement when more mode transitions are skipped leads to a reduced average efficiency. As the modulation bandwidth increases the number of skipped transitions required to maintain the same distortion level increases proportionally, severely limiting overall efficiency enhancement.

The described problems associated with mode-switching glitches makes it desirable to find techniques which leverage the efficiency benefit of multiple power supplies, yet do not require instantaneous reconfiguration of the entire PA. This would allow for improved efficiency beyond 6 dB back-off without the large, sudden changes associated with mode-switching.

3.3 Proposed Architecture

In this work, the VMD and CG-SCPA architectures are combined for efficiency peaking at both 6dB and 12dB back-off. The architecture is termed Class-G Voltage-Mode Doherty (CG-VMD). First, the VMD and CG-SCPA architectures, each of which provides 6dB efficiency peaking, will be discussed, and then the use of the two techniques in concert to form the CG-VMD will be introduced.

3.3.1 Voltage Mode Doherty

VMD is a modification of the Current-Voltage Doherty (Fig. 3.3a) used by Doherty as a starting point for the derivation of the classic Doherty PA[3]. In the Current-Voltage Doherty architecture, the peaking PA (voltage source) modulates the load impedance of the main PA (current source) such that higher impedance is presented at lower power resulting in efficiency peaking at 6 dB back-off. The advantage of this topology is that it does not require a narrowband

impedance inverter [16] to achieve load modulation, enabling wide bandwidth. In VMD, the main PA is replaced with a voltage source, without changing the load modulation property of the main PA, and the floating load is replaced with a balun driving a single ended load (Fig. 3.3b). It can be shown that the impedance seen by the main PA is given by $R_m = R_L/(1 + V_p/V_m)$, where V_m and V_p are the main and peaking amplifier voltages respectively [10]. The operation from zero power to full power is as follows: the main PA turns on first and its voltage increases until the main PA saturates at 6 dB back-off, then the peaking PA voltage increases until it also reaches saturation. This results in the main PA impedance profile of Fig. 3.3c, and efficiency peaking at 6 dB back-off (Fig. 3.3d). Note that there is no additional switch [17] required to short the peaking PA at low power since it is a voltage source and thus itself provides a short when turned off. The high efficiency voltage sources in the VMD are realized with switched capacitor PAs [18] (SCPA) which provide high efficiency, linearity, and dynamic range, at GHz frequencies.

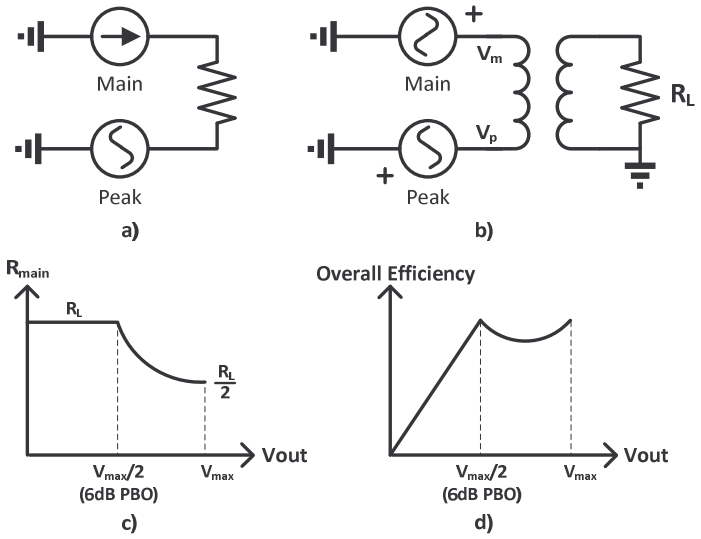


Figure 3.3 : a)Current-Voltage Doherty topology; b)Voltage Mode Doherty; c)Main PA impedance trajectory; d)Overall efficiency of Voltage Mode Doherty.

For wideband, high efficiency operation, the VMD takes advantage of primary load modulation [10][15] to completely utilize the transformer structure at all power levels. To implement the VMD alone with peaking at 12 dB back-off, four transformers would need to be stacked and secondary load modulation must be used [19]. This results in low efficiency and narrow bandwidth when the PA operates at 12 dB back-off.

3.3.2 Class-G Switched Capacitor PA

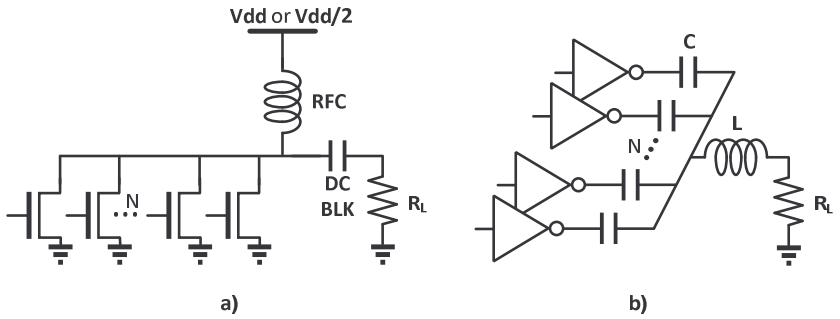


Figure 3.4 : a)Conventional Class-G RF-DAC b)Switched Capacitor Power Amplifier (SCPA)

Conventional Class-G PAs have the drawback of a mode-switching glitch [14]. This is because there is a single power supply for the entire PA (Fig. 3.4a). At low power, the PA operates in half-supply mode, reaching saturation at about 6 dB back-off. To further increase output power to the load, the power supply must be switched to full-supply. Though the AM-AM distortion from supply switching can be corrected in steady state, this correction is sensitive to PVT variations. Additionally correcting the static AM-AM does not remove potential AM-PM discontinuities [11]. Even with a static correction, when the supply transitions, the voltage at the drain of the transistor cannot change instantaneously causing a brief AM-AM and AM-PM error which can be greater than an LSB, a so called "glitch". This glitch can be modeled as a short absence of signal which causes degradation in EVM, ACPR, and noise floor [14]. Since the

frequency of supply transitions increase with modulation bandwidth, power supply switching glitches limit the usefulness of conventional class-G techniques to narrow-band modulation. By contrast, in a SCPA all unit cells are ac-coupled to the output (Fig. 3.4b), allowing individual unit cells to operate from different power supplies. This flexibility gives glitch-free class-G operation [6]. At low power, all unit cells operate in half-supply mode until saturation is reached. To further increase the output power, unit cells operating at half-supply can transition to full-supply one-by-one without introducing a significant glitch in the PA output. The supply-switching glitch in a CG-SCPA is that of a single unit cell; as the resolution of the CG-SCPA increases, the supply switching glitch becomes arbitrarily small.

To extend the CG-SCPA concept to 12 dB back-off, unit cells would need to be capable of operating at full-, half-, and quarter-supply, significantly increasing unit cell design complexity and resulting in poor overall efficiency.

3.3.3 Class-G Voltage Mode Doherty

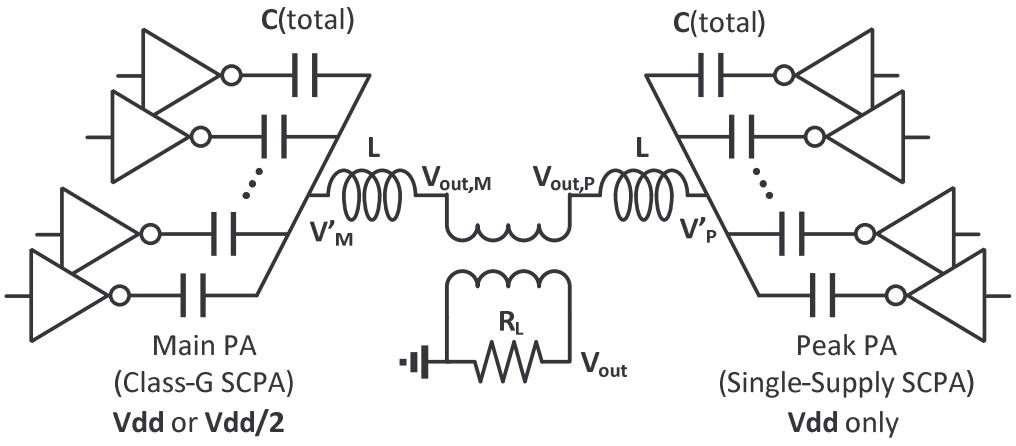


Figure 3.5 : The Class-G Voltage Mode Doherty. The unit cells in the main PA can independently operate at either full-supply or half-supply.

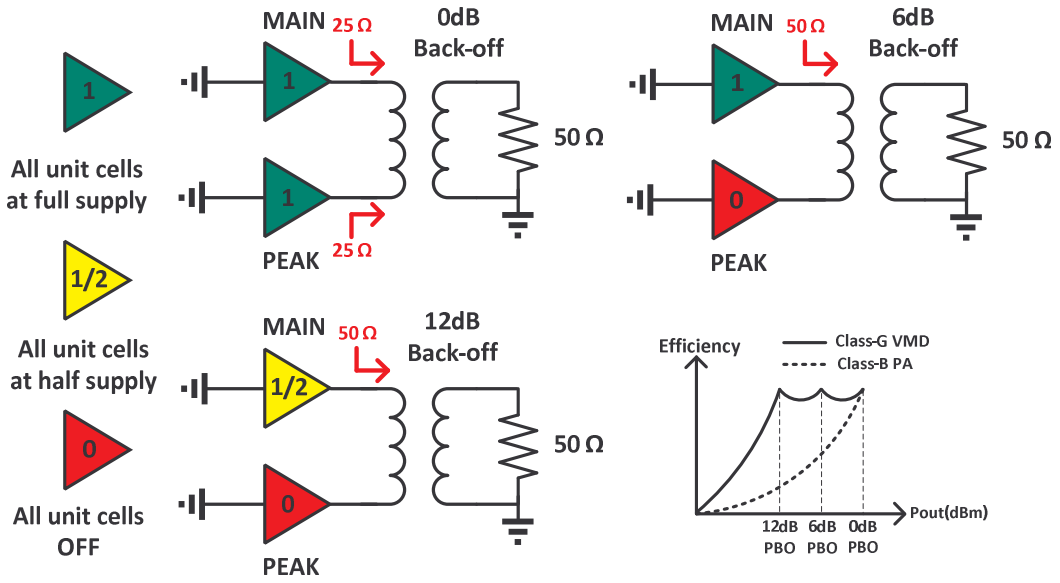


Figure 3.6 : Class-G Voltage Mode Doherty operation at different efficiency peaking points. At 6dB back-off, Voltage Mode Doherty gives efficiency peaking. At 12dB back-off, a combination of Voltage Mode Doherty and Class-G SCPA provide the peaking.

The CG-VMD [20] is composed of a CG-SCPA used for the main PA and a SCPA for the peaking, operating across a transformer (Fig. 3.5). As shown in Fig. 3.6, at full power, the main and peaking PAs drive the transformer in anti-phase at full amplitude with a 25 Ω impedance seen by each PA. From full power to 6 dB back-off, the peaking PA unit cells start to turn off, reducing the output amplitude, and increasing the impedance seen by the main PA until it reaches 50 Ω. At 6 dB back-off the peaking PA is completely off and the main PA operates in saturation from full-supply, providing efficiency peaking [10]. From 6 dB to 12 dB back-off, the main PA unit cells transition one-by-one from full-supply to half-supply, gradually decreasing the main PA amplitude until all unit cells operate at half-supply. With high impedance (50 Ω) load and half-supply for the main PA, efficiency peaking at 12 dB back-off is achieved. The unit cell turn-on sequence for a CG-VMD with four unary-weighted unit cells in both the main and

peaking amplifier is summarized in Fig. 3.7. As shown, only one unit cell changes state at a time, reducing jumps in power supply or impedance to a single unit cell step. Moreover, once the unit cell turn-on sequence is chosen, the operation of CG-VMD is as simple as that of a standard RFDAC [21], with no additional synchronized mode-switching path needed [11][17].

Vout	Back Off (dB)	CG-SCPA (Main)				SCPA (Peak)			
0	OFF	0	0	0	0	0	0	0	0
1/16	24	.5	0	0	0	0	0	0	0
2/16	18	.5	.5	0	0	0	0	0	0
3/16	15	.5	.5	.5	0	0	0	0	0
4/16	12	.5	.5	.5	.5	0	0	0	0
5/16	10	1	.5	.5	.5	0	0	0	0
6/16	9	1	1	.5	.5	0	0	0	0
7/16	7	1	1	1	.5	0	0	0	0
8/16	6	1	1	1	1	0	0	0	0
10/16	4.1	1	1	1	1	1	0	0	0
12/16	2.5	1	1	1	1	1	1	0	0
14/16	1.2	1	1	1	1	1	1	1	0
16/16	0	1	1	1	1	1	1	1	1

0
Off

0.5
Half Supply

1
Full Supply

Figure 3.7 : The unit cell turn-on sequence of CG-VMD.

3.4 Detailed Analysis

Inasmuch as a variety of non-idealities will inevitably degrade back-off efficiency, the class-G voltage-mode Doherty PA will be analyzed considering all relevant loss mechanisms. We will first assume ideal transistors and matching network to demonstrate the CG-VMD principle and its inherent capacitive divider losses. Then non-idealities of the totem-pole driver and output matching network will be included to show the design trade-offs at GHz frequencies.

3.4.1 Class-G Voltage-Mode Doherty with Ideal Components

The loss of the class-G voltage-mode Doherty comes primarily from the charging-and-discharging of the capacitive divider banks of the main and peaking PAs which occurs at the rising and falling edges of the RF input signal. We will first calculate the capacitive divider loss of the CG-SCPA and then generalize it to the CG-VMD.

3.4.1.1 Capacitive Divider Loss of CG-SCPA

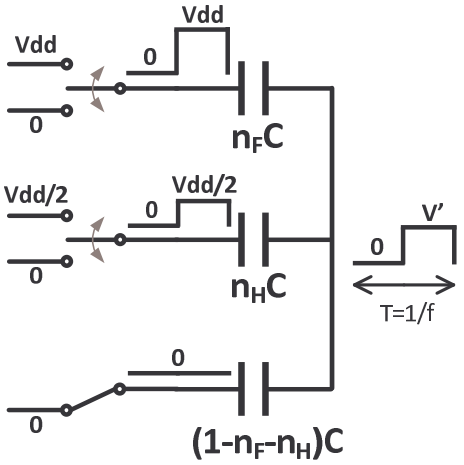


Figure 3.8 : CG-SCPA equivalent circuit for capacitive divider loss analysis.

Assuming fast rising/falling edges at the driver output, the inductors in the CG-SCPA matching network will act as open circuits at voltage transitions [18]. The equivalent circuit of the main PA (CG-SCPA) can be simplified as shown in Fig. 3.8 where the unit cells are lumped into three groups: switching at full supply, switching at half supply, and off. If n_F,n_H are the fraction of unit cells operating at full- and half-supply respectively, by the capacitive divider principle, the voltage swing at V' can be written as

$$V' = V_{dd}n_F + 0.5V_{dd}n_H = (n_F + 0.5n_H)V_{dd} \quad (1)$$

At the rising edge, the amount of charge taken from full- and half-supplies is

$$Q_F = n_F C(V_{dd} - V') = n_F C V_{dd}(1 - n_F - 0.5n_H) \quad (2)$$

$$Q_H = n_H C(0.5V_{dd} - V') = n_H C V_{dd}(0.5 - n_F - 0.5n_H) \quad (3)$$

and with RF carrier frequency f, the power dissipation due to the capacitive divider is

$$P_{cd} = [n_F(1 - n_F) + 0.25n_H(1 - n_H) - n_F n_H]CV_{dd}^2 f \quad (4)$$

The waveform at node V' is filtered by the series LC resonator resulting in a sinusoidal waveform at the primary side of the transformer (Fig. 3.5) with amplitude

$$V_{out,M} = \frac{2}{\pi}V' = \frac{2}{\pi}(n_F + 0.5n_H)V_{dd} \quad (5)$$

3.4.1.2 Efficiency of CG-VMD

The efficiency of the CG-VMD for any choice of amplitude control word (ACW) is derived in this section. From Fig. 3.5, the capacitive divider loss and output voltage are

$$P_{cd} = P_{cd,M} + P_{cd,P} \quad (6) \qquad \text{and} \qquad V_{out} = V_{out,M} + V_{out,P} \quad (7)$$

which can be expanded to

$$P_{cd} = [n_{FM}(1 - n_{FM}) + n_{FP}(1 - n_{FP}) + 0.25n_{HM}(1 - n_{HM}) - n_{FM}n_{HM}]CV_{dd}^2 f \quad (8)$$

$$V_{out} = \frac{2}{\pi}(n_{FM} + n_{FP} + 0.5n_{HM})V_{dd} \quad (9)$$

where the M and P subscripts denote main and peaking amplifier respectively ($n_{HP} = 0$). The

output power and efficiency are then

$$P_{out}^{0} = \frac{V_{out}^{2}}{2R_L} = \frac{2}{\pi^2 R_L} V_{dd}^{2}(n_{FM} + n_{FP} + 0.5n_{HM})^2 \quad (10)$$

$$\eta = \frac{P_{out}^{0}}{P_{out}^{0} + P_{cd}} = \frac{1}{1 + \frac{P_{cd}}{P_{out}^{0}}} \quad (11)$$

$$\eta = \frac{1}{1 + \frac{\pi}{2Q_L} \frac{n_{FM}(1 - n_{FM}) + n_{FP}(1 - n_{FP}) + 0.25n_{HM}(1 - n_{HM}) - n_{FM}n_{HM}}{(n_{FM} + n_{FP} + 0.5n_{HM})^2}} \quad (12)$$

with $Q_L = \frac{1}{2\pi f R_L \frac{C}{2}}$ being the loaded quality factor of the CG-VMD structure.

Though the capacitive divider loss of the PA is proportional to the carrier frequency as indicated by (8), it does not increase with frequency. This is because as frequency increases, the capacitor size decreases proportionally to maintain the same reactance. The efficiency of the PA depends on the loaded quality factor Q_L, with higher Q_L leading to lower capacitive divider switching loss and improved efficiency, but also reduced bandwidth, increased matching network insertion loss, and increased voltage stress on the capacitor bank. These issues limit practical implementations with on-chip matching networks to $Q_L \approx 2$ [10].

3.4.1.3 Efficiency Comparison

In this section, the ACW trajectories (n_{FM},n_{HM},n_{FP} vs V_{out}) for differential SCPA, voltage-mode Doherty and class-G voltage-mode Doherty will be described and the normalized loss and efficiency for these cases will be compared.

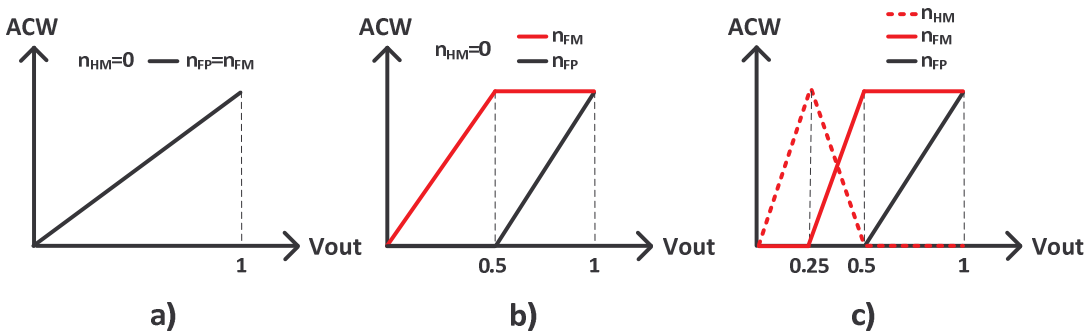


Figure 3.9 : Amplitude control word trajectory of a)Differential SCPA b)Voltage Mode Doherty and c) Class-G Voltage Mode Doherty.

Fig. 3.9a shows differential SCPA operation, with the main and peaking PAs operating from full-supply with equal magnitudes. Fig. 3.9b shows VMD operation, with both PAs operating at full supply. The main PA ACW increases until it saturates at 6 dB back-off, and then the peaking PA increases to saturation. Fig. 3.9c shows the CG-VMD operation. The unit cells of the main PA operate at half-supply until saturation at 12 dB back-off. Then the unit cells of the main PA transition one-by-one to full-supply thus n_{FM} increases as n_{HM} decreases. At 6 dB back-off, the main PA saturates at full supply. The peaking PA ACW then increases in the fashion as VMD.

The normalized loss and efficiency for SCPA, VMD, and CG-VMD are plotted in fig. 3.10. In VMD the peak capacitive divider loss is half that of the SCPA, and there is also a loss null at 6dB back-off, resulting in the corresponding 6 dB efficiency peak. Beyond 6 dB back-off, CG-VMD reduces the peak loss by another factor of 4 with an additional loss null at 12dB back-off, leading to 12 dB efficiency peaking.

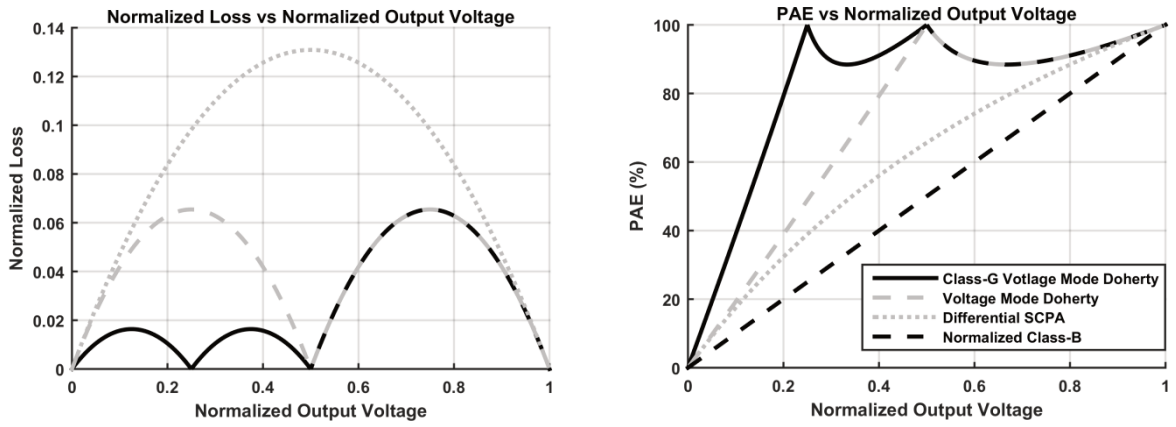


Figure 3.10 : Normalized loss and efficiency comparison of differential SCPA, Voltage Mode Doherty and Class-G Voltage Mode Doherty. (Q_L=1.5 assumed)

3.4.2 Class-G Voltage Mode Doherty with Non-ideal Components

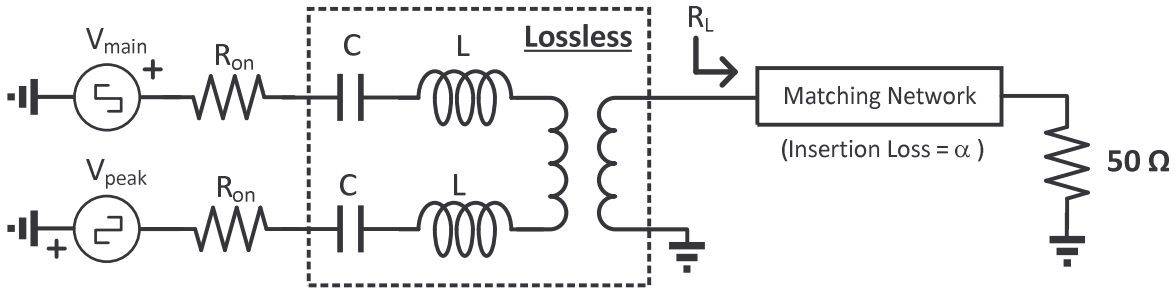


Figure 3.11 : Equivalent Circuit for loss analysis. The loss of capacitor bank, inductor and transformer are lumped into matching network loss.

The SCPA/CG-SCPA can be modeled as a square wave voltage source with on-resistance R_{on} as shown in fig. 3.11 [10]. The power delivered by the PA to the output matching network is

$P'_{out} = \frac{P^0_{out}}{\left(1+\frac{2R_{on}}{R_L}\right)^2}$ (13) , and the conduction loss is $\frac{P_{cond}}{P'_{out}} = \frac{2R_{on}}{R_L}$ (14).

Insertion loss attenuates the power delivered to the load by $P_{out} = \alpha P'_{out}$.

Switching losses come from the charge/discharge of parasitic capacitors and crowbar current in the SCPA/CG-SCPA drivers. This loss can be represented by an equivalent loss capacitance $C_{sw} \equiv \frac{P}{V^2_{supply} f}$ where P is the power dissipated by the SCPA/CG-SCPA, including predrivers, when all cells are switching at frequency f, operating at V_{supply}, and drive no load. With this equivalent loss capacitance, the switching loss is

$$P_{sw} = n_{FM} C_{sw,FM} V^2_{dd} f + n_{HM} C_{sw,HM} (0.5V_{dd})^2 f + n_{FP} C_{sw,FP} V^2_{dd} f \quad (15).$$

Conduction and switching losses can be traded through the sizing of the output stage transistors, with $R_{on} \propto \frac{1}{W}$ and $C_{sw} \propto W$. Therefore, the product $R_{on} C_{sw}$ is constant and we can define the totem pole driver figure of merit $f_{sw} = \frac{1}{2\pi R_{on} C_{sw}}$ [10]. CMOS process scaling, anti-shoot-through current driver design, and good layout practice can improve f_{sw}. The switching loss relative to the power delivered to matching network is

$$\frac{P_{sw}}{P'_{out}} = \frac{\pi}{2} \frac{R_L}{2R_{on}} \left(1 + \frac{2R_{on}}{R_L}\right)^2 \frac{f}{f_{sw}} \frac{n_{FM} + 0.25k' n_{HM} + n_{FP}}{(n_{FM} + 0.5n_{HM} + n_{FP})^2} \quad (16)$$

where f_{sw} is defined for the CG-SCPA operating at full supply, and $k' = \frac{f_{sw,Vdd}}{f_{sw,Vdd/2}}$ is the ratio of CG-SCPA figures of merit when operating at full and half supply respectively.

The overall output power and efficiency can now be written as

$$P_{out} = \frac{\frac{2\alpha}{\pi^2}\frac{V_{dd}^2}{R_L}(n_{FM} + 0.5n_{HM} + n_{FP})^2}{\left(1 + \frac{2R_{on}}{R_L}\right)^2} \quad (17) \quad \text{and} \quad \eta = \frac{\alpha}{1 + \frac{P_{cond}}{P'_{out}} + \frac{P_{sw}}{P'_{out}} + \frac{P_{cd}}{P'_{out}}} \quad (18)$$

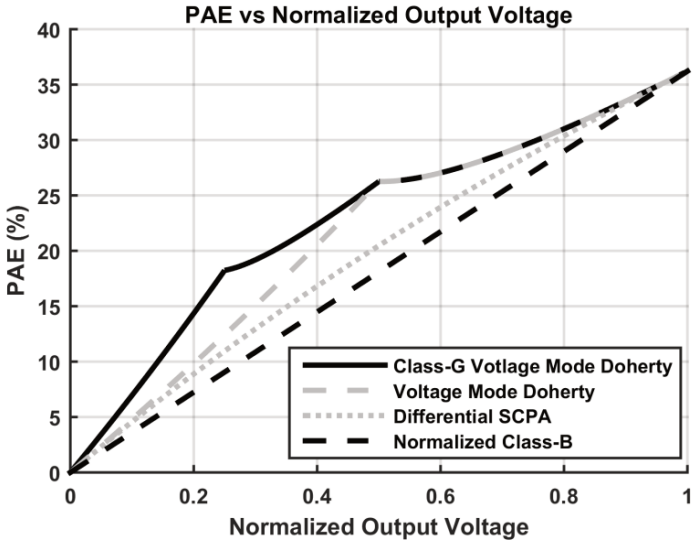


Figure 3.12 : Efficiency comparison of SCPA, VMD and CG-SCPA with all relevant losses included. (α=0.7, 2Ron/RL =0.2, fsw=27 GHz, f=3.5 GHz, and k'=1.8)

Fig. 3.12 shows the overall efficiency of the class-G voltage-mode Doherty, using representative values of α, $2R_{on}/R_L$, f_{sw}, k', and f, used in this work. Note that when conduction and switching losses are added, the efficiencies 0 dB, 6 dB and 12 dB back-off are no longer 100 %, and the efficiency peaking at deeper back-off is lower.

At critical powers, the capacitive divider loss is zero and since the relative conduction loss ($\frac{P_{cond}}{P'_{out}}$) is constant, the only factor reducing efficiency of the CG-VMD at deeper back-off is increased relative conduction loss. Let $2A_0 = \frac{\pi}{2}\frac{R_L}{2R_{on}}\left(1 + \frac{2R_{on}}{R_L}\right)^2 \frac{f}{f_{sw}}$. Then by equation 16, the relative switching loss at 0dB/6dB/12dB back-off is $\frac{P_{sw}}{P'_{out}}(0dB) = 2A_0\frac{1+0+1}{(1+0+1)^2} = A_0$,

$\frac{P_{sw}}{P'_{out}}(6dB) = 2A_0\frac{1+0+0}{(1+0+0)^2} = 2A_0$, $\frac{P_{sw}}{P'_{out}}(12dB) = 2A_0\frac{0+0.25k'+0}{(0+0.5+0)^2} = 2k'A_0 \sim 4A_0$. The increase in relative switching loss at 6dB back-off is due to the switching loss halving (only half of the unit cells are switching), while the output power is reduced by a factor of 4 [10]. The relative switching loss doubles again from 6 dB to 12 dB due to the decrease in f_{sw} of class-G inverter when operating at half supply. The doubling of relative switching loss in the CG-VMD for every 6 dB back-off in power emphasizes the difficulty in achieving high back-off efficiency [13]. Similar efficiency degradation is also present in the conventional Doherty PA due to a sub-optimal load impedance in back-off [22].

3.5 Implementation

The class-G voltage-mode Doherty (Fig. 3.13) is implemented as a digital polar PA [21], in which an identical phase modulated RF (PMRF) drives all unit cells, and the ACW determines whether each unit cell is OFF, ON at half-supply, or ON at full-supply. The main and peaking PAs are designed using a 5b unary, 4b binary, segmented DAC architecture such that the quantization noise will not limit the performance of the PA [24]. The PA is implemented in 45nm CMOS SOI with integrated output transformer, and drives a 50Ω load with no off-chip matching.

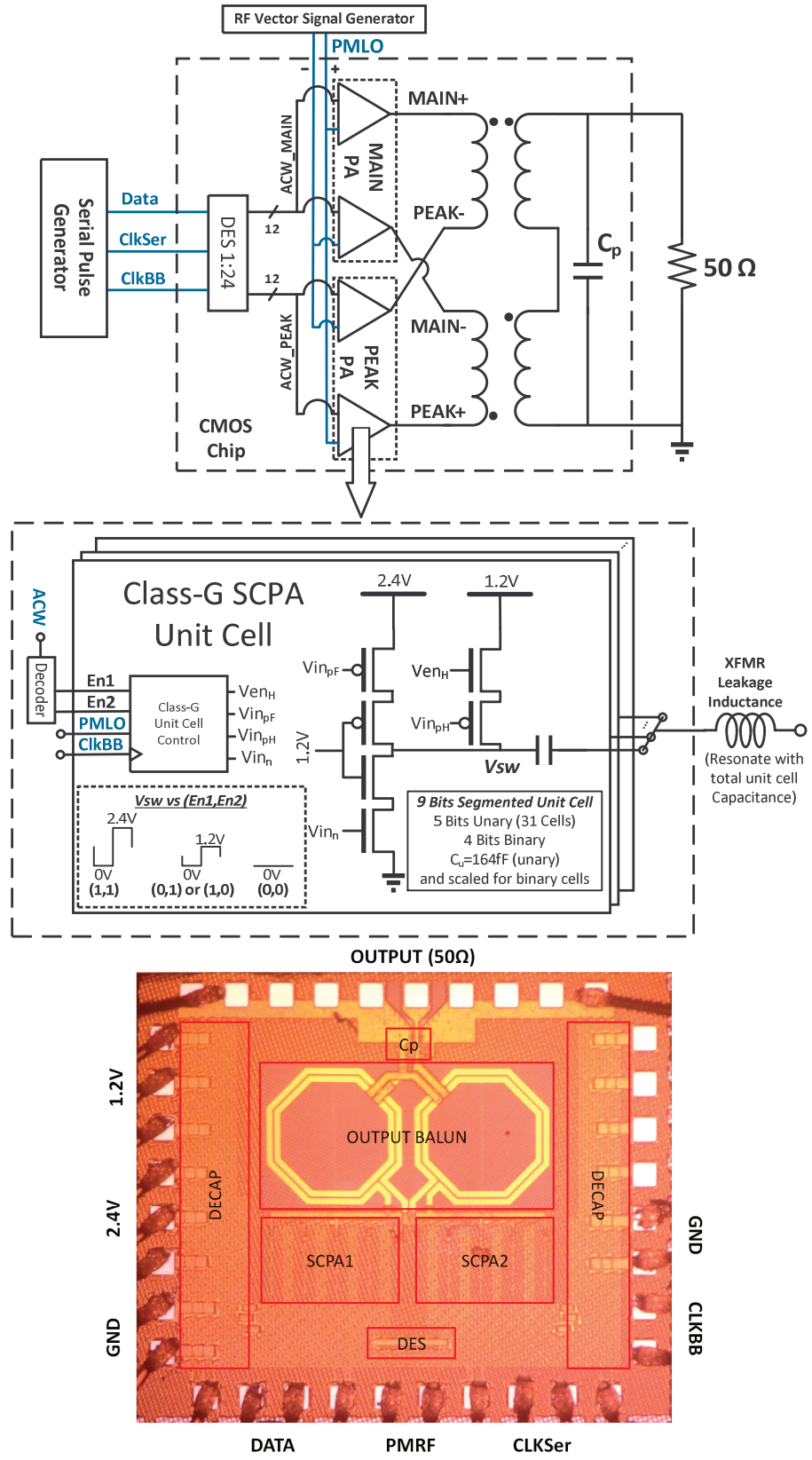


Figure 3.13 : Class-G Voltage Mode Doherty implementation and die micrograph

3.5.1 Output Transformer

The output transformer serves four purposes: differential to single-ended conversion, power combining, active load modulation, and wideband matching. First, the differential to single-ended conversion of the transformer allows the PA to be pseudo differential, increasing output power by 6 dB and reducing sensitivity to supply/ground inductance [10]. Second, the voltages of the main and peaking PAs are combined in series, increasing the peak output power by another 6 dB. Third, the transformer provides the VMD load modulation, doubling the impedance seen by the main PA at back-off, resulting in high efficiency. Moreover, primary load modulation fully utilizes the transformer structure at all power levels resulting in high back-off efficiency [15]. Lastly, the magnetizing and leakage inductances of the transformer are used as a wideband matching network such that no additional inductors are required.

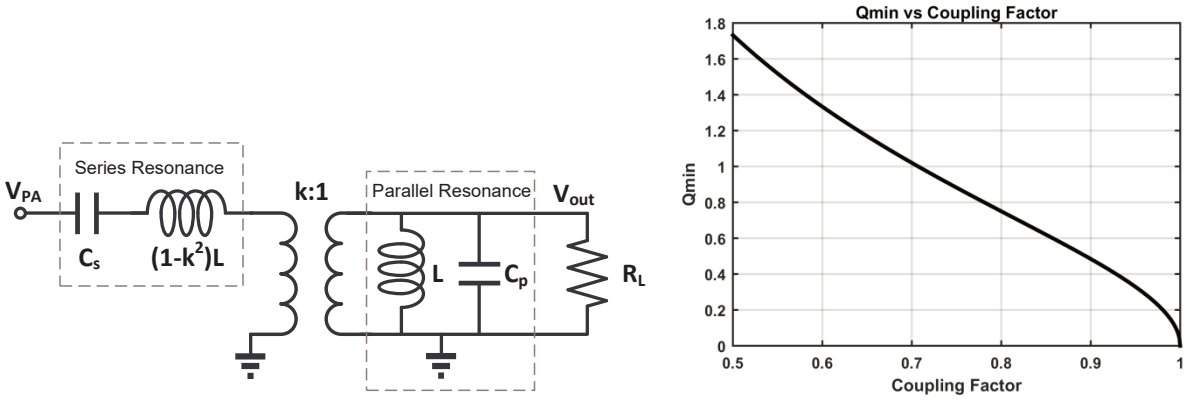


Figure 3.14 : Transformer as part of CG-VMD matching network, with the series resonance formed by leakage inductance and SCPA/CG-SCPA total unit cell capacitance, and the parallel resonance formed by magnetization inductance and a parallel matching capacitor. Qmin vs coupling factor shows the bandwidth limitation imposed by a limited coupling factor for the transformer.

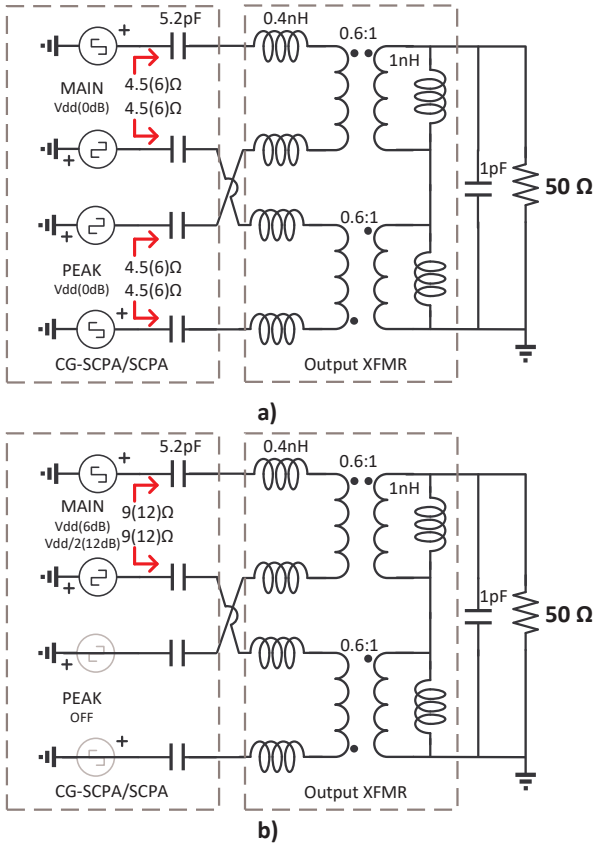


Figure 3.15 : Output transformer operation at a)peak power (0dB back-off) and b)6dB and 12dB back-off. The load impedance seen by the main PA is doubled at back-off as expected. The impedance shown excludes transformer loss. When the loss is included, the impedance increases as shown in parentheses.

The transformer can be modeled as coupled inductors with coupling factor k. At GHz frequencies, on-chip and low insertion loss transformers typically have $k \approx 0.7$, resulting in a leakage inductance comparable to the magnetizing inductance. Increasing transformer inductance lowers the quality factor of the parallel resonance $Q_p = \frac{R_L}{\omega L}$, but increases that of the series resonance $Q_s = \frac{\omega(1-k^2)L}{k^2 R_L}$ (Fig. 3.14). The overall bandwidth is determined by $\max(Q_s, Q_p)$. It can be shown that the minimum possible $\max(Q_s, Q_p)$ is $Q_{min} = \frac{\sqrt{1-k^2}}{k}$ which increases with

decreasing coupling factor (Fig. 3.14). Therefore, the bandwidth of the CG-VMD is limited by the achievable coupling factor of the transformer. The matching network in Fig. 3.14 provides reactance compensation at offsets from the center frequency. Above/below the center frequency, the series resonance has positive/negative reactance which cancels the negative/positive reactance of the parallel resonance resulting in wider bandwidth.

The transformer in this work is implemented as a figure-8 [23]. Electromagnetic simulations give k=0.6 and IL=1.6 dB for the balun. The load modulation of the CG-VMD output network operating at 0dB/6dB and 12dB back-off is shown in Fig. 3.15.

3.5.2 Class-G SCPA Unit Cell Design

To minimize the delay mismatch between main and peaking PAs, the unit cells of both PAs are implemented with CG-SCPA unit cells (Fig. 3.13). The half-supply mode of the peaking PA is disabled and thus it functions as a SCPA. To equalize voltage steps between the main and peaking PAs, the LSB cell of the main PA is also disabled. Each unit-cell is pseudo-differential to keep the fundamental virtual ground within the unit cell, reducing on-chip supply network loss and ripple [10]. The functionality of the CG-SCPA unit cell is explained in great detail in [6]; a brief explanation is provided here. In full-supply mode, Vin_{pF} and Vin_{n} switch, providing a 2.4V pk-pk square wave, and Ven_{H} prevents current flow from the 2.4V to 1.2V supply. In half supply mode, Vin_{pH} and Vin_{n} switch, providing a 1.2V pk-pk square wave. When the unit cell is off, Vin_{n}=1.2V, Vin_{pF}=2.4V, and Vin_{pH}=1.2V, tying the unit cell capacitor to ground.

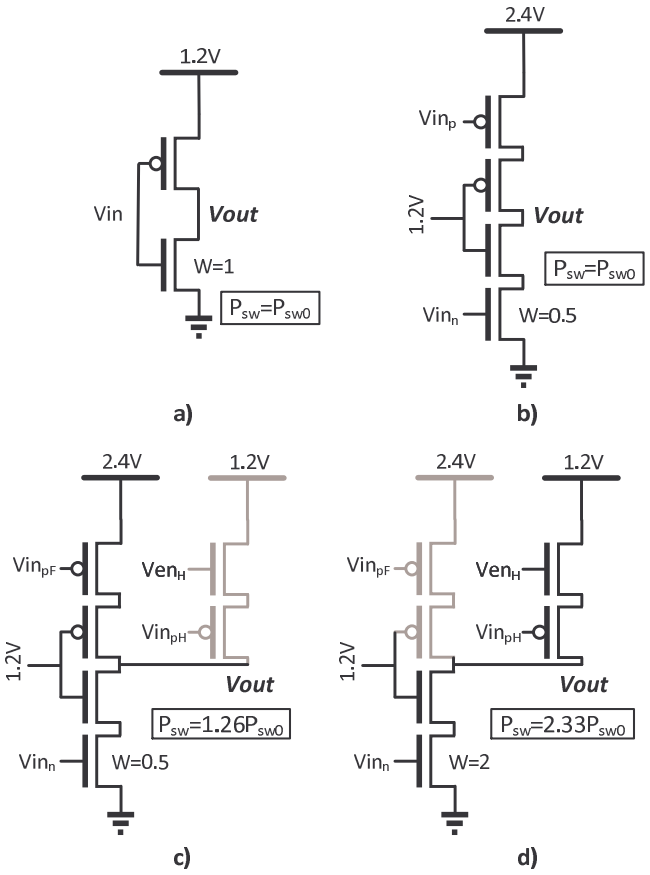


Figure 3.16 : Different totem pole driver designs: a)Simple inverter b)Cascode inverter c)Class-G inverter operating at full supply d)Class-G inverter operating at half supply. The relative size of NMOS transistors is shown in the figure; the PMOS transistors are scaled to achieve the same drive strength.

An important design metric of the unit cell is the totem pole driver figure of merit, f_{sw} discussed in section IV, which affects overall efficiency of the PA. Different totem pole driver designs are shown in Fig. 3.16. To compare f_{sw} among these topologies, the final stage is sized to deliver the same power to the load with the same conduction loss R_{on}/R_L, and the switching losses are compared. The simplest totem pole driver is a simple inverter, suitable for low power PAs. The cascode inverter doubles voltage swing, thus the load impedance can be 4 times higher for the same output power, reducing the transistor size in half. Though the cascode inverter by

itself has higher switching loss than a simple inverter, the power of the pre-driver is greatly reduced due to the smaller transistors, resulting in overall switching loss similar to that of a simple inverter. When operating at full supply, the class-G inverter is simply a cascode inverter with parasitic half-supply branch increasing switching loss by about 26%. The half-supply branch of the class-G inverter is stacked to withstand the full supply swing. This means, compared to a simple inverter, the transistors size must be doubled to maintain the same conduction loss, resulting in twice the switching loss. Including the parasitic full-supply branch, the switching loss is increased by 133%. This means that the relative switching loss of a class-G inverter when operating at half-supply compared to full-supply is $k' = \frac{f_{sw,Vdd}}{f_{sw,Vdd/2}} = 1.8$ (Fig. 3.12).

3.6 Measurement Setup and Result

The measurement setup is shown in Fig. 3.13. A RF vector signal generator (RF-VSG) is used to provide the phase-modulated LO (PM-LO), and a serial pulse pattern generator (PPG) is used to provide the ACW. The RF-VSG and PPG are synchronized with 10 MHz reference, and time alignment is performed at baseband. The output is probed with a 50 Ω GSG probe. The PAE accounts for all power consumed on the chip, including pre-drivers for all unit cells, LO distribution, and logic. The external PM-LO and serial ACW input signal powers are excluded, as most of the power is consumed in the termination resistors, while the power needed to drive a few minimum size inverters is all that would be required in an integrated implementation. Baseband signal generation, time alignment, and memoryless linearization is performed in MATLAB, with baseband sample frequency of 90 MHz, limited by the RF-VSG. Zero-order hold digital replicas appear at multiples of 90 MHz offset from the center frequency, and can be

improved by the use of on-chip interpolation filter and wideband phase modulator [17].

The 45nm CMOS SOI chips were fabricated on low resistivity and trap-rich high resistivity substrates. Unless stated, results shown are from low resistivity samples.

3.6.1 CW Measurement

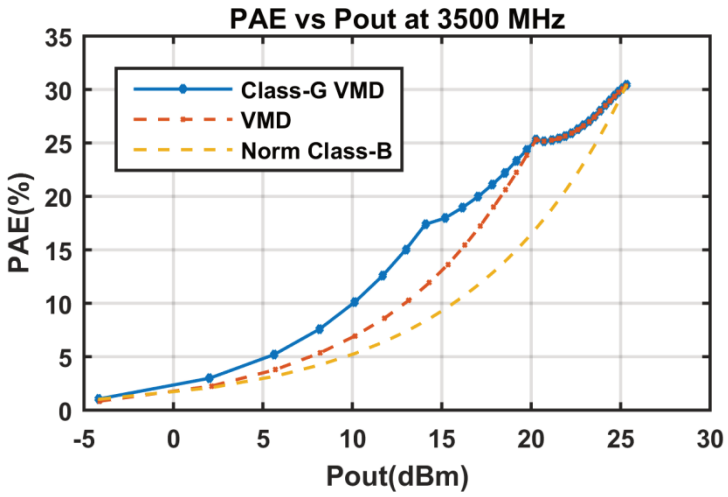


Figure 3.17 : Measured PAE vs Pout of CG-VMD at 3.5 GHz

For CW measurement, the ACW is swept and the output power and PAE are measured at different LO frequencies using a power meter. Fig. 3.17 shows the measured performance of CG-VMD at 3.5 GHz. The saturated power, peak PAE, 6 dB PAE and 12 dB PAE are 25.3 dBm, 30.4%, 25.3% and 17.4% respectively. Compared to normalized Class-B, this gives a 1.6x and 2.3x improvement in PAE at 6 dB and 12 dB back-off respectively. For comparison, the performance of a VMD is also measured (Fig. 3.17) using ACW of Fig. 3.9b. The CG-VMD improves efficiency beyond 6 dB back-off as expected (VMD with cascode driver would have slightly higher peak and 6 dB back-off efficiency due to smaller driver switching loss as

explained in section V.B). The measured performance across frequency from 2.9 GHz to 4.3 GHz is shown in Fig. 3.18, with 1 dB Psat fractional bandwidth of more than 38% and efficiency enhancement at both 6 dB and 12 dB back-off maintained across the band, compared to a conventional Doherty PA which has narrow back-off efficiency bandwidth [16]. The trap-rich high resistivity substrate variant was also measured (Fig. 3.18) and shows higher PAE as expected due to lower substrate loss, in agreement with our analysis in Fig. 3.12.

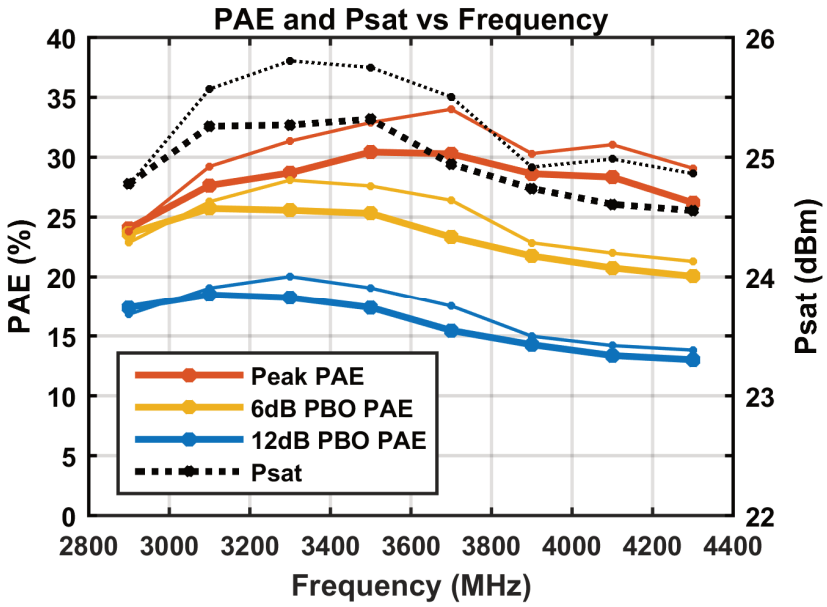


Figure 3.18 : Measured Psat and PAE at 0dB/6dB/12dB back-off across frequency. Results with low-resistivity and trap-rich high-resistivity substrates are shown in thick and thin lines, respectively.

The measured back-off PAE of the class-G VMD across frequency are plotted in Fig. 3.19 along with normalized class-B efficiency. The PA shows high efficiency enhancement at both 6 dB and 12 dB back-off over more than 1 GHz bandwidth.

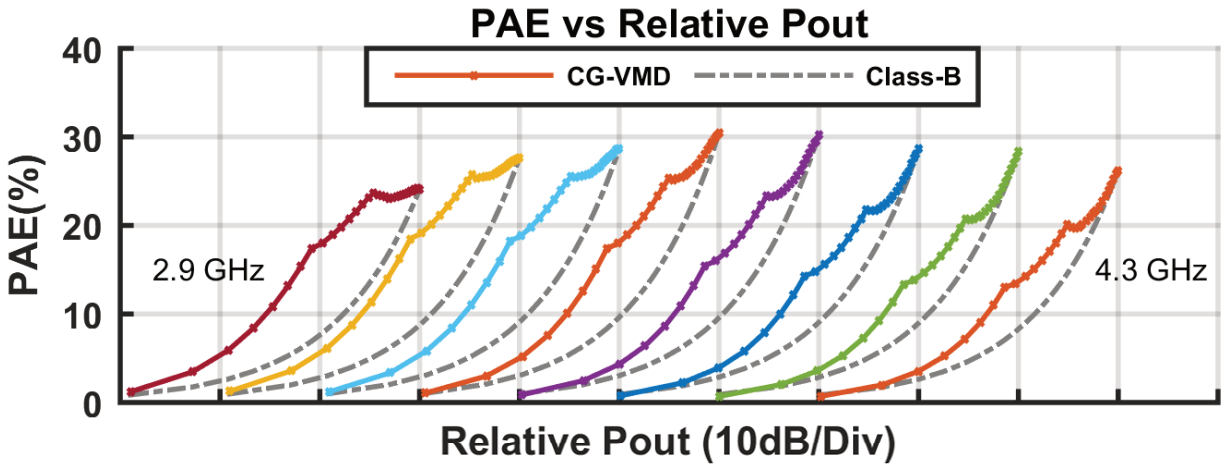


Figure 3.19 : Measured PAE back-off characteristics from 2.9 GHz to 4.3 GHz with 200 MHz step. Significant improvement over normalized class-B efficiency is observed over wide bandwidth.

3.6.2 Modulation Measurement

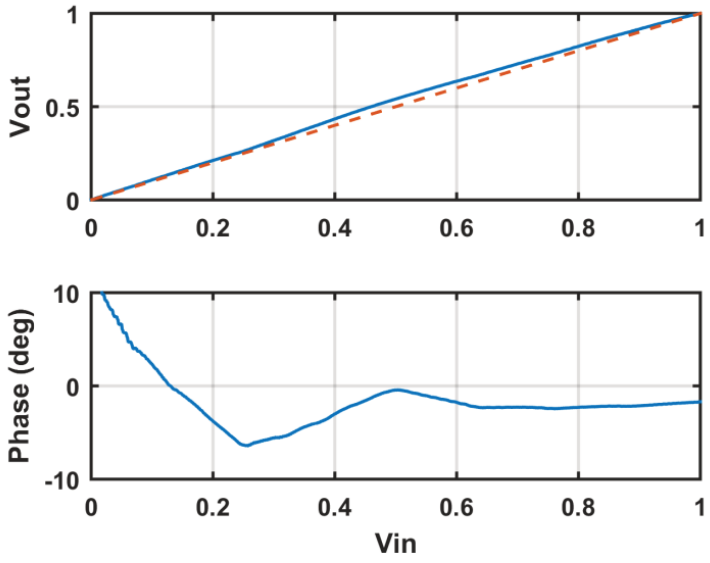


Figure 3.20 : Measured static AM-AM/PM of the PA at 3.5GHz. No discontinuity jump is observed at 6dB/12dB back-off.

For measurement of modulated data, the PA is linearized with memory-less 1024 element AM-AM and AM-PM look-up tables (LUTs); the number of elements can be significantly reduced with interpolation techniques without affecting the performance. Fig. 3.20 shows the measured AM-AM/-PM characteristics of the PA, generated by applying a 30 kHz AM signal with 100% modulation index centered at 3.5 GHz. At each carrier frequency, the LUT used to linearize the PA is generated in a similar manner, without any additional adaptation. Prior to linearization, the AM-AM/-PM characteristics are free of any discontinuities present in conventional mode-switching efficiency-enhanced PAs. The AM-PM variation is due to a difference in the delay of unit cells when operating at full and half supply respectively and can be improved with delay compensation over process corners.

3.6.2.1 Narrowband Modulation

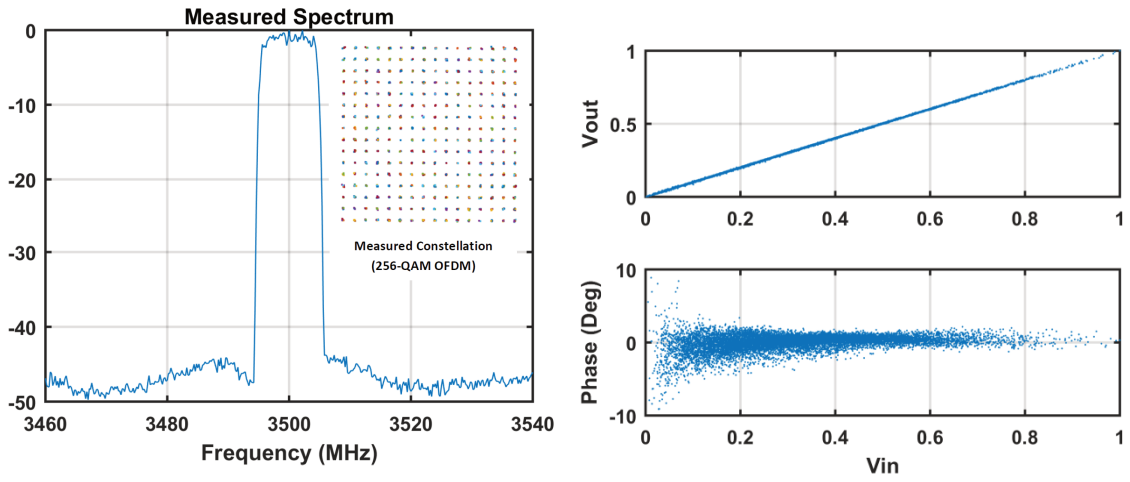


Figure 3.21 : Measured spectrum (500 kHz RBW), constellation, and dynamic AM-AM/PM of 10MHz 256-QAM OFDM with 8.2dB PAPR. The dynamic AM-AM/PM shows no glitch around 6dB/12dB back-off. The asymmetry in the spectrum is due to the measurement equipment reconstruction filter in the PM-LO path causing the distortion in polar architecture.

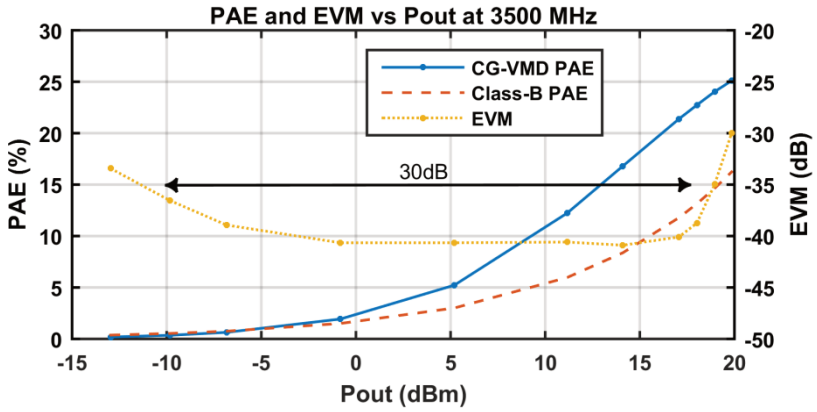


Figure 3.22 : Measured PAE and EVM of 10MHz 256-QAM OFDM at various transmit power levels.

With 10MHz 32-carrier 256-QAM OFDM with 8.2 dB PAPR, the PA achieves 17.1 dBm Pavg, -40.1 dB EVM, >45 dBc ACPR, and 21.4% PAE (Fig. 3.21), a more than a 1.8x improvement in efficiency compared to class-B back-off. The dynamic AM-AM/-PM of the PA are glitch free at 6 dB and 12 dB back-off as expected. Fig. 3.22 shows the trade-off between EVM and PAE as the transmit power is varied. Measurement shows that the PAE can be improved by intentionally clipping the signal in exchange for degraded linearity. In particular, the CG-VMD achieves 19 dBm, 24% PAE while maintaining the required EVM to transmit 256-QAM OFDM. Excellent EVM is achieved over a wide dynamic range demonstrating the robustness of this PA with non-adaptive memoryless linearization (linearized PAs often require adaptive LUTs to operate over a wide dynamic range). At very low power, the efficiency is limited by the LO distribution power, and the EVM is limited by quantization noise. Fig. 3.23 shows the efficiency and linearity of the PA when transmitting the 10 MHz 32 carrier 256-QAM OFDM signal at different frequencies. An efficiency enhancement of at least 1.7x is achieved while maintaining better than -38dB EVM over 1 GHz bandwidth.

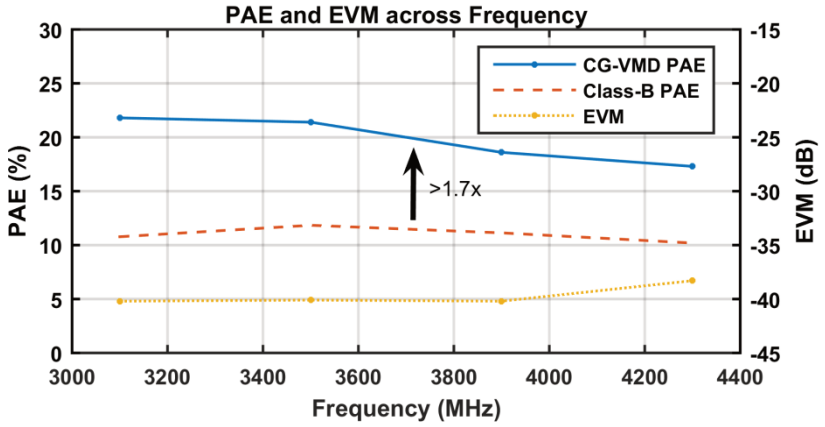


Figure 3.23 : Measured PAE and EVM of 10MHz 256-QAM OFDM across frequency. Low EVM of better than -38dB and efficiency enhancement of at least 1.7x is achieved over greater than 1 GHz bandwidth.

3.6.2.2 Wideband Modulation

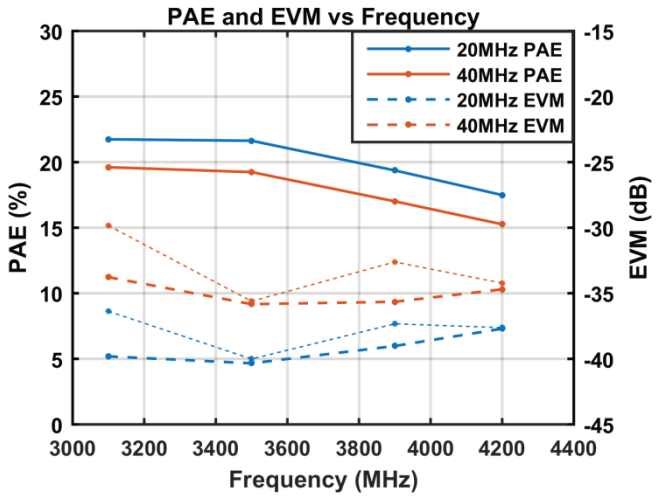


Figure 3.24 : PAE and EVM for 20 MHz / 40 MHz 256-QAM OFDM. For EVM, thin and thick lines indicate with and without receive amplitude equalization respectively.

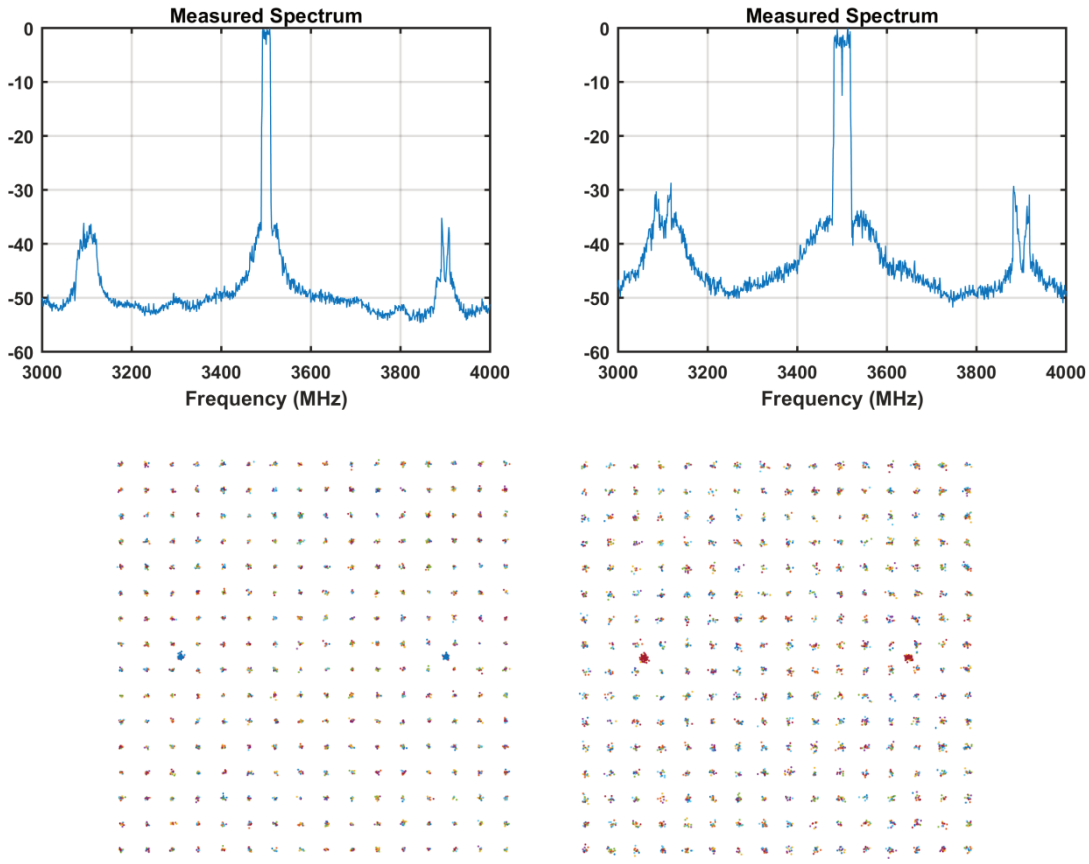


Figure 3.25 : Spectra (1 MHz RBW) and constellations for 256-QAM OFDM at 20 MHz (left) and 40 MHz (right).

For wideband modulation measurements, the RF-VSG is replaced by a 65GSa/s arbitrary waveform generator (Keysight M8195A) which directly generates the wideband PM-RF signal. A baseband sampling frequency of 400 MHz is used. Although the M8195A is synchronized to the PPG with 10 MHz reference, a slow carrier phase drift is observed which is calibrated out in the reported results. With trap-rich high-resistivity substrate, the PA achieved -40.3 dB / -35.8 dB EVM and 21.6%/19.2% PAE for 20 MHz / 40 MHz 256-QAM OFDM modulation with 8.8 dB / 10.1 dB PAPR at 3.5GHz (Fig. 3.24). The corresponding spectra and constellations are shown in Fig. 3.25, with measurement noise floor of better than -45dBc. The far-out spectrum is

limited by large ZOH replicas, making it difficult to conclusively demonstrate a glitch free far-out spectrum. An on-chip interpolation filter [17] would be required to move the replicas to a higher offset and demonstrate that far-out glitches do not exist. In the 40 MHz modulation measurement, the 802.11 mask is not quite met due to memory effects from the power supply decoupling network on the PCB. To support wider modulation bandwidth without significantly degrading modulation accuracy, the bypass capacitors would need to be moved closer to the chip and the supply/ground bondwires would need to be shorter.

Table 3.1 compares the performance of this PA to the current state-of-the art PAs with efficiency peaking beyond 6 dB back-off. The removal of mode-switching glitches enabled by the CG-VMD architecture allows for significant efficiency enhancement while maintaining excellent EVM without any further glitch mitigation technique. The efficiency can be further improved by migration to a finer linewidth CMOS process (higher f_{sw}) and reduced transformer loss using on-package transformer.

3.7 Conclusion

This work demonstrates the combination of voltage mode Doherty and class-G switched capacitor power amplifier achieving efficiency peaking at 6dB and 12dB back-off without introducing mode switching glitches present in conventional architectures. The absence of the glitches and the narrowband impedance inverter allow this architecture to achieve high efficiency with excellent EVM while transmitting high PAPR modulation over wide bandwidth. As the need for higher spectral efficiency continues, modulation is expected to have ever higher PAPR and required EVM, and the techniques presented in this work will help enable high efficiency transmitters in future standards.

3.8 Acknowledgement

The authors would like to thank GlobalFoundries for circuit fabrication and Integrand Software for use of an electromagnetics simulation tool (EMX).

Chapter 3, in full, is a reprint of the material as it appears in A Class-G Voltage-Mode Doherty Power Amplifier in IEEE Journal of Solid-State Circuits, vol. 52, no. 12, pp. 3348-3360, Dec. 2017. V. Vorapipat, C. S. Levy and P. M. Asbeck. The dissertation author was the primary investigator and author of this paper.

Table 3.1 : Comparison with CMOS PA with greater than 6dB back-off efficiency enhancement

	This Work			[11]	[12]	[13]
Frequency (GHz)	3.5			3.7	2.4	2.4
1dB Psat Bandwidth(%)	38			48	-	43
Psat (dBm)	25.3			26.7	27.7	31.5
CMOS Node (nm)	45 SOI			65	65	45
Supply Voltage	1.2/2.4			1.65/3	2.5/1.8/1.35/0.85	2.4
Peak/6dB/12dB PAE (%)	30.4/25.3/17.4			40.2/37.0/26.2†	45.1/42/20***	27/20/13***
Topology	Class-G Voltage Mode Doherty			Class-G Conventional Doherty	Multi-Level Outphasing	Dynamic Power Control Outphasing
Glitch	No glitch††			Supply switching, and PA input discontinuities.	Supply switching, outphasing angle discontinuities.	Outphasing angle and impedance discontinuities.
Glitch Mitigation	Not needed			None	Supply damping network	Skipping window
Wideband back-off efficiency enhancement	>1.7x over 1 GHz		>1.6x over 1 GHz	2 discrete frequencies shown (3.7 GHz and 4.3 GHz)	N/A	N/A
Modulation	**10 MHz 32 Carriers 1024-QAM**	**10 MHz 32 Carriers 256-QAM**	**40 MHz 802.11ac 256-QAM**	1 MHz Single-Carrier 16-QAM	20 MHz 802.11g 64-QAM	20 MHz 64-QAM WiFi
Pavg (dBm)	**14.8**	**17.1**	**15.6****	20.8	20.2	24.8
Output PAPR(dB)*	**10.5**	**8.2**	**10.1**	5.9	7.5	6.7
EVM (dB)	**-40.3**	**-40.1**	**-35.8**	-24	-31.4	-25
Average PAE(%)	**18.0**	**21.4**	**19.2****	28.8†	27.6	16
Matching Network	On-Chip			On-Chip	On-Package	On-Chip

*Output PAPR = Psat(dBm)-Pavg(dBm)
**Trap-rich high resistivity substrate
***Estimated from figure
†Drain Efficiency, not PAE
††LSB step glitch, as large as conventional RFDAC

3.9 References

[1] R. Pengelly, C. Fager and M. Ozen, "Doherty's Legacy: A History of the Doherty Power Amplifier from 1936 to the Present Day," in IEEE Microwave Magazine, vol. 17, no. 2, pp. 41-58, Feb. 2016.

[2] S. C. Cripps, RF Power Amplifiers for Wireless Communications, 2nd ed. Norwood, MA, USA: Artech House, 2006.

[3] W. H. Doherty, "A new high-efficiency power amplifier for modulated waves," in The Bell System Technical Journal, vol. 15, no. 3, pp. 469-475, July 1936.

[4] H. Chireix, "High Power Outphasing Modulation," in Proceedings of the Institute of Radio Engineers, vol. 23, no. 11, pp. 1370-1392, Nov. 1935.

[5] J. S. Walling, S. S. Taylor and D. J. Allstot, "A Class-G Supply Modulator and Class-E PA in 130 nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 44, no. 9, pp. 2339-2347, Sept. 2009.

[6] S.-M. Yoo, J. S. Walling, O. Degani, B. Jann, R. Sadhwani, J. C. Rudell, D. J. Allstot, "A class-G switched-capacitor RF power amplifier", IEEE J. Solid-State Circuits, vol. 48, no. 5, pp. 1212-1224, May 2013.

[7] M. Iwamoto, A. Williams, Pin-Fan Chen, A. G. Metzger, L. E. Larson and P. M. Asbeck, "An extended Doherty amplifier with high efficiency over a wide power range," in IEEE Transactions on Microwave Theory and Techniques, vol. 49, no. 12, pp. 2472-2479, Dec 2001.

[8] G. Liu, P. Haldi, T. J. K. Liu and A. M. Niknejad, "Fully Integrated CMOS Power Amplifier With Efficiency Enhancement at Power Back-Off," in IEEE Journal of Solid-State Circuits, vol. 43, no. 3, pp. 600-609, March 2008.

[9] H. Golestaneh, F. A. Malekzadeh and S. Boumaiza, "An Extended-Bandwidth Three-Way Doherty Power Amplifier," in IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 9, pp. 3318-3328, Sept. 2013.

[10] V. Vorapipat, C. S. Levy and P. M. Asbeck, "Voltage Mode Doherty Power Amplifier," in IEEE Journal of Solid-State Circuits, vol. 52, no. 5, pp. 1295-1304, May 2017.

[11] S. Hu, S. Kousai and H. Wang, "A Broadband Mixed-Signal CMOS Power Amplifier With a Hybrid Class-G Doherty Efficiency Enhancement Technique," in IEEE Journal of Solid-State Circuits, vol. 51, no. 3, pp. 598-613, March 2016.

[12] P. A. Godoy, S. Chung, T. W. Barton, D. J. Perreault and J. L. Dawson, "A 2.4-GHz, 27-dBm Asymmetric Multilevel Outphasing Power Amplifier in 65-nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 47, no. 10, pp. 2372-2384, Oct. 2012.

[13] W. Tai, H. Xu, A. Ravi, H. Lakdawala, O. Bochobza-Degani, L. Carley, Y. Palaskas, "A transformer-combined 31.5 dBm outphasing power amplifier in 45 nm LP CMOS with dynamic power control for back-off power efficiency enhancement", IEEE J. Solid-State Circuits, vol. 47, no. 7, pp. 1646-1658, Jul. 2012.

[14] S. Sehajpal, S. S. Taylor, D. J. Allstot and J. S. Walling, "Impact of Switching Glitches in Class-G Power Amplifiers," in IEEE Microwave and Wireless Components Letters, vol. 22, no. 6, pp. 282-284, June 2012.

[15] E. Kaymaksut and P. Reynaert, "Dual-Mode CMOS Doherty LTE Power Amplifier With Symmetric Hybrid Transformer," in IEEE Journal of Solid-State Circuits, vol. 50, no. 9, pp. 1974-1987, Sept. 2015.

[16] A. Cidronali, S. Maddio, N. Giovannelli and G. Collodi, "Frequency Analysis and Multiline Implementation of Compensated Impedance Inverter for Wideband Doherty High-Power Amplifier Design," in IEEE Transactions on Microwave Theory and Techniques, vol. 64, no. 5, pp. 1359-1372, May 2016.

[17] L. Ye, J. Chen, L. Kong, E. Alon and A. M. Niknejad, "Design Considerations for a Direct Digitally Modulated WLAN Transmitter With Integrated Phase Path and Dynamic Impedance Modulation," in IEEE Journal of Solid-State Circuits, vol. 48, no. 12, pp. 3160-3177, Dec. 2013.

[18] S. M. Yoo, J. S. Walling, E. C. Woo, B. Jann and D. J. Allstot, "A Switched-Capacitor RF Power Amplifier," in IEEE Journal of Solid-State Circuits, vol. 46, no. 12, pp. 2977-2987, Dec. 2011.

[19] A. Passamani, D. Ponton, E. Thaller, G. Knoblinger, A. Neviani and A. Bevilacqua, "13.9 A 1.1V 28.6dBm fully integrated digital power amplifier for mobile and wireless applications in 28nm CMOS technology with 35% PAE," 2017 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, 2017, pp. 232-233.

[20] V. Vorapipat, C. Levy and P. Asbeck, "2.8 A Class-G voltage-mode Doherty power amplifier," 2017 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, 2017, pp. 46-47.

[21] D. Chowdhury, S. V. Thyagarajan, L. Ye, E. Alon and A. M. Niknejad, "A Fully-Integrated Efficient CMOS Inverse Class-D Power Amplifier for Digital Polar Transmitters," in IEEE Journal of Solid-State Circuits, vol. 47, no. 5, pp. 1113-1122, May 2012.

[22] J. C. Pedro, L. C. Nunes and P. M. Cabral, "A Simple Method to Estimate the Output Power and Efficiency Load–Pull Contours of Class-B Power Amplifiers," in IEEE Transactions on Microwave Theory and Techniques, vol. 63, no. 4, pp. 1239-1249, April 2015.

[23] P. Haldi, D. Chowdhury, P. Reynaert, G. Liu and A. M. Niknejad, "A 5.8 GHz 1 V Linear Power Amplifier Using a Novel On-Chip Transformer Power Combiner in Standard 90 nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 43, no. 5, pp. 1054-1063, May 2008.

[24] C. D. Presti, F. Carrara, A. Scuderi, P. M. Asbeck and G. Palmisano, "A 25 dBm Digitally Modulated CMOS Power Amplifier for WCDMA/EDGE/OFDM With Adaptive Digital

Predistortion and Efficient Power Control," in IEEE Journal of Solid-State Circuits, vol. 44, no. 7, pp. 1883-1896, July 2009.

Chapter 4

Mode-Switching Glitch in Dynamic Reconfigurable PAs

In recent years, due to the widespread use of high PAPR modulation, several back-off efficiency enhancement methods have been proposed [1-5] in addition to the well-known techniques such as Doherty[6], Outphasing[7] and envelope tracking[8]. Most of these techniques were originally used for average power tracking [9-10] (APT) where the configuration of the PA occasionally change with average transmitted power to save power. The advantage of APT is its simplicity since the configuration of PA such as power supply and load impedance changes only occasionally and happened outside data transmission frame, the abrupt change in PA configuration is allowed and will not distort the transmitted signal or cause significant degradation in the transmitted spectrum. The drawback of APT is that it does not improve the efficiency of the PA when transmitting high PAPR modulation. Therefore, several attempts have been proposed to dynamically apply the efficiency enhancement techniques used in APT to improve the efficiency of the PA when transmitting high PAPR modulation. For example, dynamic class-G (supply switching)[3-4] and dynamic power combined Outphasing[2] changes the power supply/output combiner configuration of the PA according to the envelope of the transmitted signal to improve efficiency. The dynamic applications of APT efficiency

enhancement techniques have been shown to have a promising improvement in efficiency [2-4] when transmitting high PAPR modulation. However, one often overlooked issue is the increased distortion due to discontinuity glitch [5] which occurs when the configuration of the PA changes. In APT, the PA operates in different configuration called modes. For example, in class-G PA, the low/high supply mode is often called low/high power mode respectively. Therefore we will refer to the change in configuration of the PA as mode-switching in this work. Several works have mentioned the degradation of transmitted signal due to mode-switching. In [5], it is shown that the class-G power supply switching results in glitches that degraded noise floor and EVM of the transmitted signal. In [2], the transmitted spectrums of dynamic power combined PA can be significantly improved by skipping some of the mode-switching trading off the efficiency during the skipped mode transition. The goal of this work is to investigate the distortion caused by mode-switching glitches, its correction and comparison with the glitch-free architectures.

4.1 Mode-Switching Glitch

In general, mode switching glitch occurs when small change in signal causes a large discontinuity change in the PA configuration such as supply voltage and load impedance. The discontinuity change in power supply voltage is occurred in Class-G PA and the discontinuity change in load impedance occurred in output combiner reconfiguration PA. These two architectures will be discussed in detail in this section as it represent majority of the dynamic reconfigurable PA.

4.1.1 Class-G

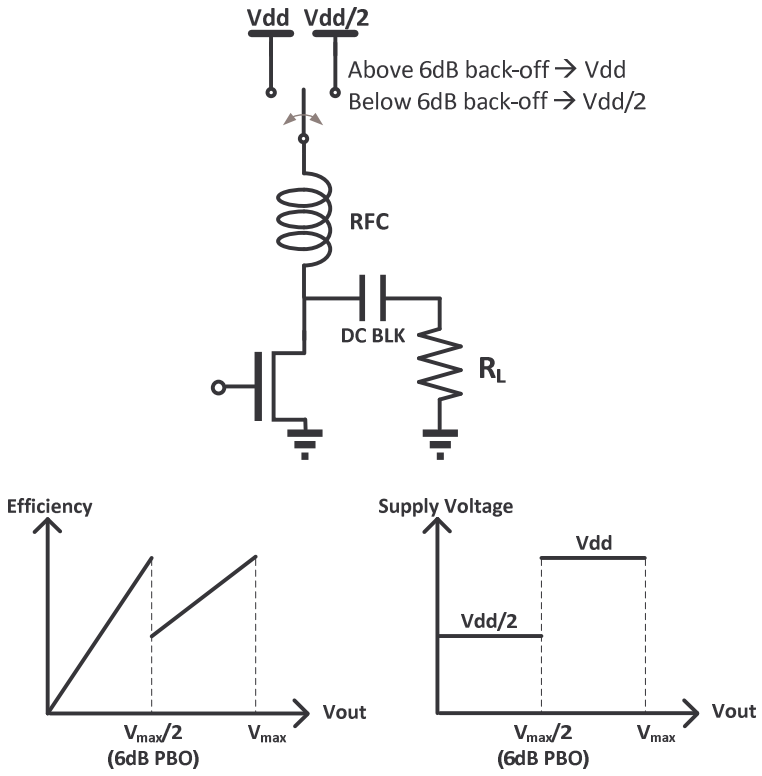


Figure 4.1 : Class-G PA and its operation

The class-G PA[5] is shown in figure 4.1, to achieve power saving, the class-G PA operate at low power supply when transmitting low power and switch to high power supply when transmitting high power. As a result of its operation, there is a discontinuity in its power supply at 6dB back-off. Since the DC voltage at the drain of the transistor cannot change instantaneously (due to parasitic drain capacitance), the glitch is unavoidable. Moreover the step change in current drawn from each power supply will cause significant ringing which further

worsen the distortion, in most class-G PAs the power supply damping network[3] must be used to suppress the power supply ringing to an acceptable level.

4.1.2 Power Combined Transformer Reconfiguration

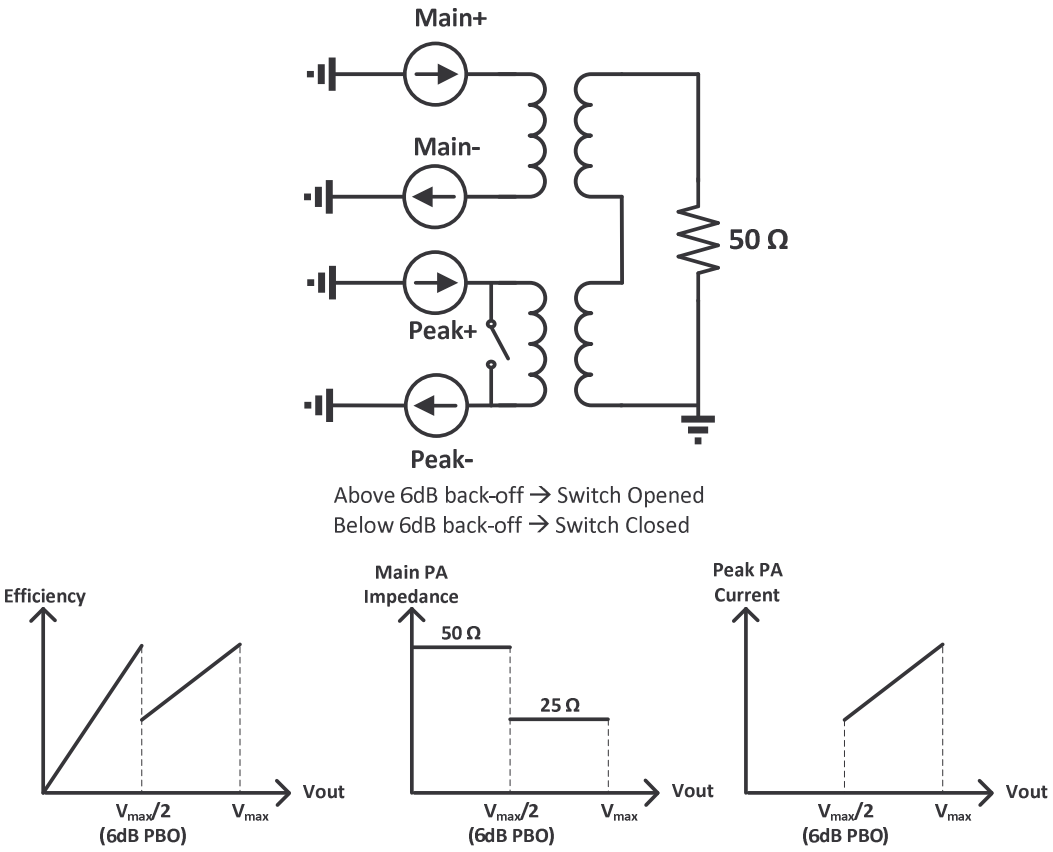


Figure 4.2 : Power Combined Transformer Reconfiguration PA and its operation

An example of power combined transformer reconfiguration PA[1] (XFMR-SW) is shown in figure 4.2, the switched is closed at low power to present high impedance to the main PA. The high impedance causes the PA operate closer to saturation and improved the efficiency. At high power, the switch is opened and the peak PA turned on such that its current match the

main PA, the impedance presented to the main PA is lowered allowing more power to be delivered to the load. It is clear from the operation that the glitch will occurs at 6dB back-off due to the discontinuity of impedance presented to the main PA and the imperfect timing of the RF switch at the transformer. Moreover since the efficiency also has step change at 6dB back-off, the current consumption of the PA is also discontinuous at 6dB back-off causing the power supply ringing similar to the class-G PA.

These two examples showed that the glitch is inevitable in dynamic reconfigurable PA due to the discontinuities at the mode-switching. The mode-switching glitch can now be defined as the deviation of the output signal from the steady state response. The glitch in dynamic power combined transformer reconfiguration (XFMR-SW) will be investigated in this work.

4.1.3 Effect of the mode-switching glitch on signal envelope

During mode-switching several step-changes in the PA configurations creates the glitch in the output signal. It has been shown in [5] that the severity of the glitch depends on both its magnitude and duration. Therefore, it is important to understand the dominant factor that contributes to mode-switching glitch in order to understand its effect in order to develop its correction. It turned out that the dominant factor of mode-switching glitch is the same for both Class-G and XFMR-SW architecture, the slow settling of the power supply. This is because while other factors such as power-supply switching and matching network reconfiguration can contribute to large glitch magnitude, its duration can be made small, usually in the order of RF cycles which is short compared to modulation symbol rate. The power supply settling on the other hand causes large glitch and can last relatively long making it a likely the dominant source of the mode-switching glitch.

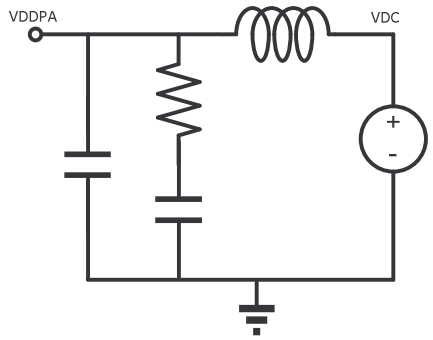


Figure 4.3 : Simplified Power Supply Network

A typical power supply network is shown in figure 4.3, the RC snubber is there to suppress the voltage/current ringing of the power supply. In a class-G PA, the PA switches between two power supplies when mode switching occurs. Independent of the direction of mode-switching, when the PA switches to a new supply it will cause the step current drawn from that power supply. Since the initial current of the power supply is zero and the current through the inductor cannot change instantaneously, we can conclude that the power supply of the PA momentarily go down right after the supply switching. The drop in power supply causes the envelope of the transmitted signal to momentarily drop as shown in figure 4.4 in agreement with the observation in [5].

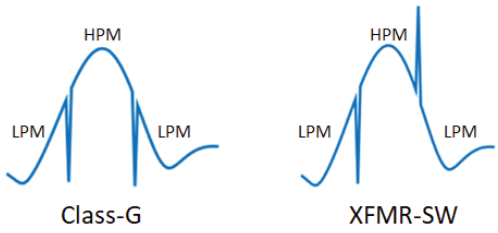


Figure 4.4 : Effect of Mode Switching on the Output Signal Envelope

For the XFMR-SW architecture, the PA always connected to the same power supply. First, let's consider the transition from low-power mode (LPM) to high-power mode (HPM). At this transition the PA transmit the same output power in steady state however with lower efficiency in HPM. The lower efficiency of HPM means that the PA will have a step increase in current consumption from the power supply. Since the current of inductor in figure 4.3 cannot change instantaneously, the supply voltage of the PA is expected to momentarily go down right after LPM to HPM mode switching. This results in negative glitch in the envelope as shown in figure 4.4b. At HPM to LPM transition, the opposite occur since the LPM is more efficient. The higher efficiency of LPM means that the PA will have a step decrease in current consumption from power supply. Since the inductor in figure 4.3 will still continue to deliver high current of HPM, the excess current will charge up the PA supply node to a higher value. This results in a positive glitch in the signal envelope as shown in figure 4.4.

4.2 Generating Mode-Switching Glitch

To enable the comparison between the glitch-prone technique of dynamic power combined transformer reconfiguration (figure 4.2) and the glitch-free technique of voltage-mode Doherty (VMD) [11], the two PAs should be similar in power level, implementation and measurement setup. Fortunately, the glitch in XFMR-SW PA can be emulated using discontinuous amplitude control word (ACW) in place of continuous ACW generally used in VMD in its normal operation. This enable the direct comparison since exactly the same PA and measurement setup is used. Figure 4.5 showed the VMD configured with XFMR-SW ACW and normal ACW respectively, it is clear from the figure that the XFMR-SW ACW emulate the impedance discontinuity at 6dB back-off as it appear in figure 4.2 and thus the glitch will be

expected. In the case of VMD ACW, the impedance is continuous and no glitch is expected. Note that the RF switch for XFMR-SW architecture in figure 4.2 is not required because the peak PA is a voltage source and present low impedance in place of the RF switch when off, this results in a “perfect” mode-switching timing and the lowest possible distortion.

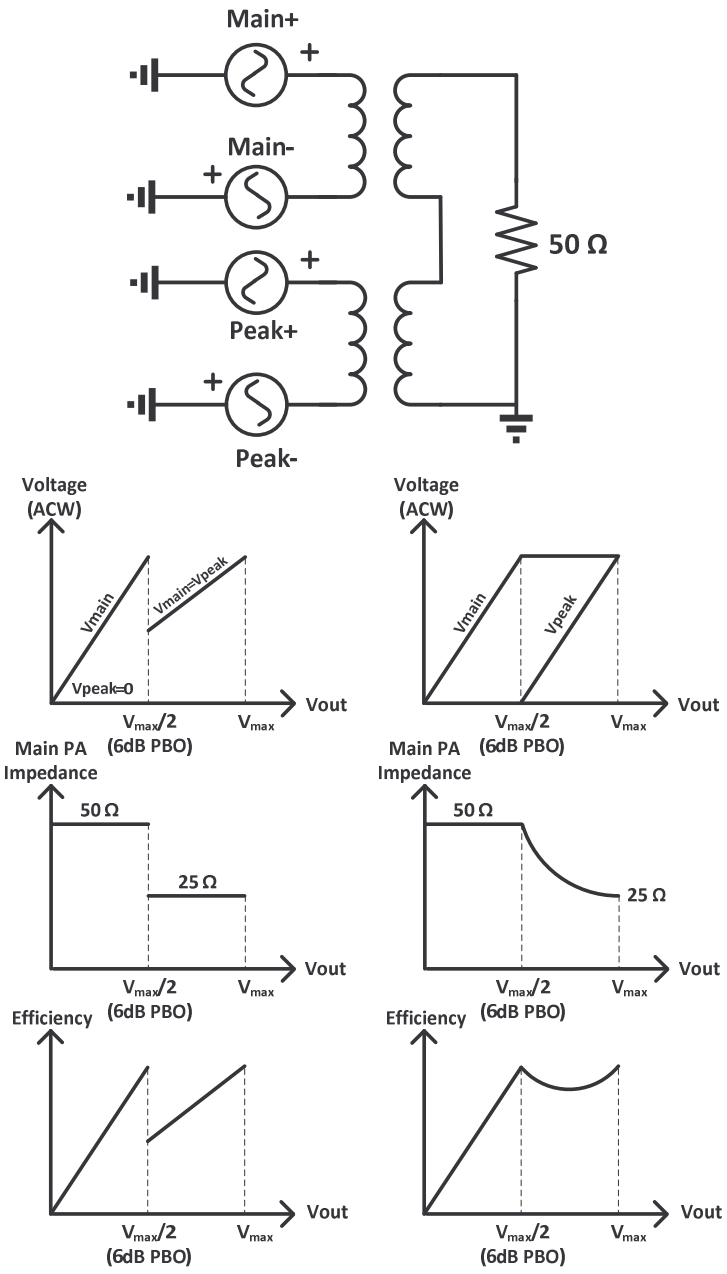


Figure 4.5 : Voltage-Mode Doherty with XFMR-SW ACW (left) and VMD ACW (right)

4.3 Glitch Measurement

The same PA and measurement setup in Chapter 3 [12] is used with the class-G functionality of the PA disabled. The VMD ACW and XFMR-SW ACW shown in figure 4.5 are used. The transmit signal is the 10 MHz OFDM modulation with 9.2dB PAPR centered at 3500MHz. The transmitter baseband sampling frequency is 200MHz and the IQ demodulator bandwidth is 160MHz with 200MHz sampling frequency. The lower power supply of 1V/2V is used to protect the transistor device from the overvoltage of mode-switching glitch as analyzed in section 4.1.3.

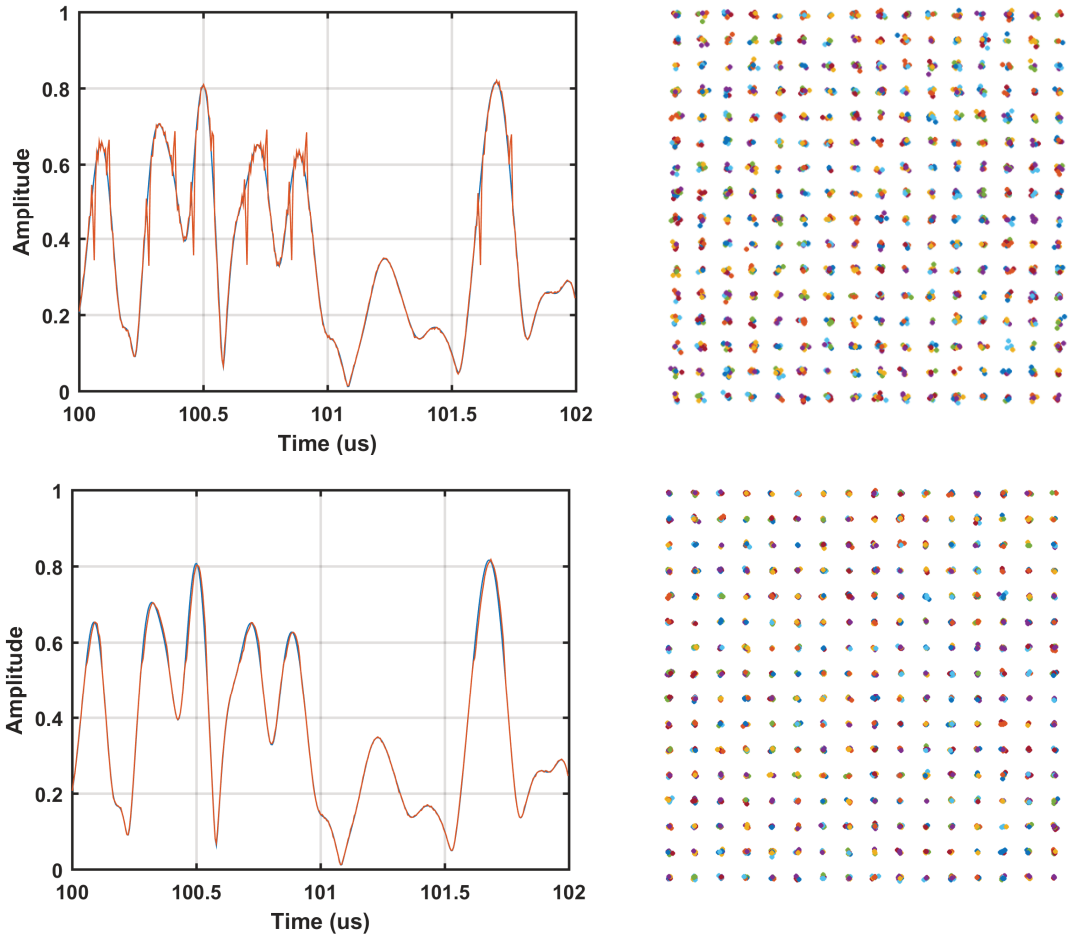


Figure 4.6 : Measured envelope and constellation for XFMR-SW (top) and VMD (bottom)

The measured signal envelope (figure 4.6) clearly showed the glitch in XFMR-SW which occurred due to mode-switching at 6dB back-off. The glitches for LPM to HPM and HPM to LPM mode transitions are negative and positive respectively consistent with the prediction in figure 4.4. Further analysis showed that the glitches are predictable; the LPM to HPM and HPM to LPM has normalized magnitude of 0.228/0.139 with rms error of 0.009/0.008 respectively. This predictability of the glitch enabled the possibility of correction discussed in the next section. Even though these glitch pulses are very short compared to data symbol rate, its spectrum is wideband which not only degrade the spectrum of the transmit signal but also the transmit constellation. The EVM performance of the PA is degraded by 6dB from -41.3dB in VMD to -35.3dB in XFMR-SW. To confirm the effect of the glitch, the negative/positive glitch of magnitude of 0.228/0.139 is added to the measured glitch-free VMD signal at the expected mode-transition of XFMR-SW architecture. This results in EVM of -35.8dB which is very close to the measured result with in 0.5dB.

4.4 Glitch Modelling and Correction

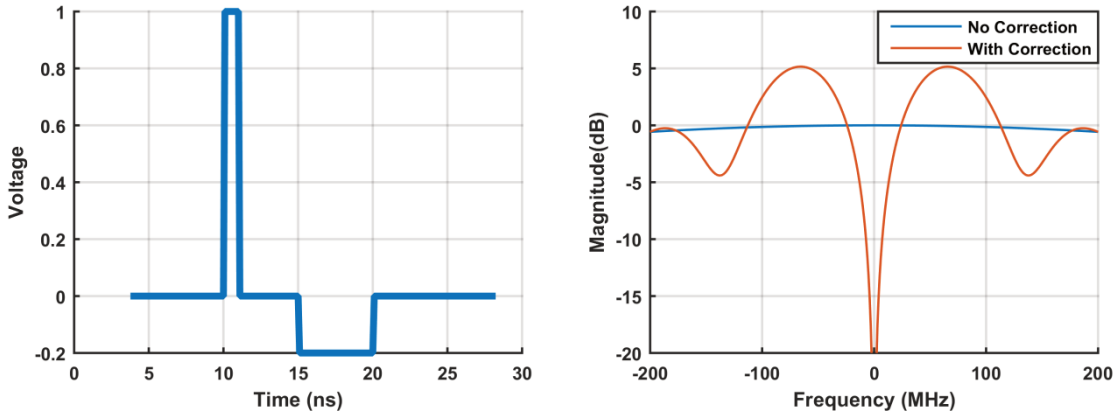


Figure 4.7 : Time domain glitch correction and its corresponding frequency domain.

The mode-switching glitches observed in figure 4.6 are positive and negative narrow spikes depending on the direction of mode the transition. Due to the predictability of the glitch magnitude and direction, it is possible to cancel it with spike of the same magnitude with opposite direction. Since the baseband down-converter has limited IQ bandwidth of 160MHz and 200MHz sampling rate, we may conclude that the glitch pulses are narrower than 5ns. Since the glitch pulse is expected to be much narrower than the TX baseband modulator sampling frequency of 200MHz, we have no way of perfectly reconstruct the glitch pulse and cancel it. The realistic glitch cancellation is to use delayed, much wider pulse to cancel the glitch pulse as shown in figure 4.7. The glitch is cancelled by the wider pulse of equal area with opposite sign, this make sure that perfect cancellation is achieved at DC, the delay and difference in pulse shape limit the achievable cancellation bandwidth. The frequency domain of the corrected glitch (figure 4.5) showed perfect cancellation at DC with more than 10dB cancellation up to +/- 10 MHz which is more than sufficient for 10MHz modulation used in the study. In addition to imperfect cancellation, different pulse shape and delay also cause out-of-band peaking which will increase the out-of-band distortion. In general, as long as the glitch and glitch correction pulse does not overlap, the glitch correction will improve in-band distortion but worsen out-of-band distortion. This is due to the increase in overall distortion energy when the glitch correction pulse is added in time domain. Since the energy is conserved, the glitch correction shaped the distortion energy out of the band in frequency domain. The distortion energy can be reduced by using smaller magnitude and wider pulse of equal area for glitch correction; this however will reduce the cancellation bandwidth due to worse pulse shape mismatch and longer delay.

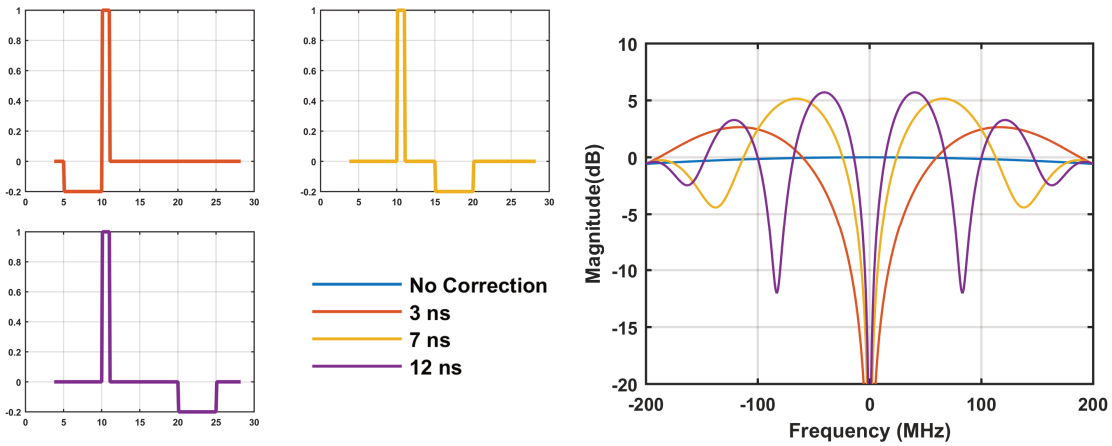


Figure 4.8 : Effect of delay on glitch correction.

The effect of delay on glitch correction is shown in figure 4.8. The glitch pulse is 1ns and the correction pulse is 5ns in all cases, the only difference is the delay. From the spectra, it is clear that the shorter delay results in wider bandwidth correction which is as expected. The additional benefit of short delay is the lower close-in out-of-band distortion (the total distortion energy are the same in all cases) which is desirable since the far-out out-of-band distortion is usually suppressed by the bandpass characteristic of the PA. It is clear that the shortest delay cancellation pulse shown in the top left of figure 4.8 should be used, however due to the constraint of the system it is not always possible. In our case, the LPM to HPM mode-switching the glitch pulse is negative and using the top left of figure 4.8 for glitch cancellation would results in amplitude higher than 6dB back-off in LPM which is impossible. For HPM to LPM mode-switching, it will introduce memory effect which is beyond the scope of this work. Due to the constraint of the system, the glitch cancellation shown in top right of figure 4.8 will be used.

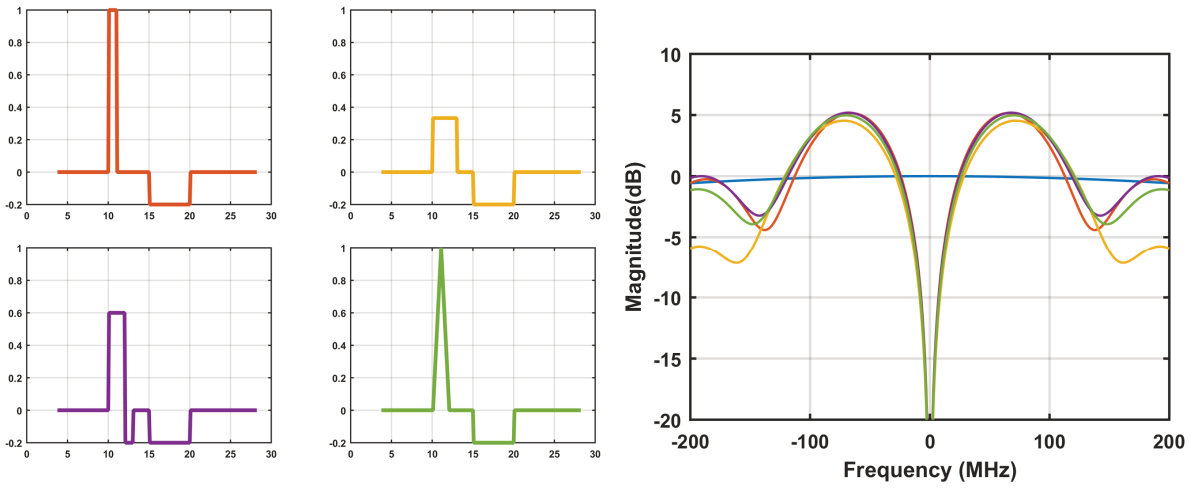


Figure 4.9 : Effect of glitch pulse shape on glitch cancellation.

Thus far, the glitch pulse shape is assumed to be 1ns rectangular pulse. In reality, the pulse shape is not known due to the limited capture bandwidth of the receiver. The pulse shape may have effect on the glitch cancellation. Figure 4.9 showed the glitch cancellation for different glitch pulse shape of equal area. The result clearly showed that the in-band cancellation is insensitive to the glitch pulse shape; this is as expected because the low frequency spectrum of the glitch pulse is constant as long as the pulse is very short and has the same area.

Since the glitch pulse shape does not matter and the delay should be minimized for cancellation, the glitch cancellation pulse in figure 4.7 will be used which is to apply the 5ns correction pulse in the sample right after the sample where glitch has occurred. The only two unknowns are the magnitude of these correction pulses, A_{LH} for LPM to HPM mode-switching and A_{HL} for HPM to LPM mode-switching.

4.5 Glitch Correction Measurement

In this part of the measurement, the glitch correction pulse is applied to the baseband transmit signal. The value A_{LH} and A_{HL} are varied until the minimum EVM is reached, the A_{LH} and A_{HL} effect on EVM are independent making the optimum value converges quickly. A few iterations are required as the each value effect the EVM floor of the other. The training signal was used and the (A_{LH}, A_{HL}) = (0.33, -0.23) gives the minimum EVM. The optimum magnitude of A_{LH} and A_{HL} are higher than predicted by our earlier glitch measurement, this is because the actual glitch correction pulse will be smaller than the programmed A_{LH} and A_{HL} due to finite bandwidth of the PA and power supply network.

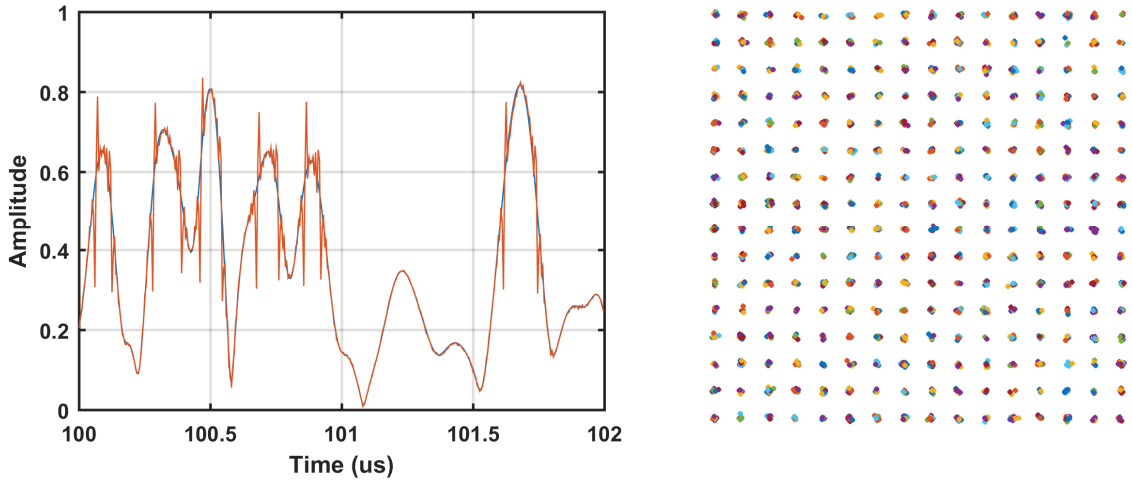


Figure 4.10 : Measured envelope and constellation after glitch correction.

Figure 4.10 showed the measured result of the glitch correction for the modulation used in figure 4.6. The measured envelope plot clearly shows the glitch pulse immediately followed by the correction pulse. The EVM of the modulation was significantly improved from -35.3dB to

-39.2dB; the parameter (A_{LH}, A_{HL}) for minimum still remains the same which confirm the validity and robustness of this glitch correction approach. Due to the robustness of the glitch cancellation observed in the measurement, offline calibration should be sufficient for its operation.

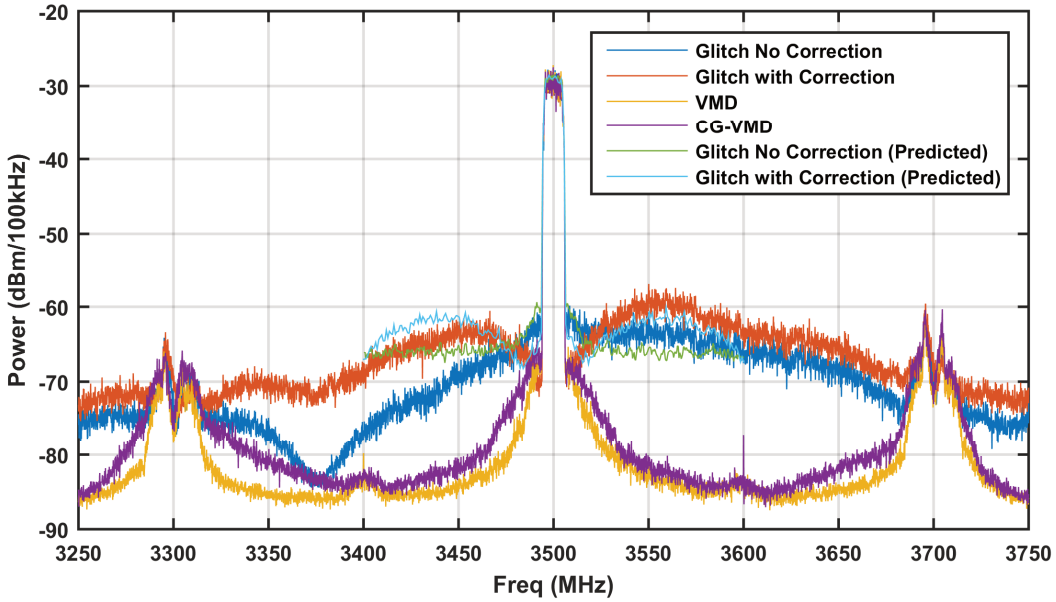


Figure 4.11 : Measured spectra of dynamic reconfigurable PA (XFMR-SW) and the glitch-free PA (VMD and CG-VMD)

The measured spectra showed that the distortion due to mode-switching glitch significantly increased the noise floor. The glitch correction technique shaped the distortion out-of-band but increased overall noise floor as expected. The spectra clearly showed the advantage of glitch-free architecture of VMD[11] and CG-VMD[12] which gives excellent EVM and has much lower noise floor than dynamic reconfigurable PA architecture. The measured spectra for XFMR-SW case agree well with the theory both before and after correction. The discrepancy

between the theory and measurement is likely due to the phase distortion from mode switching glitch which is not modelled in the theory.

Table 4.1 : Measurement Summary for 10MHz OFDM signal centered at 3.5GHz

	[12]*				[4]	[3]	[2]	[1]
Frequency (GHz)	3.5				3.7	2.4	2.4	2.2
Psat (dBm)	24.1				26.7	27.7	31.5	23.3
CMOS Node (nm)	45 SOI				65	65	45	65
Supply Voltage (V)	1.0/2.0				1.65/3	2.5/1.8/1.35 /0.85	2.4	1.2
Peak PAE (%)	35				40.2	45.1	27	43
Topology	XFMR -SW	XFMR-SW	VMD	CG-VMD	Glitchy Class-G Doherty	Multi-Lvl Class-G Outphasing	Dynamic Power Control Outphasing	XFMR-SW
Glitch Mitigation	No	DSP	No glitch	No glitch	No	Supply Damping Network	Skipping Window	Supply Damping Network
Modulation	10 MHz 32 Carriers OFDM				1 MHz Single Carrier	20 MHz 802.11g	20 MHz 802.11g	20 MHz 802.11g
Pavg (dBm)	14.9				20.8	20.2	24.8	16.8
Output PAPR (dB)	9.2				5.9	7.5	6.7	6.5
EVM(dB)	-35.3	-39.4	-41.3	-40.1	-24	-31.4	-25	-28
Average PAE (%)	19	19	19.4	23.3	28.8	27.6	16	21.8
*Trap rich hi-res substrate version operated at reduced supply voltage								

4.6 Conclusion

This work investigate the glitch in dynamic power combined reconfiguration PA, the measurement result confirm the existence of mode switching glitch which distorts the transmit signal. The method for in-band glitch cancellation which improved the transmit signal EVM is discussed and validated. It can be concluded that the in-band distortion due to mode-switching glitch can be corrected at the expense of higher out-of-band distortion. This makes it difficult for the PA with mode-switching glitch to be used in FDD system where the stringent Rx band noise is required. As the modulation accuracy requirement and the bandwidth of modern modulation increases, it will be increasingly difficult to use the efficiency enhancement techniques that generate glitch as the glitch duration will become comparable to the symbol rate. The measured EVM and spectrum of the VMD and CG-VMD showed much lower noise floor compared to the architecture with mode-switching glitch. This confirms the absence of glitch in our VMD and CG-VMD work, making them viable for current and future modulation format.

4.7 Future Work

4.7.1 Hardware-Level Glitch Correction

The limitation of the DSP approach for glitch correction is the limited time resolution which leads to relatively narrow correction bandwidth and increased out-of-band distortion. If the narrow pulse comparable to the glitch can be generated right when the glitch occurred, a wideband glitch cancellation is possible. Figure 4.12 show a conceptual circuit that can correct the glitch. Its operation followed from the discussion in section 4.1.3. At LPM to HPM transition

in XFMR-SW architecture, the PA has step increase in current causing a momentarily drop in VDDPA which leads to the glitch. The drop in VDDPA can be corrected by switching V_{corr} from low to high such that the charge in the capacitor Cc replenish the charge loss at VDDPA node mitigating the momentarily drop in VDDPA. If the capacitor value Cc and the rise time is properly tuned, it is possible to cancel most of the mode-switching glitch. A similar principle applies for HPM to LPM transition, by switching VCorr from high to low.

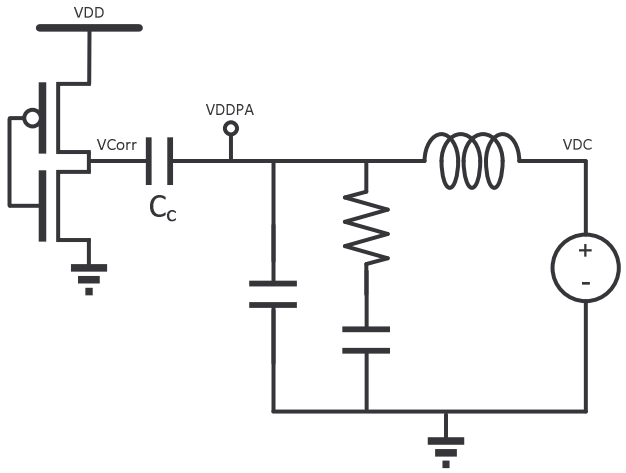


Figure 4.12 : Glitch Correction Circuit.

4.8 References

[1] L. Ye, J. Chen, L. Kong, E. Alon and A. M. Niknejad, "Design Considerations for a Direct Digitally Modulated WLAN Transmitter With Integrated Phase Path and Dynamic Impedance Modulation," in IEEE Journal of Solid-State Circuits, vol. 48, no. 12, pp. 3160-3177, Dec. 2013.

[2] Wei Tai, Hongtao Xu, Ashoke Ravi, Hasnain Lakdawala, Ofir Bochobza-Degani, L. Richard Carley and Yorgos Palaskas, "A Transformer-Combined 31.5 dBm Outphasing Power Amplifier in 45 nm LP CMOS With Dynamic Power Control for Back-Off Power Efficiency Enhancement," in IEEE Journal of Solid-State Circuits, vol. 47, no. 7, pp. 1646-1658, July 2012.

[3] P. A. Godoy, S. Chung, T. W. Barton, D. J. Perreault and J. L. Dawson, "A 2.4-GHz, 27-dBm Asymmetric Multilevel Outphasing Power Amplifier in 65-nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 47, no. 10, pp. 2372-2384, Oct. 2012.

[4] S. Hu, S. Kousai and H. Wang, "A Broadband Mixed-Signal CMOS Power Amplifier With a Hybrid Class-G Doherty Efficiency Enhancement Technique," in IEEE Journal of Solid-State Circuits, vol. 51, no. 3, pp. 598-613, March 2016.

[5] S. Sehajpal, S. S. Taylor, D. J. Allstot and J. S. Walling, "Impact of Switching Glitches in Class-G Power Amplifiers," in IEEE Microwave and Wireless Components Letters, vol. 22, no. 6, pp. 282-284, June 2012.

[6] W. H. Doherty, "A New High Efficiency Power Amplifier for Modulated Waves," in Proceedings of the Institute of Radio Engineers, vol. 24, no. 9, pp. 1163-1182, Sept. 1936.

[7] H. Chireix, "High Power Outphasing Modulation," in Proceedings of the Institute of Radio Engineers, vol. 23, no. 11, pp. 1370-1392, Nov. 1935.

[8] Feipeng Wang, A. H. Yang, D. F. Kimball, L. E. Larson and P. M. Asbeck, "Design of wide-bandwidth envelope-tracking power amplifiers for OFDM applications," in IEEE Transactions on Microwave Theory and Techniques, vol. 53, no. 4, pp. 1244-1255, April 2005.

[9] E. Kaymaksut and P. Reynaert, "Dual-Mode CMOS Doherty LTE Power Amplifier With Symmetric Hybrid Transformer," in IEEE Journal of Solid-State Circuits, vol. 50, no. 9, pp. 1974-1987, Sept. 2015.

[10] G. Liu, P. Haldi, T. J. K. Liu and A. M. Niknejad, "Fully Integrated CMOS Power Amplifier With Efficiency Enhancement at Power Back-Off," in IEEE Journal of Solid-State Circuits, vol. 43, no. 3, pp. 600-609, March 2008.

[11] V. Vorapipat, C. S. Levy and P. M. Asbeck, "Voltage Mode Doherty Power Amplifier," in IEEE Journal of Solid-State Circuits, vol. 52, no. 5, pp. 1295-1304, May 2017.

[12] V. Vorapipat, C. S. Levy and P. M. Asbeck, "A Class-G Voltage-Mode Doherty Power Amplifier," in IEEE Journal of Solid-State Circuits, vol. 52, no. 12, pp. 3348-3360, Dec. 2017.

Chapter 5

Conclusions

5.1 Research Summary

The high PAPR of high spectral efficiency modulations used in recent communication standards leads to poor efficiency of the RF transmitter. This is because the efficiency of high efficiency linear PAs like class-B PAs degrades by half for every 6dB back-off in power. A modern modulation with a typical PAPR of 12dB would leads to sub 20% average efficiency in an ideal class-B PA. This has motivated the development of several efficiency enhancement techniques, notably the Doherty PA, which is widely used for basestations and will likely become a preferred choice for handsets in the near future. A well-known issue for Doherty PAs is narrow bandwidth due to the impedance inverter used in the implementation. Several researches have tried unsuccessfully to eliminate the impedance inverter. This is due to the current source characteristics of the building-block PAs, which require an impedance inverter to achieve back-off efficiency enhancement.

In the first part of this dissertation, the impedance inverter used in a Doherty PA is eliminated by using building-block PAs with voltage source characteristics. The Voltage Mode Doherty PA achieved similar back-off efficiency enhancement to the classical Doherty PA without

the narrowband impedance inverter, resulting in wide bandwidth in term of output power, peak efficiency and back-off efficiency. The Voltage Mode Doherty PA is implemented in 65 nm low-leakage CMOS and achieves 24 dBm saturated power with 45%/34% PAE at peak and 5.6dB back-off over 750 MHz to 1050 MHz 1dB bandwidth. With memory-less linearization, this PA can transmit 40 MHz 256-QAM 9dB PAPR 802.11ac modulation signals centered at 900 MHz, meeting the spectral mask for the 802.11ac standard with measured EVM of -34.8dB and 22% PAE without backing-off or equalization. Compared to other published CMOS Doherty PA works, this PA provides similar efficiency enhancement but with a much wider bandwidth.

The typical back-off efficiency enhancement range of the Doherty PA is about 6dB, and the Voltage Mode Doherty implemented in the first part of this dissertation achieved about 5.6dB. However typical modern modulation signals have PAPR of more than 10dB, therefore the transmitter efficiency can be further improved by extending the back-off efficiency enhancement range of the PA. In the second part of the dissertation, the Voltage Mode Doherty PA is combined with the Class-G Switched Capacitor PA to achieved efficiency enhancement range of about 12dB, which is very well suited to modern modulation standards. This is done without introducing the mode-switching glitch present in most hybrid architectures reported to date. The combined techniques allow the Class-G Voltage Mode Doherty to achieve excellent EVM while maintaining high efficiency. Moreover, since both Voltage Mode Doherty and Class-G Switch Capacitor PA have wide bandwidth, the efficiency enhancement is maintained over wide bandwidth. The Class-G Voltage Mode Doherty PA is fabricated in 45-nm CMOS SOI with integrated balun for power combining and matching. At 3.5 GHz a saturated output power of 25.3 dBm is measured with 30.4%/25.3%/17.4% power added efficiency (PAE) at 0/6/12 dB back off. With memoryless, nonadaptive linearization, the PA achieves 19.2% PAE with −35.8 dB error vector magnitude

(EVM) while transmitting a 40 MHz 256-QAM 10.1 dB PAPR 802.11ac modulation. Significant efficiency improvement compared to class-B and EVM better than −34 dB is maintained over more than 1 GHz bandwidth. Compared to other published hybrid PA architectures, the absence of glitching allowed this PA to achieve a much better EVM while maintaining high efficiency over a wide bandwidth.

The absence of mode-switching glitch is mentioned in the first and second part of the dissertation as a key to achieving excellent EVM and ACPR. The third part of the dissertation investigates the cause of mode-switching glitch and how it affects the transmit signal. This part of the dissertation showed that the dominant cause of the glitch comes from the step in current from the power supply when the PA switches between high and low power modes, which results in a negative envelope spike in class-G PAs and positive/negative spikes in dynamic output combiner reconfiguration PAs. Since the PAs implemented in the first and second parts of the dissertation do not have large discontinuity in their configurations as the output power level changes and thus do not generate supply current steps, the mode-switching glitch is avoided. The effect of the glitch on the transmit signal is also investigated. Due to the signal-dependent quasi-random occurrence of mode-switching and narrow glitch spikes, the in-band and close-in out-of-band distortion has flat frequency response and the far out-of-band distortion is shaped by the glitch pulse shape, which is specific to the PA implementation. It is also shown that the in-band distortion can be reliably corrected at the cost of higher out-of-band distortion. Overall, the glitch significantly increases the transmit noise floor of the PA. The investigation of the glitch confirms the absence of the glitch in the PA implemented in the first and second part of the dissertation and demonstrates the advantage of glitch-free architecture.

5.2 Future Work

5.2.1 Current-Voltage Doherty

The original idea of Voltage Mode Doherty comes from the modification of Current-Voltage Doherty in Doherty's original work. To the authors best knowledge, the current-voltage Doherty PA was never implemented. This architecture may have advantages in some applications.

5.2.2 Outphasing with Voltage Source PA

To date, most implementations of Outphasing PAs have been implemented with current source PAs driven into saturation. This leads to several drawbacks including reliability, difficulty in power control and non-ideal output power vs phase difference characteristics. Using a true voltage source PA can allow a reliable implementation of Outphasing PAs with the capability of simple power control.

5.2.3 Quadrature Implementation of Voltage Mode Doherty

The Voltage Mode Doherty was implemented in this dissertation with polar architecture. A resulting drawback is increased difficulty in input signal generation, which has bandwidth expansion in both amplitude and phase relative to I / Q input signals. A quadrature implementation would simplify the signal generation and allow simple all-digital implementation while maintaining reasonable efficiency (although lower than for the polar implementation).

5.2.4 Voltage Source PA implementation with Non-Complementary Device

Currently known implementations of voltage source PAs require complementary device pairs These are readily available as NMOS and PMOS in CMOS processes. The process technologies for high power PAs such as GaAs and GaN do not have complementary devices with similar performance. Therefore, being able to implement voltage source PAs without complementary devices would allow implementation of Voltage Mode Doherty PAs at higher power than achievable with CMOS.

5.2.5 Digital Replica Improvement

One of the issues in RFDAC architecture is the presence of digital replicas at multiples of the baseband sampling frequency. This is due to the zeroth-order hold characteristics of the RFDAC, which make the signal deviate from the intended waveform. The baseband sampling rate is often limited by the chip-to-chip data rate, which is constrained by power consumption and pin count. Therefore, to suppress the digital replicas, an on-chip interpolation filter or replica cancellation techniques are required. This issue is very critical for FDD systems where the distortion in the received band (at LNA input) must be below the thermal noise floor.