University of California
Santa Barbara

Integrated Electronics for Energy-Efficient Direct and Coherent Detection in Data Center Optical Interconnects

A dissertation submitted in partial satisfaction
of the requirements for the degree

Doctor of Philosophy
in
Electrical and Computer Engineering

by

Luis A. Valenzuela

Committee in charge:

Professor James Buckwalter, Chair
Professor Clint Schow
Professor Mark Rodwell
Professor Loai Salem

March 2022

The Dissertation of Luis A. Valenzuela is approved.

Professor Clint Schow

Professor Mark Rodwell

Professor Loai Salem

Professor James Buckwalter, Committee Chair

February 2022

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For my wife, Mari,
and my parents, Luis and Angelica

Acknowledgements

First, I would like to thank my advisor Prof. Jim Buckwalter. It has been a real privilege to have been a member of Jim's research group: the RF and Mixed-Signal Integrated Systems Lab for nearly six years. I can write many things, but I believe best way to describe what kind of advisor Jim is by recalling a time we worked on a paper together on Overleaf well past midnight while he was on vacation.

I would also like to thank Prof. Clint Schow. Although he was not officially my PI, he spent a lot of time and effort helping me throughout countless problems. I always felt comfortable enough to crash his office at random times for questions or updates on an exciting measurement results. I anticipate I will continue to do the same over email.

I would also like to thank the rest of my committee, Prof. Mark Rodwell and Prof. Loai Salem for their time and feedback.

I would also like to thank my colleagues at the RF and Mixed-Signal Integrated Systems Lab - including those who have since graduated: Navid Hosseinzadeh, Kang Ning, Hussam Al'shammary, Cameron Hill, Hector Andrade, Mayank Singh, Ahmed Hamza, Ghazal Movaghar, Rohit Reddy Karnaty, Andrea Arias, Everett O'malley, Jeff Chien, Jonathan Tao, Shu-Ming Chang, James Dalton, Eythan Lam, and Wonho Lee. I cannot proceed without a special shout-out to the folks that I have had the privilege of sharing offices with: Cameron Hill, Ahmed Hamza, Mayank Singh, Hussam Al'Shammary, Navid Hosseinzadeh, Ghazal Movaghar, Navid Hosseinzadeh, Ainhoa Rezola, and Andrea Arias. We spent countless hours together and had many conversations that I will always remember. Of this group, I would like to especially thank Navid Hosseinzadeh, my first unofficial group mentor who was always available to answer my many unfiltered questions. I still have the urge today to go over a post-layout simulation with you so you can point out where I butchered the EM simulation setup!

The folks in the Schow Lab were an extension of my immediate research group. I have had the privilege of closely collaborating with Aaron Maharry, Yujie Xia, Takako Hirokawa, and Junqian Liu in the OTC lab. Throughout the early part of the COVID pandemic, Aaron Maharry and Yujie Xia were just about the only people I saw in-person at UCSB for what seemed like almost a year!

There are people that helped me a great deal during my undergraduate days at Cal Poly Pomona that really helped push me toward a career in research. From Cal Poly Pomona, I would like to thank Prof. Alexander Rudolph, Prof. James Kang, Prof. Phyllis Nelson, Prof. Winny Dong and the McNair Scholars community. REUs solidified my decision to pursue graduate research. To this end, I would like to thank my REU advisors, Dr. Virginia Gulick from the SETI Institute and Prof. Ruonan Han from MIT. I will always be grateful for their mentorship and guidance.

I am very grateful to the Diaz family, especially Adriana and Andrea. Adriana, thank you for being the best mother-in-law I could have asked for. You are missed every day.

This acknowledgement would not be complete without mention of my family. Pa, your journey from Cartagena continues to inspire me. I'm writing this thesis now because of the decades you spent working before dawn to put food on my plate. Ma, I've never felt lost in my life because I knew you were always behind me. My siblings, Chris, Damian, and Brianna get a special shout-out for making sure that a day at home is always full of laughter.

Finally, I want to thank the love of my life, Mari. You have been through so much in the last several years, and even through the chaos, you were, inexplicably, always there for me in the pursuit of my dreams. Your endless love and support is the muse of my thesis, and I am in awe of you every single day. You've been by my side as my friend during high school, my girlfriend during undergrad, and as my wife through grad school. I am so grateful to know that the next chapter of my life will be with you.

Curriculum Vitæ

Luis A. Valenzuela

Education

2022	Ph.D. in Electrical and Computer Engineering, University of California, Santa Barbara.
2019	M.S. Electrical and Computer Engineering, University of California, Santa Barbara.
2015	B.S. in Electrical and Computer Engineering, California State Polytechnic University, Pomona.

Journal Publications

(J-1) **L. A. Valenzuela**, Y. Xia, A. Maharry, H. Andrade, C. L. Schow and J. F. Buckwalter, "A 50-GBaud QPSK Optical Receiver with a Phase/Frequency Detector for Energy-Efficient Intra-data Center Interconnects," in IEEE Open Journal of the Solid-State Circuits Society, doi: 10.1109/OJSSCS.2022.3150291.

(J-2) **L. A. Valenzuela**, A. Maharry, H. Andrade, C. L. Schow and J. F. Buckwalter, "Energy Optimization for Optical Receivers Based on a Cherry-Hooper Emitter Follower Transimpedance Amplifier Front-end in 130-nm SiGe HBT Technology," in Journal of Lightwave Technology, vol. 39, no. 23, pp. 7393-7405, Dec.1, 2021, doi: 10.1109/JLT.2021.3115403.

(J-3) T. Hirokawa, S. Pinna, N. Hosseinzadeh, A. Maharry, J. Liu, T. Meissner, S. Misak, G. Movaghar, **L. A. Valenzuela**, Y. Xia, S. Bhat, F. Gambini, J. Klamkin, A. A. M. Saleh, L. Coldren, J. F. Buckwalter, and C. L. Schow, "Analog Coherent Detection for Energy Efficient Intra-Data Center Links at 200 Gbps Per Wavelength," in Journal of Lightwave Technology, vol. 39, no. 2, pp. 520-531, 2021, doi: 10.1109/JLT.2020.3029788.

(J-4) H. Andrade, A. Maharry, T. Hirokawa, **L. Valenzuela**, S. Pinna, S. Simon, C. L. Schow, and J. F. Buckwalter, "Analysis and Monolithic Implementation of Differential Transimpedance Amplifiers," in Journal of Lightwave Technology, vol. 38, pp. 4409-4418, 2020, doi: 10.1109/JLT.2020.2990107.

Conference Publications

(C-1) **L. A. Valenzuela**, N. Hosseinzadeh, G. Movaghar, J. Dalton, A. Maharry, H. Andrade, C. L. Schow and J. F. Buckwalter, "An Energy-Efficient, 60-Gbps Variable Transimpedance Optical Receiver in a 90-nm SiGe HBT Technology," accepted for presentation at the 2022 IEEE/MTT-S International Microwave Symposium (IMS), 2022.

(C-2) **L. A. Valenzuela**, J. Dalton, A. Maharry, G. Movaghar, H. Andrade, C. L. Schow and J. F. Buckwalter, "An 80-Gbps Distributed Driver with Two-tap Feedforward Equalization in 45-nm CMOS SOI" 2022 IEEE 22th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF), 2022, pp. 1-3.

(C-3) H. Andrade, A. Maharry, **L. Valenzuela**, N. Hosseinzadeh, C. Schow and J. Buckwalter, "An 8.2-pJ/bit, 56 Gb/s Traveling-wave Modulator Driver with Large Reverse Terminations," 2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), 2021, pp. 1-4, doi: 10.1109/BCICTS50416.2021.9682462.

(C-4) H. Andrade, Y. Xia, A. Maharry, **L. Valenzuela**, J. F. Buckwalter and C. L. Schow, "50 GBaud QPSK 0.98 pJ/bit Receiver in 45 nm CMOS and 90 nm Silicon Photonics," 2021 European Conference on Optical Communication (ECOC), 2021, pp. 1-4, doi: 10.1109/ECOC52684.2021.9606026.

(C-5) A. Maharry, **L. A. Valenzuela**, H. Andrade, I. Kalifa, I. Cestier, M. Galanty, B. Atias, A. Sandomirsky, E. Mentovich, L. Coldren, J. F. Buckwalter, and C. L. Schow,"A 50 Gbps 9.5 pJ/bit VCSEL-based Optical Link," 2021 IEEE Photonics Conference (IPC), 2021, pp. 1-2, doi: 10.1109/IPC48725.2021.9592905.

(C-6) Y. Xia, **L. Valenzuela**, A. Maharry, S. Pinna, S. Dwived, T. Hirokawa, J. Buckwalter, and C. Schow, "A Fully Integrated O-band Coherent Optical Receiver Operating up to 80 Gb/s," 2021 IEEE Photonics Conference (IPC), 2021, pp. 1-2, doi: 10.1109/IPC48725.2021.9592881.

(C-7) A. Maharry, **L. A. Valenzuela**, J. F. Buckwalter and C. L. Schow, "A PCB Packaging Platform Enabling 100+ Gbaud Optoelectronic Device Testing," 2021 IEEE 71st Electronic Components and Technology Conference (ECTC), 2021, pp. 1323-1328, doi: 10.1109/ECTC32696.2021.00214.

(C-8) **L. A. Valenzuela**, A. Maharry, H. Andrade, C. L. Schow and J. F. Buckwalter, "A 108-Gbps, 162-mW Cherry-Hooper Transimpedance Amplifier," 2020 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), 2020, pp. 1-4, doi: 10.1109/BCICTS48439.2020.9392928.

(C-9) **L. A. Valenzuela**, H. Andrade, N. Hosseinzadeh, A. Maharry, C. L. Schow and J. F. Buckwalter, "A 2.85 pJ/bit, 52-Gbps NRZ VCSEL Driver with Two-Tap Feedforward Equalization," 2020 IEEE/MTT-S International Microwave Symposium (IMS), 2020, pp. 209-212, doi: 10.1109/IMS30576.2020.9223818.

(C-10) N. Hosseinzadeh, K. Fang, **L. Valenzuela**, C. Schow and J. F. Buckwalter, "A 50-Gb/s Optical Transmitter Based on Co-design of a 45-nm CMOS SOI Distributed Driver and 90-nm Silicon Photonic Mach-Zehnder Modulator," 2020 IEEE/MTT-S International Microwave Symposium (IMS), 2020, pp. 205-208, doi: 10.1109/IMS30576.2020.9223845.

(C-11) H. Andrade, A. Maharry, T. Hirokawa, **L. Valenzuela**, S. Simon, C. L. Schow, and J. F. Buckwalter "Comparison of three monolithically integrated TIA topologies for

50 Gb/s OOK and PAM4", Proc. SPIE 11286, Optical Interconnects XX, 112860W (28 February 2020).

Awards

2016 UCSB Doctoral Scholars Fellowship

Abstract

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Data centers are the pillars of modern internet infrastructure that have enabled the proliferation of emerging cloud applications, social media, and artificial intelligence, among others that are becoming increasingly integrated into our every day lives. As data center traffic continues growing at a compound annual growth rate exceeding 25% with internal server-to-server traffic accounting for well over 70% of the total, engineering increased capacity through optical intra-data center interconnects (IDCIs) is essential. In keeping up with capacity demands, energy efficiency improvements are required conserve the data center energy footprint. The performance of IDCIs are thus primarily characterized by two metrics: capacity defined in bits-per-second and energy efficiency defined as the cost of energy-per-bit.

This dissertation will broadly cover the design and measurement results of energy-efficient front-end receiver integrated circuits (RXICs) and transmitter integrated circuits (TXICs) for high data rate IDCIs.

In Part I of this thesis, a comprehensive benchmarking approach for optical receivers with implications for link power consumption in both direct and coherent detection-based links will be introduced. For direct detection links, RXIC designs operating up to 64 Gbps at less than 2.53 pJ/bit will be presented and compared with the state of the art. For coherent detection links, an I-Q Costas-based optical RXIC operating up to 100 Gbps at less than 5.34 pJ/bit will be discussed and compared to the state-of-the-art. The RXICs

are implemented in 130 nm SiGe HBT technology.

Part II of this thesis will investigate the energy efficient implementations of two-tap feedforward equalizers (FFEs) for high-speed optical TXICs in direct- and external-modulation schemes. For directly modulated, Vertical Cavity Surface Emitting Laser (VCSEL) transmitters, a TXIC implemented in 130 nm SiGe HBT technology is reported for data rates up to 60 Gbps at an energy efficiency less than 2.85 pJ/bit. For externally modulated, Mach Zehnder Modulator (MZM) transmitters, a TXIC implemented in 45 nm CMOS SOI technology is reported for data rates up to 80 Gbps at an energy efficiency less than 3.9 pJ/bit.

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Chapter 1

Introduction

Global data center traffic has grown at a compound annual growth rate of global data center traffic was 27% from 2016-2021 [1]. With the emergence of internet-based big data and cloud applications, artificial intelligence, and even the "metaverse" being floated, it is evident that there is no end in sight to the growth in demand for increasing data.

With inevitable growth, the biggest obstacle then becomes the managing the energy consumption footprint. In the last decade, energy forecasts have projected the potential for the electricity demand of the information and communication technology (ICT) sector to make up to make up nearly 21% of global electricity demand by the year 2030 [2] [3]. As these forecasts have indicated that data centers and wired networks have taken a more prominent role in the ICT sector's energy footprint with the expectation of further growth, a more recent study of the relative change between 2018 and 2010 of global data center energy-use drivers has demonstrated that energy efficiency improvements (i.e. average PUE, server energy intensity, number of servers per workload, and storage drive energy use) have maintained pace with increased installed storage capacity, IP traffic, workloads/compute instances, and installed base of servers [4]. Notably, the impact of efficient optical interconnects and network architecture have not been extensively studied

on a large scale in global data center energy efficiency surveys.

The optical interconnects that manage internal server-to-server data center traffic - often referred to as East-West traffic within the data center- presents an attractive research thrust to continue addressing simultaneous capacity and efficiency improvements in the data center for many reasons. First, East-West traffic accounted for well over 71% of overall global cloud data center traffic in 2018 and has been projected to continue growing [1]. Second, the number of interconnects in a large scale data center amount up to hundreds of thousands [5], indicating an energy consumption footprint that can be profound with unchecked efficiency. Third, optical interconnects, in pluggable modules with standardized form-factors or through co-packaged optics with high level of integration with the network switches, offer a path toward improving data center energy efficiency in a modular fashion without the need for a ground-up overhaul of physical data center infrastructure or network architecture.

Thus, to further improve energy efficiency within the data center, the Advanced Research Projects Agency - Energy, U.S. Department of Energy has kicked off the ENergy-efficient Light-wave Integrated Technology Enabling Networks that Enhance Dataprocessing (ENLITENED) program in 2017 to develop novel data center network topologies enabled by integrated photonics technologies [6].

1.1 INTREPID Platform as a Solution to Capacity and Effiency Demands of Future Intra-Data Center Interconnects

The INTREPID project, of the broader ARPA-E ENLITENED program, investigates the two-pronged research thrust of intra-data center optical interconnects and data center

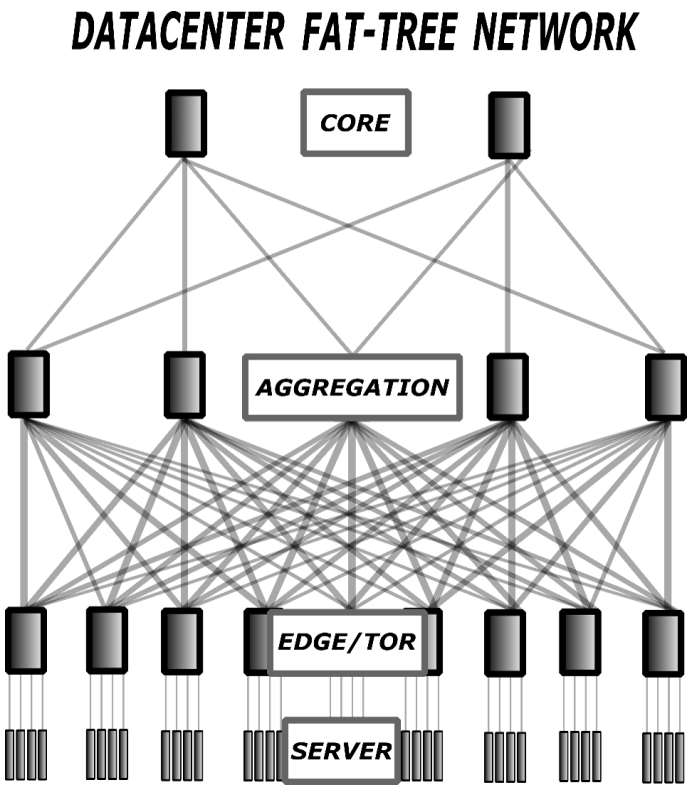


Figure 1.1: Illustration of data center fat tree network.

network architecture. The common workhorse network architecture used in data centers is called the fat tree network and is illustrated in Figure 1.1 [7]. The conventional fat tree network consists of three switching layers: (1) the edge/top-of-rack (TOR), (2) aggregation, and (3) core switching layers.

The INTREPID platform proposes optical interconnects (1) below the TOR switching layer comprised of short-reach (i.e. 3 m) multi-mode fiber-based direct detection links using Vertical Cavity Surface Emitting Lasers (VCSELs) operating at 850 nm to replace existing electrical I/O, and (2) above the TOR switch - below the core switch - as mid-reach (less than 2 km) single-mode fiber-based analog coherent detection links in the O-band (i.e. 1310 nm) [8–12]. Notably, at the switch end, there is promise for co-packaged optical modules which can offer greater efficiency improvements through tighter integration of the switch ASIC and optical interconnect modules.

Although in-depth discussions regarding the redesign of the network architecture remain out of the scope of this thesis, it is sufficient to highlight a path that may be undertaken in the design of future data center network architectures, namely, the use of higher radix switching through optical switching. Larger radix switches flatten the network by removing layers of hierarchy while simultaneously supporting a large number of interconnected servers allowing for significant improvements in efficiency and latency [8–10]. Large radix switches have been explored using optical switches as an alternative solution to existing electrical switches [13]. In order to enable the use of optical switching in the data center network, there is an additional requirement for increased unallocated link budget due to switching losses which make existing intensity-modulated direct-detection (IM-DD) based solutions unsuitable [11]. Analog coherent has been presented as a viable alternative to address the unallocated link budget bottleneck for existing IM-DD solutions [11].

1.2 Thesis Objectives and Organization

This thesis will broadly cover the design and measurement results of energy-efficient analog front-end receiver and transmitter integrated circuits for high data rate optical interconnects in two parts and the presented works will be compared to the state-of-the-art to qualify their merits.

The first part of the thesis encompasses the receiver integrated circuits (RXICs) of the optical interconnect. First, a new optical receiver benchmark for direct- and coherent detection is proposed, and RXIC designs are explored in both direct- and coherent detection links.

Chapter 2 introduces link efficiency considerations and proposes a figure of merit for comprehensive benchmarking of optical receivers. The optical receivers presented in

this thesis are benchmarked using this updated graphical figure of merit with the state of the art. The material of this chapter were previously published in part in the IEEE/OSA Journal of Lightwave Technology [14] ©2021 IEEE and in the IEEE Open Journal of the Solid State Circuits Society [15].

Chapter 3 discusses the design and measurement of two RXIC variants based on a Cherry-Hooper front-end, Gilbert-cell variable gain amplifier (VGA) intermediate stage, and a 50 Ω output buffer with passive bandwidth extension techniques. The material of this chapter was previously published in part in the 2020 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium [16] ©2020 IEEE and the IEEE/OSA Journal of Lightwave Technology [14] ©2021 IEEE.

Chapter 4 presents the design and measurement of an I-Q optical receiver with a QPSK Costas-based phase-frequency detector intended for analog coherent links. The material of this chapter has been published in part in the IEEE Open Journal of the Solid State Circuits Society [15].

Chapter 5 discusses the design of a novel variable transimpedance amplifier design. The material of this chapter has been accepted for presentation to the 2022 IEEE International Microwave symposium ©2022 IEEE.

Chapter 6 concludes Part I and demonstrates the future work.

The second part of the thesis encompasses the transmitter integrated circuits (TXICs) of the optical interconnect. Novel equalization architectures are explored in multi-mode and single-mode fiber optical links.

Chapter 7 introduces a novel consolidated output driver and equalizer design intended for Mach-Zehnder Modulator-based optical transmitters. The material of this chapter has been published in part in the 2022 IEEE 22th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF) [17] ©2022 IEEE.

Chapter 8 introduces a novel driver and equalizer design intended for vertical-cavity

surface-emitting lasers (VCSELs). The material of this chapter has been published in part in the 2020 IEEE International Microwave Symposium [18] ©2020 IEEE.

Chapter 9 concludes Part II and demonstrates the future work.

Part I

Receiver Integrated Circuits (RXICs) for Optical Interconnects

Chapter 2

An Optical Receiver Integrated Circuit Benchmark with Implications to Link Power Minimization

Link power optimization will be explored in this chapter for direct detection in 2.1.1 and coherent detection in 2.1.4. A case study on shunt-feedback TIAs in direct detection links will be discussed in Section 2.1.2 for both HBT and FET technologies. A second case study will describe common-base andcommon-gate TIAs in direct detection links in Section 2.1.3. Following the analyses, a novel optical receiver survey which points to the trends in the state-of-the-art in optical receiver designs across various technology platforms will introduced in 2.2.

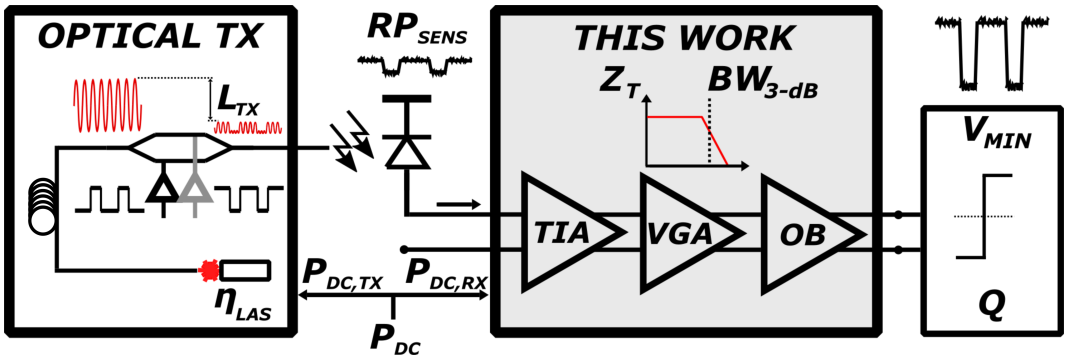


Figure 2.1: Block diagram of a DCI link and sources of power consumption in the link

2.1 Energy Minimization of Optical Receivers based on Figures of Merits (FOMs) and Noise Performance

This section is in part a reprint of material published in the following manuscripts; "Energy Optimization for Optical Receivers based on a Cherry-Hooper Emitter Follower Transimpedance Amplifier Front-end in 130-nm SiGe HBT Technology," published in the IEEE Journal of Lightwave Technology [14] ©2021 IEEE, and "A 50-GBaud QPSK Optical Receiver with a Phase/Frequency Detector for Energy-Efficient Intra-data Center Interconnects," published in the IEEE Open Journal of the Solid-State Circuits Society [15].

2.1.1 Direct-detection

An optical receiver (ORX) converts the optical input power into a voltage for sampling, ideally near minimum power consumption. The total power consumption of a short-range DCI link, discounting the transmitter electronics, includes the optical power required to provide a minimum sensitivity at the receiver, P_{SENS}, and the DC power

required to amplify the signal to a minimum required output voltage eye opening, V_{MIN}, given the link BER and Q-factor requirement. We assume in this case that the transmitter can be characterized by the wall-plug efficiency of a laser, η_{LAS}, and the passive optical losses introduced by the transmit modulator, L_{TX}, as might be encountered with a Mach-Zehnder or ring modulator. The total power consumption of the link is

$$P_{DC} = P_{DC,TX} + P_{DC,RX}, \tag{2.1}$$

where $P_{DC,TX} = \frac{P_{SENS}L_{TX}}{\eta_{LAS}}$. The first term captures the power consumption to generate and modulate the optical carrier in terms of the sensitivity at the receiver while the second term is the RX power consumption, which will subsequently attempt to characterize.

A common figure of merit (FOM) for the ORX amortizes the transimpedance bandwidth by the DC power consumption [19].

$$FOM_{BW} = \frac{R_T \cdot BW}{P_{DC,RX}} \tag{2.2}$$

FOM_{BW} is useful in circuit simulations and measurement comparisons and, notably, has units of $\frac{Hz}{A^2}$. However, the limitation of FOM_{BW} is that it discounts the noise contribution of the ORX or ability to reach a BER. To address the latter issue, a more practical metric would use data rate, rather than the bandwidth, based on a desired bit-error rate (BER). Often, the bit rate BR is related to the BW by a rule of thumb bandwidth such as 0.7. However, at higher frequency, the photodiode and interconnects complicate the application of this rule of thumb. Therefore, we could alternately define

$$FOM_{BR} = \frac{R_T \cdot BR}{P_{DC}}. \tag{2.3}$$

The units of this FOM are $\frac{Hz}{bit \cdot A^2}$. Still, either FOM is ultimately incomplete since it does

not include other critical specifications such as sensitivity due to the noise contributions of the TIA, the harmonic distortion in the case of PAM modulation, and gain control.

To account for sensitivity, we can recast (2.25) in terms of optical link parameters. First, the sensitivity is calculated from

$$P_{SENS} = \frac{2Qi_{n,rms}}{\mathcal{R}}, \tag{2.4}$$

where Q is based on the required bit error rate (BER), $i_{n,rms}$ is the input rms current, $\mathcal{R}$ is the responsivity of the photodetector. The P_{SENS} can also be related to the required amplification in the ORX according to $V_{MIN} = P_{SENS}\mathcal{R}R_T$, where R_T is the transimpedance of the ORX. Therefore, total DC power can be recast in terms of these link parameters.

$$P_{DC} = \frac{2QL_{TX}}{\mathcal{R}\eta_{LAS}} i_{n,rms} + \frac{V_{MIN}BW}{2QFOM_{BW}} \frac{1}{i_{n,rms}}. \tag{2.5}$$

To minimize the DC power consumption, there exists an optimum rms noise for the ORX.

$$i_{n,rms,OPT} = \sqrt{\frac{\eta_{LAS}\mathcal{R}V_{MIN}BW}{4Q^2L_{TX}FOM_{BW}}}. \tag{2.6}$$

and the minimum DC power is

$$P_{DC,MIN} = 2\sqrt{\frac{L_{TX}V_{MIN}BW}{\mathcal{R}\eta_{LAS}FOM_{BW}}}. \tag{2.7}$$

As expected, the DC power increases as the link loss, minimum sampling voltage, or bandwidth increases. Revisiting the optimum rms noise current, we define the average

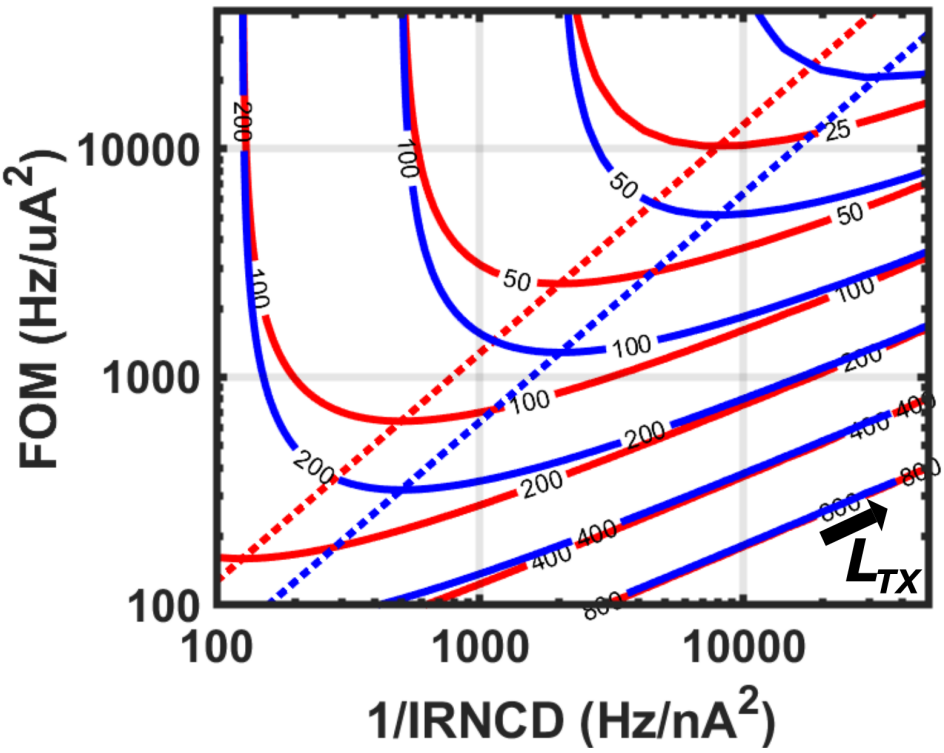


Figure 2.2: Link power minimization as a function of FOM and IRNCD for $L_{TX} = 20$ dB (red) and 23 dB (blue), $\eta_{LAS} = 0.25$, $\mathcal{R} = 1$, $V_{min} = 0.1$, $BW_{3-dB} = 40$ GHz and $Q = 7$. Constant DC power contours are indicated in the red and blue curves (mW). The minimum power occurs at 2.5 mW for $L_{TX} = 20$ dB and 3.6 mW for $L_{TX} = 23$ dB.

input-referred noise current density (IRNCD) by amoritizing (2.6) against the bandwidth.

$$IRNCD = \frac{i_{n,rms}^2}{BW} \tag{2.8}$$

Using this definition, the product of the optimal IRNCD and FOM obeys

$$IRNCD_{OPT}FOM_{BW} = \frac{\eta_{LAS}\mathcal{R}V_{MIN}}{4Q^2L_{TX}}. \tag{2.9}$$

This relationship provides guidance on how the circuit design balances the FOM and the IRNCD to meet the minimum power consumption required for a particular link

budget. The terms on the left side indicate the relationship between the IRNCD and the FOM of the ORX circuit. The link parameters form a constant on the right side of the link. Notably, this product is independent of bandwidth. We will investigate insights into this expression through analysis and later to compare different ORX circuits and device technologies through measurement according to the tradeoffs in (2.9).

We plot the relationship in (2.9) in Fig. 2.2 in the black curve by plotting the FOM on the y-axis and one over IRNCD on the x-axis so that the minimum power consumption is achieved in the upper-right corner of the plot. Additionally, we plot the DC power consumption contours for the loss cases, $L_{TX} = 20$ dB and $L_{TX} = 23$ dB, from (2.28) to indicate combinations of the FOM and IRNCD that achieve constant power consumption.

Notably, different loss generates different power contours and minimum power.

Section 2.1.2 will explore the implications of the analysis of this section to shunt-feedback transimpedance amplifiers and Section 2.1.3 will explore common-base/common-gate transimpedance amplifiers.

2.1.2 Case Study: Shunt Feedback TIA

The transimpedance of a broadband shunt-feedback ORX is

$$Z_{TIA}(s) = \frac{R_F A(s)}{1 + A(s)}, \tag{2.10}$$

where the $A(s)$ is the amplifier voltage gain frequency response and R_F is the feedback resistance. The 3-dB bandwidth of the TIA is $BW = \frac{\sqrt{2A(A+1)}}{2\pi R_F C_T}$, where $C_T = C_{PD} + C_{IN}$ is the sum of the photodiode and amplifier input capacitance. These insights lead to the

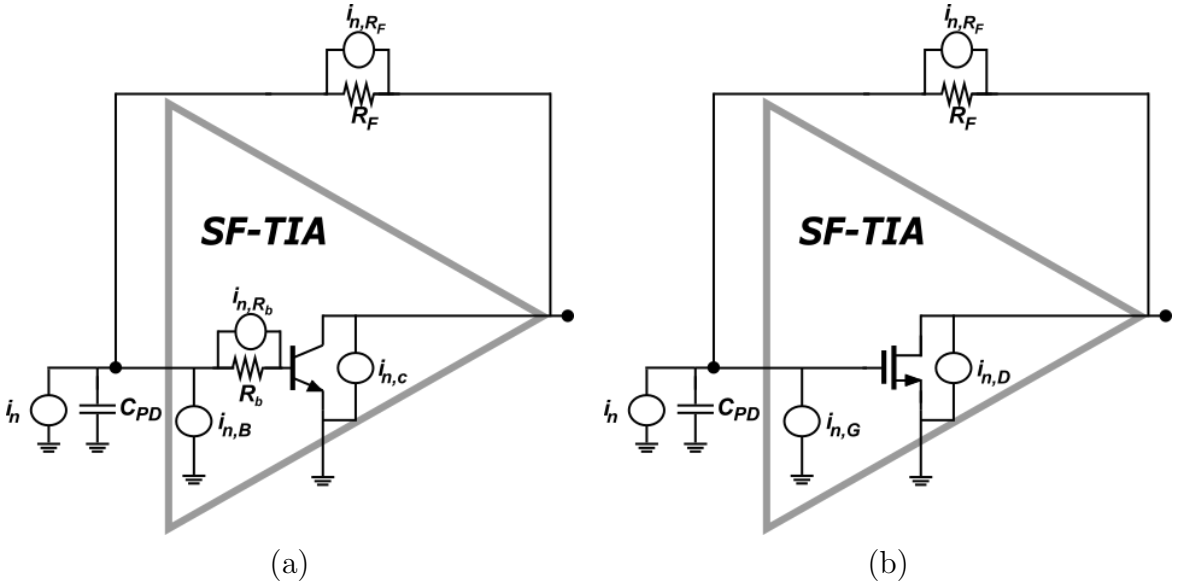


Figure 2.3: Schematic of two shunt-feedback TIAs using an (a) HBT common-emitter device and a (b) MOSFET common-source device.

well-known transimpedance bound [20].

$$R_T \leq \frac{f_T}{2\pi C_T BW^2} \tag{2.11}$$

This expression suggests that better device technologies with higher f_T as well as lower photodetector capacitance C_{PD} translate to higher FOM. Previous work investigated the role of multiple gain stages on the TIA limit and indicated that ultimately a transimpedance bound would occur for a given process [21].

We can also express the rms noise current given the input referred noise current spectral density of the form $\alpha_0 + \alpha_2 f^2$ for bipolar- and MOSFET-based front-ends illustrated in Fig. 2.3 using the Personick noise bandwidths as demonstrated in [22],

$$i^2_{n,rms,SF,bipolar} = \left(\frac{4kT}{R_F} + \frac{2kTg_m}{\beta} + \frac{4kTR_b}{R_F^2} + \frac{2kT}{g_m R_F^2}\right) b_2 BW + (\frac{2kT}{3g_m}(2\pi C_T)^2 + 4kTR_b(2\pi C_{PD})^2) b_3 BW^3. \quad (2.12a)$$

and

$$i^2_{n,rms,SF,MOSFET} = \left(\frac{4kT}{R_F} + 2qI_G + \frac{4kT\gamma}{g_m R_F^2}\right) b_2 BW + \left(\frac{4kT\gamma}{3g_m}(2\pi C_T)^2\right) b_3 BW^3. \quad (2.12b)$$

The noise bandwidths are scaled from the Personick integrals, resulting in the 3-dB bandwidth scaling factors, $b_2 = 1.11$ and $b_3 = 3.3$ for a second-order Butterworth response [23]. Note that because the target data exceeds multi-gigabit-per-second operation, flicker $(1/f)$ noise is not an important contributor to the overall noise of the MOSFET case in Eqn. 2.12b [22]. The bipolar case of (2.12a) can be simplified by assuming the base resistance, R_b, is negligible, β is high, and $g_m R_F^2 >> 2kT$. The MOSFET case of (2.12b) can be simplified assuming that the gate shot noise, I_G is negligible, and $g_m R_F^2 >> 4kT\gamma$. These assumptions results in the following two expressions,

$$i^2_{n,rms,SF,bipolar} = \frac{4kT}{R_F} b_2 BW + \frac{2kT}{3g_m}(2\pi C_T)^2 b_3 BW^3. \quad (2.13a)$$

and

$$i^2_{n,rms,SF,MOSFET} = \frac{4kT}{R_F} b_2 BW + \frac{4kT\gamma}{3g_m}(2\pi C_T)^2 b_3 BW^3. \quad (2.13b)$$

Notably, the f^2 (i.e. BW^3) noise term is greater for the MOSFET case by a factor

of 2γ. This suggests that if two SF-TIAs were designed in both HBT and MOSFET technologies achieving the same BW at respective R_F and g_m values, the noise in the bipolar-based SF-TIA would still be lower unless $\gamma \leq 0.5$ which is not possible for advanced MOSFET channel lengths (i.e. less than 0.18 μm) [24].

Since the FOM and the IRNCD both depend on the feedback resistance R_F, using (2.2), (2.13a), and (2.13b) the products from (2.9) can be written as

$$(IRNCD \cdot FOM_{BW})_{SF,bipolar} = \frac{2kT}{P_{DC,RX}} \left(\frac{b_2 f_T}{\pi R_F C_T BW} + \frac{b_3 C_T BW}{3C_{IN}} \right) \tag{2.14a}$$

and

$$(IRNCD \cdot FOM_{BW})_{SF,MOSFET} = \frac{2kT}{P_{DC,RX}} \left(\frac{b_2 f_T}{\pi R_F C_T BW} + \frac{2b_3 C_T \gamma BW}{3C_{IN}} \right). \tag{2.14b}$$

Since these products should be fixed by the link parameters according to (2.9), the minimum power consumption in the RX occurs for a specific choice of the shunt feedback resistor. As kT is a fundamental parameter, the term in parenthesis must be minimized according to P_{DC}. Finding the optimum BW in (2.14a) and (2.14b) allows us to find the following optimum feedback resistances.

$$R_{F,MIN,SF,bipolar} = \frac{6b_2}{b_3} \frac{C_{IN}}{C_T} \frac{f_T}{2\pi C_T BW^2} \tag{2.15a}$$

and

$$R_{F,MIN,SF,MOSFET} = \frac{3b_2}{b_3} \frac{C_{IN}}{C_T} \frac{1}{\gamma} \frac{f_T}{2\pi C_T BW^2}. \tag{2.15b}$$

The last ratio in this expression is the transimpedance bound in (2.11). Under the condition that $C_{IN} \approx C_{PD}$ and using the Personik coefficients for the noise bandwidth, we find that $\frac{3b_2}{b_3} = 1$ for the Butterworth response. Consequently, the optimum choice of R_F is $\frac{f_T}{2\pi C_T BW^2}$ for the bipolar case and is the upper bound from (2.10), and for the MOSFET case, the optimum choice of R_F is $0.5\frac{1}{\gamma}\frac{f_T}{2\pi C_T BW^2}$. However, these results depend on the RX frequency response. For a Bessel second-order frequency response ($b_2 = 1.15, b_3 = 5.64$), the optimum choices for R_F are $0.6\frac{f_T}{2\pi C_T BW^2}$ and $0.3\frac{f_T}{2\pi C_T BW^2}$ for the bipolar and MOSFET cases, respectively.

Finally, the minimum DC power of the ORXs can be evaluated using (2.14a), (2.14b) and (2.9),

$$P_{DC,RX,MIN,SF,bipolar} = \frac{16kTBWQ^2L_{TX}}{\mathcal{R}\eta_{LAS}V_{MIN}}\frac{b_3}{3}\left(1+\frac{C_{PD}}{C_{IN}}\right) \tag{2.16a}$$

and

$$P_{DC,RX,MIN,SF,MOSFET} = \frac{32kTBWQ^2L_{TX}\gamma}{\mathcal{R}\eta_{LAS}V_{MIN}}\frac{b_3}{3}\left(1+\frac{C_{PD}}{C_{IN}}\right). \tag{2.16b}$$

Using the previous link parameters of 2.1.1, the shunt feedback TIA is limited to a minimum RX power consumption of 2mW at 40 GHz bandwidth for the bipolar case and 4mW for the MOSFET case. It is important to reiterate that this considers only the front-end. This limit can be used to compare design approaches and technologies in a shunt feedback TIA circuit. Assuming a bit rate of 56 Gbps for the RX with 40 GHz bandwidth, we can translate these results to energy efficiency by amortizing the DC power consumption by the bit rate,

$$EE_{RX,MIN,SF,bipolar} = 3.81\frac{kTQ^2L_{TX}b_3}{\mathcal{R}\eta_{LAS}V_{MIN}}\left(1+\frac{C_{PD}}{C_{IN}}\right) \tag{2.17a}$$

and

$$EE_{RX,MIN,SF,MOSFET} = 7.62\frac{kTQ^2L_{TX}\gamma b_3}{\mathcal{R}\eta_{LAS}V_{MIN}}\left(1+\frac{C_{PD}}{C_{IN}}\right). \tag{2.17b}$$

This calculation suggests that the energy efficiency can theoretically reach 0.02 pJ/b for links with 20 dB of loss for the bipolar case and 0.04 pJ/bit for the MOSFET case. Of course, real implementations remain orders of magnitude above these limits. Furthermore, DC power consumptions and energy efficiencies as ultimate figures of merits favor FET-based designs considerably in the recent literature [25, 26]. The availability of low-power inverter-based gain cells in FET-based technologies allows for significantly efficient performance in real-world RXICs. Furthermore, with the implementation of RXICs through multi-stage design and aggressive high-frequency peaking techniques as demonstrated in [14, 25–27], the limits of (2.16a), (2.16b), (2.17a), and (2.17b) are effectively circumvented. Ultimately, this case study of the analysis presented in Section 2.1.1 did demonstrate, however, the favorable implications of the noise characteristics in a bipolar device in the context of minimizing RX DC power in the context of a full optical link. One interesting implication of the calculations of this case study is that the energy efficiency is independent of bandwidth (or bit rate) of the receiver and photodetector capacitance. A larger photodetector capacitance forces a reduction in the minimum feedback resistance from (2.15a) and (2.15b). This minimum resistance value generates more noise and, therefore, reduces the sensitivity of the link. The overall amount of power consumption and, consequently, energy efficiency is independent of the photode-

tector capacitance to first order as long as the input transistor is chosen with capacitance equal to the photodetector.

2.1.3 Case Study: Common-base (CB) and Common-gate (CG) TIAs

The transimpedance of a broadband CB and CG ORXs is detailed in [20] and written as

$$Z_{TIA,CB/CG}(s) = \frac{R_L}{(1+a_1 s)(1+a_2 s)}, \tag{2.18}$$

where the R_L is the common-base/common-gate load resistor that is equivalent to the midband transimpedance gain, and the poles of the TIA are $a_1 = (\frac{C_T}{g_m})^{-1}$ and $a_2 = R_L C_L$ where $C_T = C_{PD} + C_{IN}$. The time constant, a_1, assumes that the input resistance of the CB or CG transistors is simply $1/g_m$. Because the 3-dB bandwidth of the CB/CG TIA is less than the poles indicated by the time constants a_1 and a_2, a ratio can be defined as $\chi = \frac{a_2}{a_1}$ which is denoted as a pole-spacing ratio in [20]. The transimpedance bound is subsequently determined to be similar to the shunt feedback TIA [20], [28].

$$R_{T,CB/CG} \leq \frac{\zeta f_T}{2\pi C_T BW^2} \tag{2.19}$$

where $\zeta = \frac{\sqrt{\chi^4+6\chi^2+1}-\chi^2-1}{2\chi}$ [20]. Given a large enough χ, the expression results in the same transimpedance limit as the shunt-feedback TIA as in (2.11).

We can also express the rms noise current given the input referred noise current spectral density of the form $\alpha_0 + \alpha_2 f^2$ for bipolar common base and MOSFET common gate [29] front-ends illustrated in Fig. 2.4 using the Personick noise bandwidths as demonstrated in [22, 28],

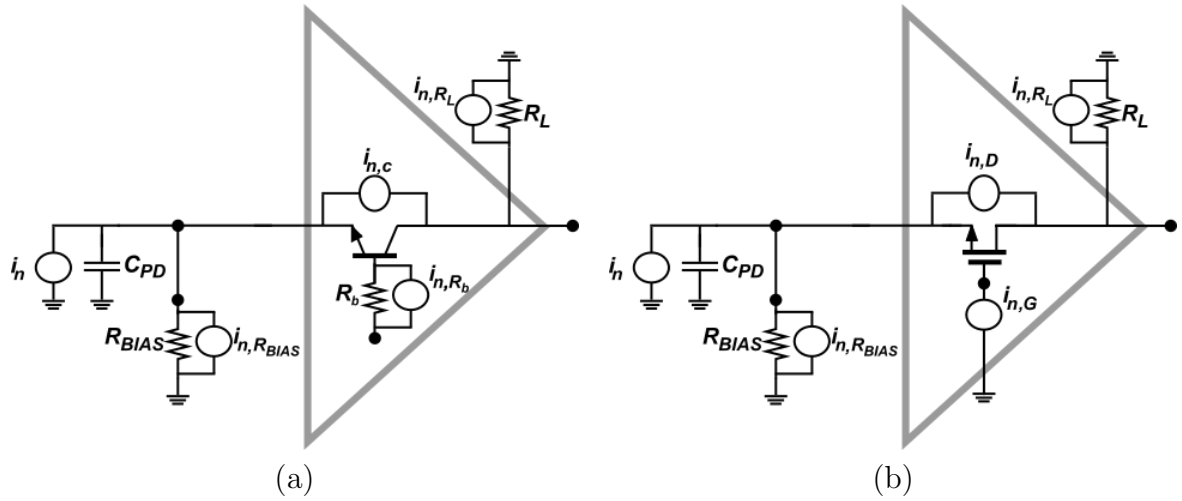


Figure 2.4: Schematic of two TIAs using an (a) HBT common-base device and a (b) MOSFET common-gate device.

$$i_{n,rms,CB}^2 = \left(\frac{4kT}{R_L} + \frac{4kT}{R_{BIAS}} + \frac{2kTg_m}{\beta}\right) b_2 BW + ... \\ + \frac{2kT}{3}\left(\frac{1}{g_m}(2\pi C_T)^2 + 2R_b(2\pi C_{PD})^2\right) b_3 BW^3 \quad (2.20a)$$

and

$$i_{n,rms,CG}^2 = \left(\frac{4kT}{R_L} + \frac{4kT}{R_{BIAS}} + 2qI_G\right) b_2 BW + \frac{4kT\gamma}{3g_m}(2\pi C_T)^2 b_3 BW^3. \quad (2.20b)$$

As in Section 2.1.2, flicker ($1/f$) noise is ignored in the MOSFET case in (2.20a) and (2.20b) [22]. To simplify the noise expressions, the following assumptions can be made in the bipolar case of (2.20a): we can assume the base resistance, R_b, is negligible and that β is high. Furthermore, in the FET case of Eqn. 2.20b, we can assume that the gate shot noise, I_G is negligible. These assumptions results in the following two expressions,

$$i_{n,rms,CB}^2 = \frac{4kT}{R_{TOT}} b_2 BW + \frac{2kT}{3g_m}(2\pi C_T)^2 b_3 BW^3 \tag{2.21a}$$

and

$$i_{n,rms,CG}^2 = \frac{4kT}{R_{TOT}} b_2 BW + \frac{4kT\gamma}{3g_m}(2\pi C_T)^2 b_3 BW^3. \tag{2.21b}$$

where $R_{TOT} = R_{BIAS}||R_L$. Notably, the same observations which indicate HBT-based TIA designs have superior (i.e. lower) noise performance as in Section 2.1.2 apply.

Since the FOM and the IRNCD both depend on R_T and R_L, respectively, using (2.2), (2.21a), and (2.21b) the products from (2.9) can be written as

$$(IRNCD \cdot FOM_{BW})_{CB} = \frac{2kT\zeta}{P_{DC,RX}} \left(\frac{b_2 f_T}{\pi R_{TOT} C_T BW} + \frac{b_3 C_T BW}{3C_{IN}} \right) \tag{2.22a}$$

and

$$(IRNCD \cdot FOM_{BW})_{CG} = \frac{2kT\zeta}{P_{DC,RX}} \left(\frac{b_2 f_T}{\pi R_{TOT} C_T BW} + \frac{2b_3 C_T \gamma BW}{3C_{IN}} \right). \tag{2.22b}$$

Since these products should be fixed by the link parameters according to (2.9), the minimum power consumption in the RX occurs for a specific choice of the load and bias resistors. As kT is a fundamental parameter, the term in parenthesis must be minimized according to P_{DC}. Finding the optimum BW in (2.22a) and (2.22b) allows us to find an optimum feedback resistance.

$$R_{TOT,MIN,CB} = \frac{6b_2}{b_3}\frac{C_{IN}}{C_T}\frac{f_T}{2\pi C_T BW^2} \tag{2.23a}$$

and

$$R_{TOT,MIN,CG} = \frac{3b_2}{b_3}\frac{C_{IN}}{C_T}\frac{1}{\gamma}\frac{f_T}{2\pi C_T BW^2}. \tag{2.23b}$$

Notably, the expressions for an optimal choice in R_{TOT} in (2.23a) and (2.23b) are equivalent to the expressions for the optimal feedback resistor of a shunt feedback resistor in (2.15a) and (2.15b).

The minimum power of the ORX can be evaluated using (2.23a), (2.23b), and (2.9),

$$P_{DC,RX,MIN,CB} = \frac{16kTBWQ^2L_{TX}\zeta}{\mathcal{R}\eta_{LAS}V_{MIN}}\frac{b_3}{3}(1+\frac{C_{PD}}{C_{IN}}) \tag{2.24a}$$

and

$$P_{DC,RX,MIN,CG} = \frac{32kTBWQ^2L_{TX}\zeta}{\mathcal{R}\eta_{LAS}V_{MIN}}\frac{b_3}{3}(1+\frac{C_{PD}}{C_{IN}}). \tag{2.24b}$$

2.1.4 Coherent Detection

The total power consumption of a short-range coherent link, discounting the transmitter electronics, includes the optical power required for a minimum optical receiver sensitivity, P_{SENS}, and the DC power required to amplify the signal to a sampling threshold, $V_I, V_Q \geq V_{MIN}$. We assume that the transmitter can be characterized by the wall-plug efficiency of a laser, η_{LAS}, and the total passive optical losses introduced

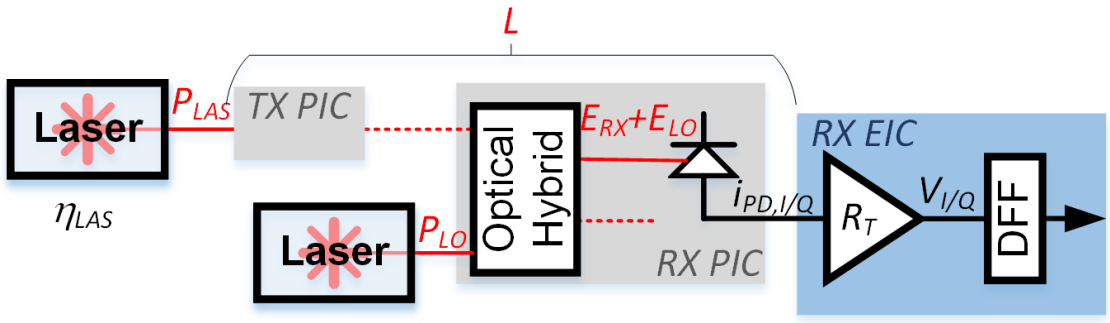


Figure 2.5: Illustration of link analysis parameters used in calculating energy efficiency

by the transmitter modulator, interconnect, and receiver hybrid are L.

The total DC power consumption of the link is

$$P_{DC} = \frac{P_{LAS} + P_{LO}}{\eta_{LAS}} + P_{DC,RX} = P_{LO}\frac{1+\gamma}{\eta_{LAS}} + P_{DC,RX}. \tag{2.25}$$

The relationship between laser power, P_{LAS}, and LO laser power, P_{LO} is defined by $\gamma = \frac{P_{LAS}}{PLO}$. The first term in (2.25) captures the DC power to generate the optical carrier and LO while the second term is the total (I and Q) RX power consumption.

The figure of merit introduced in 2.1.1 in Eqn. 2.2 which amortizes the transimpedance-bandwidth product by the DC power consumption is also used in this section.

FOM_{BW} is useful in circuit simulations and measurement comparisons and, notably, has units of $\frac{Hz}{A^2}$. However, the limitation of FOM_{BW} is that it discounts the noise contribution of the CoRX to achieve a target bit-error rate (BER).

The sensitivity is related to the minimum required amplification in the CoRX according to $V_{MIN} = P_{SENS}\mathcal{R}R_T$. Since the optical power that reaches the EIC is $P_{SENS} = 2P_{LO}\sqrt{\frac{\gamma}{L}}$, the total DC power can be recast in terms of these link parameters.

$$P_{DC} = P_{LO}\frac{1+\gamma}{\eta_{LAS}} + \frac{V_{MIN}BW}{\mathcal{R}FOM_{BW}P_{LO}}\sqrt{\frac{L}{\gamma}} \tag{2.26}$$

To minimize the DC power consumption, there exists an optimum LO power for the CoRX from (2.26).

$$P_{LO,MIN} = \sqrt[4]{\frac{L}{\gamma}}\sqrt{\frac{V_{MIN}BW\eta_{LAS}}{(1+\gamma)\mathcal{R}FOM_{BW}}} \tag{2.27}$$

Finally, the minimum LO power is related to the sensitivity, $P_{SENS} = 2\sqrt{\frac{\gamma}{L}}P_{LO,MIN}$ and the minimum DC power consumption,

$$P_{DC,MIN} = 2\sqrt[4]{\frac{L}{\gamma}}\sqrt{\frac{(1+\gamma)V_{MIN}BW}{\eta_{LAS}\mathcal{R}FOM_{BW}}}. \tag{2.28}$$

From this expression, the power consumption of the coherent link in (2.28) is that the DC power increases with $\sqrt[4]{L}$ suggesting that ACD offers robustness to link loss compared to IMDD. Examining the role of γ, the DC power consumption further reaches a minimum for the choice of $\gamma = 1$, however, balancing the LO power with the transmitter laser power is impractical. The minimum power consumption occurs for $\gamma = 1$, however, the power consumption increases only slightly for deviations in the choice of γ over an order of magnitude. Moreover, the LO power reduces as one tends to use a higher choice of γ.

To understand the tradeoffs in terms of the CoRX FOM and RMS input referred noise current, $i_{n,rms}$, we can recast (2.27) using $P_{SENS} = \frac{2Qi_{n,rms}}{\mathcal{R}}$, where Q is based on the required bit error rate (BER). Therefore, the product of the mean-square noise current and the FOM of the CoRX is

$$\overline{i_n^2} \cdot FOM_{BW} = \frac{V_{MIN}BW\eta_{LAS}\mathcal{R}}{2Q^2(1+\gamma)}\sqrt{\frac{\gamma}{L}}. \tag{2.29}$$

This expression indicates the CoRX EIC tradeoffs on the left and the optical link parameters on the right hand side of the equation. Eqn. 2.28 are expressed in terms of $i_{n,rms}$ given the relationship $P_{LO} = \frac{1}{2}P_{SENS}\sqrt{\frac{L}{\gamma}}$.

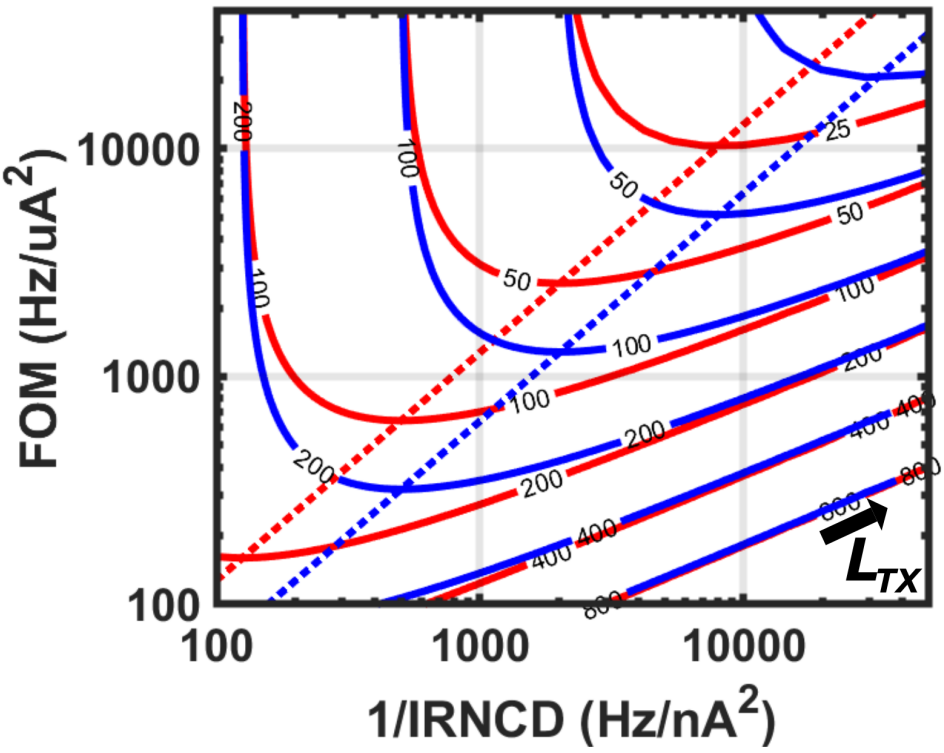


Figure 2.6: Receiver FOM as a function of inverse noise power spectral density for $L = 20$ dB. ($V_{MIN} = 0.1$V, $BW = 40$GHz, $\eta_{LAS} = 25\%$, and $\mathcal{R} = 1$ A/W). The blue contour lines indicate the DC power consumption in mW. The state of the art in optically (red) and electrically (black) measured CoRXs are surveyed here. Note: the FOMs have been scaled for a uniform transimpedance gain definition as indicated in Table 7.1 (i.e. $Z_{T,diff} = 2Z_T = 2\Delta V_{out}/\Delta I_{in}$).

$$P_{DC} = \frac{1+\gamma}{\eta_{LAS}} \frac{Q}{\mathcal{R}} \sqrt{\frac{L}{\gamma}} i_{n,rms} + \frac{V_{MIN} BW}{QFOM_{BW}} \frac{1}{i_{n,rms}} \tag{2.30}$$

The power contours in Fig. 2.6 illustrate the regions where the tradeoff between the FOM and the inverse current power spectral density provides the minimum power consumption. A minimum power consumption is achieved as both the FOM and inverse noise power spectral density are increased. The contours indicate how different combinations of noise and FOM achieve lower power.

2.2 Surveying the State-of-the-Art in Optical Receivers

There are a plethora of metrics that are reported in the state of the art of optical RXIC literature. The commonly-reported metrics include the following:

- Bit Rate, BR (bits/second)
- P_{sens} @ BER (dBm)
- Energy efficiency, $\frac{BR}{P_{DC,RX}}$ (pJ/bit)
- 3-dB Bandwidth (Hz)
- Transimpedance Gain, $Z_T(0)$ (dBΩ)
- Input-referred RMS noise current, $i_{n,rms}$ (μA_{rms})
- Transimpedance gain-bandwidth efficiency, FOM_{BW}, $\frac{R_T BW_{3dB}}{P_{DC,RX}}$ ($\frac{\Omega GHz}{mW}$)
- Total harmonic distortion, THD, (%)

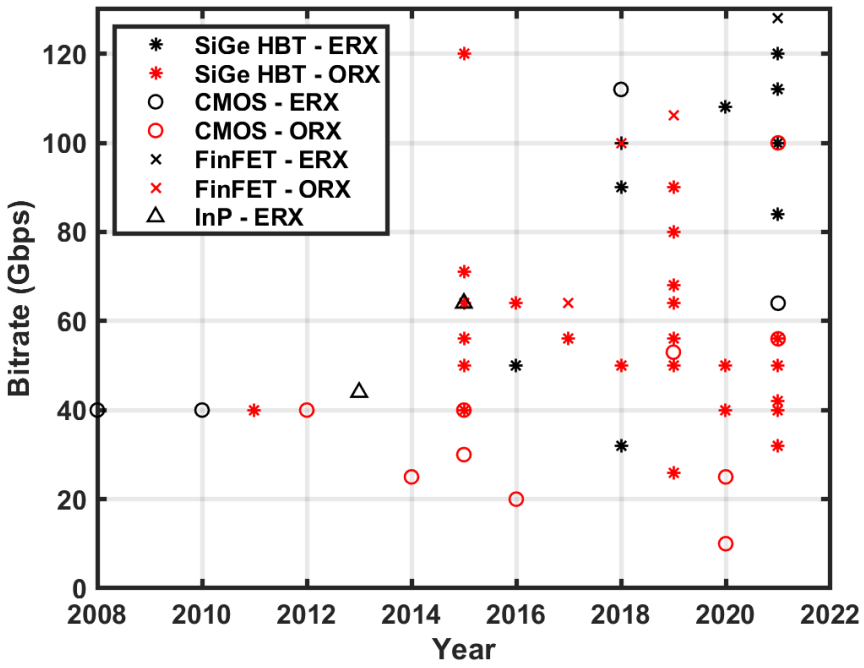


Figure 2.7: Surveyed optical RXIC bit rate vs. year reported.

Given a large set of metrics, the task of evaluating optical RXICs against each other becomes a challenging task. In this section, a survey of the state-of-the-art in optical receiver literature will be presented based on the works reported in [14, 16, 19, 21, 25–27, 30–72]. The surveyed optical RXICs spanned conference and journal publications of the Institute of Electrical and Electronics Engineers (IEEE) and the Optical Society of America (OSA), which has been recently rebranded as Optica. The modulation schemes of the prior arts span direct detection-based NRZ and 4-PAM formats as well as coherent detection-based QPSK and 16-QAM formats. The technologies of the reported works included SiGe HBT, CMOS (bulk and SOI), FinFET, and InP HBT platforms.

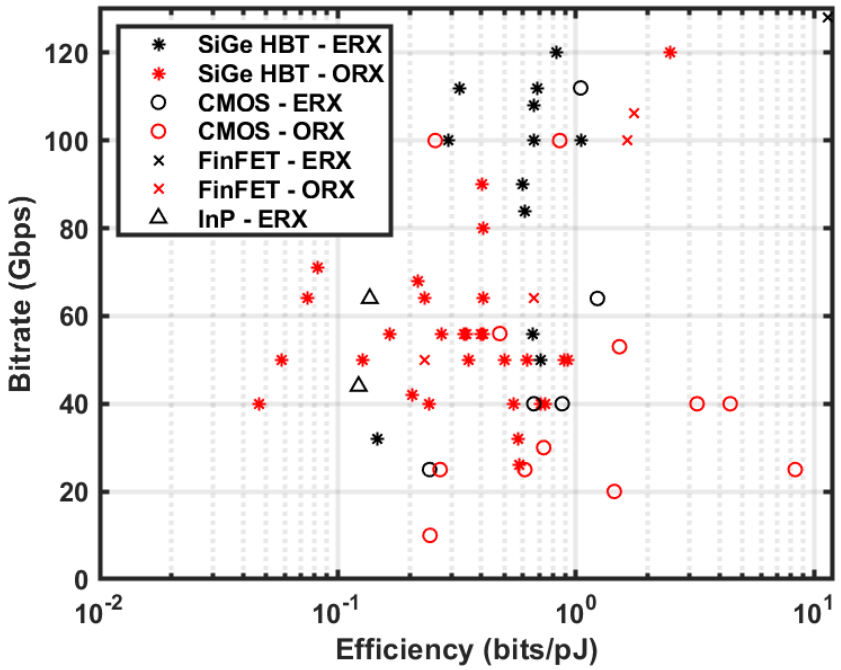


Figure 2.8: Surveyed optical RXIC bit rate vs. bit per picojoule efficiency (i.e. inverse conventional energy efficiency).

2.2.1 Bit-rate and Energy Efficiency

Because the design of optical DCIs are primarily driven by increasing capacity and energy efficiency as described in Chapter 1, the following two figures can provide reasonable insight towards recent breakthroughs. Figure 2.7 indicates a Moore's law-style plot illustrating the reported bit rates over the years, while Figure 2.8 demonstrates the bit rates with their respective bit-per-joule efficiencies. Notably, Figure 2.7 highlights the increase of bit rates since 2010 from roughly 40 Gbps to as high as 128 Gbps, and Figure 2.8 demonstrates that the majority of the reported works have their bits-per-picojoule efficiencies largely clustered between 0.1 to 1 bit/pJ. Furthermore, the technology platform has a great impact on the efficiency of the optical RXICs: the only works exceeding 1 bit/pJ are based on CMOS and FinFET technologies. Consequently, from this data set, one can gather that CMOS/FinFET-based optical RXICs have significant efficiency

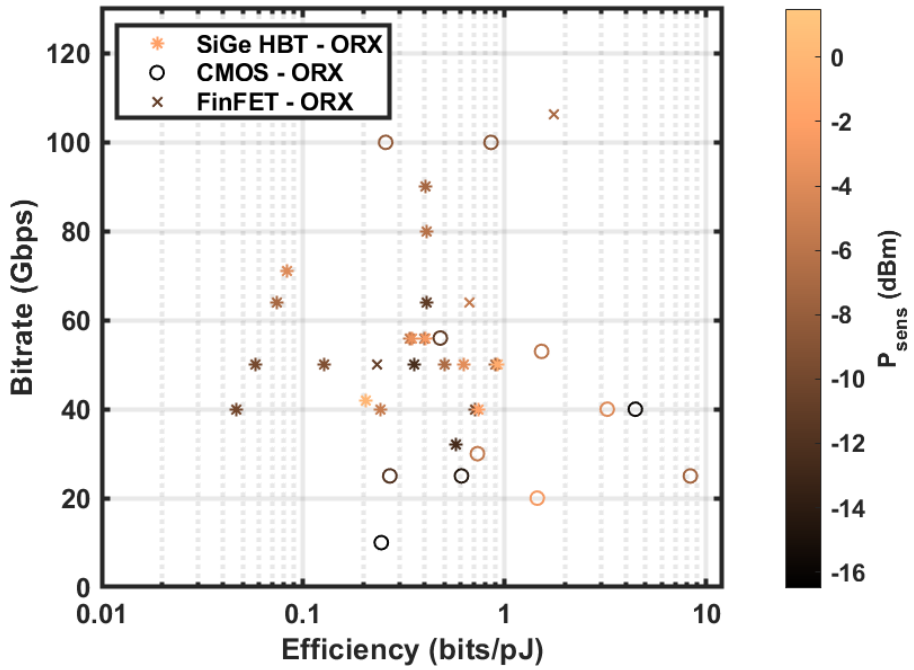


Figure 2.9: Surveyed optical RXIC sensitivity over bit rate vs. bit per picojoule efficiency (i.e. inverse conventional energy efficiency).

advantages over HBT technologies. The primary caveat to the survey of Fig. 2.8 is that there is no information as to what the input conditions were for the receivers. For example, for the optically measured receivers, Fig. 2.8 does not indicate the input optical modulation amplitude (OMA). This means that there is no discrepancy between RXICs with drastically different noise/sensitivity performance which is critical in optical receivers.

2.2.2 Optical Receiver Sensitivity

The optical receiver sensitivity, P_{sens}, at a defined bit-rate and input power level is largely agreed upon as the ultimate performance metric for an optical receiver assembly when measured using real-time BER. Figure 2.9 demonstrates the reported sensitivities in dBm over the bitrate vs. efficiency plot.

Although all the necessary information from a system-level perspective with respect to bitrate, efficiency and sensitivity (i.e. noise) performance is provided, it is very difficult to read and gather relations quickly. In fact, two points of comparable bitrate and efficiency at approximately 40 Gbps and 0.7 bits/pJ indicate a roughly 11.5 dB difference in sensitivity. Furthermore, the survey of Figure 2.9, while based on the gold standard of system-level measurements, is difficult to adopt as a universal comparison of intrinsic RXIC designs for several reasons. First, this approach has the disadvantages of long measurement times which has led to the IEEE 802.3 Ethernet standard that has adopted transmitter and dispersion eye closure quaternary (TDECQ) as an alternative is a system-level transmitter and a channel compliance metric which estimates the BER based on eye diagrams for 4-PAM by leveraging reference receivers that mimic the bandwidth and equalization capabilities of real-world receivers [68], [73].

The adoption of an alternative BER estimation method for 4-PAM results indicates the difficulty of adopting a real-time BER sensitivity standard across various modulation formats. This also demonstrates that the metric of sensitivity across the literature is ambiguous. Second, real-time BER sensitivity measurements of a receiver captures the performance enhancement (or degradation) of unique advanced optical packaging technologies such as heterogeneous integration [74] and monolithic integration [75] such that different parasitic capacitances and inductances must be compensated, and architecturally-dependent performance; for example, a fully-differential receiver in which the anode and cathode of a single photodetector drive the complementary TIA inputs can improve the sensitivity performance by 3 dB over a balanced differential receiver in which the anodes of two photodetectors drive the complementary inputs of the TIA [50], [48]. Consequently, the embedding of the aforementioned packaging and architecturally-related optical RX assemblies hide the intrinsic performance of RXIC designs which would be of interest to an EIC-oriented designer. Finally, using Psesns as a metric makes it dif-

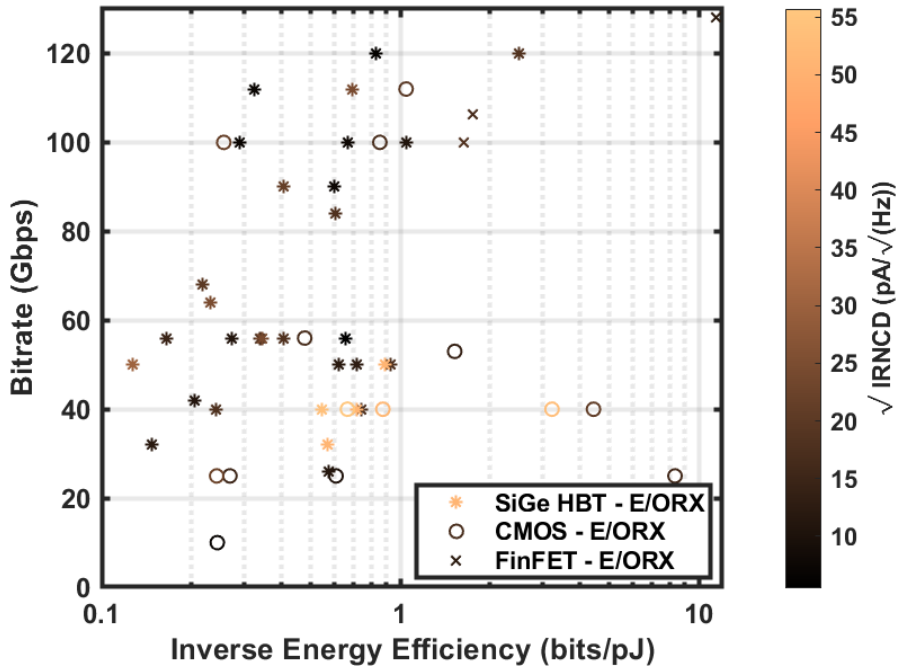


Figure 2.10: Surveyed optical RXIC $\sqrt{IRCND}$ over bit rate vs. bit per picojoule efficiency (i.e. inverse conventional energy efficiency).

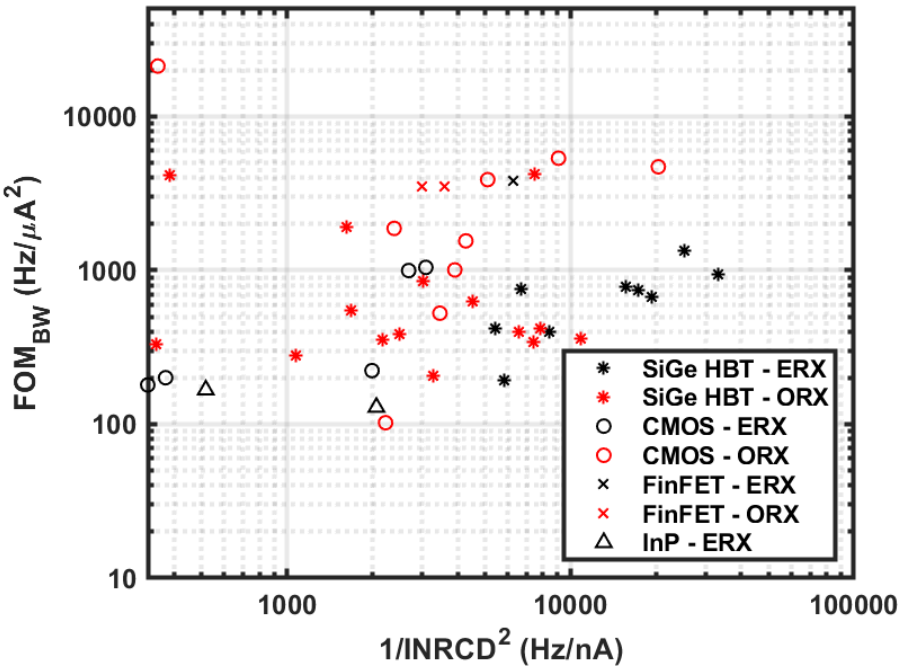
ficult to compare electrically measured RXICs vs optically measured RXICs. For all these reasons, the survey of Figure 2.9, while based on the gold standard of system-level measurements, is difficult to adopt as a universal comparison of intrinsic RXIC designs.

2.2.3 Input-referred Noise Current Spectral Density

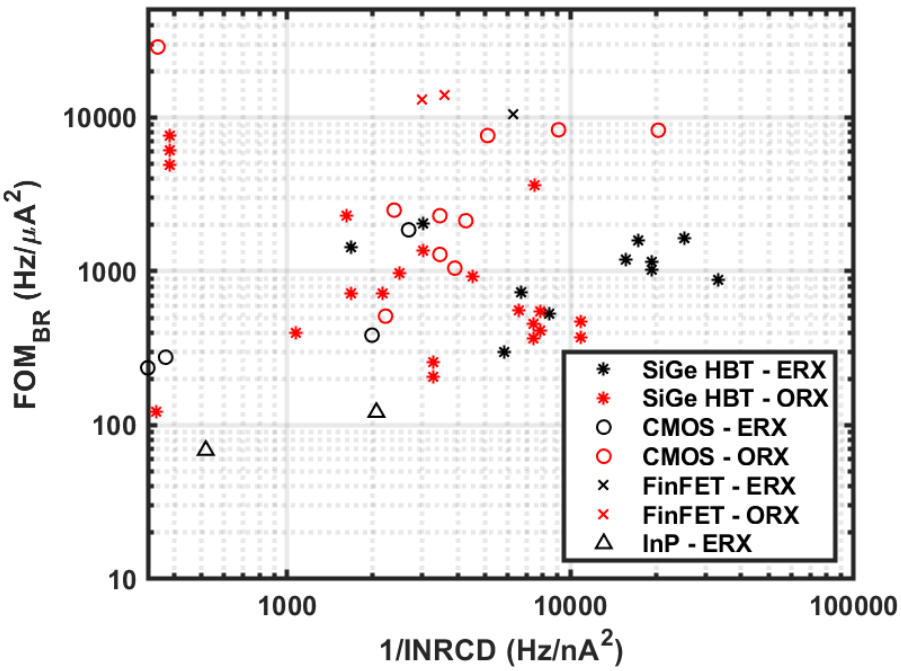
As an alternative to using P_{sens} which can only be accurately reported in an optical environment. The average input-referred noise current density, in this thesis denoted as $\sqrt{IRNCD}$ and nominally defined as the input rms noise current divided by the square-root of the 3-dB bandwidth, i.e. $\frac{i_{n,rms}}{\sqrt{BW_{3-dB}}}$, can be used. Fig. 2.10 demonstrates the reported spectral noise density in $\frac{pA}{\sqrt{Hz}}$ over the bitrate vs. efficiency plot. The utility of Fig. 2.10 is in its inclusion of the electrically reported RXICs in the literature enabling broader scope when compared to the survey in Fig. 2.9.

2.2.4 Figures of Merits (FOMs) and Noise Performance

Given the utility of FOM_{BW} and $IRNCD$ in visualizing link-level DC power consumption minimization by increasing FOM_{BW} and reducing $IRNCD$, FOM_{BW} (and FOM_{BR}) vs. inverse $IRNCD$ is plotted in Fig. 3.19. The plots indicate notable technology trends. For example, SiGe HBT designs are trended to lower noise performance with reasonably high $FOM_{BW/BR}$, and CMOS/FinFET designs are trending to very high $FOM_{BW/BR}$ performance at reasonably low noise performance. The following plots will be used to directly compare the works in Chapters 3 and 4.



(a)



(b)

Figure 2.11: Trends in state-of-the-art ERX and ORX (a) FOM_{BW} vs. $1/IRNCD$ and (b) FOM_{BR} vs. $1/IRNCD$ performance across SiGe HBT and CMOS technologies. The enlarged markers represent the variants of the work in 3.

Chapter 3

Optical Receivers for Direct Detection based on a Cherry-Hooper Emitter Follower Transimpedance Amplifier Front-end in 130-nm SiGe HBT Technology

This chapter is in part a reprint of material in the manuscript, "Energy Optimization for Optical Receivers based on a Cherry-Hooper Emitter Follower Transimpedance Amplifier Front-end in 130-nm SiGe HBT Technology," published in the IEEE Journal of Lightwave Technology [14]

We present an interpretation of conventional figure-of-merit (FOM) and average input-referred noise current density (IRNCD) that characterizes optical receivers to determine how technologies and circuits best address energy efficiency. A design methodology is presented for differential optical receivers based on Cherry-Hooper Emitter Follower

(CHEF) front-end designs targeting 56-Gbps applications is realized in a 130-nm SiGe BiCMOS process. The electrical measurements in a 50-Ω environment demonstrate data rates up to 112 Gbps and 84 Gbps for two design variants. In an open input and maximum gain configuration, the rms input referred noise currents are 3.59 μA_{RMS} and 2.41 μA_{RMS} and the corresponding average input referred noise current densities are 17.25 $pA/\sqrt{Hz}$ and 12.86 $pA/\sqrt{Hz}$. The packaged electro-optical measurements of the receiver variants is carried out with a single commercial off-the-shelf (COTS) photodetector demonstrate open eyes at data rates up to 64 Gbps. At 60 Gbps, the receiver variants achieve a $BER < 10^{-10}$ and $BER < 10^{-9}$. The total power consumption for the variants are 162 mW and 138 mW for overall energy efficiencies (with respect to electro-optical performance) of 2.53 pJ/bit and 2.3 pJ/bit.

3.1 Introduction

Intra-data center interconnects (IDCI) of reach below 2 km are increasingly pushing toward aggregate per lambda data rates of 200 Gbps to keep pace with next generation requirements. Data rate scaling has also been accompanied by attention to energy requirements [4]. This short-reach regime of the broader DCI space demands examination of fundamental bounds on the energy efficiency of front-end opto-electronic circuits based on the overall link expectations [11]. Similarly, low-noise operation at the receiver plays a similarly important role in improving overall link efficiencies. Low-noise receivers offer larger link budget margin to alleviate transmitter requirements and power consumption as well as design robustness to link variability. These trends have pushed recent optical receiver designs to optimize for simultaneous high-data rate, low-noise, and low-power operation.

Earlier literature has demonstrated results for receiver integrated circuits (RXIC)

across SiGe, CMOS, and FinFET based technologies in 50 Ω measurement environments which will be referred to as electrical RXICs (ERXICs), and optical environments which will be referred to as optical RXICs (ORXICs). The state-of-the-art has demonstrated record results across the metrics that include data rates measured in bits/s, energy efficiency measured in pJ/bit, and average input-referred noise current density ($\sqrt{IRNCD}$) measured in $pA/\sqrt{Hz}$.

While this paper will describe a SiGe-based RXIC for single-mode fiber (SMF) links at 1310 nm and optimization of FOM and IRNCD, we also seek to unify earlier understanding of how to compare technologies and circuits based on these characterizations. In CMOS-based ORXICs, data rates up to 53 Gbps have been demonstrated for NRZ-based links [26]. CMOS-based ERXICs, have achieved data rates up to 112 Gbps using 4-PAM [62]. In SiGe HBT-based ORXICs, data rates up to 90 Gbps using transmitter equalization for error-free (BER $< 10^{-5}$) in NRZ-based links have been demonstrated [48]. In SiGe HBT-based ERXICs, NRZ data rates up to 112 Gbps and up to 96 Gbps error-free (BER $< 10^{-10}$) and 4-PAM data rates up to 100 Gbps have been demonstrated [36], [16], [42]. Finally, a FinFET-based ORXICs achieving 4-PAM data rates up to 106.25 Gbps in optical measurements has been reported [68]

An $\sqrt{IRNCD}$ for CMOS-based ORXICs has been reported as low as 14 $pA/\sqrt{Hz}$ for CMOS-based designs [26]. An $\sqrt{IRNCD}$ as low as 9.6 $pA/\sqrt{Hz}$ has been demonstrated for SiGe HBT ORXICs and 5.5 $pA/\sqrt{Hz}$ for SiGe HBT ERXICs [50], [41]. For FinFET-based ORXICs, an $\sqrt{IRNCD}$ of 16.7 $pA/\sqrt{Hz}$ has been demonstrated [68].

In CMOS-based ORXICs, energy efficiencies have been reported in NRZ-based designs as low as 0.225 pJ/bit for 40 Gbps and 0.66 pJ/bit for designs above 53 Gbps [19], [26]. For CMOS-based ERXICs, energy efficiencies have reached 0.96 pJ/bit for 4-PAM based designs [62]. SiGe HBT-based ORXICs achieved energy efficiencies as low as 1.08 pJ/bit for NRZ data rates above 50 Gbps which has been enabled through monolithic integration

of the photodetector and the RXIC [50]. FinFET-based ORXICs have achieved energy efficiencies of 0.57 pJ/bit for 4-PAM data rates up to 106.25 Gbps [68].

SiGe HBT-based designs appear well positioned to lead RXIC designs in terms of both data rates and noise performance (i.e. IRNCD) with energy efficiencies remaining competitive. Though these three metrics are the primary means of comparing RXIC designs through a table comparison, the circuit designer is confronted by making trade-offs in terms of the transimpedance or the sensitivity of the receiver against the power consumption given a particular process technology. This paper seeks to demonstrate how receiver sensitivity and transimpedance can be related to reach energy efficiency optimizations across IDCIs. Therefore, five primary metrics are often optimized in transimpedance amplifier (TIA) designs: bit rate, power consumption, transimpedance gain, 3-dB bandwidth, and noise.

An extension of [16] is presented for two RXIC variants based on CHEF TIA front-ends. The RXIC variants consume 162 mW and 138 mW. The data rates and energy efficiencies achieved in a 50-Ω environment are 112 Gbps and 1.45 pJ/bit, and 84 Gbps and 1.64 pJ/bit, respectively. In an optical configuration with a single 38 GHz InGaAs/InP photodetector at the input of the TIA, the data rates and energy efficiencies achieved are 64 Gbps and 2.53 pJ/bit, and 60 Gbps and 2.3 pJ/bit, respectively. The $\sqrt{IRNCDs}$ of the RXIC variants are 17.25 $pA/\sqrt{Hz}$ and 12.86 $pA/\sqrt{Hz}$, respectively.

Section 3.2 presents the implementation of two RXIC variants. Section 3.3 presents the measured electrical and optical characteristics of the two variants in the time domain. Section 3.4 highlights the performance of the variants of this work against trends of the state of the art in RXIC designs. Finally, the chapter closes with concluding remarks.

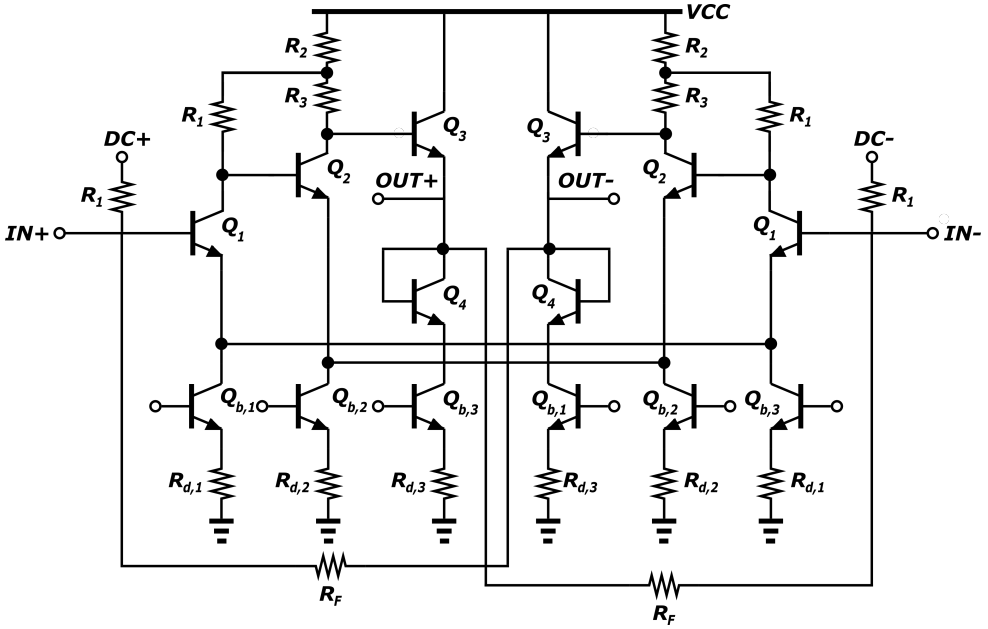


Figure 3.1: Schematic of CHEF TIA for the low R_F and high R_F.

3.2 Energy-efficient Optical Receiver SiGe Implementation

We designed two different TIAs with different values of front-end transimpedance gain to explore the tradeoff in IRNCD and FOM; one with low R_F (250 Ω) for higher bandwidth and one with a high R_F (1000 Ω) for better IRNCD. The following sections describe the circuit design of each of these three sections in terms of the FOM and the IRNCD contributions.

3.2.1 Cherry-Hooper Emitter Follower TIA

The TIA stage is implemented using a standard shunt feedback-based Cherry-Hooper Emitter Follower (CHEF) TIA. Generally, common emitter-based amplifiers are used in shunt feedback TIAs. The CHEF amplifier can be described as a cascaded transconductance and transimpedance amplifier. This cascade of stages design allows for independent

Table 3.1: CHEF TIA parameter values.

Parameter/Variant	**Low** R_F	**High** R_F
R_F (Ω)	250	1000
R_1, R_2, R_3 (Ω)	20, 50, 30	159, 60, 15
L_{e,Q_1}, L_{e,Q_2}, L_{e,Q_3}, L_{e,Q_4} (μm)	4, 4, 5.3, 5.3	4, 4, 5.3, 5.3
R_{DC} (Ω)	2000	2000
$L_{e,Q_{b,1}}$, $L_{e,Q_{b,2}}$, $L_{e,Q_{b,3}}$ (μm)	6.8, 4, 9	6.8, 4, 9
$R_{d,1}$, $R_{d,2}$, $R_{d,3}$ (Ω)	65, 100, 49	65, 100, 49
I_1, I_2, I_3 (mA)	3, 2, 4	3.7, 2.4, 4.9

tuning of the gain and bandwidth of the amplifier core through bias currents, I_1 and I_2 of the respective stages. This breaks the direct gain-BW tradeoff presented in typical common-emitter amplifiers.

With respect to energy efficiency, we leverage the high f_T of the 130-nm SiGe HBT process ($300GHz$) and roll back the bias currents well below the peak f_T point while maintaining a suitable high-speed and mid-high gain operation. The frequency response of this front-end stage is shown in Fig. 3.2. The capacitance of the input pads and the loading of the intermediate stage of the receiver chain are captured. The low-R_F and high-R_F variants present transimpedance gains of 44 dBΩ and 59.1 dBΩ and 3-dB bandwidths of 25.8 GHz and 25.3 GHz, respectively.

The total power consumption for the CHEF TIA is 54 mW for the low R_F variant and 66 mW for the high R_F variant.

3.2.2 Intermediate-stage Gilbert-cell VGA

The VGA stage is implemented as a cascade of a Gilbert-cell (GC) amplifier and an emitter follower (EF) buffer. The VGA schematic is illustrated in Fig. 3.3. The low-R_F TIA has an intermediate stage that is composed of a cascade of two GC VGA stages, while

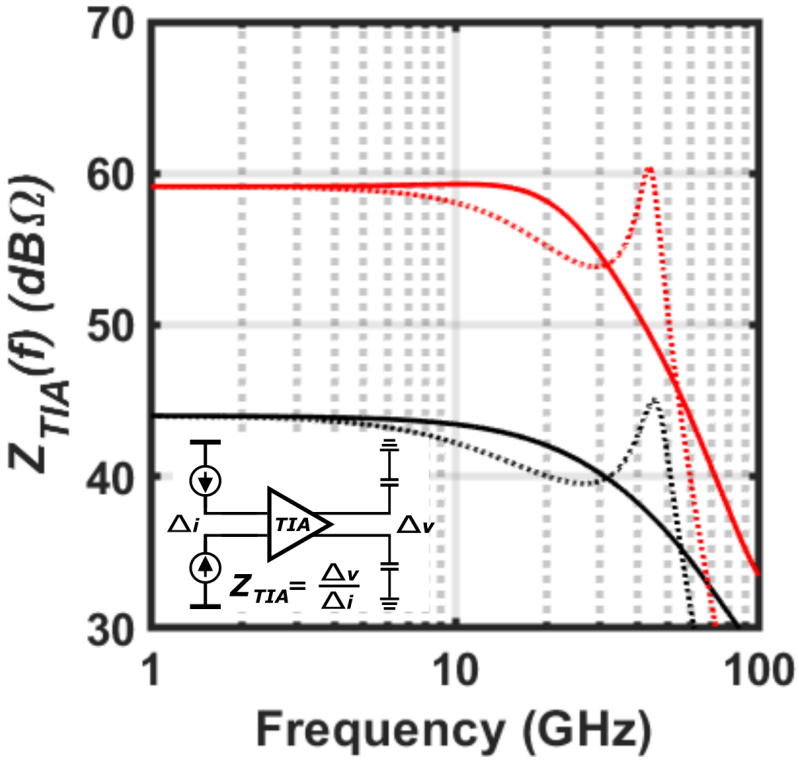


Figure 3.2: Simulated frequency response of the TIA stage of the low-R_F variant (black) and high-R_F variant (red). The solid line indicates the de-embedded TIA performance, and the dotted line represents the TIA with $L_{WB,OUT} = L_{WB,PD} = 250pH$, $C_{PD} = 80fF$, and $R_{S,PD} = 5\Omega$.

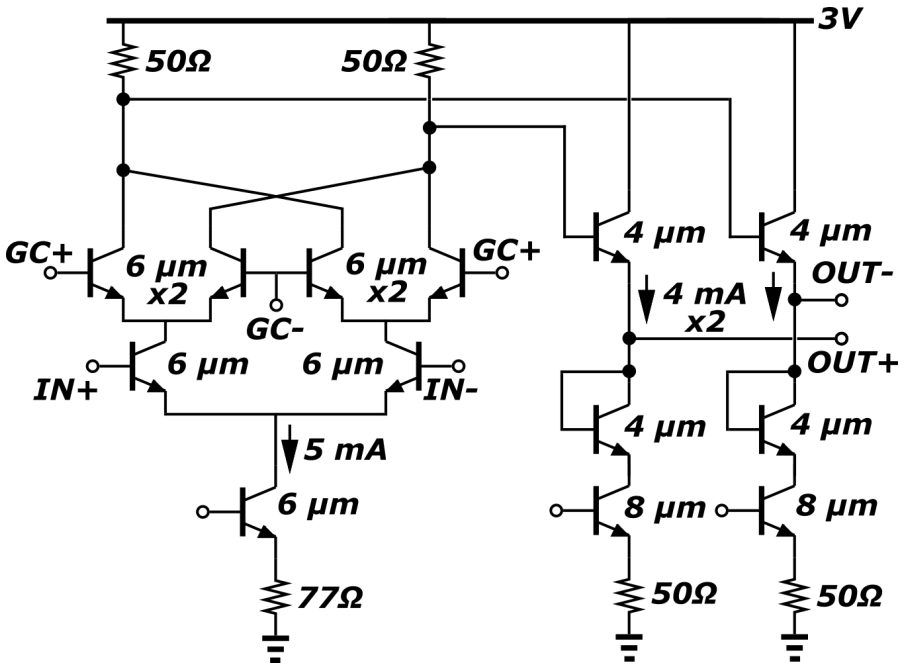


Figure 3.3: Schematic of VGA stage common to both variants. Note: The low-R_F TIA cascades two VGA cells and the high-R_F TIA includes only one VGA cell.

the high-R_F TIA only consists of a single GC VGA stage. For the low-R_F and high-R_F TIAs, the tunable transimpedance gain range is 21 dB and 10 dB, respectively. The gain control voltage, $\Delta V_{GC} = V_{GC+} - V_{GC-}$, is set by two sub-100 μA current mirror references that desensitize the I_C-V_{BE} relation for manual tuning. Bypass capacitors are placed as close as possible to the base of the GC devices and provide two important functions: (1) isolation from the external environment in conjunction with the current mirror reference and (2) configuring the the GC stage of the VGA as common-base devices which mitigate the Miller effect and loading on the TIA output.

The individual GC stages consume 5 mA through a 3 V supply for a power consumption of 15 mW. The EF stage consumes 8 mA through a 3 V supply for a power consumption of 24 mW. The total power consumption of the VGA stage is 78 mW for the low-R_F variant and 39 mW for the high-R_F variant.

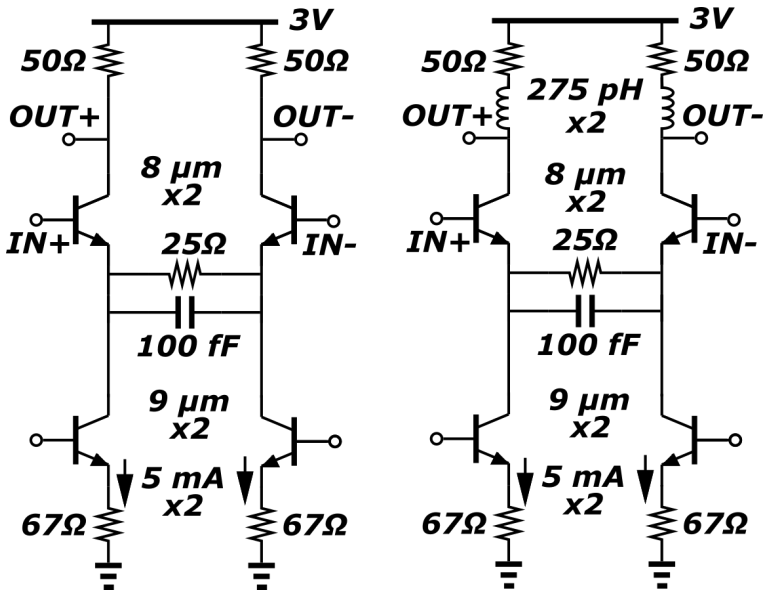


Figure 3.4: Schematic of OB with CTLE for the low-R_F variant (left) and high-R_F variant (right).

3.2.3 50 Ω Output Buffer with Continuous-Time Linear Equalization

The OB stage primarily functions as a unity-gain interface between the the front-end optical receiver cascade and a 50-Ω interface which may be a CMOS high-speed DSP/SERDES unit with a voltage swing up to 500 mV_{p-p}. Because the OB including the preceding emitter follower stage makes up nearly half of the receiver IC power consumption, a passive equalization technique, continuous-time linear equalization (CTLE), is utilized to extend the overall receiver chain 3-dB bandwidth and, thus, the energy efficiency of the ORX IC. The CTLE network is comprised of a parallel resistor-capacitor network which degenerates the differential pair of the OB. Given the effective transconductance of the OB, $g_{m,CTLE} = \frac{g_m}{1+g_m Z_{CTLE}}$, and the output impedance, $Z_{OUT,OB} = \frac{R_L+sL_{OUT}}{2+sL_{OUT}/R_L}$, the OB gain, $A_v(s)$ can be written as

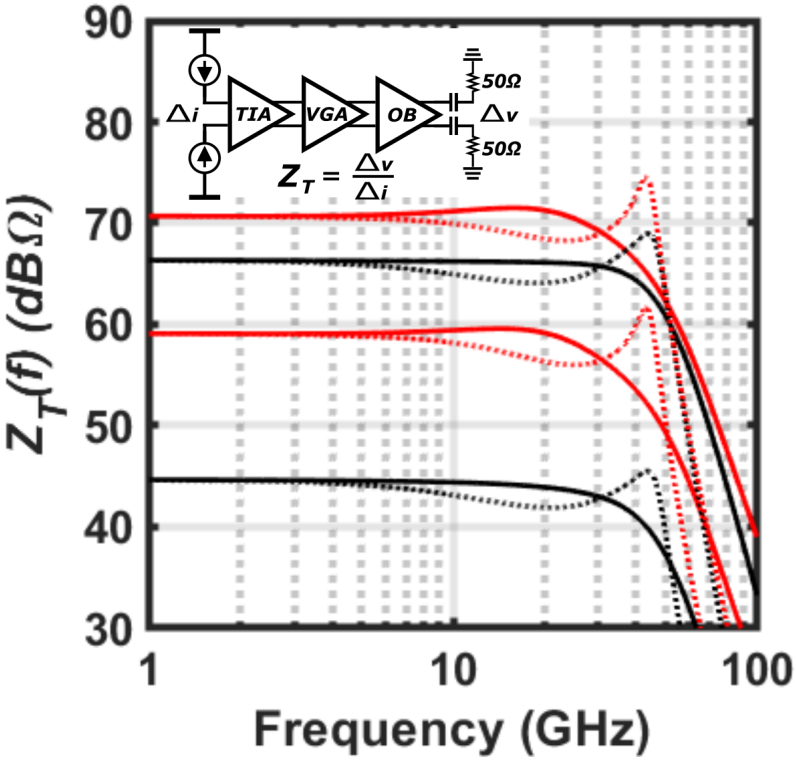


Figure 3.5: Simulated $Z_T(f)$ for low-R_F TIA (black) and high-R_F TIA (red) at minimum and maximum VGA gain settings. The low-R_F TIA is plotted in black and the high-R_F TIA is plotted in red. The solid line indicates the de-embedded TIA performance, and the dotted line represents the TIA with $L_{WB,OUT} = L_{WB,PD} = 250$ pH, $C_{PD} = 80$ fF, and $R_{S,PD} = 5\ \Omega$. Note: the frequency response plots are characterized for the differential testbench illustrated in the inset of (a).

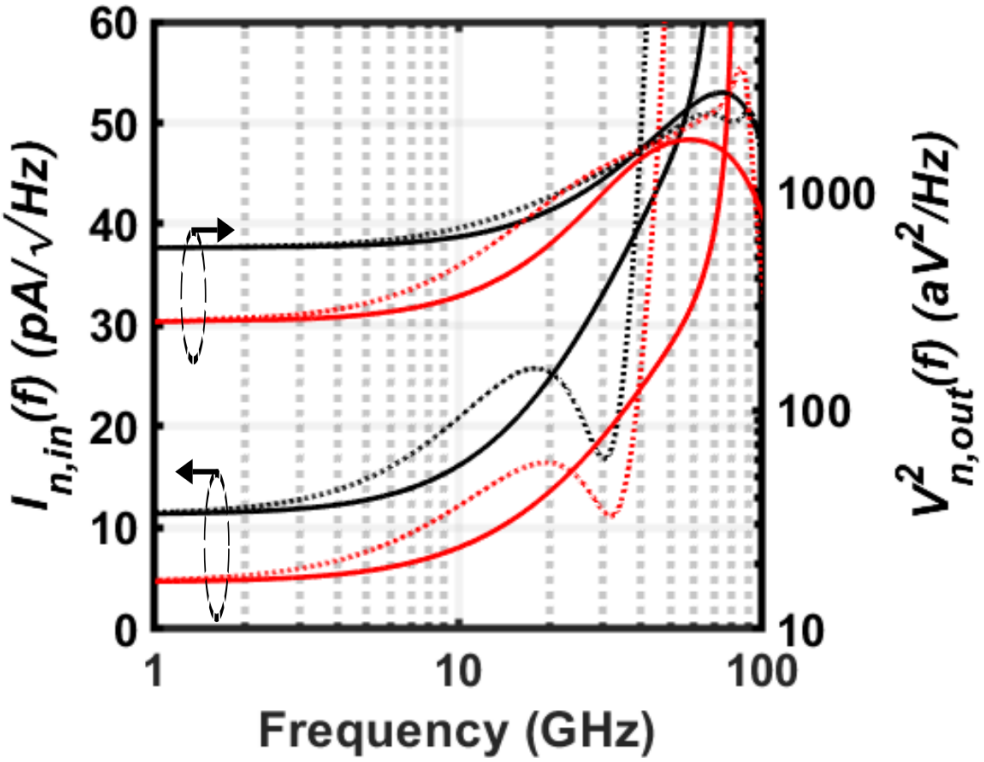


Figure 3.6: Simulated $I_{n,in}(f)$ and $V^2_{n,out}$ at maximum gain settings. The low-R_F TIA is plotted in black and the high-R_F TIA is plotted in red. The solid line indicates the de-embedded TIA performance, and the dotted line represents the TIA with $L_{WB,OUT} = L_{WB,PD} = 250$ pH, $C_{PD} = 80$ fF, and $R_{S,PD} = 5\ \Omega$. Note: the frequency response plots are characterized for the differential testbench illustrated in the inset of (a).

$$A_{v,OB}(s) \approx \frac{R_L}{R_{CTLE}} \frac{(1+s\tau_{CTLE})(1+s\frac{L_{OUT}}{R_L})}{(1+s\frac{C_{CTLE}}{g_m})(2+s\frac{L_{OUT}}{R_L})} \tag{3.1}$$

where $\tau_{CTLE} = C_{CTLE}R_{CTLE}$.

The peaking in the OB frequency response is due to the zero provided by the CTLE network and compensates for the frequency response roll-off of the preceding receiver chain cascade. CTLE is also commonly used across wireline TX-based equalizers [76]. Post-TIA peaking techniques enables increased bandwidth with reduced IRNCD contributions over RXICs with wideband front-end TIAs [59], [27]. Furthermore, because the high-frequency equalization is not of an active feedforward equalization (FFE) architecture as in [64], the improvement in bandwidth performance is obtained at no additional costs in power.

The OB stage consumes 10 mA through a 3 V supply for a power consumption of 30 mW for both TIA variants.

The frequency response of the transimpedance gain, $Z_T(f)$, and noise spectral densities, $I_{n,in}(f)$ and $V^2_{n,out}(f)$, are plotted for the full low-R_F and high-R_F receive chains in Fig. 3.5 and Fig. 3.6. From Eq. 2.13a, the input referred noise current spectral density takes the form of $\alpha_0 + \alpha_2 f^2$. Figure 3.5 demonstrates the cases where (1) the RXIC is de-embedded assuming an ideal differential current source input, and (2) the receiver is assembled with a photodetector assuming the following parameters: $L_{WB,OUT} = L_{WB,PD} = 250$ pH, $C_{PD} = 80$ pH, and $R_{S,PD} = 5\ \Omega$. A few observations are made with respect to the high-frequency peaking around 30 GHz observed in $Z_T(f)$: (1) from 3 to 20 GHz, $I_{n,in}$ increases from the de-embedded TIA curve, (2) right around 30 GHz, there is a decrease in $I_{n,in}$ due to the resonance of C_{PD}, $C_{in,TIA}$ and $L_{WB,PD}$, and (3) above 30 GHz, $I_{n,in}$ increases rapidly due to the $Z_T(f)$ roll-off, indicating the

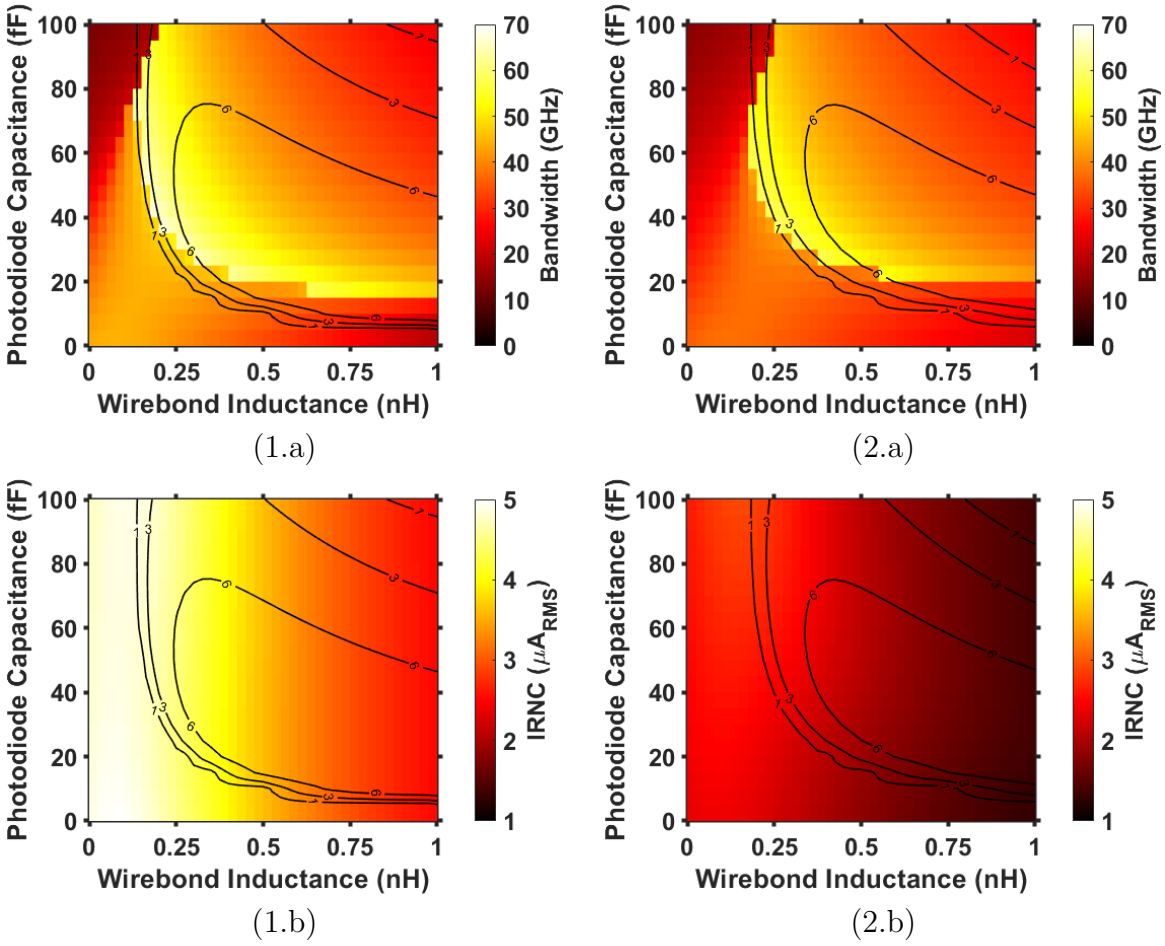


Figure 3.7: Simulated bandwidth and IRNC in Hz (color plots) and transimpedance gain peaking in dB (contour lines) for low-R_F variant (1.a-1.b) and high-R_F variant (2.a-2.b). Note: the VGA is set to maximum gain.

nominal f^2 noise region.

3.2.4 Characterizing the Optical Receiver Assembly

The C_{PD} and L_{WB} at the input and output have a significant impact on the overall bandwidth and noise of the receiver. There are constraints in the total wirebond length in the photodetector interface as well as the output of the TIA. Figure 3.7 illustrates the achievable bandwidths in GHz and IRNC in μA_{RMS} with transimpedance gain peaking in dB indicated by contour lines for various photodetector capacitance values and wirebond inductances at the input and output. Three assumptions are made. First, the relative lengths of both the input and output wirebonds; i.e. $L_{WB,PD} = L_{WB,out}$. Second, the photodiode capacitance lumps the total capacitance of $C_{PD} + C_{PD,pad}$. Third, a series resistance, $R_{S,PD} = 5\ \Omega$ is included in the photodetector model. It is critical that the assembly parasitics - $L_{WB,PD}$, $L_{WB,out}$, and C_{PD} - maintain less than 1-3 dB peaking in the transimpedance gain frequency response to ensure low deterministic jitter.

3.3 Measurements

The ORX variants were measured in two separate testbenches to characterize: (1) the electrical-only time-domain performance in a 50 Ω I/O impedance environment, and (2) the electro-optical time-domain performance with a photodetector assembly.

3.3.1 Electrical Measurements

The time-domain characterization of the ERXIC was carried out on a custom-designed FR-4 PCB assembly with 50-Ω test equipment. The PCB assembly for the ERXIC measurement presents roughly 5 dB loss at 40 GHz [77]. A bit pattern generator (BPG)

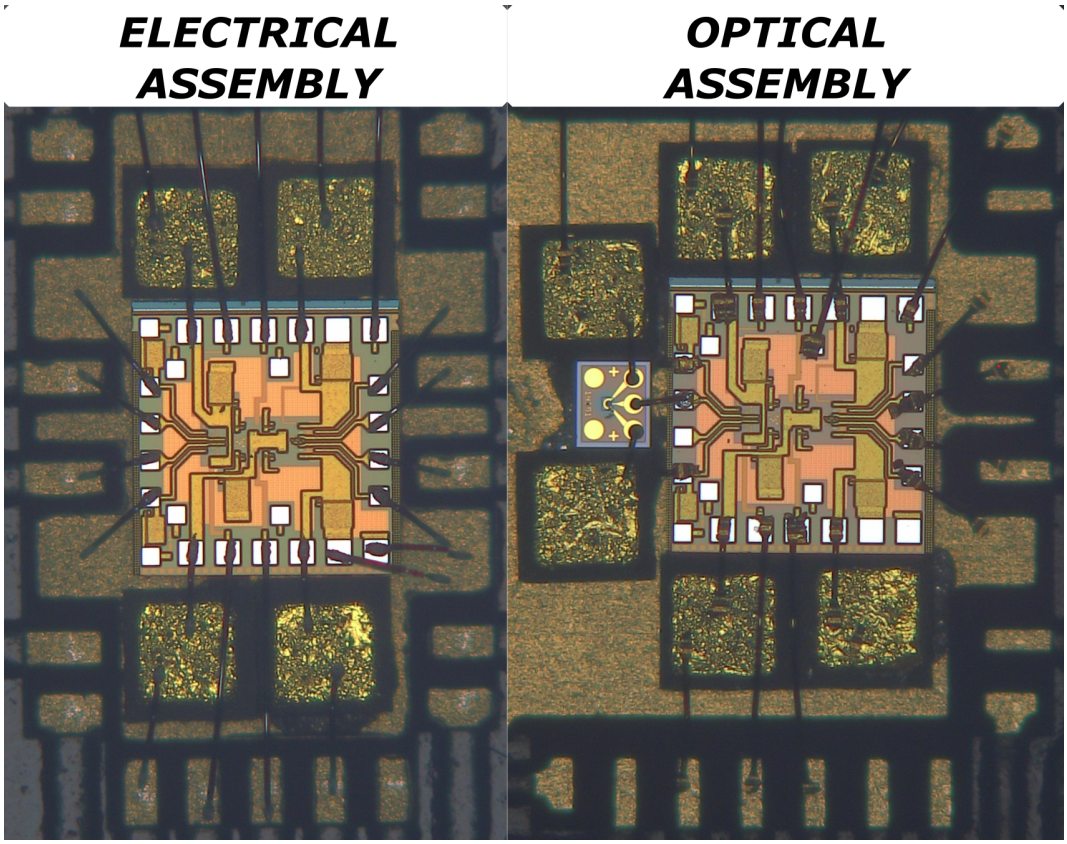


Figure 3.8: Chip microphotographs of the ORX variants with electrical/50 Ω and optical assemblies. Both ICs occupy 1 mm^2 including the padframe.

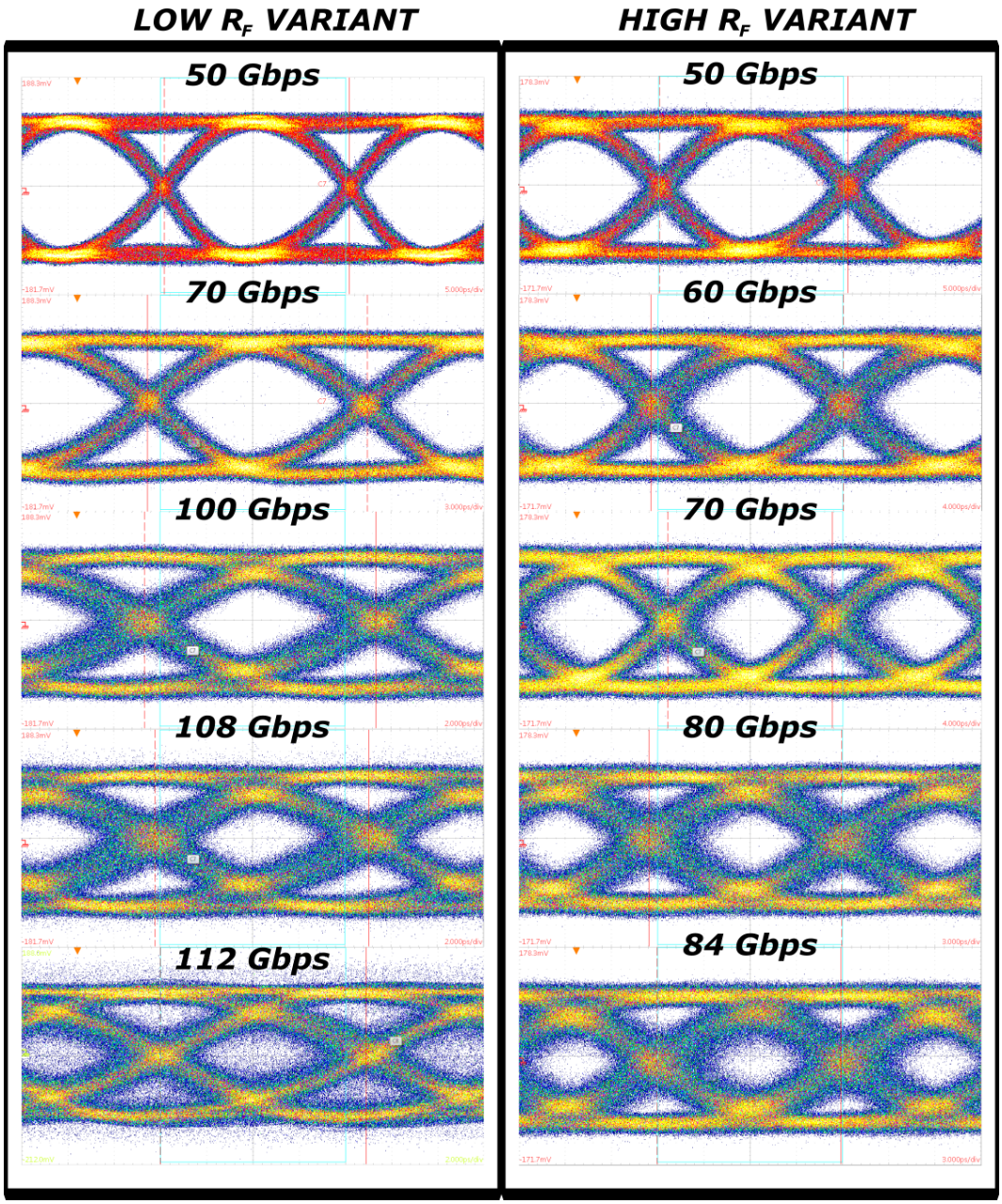


Figure 3.9: Eye diagrams for the two ORX variants in an electrical measurement setup. The measured single-ended output voltage swing is over 225 mV for both variants. A PRBS31 pattern was used with 200 waveform acquisitions performed.

(SHF 12105A) was synchronized with a synthesized clock generator (CG) (SHF 78212A) at full-clock rate in order to generate two independent data streams at a baseline data rate equal to the clock frequency. The single-ended data streams are then multiplexed (SHF 603A) through two 8-inch 67 GHz cables in order produce a differential NRZ waveform at double the data rate. The differential output of the multiplexer is attenuated to an amplitude as low as 100 mV and interfaced to the PCB assemblies through two 4-inch 67 GHz cables, 65 GHz mini-SMP connectors, and 5 mm PCB transmission lines. The ERXIC output was connected through a cascade of 5 mm PCB transmission lines, 65 GHz mini-SMP connectors, 4-inch 67 GHz cables, and a SHF DC blocking capacitors (SHF DCB-65R-A) with a cutoff frequency of 30 kHz, and observed through a Tektronix digital serial analyzer sampling oscilloscope (DSA8300) set to 70 GHz bandwidth through a sampling module (Tektronix 80E11) with a 2 meter extender (Tektronix 80X02). The inverted output was terminated to 50 Ω with an identical connector, cable, and DC block cascade. All electrical measurements were carried out in time-domain settings (i.e. eye diagrams and real-time bit error rate tests). Furthermore, assembly packaging and cable interfacing were not de-embedded or compensated (i.e. post-processing and/or scope equalization), and thus are captured in the measurements.

Fig. 3.9 demonstrates the single-ended output eyes of the ORX with a differential input. Notably, the low R_F variant can reach data rates up to 112 Gbps whereas high R_F variant reaches data rates up to 84 Gbps. At 112 Gbps, minimal bandwidth-induced eye closure is observed, however, clock distribution issues between the CG, BPG, MUX, and sampling scope deteriorated the eye diagram that prevented BER measurement. The nominally high impedance at low frequencies of the photodetector and capacitance will have a significant impact on the maximum data rate and sensitivity of the ORX variants.

The BER performance was measured using an SHF error analyzer (EA) (SHF 1104A). Fig. 3.10 demonstrates the BER bathtub performance of the low R_F variant for data

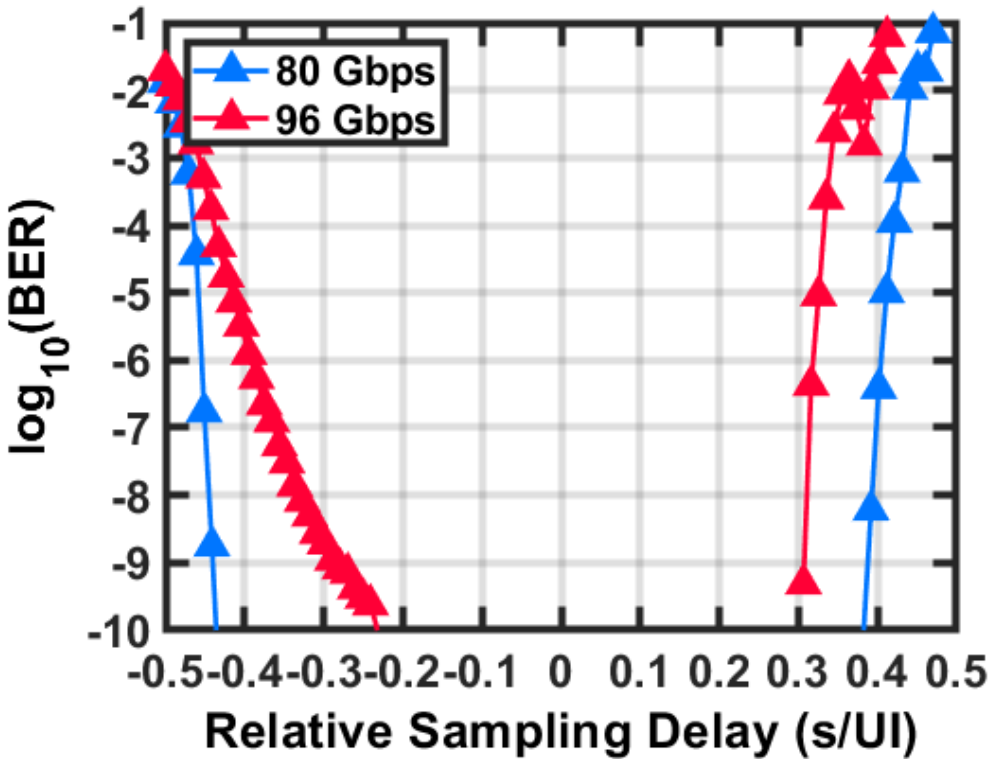


Figure 3.10: BER bathtub curves for the low-R_F variant in an electrical measurement setup. The input differential voltage swing was 100 mV_{pp} and a PRBS7 pattern was used.

rates of 80 and 96 Gbps. The BER measurements were configured to run a duration such that a confidence-level above 95% for a minimum of 10 errors at the target error rate of 10^{-11} is acquired. The BER measurements at data rates of Fig. 3.10 require the use of a demultiplexer (SHF 623A) to divide the data rate by a factor of two. The demultiplexer is driven differentially by the receiver IC outputs through 4 inch 67 GHz cables. The demultiplexer requires that the TIA output eye opening is at least 100 mV to register a BER of 10^{-09} up to 120 Gbps. When using the multiplexer and demultiplexer simultaneously with the BPG and EA, clock distribution limitations in our measurement setup prevent repeatable results above 96 Gbps.

3.3.2 Noise Measurements

The noise characterization of the ORX variants were carried out on the electrical assemblies shown in Fig. 3.8 to test the intrinsic noise performance of the ORX independent of the photodetector. The noise acquisition was carried out using the DSA vertical histogram function at a single output of the receiver through 4-inch 67 GHz cables with the inverted output terminated to 50 Ω. The maximum value of the DSA sampling scope bandwidth is 70 GHz. For the low R_F variant, this implies the measured value is just below the nominally required $2 \times BW$ integration limits to obtain the true $i_{n,rms}$. The standard deviation acquired by the histogram function is the measured integrated output noise voltage. The output noise voltages of the receiver variants are plotted against transimpedance gain settings in the upper plot of Fig. 3.11. The transimpedance gain is varied by tuning the VGA gain alone through $GC+$ and $GC-$ indicated by Fig. 3.3 with the RXIC bias currents and DC power consumption fixed. The noise voltage is multiplied by a factor of two to account for the differential output noise.

The input referred noise current (IRNC) and average input noise current density

Table 3.2: State-of-the-Art for NRZ-modulated TIA circuits measured with electrical input (50 Ω source).

Ref.	Technology	Bit rate (Gbps)	BW_{3dB} (GHz)	Z_T (dBΩ)	P_{DC} (mW)	$\sqrt{IRNCD}$ $(pA/\sqrt{Hz})$	FOM_{BW} $(\frac{Hz}{\mu A^2})$	FOM_{BR} $(\frac{bit\dot{Hz}}{2})$
[27]	130 nm SiGe HBT	100	66	65[1]	150	8	782[1]	1186[1]
	250 nm SiGe HBT	90	42	68.5[1]	150	7.6	745[1]	1596[1]
[41]	130 nm SiGe HBT	56	60	62.5[1]	85	5.5	941[1]	879[1]
[36]	130 nm SiGe HBT	112	65[2]	71	345	7.2	668	1152
[58]	0.18 μm CMOS	40	30.5	51	60.1	55.7	180	236
[21]	0.13 μm CMOS	40	30	55	45.7	51.3	201	277
Low R_F	**130 nm SiGe HBT**	**112**	**43.2**[3]	**66.3**[3]	**162**	**17.25**[4]	**551**	**1377**
High R_F	**130 nm SiGe HBT**	**84**	**35.2**[3]	**70.5**[3]	**138**	**12.86**[4]	**854**	**2039**

[1] differential transimpedance gain: $Z_{T,diff} = 2Z_T = \Delta V_{out}/(\Delta I_{in}/2$, [2] extracted s-parameters with 65 fF photodiode capacitance and 165 pH wirebond inductance [3] extracted from simulated $Z_T(f)$ of de-embedded RXIC, [4] calculated from twice the measured rms output noise voltage and the simulated $Z_T(f)$

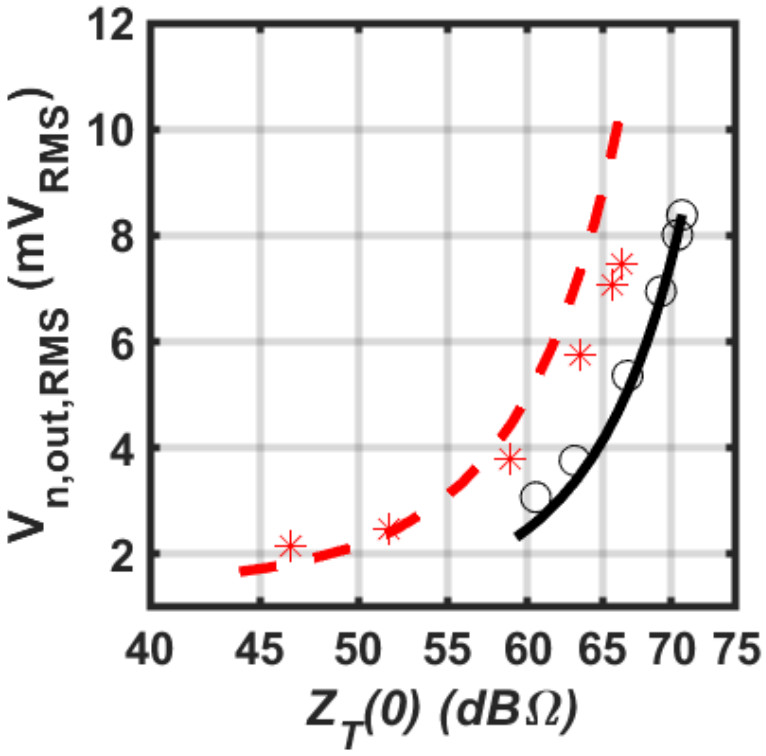


Figure 3.11: Differential output rms noise voltage vs. total transimpedance gain. The dashed curves and '*' markers correspond to the simulated and measured quantities for low-R_F variant and the solid curves and 'o' markers correspond to the simulated and measured quantities for the high-R_F TIA.

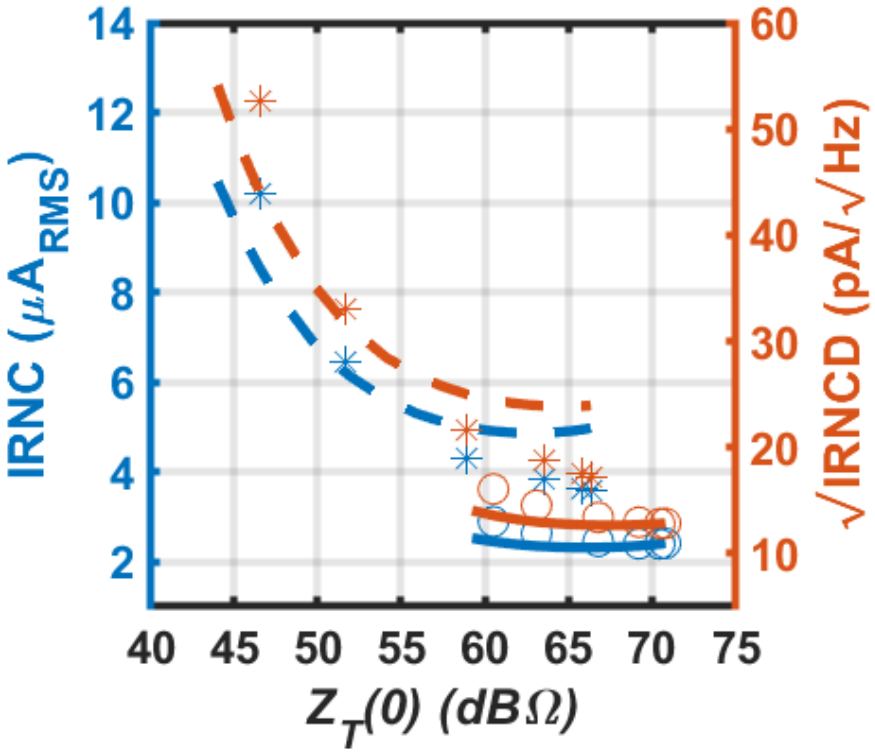


Figure 3.12: IRNC and $\sqrt{IRNCD}$ vs. total transimpedance gain. The dashed curves and '*' markers correspond to the simulated and measured quantities for low-R_F TIA and the solid curves and 'o' markers correspond to the simulated and measured quantities for the high-R_F TIA.

(IRNCD) are determined from

$$IRNC = i_{n,rms} = \frac{1}{R_T}\sqrt{2\int_0^{2BW} v_{n,out}^2(f)df} \tag{3.2}$$

and (2.8). The IRNC and $\sqrt{IRNCD}$ are plotted in Fig. 3.12. There is substantial improvement in noise performance for high-R_F variant with notably consistent $i_{n,rms}$ across the VGA gain settings where the minimum gain point is set to the 0 dB VGA gain contribution. At maximum transimpedance gain, the measured IRNC and $\sqrt{IRNCD}$ are 3.59 μA_{RMS} and 17.25 $pA/\sqrt{Hz}$ for the low-R_F TIA, and 2.41 μA_{RMS} and 12.86 $pA/\sqrt{Hz}$ for the high-R_F TIA. At the minimum transimpedance gain, the measured IRNC and $\sqrt{IRNCD}$ are 10.19 μA_{RMS} and 52.53 $pA/\sqrt{Hz}$ for the low-R_F TIA, and 2.90 μA_{RMS} and 16.08 $pA/\sqrt{Hz}$ for the high-R_F TIA. The simulated bandwidth and transimpedance gain values at the corresponding VGA gain settings of the measured values were used to compute the IRNC and $\sqrt{IRNCD}$. The sensitivities of the receiver variants can also be predicted from the IRNC using (2.4).

For a bit error rate of 10^{-12} ($Q \approx 7$), and a responsivity, R, approximated as 1, we can predict the best possible receiver sensitivities in terms of optical modulation amplitude (OMA) as -13 dBm and -14.72 dBm for the low-R_F and high-R_F TIAs, respectively. It is expected that with a sub-unity photodetector responsivity, inter-symbol interference (ISI) due to bandwidth limitations of the assembly (i.e. photodetector capacitance (C_{PD}) and wirebond inductances), the overall sensitivity in OMA of the receiver will be degraded. For reference, a responsivity of 0.8 - the specified responsivity of the photodetector used to evaluate the electro-optical performance of the receiver variants - will lead to a best-case sensitivity degradation of approximately 0.97 dB ($\approx$ 1 dB) in OMA.

Table 3.2 demonstrates the performance of both RX variants when tested in a 50 Ω environment at both the input and output. Notably, the low-R_F variant demonstrates

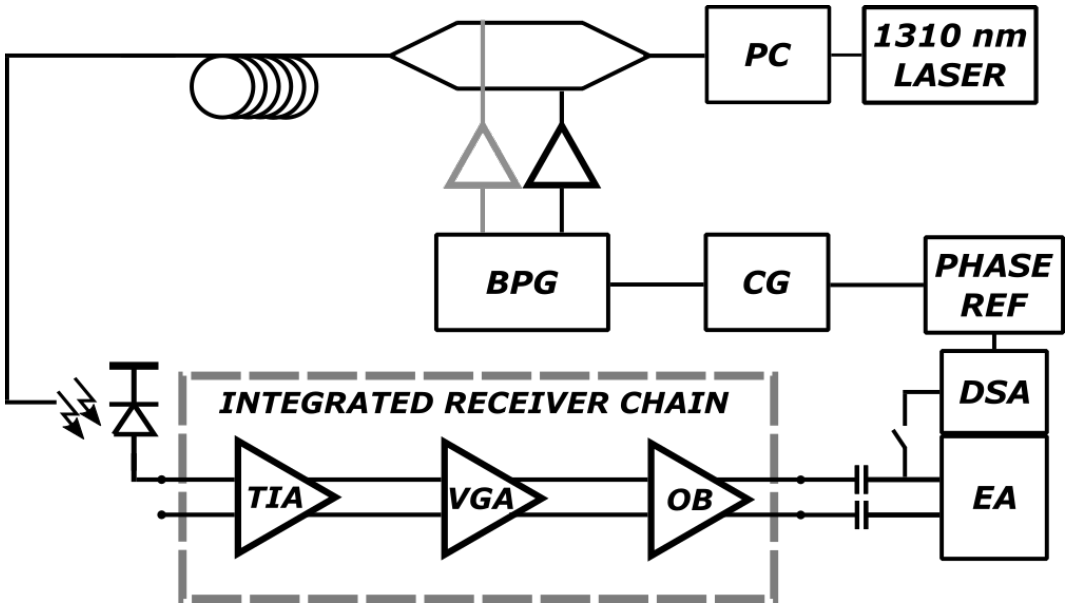


Figure 3.13: Block diagram of measurement setup for electro-optical characterization.

record NRZ data rate at a competitive energy efficiency when compared to the state of the art of TIA designs across SiGe HBT and CMOS technologies. Furthermore, the low-R_F variant achieves the third highest FOM_{BR} although it trails the state-of-the-art in FOM_{BW}. The high-R_F variant achieves the third highest FOM_{BW} and highest FOM_{BR} among the state-of-the-art. It is important to note that although Table 3.2 surveys TIAs in 50-Ω environments, the noise is reported in an open input configuration as described in Section 3.3.2.

3.3.3 Optical Measurements

The ORX variants assembled on a custom-designed FR-4 PCB with an InGaAs/InP photodetector specified with 0.8 A/W responsivity at 1310 nm and 38 GHz 3-dB BW. The PCB assembly for the ORXIC measurement presents roughly 4 dB loss at 40 GHz [77].

The ORX supplies and photodetector cathode are decoupled using off-chip 1.2 nF wirebondable capacitors to ensure a wideband ac-ground. The high-speed differential

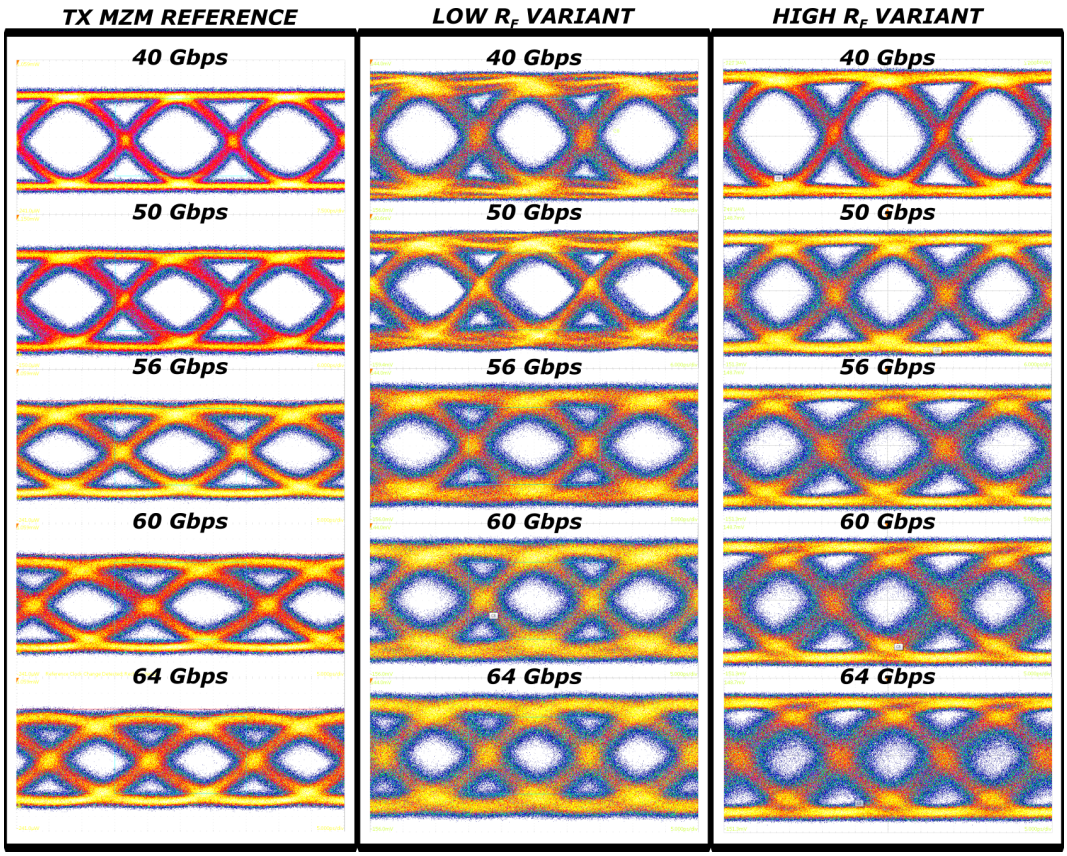


Figure 3.14: Eye diagrams for the two ORX variants in an optical measurement setup. The receiver eyes were taken at an average photodetector current of 150 μA. The MZM reference eye diagrams are shown to demonstrate that the two-tap equalization used simply compensates for the TX assembly bandwidth limitations alone and not the receiver ICs. A PRBS31 pattern was used with 200 waveform acquisitions performed.

output was wirebonded onto the 5 mm long 50-Ω PCB transmission lines tapped out by surface mount 65 GHz mini-SMP connectors. Fig. 3.8 demonstrates that the wirebond lengths along high-frequency paths and ac-ground nodes were kept at short lengths (less than 300 microns) to minimize inductive ringing and bandwidth throttling. All optical measurements were carried out in time-domain settings (i.e. eye diagrams and real-time bit error rate tests). Furthermore, assembly packaging and cable interfacing were not de-embedded or compensated (i.e. post-processing and/or scope equalization), and thus are captured in the measurements.

The optical NRZ waveform is generated by the BPG driving a Centellax amplifier (OA4SMM4) with 50 GHz bandwidth and 21 dB gain. Short 4 inch V-band-to-mini-SMP cables were used between the BPG and the Centellax amplifier. The amplifier then drives a Fujitsu 25 GHz $LiNbO_3$ Mach-Zehnder Modulator (MZM) through a single arm for data rates lower than 50 Gbps. For higher data rates up to 64 Gbps, the second arm of the MZM is driven using a two-tap feedforward equalization scheme reported in [78] such that the roll-off of the 25 GHz MZM is compensated to minimize the throttled bandwidth-induced ISI in the transmitter reference eye diagram. The MZM modulates a 1310 nm laser. The MZM has a central operating frequency at 1550 nm, however, the MZM exhibits a good response at 1310 nm. Short 4 inch V-band-to-mini-SMP cables were used between the Centellax amplifier and the MZM arms. A single-mode fiber is then used to couple light via a lensed fiber probe into the photodetector aperture.

The eye diagrams of the single-ended output of the receiver variants to the optical NRZ waveform at data rates between 40 Gbps and 64 Gbps are shown in Fig. 3.14. The reference transmitter eyes were taken using a 70 GHz optical sampling module from the DSA and it is clear across the data rates that there is some notable eye closure above 56 Gbps even with transmitter equalization. The low-R_F variant exhibits more eye opening up to 64 Gbps relative to the high-R_F variant, which exhibits eye opening to 60 Gbps.

Because the ORX front-end is intended for a balanced differential photodetector configuration, the single input photodetector DC current was manually compensated through the 2 kΩ resistor at the input of the TIA through a Keithley supply which is capable of current sinking. The inverted input was left open.

For BER measurements, short 4-inch 67 GHz cables were used between the BPG and the Centellax driver, between the Centellax driver and the MZM, and finally between the receiver IC and the EA. This reduction in cable assembly allowed us to minimize bandwidth degradation in the BER measurement setup. The ORXIC differential outputs

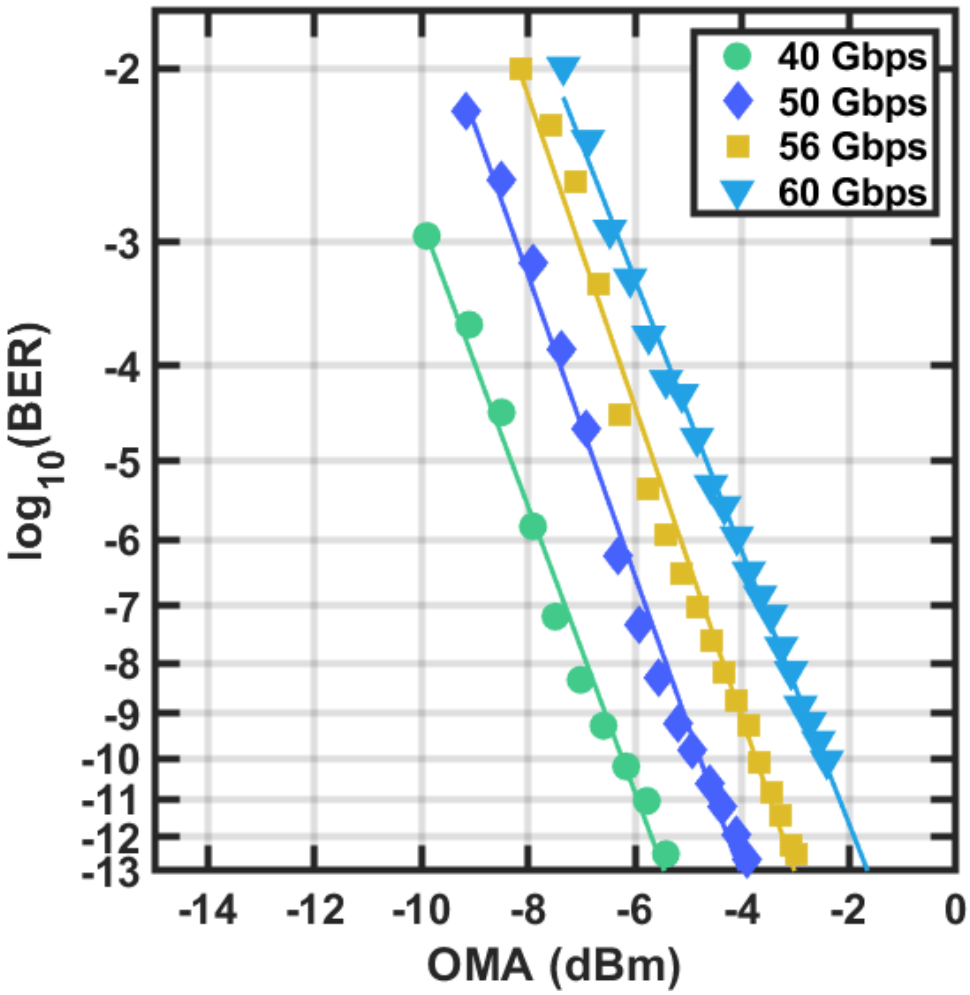


Figure 3.15: Sensitivity curves for the low R_F taken at data rates of 40, 50, 56, and 60 Gbps. A PRBS7 test pattern was used.

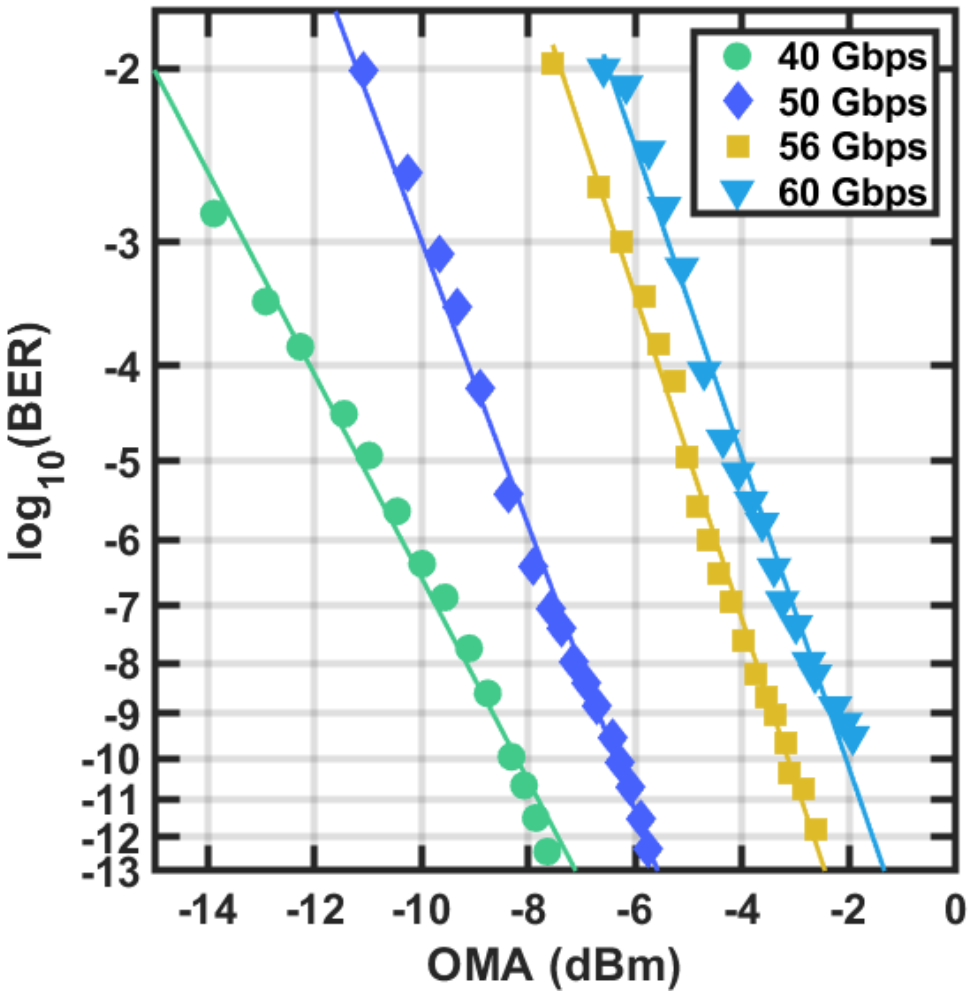


Figure 3.16: Sensitivity curves for the high R_F variant taken at data rates of 40, 50, 56, and 60 Gbps. A PRBS7 test pattern was used.

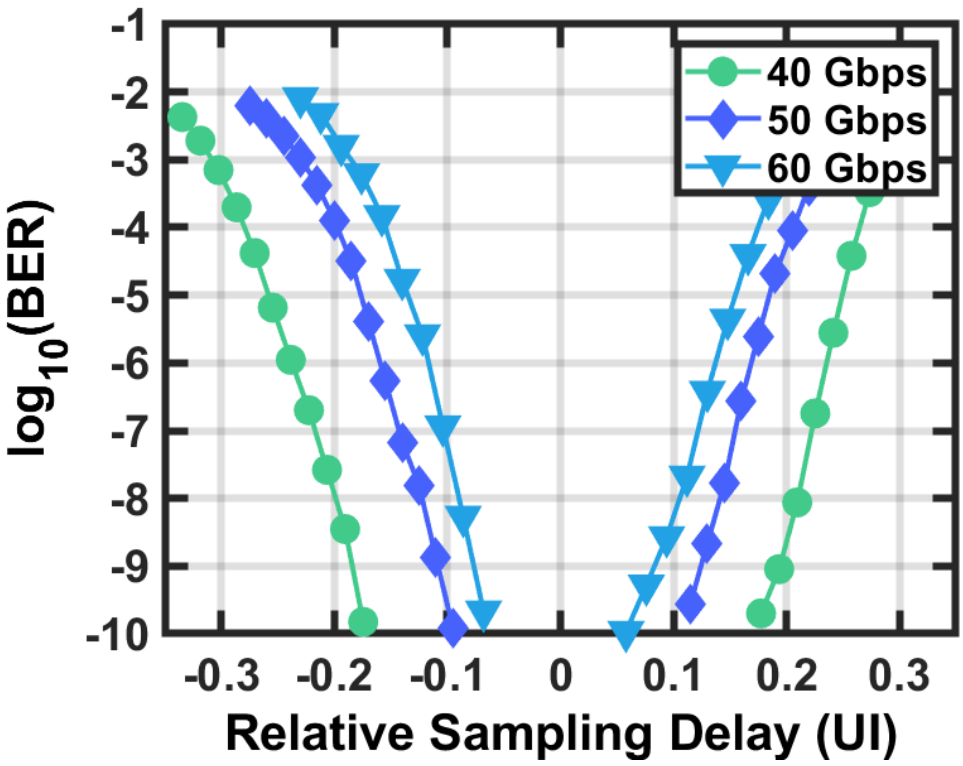


Figure 3.17: Bathtub BER curves for the low-R_F variant taken at 40 Gbps, 50 Gbps, and 60 Gbps. A PRBS7 test pattern was used.

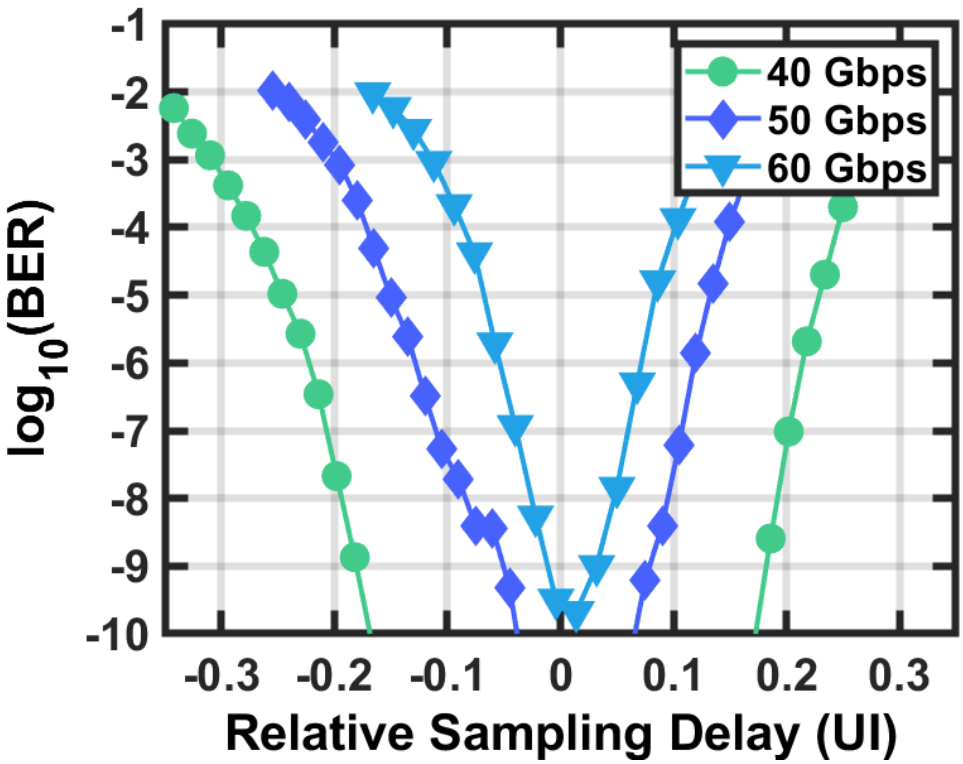
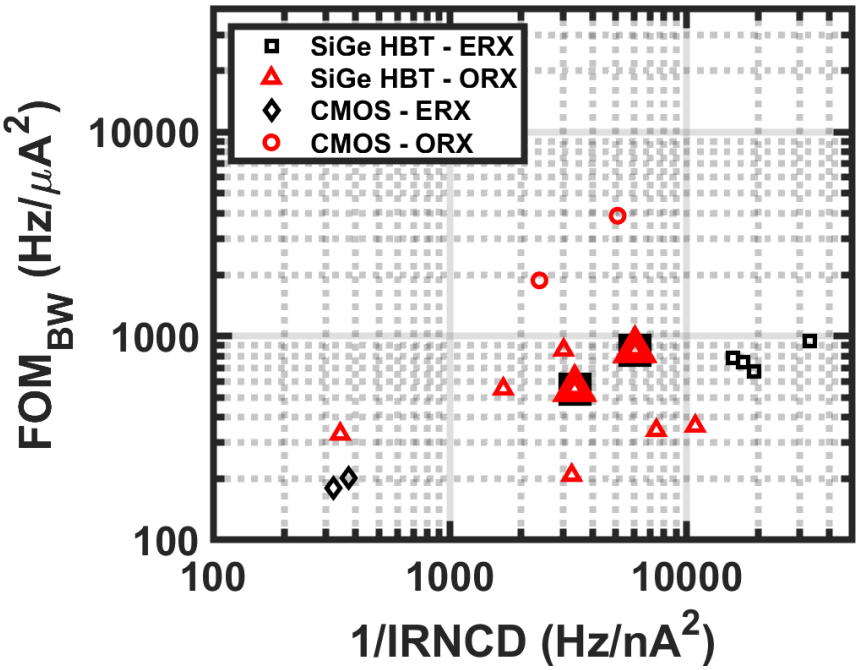
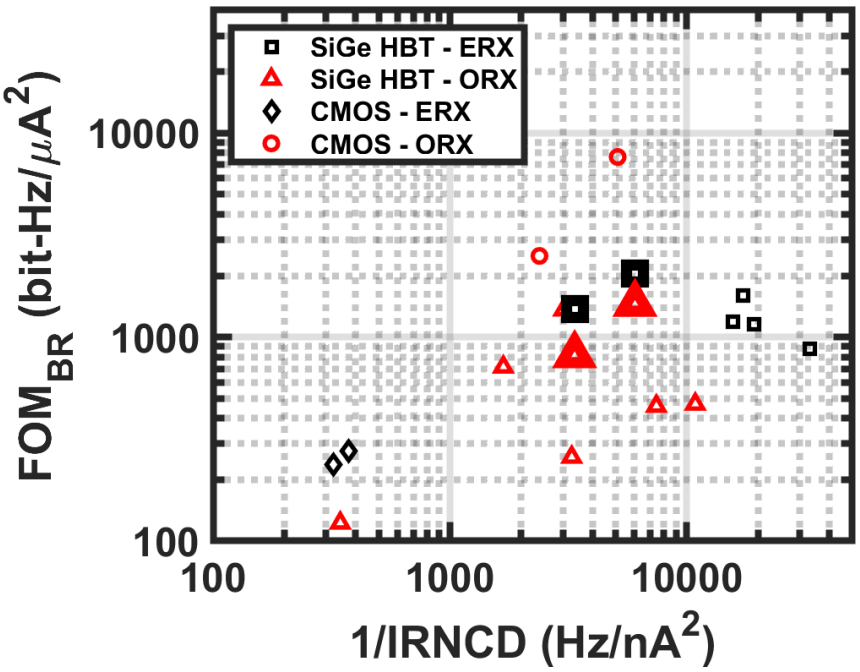


Figure 3.18: Bathtub BER curves for the high-R_F variant taken at 40 Gbps, 50 Gbps, and 60 Gbps. A PRBS7 test pattern was used.



(a)



(b)

Figure 3.19: Trends in state-of-the-art ERX and ORX (a) FOM_{BW} vs. $1/IRNCD$ and (b) FOM_{BR} vs. $1/IRNCD$ performance across SiGe HBT and CMOS technologies for NRZ signaling. The enlarged markers represent the variants of this work.

were both connected to the EA in order to ensure the highest possible output voltage swing into the EA and to remove common-mode noise. The BER measurements were configured to run a duration such that a confidence-level above 95% for a minimum of 5 errors at the target error rate of 10^{-12} is acquired.

Figure 3.15 and Figure 3.16 demonstrate the sensitivity curves of the receiver IC at data rates of 40, 50, and 60 Gbps for the low-R_F variant and high-R_F variant, respectively. Notably, there is an improvement of about 2 dB in the sensitivity for the high-R_F variant at 40 Gbps and 50 Gbps. At 56 Gbps and 60 Gbps, the low-R_F performs better due to its higher bandwidth in the transimpedance frequency response. It should be noted that because the differential ORXICs are evaluated using a single photodetector as indicated in Fig. 3.13, there is a sensitivity penalty of 3 dB.

Figure 3.17 and Figure 3.18 demonstrate the BER bathtub curves of the receiver IC at data rates of 40, 50, and 60 Gbps for the low-R_F and high-R_F variants, respectively. Notably, there is roughly equal sampling phase margin at BER of 10^{-10} between the two variants in both variants. At 50 Gbps and 60 Gbps, the sampling phase margin improvements are roughly 0.1UI in the low-R_F variant.

Table 3.3 demonstrates the performance of both RX variants when tested in an optical link. Notably, the high-R_F variant demonstrates record FOM_{BW} and FOM_{BR} for NRZ-modulated SiGe HBT ORXICs up to 56 Gbps, and the third highest FOM_{BW} and FOM_{BR} behind the CMOS-based ORXICs [19] and [26]. Although the SiGe HBT ORXIC reported in [48] demonstrates the highest FOM_{BR} at 50 Gbps, the differential transmipedance gain definition considers a single photodetector driving current into the differential input (i.e. $Z_{T,diff} = 2Z_T = \Delta V_{out}/(\Delta I_{in}/2)$) which results in an increase of the calculated FOM_{BR} by a factor of 2 over the definition maintained in this work as indicated by the inset of Fig. 3.5.a (i.e. $Z_{T,diff} = Z_T = \Delta V_{out}/\Delta I_{in}$).

Table 3.3: State-of-the-Art comparison NRZ-modulated TIAs measured with optical input.

Ref.	Tech. Node	Bit rate (Gbps)	BW_{3dB} (GHz)	Z_T (dBΩ)	P_{DC} (mW)	$\sqrt{IRNCD}$ ($pA/\sqrt{Hz}$)	P_{SENS} @ 10^{-12} (dBm)	Pattern Type	FOM_{BW} ($Hz/\mu A^2$)	FOM_{BR} ($bitHz/\mu A^2$)
[38]	120 nm SiGe HBT	40/160[1]	108	47	73	53.9	N/A	PRBS31	331	123/492[1]
[50]	250 nm SiGe HBT	50[2]	40.3	48.9	54	17.5	-9[3]	PRBS31	208	258
		50[2]	37.6	53.9	54	11.6	-8[3]	PRBS31	345	459
		50[2]	38.6	54.1	54	9.6	-9[3]	PRBS7	362	469
[48]	55 nm SiGe HBT	50	N/A	75[4]	141	N/A	-12.4	PRBS9	N/A	1994[4]
		56	N/A	70[4]	141	N/A	-11.2	PRBS9	N/A	1256[4]
		90	N/A	65[4]	222	N/A	N/A	PRBS9	N/A	721[4]
[64]	130 nm SiGe HBT	71	N/A	N/A	860	N/A	-4.2/-10[5]	PRBS7	N/A	N/A
[19]	45 nm CMOS SOI	40	30	55	9	20.47	-16[6]	PRBS31	1874	2499
[26]	28 nm CMOS	53	27	74	34.8[7]	14[8]	-6	PRBS7	3889[7]	7633[8]
[69]	14 nm FinFET	64	25	N/A	96	N/A	-5.5	PRBS7	N/A	N/A
[70]	14 nm FinFET	50	N/A	N/A	215	N/A	-10.9	PRBS7	N/A	N/A
This work:										
Low R_F	**130 nm**	**56**[9]	**43.2**[10]	**66.3**[10]	**162**	**17.25**[11]	**-3.2/-13**[11]	PRBS7	**551**	**714**
High R_F	**SiGe HBT**	**56**[9]	**35.2**[10]	**70.5**[10]	**138**	**12.86**[11]	**-2.6/-14.7**[11]	PRBS7	**854**	**1359**

[1] extracted using PD model and measured s-parameters, [2] with 2-Tap FFE in TX, [3] measured at 20 Gbps, [4] differential transimpedance gain: $Z_{T,diff} = 2Z_T = \Delta V_{out}/(\Delta I_{in}/2$, [5] -10 dBm OMA is for 40G, [6] calculated from rms output noise voltage and frequency response, [7] without output buffer power consumption, [8] calculated from reported $i_{n,in}$ and bandwidth, [9] open eyes measured up to 64 Gbps, [10] simulated $Z_T(f)$ of the standalone RXIC, [11] calculated from measured noise histogram and simulated frequency response.

3.4 Trends in the State of the Art in Optical Receiver Design

The analysis of 2.1.1 presented an link-loss-based analysis which allows us to visualize the energy efficiency trade-offs in terms of the FOMs defined by (2.2) and (2.3), as well as the noise performance (i.e. $\sqrt{IRNCD}$) defined by (2.8). This analysis allows for a comprehensive survey of the state of the art in ORX designs with respect to the widely-reported performance parameters that include: transimpedance gain, 3-dB bandwidth, bit rate, DC power consumption, and IRNCD.

Figure 3.19 plots the FOMs defined in (2.2) and (2.3) with respect to the inverse IRNCD for the state of the art in NRZ-modulated receiver ICs referenced in Table 3.2 and Table 3.3 across SiGe HBT and CMOS technologies.

Figure 3.19.a plots the FOM defined in (2.2) as a function of the inverse squared IRNCD for state of the art in receiver ICs. Alternatively, Figure 3.19.b uses the FOM defined in (2.3). These plots would place an ideal ORX on the top right corner as illustrated in Fig. 2.2; i.e. lower noise is indicated on the right half of the plot, and higher efficiency is indicated on the top half of the plot which allows for observation of the trends of ORX metrics across various processes.

3.5 Conclusion

This paper discusses optical receiver characterization for minimum power consumption through the use of the transimpedance figure of merit and input-referred noise current density. We demonstrate two prototypes based on a Cherry-Hooper TIA and Gilbert-cell VGA that explore different trade-offs in the transimpedance FOM and noise. Measurements indicate record data rates up to 112 Gbps and error-free (i.e. $10^{-}10$) up to 96 Gbps

for the ERX in a 50 Ω environment. Furthermore, the highest FOM_{BW} and FOM_{BR} are reported for NRZ- and SiGe HBT technology-based ORXICs. Compared to prior literature, the RXIC designs presented in this work offer competitive FOM_{BW}-$IRNCD$ and FOM_{BR}-$IRNCD$ performance against SiGe HBT and CMOS ERXICs and ORXICs.

Chapter 4

Towards an Analog Coherent QPSK Optical Receiver

This chapter is in part a reprint of material in the manuscript, "A 50-GBaud QPSK Optical Receiver with a Phase/Frequency Detector for Energy-Efficient Intra-data Center Interconnects," published in the IEEE Open Journal of the Solid-State Circuits Society.

This paper describes the energy-efficient realization of an analog coherent optical receiver (CoRX) for short-reach intra-datacenter interconnects. The CoRX comprises inphase and quadrature channels for each polarization and a high-speed phase-frequency detector (PFD) that provides feedback to stabilize an optical local oscillator (LO) and maintain coherence with the received optical signal. Each receive (RX) channel consists of a transimpedance amplifier (TIA) based on a Cherry-Hooper emitter follower (CHEF). The electronic RX is implemented in a 130-nm SiGe HBT technology (f_T = 300 GHz), consumes 534 mW of DC power for a total electrical RX energy efficiency of 5.34 pJ/bit, and occupies 2.8 mm^2. Electrical characterization of the CoRX on an FR-4 PCB assembly demonstrates operation up to 60 GBaud with a bit error rate (BER) of less than 10^{-12}. A co-packaged optical/electrical CoRX assembly with a silicon photonic receiver

is characterized using a commercial-off-the-shelf quadrature phase-shift keying (QPSK) transmitter for constellations up to 50 GBaud (100 Gbps) at BER below KP4-FEC (2.2×10^{-4}).

4.1 Introduction

Intra-data center (IDC) interconnects are trending toward aggregate data rates between 200 to 400 Gbps per wavelength for mid-reach lengths (< 2 km). Scaling current intensity modulated direct detection (IMDD) links to these data rates will require higher-order pulse-amplitude modulation (PAM) formats, e.g. 4-PAM, in which energy efficiency improvements would be challenging due to more severe link loss requirements [79]. Coherent links using QPSK or 16-QAM have been proposed to scale future IDC link data rates. Conventional long reach coherent links rely heavily digital signal processing (DSP) to track and correct frequency and phase of the received signal, as well as to compensate for fiber impairments. Digital coherent schemes using 56 Gbaud dual-polarization (DP)-QPSK and 28 Gbaud DP-16QAM require analog-to-digital converters (ADCs) with high sampling rates (112 GS/s and 56 GS/s, respectively) and high effective number of bits. These ADCs currently consume nearly 2.8 W (0.7 W per ADC) for a 224 Gbps (112 Gbps per polarization) coherent RX, adding 12.5 pJ/bit of power consumption [80].

Forgoing high-resolution ADCs and related DSP functions for short-reach coherent links is an attractive approach to implement future low cost and low power consumption IDC links. A DSP-free DP-QPSK CoRX architecture has been determined to incur a small power penalty of 1 dB with respect to digital coherent counterparts in the low chromatic dispersion regime (i.e. sub 10-km scale IDC scale links) [81]. Furthermore, a recent link budget analysis has demonstrated that analog coherent detection (ACD) simultaneously improves the sensitivity of the RX through additional unallocated link

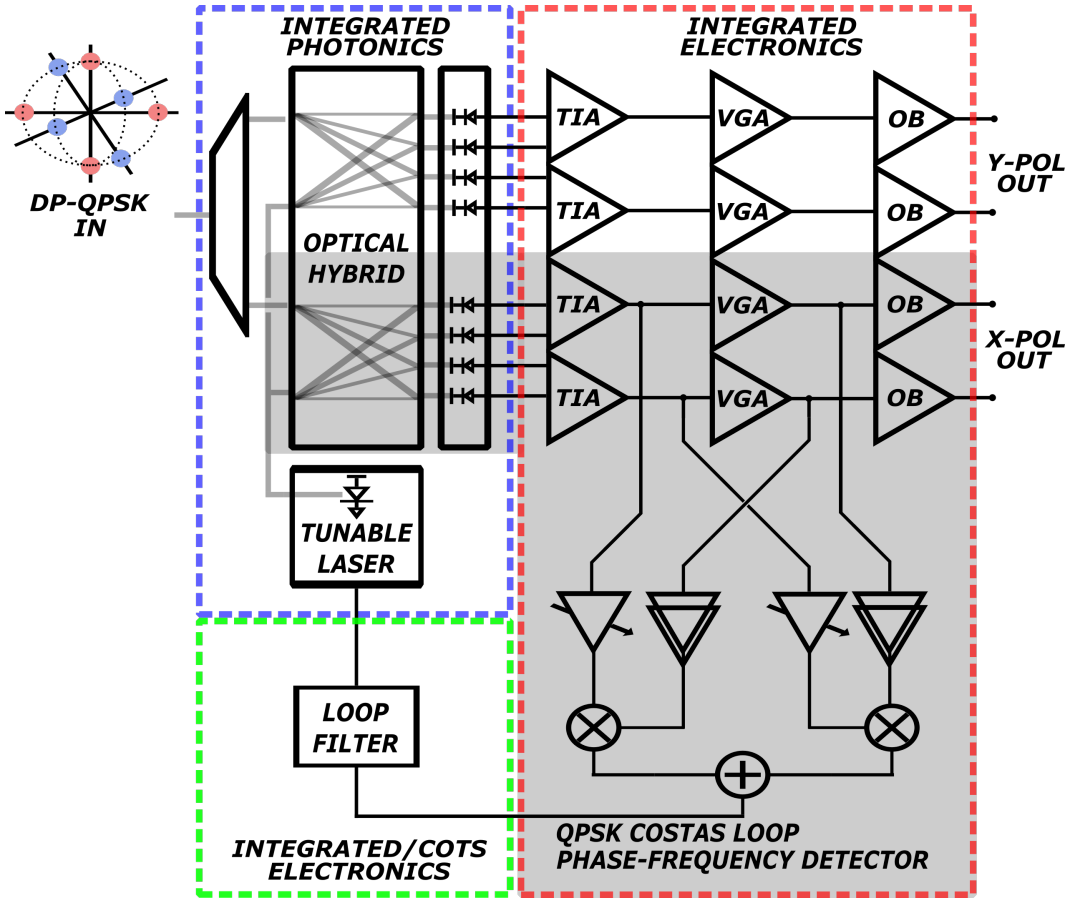


Figure 4.1: Illustration of a DP-QPSK analog CORX architecture using an OPLL. Here, we describe a single-polarization I/Q photonic and electronic receiver (RX) and QPSK Costas loop phase-frequency detector as shown in the shaded gray region.

budget and should be able to reach an energy efficiency under 5 pJ/b [11]. ACD circumvents the need for such high-resolution and power-hungry ADCs by delegating the amplitude-leveling, carrier recovery and phase estimation using the optical phase-locked loop (OPLL).

Figure 4.1 illustrates a block diagram of a DP-QPSK analog CoRX comprising a photonic integrated circuit (PIC) and an electronic integrated circuit (EIC). The PIC consists of an optical hybrid that splits the received optical signal into quadrature components and mixes the signal with the optical LO in a photodetector. The EIC consists of a pair of I/Q channels and a Costas loop to support the OPLL. The Costas phase-frequency detector (PFD) tunes the laser to track the phase and frequency of the received optical signal.

This work presents a CoRX based on a PIC and EIC that supports QPSK. In earlier work, the receiver channel was characterized electrically at NRZ data rates up to 108 Gbps and energy efficiencies as low as 1.5 pJ/bit, and optically in a 1310 nm direct-detection link at NRZ data rates up to 64 Gbps and energy efficiencies as low as 2.53 pJ/bit [16], [14]. Recent results report energy efficiencies for CoRXs that range from 4.33 to 6.8 pJ/bit but have not implemented the PFD [37], [39], [40].

This paper presents a dual-channel 50 GBaud (100-Gbps) CoRX for single-mode fiber interconnects in a 130-nm Silicon-Germanium (SiGe) process. Section II reviews the requirements of analog coherent optical receivers. Section III presents an energy efficiency for the ACD scheme and demonstrates fundamental energy efficiency limits and relationships to figure of merits (FOM) and input referred current noise density for the EIC. Section IV presents the design of the CoRX PIC and EIC. Section V details an optical phase locked loop model to predict frequency response and residual phase error. Section VI presents the electrical and optical measurements to show the performance at the FEC limit BER and comparison to the state of the art. The reported results

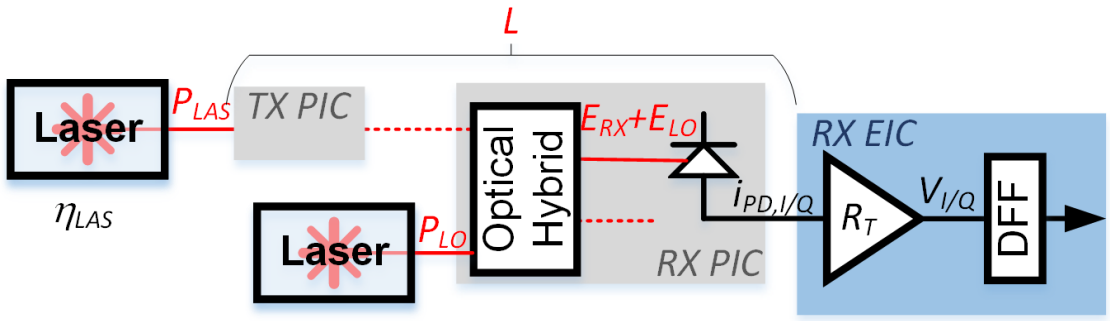


Figure 4.2: Illustration of link analysis parameters used in calculating energy efficiency

demonstrate the lowest energy efficiency and average input-referred noise current density for coherent detection.

4.2 QPSK Coherent Optical Receivers

The CoRX illustrated in Figure 4.1 indicates a total of four differential channels - two differential I/Q channels in each of the X/Y polarizations. The CoRX is implemented for a single polarization with parameters used in the CoRX analysis in Fig. 4.2. The received optical signal after the hybrid in the I and Q channels is written in terms of the RX and LO electric field terms.

$$E_{RX}(t) = \sqrt{P_{RX}(t)}e^{j(\omega_{RX}(t)+\phi_{RX}(t))} \tag{4.1a}$$

and

$$E_{LO}(t) = \sqrt{P_{LO}(t)}e^{j(\omega_{LO}(t)+\phi_{LO}(t))} \tag{4.1b}$$

The photodetector (PD) I/Q channel current is

$$i_{PD,I\pm} = 0.25\mathcal{R}(P_{OPT} \pm P_S\cos(\Delta\omega t + \Delta\phi(t))) \tag{4.2a}$$

and

$$i_{PD,Q\pm} = 0.25\mathcal{R}(P_{OPT} \pm P_S \sin(\Delta\omega t + \Delta\phi(t))), \tag{4.2b}$$

where $P_{OPT} = P_{RX} + P_{LO}$ is the optical input power to the RX and LO ports, $P_S = 2\sqrt{P_{RX}(t)P_{LO}}$ is the optical signal power, R is the PD responsivity, $\Delta\omega$ is the beat frequency between ω_{LO} and ω_{TX}, and $\Delta\phi(t)$ is the time-varying phase due to the received symbol and systematic perturbations and noise; that is, $\Delta\phi(t) = \phi_{sym}(t) + \phi_{noise}$.

A key advantage of a coherent architecture is the enhancement of the overall RX sensitivity due to the multiplicative contribution of the LO laser power allowing for reduced P_{RX} below the sensitivity that would be found for direct detection receivers [82].

When the $\Delta\omega$ is zero, the CoRX recovers the QPSK signal according to $\phi_{sym} = \frac{\pi}{2}(1 + m_I)$ for the I channel and $\phi_{sym} = \frac{\pi}{2}(2 + m_Q)$, where $(m_I, m_Q) = (\pm 1, \pm 1)$. We use a pair of TIAs and LAs to amplify the I and Q channels separately. Consequently,

$$V_{I/Q} = R_T i_{PD,I/Q} = \frac{1}{4} P_S \mathcal{R} R_T m_{I/Q} \tag{4.3}$$

where R_T is the transimpedance of the CoRX.

In order to achieve the homodyne operation ($\Delta\omega = 0$), the LO and TX phase and frequency must be locked. OPLLs based on a Costas loop have been demonstrated as a suitable solution for homodyne BPSK links up to 40 Gbps [83], [84]. To accommodate phase-and-frequency locking for QPSK optical waveforms, a QPSK Costas loop must be implemented. The ideal QPSK Costas loop is defined as

$$v_{PFD} = K_{PFD}(V_Q \cdot SGN(V_I) - V_I \cdot SGN(V_Q)), \tag{4.4}$$

where $SGN(x)$ is the sign function of the input argument x with bounds of ± 1.

The PFD is characterized with a sensitivity characteristic visualized in the I and

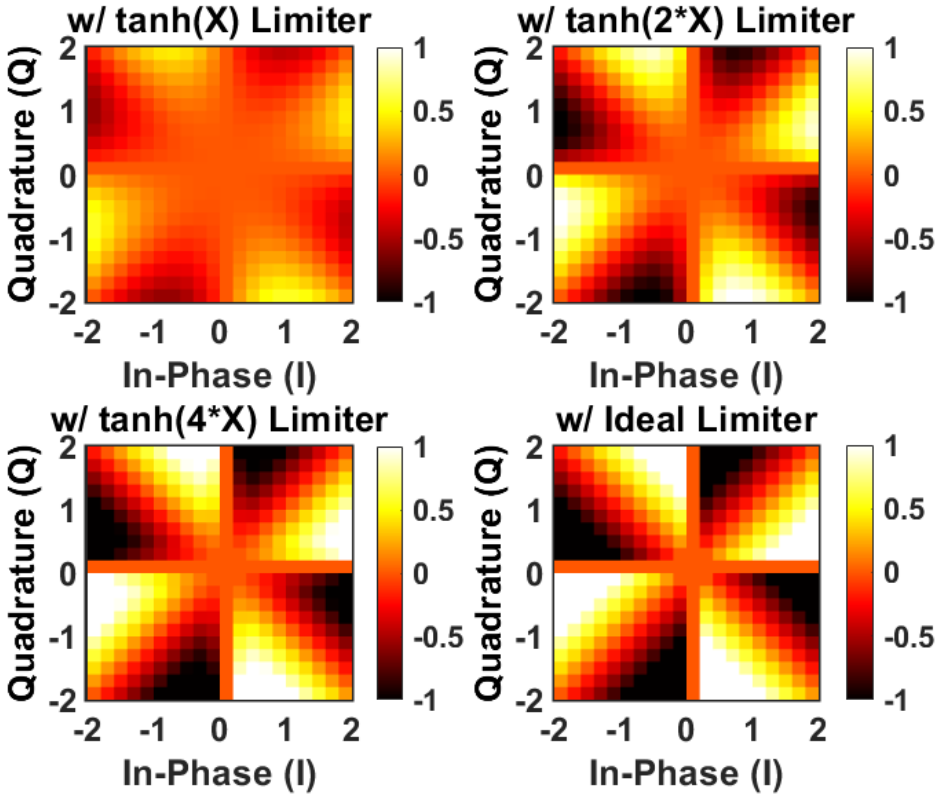


Figure 4.3: Normalized QPSK Costas Loop characteristic with respect to the I/Q domains with for various nonidealities in the limiting stage.

Q plane in Fig. 4.3. The diagonal indicates the equilibrium points of the QPSK. Alternatively, the characteristic can be traced along the unity circle in which the constellation symbols are mapped and the voltage response results in a sawtooth function. Fig. 4.3 indicates how a hyperbolic tangent approximation of the limiting function, e.g. $SGN(X) \approx tanh(\alpha X)$, impacts the sensitivity K_{PFD}. Consequently, the Costas loop must be driven with a strong limited response to generate the desired PFD response.

Analog CoRX using an OPLL is enabled in part by high levels of integration of the PIC, EIC, and loop filter components. In particular, for an OPLL to maintain stable operation, the loop delay and loop bandwidth trade off according to the following relation, $\omega_n \tau < 0.736$ [85]. InP-based PICs with monolithically integrated tunable lasers

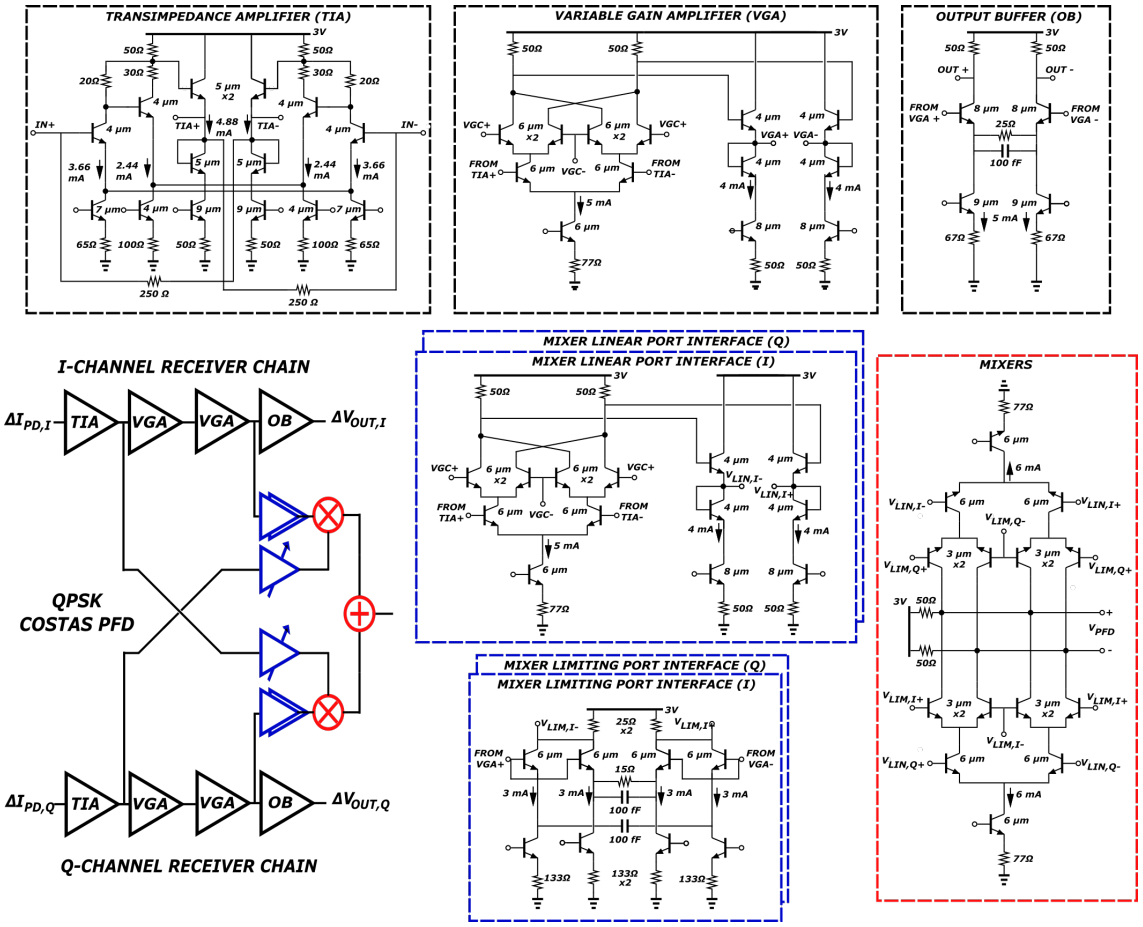


Figure 4.4: Schematics of the implemented single-polarization QPSK CoRX. The receiver chain consists of a TIA stage, two cascaded VGA stages, and an output buffer. The Costas PFD is comprised of two mixers which include a linear port interface and a limiting port interface.

have enabled OPLLs with loop delays as low as 120 ps and loop bandwidths as high as 1.1 GHz [83], [84].

4.3 Coherent Receiver Integrated Circuit Design

4.3.1 Transimpedance Amplifier

The RX circuit consists of two functional blocks: a dual-channel (I/Q) channel and a QPSK Costas PFD to stabilization of the OPLL. The receive chain builds on recently

reported work in [16] and [14], and includes a TIA, a two-stage variable-gain amplifier (VGA), and an output buffer (OB). The schematics of the RX EIC is illustrated in Fig. 4.4 and details the TIA, VGA, and OB stages. The transimpedance gain is found from the cascade of these three stages.

$$Z_T(s) = \frac{V_{OUT}(s)}{I_{IN}(s)} = Z_{TIA}(s)A_{v,VGA}(s)A_{v,OB}(s) \tag{4.5}$$

The first stage is based on a Cherry-Hooper shunt-feedback TIA with $Z_{TIA} = R_F\frac{A_V}{1+A_V}$ with a g_m-Z_T cascade followed by an emitter follower buffer as shown in Fig. 4.4. The VGA gain is distributed by a cascade of Gilbert cells which provide a maximum gain of $A_{v,VGA} \approx (g_m R_L \cdot g(\Delta V_{GC}))^2$ where $g(\Delta V_{GC})$ represents the gain control of the Gilbert cell which allows for 21 dB of gain tuning range. Finally, the output buffer gain is $A_{v,OB}(s) \approx \frac{R_L}{R_{CTLE}}\frac{(1+s\tau_{CTLE})(1+s\frac{L_{OUT}}{R_L})}{(1+s\frac{C_{CTLE}}{g_m})(2+s\frac{L_{OUT}}{R_L})}$, where $\tau_{CTLE} = C_{CTLE}R_{CTLE}$.

Based on the noise in the TIA stage, the EIC sensitivity is expected to be dominated by the feedback resistor noise,

$$\frac{\overline{i^2}}{\Delta f} = \frac{4kT}{R_F} + 2qI_b + \frac{4kT\Gamma}{g_m}\omega^2(C_{BE} + C_{BC} + C_{PD})^2. \tag{4.6}$$

Considering a high β SiGe HBT device, the dominant input-referred noise current source at low frequency is due to R_F.

The simulated transimpedance gain and noise spectral densities are illustrated in Fig. 4.5 with and without the packaging parasitics. The total achievable transimpedance gain ranges from a minimum of 46.2 dBΩ with a bandwidth that exceeds 30.6 GHz and a maximum of 67.2 dBΩ with a bandwidth that exceeds 35.2 GHz. The input-referred noise current spectral density of the differential TIA, $I_{n,in}(f)$ is plotted in the bottom of the figure and demonstrates that effective feedback resistance is 250 Ω, indicating

that the g_m-Z_T core of the TIA contributes negligible noise compared with the feedback resistance. At higher frequencies (i.e. > 10 GHz) , circuit parameters (i.e. g_m, C_{BE}, and C_{BC}) dominate the high-frequency noise contributions.

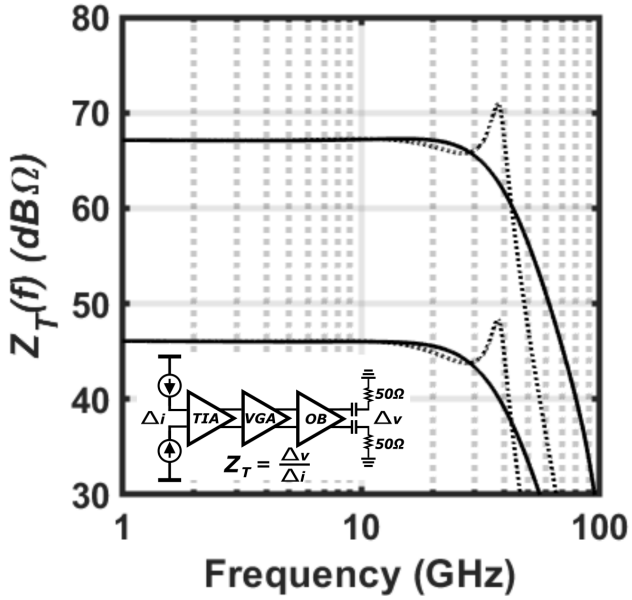
4.3.2 Costas PFD

The QPSK Costas loop uses two mixers where the inputs of the two mixers are driven by the outputs of the TIA and VGA stages in both I- and Q-branches through interfacing circuits detailed in Fig. 4.6. The output of the two mixers is then differenced in the current mode as demonstrated in the schematic of Fig. 4.4 to generate the feedback signal to the loop filter in the coherent RX as illustrated in Fig. 4.1.

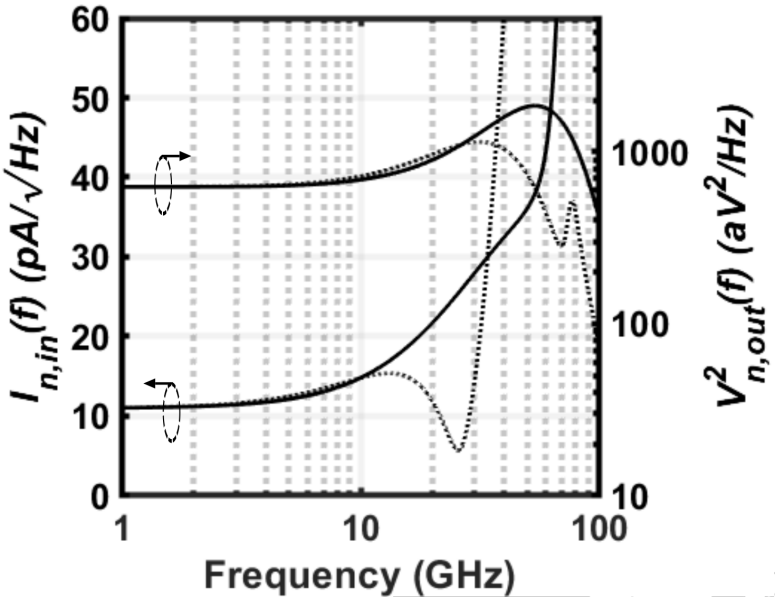
The ideal QPSK Costas PFD sawtooth behavior can be observed in two cases which involve tracing the unity circle of the characteristic plotted in Fig. 4.3 through (1) an I/Q beat-tone stimulus, or (2) rotation of the received QPSK constellation. Fig. 4.6 demonstrates the simulated sawtooth characteristics in both cases. From the latter case, by observing the average output voltage of the Costas PFD, K_{PFD} can be determined as 117 mV/rad. At high-speeds (e.g. 50 Gbaud), the ideal Costas behavior is difficult to realize due to the high harmonic content required to generate a sawtooth waveform in the PFD response. Fig. 4.7 demonstrates the transient waveforms of the Costas PFD at various constellation rotations. The PFD under different VGA settings produces a linear gain coefficient between 3.5 mV/GHz to 7 mV/GHz.

4.3.3 RX PIC

Previous work has demonstrated Silicon Photonic (SiPh) DP-QPSK RX PICS operating up to 112 Gbps [86]. The PIC in this work is realized in the GF 9WG SiPh process and consists of a polarization splitter/rotator (PSR), optical hybrid (OH), and



(a)



(b)

Figure 4.5: Frequency response of the EIC (a) transimpedance gain at minimum and maximum VGA gain settings and (b) input and output noise spectral densities at the maximum VGA gain setting in a de-embedded (solid) and packaged (dotted) configuration (i.e. input and output wirebond inductances of 600 pH and a photodiode capacitance of 40 fF are included). Note: the inset of (a) illustrates the evaluated testbench and transimpedance gain definition.

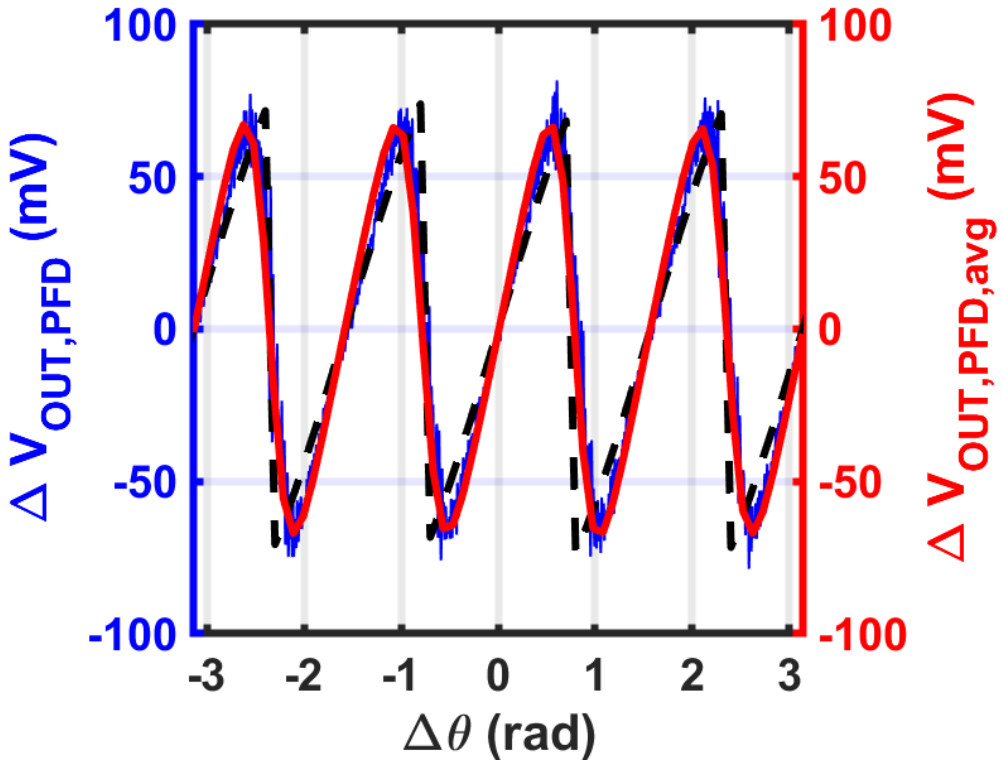


Figure 4.6: Simulated saw-tooth PFD characteristic of the QPSK Costas loop. The blue curve indicates the characteristic produced by a 100 MHz beat tone stimulus in both I- and Q channels for 100 $\mu A_p p$ input current with the PFD VGA set to maximum gain. The red curve indicates the charcteristic produced by the rotation of the I/Q constellation. The ideal characteristic of Eqn. 4.4 is also plotted (dashed black).

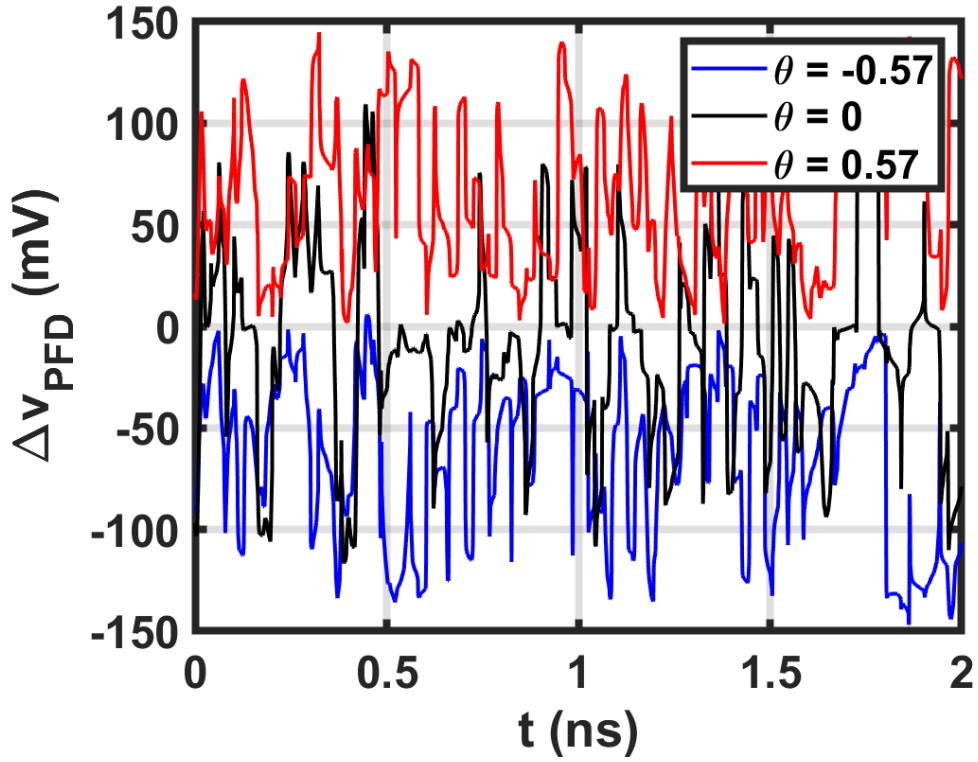


Figure 4.7: Simulated transient waveform of the PFD output given that the I/Q channels are driven by uncorrelated PRBS7 waveforms at 50 Gbaud for three cases of constellation rotation: θ= -0.57, θ= 0, and θ= 0.57.

Ge photodiodes (PDs). The CoRX PIC schematic and microphotograph is shown in Fig. 4.8.

The OH detailed in Fig. 4.8 uses two directional couplers at the input to mix the LO and RX optically through four waveguides - two of which are directly passed through thermal phase, and two of which are intersecting with no phase shifters - and two additional directional couplers at the output in order to produce differential in-phase and quadrature components. The field mixing components through the optical hybrids are annotated on the schematic in Fig. 4.8. The PSR nominally splits the X and Y polarizations of a dual-polarization RX signal with less than 1 dB insertion loss and 27 dB extinction ratio [87]. It should be noted that the PIC is evaluated in a single-polarization configuration in which the PSR only presents a low insertion loss. The edge couplers are based on a metamaterial waveguide taper and V-groove trench that allows for a cleaved SMF-28 fiber to be coupled with transmission efficiencies up to -1.3 dB with a 0.8 dB penalty over 100 nm bandiwdth centered around the O-band (i.e. 1310 nm) [88]. The PD bandwidth has been reported to achieve up to 40 GHz bandwidth and $\approx$ 1 A/W responsivity [89].

4.4 Costas Loop Optical Phase Locked Loop

In evaluating the PFD characteristic, the residual phase error of the OPLL deteriorates the received constellation and sets a BER floor. To predict the residual phase error, the loop frequency response must be determined in addition to the phase noise spectral densities. Assuming the loop filter topology demonstrated in [83], [84], the open-loop transfer function is

$$G(s) \approx \frac{K}{1+s\tau_{las}}\left(\frac{(1+s\tau_2)}{s\tau_1(1+s\tau_{op})}\frac{e^{-s\tau_{d,op}}}{R_1+R_{ph}}+\frac{sC_{FF}}{2}\right)e^{-s\tau_l} \tag{4.7}$$

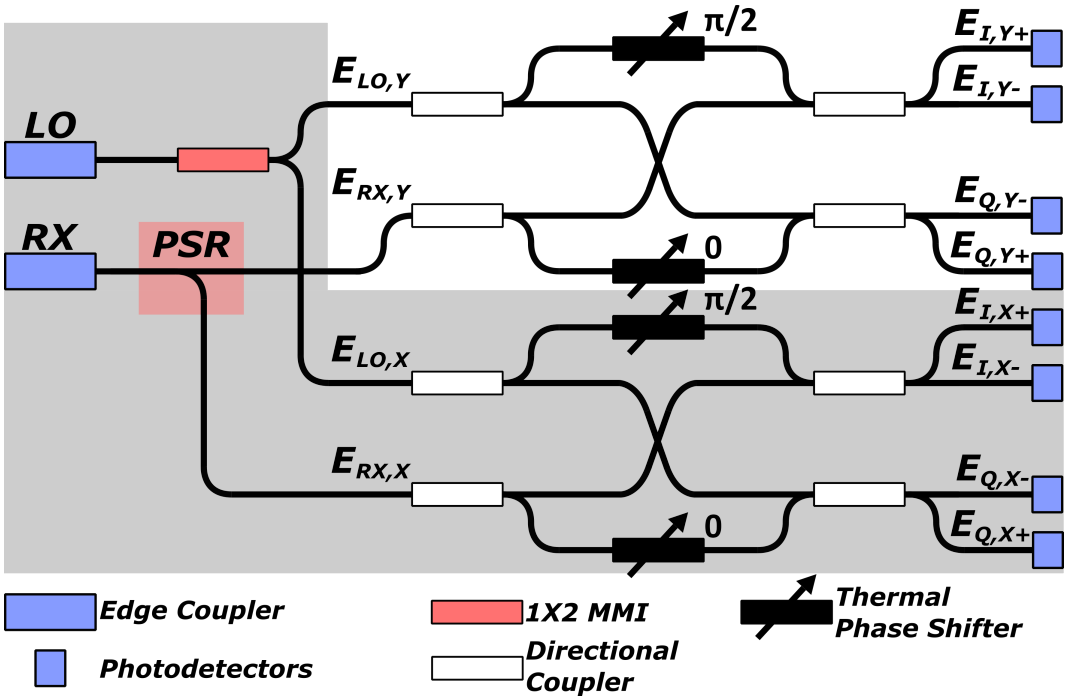


Figure 4.8: Schematic of the PIC with the shaded region indicated the polarization used in this work.

where $K = K_{PD}K_{CCO}$. The loop parameters of the numerical OPLL analysis are listed in Table 4.1. The frequency response is plotted in Fig. 4.10. The residual phase noise spectral density is then determined and plotted in Fig. 4.9.

The phase error variance due to the phase noise can be written as [90], [91]

$$\sigma_{PN}^2 = \int_0^\infty \frac{S_{FN}(f)}{f^2} \left| \frac{1}{1+G(f)} \right|^2 df \tag{4.8}$$

where $S_{FN}(f) = \frac{1}{2\pi} S_{FN,ST} \left(1 + \alpha^2 |H(f)^2|\right) + \frac{C}{f}$ is the frequency noise of a semiconductor laser.

The calculated loop bandwidth is 382 MHz, the phase margin is 89°, the gain margin is 10.5 dB, and the residual phase error is 4.7°. Recent work has indicated that residual rms phase error of 5^circ for a QPSK CoRX achieves BER better than 10^-6 for an SNR of around 15 dB. [92].

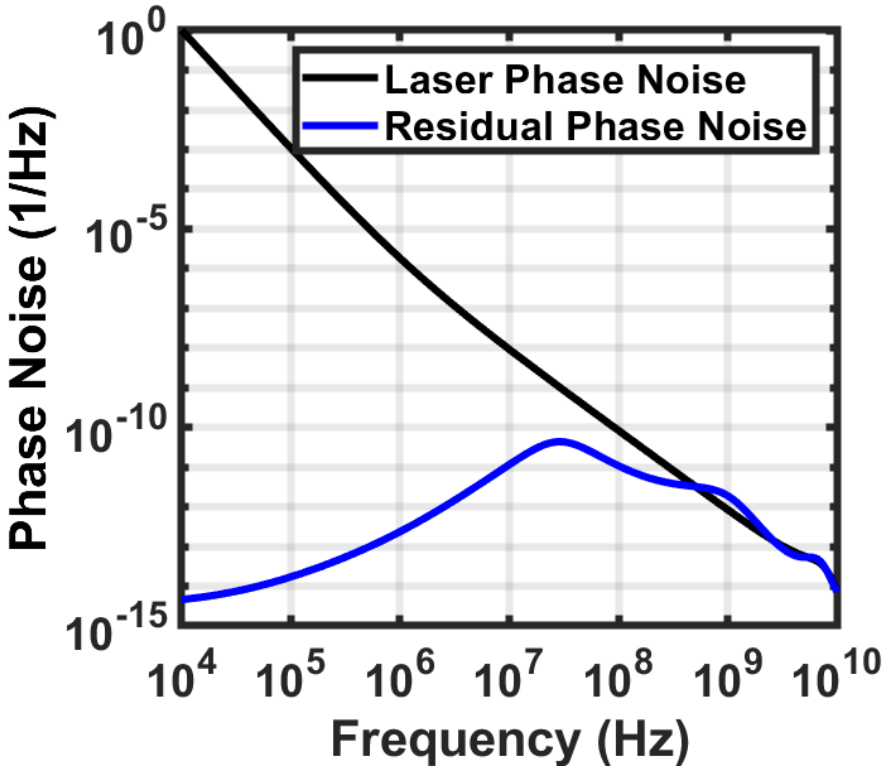


Figure 4.9: Phase noise spectral density of SG-DBR laser and residual phase error spectral density predicted by OPLL model based on parameters listed in Table 4.1.

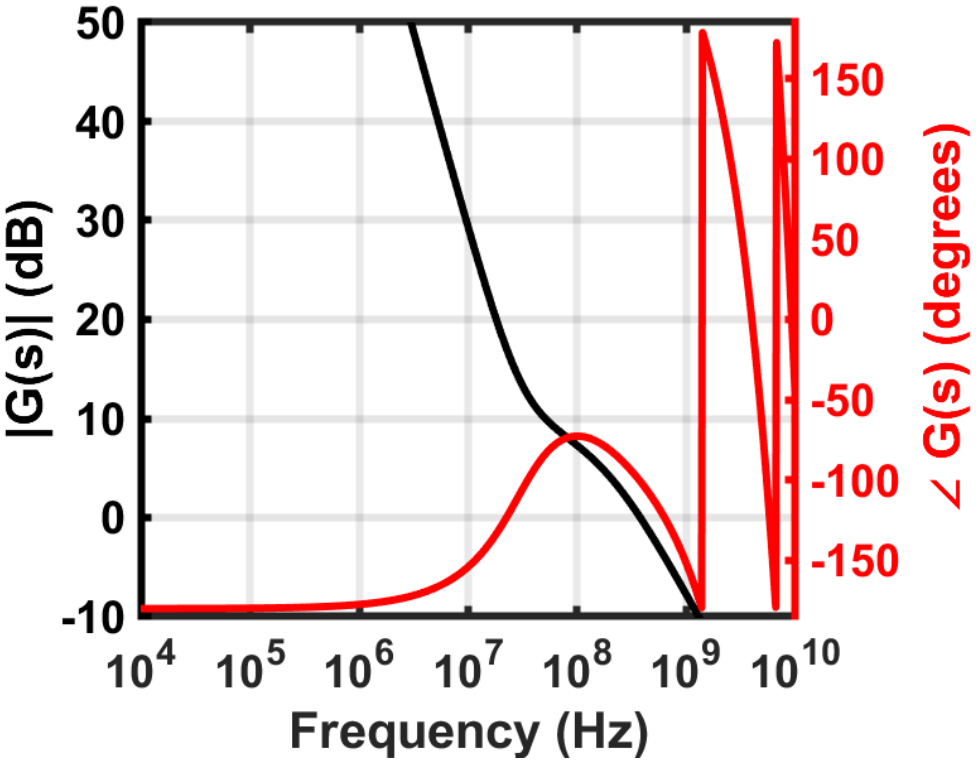


Figure 4.10: Open-loop frequency Response of OPLL model based on parameters listed in Table 4.1.

Table 4.1: Estimated OPLL Model Parameters

Parameter	**Value**	**Detail**
K_{PD} (mV/rad)	117	Phase detector responsivity
K_{CCO} (GHz/mA)	0.75	Laser tuning responsivity [93]
$R_1 + R_{ph}$ (Ω)	200	LF in/output series resistances
τ_{las} (ns)	1.59	100 MHz phase shifter BW
C_{FF} (pF)	15	Feedforward capacitor
τ_1, τ_2, τ_{op} (ns)	25, 10, 79.6	LF time constants
τ_l, $\tau_{d,op}$ (ps)	188, 200	Loop delay, op-amp delay-
$S_{FN,ST}$ (kHz^2/Hz)	0.2	Schalow-Townes freq. noise spectrum [91]
α (unitless)	5	Linewidth enhancement factor [91]
ω_R (Grad/s)	16π	Natural freq. of relaxation oscillation [91]
γ (Grad/s)	$0.7\omega_R$	Damping factor of laser [91]
C (MHz^2)	250	1/f noise constant [91]

4.5 Measurements

The QPSK CoRX was fabricated in a 130-nm SiGe BiCMOS process and assembled on two custom FR-4 PCB assemblies (one for electrical test, and one for optical tests) capable of supporting NRZ data rates above 100 Gbps [77]. The voltage supplies are decoupled using off-chip 1.2 nF surface-mount capacitors to ensure a broadband AC ground.

4.5.1 Electrical Measurements

The high-speed differential input and output pads of the I and Q channels are wire-bonded onto the 50-Ω PCB traces tapped out by surface mount 65-GHz mini-SMP connectors. The assembly and cabling parasitics were captured in the eye diagram and BER measurements.

Eye diagrams and the BER were measured with an SHF 12104A bit pattern generator (BPG) and an SHF 11104A error analyzer (EA) synchronized with an SHF 78212A synthesized clock generator (CG) in a full-clock rate mode to provide two differential independent data streams (PRBS31) to the I- and Q-channel inputs of the EIC at a data rate equal to the CG frequency. The amplitude of the BPG output is attenuated by 20 dB and connected to the input channels of the RX PCB through DC blocking capacitors with 30 kHz cutoff frequency and 8-inch 67 GHz cables.

The I/Q channels were measured such that the crosstalk is generated from equal input amplitude levels on both channel. To measure eye diagrams, the input amplitude of the CoRX IC is attenuated to 19.2 mV and the I/Q-channel single-ended outputs are connected to a Tektronix DSA8300 digital serial analyzer (DSA) at 70 GHz bandwidth through a 80E11 sampling module with a 2-meter 80X02 extender. DC blocking capacitors with a cutoff frequency of 30 kHz and 4-inch 67 GHz cables were used between the sampling oscilloscope and the RX assembly. Fig. 4.11 plots the I/Q eye diagrams at data rates of 40, 50, and 64 Gbps. The eye openings in all cases are similar on both channels in the presence of crosstalk.

To measure the BER, the differential outputs were connected to the EA through DC blocking capacitors and 6-inch 67 GHz cables. The BER sensitivity curves are measured for the data rates of 56 and 60 Gbps and are demonstrated in Fig. 4.12 and indicate BER well below the KP4-FEC limit for input voltage amplitudes below 10 mV. With the simulated input impedance of the TIA, 160 Ω, in parallel with the 50 Ω BPG, we can determine the corresponding OMA for a 10 mV amplitude is roughly 526 μW or -2.75 dBm, assuming a photodetector responsivity of 1 A/W. During the BER sensitivity measurements, a sufficient number of bits to offer a confidence level above 95% for a minimum of 5 errors at the target error rate of 10^{-12} was acquired. The BER bathtub curves are measured at data rates of 56 and 60 Gbps in a dual-channel operation with two

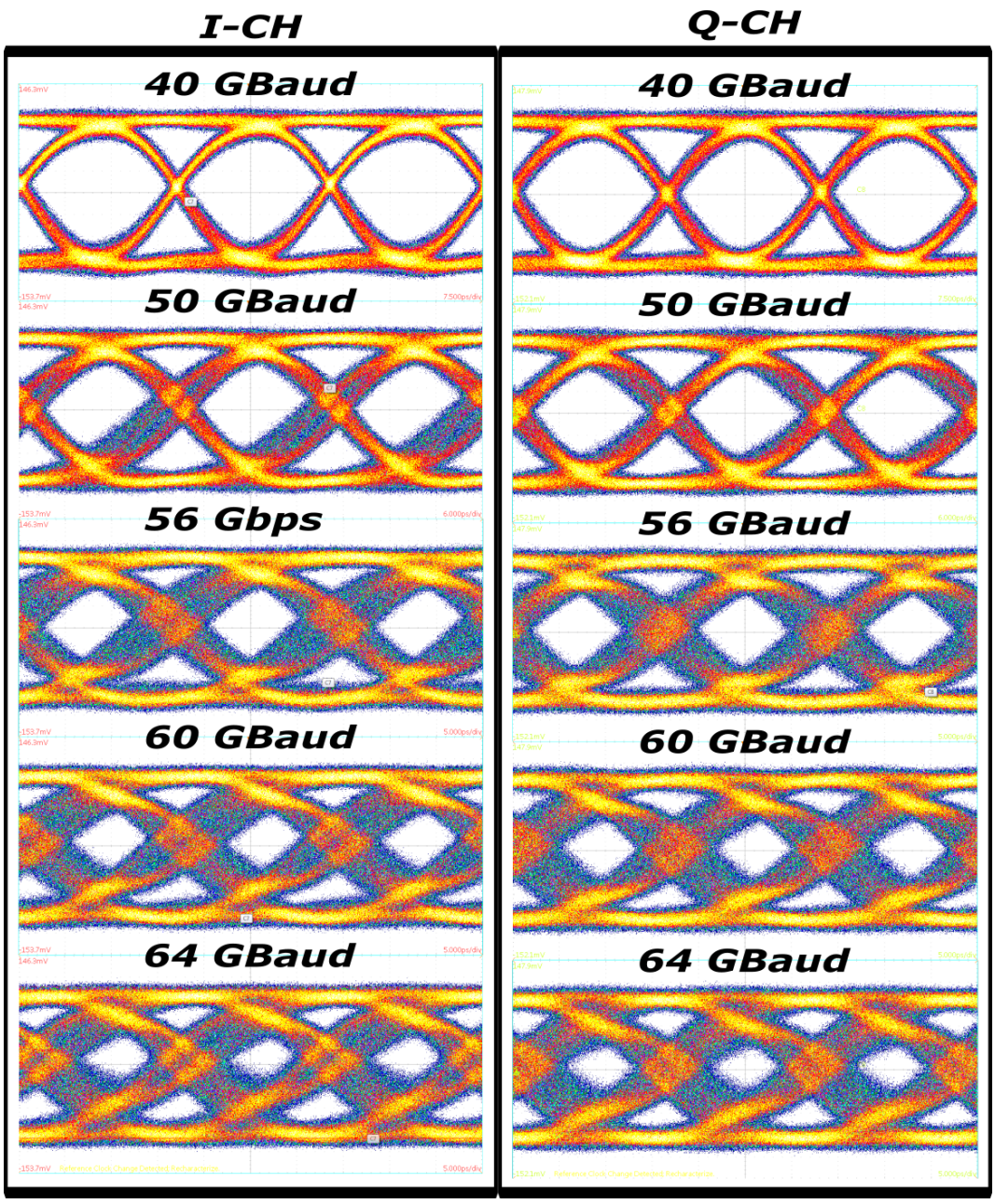


Figure 4.11: Eye diagrams for I- and Q-channel single-ended outputs in a dual-channel operation with Costas PFD. The single-ended output voltage swing of the RX IC is 225 mV and 500 waveforms of a PRBS31 test pattern were acquired.

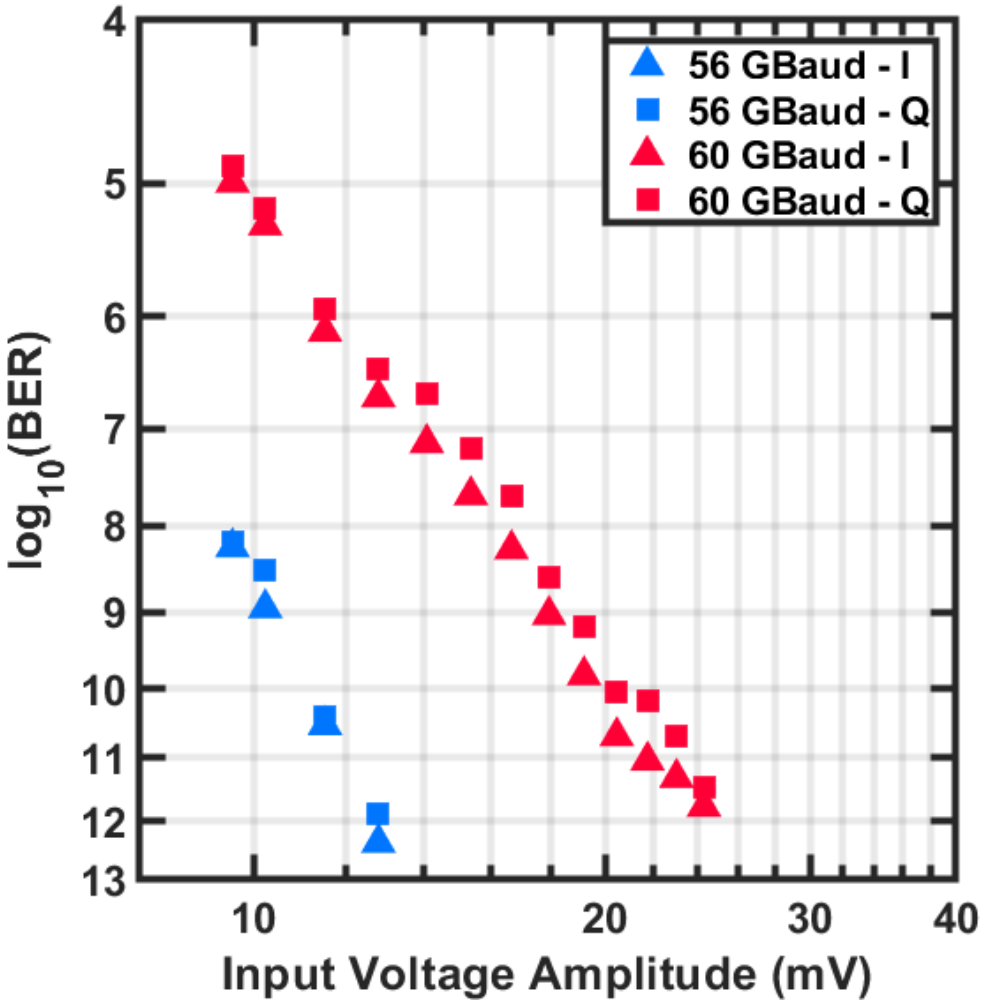


Figure 4.12: BER sensitivity curves for the the I- and Q- channels for data rates of 56 Gbps and 60 Gbps in a dual channel configuration using a PRBS7. The test patterns were PRBS7 with I- and Q- bit streams decorrelated by bit delay.

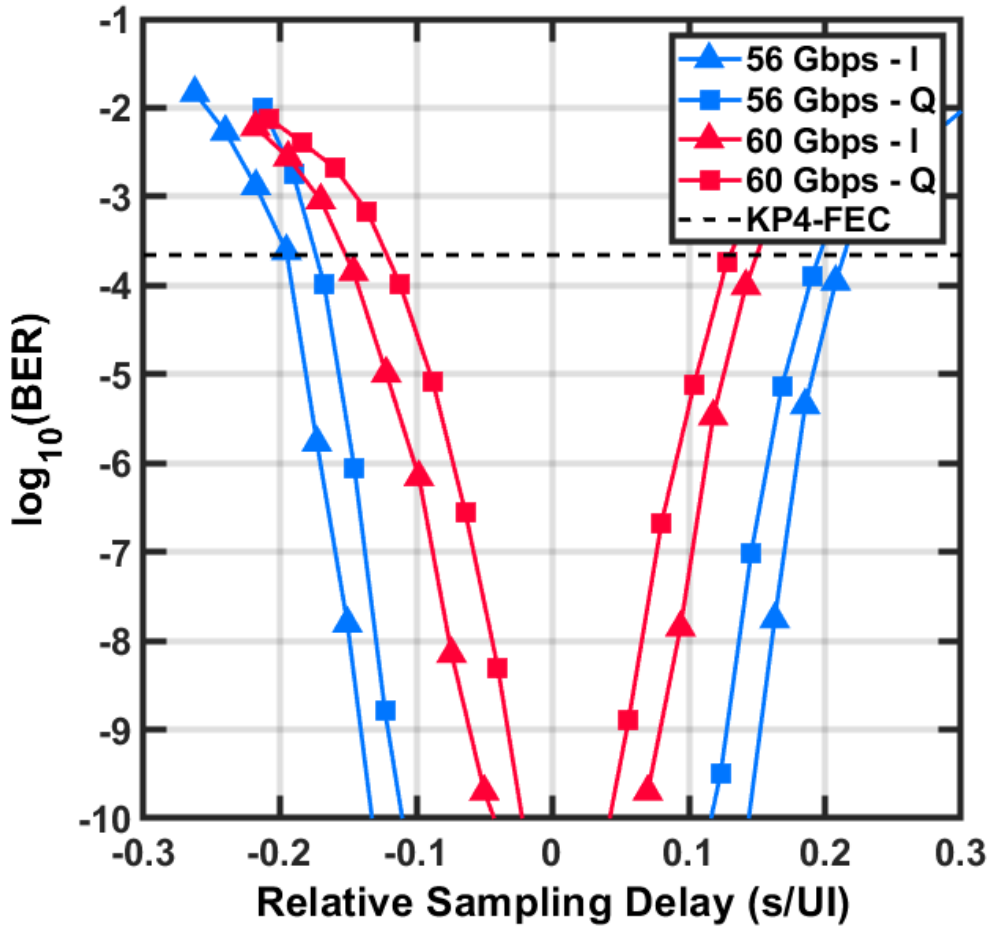


Figure 4.13: BER bathtub measurements for the I- and Q- channels for data rates of 56 Gbps and 60 Gbps in a dual channel configuration. The test patterns were PRBS7 with I- and Q- bit streams decorrelated by bit delay.

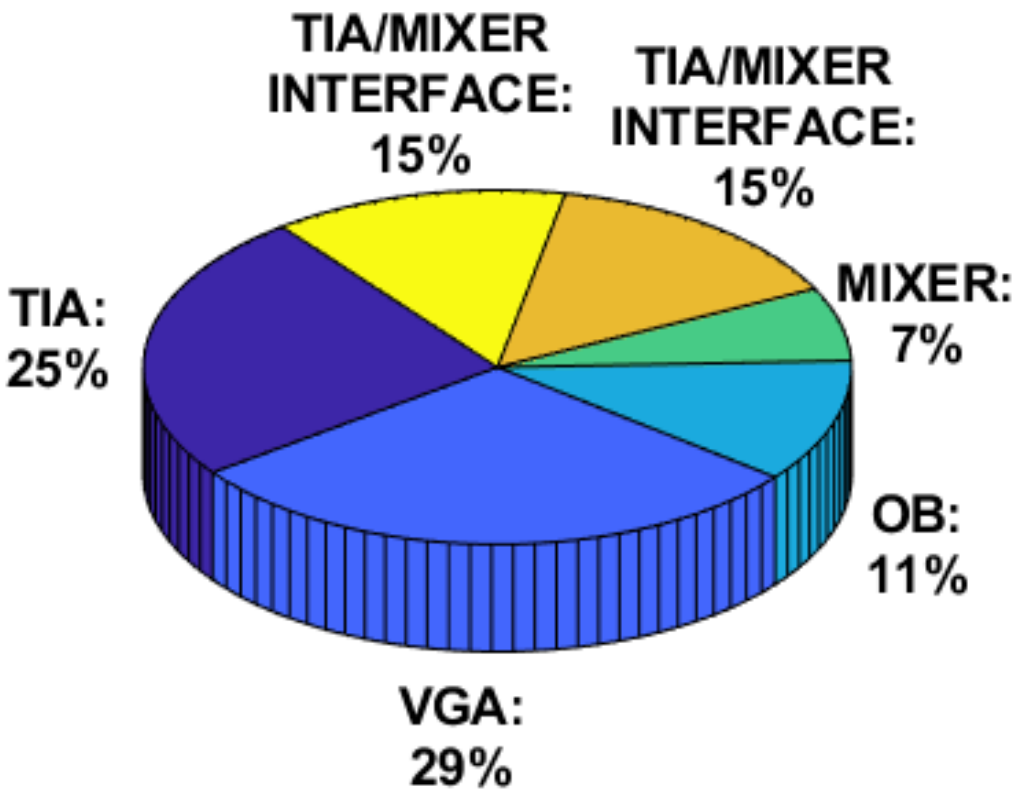


Figure 4.14: Distribution of DC power consumption of the CoRX EIC.

uncorrelated PRBS7 patterns and demonstrated in Fig. 7.8. During the BER bathtub measurements, a sufficient number of bits to offer a confidence level above 95% for a minimum of 10 errors at the target error rate of 10^{-10} was acquired. The BER bathtub curves indicate considerable sampling phase margin greater than 0.2 UI at the KP4-FEC limit up to 60 Gbps as the assembly and setup parasitics begin to degrade the high-frequency performance.

4.5.2 Noise Measurements

The noise of the RX EIC was characterized on the PCB assembly with the mini-SMP connectors at the inputs left open. The histogram function of the DSA acquired

the output noise statistics of the I- and Q-channel single-ended outputs with the complementary outputs terminated to 50 Ω. With the DSA bandwidth set to 70 GHz, the rms output noise voltages were measured across various transimpedance gain settings. Fig. 4.15 plots the rms input referred noise current ($i_{n,rms}$) which is determined from $i_{n,rms} = \frac{1}{R_T}\sqrt{2\int_0^{2BW} v_{n,out}^2(f)df}$. The simulated frequency response for $Z_{T,midband}$ and the 3-dB bandwidth from Fig. 4.5 were used to determine $i_{n,rms}$. At maximum $Z_{T,midband}$, $i_{n,rms}$ is roughly 2 μA_{RMS} for both channels. At minimum $Z_{T,midband}$, $i_{n,rms}$ is 7 μA_{RMS} across both channels.

Assuming a $\mathcal{R}$ of 1 A/W and a BER requirement of 10^-12 ($Q \approx 7$), the range in sensitivity for the I and Q channels is roughly between −13.09 dBm and −18.54 dBm. This bound on the sensitivity of the optical assembly does not include the photodetector capacitance and wirebond inductance impact on the noise and bandwidth of the receiver.

4.5.3 Optical Measurements

The optical measurement setup is detailed in Fig. 4.16 based on the assembly shown in Fig. 4.17 with insets of the microphotograph of the EIC and PIC. The EIC occupies an area of 1.475 mm by 1.9 mm. The CoRX assembly was evaluated using an EXFO T100S-HP-O external cavity laser (ECL) tuned to 1310 nm with an output power set to 13 dBm. The ECL output was split into the TX and LO paths using a 50/50 optical power splitter. The TX assembly consisted of a 25 GHz IQ Mach Zehnder Modulator (MZM) biased at QPSK operation driven by PRBS7 waveforms from the BPG through SHF amplifiers. A total of four channels were used from the BPG and combined using 50 GHz resistive power combiners in order to produce a two-tap feed-forward equalization (FFE) waveform in both I and Q channels to compensate the 25 GHz bandwidth of the MZM. Because of the MZM loss, a praseodymium-doped fiber amplifier (PDFA) was

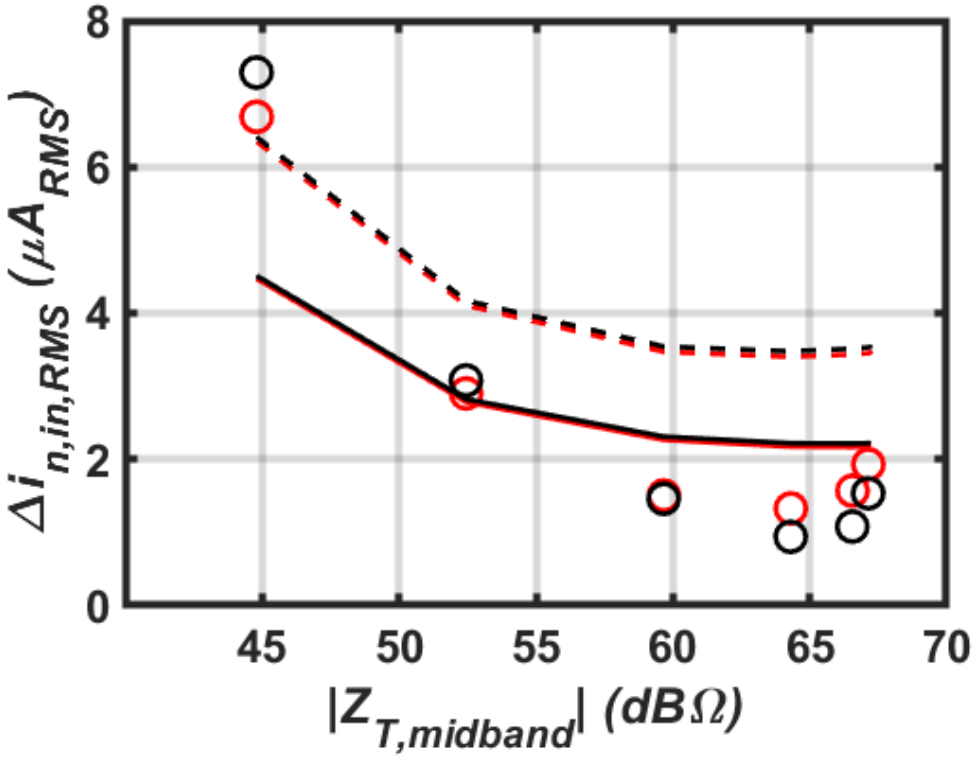


Figure 4.15: Measured RMS input-referred current noise vs. transimpedance gain.

used to amplify the optical QPSK waveform. The LO path was also amplified using a semiconductor optical amplifier (SOA). Both the amplified TX and LO paths were passed to polarization controllers (PC) and edge coupled into the CoRX PIC. The EIC included 2 kΩ resistors at the input of the TIA in order to sink the DC currents of the PIC photodetector outputs. The EIC outputs were then connected to a two-channel Keysight real-time oscilloscope (RTO) in a single-ended configuration with the complementary outputs terminated to 50 Ω. Raw samples of the EIC outputs produced the constellations in Fig. 4.18 and the BER curves in Fig. 4.18. The BER curves indicate that at 50 Gbaud the OMA to achieve 10^{-6} BER is -6 dBm. Compared to our calculation of the equivalent OMA for the electrical BER testing of -2.75 dBm.

The CoRX circuit draws 178 mA from a 3-V supply for a total power consumption of

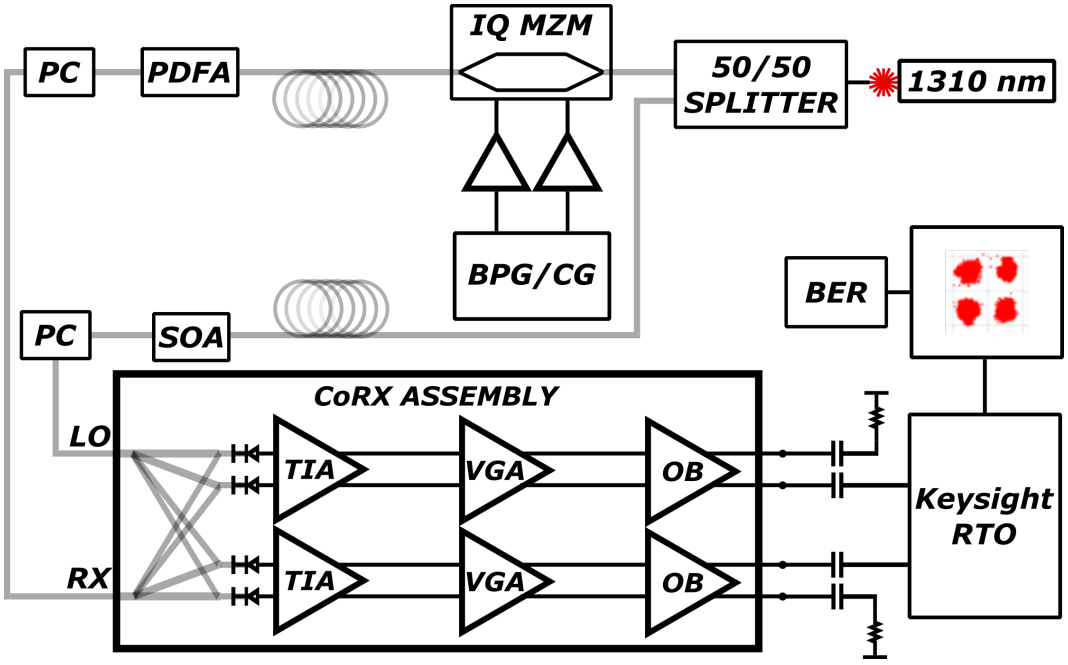


Figure 4.16: Block diagram of OE measurement setup.

534 mW and energy efficiency of 5.34 pJ/bit with a breakdown given in Fig. 4.14. Each RX channel consumes approximately 166 mW or 332 mW for the dual-channel energy efficiency of about 3.32 pJ/bit. The power consumption for the Costas loop PFD including the interfacing circuits from the TIA and VGA outputs is 186 mW corresponding to an energy efficiency of 1.86 pJ/bit.

Comparison with prior work in Table 1 illustrates that this work offers the lowest energy efficiency (excluding the Costas loop circuits) and average input-referred noise current density for optical CoRX ICs capable of data rates above 100 Gbps/polarization.

4.6 Conclusion

Energy-efficient analog CoRXs are described for QPSK and demonstrated in a SiGe process for 100 Gb/s operation. The RX block consumes a total of 332 mW for the

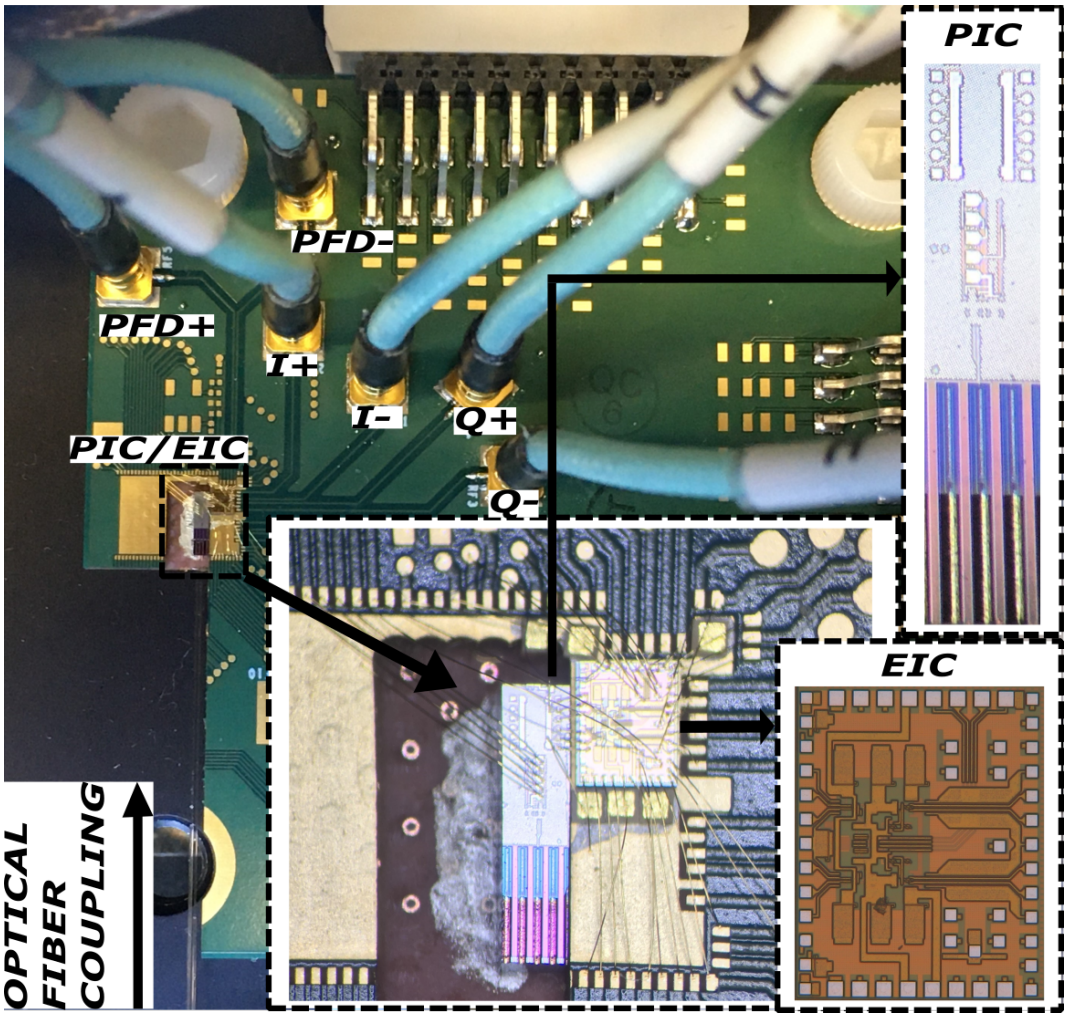
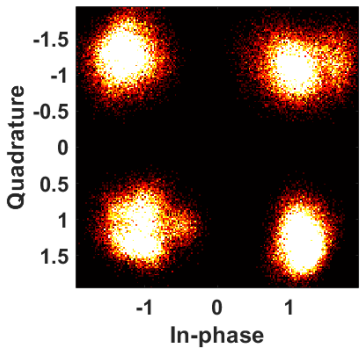
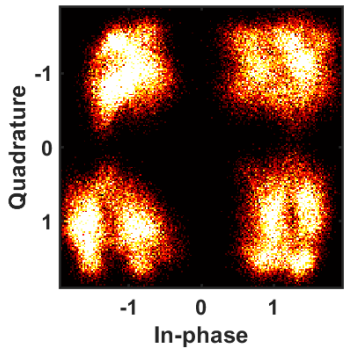


Figure 4.17: Photographs of the EO CoRX assembly with the PIC and EIC mounted adjacent. Light is coupled into the PIC through edge couplers.



(a)



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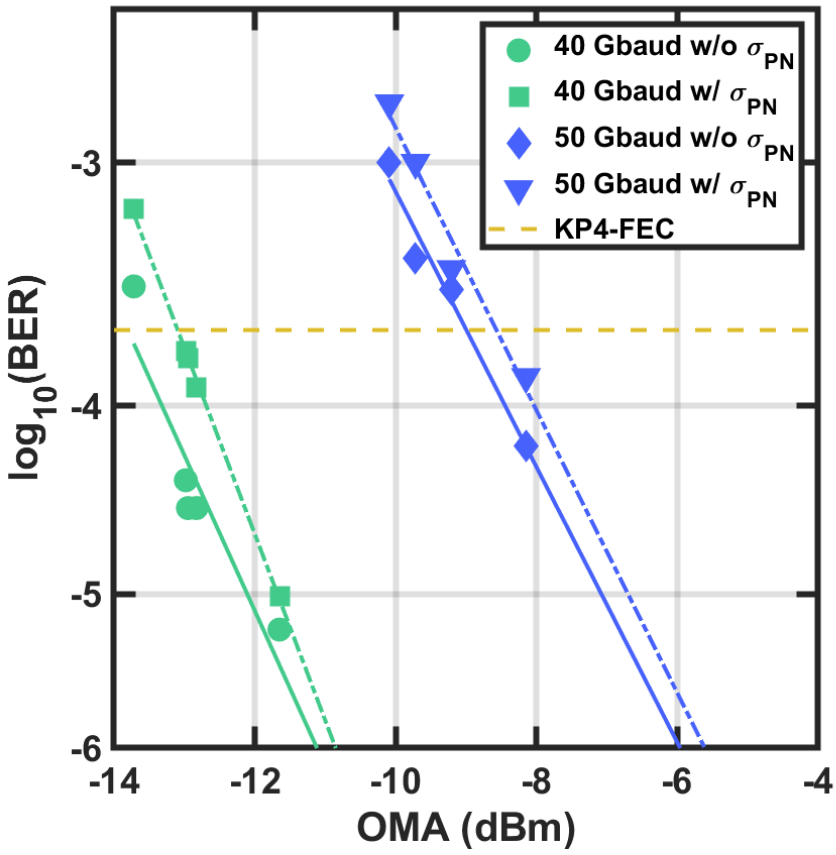


(c)

Figure 4.18: Measured constellations for QPSK modulation at (a) 40 GBaud and (b) 50 Gbaud operation for PRBS7 patterns. Measured BER (c) of OE assembly for data rates of 40 GBaud and 50 GBaud with (dashed-line) and without (solid-line) the residual phase error of 4.7 ° as determined by Eqn. (4.8). The KP4-FEC limit are also shown. Note: the measured RX power per photodetector is -15.23 dBm (-9 dBm into the optical hybrid).

Table 4.2: State-of-the-Art Comparison of SiGe HBT-based Coherent Receivers

Reference	[37]	[39]	[40]	**This Work**
Technology Node	130 nm SiGe	130 nm SiGe	130 nm SiGe	**130 nm SiGe**
Modulation	16QAM	QPSK	QPSK	**QPSK**
Bit rate (Gbps/Pol.)	136	64	128	**100**
BW_{3dB} (GHz)	27	53	33	**35.2**
P_{DC} (mW/TIA)	313[1]	218[1]	277[1]	**166**[1]**/267**[2]
Efficiency (pJ/bit)	4.6[1]	6.81[1]	4.33[1]	**3.32**[1]**/5.34**[2]
TI Gain (dBΩ)	73	74[3]	80[3]	**67.2**
Avg. IRNCD (pA/sqrt(Hz))	20	12.2[3]	24.86[3]	**10.7**[4]
FOM_{BW} (dBΩ-GHz/mW)	385/770[3]	758[3]	1913[3]	**486**[1]**/972**[1,3]
Optical/Electrical	Optical	Electrical	Optical	**Optical**

[1] only RX circuits, [2] RX and Costas loop circuits, [3] differential transimpedance gain: $Z_{T,diff} = 2Z_T = 2\Delta V_{out}/\Delta I_{in}$, [4] Calculated using simulated gain/BW and measured output noise histogram statistics at the maximum gain setting

I/Q data channels and 186 mW for the PFD. This work substantiates the potential for picojoule-per-bit analog coherent transmission schemes in future intra-datacenter interconnects.

Chapter 5

A Variable Transimpedance Amplifier Design based on a Shunt-feedback A_v-R_F Matching Condition

This chapter is a reprint of material in the manuscript, "An Energy-Efficient, 60-Gbps Variable Transimpedance Optical Receiver in a 90-nm SiGe HBT Technology," to be presented at the 2022 IEEE International Microwave Symposium

5.1 Introduction

This paper presents a differential optical receiver integrated circuit (RXIC) with a variable-transimpedance amplifier (VTIA), a two-stage variable-gain amplifier, and 50-Ω output buffer based on a 90-nm SiGe BiCMOS technology. The VTIA incorporates tunable load and feedback resistors to adjust the gain and frequency response and intro-

duces higher dynamic range in the RXIC. Electrical measurements of the RXIC on an FR-4 PCB assembly demonstrate open-eye NRZ data rates up to 60 Gbps, error-free (i.e. 10^{-11}) at 50 Gbps. The total power consumption of the RXIC is 137 mW for an energy efficiency of 2.28 pJ/bit. The transimpedance-bitrate relative to power consumption is among the highest reported relative to the state-of-the-art.

Capacity demands for intra-datacenter interconnects under 2 km reach are pushing aggregate per-λ data rates of optical links above 200 Gbps. Intensity modulation direct detection (IM-DD), e.g. PAM, and coherent, e.g. QAM, waveforms have been explored as solutions to address data rate scaling with commensurate energy efficiency improvements to keep overall data center energy requirements relatively constant [4]. Variable-transimpedance amplifiers (VTIAs) accommodate requirements for IM-DD NRZ and coherent QPSK links where optical power can vary, as well as multi-level IM-DD 4-PAM and coherent 16-QAM [37], [48]. The RXIC is a key building block for energy-efficient optical links, requiring high bandwidth, low noise, low power consumption, and high dynamic range with tuning to optimize the signal to noise ratio (SNR) of the data eye. NRZ data rates over 90 Gbps have been reported with energy efficiencies below 3 pJ/bit and average input-referred noise current densities (IRNCD) below 20 pA/$\sqrt{}$Hz in [48], [27], [36], [14].

Previous work has demonstrated a VTIA using an NMOS resistor bank in the feedback path with a fixed load resistor [37]. However, the feedback resistor only changes the input impedance and transimpedance. This paper introduces tunable feedback and load elements into a shunt-feedback common-emitter/cascode amplifier constrained by an A_v-R_F condition illustrated by Fig. 5.1 to provide gain peaking. This tuning allows gain control in the TIA to maximize the input dynamic range and eye opening SNR. In order to tune A_v, the circuit is tuned by the following parameters: (1) the load resistor, R_L, (2) the bias current, and (3) feedback resistance (with a fixed bias). Variation of these

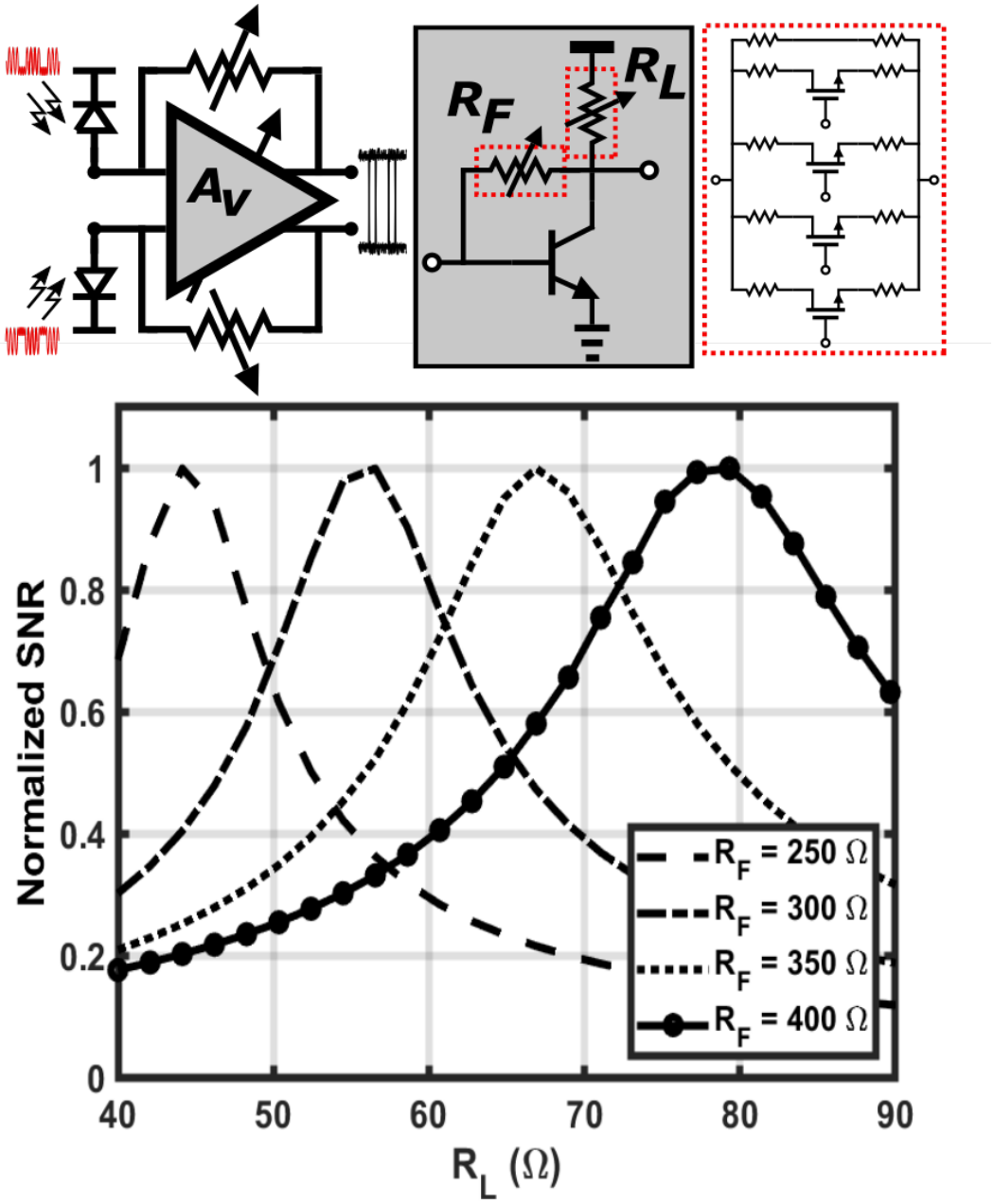


Figure 5.1: Simplified schematic of a VTIA of the optical RXIC based on a shunt-feedback TIA with a switchable R_F and R_L network (top) and the simulated dependence of the normalized eye SNR at 50 Gbps across various R_F and R_L combinations for the VTIA of this work.

parameters corresponds to tuning the gain of the VTIA A_v core. The SNR of the eye is defined by

$$SNR_{eye} = \frac{V_1 - V_0}{\sigma_0 + \sigma_1} \tag{5.1}$$

where V_1 and V_0 are the voltage levels of the 1 and 0, respectively, and σ_1 and σ_0 are the standard deviations of the normal distribution of the 1 and 0 levels, respectively. The advantage of using the SNR of the eye diagram as the figure of merit for optimizing the A_v-R_F relation per input modulation current is that both ISI-induced eye closure and overpeaked eye diagrams are penalized. The normalization of the SNR for the individual R_F conditions allows us to simply identify the optimal SNR point as unity.

Section II presents the design of the differential VTIA circuit. Section III presents the measured electrical characteristics. To our knowledge, this is the first optical RXIC with a variable-TIA design using switchable feedback and load resistance banks integrated capable of error-free operation to 50 Gbps and operation to 60 Gbps at an energy efficiency of 2.28 pJ/bit.

5.2 Receiver Circuit Design

The RXIC comprises of three stages: (1) the VTIA, (2) two intermediate variable gain amplifiers (VGA), and (3) the 50-Ω output buffer. Fig. 5.2 illustrates the schematic of the core RXIC design with associated transistor sizing and biasing.

The VTIA stage comprises a cascode common-emitter amplifier followed by an emitter follower stage. The feedback and load resistors, R_F and R_L, are switchable resistor banks which allow for discretely tunable transimpedance gain and simultaneous

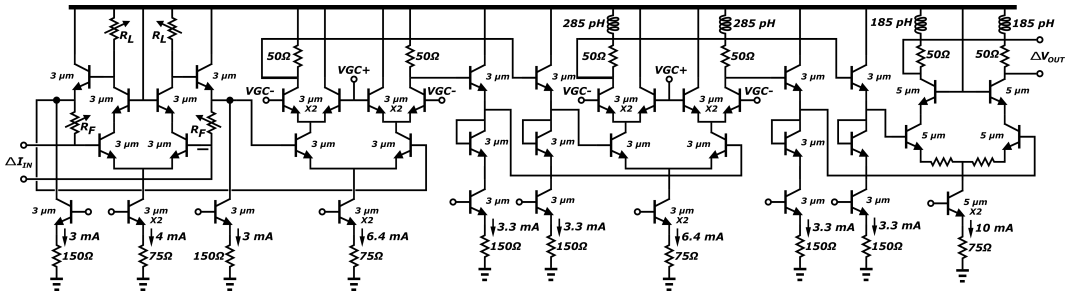


Figure 5.2: Schematic of the RXIC including the VTIA, VGA, and output buffer. Note: R_F ranges between 250 and 400 Ω and R_L ranges between 45 and 85Ω

A_v-R_F-matching for eye optimization across the tuning range. Fig. 5.1 demonstrates the schematic of the front-end TIA circuit with the switchable resistor banks of R_F and R_L. Because the switchable resistor banks contribute to additional parasitic capacitance along the feedback and load resistors, the cascode amplifier and emitter follower concurrently allow for isolation of the resistors and the corresponding parasitic capacitance, reduce the Miller effect, and isolate the load capacitance of the intermediate amplifier input. The switchable R_F and R_L banks allow for four discrete transimpedance gain states in the VTIA 47, 49, 52, and 52.8 dBΩ. The simulated 3-dB bandwidths across these gain configurations range between 16.4 GHz to 25.1 GHz. In order to support data rates above 50 Gbps, bandwidth extension techniques are used along the RXIC chain.

The VTIA is followed by the cascaded variable gain amplifiers (VGA) based on Gilbert cell circuits. The VGA contributes an additional 18 dB of tunable gain. The second Gilbert cell includes shunt-inductive peaking for bandwidth extension. The output buffer provides less than 1 dB gain and up to 500 mV_{p-p} to a 50 Ω interface and additional broadband performance through shunt-inductive peaking.

Fig. 5.3 demonstrates the simulated frequency response of the RXIC with the four switchable A_v-R_F settings in the VTIA. The maximum RXIC transimpedance gain is 71.5 dBΩ at 3-dB bandwidth of 37.5 GHz. The RXIC transimpedance gain can be backed off (i.e. tuning the VGA to 0 dB) to 47 dBΩ at a 3-dB bandwidth of 48.8 GHz.

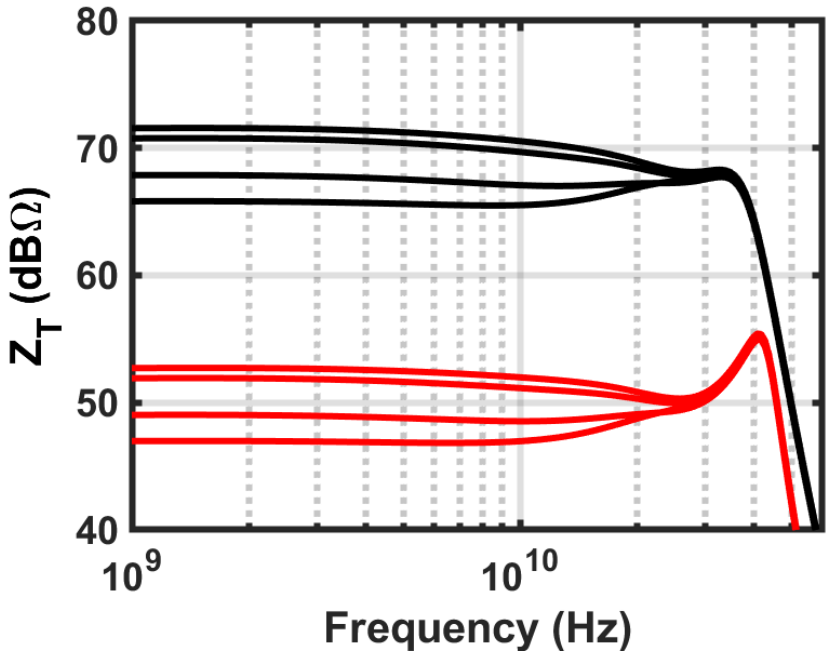


Figure 5.3: Simulated frequency response of the RXIC with various front-end gain settings. The black curves indicate 18 dB gain contribution from the VGA, and the red curves indicate 0 dB contribution from the VGA. Note: 500 pH and 750 pH wirebond inductances were used at the input and output of the RXIC to correspond with the measured assembly.

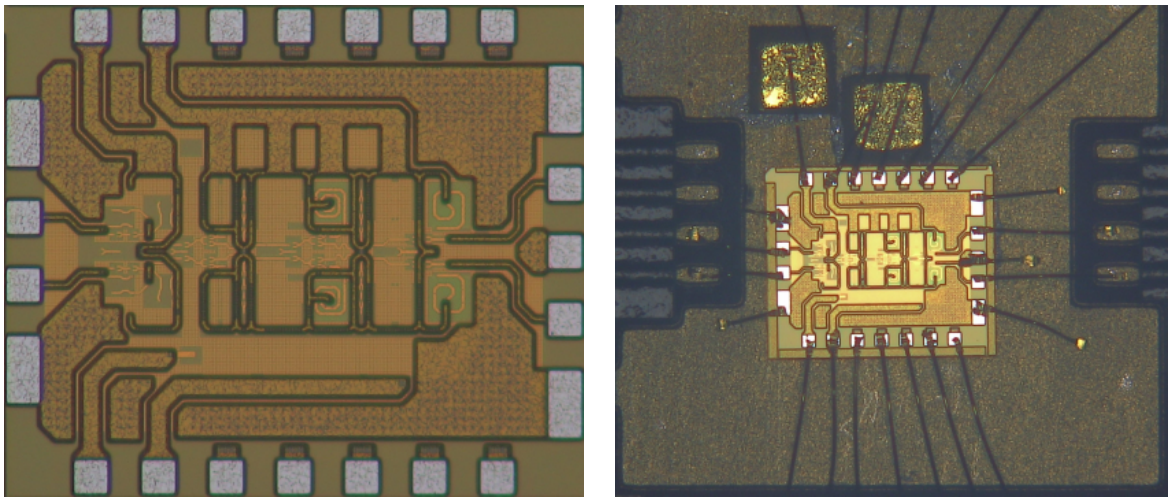


Figure 5.4: Microphotograph of the fabricated chip (left) and PCB assembly for testing at 60 Gbps (right)

5.3 Measurements

The RXIC was fabricated in a 90-nm SiGe HBT process with an area of 1.43 mm^2 (1.3 mm by 1.1 mm). Fig. 5.4 illustrates the chip microphotograph. The RXIC draws under 46 mA from a 3-V supply for a power consumption of 137 mW. The fabricated IC was characterized in the time-domain (i.e. eye diagrams and bit error rate (BER)) using a custom FR-4 PCB assembly with over 5-dB packaging loss at 40 GHz. The PCB assembly parasitics, including long wirebonds at the input and output were embedded in the time-domain measurements.

NRZ data rates up to 60 Gbps were produced using a high-speed bit pattern generator (BPG) (SHF 12105A) was synchronized with a clock generator (CG) (SHF 78212A) in a full-clock configuration. The BPG output was passed through 20 dB attenuators to drive the RXIC input well below the 75 mV BPG amplitude limit. The differential output of the RXIC was connected to a Tektronix digital serial analyzer sampling oscilloscope (DSA8300) through a sampling module (Tektronix 80E11) with a 2 meter extender (Tektronix 80X02) for eye diagram measurements, and to an error analyzer (EA) (SHF

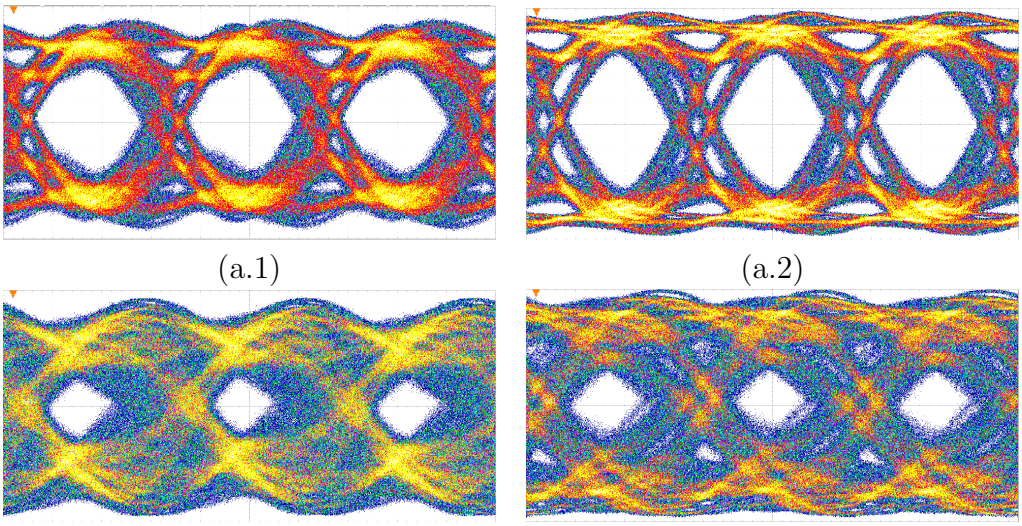


Figure 5.5: Measured differential NRZ eye diagrams at (a.1-2) 40 Gbps and (b.1-2) 60 Gbps with the RXIC transimpedance gain set to 65.5 dBΩ and 71.5 dBΩ, respectively. The output swing is 500 mV_{p-p} and the BPG input amplitude was set to 100 mV through 20 dB attenuators. 500 PRBS31 waveforms were acquired.

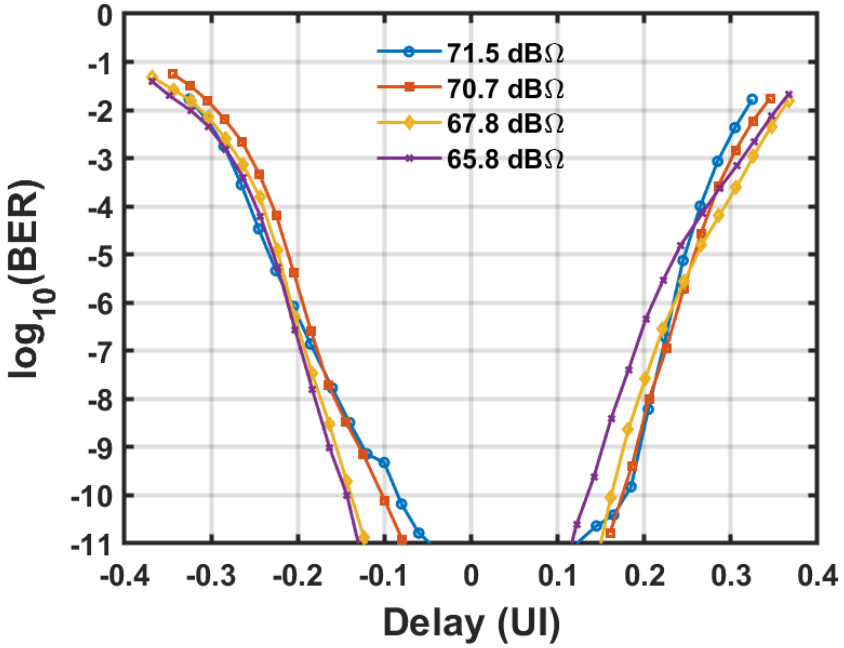


Figure 5.6: Measured BER bathtub curves at 50 Gbps for various transimpedance gain settings. Notably, at the sampling margin is consistent across the various front-end gain settings. A PRBS7 pattern was used.

Table 5.1: State-of-the-Art Comparison of Differential Optical RXICs.

Ref.	[36][1]	[27][1]	[48]	[14]	**This work**
Tech. Node	130 nm SiGe	130 nm SiGe	55 nm SiGe	130 nm SiGe	90 nm SiGe
f_T (GHz)	300	300	320	300	310
DR (Gbps)	112[1]	100[1]	90	112/84	60
P_{DC} (mW)	345	150	222	162/138	137
Eff. (pJ/bit)	3.08/3.45	1.5	2.47	1.5/1.64	2.28
$Z_T(0)$ (dBΩ)	71	65	65	66.3/70.5	71.5
Avg. IRNCD ($pA/\sqrt{Hz}$)	7.2	7.6	N/A	17.3/12.9	11.5[2]
FOM_{BR} (Gbps-Ω/mW)	1151	1185	1438	1377/ 2036	1646
Testbench	50 Ω	50 Ω	w/ PD	50 Ω	50 Ω

[1] no BER reported, [2] Calculated w/ simulated gain/BW, and measured noise

1104A) synchronized with the CG for BER measurements. Short 4-inch 67 GHz cables and 30 kHz DC-blocking capacitors were used between the differential input and output of the RXIC PCB assembly.

Fig. 7.5 demonstrates the measured differential NRZ output eye diagrams of the RXIC at 40 Gbps and 60 Gbps with the VTIA configured to 47 dBΩ and 52.8 dBΩ transimpedance gain. Fig. 7.8 demonstrates the measured BER bathtub curves at 50 Gbps across the four switchable VTIA states.

The output noise histograms of the RXIC were acquired with open inputs. Using the frequency response from Fig. 5.3, the input-referred RMS noise current is determined by the following equation; $i_{n,rms} = \frac{1}{R_T}\sqrt{2\int_0^{2BW} v_{n,out}^2(f)df}$. Fig. 5.7 demonstrates the measured differential output RMS noise voltage and average IRNCD. Most notably, the IRNCD does not change substantially across the transimpedance tuning range implying constant sensitivity with the gain control.

Table 7.1 demonstrates the state-of-the-art performance for SiGe HBT-based differ-

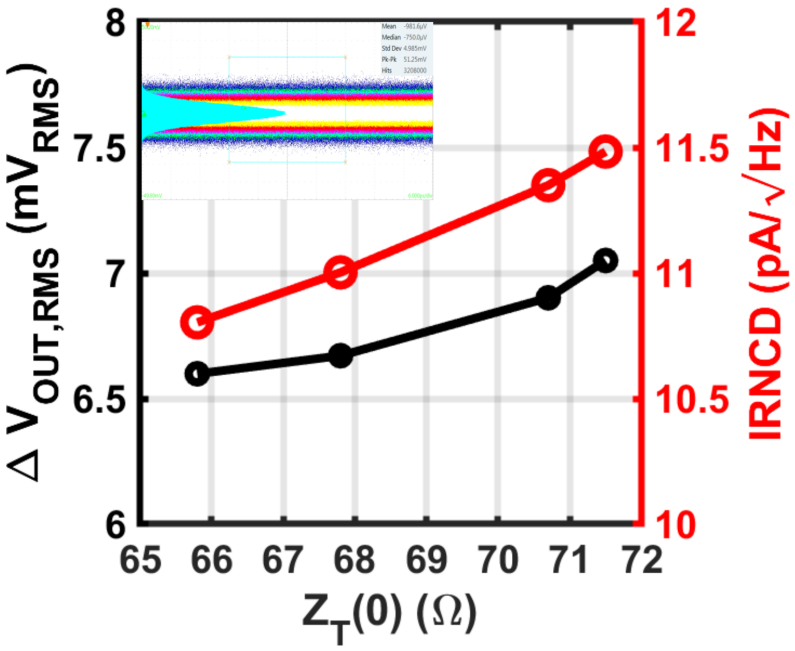


Figure 5.7: Measured output rms noise voltage and calculated input-referred noise current density. Note: the inset is a measured noise histogram with the RXIC set to maximum transimpedance gain: i.e. 71.5 dBΩ.

ential RXICs. Notably, this work provides competitive FOM_{BR} and average IRNCD while providing tuning for higher dynamic range.

5.4 Conclusion

An integrated differential RXIC consisting of a VTIA with A_V-R_F matching is demonstrated to operate with open-eye NRZ transmission up to 60 Gbps and error-free NRZ transmission up to 50 Gbps at BER below 10^{-11}. The total circuit consumes 137 mW for energy efficiency of 2.28 pJ/bit.

Chapter 6

Conclusions to Part I

Part I has introduced a novel benchmarking method was proposed for optical receivers using a FOM_{BW} vs. $\frac{1}{IRNCD^2}$ or FOM_{BR} vs. $\frac{1}{IRNCD^2}$ plot in Chapter 2. The implications on link DC power optimization were thoroughly discussed for direct detection and coherent detection, and case studies involving shunt-feedback and common-base/gate TIAs were explored. The optical receivers in both direct detection links in Chapter 3 and coherent detection links in Chapter 4 exhibited favorable FOM_{BW}-$\frac{1}{IRNCD^2}$ performance versus the state-of-the-art referenced in Chapter 2. In Chapter 5, a variable transimpedance amplifier front-end was demonstrated and exhibited strong FOM_{BR}-$\frac{1}{IRNCD^2}$ versus the state-of-the-art.

6.1 Future Work and Investigation

Multi-level signaling such as 4-PAM in direct detection links and 16-QAM in coherent detection links are pervasive in both industry and academic research thrusts as a means to increase capacity via spectral efficiency. The works presented in Chapters 3, 4, and 5 present RXICs which can be modified to achieve a desirable linearity performance via

THD, and can be optimized in conjunction with the $FOM_{BW/BR}$-$IRNCD$ performance. Continued development of multi-level signaling could potentially pave the way beyond 100s Gbps-per-lambda optical signaling.

Part II

Transmitter Integrated Circuits (TXICs) for Optical Interconnects

Chapter 7

A High-speed TW-MZM Driver Design with Artificial Transmission Line-based Realization of Differential-mode Feed-forward Equalization in a 45-nm CMOS SOI Platform

This chapter is in part a reprint of material in the manuscript, "An 80-Gbps Distributed Driver with Two-Tap Feedforward Equalization in 45-nm CMOS SOI," presented at the 2022 IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF) [17]

This paper presents an integrated differential, distributed Mach-Zehnder modulator (MZM) driver with two-tap feedforward equalization (FFE). The driver consists of two-

stack, pseudo-differential FET stages capable of voltage swings exceeding the V_{DD} (1 V). The measured chip produces error-free (BER $< 10^{-11}$) NRZ transmission up to 64 Gbps with 0.3 UI sampling margin and four-level pulse amplitude modulation (PAM-4) transmission up to 80 Gbps (40 Gbaud) in a 50 Ω environment. The total power consumption of the driver is 310 mW for an energy efficiency of 4.8 pJ/bit for NRZ and 3.9 pJ/bit for PAM-4 when driving a 50 Ω load in an FR-4 PCB assembly.

The driver integrated circuit is also evaluated in an optical transmitter assembly with a traveling-wave Mach-Zehnder Modulator (TW-MZM).

7.1 Introduction

With the increase in data center traffic over the recent years, silicon photonics (SiPh) has emerged as a low-cost and high-volume platform for high-speed and energy-efficient optical links. In traveling-wave Mach-Zehnder modulator (MZM) transmitters, driver circuits make up a significant portion of overall link power consumption due to the need to drive large voltage swings to low-impedance transmission lines. Scaled 45 nm CMOS technology with co-packaged photonics has enabled optical transmitters with data rates up to 50 Gbps and voltage swings up to 4.4 V_{pp} at an energy efficiency of 9 pJ/bit through the use of aggressive two-tap FFE off-chip and stacked FET driver cells [94].

Although monolithic electro-optical SiPh solutions have been proposed. A fully integrated optical transmitter with 90-nm CMOS driver based on a distributed amplifier merged in a travelling wave Mach-Zehnder modulator was reported with open eye transmission up to 30 Gbps while consuming 480 mW (16 pJ/bit) was reported [95].

A 45 nm CMOS SiPh monolithic platform has been demonstrated with the potential to push SiPh-based optical links up to 100 Gbps [75]. This work introduces a stacked-FET driver with an integrated two-tap FFE in 45 nm CMOS SOI technology to enable

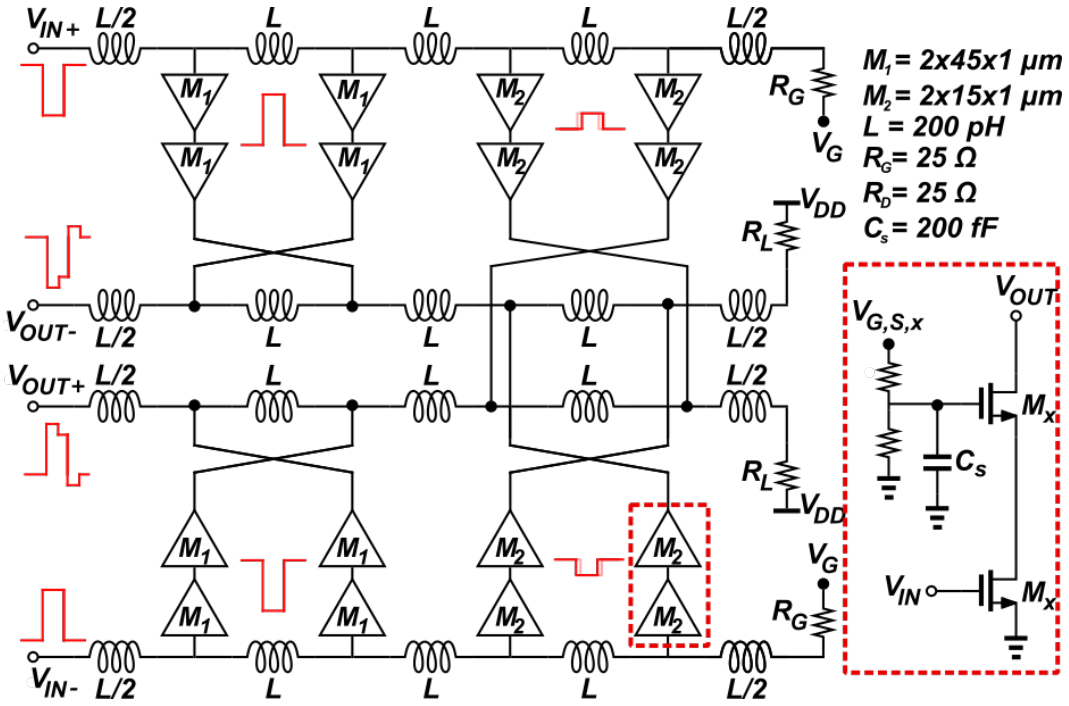


Figure 7.1: Schematic of the integrated MZM driver with a traveling-wave, differential-mode 2-tap feedforward equalizer.

co-packaged and monolithic SiPh MZM-based transmitters above 50 Gbps.

Section II presents the design of the differential FFE driver. Section III presents the measured electrical characteristics in the frequency and time domains. To our knowledge, this paper presents the first high-voltage swing stacked FET MZM driver integrated with a differential feed-forward equalizer integrated on a 45 nm CMOS SOI platform capable of the highest error-free NRZ data rate (64 Gbps) with widest error-free unit-interval sampling margin (0.3UI), the fastest open-eye PAM-4 data rate (80 Gbps), and the lowest energy efficiency for integrated drivers capable of data rates above 40 Gbps.

7.2 Design of MZM FFE Driver

The MZM driver comprises a distributed two-tap FFE with stacked FET-based g_m cells in a pseudo-differential configuration. The g_m cells of each tap comprise the cross-

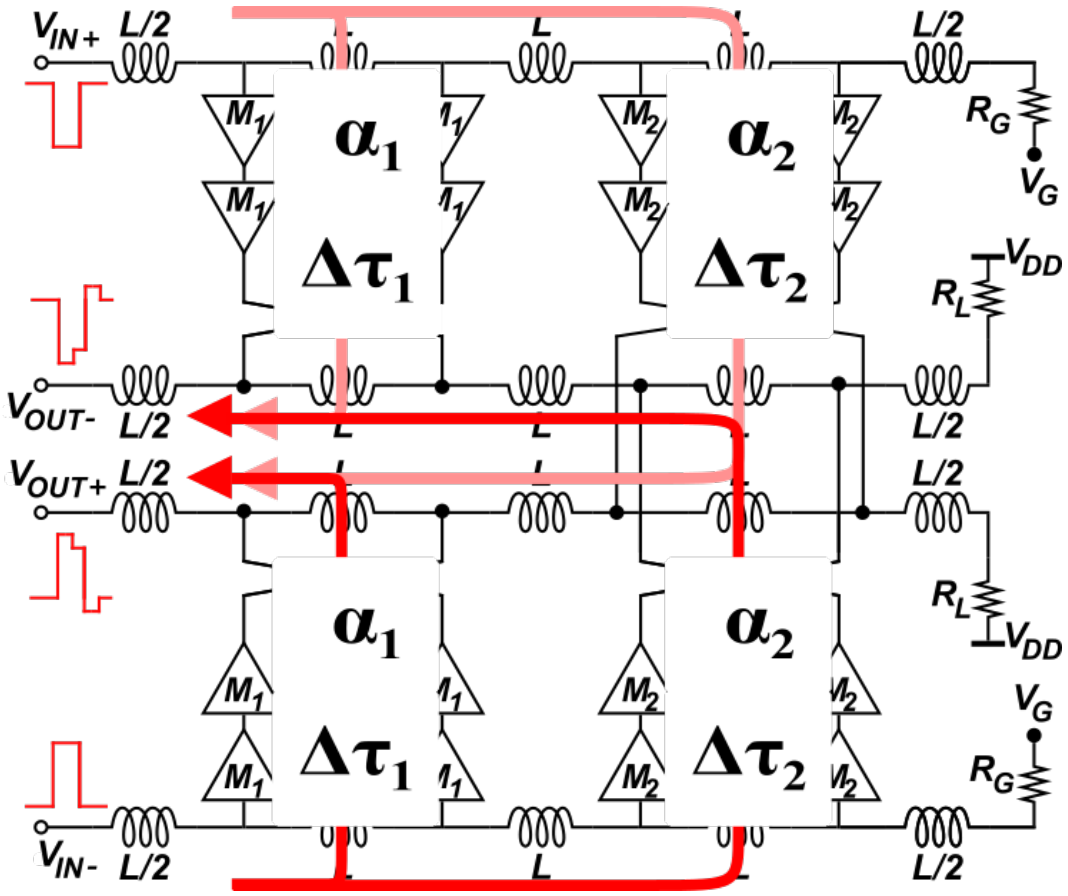


Figure 7.2: Schematic of the integrated MZM driver with a traveling-wave, differential-mode 2-tap feedforward equalizer with details of the waveform construction.

over topology which allow for simultaneous maximization of the tap delay, bandwidth, and gain [96]. Furthermore, the two-tap FFE is constructed by a differential crossover of the second distributed tap such that a subtractive operation is performed as indicated in the following expression,

$$\Delta V_{out,2-FFE} = \alpha_1 V_{in}(t - \Delta\tau_1) - \alpha_2 V_{in}(t - \Delta\tau_2) \tag{7.1}$$

where α_1 and α_2 are the tap coefficients, and τ_1 and τ_2 are the tap delays. The schematic of the MZM driver and the construction of the differential two-tap FFE waveform is illustrated in Fig. 7.1 and Fig. 7.2.

The NMOS devices of the main tap, $M_{1,p}$ and $M_{1,n}$, are sized as 2x45x1 μm and the NMOS devices of the second tap, $M_{2,p}$ and $M_{2,n}$, are sized as 2x15x1 μm. The sizing was determined to produce an baseline voltage swing of 2.5 V_{pp} and a peaked (i.e. two-tap FFE) voltage swing of 2 V_{pp}. The gate and drain capacitors are distributed through small 200 pH inductors which allows for a sub-unit interval second tap delay of 3 ps from the gate of M_1 to the gate of M_2. Consequently, the total second-tap delay is maintained below 6 ps which indicates less than 0.4UI of peaking at 64 Gbps. The two-tap FFE waveform peaking (i.e. delayed amplitude subtraction) can be adjusted up to 20% of the main-tap voltage swing by tuning $V_{G,S,2}$ of M_2. The ac-grounds at V_{DD} and V_G are set by large bypass capacitor banks of roughly 120 pF.

7.3 Measurements

7.3.1 Electrical Characterization

The RFIC was fabricated in a 45-nm CMOS SOI process with an area of 1.45 mm-sq. Fig. 7.3 illustrates the chip microphotograph. The FFE driver draws 94 mA from a

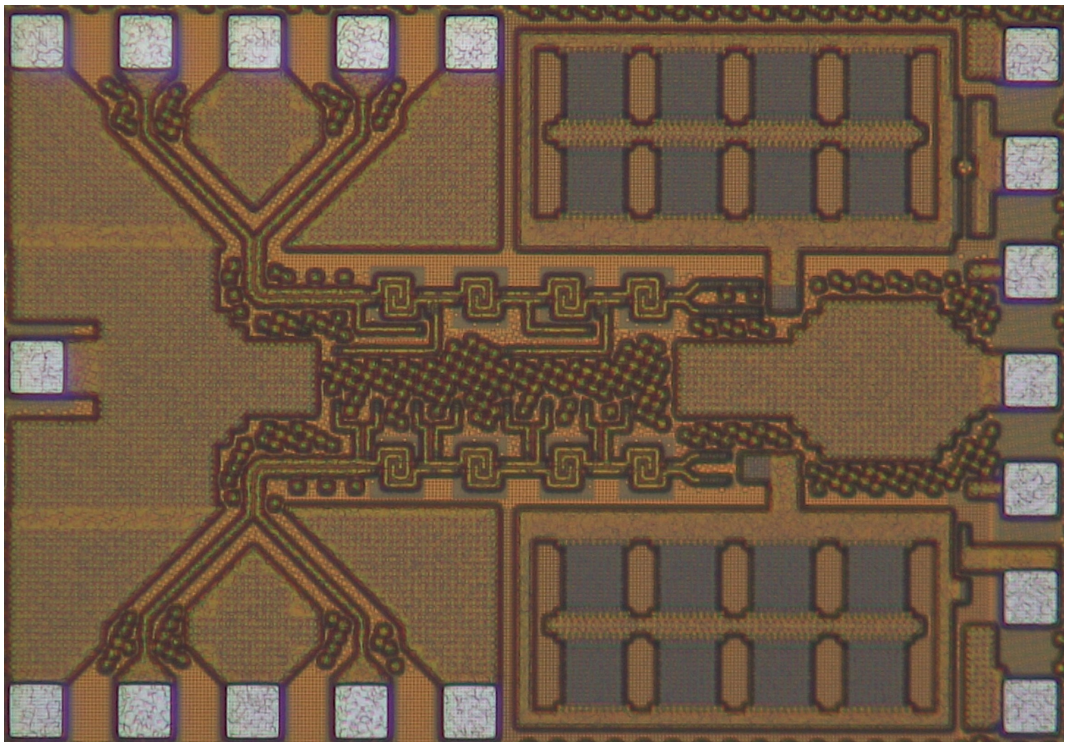


Figure 7.3: Microphotograph of MZM driver.

3.3-V supply for a power consumption of 310 mW.

The electrical frequency response characteristics were measured using a Keysight PNA-X and 67 GHz GGB GSGSG RF probes. True differential S-parameters were measured up to 67 GHz. The measured $S_{DD,21}$ of the chip is plotted in Fig. 7.4 and indicates that the equalizer can produce over 3 dB peaking between the low and high-frequency response.

Eye diagrams and bit error rate (BER) were measured on a custom FR-4 PCB assembly with roughly 5 dB packaging loss at 40 GHz [77]. A high-speed bit pattern generator (BPG) (SHF 12105A) was synchronized with a clock generator (CG) (SHF 78212A) in a full-clock configuration. The output of the driver was then alternately connected to a Tektronix digital serial analyzer sampling oscilloscope (DSA8300) through a sampling module (Tektronix 80E11) with a 2 meter extender (Tektronix 80X02) for eye diagram

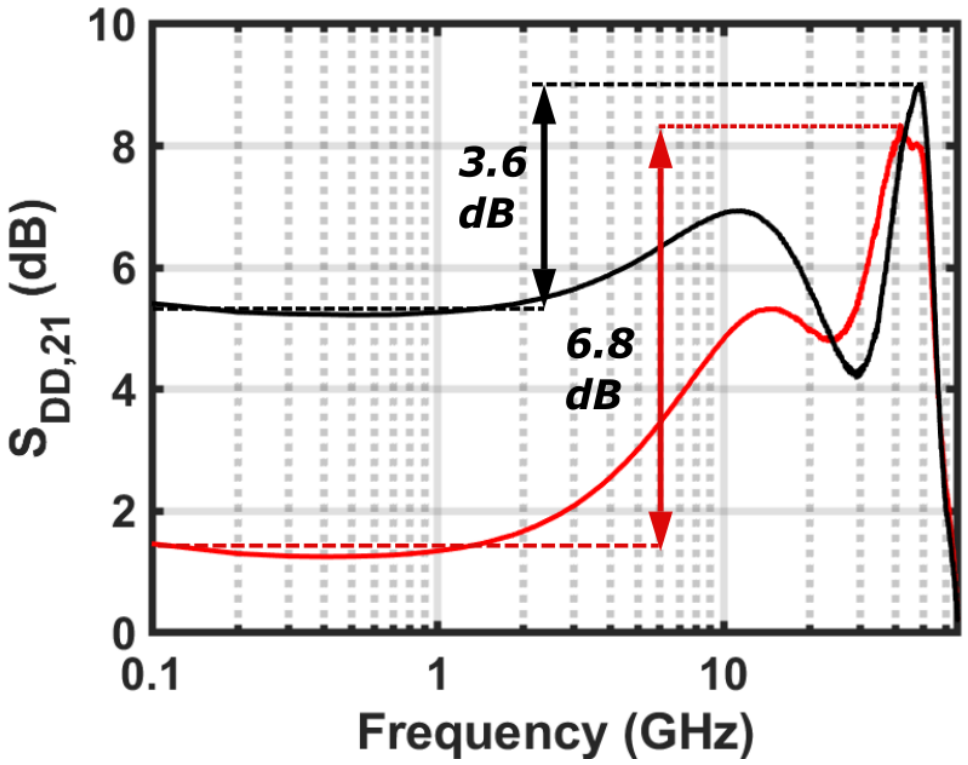
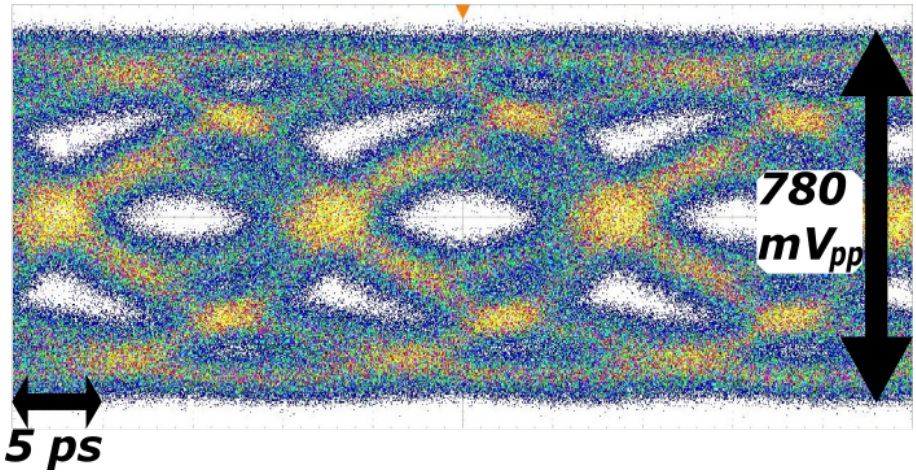
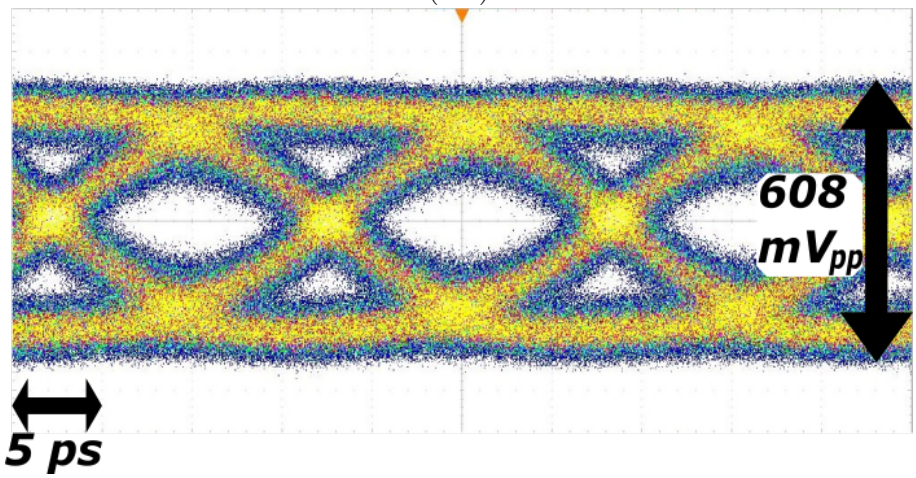


Figure 7.4: Measured $S_{DD,21}$ with the second tap off (black) and on (red).



(2.a)



(2.b)

Figure 7.5: Measured differential eye diagrams at 64 Gbps with the second tap (a) off and (b) on using PRBS31.

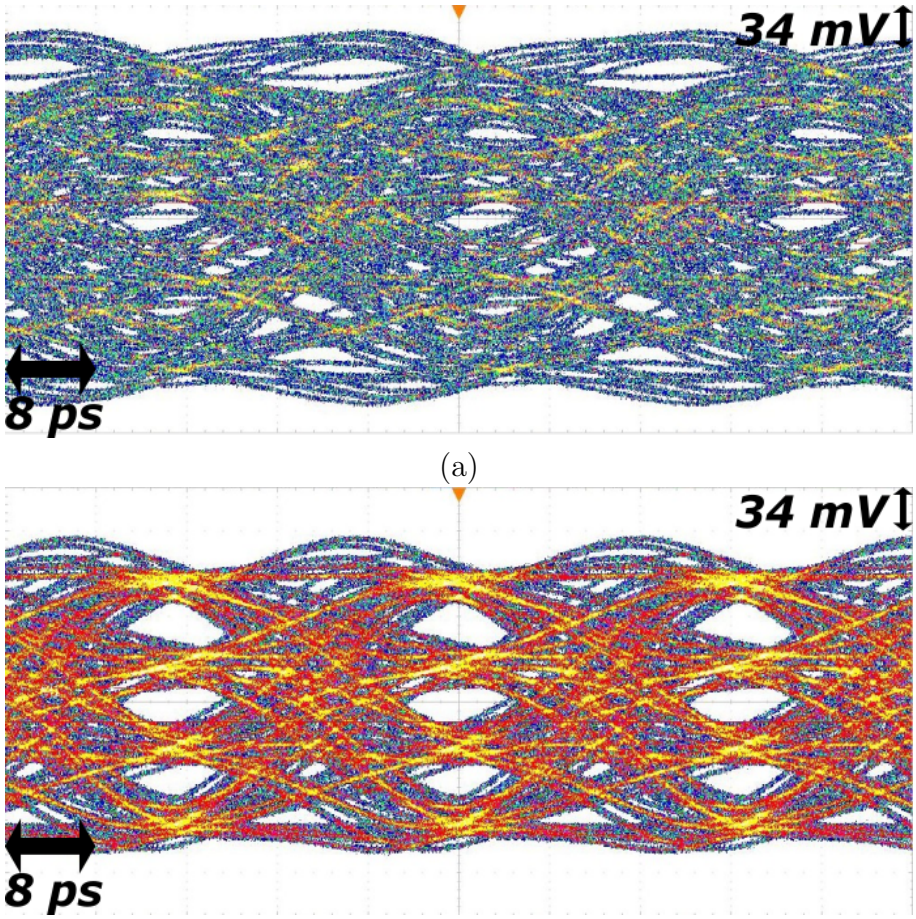


Figure 7.6: Measured PAM-4 eye diagrams for 40 Gbaud (80Gbps) with the second tap (a) off and (b) on using PRBS31.

measurements, and to an error analyzer (EA) (SHF 1104A) which is synchronized with the CG for real-time BER measurements. Short 4-inch 67 GHz cables and 30 kHz DC-blocking capacitors were used between the differential input and output of the driver PCB assembly.

Fig. 7.5 demonstrates the measured differential NRZ output eye diagrams of the MZM driver with a 10 dB attenuator at the output of the driver with the BPG data rate set to 64 Gbps at an input amplitude of 650 mV. Additionally, Fig. 7.6 demonstrates the measured differential PAM-4 output eye diagrams at 40 GBaud or 80 Gb/s to indicate open eye conditions.

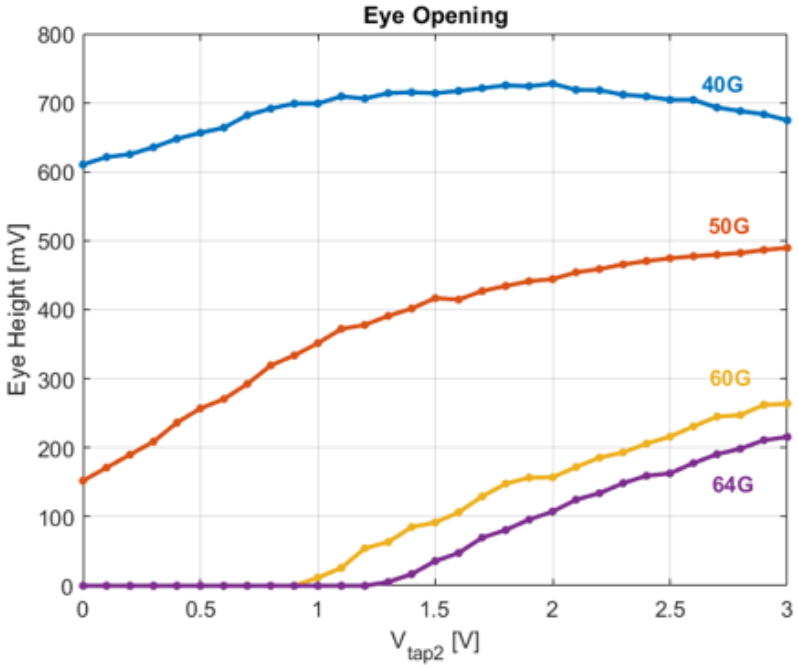


Figure 7.7: Measured eye opening vs. second tap bias at data rates 50 Gbps, 60 Gbps, and 64 Gbps.

The BER measurements for NRZ transmission were measured with the second tap of the driver on and configured to run for two minutes with zero errors counted. This corresponds to a confidence level between 99.8% at 50 Gbps to 99.95% at 64 Gbps for a BER $< 10^{-13}$. The BER bathtub measurements are demonstrated in Fig. 7.8 for data

Table 7.1: State-of-the-art Comparison for NRZ and PAM-4 CMOS and SiGe Optical MZM Drivers

Parameter \ Reference	[97]	[98]	[99]	[100]	[94]	[101]	This Work
Technology	22 nm CMOS SOI	65 nm CMOS	0.25 μm BiCMOS	28 nm CMOS	45 nm CMOS SOI	0.25 μm BiCMOS	45 nm CMOS SOI
Modulation	NRZ	NRZ	NRZ	NRZ	NRZ	PAM-4	NRZ/PAM-4
Data Rate (Gbps)	30	30	28	44	50	40	64/80
Voltage Swing (V_{pp})	3.75	1.68	3	4.3-5.2	4.4	4	2-2.5
Energy (pJ/bit)	2.2	10.8	6.25	9.3	9	27.5	4.84/3.9
E/O Integration	No	Yes	No	Yes	Yes	Yes	No

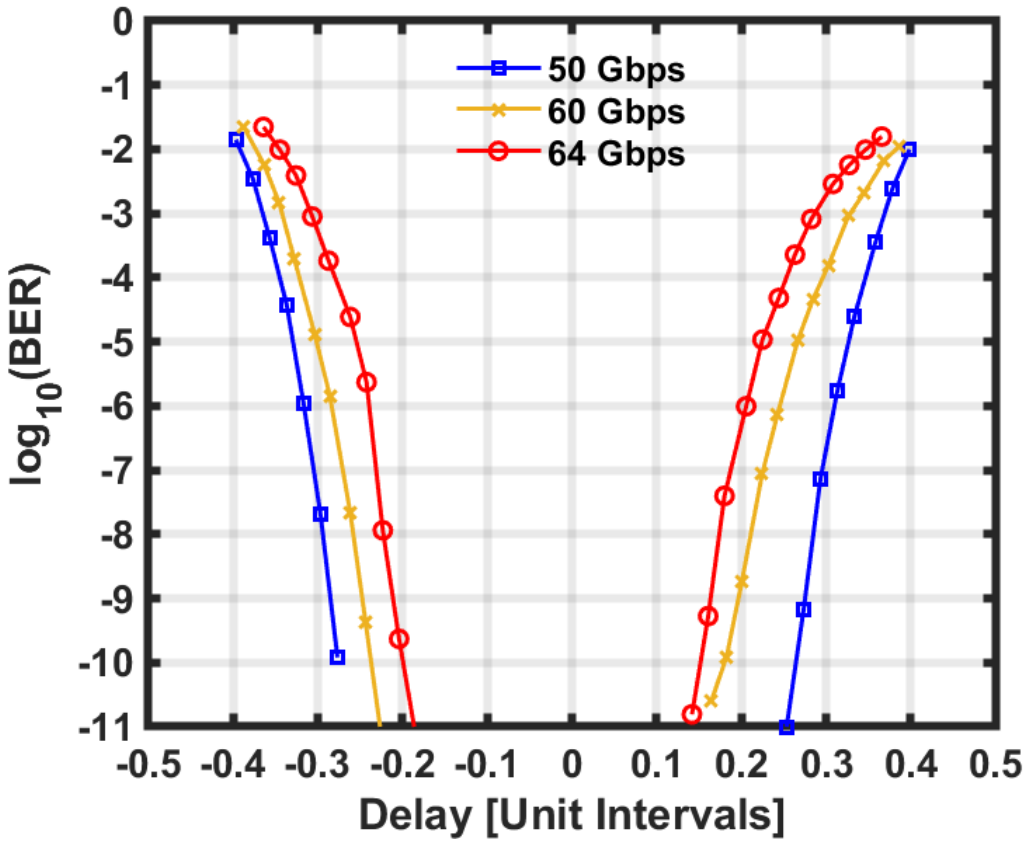


Figure 7.8: Measured BER bathtub curves for data rates of 50 Gbps, 60 Gbps, and 64 Gbps for PRBS7.

rates of 50 Gbps, 60 Gbps, and 64 Gbps. Notably, at a BER of $< 10^{-11}$, over 0.5UI sampling margin is produced at 50 Gbps and over 0.3UI at 64 Gbps.

Table 7.1 demonstrates the state-of-the-art performance for MZM drivers across CMOS and complementary BiCMOS technologies. Notably, this work provides the highest data rate and energy efficiency.

7.3.2 Optical Characterization

The assembly pictured in Fig. 7.9 was used to evaluate the electro-optical performance of the optical MZM transmitter. The optoelectronic transmitter time domain

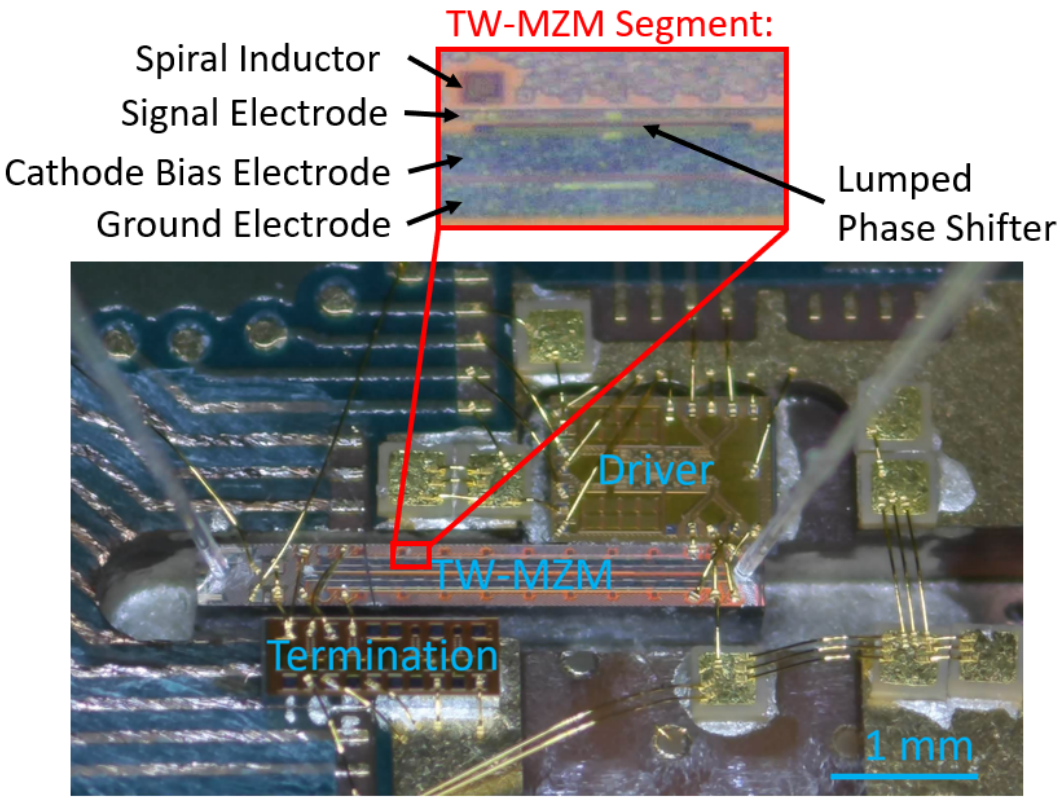


Figure 7.9: Measured BER bathtub curves for data rates of 50 Gbps, 60 Gbps, and 64 Gbps for PRBS7.

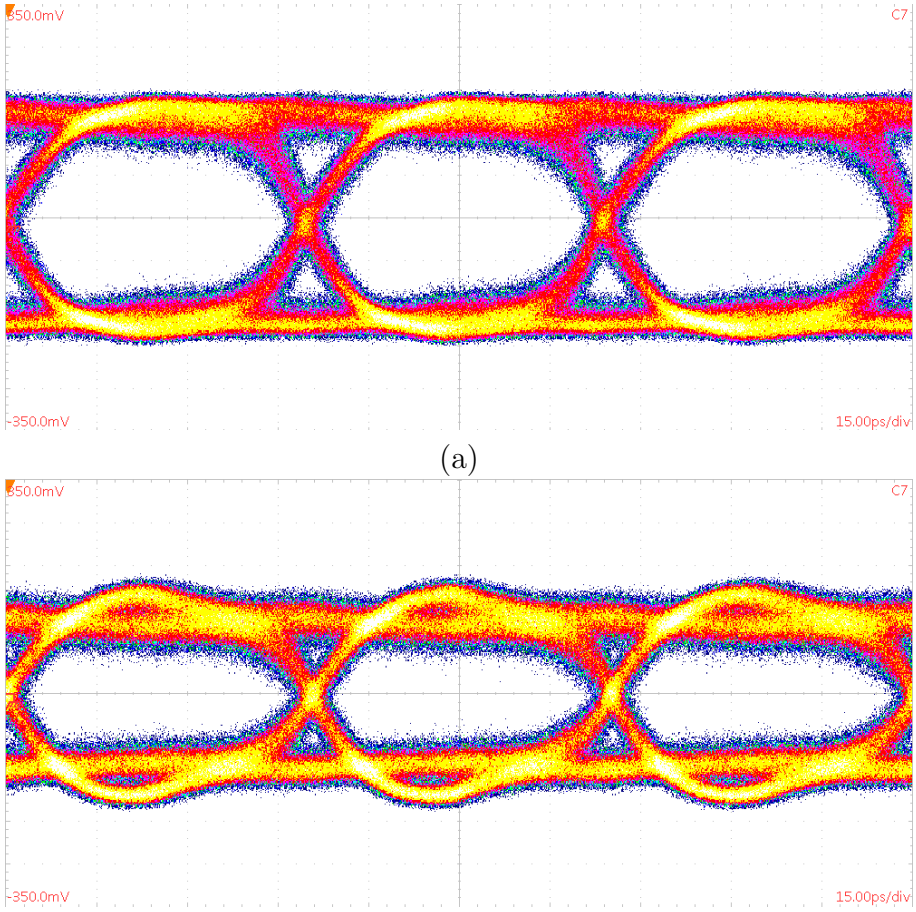
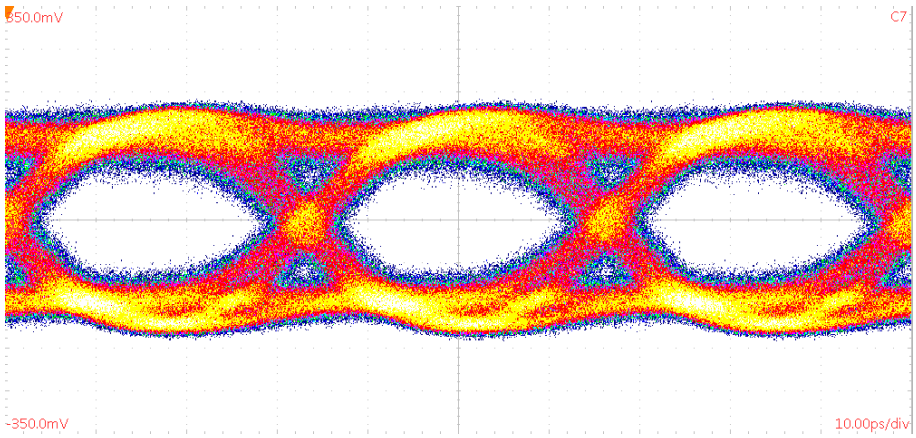


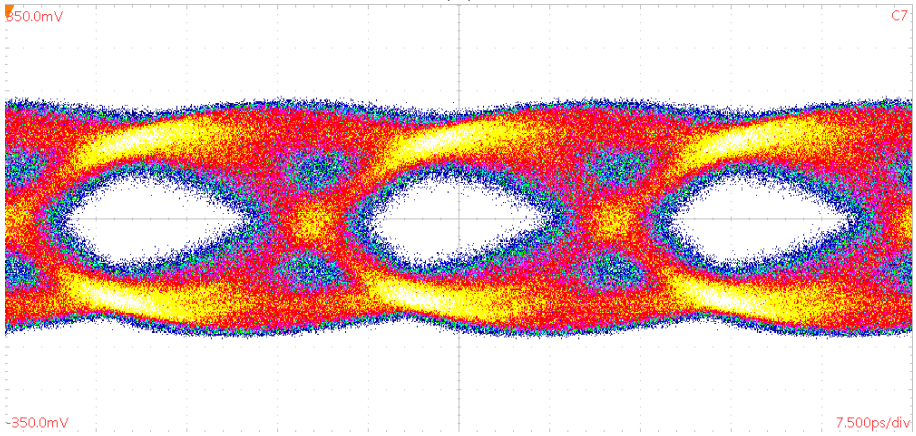
Figure 7.10: Measured 20 Gbps NRZ optical eye diagrams showing effect of the 2-Tap FFE (a) off and (b) on.

performance was measured by driving it with bit pattern generator (SHF 12105 A) with 1300 $mV_{pp,diff}$. A 43 Gbps reference receiver (Finisar XPRV2322A) and electrical sampling module (Tektronix 80E11) with 60 GHz BW were used to measure the eye diagrams shown in Fig. 7.10 and Fig. 7.11. Reasonably open eye diagrams were produced up to 50 Gbps.

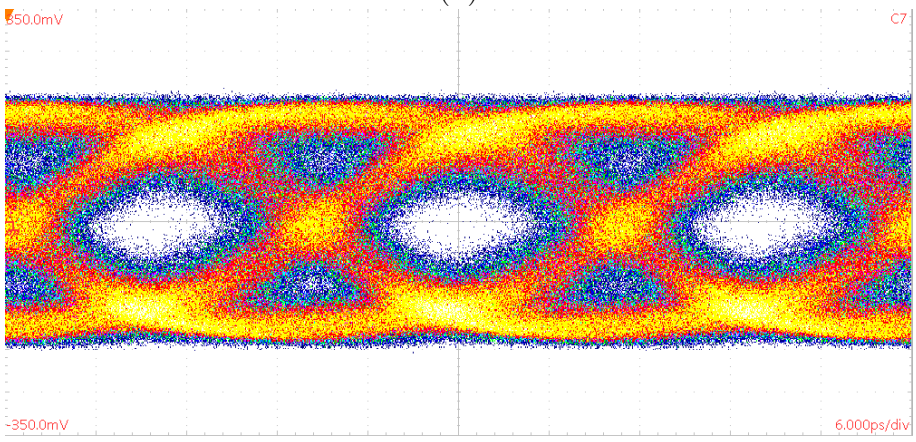
Bathtub curves characterizing the full transmitter operation with the reference receiver and a bit error rate tester (SHF 11104A) are shown in Fig. 7.12. Due to the BW limitations of the reference receiver, higher baudrate bathtubs are not reported. The



(a)



(b)



(c)

Figure 7.11: Measured NRZ optical eye diagrams with the 2-Tap FFE on for (a) 30, (b) 40, and (c) 50 Gbps.

overall transmitter consumes 233 mW with driver FFE off, and 282 mW with driver FFE on, corresponding to 4.7 and 5.6 pJ/bit at 50 Gbps, respectively.

7.4 Conclusions

An integrated differential, traveling-wave 2-tap FFE driver is demonstrated to operate with error-free NRZ transmission up to 64 Gbps with 0.3 UI sampling margin at BER below 10^{-11}. The total circuit consumes 310 mW for energy efficiency of 4.8 pJ/bit with NRZ and 3.9 pJ/bit with PAM-4. Optical characterization indicates 50 Gbps operation at 5.6 pJ/bit.

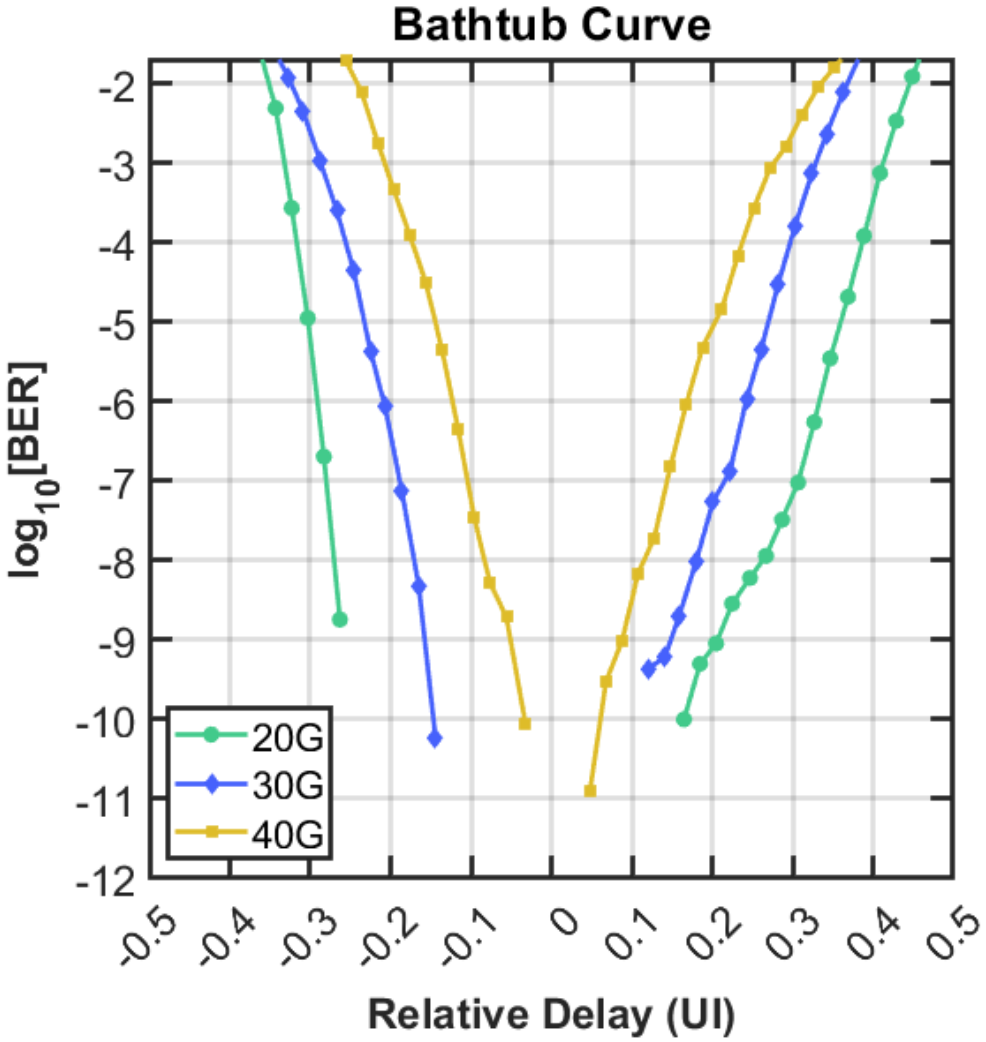


Figure 7.12: Measured BER bathtub curves for data rates of 50 Gbps, 60 Gbps, and 64 Gbps for PRBS7.

Chapter 8

Consolidated Equalizer and Driver Design for Energy-efficienct and High-Speed VCSEL-based Transmitters

This chapter is in part a reprint of material in the manuscript, "A 2.85 pJ/bit, 52-Gbps NRZ VCSEL Driver with Two-Tap Feedforward Equalization," presented at the 2020 IEEE International Microwave Symposium [18]

We report an energy-efficient vertical cavity surface-emitting laser (VCSEL) driver implemented in a 130 nm SiGe HBT technology. Operation at data rates as high as 60 Gbps is demonstrated with the use of two-tap feed-forward equalizer (FFE) using a differentiator circuit at the output driver stage that eliminates the need for inductors and results in compact area (0.032 mm^2). The current contribution of the differentiator produces a trade-off between energy efficiency and bandwidth enhancement. Error-free (BER $< 10^{-12}$) non-return-to-zero (NRZ) transmission up to 52 Gbps is reported at an

efficiency of 2.85 pJ/bit.

8.1 Introduction

Recent trends in data center interconnects (DCI) have pushed data rates to more than 56 Gb/s and energy-efficient technologies are demanded to maintain growth of emerging 5G and Internet of Things (IoT) applications [1]. DCI comprise two types of links: short-reach interconnects within the rack (<3m) and longer-reach interconnects between racks (<2km). The low loss of short-reach interconnects can allow direct modulation of VCSELs as an active cable replacement. Above 56 Gb/s, PAM-4 has been adopted as a standard for high-speed signaling with significant forward error correction (FEC). However, NRZ links continue to demonstrate error-free transmission without the need for FEC [**?**].

The main limitation of short-reach optical links is that VCSELs are bandwidth-limited in both electrical (parasitic low-pass filtering) and optical (damping in optical laser dynamics) domains. To overcome these bandwidth limitations, FFE architectures have been proposed for driver circuitry leading to record error-free data rates up to 71 Gbps in prior work [64]. More recently, the focus has been on optimization of VCSEL links for energy-efficiency at 40 to 50 Gbps [102] [103].

This paper presents a 52-Gbps VCSEL driver with a modified two-tap FFE design for short-reach multi-mode fiber (MMF) links for short-range DCI. The design of the two-tap FFE obtains error-free electrical data transmission up to 52 Gbps at a energy efficiency of 2.85 pJ/bit. Section II covers the design of the VCSEL driver with FFE. Section III presents the measured electrical characterization data from the fabricated SiGe chip. Through consolidation of FFE, bias, and drive circuitry at the output stage, this is the most energy-efficient VCSEL driver above 50 Gb/s to our knowledge.

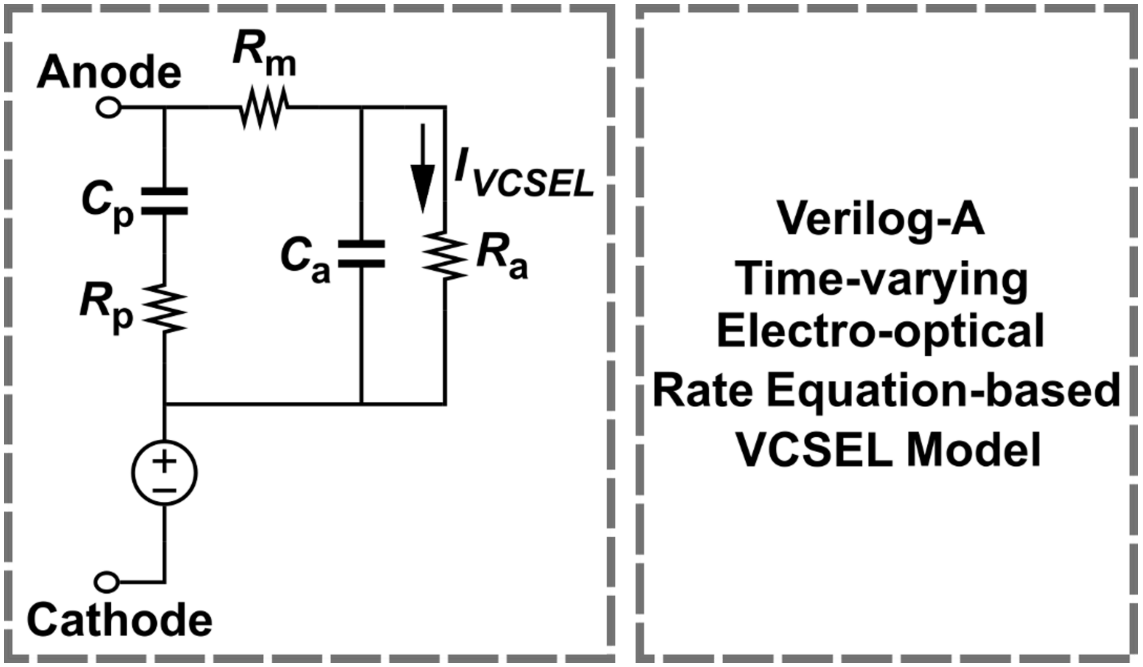


Figure 8.1: VCSEL model.

8.2 Modeling VCSEL Dynamics

8.2.1 Frequency-dependent Characteristics

The frequency-dependent VCSEL dynamics can be broken down into two categories: the electrical dynamics and the electro-optical dynamics. These categories are illustrated in Figure 8.1. The electrical dynamics are dictated by an RC network which accounts for the parasitics of the fabricated VCSEL device that the input current sees. The resulting current, I_{VCSEL}, injects the electrical carriers for VCSEL to emit light. The emission of light in the VCSEL device is dictated by highly nonlinear mechanisms that depend on: (1) the bias current, (2) the modulation current, and (3) the VCSEL device structure. Consequently, the design of a driver integrated circuit must accommodate variation in VCSEL device structure, so tunability of the bias current and modulation current is desirable. Furthermore, by modeling of the VCSEL's nonlinear dynamics, the bias and

modulation currents of the driver circuit can be configured for the desired response.

Previous work has captured the nonlinear rate-equation-based modeling using Verilog-A to enable co-design of an electronic driver and a given VCSEL device [102, 104–107]. Comprehensive modeling which includes thermal-dependence of VCSEL model parameters have been explored in [104].

The electro-optical dynamics of a VCSEL are described by the coupled rate-equations of Eqns. 8.1a and 8.1b [108].

$$\frac{dN_e}{dt} = \frac{I_{VCSEL}}{qV} - \frac{N}{\tau_{sp}} - GN_eN_p \tag{8.1a}$$

$$\frac{dN_p}{dt} = GN_eN_p + \frac{\beta_{sp}}{\tau_{sp}} - \frac{N}{\tau_{sp}} \tag{8.1b}$$

The Laplace transform allows the rate equations to be expressed as a second-order transfer function as described by (8.2).

$$\frac{P_{opt}(s)}{\eta(I_{VCSEL} - I_{th})(s)} = \frac{1}{1 - \frac{f^2}{f_r^2} + \frac{j\gamma f}{f_r^2}} \tag{8.2}$$

where γ, f_r, and η can be expressed as (8.3a), (8.3b), and (8.3c), respectively.

$$\gamma = Kf_r^2 + \gamma_o \tag{8.3a}$$

$$f_r = D\sqrt{I_{VCSEL} - I_{th}} \tag{8.3b}$$

$$\eta = \frac{hvv_g\alpha_m}{q} \tag{8.3c}$$

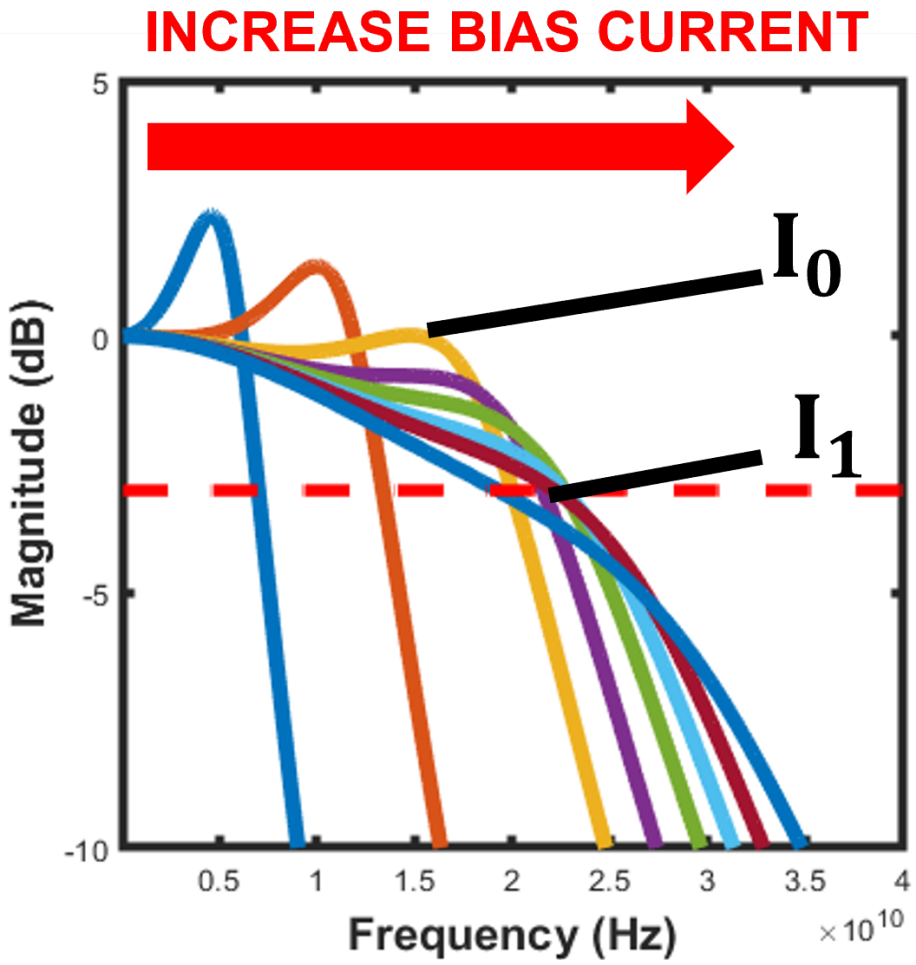


Figure 8.2: Frequency response of VCSEL device with varied bias current. Notably, the VCSELs bandwidth and peaking are highly dependent on the bias current. A high extinction ratio operation can reduce the frequency response to a simple low-pass filter.

The resulting frequency response at various bias currents can be visualized for a generic VCSEL device in Fig. 8.2.

8.3 2-Tap FFE VCSEL Driver Design

The VCSEL driver is designed to source a fixed current through the VCSEL during the ON state and steer the current into the dummy load during the OFF state. Typically, the VCSEL consumes less than 10 mA from a 2 V supply for high-speed operation.

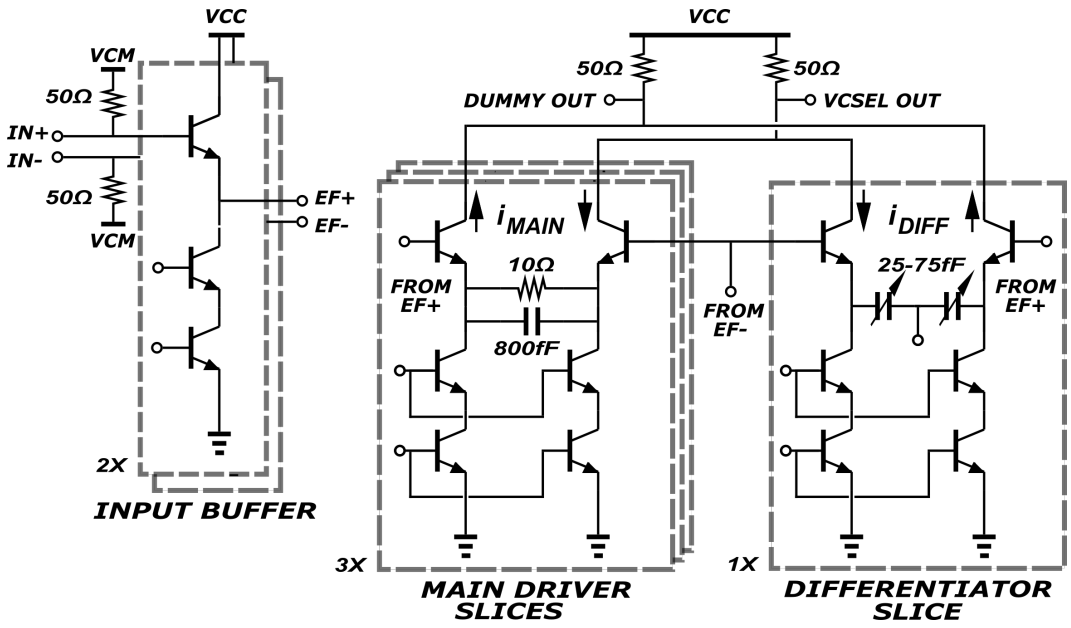


Figure 8.3: Circuit schematic of the proposed 2-tap FFE VCSEL driver

Table 8.1: Emitter lengths for VCSEL driver 130-nm NPN devices.

Emitter Length	Diff. Pair	Current Source
Input Buffer	3 μm	2 μm
Main: Slice 1	2 μm	2 μm
Main: Slice 2	3 μm	2 μm
Main: Slice 3	6 μm	4 μm
Differentiator	6 μm	4/2/2 μm

Due to the current steering, the DC power consumption is relatively fixed at 20 mW. Consequently, a VCSEL driver can theoretically achieve extremely low energy efficiency at less than 1 pJ/b for 56 Gb/s data rates. However, the VCSEL requires some overhead that increases the required power such as equalization that compensates for the VCSEL electro-optical response to achieve high baud rates, resulting in an increase in energy efficiency.

Conventional two-tap FFE has been demonstrated to improve link performance via bit rate, sensitivity, jitter, and power efficiency [109].

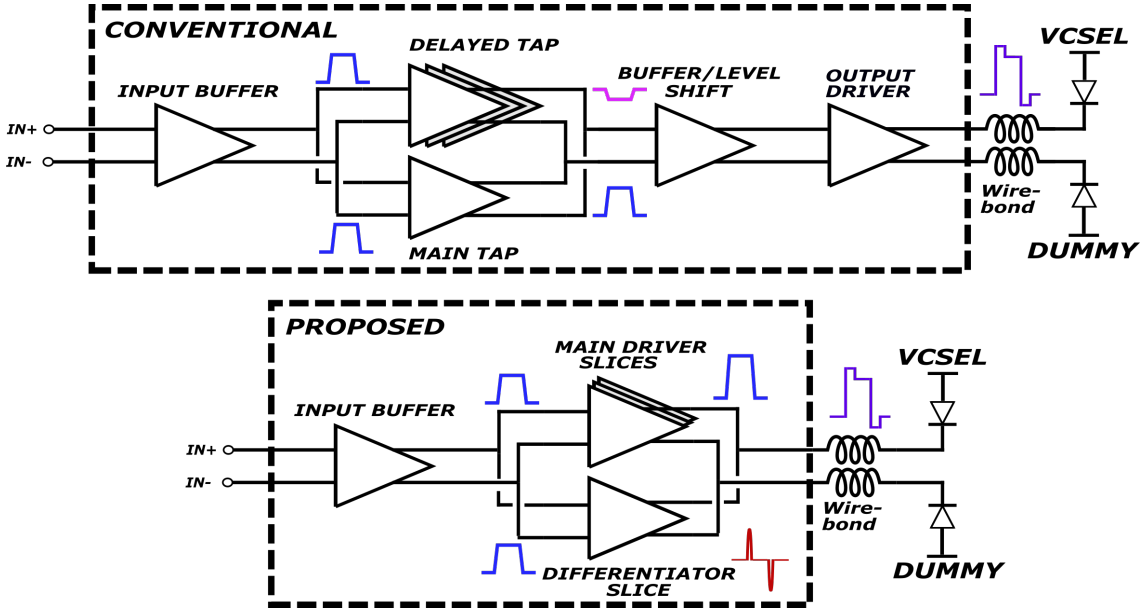


Figure 8.4: VCSEL transmitter block diagrams for a conventional 2-Tap FFE implementation and the proposed modified 2-Tap FFE implementation.

A conventional two-tap FFE is implemented in an intermediate stage as two differential pair stages with a delay included in one branch as illustrated at the top of Fig. 8.4. The delay cell is typically one half of a unit interval (UI) which can be tuned if implemented as active delay. While the primary branch establishes the on and off current levels, the secondary branch is modulated at a lower amplitude and inverted before summing with the primary branch to shape the rising and falling edge of the data.

Prior work modified the FFE design by reducing the number of delay cells needed for a three-tap FFE from two delays to one delay [**?**]. The disadvantage of these FFE approaches are the power consumption to implement the delays and/or the out-of-phase current combining that results in amplitude de-emphasis.

The proposed driver design is shown at the bottom of Fig. 8.4 and modifies the FFE architecture to minimize the area and power costs of active or passive delay implementations for 2- and 3-tap FFE designs while also consolidating the FFE implementation at the output stage. Furthermore, energy efficiency is improved because the full ampli-

tude swing of the main path is preserved as the current for peaking does not reduce the amplitude.

The schematic of the VCSEL driver is illustrated in Fig. 8.3 and realizes the primary and differentiator branches through current summing. The input voltage is terminated into 50 Ω at a common-mode voltage node decoupled through on-chip capacitance. The 50 Ω terminations are followed by emitter follower stages that increase the input impedance of the driver circuit to increase the bandwidth-limiting pole that would arise from the 50 Ω termination and the common emitter-based output driver stage. The output stage consolidates three functions for a VCSEL driver: (1) current modulation through the main slice, (2) versatile peaking/fast modulation and (3) bias current to the load (i.e. VCSEL) through the differentiator slice.

The frequency response can be expressed in terms of the VCSEL current I_{out} produced in response to an applied voltage V_{in}. The primary branch uses emitter degeneration to provide some peaking of the response. The differentiator branch uses only capacitive emitter degeneration to produce the peaking. The output current is

$$\begin{aligned} I_{out} &= \alpha_0 V_{in} + s\alpha_1 V_{in} \\ &\approx (\frac{1}{R_e}\frac{1+sC_eR_e}{1+sC_e/g_{m1}} + \frac{sC_{diff}}{1+sC_{diff}/g_{m2}})V_{in} \end{aligned} \tag{8.4}$$

where g_{m2} is the transconductance of the differentiator stages, R_e, C_e are the emitter degeneration of the main branch and C_{diff} is the capacitor in the differentiator branch. By controlling the C_{diff} and gm_2, the peaking of the differentiator can be tailored. By controlling gm_1, the amplitude of the current is modulated.

The main driver slice comprises three differential pair stages with RC degeneration in parallel with the current sources. The three main modulation slices provide 8-level modulation current control. The HBT devices of each slice are optimized for peak f_T

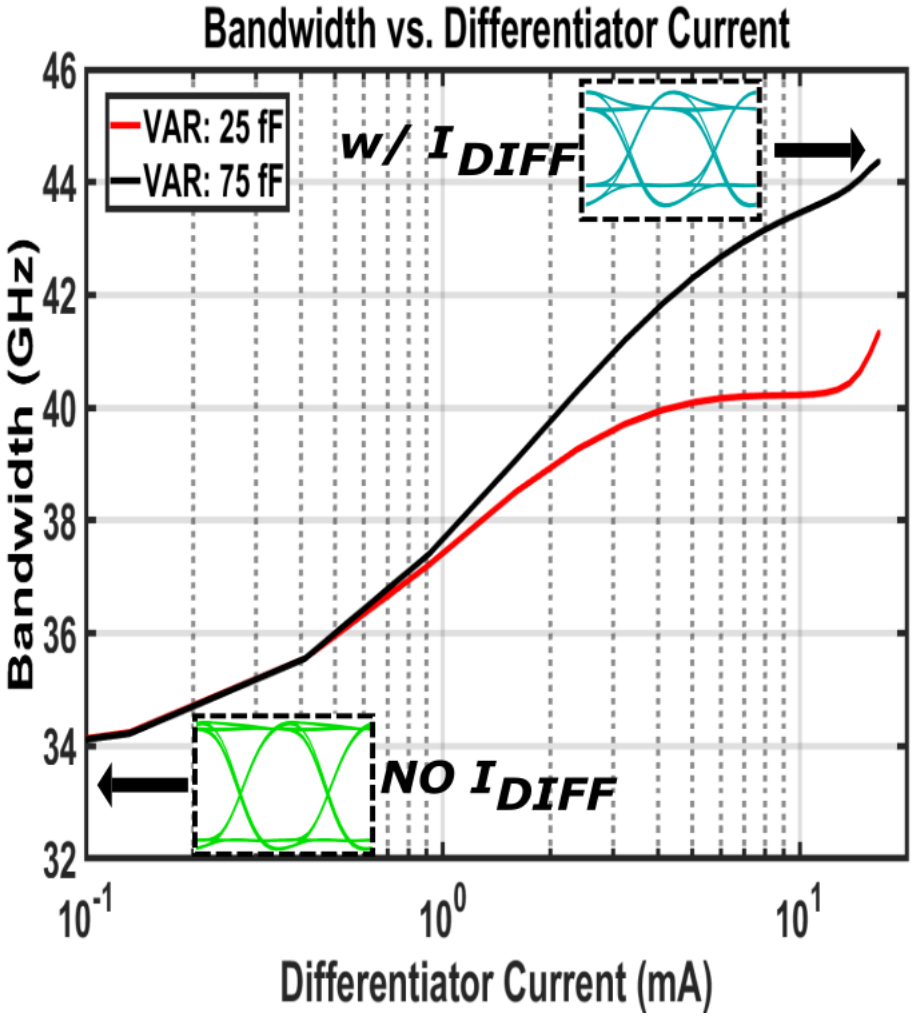


Figure 8.5: Simulated effect of differentiator current in peaking mode on VCSEL driver bandwidth. Simulated eye diagrams predict peaking in eyes with increased differentiator current at 50 Gbps.

for modulation currents of 2 mA, 4 mA, and 8 mA. This enables variable modulation intensity in a VCSEL optical link without compromising speed of main slice devices. Table 1 lists the transistor sizing for the input buffer, main, and differentiator stages.

In order to minimize capacitive loading at the output only a single differentiator slice was included and the npn device size was optimized for peak f_T in the mid-level of the operating bias current range of 2 mA to 14 mA (4 mA to 28 mA for differential pair). The capacitors degenerating the differential pair are back-to-back varactors tapped for tunable capacitive control over 25 fF to 70 fF. The differentiator is simulated to have a strong effect on bandwidth extension of the driver. Furthermore, the close integration of the main slices along with the differentiator slice ensures that there is negligible delay between the current summed at the output node.

Fig. 8.5 demonstrates that the overall bandwidth of VCSEL driver can improve from 34 GHz to over 44 GHz with the varactor tuned for maximum capacitance (i.e. 75 fF) assuming 200 pH wirebonds. As predicted from (1), the bandwidth extension can be improved further with variation in the C_{diff}. This bandwidth extension allows for 50+ Gbps operation.

The differentiator slice has multiple modes of operation with respect to the input common-mode voltage as demonstrated in Fig. 8.7. This versatility allows for the differentiator slice to be utilized for frequency peaking, a standalone 2-tap FFE waveform generator, or a fast current modulator stage. The high impedance cascode-based current sources preserves constant current bias over a wide range of common-mode input voltages with a minimum headroom of 800 mV.

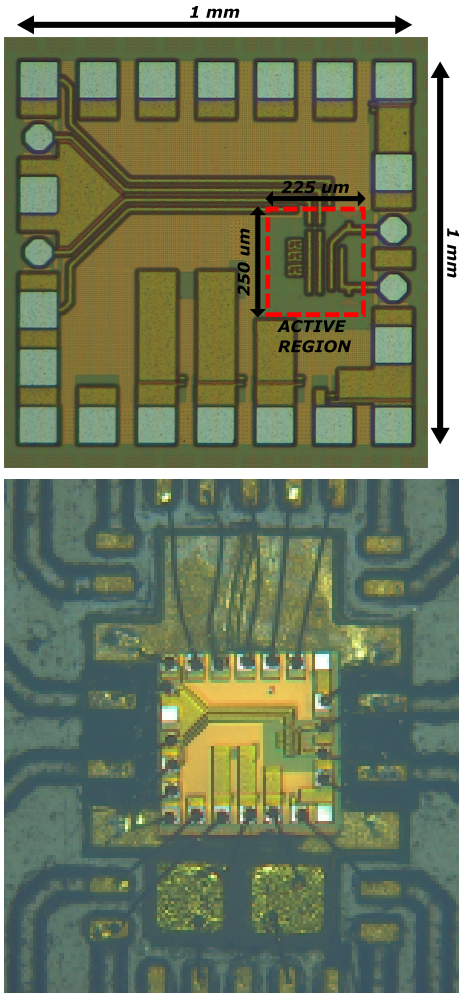


Figure 8.6: Photographs of die with active region of driver circuitry outlined and assembly on constructed PCB.

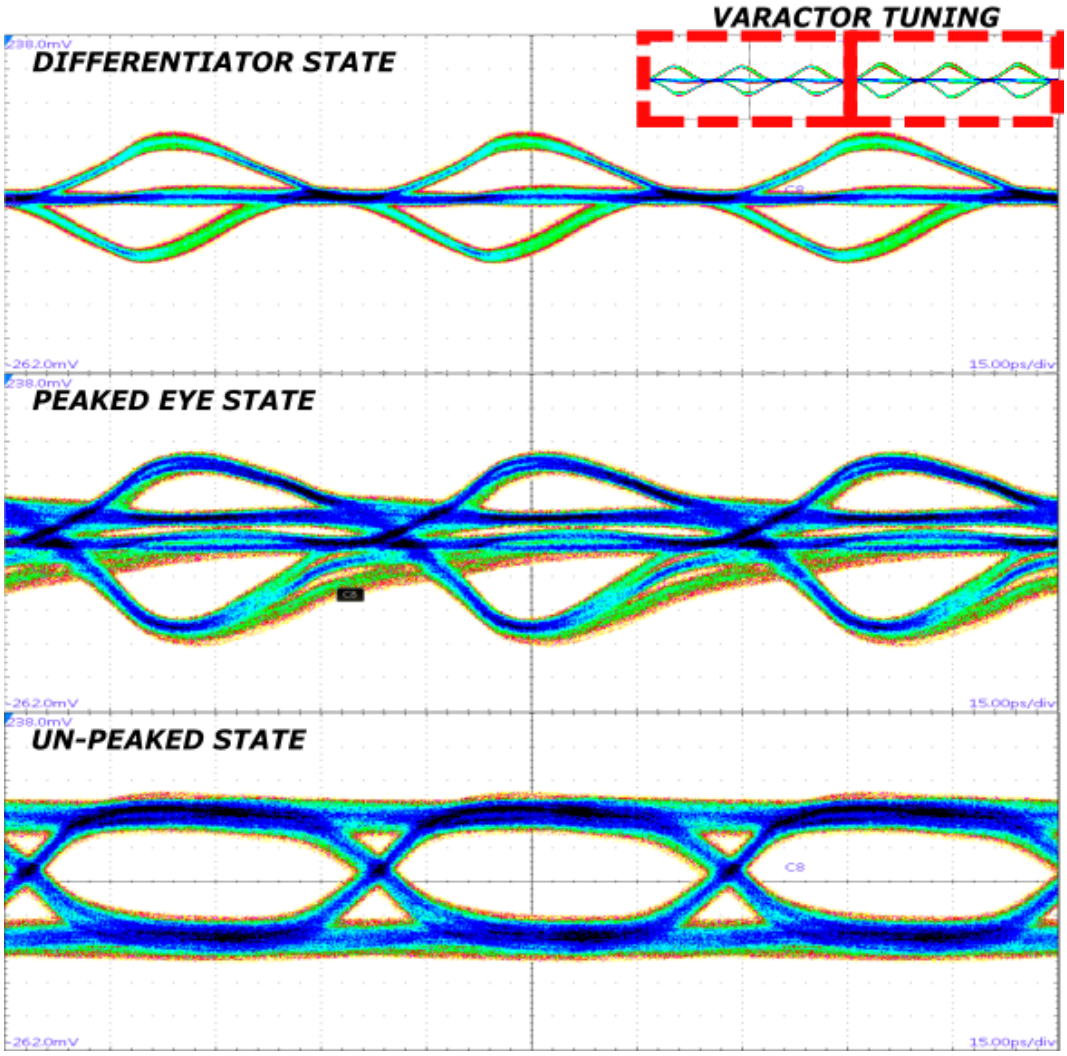


Figure 8.7: Differentiator modes of operation with respect to input common-mode voltage level within range 2.5 V to 3.1 V. The varactors allow for extended capacitance range for higher peaking (up to 10% peaking control). These images are the result of 800 acquisitions of 20 Gbps PRBS11 waveforms.

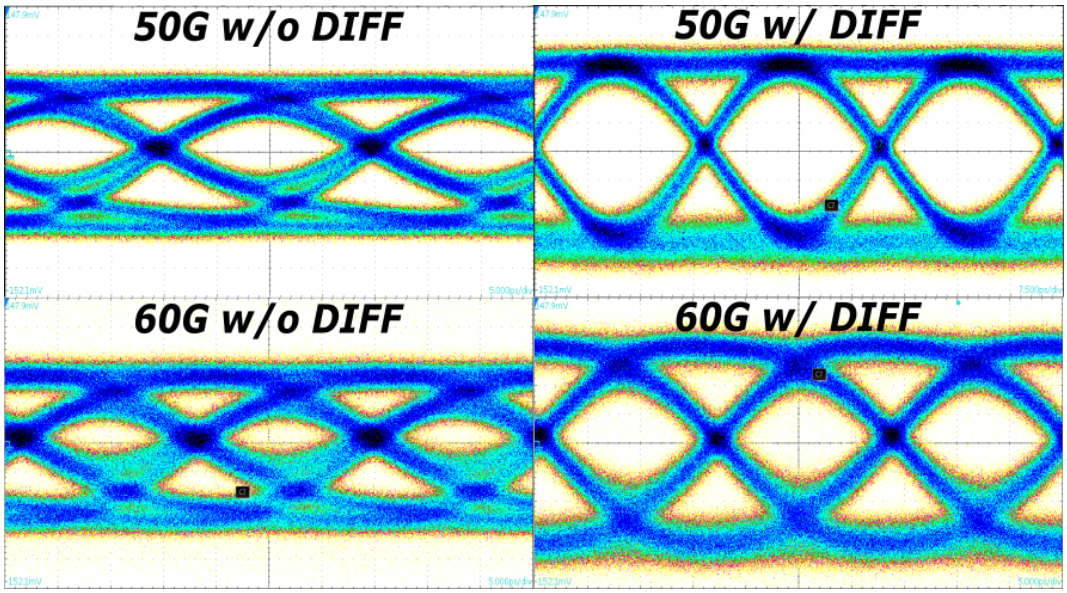


Figure 8.8: Eye diagrams at 50 and 60 Gbps with and without using the differentiator slice. These images are the result of 200 acquisitions of PRBS31 waveforms. The vertical scale on all eye diagrams is -152.1 mV to 147.9 mV.

8.4 Measurements

The VCSEL driver was fabricated on a 130-nm SiGe BiCMOS process with decoupling capacitors to ensure a wideband ac-ground for the VCSEL supply and common-mode input voltage which is set off-chip for tuning. The chip was wirebonded to a PCB with surface mount 65 GHz mini-SMP connectors, and 1.2 nF wirebond capacitor. Fig. 8.6 demonstrates that the wirebond lengths along high-frequency paths and ac-ground nodes were kept at short lengths (less than 350 microns) to minimize inductive ringing and bandwidth throttling. Since all measurements carried out were in time-domain settings (i.e. eye diagrams and bit error rate tests), no de-embedding of packaging and cable interfacing was carried out.

8.4.1 Electrical Characterization

The initial time-domain characterization of the VCSEL driver was carried out in a probed setup with 67 GHz probes at the input and 40 GHz probes at the output. A bit pattern generator (BPG) (SHF 12105A) is synchronized with an SHF synthesized clock generator (SHF 78212A) was used to provide a single-ended input voltage of 300-400 mV at low data rates (40 Gbps and below) and up to 450-500 mV for higher data rates 50+ Gbps to obtain error-free measurements. From the SHF BPG, SHF DC blocking capacitors (SHF DCB-65R-A) with a cutoff frequency of 30 kHz were used between the SHF BPG and the driver input as well as the driver output to a Tektronix digital serial analyzer sampling oscilloscope (DSA8300) through a sampling module (Tektronix 80E11) with a 2 meter extender (Tektronix 80X02).

The VCSEL driver exhibits open eye diagrams when the differentiator slice is turned on at backed off common-mode input voltage settings (2.7 V) in which it provides peaking in conjunction with the main driver slices. Fig. 8.8 demonstrates the increased eye opening at 50 Gbps and 60 Gbps. The eye diagrams on the left of Fig. 8.8 are the result of 16 mA of current sourced to the main slices while the eye diagrams on the right are the result of 8 mA of current sourced to the main slices and 16 mA of current sourced to the differentiator slice. This means that the effective cost of using the differentiator slice for equalization is 8 mA to a 3.6 V supply for a total of 28.8 mW or 0.58 pJ/bit for 50 Gbps operation and 0.48 pJ/bit for 60 Gbps operation.

For bit error rate (BER) measurements, a highly reproducible setup was necessary. A test board was assembled with 65 GHz mini-SMP connectors. Short 12 inch V-band-to-mini-SMP cables were used between the BPG and test board, and the error analyzer (EA) and the test board to maintain bandwidth in the BER measurement setup. The

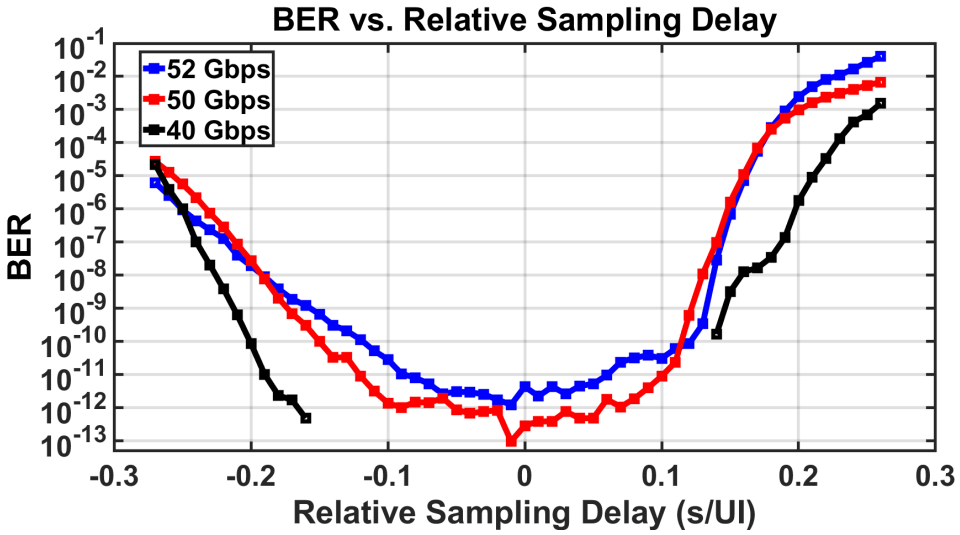


Figure 8.9: Bit error rate bathtub curves for 40 Gbps, 50 Gbps, and 52 Gbps.

BER measurements were configured to run a duration so that a confidence-level above 95% for a minimum of 5 errors at the target error rate of 10^{-12} is acquired. The measured BER bathtub curves for data rates of 40 Gbps, 50 Gbps, and 52 Gbps are demonstrated in Fig. 8.9.

A summary of performance of this work versus the state-of-the-art in high-speed VCSEL drivers is shown in Table 7.1. Notably, the energy efficiency is better than prior reported results above 50 Gb/s.

8.4.2 Optical Characterization

The VCSEL driver was evaluated with an OptiGOT 7 μm aperture device for optical measurements. A Picometrix 25 GHz 850 nm photodetector was used to evaluate the eye diagrams of the VCSEL driver.

8.5 Conclusions

This work demonstrates an error-free 52-Gbps NRZ modulated VCSEL driver in 130-nm SiGe with energy efficiency of 2.85 pJ/bit. Measurements demonstrate operation up to 60 Gbps in a bandwidth-limited setup indicating potential for energy-efficient sub-3 pJ/bit 50+ Gbps VCSEL links.

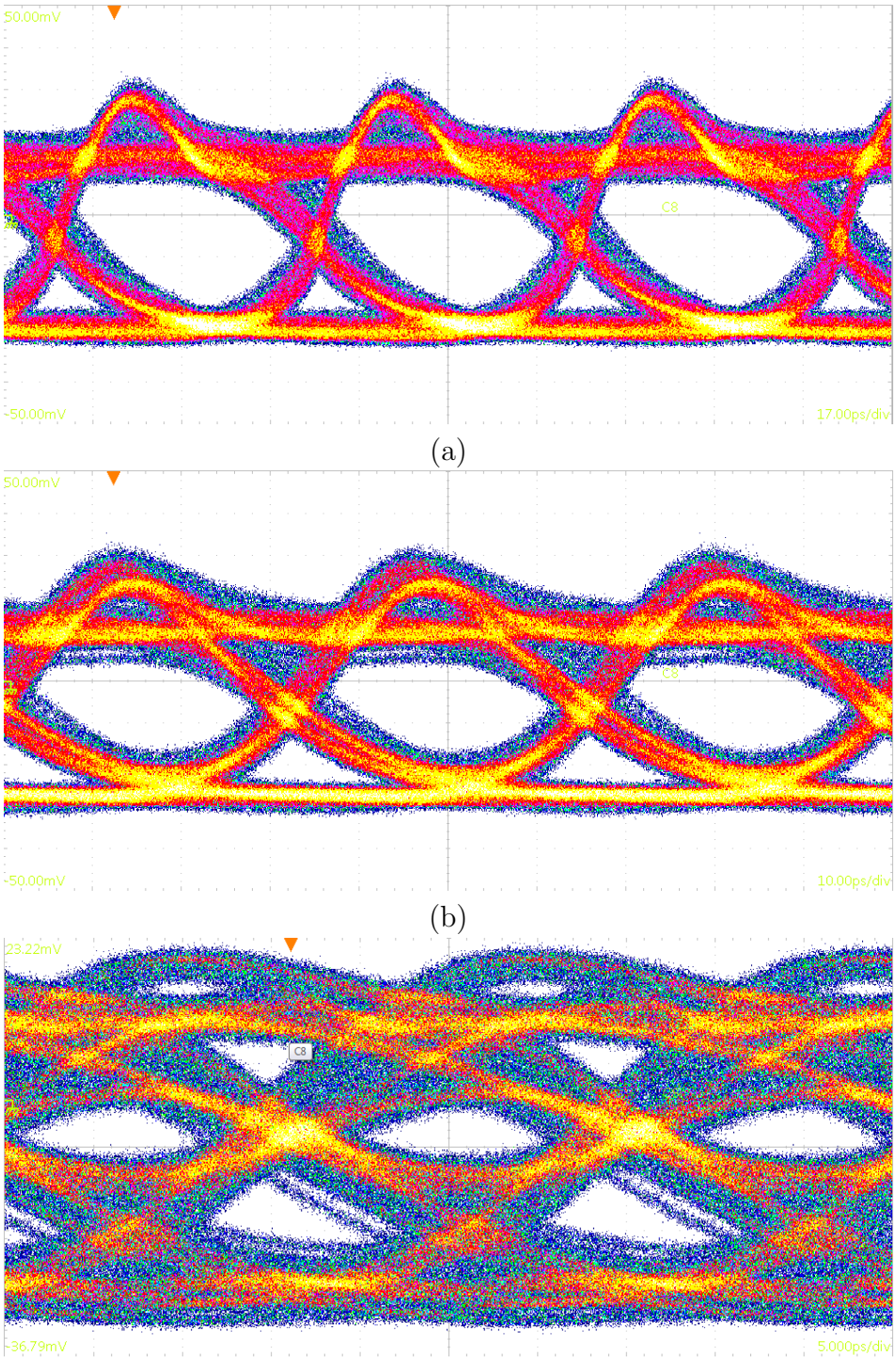


Figure 8.10: Measured optical eye diagrams from VCSEL driver assembly with OptiGOT 7 μm aperture device and Picometrix 25 GHz 850 nm photodetector at (a) 20 Gbps, (b) 30 Gbps, and (c) 52 Gbps.

Chapter 9

Conclusions to Part II

Chapters 8 and 7 have demonstrated record bit rates at their respective energy efficiencies vs. the state-of-the-art in both VCSEL-based optical transmitters and MZM-based transmitters, respectively, by leveraging low-power implementations of two-tap FFEs at the output driver stage. Chapter 8 explored a delay-less, differentiator-based 2-tap FFE implementation while Chapter 7 explored a pseudo-differential, artificial transmission line-based implementation of a conventional 2-tap FFE.

9.1 Future Work and Investigation

The design of the driver circuit in Chapter 7 can be leveraged as a building block to build a coherent optical transmitter using a nested Mach-Zehnder modulator in hybrid assemblies or monolithic assemblies above 50 GBaud. Recent technology trends point to monolithically integrated electronic-photonic front-ends such as the integrated 45-nm silicon photonics platform by Globalfoundries [75]. These technology platforms greatly reduce the assembly and wirebond parasitics at the driver-modulator interface that have been a source of significant bandwidth degradation.

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