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Investigating the growth, structural, and electrical properties of III-V semiconductor nanopillars for the next-generation electronic and optoelectronic devices

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Investigating the growth, structural and electrical properties of III-V semiconductor nanopillars for the next-generation electronic and optoelectronic devices

A dissertation submitted in partial satisfaction of the requirements for the degree of Doctor of Philosophy in Electrical Engineering

by

Andrew Lin

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ABSTRACT OF THE DISSERTATION

Investigating the growth, structural and electrical properties of III-V semiconductor nanopillars for the next-generation electronic and optoelectronic devices

by

Andrew Lin

Doctor of Philosophy in Electrical Engineering

University of California, Los Angeles, 2015

Professor Diana L. Huffaker, Chair

Extensive research efforts have been devoted to the study and development of III-V compound semiconductor nanowires (NWs) and nanopillars (NPs) because of their unique physical properties and ability to form high quality, highly lattice-mismatched axial and radial heterostructures. These advantages lead to precise nano-bandgap engineering to achieve new device functionalities. One unique and powerful approach to realize these NPs is by catalyst-free, selective-area epitaxy (SAE) via metal-organic chemical vapor deposition, in which the NP location and diameter can be precisely controlled lithographically. Early demonstrations of electronic and optoelectronic devices based on these NPs, however, are often inferior compared to their planar counterparts due to a few factors: (1) interface/surface states, (2) inaccurate doping calibration, and (3) increased carrier scattering and trapping from stacking fault formation in the NPs. In this study, the detailed growth mechanisms of different III-As, III-Sb and III-P NPs and their heterostructures are investigated. These NPs are then fabricated into

single-NP field-effect transistors (FETs) to probe their electrical properties. It is shown that these devices are highly diameter-dependent, mainly because of the effects of surface states. By growing a high band-gap shell around the NP cores to passivate the surface, the device performance can be significantly improved. Further fabrication and characterization of vertical surround-gate FETs using a high-mobility InAs/InP NP channel is also discussed. Aside from the radial NP heterostructures, different approaches to achieve purely axial heterostructures in InAs/In(As)P materials are also presented with excellent interface quality. Both single barrier and double barrier structures are realized and fabricated into devices that show carrier transport characteristics over a barrier and even resonant tunneling behavior. Antimonide-based NPs are also studied for their immense application in high-speed electronics and mid-IR optoelectronics. Different growth regimes are probed to achieve InSb NPs and InAsSb NPs.

This dissertation of Andrew Lin is approved.

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Symbols and Acronyms

1D	One-dimensional	I_{DS}	Drain-source current
NW	Nanowire	V_{DS}	Drain-source voltage
NP	Nanopillar	g_m	Transconductance
FET	Field-effect transistor	C_g	Gate capacitance
MOS	Metal-oxide-semiconductor	WZ	Wurtzite
CMOS	Complementary MOS	E_F	Fermi-level
VLS	Vapor-liquid-solid	E_i	Intrinsic Fermi-level
SAE	Selective-area epitaxy	N_A	Acceptor level
CVD	Chemical vapor deposition	N_D	Donor level
MOCVD	Metal-organic CVD	ψ_0	Electrostatic potential
MBE	Molecular beam epitaxy	q	Electron charge
SEM	Scanning electron microscopy	ε_0	Free space permittivity
TEM	Transmission electron microscopy	ε_s	Relative permittivity of SiO_x
STEM	Scanning TEM	k	Boltzmann constant
FIB	Focused ion beam	μ	Carrier mobility
d_{elec}	Effective electronic diameter	d_{dep}	Critical diameter
N_{SS}	Surface states density	ZB	Zine-blende
R_N	Normalized resistance	μ_{eff}	Effective carrier mobility
TMGa	Trimethylgallium	TMIn	Trimethylindium
TBA	tertiarybutylarsine	TBP	Tertiarybutylphosphine
DEZn	diethylzinc	V_g	Gate bias (voltage)
HEMT	High-electron mobility transistor	RT	Room temperature

SS	Subthreshold slope	g^*	Electron magnetic moment
I_{ON}	Transistor on current	eV	Electron volt
I_{OFF}	Transistor off current	Å	Angstrom
ρ	Resistivity	DFT	Density-function theory
Ω	Ohms	TMSb	trimethylantimony
ALD	Atomic layer deposition	FFT	Fast Fourier transform
QW	Quantum well	PBE	Perdew-Burke-Ernzerhof
QD	Quantum dot	Z	Atomic number
QCL	Quantum cascade laser	γ	Surface energy
T	Temperature	ΔH	Enthalpy
TBCl	Tertiarybutylchloride	μ_{sb}	Antimony chemical potential
μ_e	Electron mobility	TDMASb	trisdimethylaminoantimony
μ_h	Hole mobility	IR	Infrared
FTIR	Fourier transform IR spectrometer	MCTA	Mercury cadmium telluride
EDS	Energy-dispersive spectroscopy	LN_2	Liquid nitrogen
BCB	Benzocyclobutene	TMAl	Trimethylaluminium
IV	Current-voltage		

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This had not been the smoothest journey, but I had the good fortune to meet some of the most incredible people who contributed significantly to the completion of this dissertation and helped me grow both personally and professionally. I would like to express my deepest gratitude to my advisor and committee chair Professor Diana L. Huffaker. Her immeasurable support and guidance helped me stay afloat during my graduate studies and provided me invaluable research directions. Diana's rigorous work ethic and her self-criticalness showed me the qualities of a successful researcher and scientist, which led to the scientific and personal achievements accompanying the completion of this work, including conference presentations, publications in peer-reviewed journals, and patent filing.

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Chapter 1

Introduction

1.1 Overview

Ever since the first reports of epitaxial semiconductor nanowires in the 1960s[1] and further development in the early 1990s[2,3], research in the field of nanowire has exploded in the scientific community. Nanowires are one-dimensional nanostructures with diameters on the order of tens or hundreds of nanometers with high aspect ratio. At this dimension, quantum mechanical and surface effects play an important role on determining the materials properties, hence enabling promising and new device functionalities and making these nanowires an ideal vehicle to study low-dimensional physics and optics. In recent years, the progress in semiconductor nanowire synthesis has led to novel growth techniques and structures such as nanowire heteroepitaxy[4,5] and different heterostructures[6,7]. In addition, the advancements accomplished in materials characterization and device fabrication have resulted in new types of optoelectronic[8,9] and electronic[10,11,12] devices.

The most conventional approach to realize semiconductor nanowires is by a technique called the vapor-liquid-solid (VLS) growth[1,13]. In this method, nanometer-sized metallic (usually gold) droplets are deposited on the growth substrate followed by subsequent nanowire synthesis using either metal-organic chemical vapor deposition (MOCVD)[14,15] or molecular-beam epitaxy (MBE)[16,17]. This growth depends on the supersaturation of the introduced source molecules

(vapor) inside the molten metallic droplets (liquid) to form crystalline semiconductor materials (solid) at the droplet/semiconductor interface. While this approach can successfully produce nanowires with very small diameters (~10s of nm) and heterostrucutres with sharp interfaces, there are a few drawbacks inherent to such technique. First, unless a patterned approach is used to distribute the metallic droplets, they are usually randomly located on the substrate surface, which lead to nonuniform nanowire length and diameter with no position control. Second, nanowires synthesized using Au catalysts can lead to Au atom incorporation inside of the nanowire[18,19], which is known to create trap centers in semiconductor materials.

Nanopillars (NPs) are one type of nanowire that consist of lithographically predefined positions and diameters, grown by selective-area epitaxy (SAE) without any catalysts. In this technique, the growth substrates are patterned with a lithographically defined mask that determines where the growth occurs (see the illustration in Fig. 1.1).

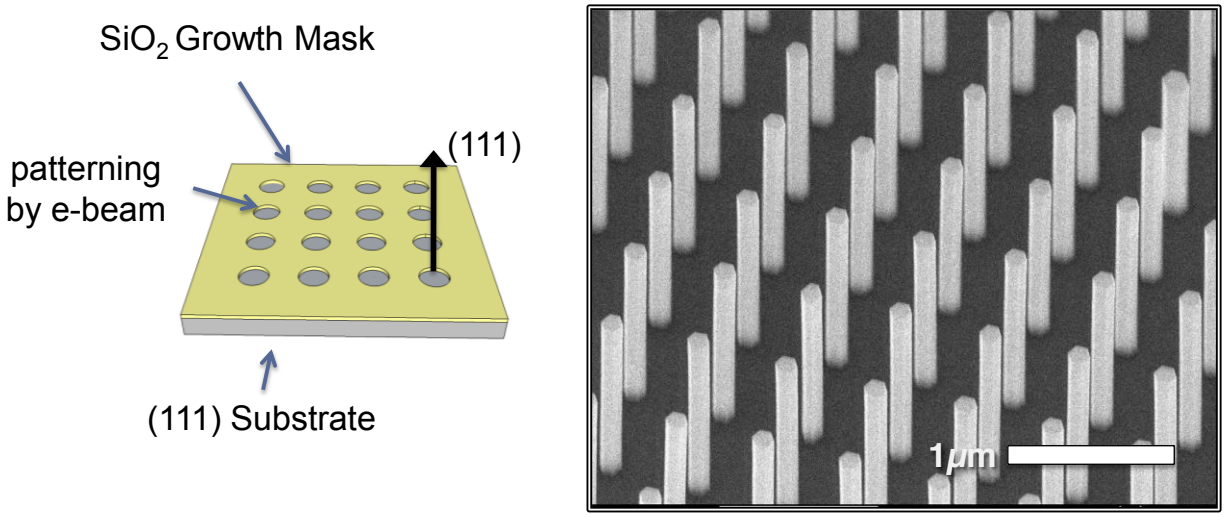

Figure 1.1: An illustration of the patterned growth substrate used in SAE and a SEM micrograph showing the resulting highly-ordered uniform array of NPs.

Unlike VLS growth, NP synthesis in SAE is initiated based on the adatom diffusion and surface energetics of the system. In most III-V semiconductor materials, the {111} surfaces usually have the highest surface energy whereas the {110} surfaces are the energetically favorable. As a result, given enough thermal energy, the adatoms diffuse to the exposed semiconductor surface to minimize the {111} surfaces while maximizing the favorable {110} surfaces. This leads to axial, hexagonal NP formation in the <111> crystal direction with six long {110} sidewalls. In SAE, the NP diameter, length, and location can be precisely controlled and engineered by the mask design. Such controllability has led to the successful demonstration of several novel NP optoelectronic devices made possible only through this technique[20,21].

Recent development in nanowire growth has enabled highly lattice-mismatched heteroepitaxy with excellent crystal integrity, which is very difficult to attain in conventional planar epitaxial techniques. This has opened a window for high-quality heterogeneous integration of highly-dissimilar materials, such as III-V semiconductors and Si[10,22], which can potentially leads to a new generation of high-performance III-V devices integrated with the current Si complementary metal oxide semiconductor (CMOS) technology.

Band-gap engineering and heterostructure formation in nanowires have also been extensively explored for their potential to further advance device functionalities. Two types of heterostructures can be generalized: axial and radial heterostructures. In axial heterostrucutres, the materials change along the growth direction whereas in radial heterostructures, the change occur in the radial direction. Both types are depicted in Fig. 1.2. Oftentimes, multiple heterostructures or a mixture of both types heterostructures are used simultaneously.

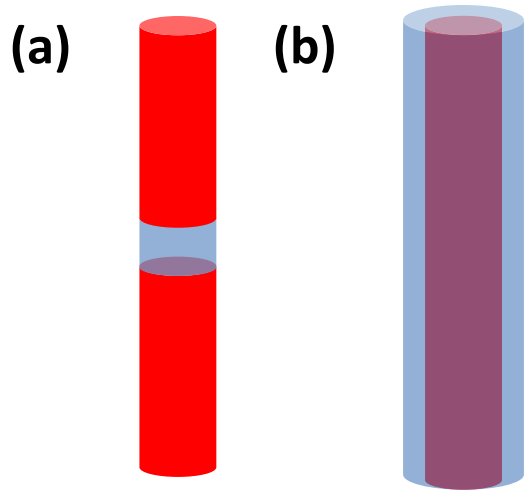

Figure 1.2: Schematics of (a) axial nanowire heterostructure and (b) radial nanowire heterostructure. Different colors represent different materials.

While successful demonstrations based on VLS nanowires have been reported to show quantum structures with abrupt interfaces[12,23], the same demonstration in SAE NPs has been elusive. This difficulty is posted by the nature of SAE because of the sensitivity of growth direction and materials incorporation based on local environment, such as temperature, different exposed surfaces and local atomic arrangements[24,25].

In the past 50 years, the world's technological advancement has been driven by the miniaturization of semiconductor devices, as predicted by the Moore's law. The continued scaling down in Si CMOS transistors, however, is facing a serious obstacle as the dimension approaches the fundamental physics limits. As the channel length shrinks, the leakage current unavoidably increases, which leads to high power consumption[26,27]. The constraints in energy dissipation have led another line of research direction in seek of a new types of channel material with low power consumption (i.e. large on/off ratio at low supply voltage < 0.5V). III-V semiconductor nanowires have been proposed as potential building blocks for future analog and digital devices[28,29]. Having much higher carrier mobility than Si, III-V channels can lead the

lower supply voltage and power consumption without sacrificing the performance. The inherent geometry of nanowire growth also allows for a surround-gate design with improved gate control and mitigated short-channel effects. Using a junction-less channel also helps avoid the increased leakage current caused by band-to-band tunneling current and drain and gate induced barrier lowering phenomena.

1.2 Surface states in semiconductors

With all the promising advantages of these semiconductor nanowires mentioned in the previous section, the development of the state-of-the-art, benchmark-setting devices has been significantly hampered by one factor - surface states. These states are created by the dangling bonds due to the termination of perfectly periodic crystal arrangement at the semiconductor surface. There exists a neutral level in the surface states. The states are acceptor type above this neutral level and donor type below it. In the case of a typical n-type semiconductor where the fermi level resides close to the conduction band, the mobile electrons will diffuse into the acceptor surface states, leaving behind immobile positive space charges and creating a depletion region near the surface[30]. When the dimension of the semiconductor approaches depletion region, as in the case of nanowires, the surface states effects can be prominent or even dominant in determining the optical and transport properties. A large portion of this dissertation is devoted to studying the effects of surface states on the transport properties and finding a robust scheme to effectively passivate the surface.

1.3 Organization

This dissertation is consisted of six chapters. The first chapter gives an overview of the background and motivation of which the work discussed here is built upon. Chapter 2 describes, in details, the investigation of GaAs NP growth and transport, in which a semi-empirical model is proposed to extract different transport parameters. Different passivation schemes are also compared. Chapter 3 starts with the growth and transport studies of InAs NPs, as studied as single NP-field effect transistors (FETs). An in-situ passivation layer is also employed to improved electrical properties. The second part of the chapter focuses on the fabrication and device characteristics of vertical surround-gate FETs based on the passivated InAs NP channels. In Chapter 4, different approaches to achieve purely-axial InAs/InP heterostructure with abrupt interface are discussed. First, a two-temperature growth technique is used to realize a single-barrier heterostructure and a double barrier tunneling structure. Then, another technique utilizing an in-situ chloride etching is presented to accomplish the same heterostructures without any temperature change or growth interruption. Chapter 5 shifts gears from heterostructure formation to the study and growth of antimonide (Sb) based NP materials, including direct InSb nanostructure formation and InAsSb NPs. Finally, the last chapter summarizes the important findings of this dissertation work and gives light to some potential future research directions.

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Chapter 2

GaAs nanopillars

2.1 Overview

In recent years, GaAs semiconductor nanowires (NWs) and nanopillars (NPs) based have been studied extensively for their potential to serve as the foundations as next-generation optoelectronics and electronics because of the direct band-gap and much higher mobility compared to Si. With the growing maturity in growth and device fabrication, different optoelectronic[1,2,3] and electronic devices[4,5] have been demonstrated. The device performance, however, is often degraded compared to conventional bulk structures due to two primary factors: interface/surface states[3,4] and inaccurate doping calibration[6]. In general, surface states can pin the Fermi-level, hence creating a depletion region to reduce the effective electronic diameter (d_{elec})[7,8] and act as recombination centers[9]. These effects become more detrimental in NP devices because of the large surface-to-volume ratio. Several studies have been reported on the influence of surface states and surface state density (N_{SS}) in Si nanostructures[10,11]. Similar studies in GaAs NPs, including effects of surface passivation, however, are still lacking. Accurate doping calibration has also been problematic since doping level measurement in NPs still proves to be difficult and common dopant incorporation is growth plane dependent[12]. Some studies have been reported to calculate doping levels based on electrical measurements but their

models assume a constant bulk-like mobility[13,14]: mobility is reported to be size dependent for NPs[15,16].

In this chapter, the transport properties, namely normalized resistance (R_N) and mobility of p-type GaAs nanopillars (NPs) from electrical measurement on the single NP FETs of varying diameter are investigated. Resulting data are fit to a model based on diameter dependent mobility to extract the doping level and N_{SS}. The impact of surface passivation by comparing the effects of in-situ and ex-situ passivation techniques on the transport properties is also discussed.

2.2 Growth of GaAs nanopillars

Vertical p-type GaAs NPs are grown on GaAs (111)B patterned substrate by catalyst-free, selective-area epitaxy (SAE) using a low-pressure (60 torr) vertical Emcore metal-organic chemical vapor deposition (MOCVD) reactor with trimethylgallium (TMGa) and tertiarybutylarsine (TBA) for the GaAs NP formation along with diethylzinc (DEZn) for p-type doping. The growth substrate is patterned with a SiO_2 mask (20-nm thick) using e-beam lithography followed by reactive-ion etching. The processed nanoholes have varying diameters, resulting in NP formation with dimensions ranging from 50 to 200 nm (± 5 nm) all on the same mask. The ability to lithographically control the NP diameter and position is a critical advantage of SAE over conventional vapor-liquid-solid (VLS) NP growth and enables the careful study presented here. The entire process is completed at a growth temperature of 715 ˚C with a V/III ratio of 9. Two samples with different intended doping levels: $N_A = 5 \times 10^{15}$ cm^{-3} (Sample A) and 5×10^{17} cm^{-3} (Sample B) are grown in order to compare the accuracy of our estimation. The intended doping levels are calibrated by planar growth on GaAs (100) substrate, measured by Hall measurement. In SAE, the growth rate depends on the nanohole size[17], leading to the

possibility of slightly different doping levels in NPs with different diameters. However, for the purpose of this study, such phenomenon is likely insignificant and can therefore be neglected. In-situ passivation is accomplished by growing a 5 nm InGaP shell to cover GaAs NP. Ex-situ passivation is done by immersing the samples into ammonium sulfide for 90 minutes at room temperature, a technique that has been proven experimentally[18,19] and theoretically[20] to reduce N_{SS} in III-V semiconductors.

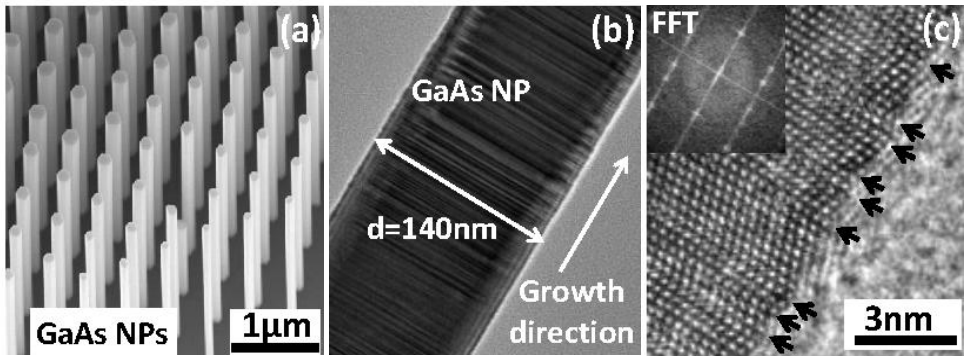

Figure 2.1: (a) Tilted SEM image of an array of p-type GaAs NPs grown on patterned (111)B GaAs substrate by MOCVD. (b) TEM image of a GaAs NP segment (d = 140 nm). (c) High-resolution TEM image of GaAs NP showing the transition between wurtzite and zinc blende structure; the inset shows the FFT of this segment with the characteristic streaking resulted from twinning.

Figure 2.1a shows the tilted scanning electron microscope (SEM) image of an array of the as-grown hexagonal GaAs NPs with heights from 4 – 5 µm and diameters from 50 – 200 nm. Figure 2.1b shows a transmission electron microscope (TEM) image of a typical p-type GaAs NP (d = 140 nm) with high-density of rotational twins or phase transition from wurtzite (WZ) to zinc-blende (ZB). The stacking faults are marked by the arrows in the high-resolution TEM image in Fig. 2.1c.

2.3 Electrical measurement of single GaAs nanopillar FETs

For single NP analysis, the NPs are moved mechanically onto a degenerately doped Si substrate covered with 300 nm of SiO_2 with Ti/Au back gate metal. Top contacts are written by e-beam lithography, using a converted JEOL SEM, followed by metal deposition of Ti (20 nm)/Au (100 nm) and liftoff as illustrated in inset of Fig. 2.2. The NPs are well preserved after fabrication as the hexagonal feature is clearly visible in the tilted SEM image of Fig. 2.2. The devices are characterized using Agilent 4156C semiconductor parameter analyzer at room temperature without any light illumination. Each device is measured several times and the average I-V characteristics are recorded for more accurate results.

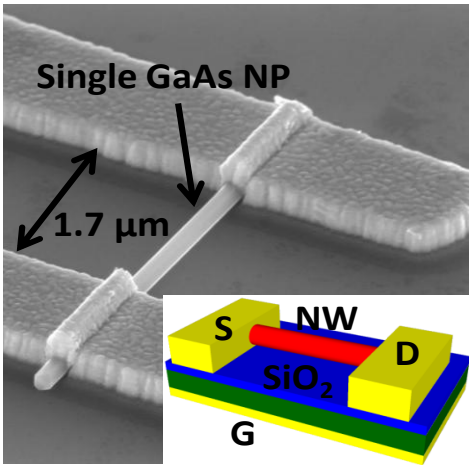

Figure 2.2: SEM image of a single-NP FET fabricated by e-beam lithography followed by metal evaporation and liftoff. Inset shows the corresponding schematic.

Figure 2.3a shows the I_{DS}-V_{DS} curves in the linear region at zero gate bias from four Sample B single-NP FETs with diameters of 89 nm, 101 nm, 110 nm and 126 nm, all from the same growth. The linear I_{DS}-V_{DS} characteristics indicate good ohmic drain and source contacts. The measured current of larger NW (d = 126 nm) is almost three orders of magnitude higher than

that of smaller NW (d = 89 nm) at the same bias level. The highly diameter-dependent I-V characteristics can be attributed to the radial surface depletion caused by surface states. From such I-V characteristics, resistance of the measured NPs can be extracted. Devices from Sample A (not shown) also show similar trends. Source-drain characteristics for the 126 nm diameter FET are plotted in Fig. 2.3b with gate biases ranging from -2 V to 2 V. The gate response clearly demonstrates p-type depletion mode behavior as I_{DS} is nonzero with 0 V gate bias and increases with more negative gate bias[21]. From the measured data, the field-effect hole mobility can be extracted using[22]:

$$g_m = \frac{d|I_{DS}|}{dV_{GS}} = \frac{\mu_{eff} C_g V_{DS}}{L^2} \qquad (2.1)$$

$$C_g \cong \frac{2\pi\varepsilon_r\varepsilon_0 L}{\ln(\frac{2h}{r})} \qquad (2.2)$$

In Eqn 2.1, g_m is the transconductance, V_{DS} the applied drain-source voltage, L the channel length and C_g the gate capacitance, which can be calculated based on the back-gate geometry and known oxide thickness, as shown in Eqn. 2.2, where L is the channel length, h the oxide thickness, r the NP radius, and ε the permittivity of the oxide.

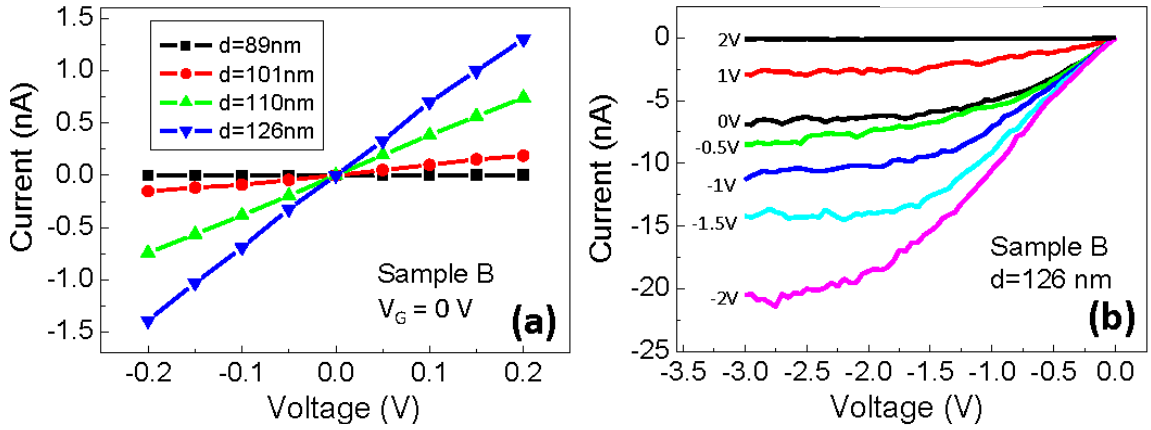

Figure 2.3: (a) I_{DS} –V_{DS} curves from four p-type GaAs NP FETs in the linear region with diameters of 89 nm, 101 nm, 110 nm and 126 nm, measured at zero gate bias (Sample B). (b) I_{DS} versus V_{DS} for a typical single-NP FET with different gate biases (d = 126 nm).

The mobility on more than thirty unpassivated (■), ex-situ passivated (★) and in-situ passivated (▲) devices from Sample A and Sample B, is measured and plotted in Fig. 2.4a and 2.4b, respectively. The dotted lines represent the empirical fitting to mobility. For Sample A, the field-effect hole mobility stays fairly constant at 0.5 cm^2/V-s and decreases rapidly below d = 162 nm. For Sample B, the mobility is constant around 0.36 cm^2/V-s then drops below d = 125 nm. The significant drop indicates that surface dominated scattering plays an important role in limiting the mobility below a certain diameter and hence the transport properties are affected accordingly. After either ex-situ chemical passivation or in-situ InGaP passivation, mobility for both Sample A and Sample B becomes insensitive to NP dimensions as it is significantly improved for smaller devices while larger ones remain unchanged. Both passivation techniques show very similar results. However, devices passivated by ammonium sulfide tend to degrade after several measurements whereas devices with InGaP shell stay passivated and do not degrade, proving that InGaP shell is a robust technique for passivating GaAs NPs. The increase in

extracted field-effect hole mobility after passivation can be attributed to two factors: an increase in drift mobility due to the reduction in surface scattering and an enhanced gate control of the channel.

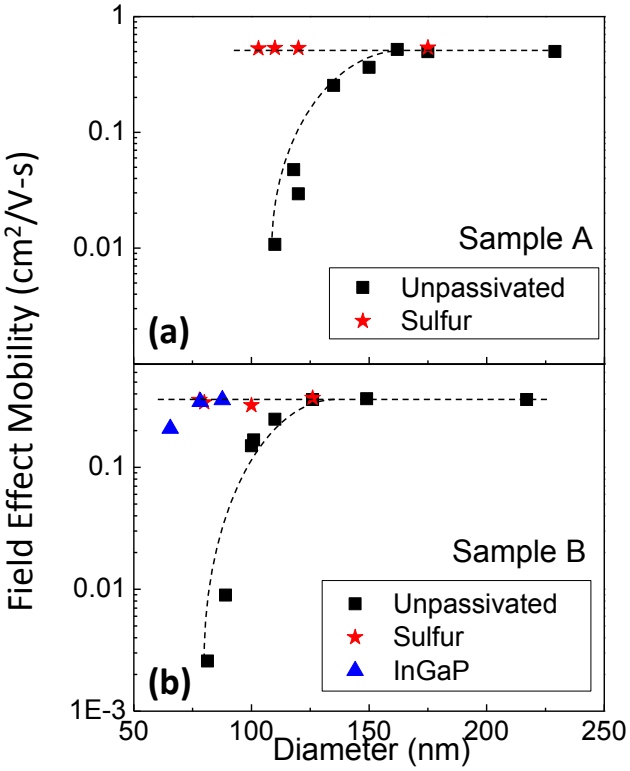

Figure 2.3: Measured field effect mobility versus NP diameter from (a) Sample A and (b) Sample before and after ex-situ chemical passivation by ammonium sulfide or in-situ InGaP passivation.

Even after surface passivation, the measured mobility is not comparable to bulk p-type GaAs mobility, likely due to high twinning density in GaAs NPs, as seen in Fig. 2.1c. Different energies between ZB and WZ phases[23] result in potential barriers in the valence band for the holes and can increase the scattering event significantly leading to reduction in mobility. It is also note that the mobility is slightly higher in Sample A than Sample B, due to higher doping in Sample B from our original growth design.

2.4 Transport modeling of GaAs nanopillars

Based on the transport measurements, a model can be established to extract important transport parameters in p-GaAs NPs. In Figure 2.5, normalized resistance (R_N) from both Sample A (■) and Sample B (★) is plotted, showing an increase over orders of magnitude in R_N as NW diameter reduces. The solid and dotted lines represent the theoretical modeling corresponding to different doping levels.

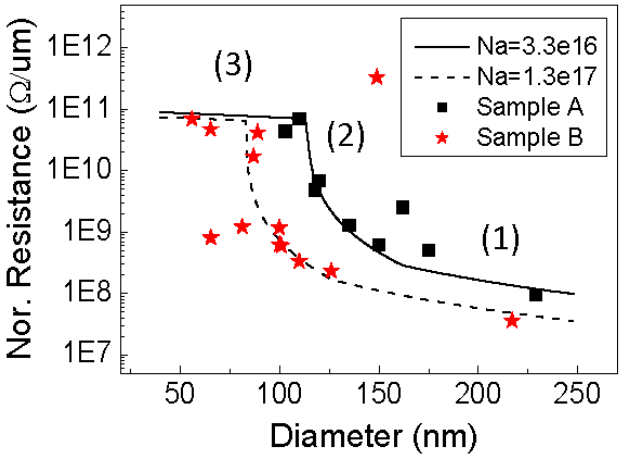

Figure 2.4: Measured NP normalized resistance over various diameters for the samples A and B (dots) and the calculated resistance with different doping levels (solid and dash lines) and a fixed surface states density of N_{SS} = 5 × 10^{12} $cm^{-2}eV^{-1}$.

The modeling is accomplished by first calculating the size of effective electronic diameter (d_{elec}), which is simply the NP diameter minus surface depletion. The effective electronic diameter, governed by NP doping levels and N_{SS}, is calculated utilizing a model based on the Boltzmann approximation assuming an abrupt junction between depletion and conducting region, and boundary conditions for Poisson equation that surface Fermi-level is pinned very close to midgap ($E_F = E_i$)[10,11]:

$$d_{elec} = 2\times\sqrt{\left(\frac{d}{2}\right)^2 - \frac{2(d/2)q^2 N_{SS}\psi_0}{q(N_A - N_D)\left(1+\frac{q^2(d/2)}{2\varepsilon_0\varepsilon_S}N_{SS}\right)}} \qquad (2.3)$$

In Eqn. 2.3, d is the actual NP diameter, N_A and N_D the acceptor and donor levels, ψ_0 the electrostatic potential at the non-depleted NP region, which can be calculated from Eqn. 2.4[10].

$$\psi_0 = \frac{kT}{q}\left[\frac{N_A - N_D}{2p_0}\left(1+\left(1-\frac{2p_0 n_0}{(N_A - N_D)^2}\right)^{1/2}\right)\right] \qquad (2.4)$$

Now, knowing d_{elec}, R_N can be calculated from Eqn. 2.5, established for a perfect cylindrical symmetry. This is not an exact match to our hexagonal NP geometry, but it provides a close approximation.

$$R_N = \frac{1}{qN_A\times\mu}\times\frac{L}{\pi(d_{elec}/2)^2} \qquad (2.5)$$

In the above equation, L is the drain-source spacing (normalized to 1 μm), and μ the hole mobility. Previously, similar models developed to predict transport parameters in NPs have assumed constant bulk mobility but mobility is indeed highly sensitive to NP size. For more accuracy, a model based on the extracted empirical formulae from measured field-effect hole mobility as a function of NP diameter for Sample A and Sample B, independently is applied to Eqn. 2.5. This approximation is likely a slight underestimation for unpassivated NPs because the surface states can also affect the effective gate capacitance. Therefore, the approximated drift mobility marks the lower boundary of the true hole mobility in the GaAs NP FET channels. The empirical relations for Sample A are $\mu = 0.5$ cm^2/V-s for d > 162 nm and μ [cm^2/V-s] = 0.0098d [nm] - 1.0951 for 115 nm < d < 162 nm. For Sample B, the relations are $\mu = 0.36$ cm^2/V-s for d > 126 nm and μ [cm^2/Vs] = 0.0093d [nm] - 0.7787 for 85 nm < d < 126 nm. In this model, the only remaining independent variables are N_{SS} and doping levels. By assuming a common N_{SS}

for Sample A and Sample B before passivation and performing an iterative fitting to the experimental data, N_{SS} and doping levels can be accurately extracted. The best fit N_{SS} for both samples is $N_{SS} = 5 \times 10^{12}$ $cm^{-2}eV^{-1}$, a value comparable to reported bulk GaAs surfaces[24].

The best fit doping levels for Sample A and Sample B are 3.3×10^{16} cm^{-3} and 1.3×10^{17} cm^{-3}, respectively. For Sample A, actual doping level is almost an order of magnitude higher than intended doping level based on planar calibration. For Sample B, it is slightly lower than that of the intended 5×10^{17} cm^{-3}. The disagreement between the intended and extracted actually doping levels is expected because growth mechanism and doping incorporation differ between the SAE NP and planar growths. Adatom diffusion and binding energy play a much more prominent role in NW epitaxy than in planar growth[25]. Planar doping sample is based on GaAs (100) substrate whereas NW grows in the (111) direction. The different binding energies of these planes may cause dopant incorporation to deviate.

The passivation effects on R_N and N_{SS} are also investigated. The ex-situ (★) and in-situ (▲) passivation results are plotted alongside the unpassivated data (■) in Fig. 2.6a for Sample A and Fig. 2.6b for Sample B. For both samples, R_N is reduced considerably after passivation. For a device from Sample A (d = 103 nm), R_N decreases from ~ 5×10^{10} Ω/μm to ~ 5×10^{8} Ω/μm. Again, the two passivaiton techniques yield similar results.

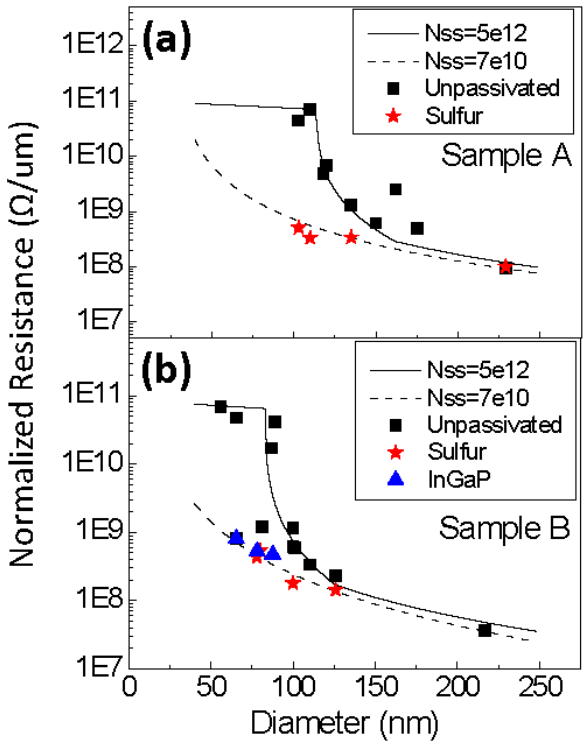

Figure 2.6: Measured normalized resistance of Sample A (a) and Sample B (b) before and after passivation (dots) and calculated resistance (lines) with fixed doping levels of 3.3×10^{16} cm^{-3} (a) and 1.3×10^{17} cm^{-3} (b) and varying N_{SS}.

The same model described in previous section is employed utilizing empirical fitting of passivated mobility from Fig. 2.4. The best-fit doping levels from unpassivated data are kept constant and only N_{SS} is varied to find N_{SS} after passviation. In the case of both samples, N_{SS} is reduced from 5×10^{12} cm^{-2}eV^{-1} to 7×10^{10} cm^{-2}eV^{-1}, matching the reported N_{SS} after passivation[19].

For unpassivated devices, the model predicts a fully depleted NP ($d_{elec} = 0$) when diameter is reduced to 113 nm for Sample A and 83 nm for Sample B. This critical diameter (d_{dep}) plays an important role in NP transport characteristics as there appears, as in Fig. 2.5, to be three NP transport regimes, marked by (1), (2) and (3).

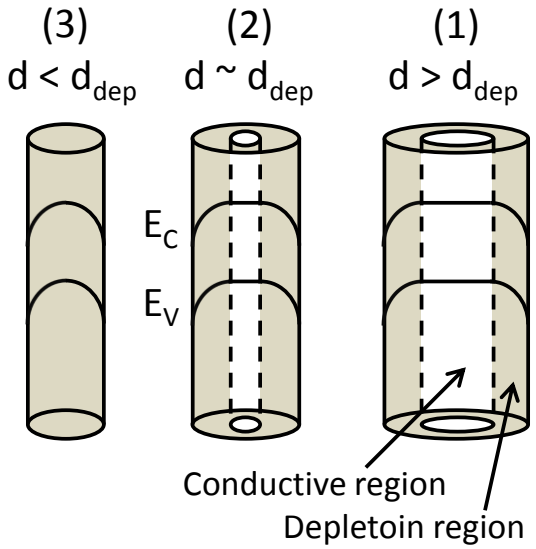

Figure 2.7: Schematics of p-type GaAs nanopillar band diagram showing the conductive region in the nanopillar core and the depletion region from surface states. Different regimes of nanopillar transport is depicted.

The different transport regimes are explained by the illustration of energy band diagrams shown in Fig. 2.7. In the first regime, NP diameter is significantly larger than the surface depletion, making surface states effects on transport minimal ($d > d_{dep}$). In the second regime, NP diameter is only slightly larger than surface depletion ($d \sim d_{dep}$) leading to surface dominated transport and results in a rapid increase in R_N. The diameters in which above it NP transport is bulk like and below surface dominated are 160 nm and 125 nm for Sample A and Sample B, respectively. In regime three the NP becomes fully depleted ($d < d_{dep}$), the resistance becomes almost constant and flattens out with decreasing diameter. After passivation, there appears to be no surface dominated regime, indicating that the surface states effects on NP transport are suppressed. This serves as direct evidence that surface passivation can improve the transport characteristics in NPs and should be taken into considerations for future design and fabrication of NP-based devices.

2.5 Summary

In summary, the transport properties of p-type GaAs NPs are investigated in detail, by comparing their electrical characteristics over a range of diameters. It is found that both the field-effect hole mobility and normalized resistance are highly dependent on NP diameter before passivation. The mobility is much lower than bulk p-type GaAs because of the surface states and possibly the high stacking fault density in GaAs NPs. A semi-empirical model based on varying mobility has been developed to calculate actual doping levels and N_{SS} in NPs. The ability to determine the actual doping level in NP allows for better device structure optimization. Finally, ex-situ chemical surface passivation with ammonium sulfide is employed to reduce N_{SS} for over an order of magnitude and a more robust passivation technique with in-situ InGaP shell growth showing comparable results as sulfur passivaiton is also presented. The work in the chapter shows the necessity of a reliable surface passivation scheme when designing and attempting any practical optoelectronic or electronic devices based on GaAs NPs; this approach should also apply to any other III-V materials.

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Chapter 3

InAs nanopillars

3.1 Overview

InAs is another III-V semiconductor nanopillar (NP) material that has been studied extensively as potential building blocks for future analog and digital electronic devices[1,2]. It serves as one of the most promising channel materials choices for high-speed, low-power devices, having room-temperature bulk electron mobility of 22,700 cm^2/V-s and electron effective mass of 0.023 m_0. Planar InGaAs/InAlAs high electron mobility transistors (HEMTs) on InP substrates have achieved high speed operation in the THz range[3,4]. Furthermore, progress in nano-heteroepitaxy has enabled uniform III-V NP formation on Si, despite the large lattice-mismatch, opening the door for heterogeneous integration of high-performance III-V devices with currently existing Si CMOS technology[5,6,7].

Several field-effect transistors (FETs) using InAs NPs as the channel have been demonstrated but device outputs in terms of mobility, switching characteristics and high-frequency performance have been inferior to their planar counterparts[8,9,10]. Many researchers have attributed such degradations to surface effects playing a more significant role in NPs. InAs is known to have a large number of surface donor states above the conduction band edge, therefore creating a surface accumulation layer of free electrons[11,12]. In InAs NPs, this effect is greatly magnified and it is possible that most carrier transport takes place in this surface

accumulation layer[13], leading to poor channel confinement, significant surface scattering, and therefore non-ideal transfer characteristics and reduced carrier mobility.

There have been reports on improved electron mobility using an InP shell to protect the InAs NP channel using vapor-liquid-solid (VLS) growth mode[14,15]. However, a detailed study of how catalyst-free InAs NP transport characteristics change with dimension and surface passivation is still lacking. In this chapter, a thorough investigation of InAs NP growth and transport, namely the resistivity and field-effect mobility (μ_{eff}), as a function of NP diameter by studying single-NP FETs is discussed[16]. An in-situ passivation scheme using a thin InP shell and its impact on the electrical transport and transistor characteristics is also reported. Finally, this chapter concludes with the fabrication and device characterization of vertical surround-gate FETs using these InAs NPs as channel.

3.2 Growth of InAs nanopillars

Vertical InAs and radial InAs/InP NPs are grown on patterned InAs (111)B substrates by catalyst-free, selective-area epitaxy (SAE) using a low-pressure (60 torr) vertical Emcore metal-organic chemical vapor deposition (MOCVD) reactor. The precursors used are trimethylindium (TMIn), tertiarybutylarsine (TBA), and tertiarybutylphosphine (TBP). The growth substrates are patterned with a SiO_2 mask (25-nm thick) with varying nanohole diameters ranging from 50 nm to 200 nm. InAs NPs are grown at a substrate temperature of 620˚C by flowing TMIn and TBA at a V/III ratio of 10 for 10 minutes without intentional doping.

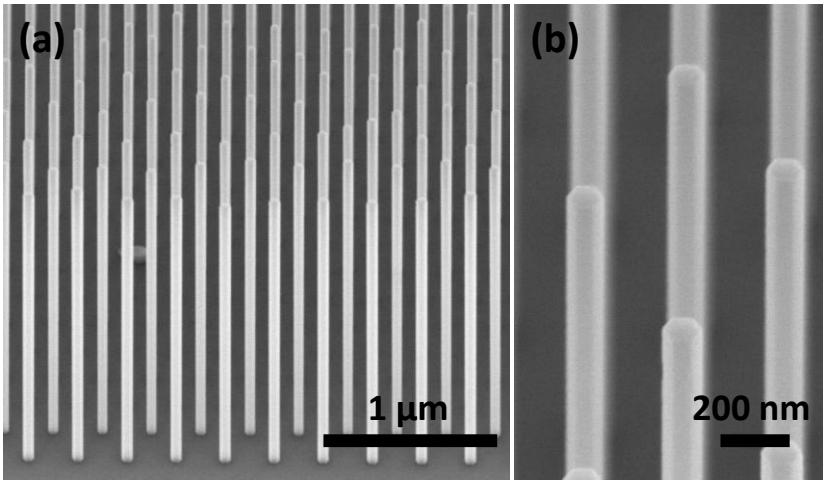

Figure 3.1: (a) SEM image of the as-grown InAs NP array. The NPs have varying height and diameter depending on the masking opening and pitch. (b) Close-up SEM image of the InAs NP array to show the hexagonal feature and the <110> sidewalls.

The as-grown InAs NPs have a much faster growth rate compared to the GaAs NPs. With a growth time of 10 minutes, the average InAs NP heights range from 4 - 6 μm, whereas on the same growth patterns, GaAs NPs come out to about 1 μm in height. In Fig. 3.1a, the SEM image shows a highly-ordered nanopillar array with good uniformity. Having a precise control of NP size is an important advantage of SAE over conventional VLS growth, allowing for the careful study of transport parameters across different diameters presented here[17]. Moreover, unlike VLS grown NPs, no contamination from the metal catalyst is expected using this catalyst-free growth mode[18].

3.3 In-situ surface passivation of InAs nanopillars

Radial InAs/InP NPs are formed by following InAs NP with an InP shell growth at 620˚C by shutting off TBA and turning on TBP simultaneously at a V/III of 10 for 30 seconds, without

any growth interruption. The resulting NPs have heights and diameters ranging from 4-6 μm and 50 - 200 nm, respectively, determined by the nanohole size.

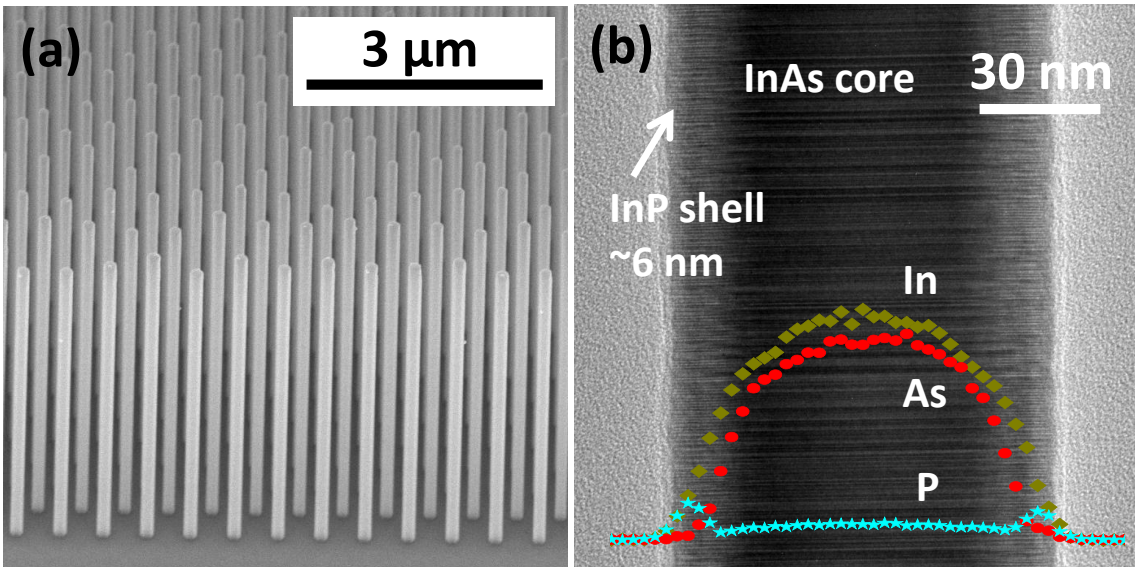

Figure 3.2: (a) Tilted SEM (52°) of an array of InAs/InP radial NPs grown by SAE. (b) TEM and EDS scan of a single InAs/InP radial NP.

Scanning electron microscopy image (SEM) shows the highly uniform, radial InAs/InP NPs (Fig. 3.2a) despite the 3.13% lattice mismatch between InAs core and InP shell. These NPs have hexagonal shapes with {01-1} sidewalls and a (111)B top surface[19]. Transmission electron microscopy (TEM) of an InAs/InP NP (d = 97 nm) shows a high density of stacking faults, or transition between zincblende and wurtzite phases, but no other structural defects. An energy-dispersive x-ray spectroscopy (EDS) line scan of In (◆), As (●) and P (★) compositions across the InAs/InP radial NP (inset of Fig. 3.2b) shows P peaks near the edges, confirming the InP shell formation. The EDS signal counts for all elements are much lower near the edges because the NP gets thinner because of the hexagonal shape. Matching the EDS scan to the TEM image, a thin InP shell can be resolved. The InP shell thickness, measured and averaged between 10

NPs, is 5.98 ± 0.12 nm. In planar thin film growth, this InP thickness would likely result in strain relaxation because it exceeds the theoretical bulk critical thickness (2~3 nm)[20]. In fact, there have been reports on strain relaxation through defect formations in other NP radial heterostructures for shell thicknesses more than several times the bulk critical thickness[21,22]. In the InAs/InP NPs, however, no strain relaxation is observed by TEM or diffraction pattern. This is likely because the InP shell is still within the coherency limits for such radial NP heterostructure, which is reported to be higher than that of planar[23].

3.4 Transport characterization of single InAs nanopillar FETs

Both InAs and InAs/InP NPs are fabricated into single-NP back-gate FETs for electrical characterization. The NPs are mechanically moved onto a degenerately p-doped Si substrate covered with 300 nm SiO_2 with a Cr/Au back gate contact. Source and drain contacts are defined using e-beam lithography followed by Cr/Au (10/120 nm) metal deposition and liftoff. Devices are characterized with an Agilent 4156C parameter analyzer at room temperature without illumination.

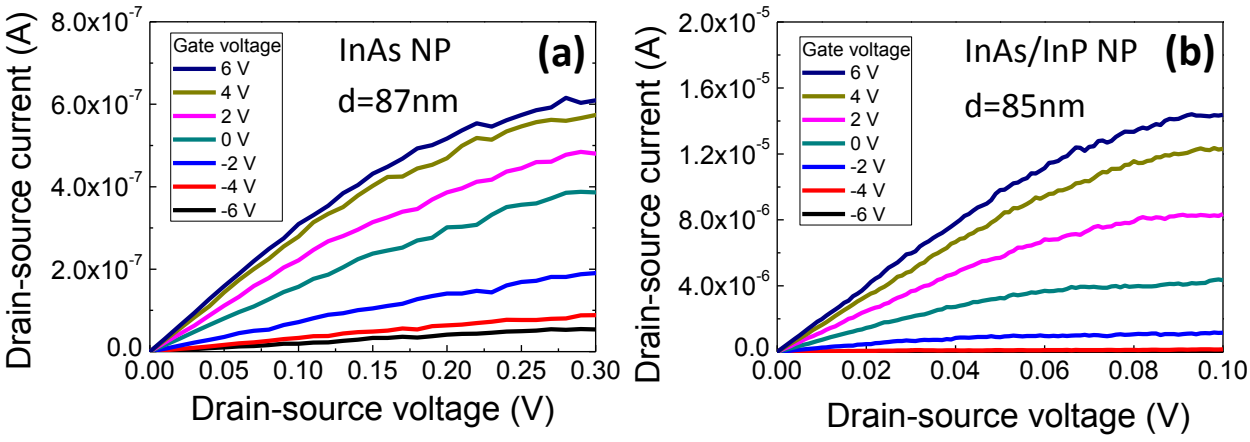

Figure 3.3: I_{DS} versus V_{DS} with back gate biases ranging from -6V to 6V for (a) an InAs NP FET and (b) an InAs/InP radial NP FET with similar diameter, measured at 300K.

Figure 3.3a and 3.3b show the drain-source current (I_{DS}) versus drain-source voltage (V_{DS}), with gate bias (Vg) ranging from -6 V to 6 V, of an InAs and an InAs/InP FET, respectively, with similar diameters. The I-V behavior of InAs FET under low V_{DS} before reaching saturation (V_{DS} < 0.05 V in Fig 3.3a) is linear, indicating good ohmic contacts. For both InAs and InAs/InP devices, there is an increase in I_{DS} with more negative Vg and the device can be turned off by applying positive Vg. Such gate response represents a depletion-mode n-type InAs channel behavior even without intentional doping during NP growth. This is likely originated from surface Fermi-level pinning in the conduction band by either surface states or the larger band-gap InP shell[13,14]. The I_{DS} of InAs/InP FET (Fig. 3.3b) measured at V_{DS} = 0.04 mV is 4.6 μA, which is a significant increase compared to the InAs FET with I_{DS} of 50 nA, measured at the same V_{DS} (Fig. 3.3a).

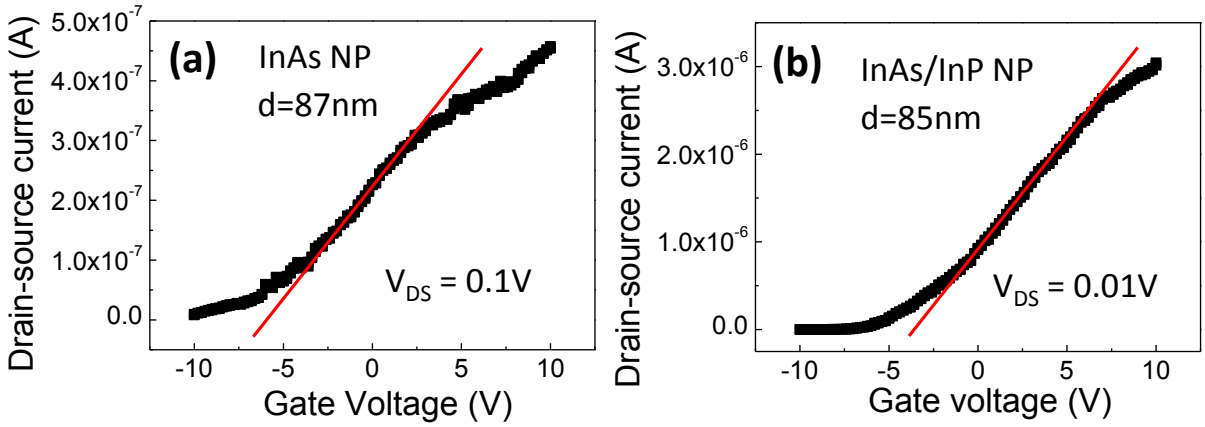

Figure 3.4: Transfer characteristics of (a) an InAs NP FET measured at V_{DS} = 0.1 V and (b) and an InAs/InP radial NP FET measured at V_{DS} = 0.01 V, with back gate biases from -10V to 10V, measured at 300K.

The transfer characteristics of the same devices, measured at V_{DS} = 0.1 V for the InAs FET and at V_{DS} = 0.01 V for the InAs/InP FET, are depicted in Fig. 3a and 3b. From the InAs device, a transconductance (g_m = dI/dVg) of 41.8 nS and a subthreshold slope (SS) of 6.93 V/dec is extracted. The on and off currents I_{ON} and I_{OFF} are measured to be 397 nA and 8.29 nA, respectively, resulting in a poor on/off ratio of 48. The transfer characteristics of the InAs/InP device shows a higher g_m of 250 nS, a lower SS of 1.48 V/dec, and a much improved on/off ratio of ~ 10^3 (I_{ON} of 3.56 μA and I_{OFF} of 1.99 nA). The current level and on/off ratio are greatly enhanced because of a reduced surface states density and the suppression of the electron accumulation layer at the surface with a thin InP shell[14]. Now, instead of traveling through the surface accumulation layer, more carriers conduct through the NP bulk. These phenomena lead to a reduction in surface scattering and better electrical transport. There are also some improvements in the FET transfer characteristics but they are still inferior to the ideal cases. It is believed further improvements can be achieved with better gate structure design with the use of a thin high-κ dielectric.

From the I_{DS}-V_{DS} linear region with zero gate bias, by measuring the resistance, the NP resistivity can be extracted using the following equation:

$$\rho = RA/L \qquad (3.1)$$

Here, R is the measured resistance, A the NP cross-section area calculated using circular approximation, ρ the resistivity and L the channel length of each device. Field-effect mobility (μ_{eff}) can also be extracted from the transfer characteristics of each device based on calculated gate capacitance according to a back-gate geometry[24,25]. By measuring different single-NP FETs, the resistivity and field-effect mobility as a function of NP diameter can be compared. The

results from the InAs (■) and radial InAs/InP (▲) NP FETs are plotted in Fig. 3.5a and Fig. 3.5b, respectively.

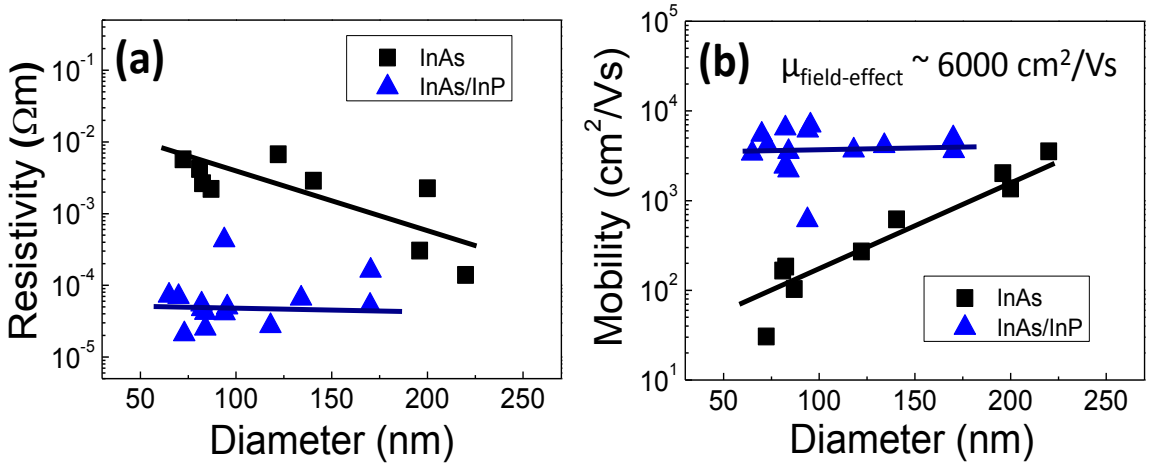

Figure 3.5: (a) Measured InAs and InAs/InP NP resistivity versus NP diameter. (b) Extracted InAs and InAs/InP field-effect mobility as a function of NP diameter.

For the InAs devices, both ρ and μ_{eff} appear to be highly dependent on the NP dimension, with ρ changing from 5.69 × 10^{-3} Ω-m to 1.4 × 10^{-4} Ω-m and μ_{eff} from 30.5 cm^2/V-s to 3,529 cm^2/V-s when the diameter increases from 72 nm to 220 nm. This observation can be explained by increased surface carrier scattering and trapping due to surface states with more pronounced effects on smaller InAs NPs. In contrast, radial InAs/InP NP devices exhibit nearly diameter independent transport behaviors with average ρ of ~ 5 × 10^{-5} Ω-m and μ_{eff} of ~ 6,000 cm^2/V-s. In particular, for the device depicted in Fig. 3, μ_{eff} is estimated to be 6,900 cm^2/V-s. From the diameter independent ρ and μ_{eff}, it is then assumed that surface states no longer have a major impact on the radial InAs/InP NP transport. Therefore, using $N_D \approx 1/q\rho\mu_n$, a carrier concentration N_D of 2.08 × 10^{-17} cm^{-3} is estimated, which is in close agreement with previous reports[26,27].

Even after the InP shell passivation, the average extracted μ_{eff} of 6,000 cm^2/V-s is still lower than the bulk mobility of 22,700 cm^2/V-s, likely due to other mechanisms, such as InAs/InP interface scattering. The high stacking fault density can also introduce band offsets[28], leading to increased carrier scattering along the NP and thus reduced μ_{eff}.. Furthermore, μ_{eff} is extracted based on the back-gate FETs using a 300 nm SiO_2 as dielectric with poor electrostatic control. Therefore, by implementing an improved gate design, such as vertical all-around gate, and a thin high-κ dielectric layer, better transistor characteristics can be achieved in these InAs FETs.

Overall, the surface states have a negative impact on InAs NP transport characteristics in terms of increased resistivity and reduced μ_{eff}, as NP dimension decreases. By growing a thin in-situ InP passivation shell, transport parameters are improved and diameter independent transport parameters because of suppressed surface states, with μ_{eff} as high as 6,900 cm^2/V-s. Moreover, the InP shell also provides better carrier confinement in the channel which leads to enhanced transistor transfer characteristics. Such radial InAs/InP NP heterostructures have the potential as an ideal material choice for NP high electron mobility transistors.

3.5 Vertical surround-gate InAs nanopillar FETs

In order to improve transistor device characteristics based on the InAs NP channel with InP in-situ passivation, another design of device geometry that provides superior electrostatic gate control is investigated and fabricated. Instead of removing the as-grown NPs onto a foreign platform to make the back-gate single-NP FETs, a vertical surround-gate NP FET design is employed. This surround-gate geometry results in the best electrostatic gate control because the entire NP channel perimeter is equally effectively modulated[2,26]. The added benefit of such a

junction-less FET design is the mitigated short channel effects encountered in the more conventional MOSFETs due to device miniaturization and scaling down. including drain and gate induced barrier lowering effects and junction break down[29].

The fabrication of vertical surround-gate NP FETs is consisted of a series of steps of deposition, planarization and etching following the NP growth. The process flow is depicted in Fig. 3.6.

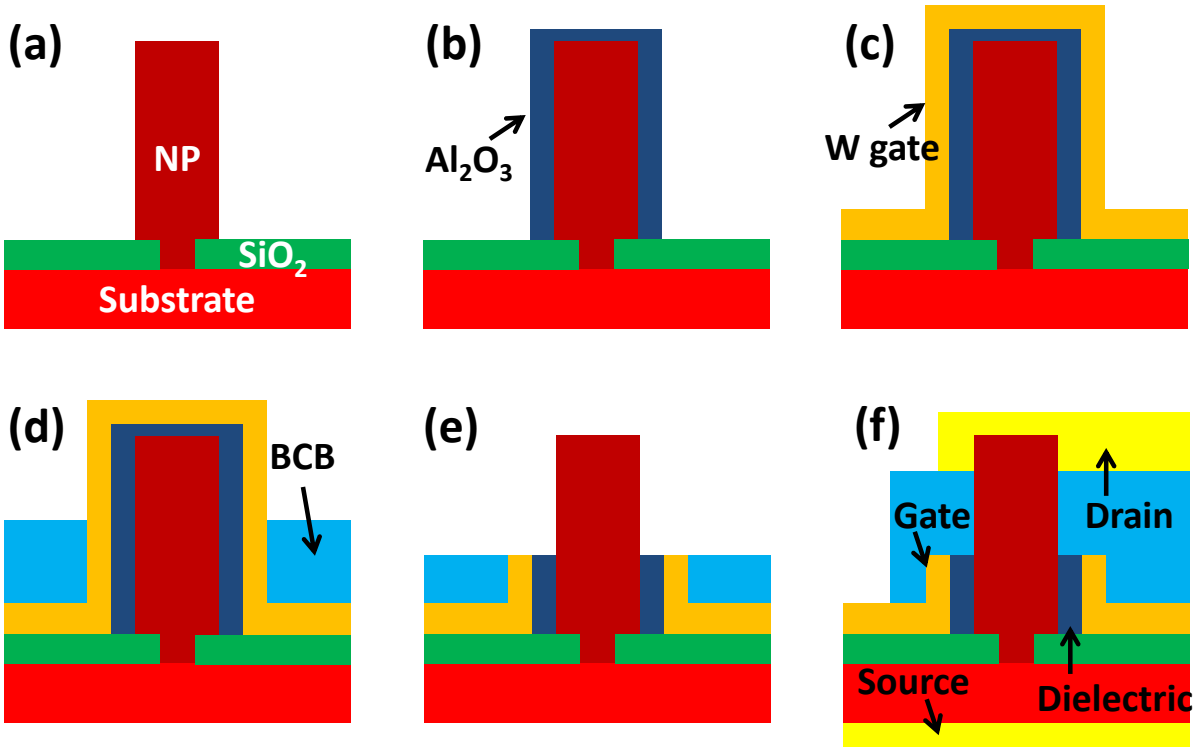

Figure 3.6: Schematics of vertical surround-gate NP FET process flow. (a) The as-grown NP on the growth substrate. (b) High-k dielectric Al_2O_3 deposition by ALD. (c) Sputtering deposition of conformal W gate around the NP. (d) Planarization by BCB followed by BCB etching to define the gate length. (e) W gate etching followed by Al_2O_3 etching to expose the NP tip. (f) Another BCB planarization and etch back followed by drain and source contact metal evaporations.

First, the InAs/InP NPs are grown under the same condition as described in the previous section. Instead of removing them, the as-grown NPs are left untouched on the growth substrate, as shown in Fig. 3.7a. The as-grown NPs have a pitch of 600 nm, diameter of 120 nm and length of 1.2 μm. A conformal high-k dielectric is then deposited by atomic layer deposition (ALD) using precursors trimethylaluminium (TMAl) and H_2O at a pressure of 0.5 Torr. A total number of 200 cycles is deposited, resulting in a dielectric thickness of 10 nm and a total diameter of 140 nm, as shown in Fig. 3.7b. The Al_2O_3 appears to be uniformly coated throughout the entire length of the NPs, despite the lattice mismatch (Al_2O_3: 4.785Å, InP: 5.869Å, InAs: 6.053Å). Following conventional photolithography to define the device region within the NP array, the tungsten (W) surround-gate metal layer is deposited by DC sputtering using Denton sputterer with a constant DC source of 0.3 A, plate rotation of 50 rpm for 15 minutes. The resulting structure after metal liftoff is displayed in Fig. 3.7c. The W sputtering is clearly not perfectly conformal. The final diameters near the tip and the base are measured to be 300 nm and 250 nm, respectively. Even with this discrepancy, the gate thickness near the base is still sufficient to provide needed electrostatic modulation and electrical connectivity with a minimum gate thickness of at least 55 nm. Planarization by benzocyclobutene (BCB) and etch back using a reactive-ion etch, the top region of which W and Al_2O_3 are to be etched off, can be defined, hence effectively determining the gate length. In this case, a gate length of 230 nm is estimated. as shown in Fig. 3.7d. The gate W metal is etched chemically using 30% H_2O_2 solution for 3 minutes (Fig. 3.7e). Finally, exposure of NP tip is completed by etching the Al_2O_3 dielectric in diluted HF solution (100:1)[30] and the resulting structures are depicted in Fig. 3.7f. As seen in the SEM image, even after extensive fabrication processes, the NPs still maintain their structural integrity. Another round of BCB planarization and etch back is employed to provide isolation

between gate and drain contacts. Drain and source contacts (Cr/Au) are coated by e-beam evaporation in two separate depositions. Finally, gate trench is selectively etched to reach the gate contact.

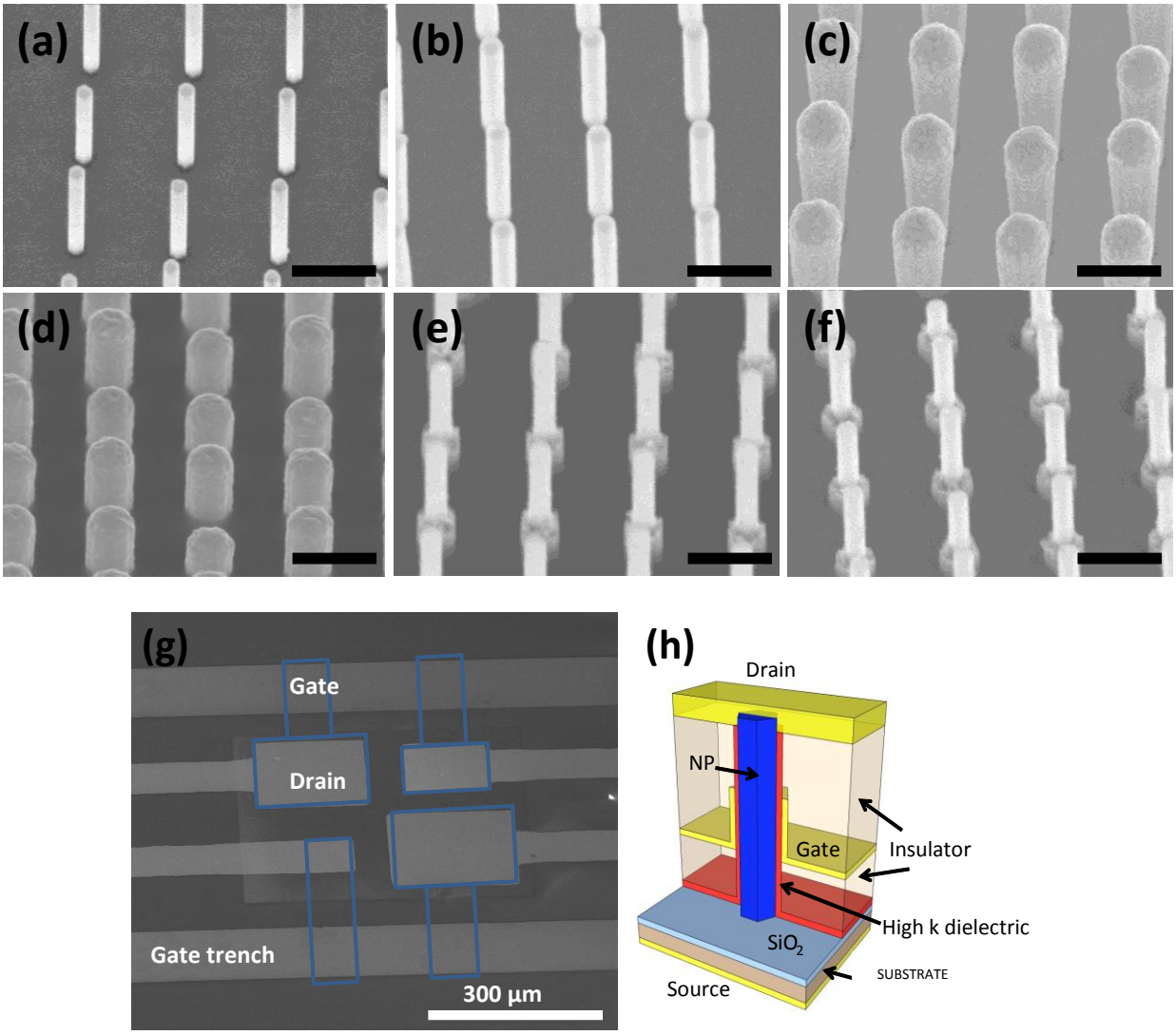

Figure 3.7: SEM images showing the process flow of vertical surround-gate NP FET fabrication. The scale bar represents 500 nm. (a) The as-grown InAs/InP NPs. (b) The NP array after Al_2O_3 deposition by ALD. (c) The NP array after W gate sputtering. (d) After BCB planarization and etch back to expose the NP tips. (d) After etching the W with H_2O_2 solution. (f) After etching the Al_2O_3 with HF solution. (g) A SEM image of the final device showing the etched trench to reach the W gate, outlined by the blue box. (h) A schematic showing the final device structure.

Figure 3.7g shows the finalized device SEM micrograph. Within the 500 μm^2 NP array, four vertical surround-gate FETs are defined, each with different number of NP channels in parallel. The blue boxes outline the W surround gate underneath the BCB and a trench is selectively etched in the BCB region to reach the gate contacts. The completed device structure is depicted schematically in Fig. 3.7h to show the top and bottom drain and source contacts, the surround-gate contact and the thin high-k dielectric.

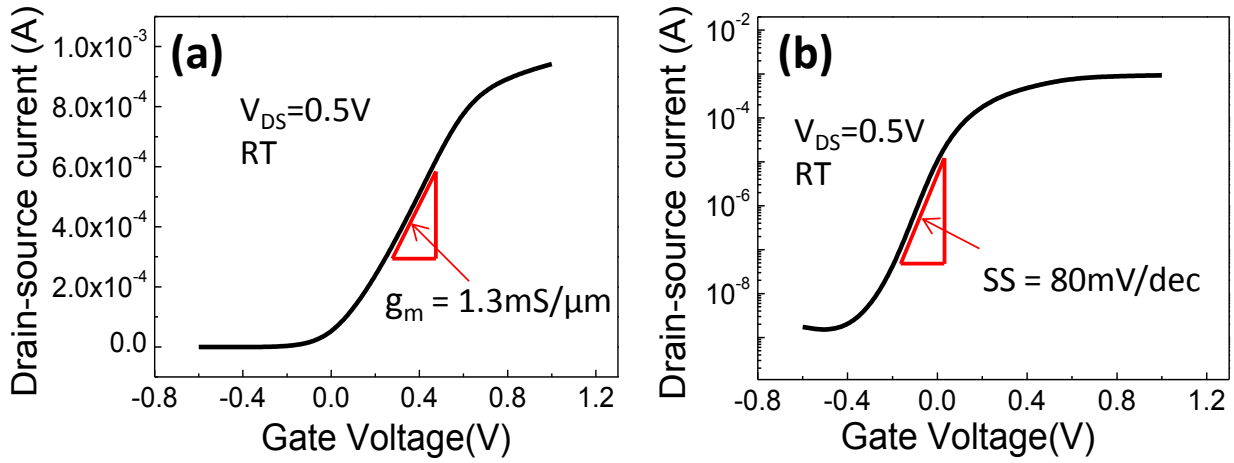

Figure 3.8: (a) The transfer characteristics of the vertical surround-gate NP FETs measured at room temperature and at V_{DS} = 0.5 V and (b) the same transfer characteristics under semi-log scale to show the subthreshold regime.

The device performance of the fabricated vertical surround-gate FETs using InAs/InP NPs as channels are studied by Agilent 4156C. The resulting transfer characteristics are displayed under linear scale (Fig. 3.8a) and semi-log scale (Fig. 3.8b), measured at room temperature at a supply voltage of V_{DS} = 0.5 V and gate bias ranging from -0.6 V to 1 V. Within this range, the tansconductance g_m, normalized to NP perimenter, is estimated to be 1.3 mS/μm,

and the subthreshold slope SS is measured to be 80 mV/dec. Both are significant improvements from the simple single-NP FET design with a global back gate, which are expected because of the better gate control and the use of high-k dielectric. The small SS of 80 mV/dec and high g_m are also close to the state-of-the-art NP FETs[2] and can prove to be a very attractive channel materials for ultra-low power logic devices.

3.6 Summary

The InAs channels, without any intentional doping during the NP growth, exhibit n-type channel characteristics. This is likely because the surface Fermi-level of InAs is pinned very close or even above the conduction band[13]. Without surface passivation, the field-effect mobility and resistivity are highly dependent on NP dimension. In-situ surface passivation is provided by growing a thin InP shell (~5nm), with an excellent crystal integrity despite the lattice mismatch. With the InP shell, the channel effective electron mobility becomes diameter independent and increases significantly to ~ 6,000 cm^2/V-s with an unintentional doping level of 2×10^{17} cm^{-3}. The InAs/InP NP channels are then fabricated into vertical surround-gate FETs employing high-k Al_2O_3 dielectric and sputtered surround W gate. Such device geometry provides much better electrostatic gate control compared to the single-NP FET design. The vertical surround-gate FETs show good DC characteristics with On/off ratio of 10^6, transconductance of 1.3mS/μm and subthreshold swing of 80mV/dec at a relative low supply voltage of 0.5V. Overall, it is shown that a robust surface passivation scheme is essential to achieve reliable and consistent NP materials properties. With good surface passivation, these InAs/InP semiconductor NPs show their potentials as next-generation electronic devices as the constant device scaling down inevitably faces the physical limitations faced by silicon.

3.7 References

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Chapter 4

InAs/InP axial heterostructures

4.1 Overview

Heterostructure formation in nanopillars (NPs) is especially interesting for device applications such as quantum well (QW) or quantum dot (QD) infrared photodetectors, tunnel transistors and quantum cascade lasers (QCLs). The two types of nanowire heterostructure generally considered are core-shell NPs, where the heterostructures are formed in the radial direction, and axial heterostructures, where the material changes along the axis of the pillar. A precise control of these two types of structures can lead to nano-bandgap engineering in three dimensions inside the NPs. Radial heterostructures in selective-area epitaxy (SAE) NPs have been demonstrated in the previous sections.

While successful demonstrations based on vapor-liquid-solid (VLS) nanowires have been reported to show quantum structures with abrupt interfaces[1,2], the same demonstration in SAE NPs has been elusive. This difficulty is posted by the nature of SAE because of the sensitivity of growth direction and materials incorporation rate based on local environment, such as temperature, different exposed surfaces and local atomic arrangements[3,4]. In the case of InP insert growth in InAs NPs, the InP region tends to form in both the radial and axial directions. The scanning transmission electron microscopy (STEM) image of such InAs/InP NP heterostructure, recorded by a high angle annular dark field (HAADF) detector, is displayed in

Fig. 4.1. In this imaging mode, the contrast is determined by the atomic number of the material under study (Z contract), which can be used to distinguish between different materials.

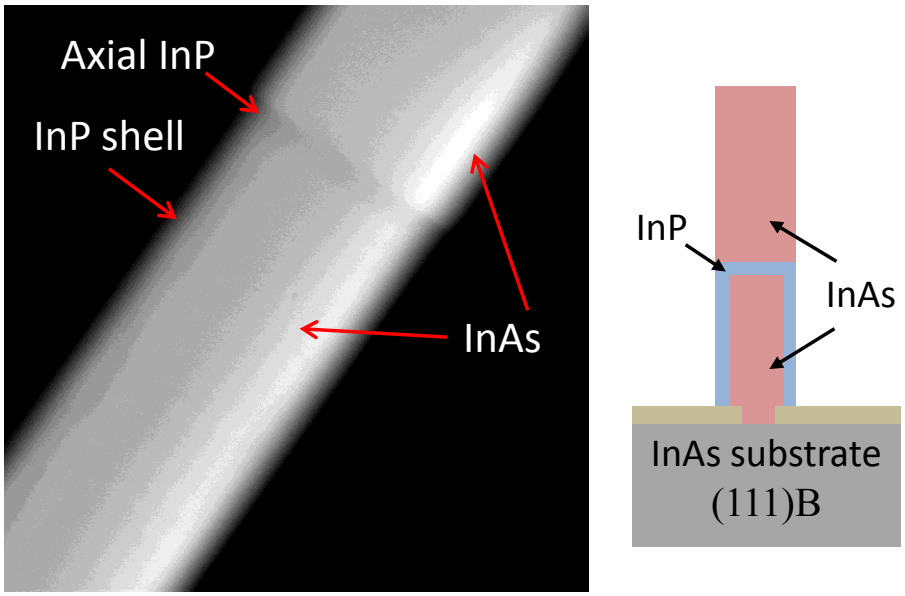

Figure 4.1: STEM image of an InAs/InP single barrier NP grown at the same temperature at 620˚C. The InP heterostructure grows in both radial and axial directions. The illustration shows the structure of the resulting growth to show the InP shell formation.

The darker regions in the STEM image denote the InP axial insert and InP radial shell growth. The illustration in Fig. 4.1 shows the radial/axial InP heterostructure. In this chapter, the effort towards realizing purely axial NP heterostructures via SAE with sharp interfaces is discussed with a focus on the InAs/In(As)P materials system. Two different growth directions are presented to achieve the proposed structures. Both single barrier and double barrier NP structures are investigated electrically to demonstrate carrier transport over or through the barriers inside the NPs.

4.2 Two-temperature growth

The first technique explored of which purely axial InAs/InP NP heterostructures can be realized is through a two-temperature growth mode. The concept is actually quite simple. Since there does not exist a common growth environment in which both materials favor vertical growth only, different growth temperatures are probed, independent of the InAs region, to find the conditions for axial InP growth (i.e. conditions for InP NPs on InP substrate). It is found that there is a narrow window for such growth at 660˚C with a V/III ratio of 49. With this knowledge, a two-temperature growth approach is employed to synthesize purely axial InAs/InP heterostructures on InAs substrates. The growth sequence is depicted in Fig. 4.2. The colors indicate when each precursor is turned on at a given time during the growth.

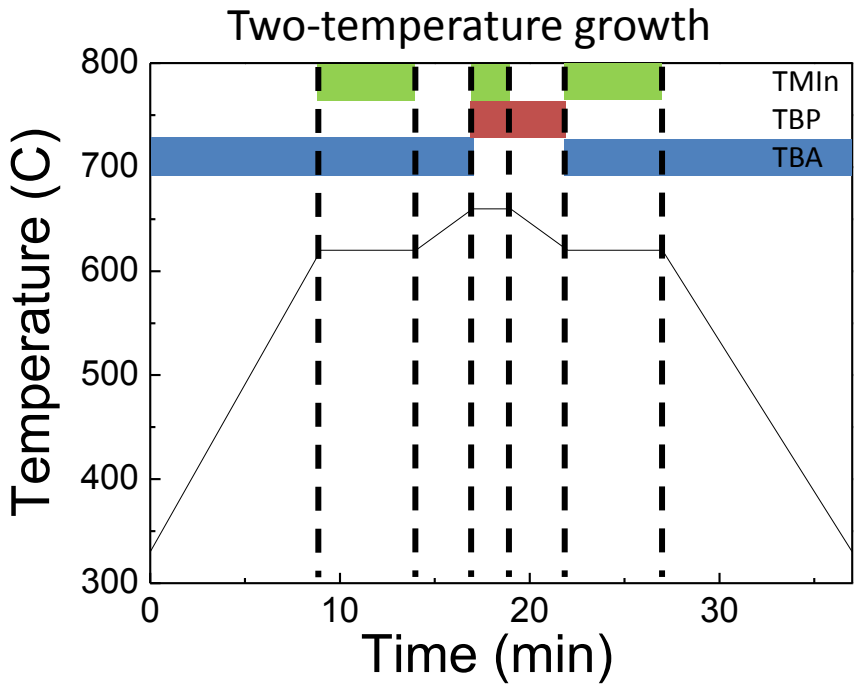

Figure 4.2: The growth sequence of the two-temperature growth to achieve purely axial InAs/InP heterostructure. The InAs segments are grown at 620˚C, whereas for the InP segment, the temperature is raised to 660˚C.

First, the temperature is ramped up to the InAs NP growth temperature of 620˚C under As overpressure by flowing TBA, followed by 5 minutes of InAs NP growth by flowing TBA and TMIn at a V/III ratio of 10. Then, the temperature is raised to the InP NP temperature of 660˚C under As overpressure to prevent desorption. Once the temperature is reached and stabilized, InP insert is grown by simultaneously turning off TBA and switching on TBP at a V/III ratio of 49 for 1 minute. The temperature is restored back to InAs temperature under P overpressure to growth the second InAs region to complete the heterostructure formation.

4.2.1 Single barrier structure

The resulting InAs/InP NP heterostructure array utilizing the two-temperature growth mode is depicted in the SEM micrograph in Fig. 4.3. The NP array shown here have a average height of 4.2 μm, diameter of 130 nm and a pitch of 500 nm.

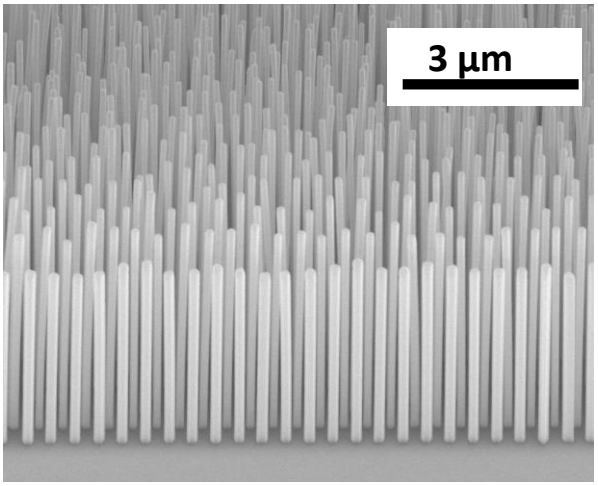

Figure 4.3: A tilted SEM image (52˚) showing the InAs/InP NP heterostructure using the two-temperature growth.

The STEM image shown in Fig. 4.4a confirms the purely axial InP insert formation, represented by the darker region in the NP. The InP thickness is measured to be 21 nm with abrupt interfaces on either side of the insert. The InAs/InP NP heterostructures are the fabricated into single-NP devices, as shown in the SEM micrograph (inset of Fig. 4.4b). When biased between -1.5 V and 1.5 V, the IV curves exhibit a non-linear, symmetric behavior, which is typical in carrier transport over or through a barrier.

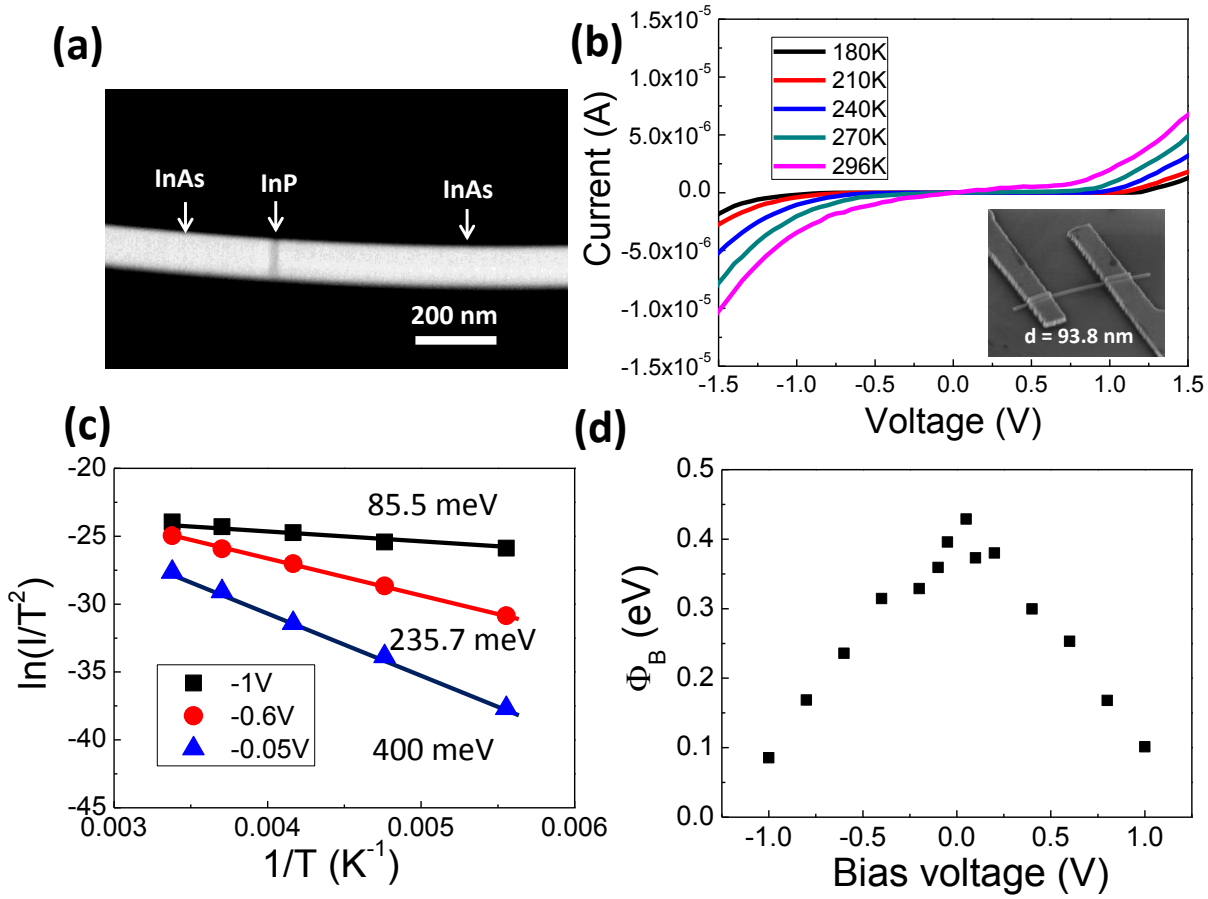

Figure 4.4: (a) A STEM image of the InAs/InP/InAs single barrier NP structure grown by the two-temperature method. (b) IV measurement of a InAs/InP single-NP device performed at different temperature. (c) The Arrhenius plot at different bias point to extract barrier height. (d) Barrier height as a function of bias.

In order to estimate this barrier height, the transport characteristics are measured at different temperature, ranging from 180 K to 296 K, cooled down by liquid nitrogen (LN_2) in a cryogenic probe station, also shown in Fig. 4.4b. Since the InAs NPs have been shown to be n-type without any intentional doping[5,6], the extracted barrier height is the conduction band offset between InAs and InP. Since the current is governed by the thermionic emission process, it must have the following relation[7]:

$$I \propto T^2 e^{\frac{-q\Phi_B}{kT}} \quad (4.1)$$

In Eqn. 4..1, I denotes the measured current, T the temperature, q the electron charge, k the Boltzmann constant and Φ_B the barrier height. By plotting the $ln(1/T^2)$ versus inverse temperature at different biases, an effective barrier height Φ_B can be extracted from the slope of the linear region in the Arrhenius plot (Fig. 4.4c) of at the given bias levels. For example, at -1 V bias, Φ_B is 85.5 meV and at -0.05 V, Φ_B is 400 meV. The barrier height is lower at larger bias because the bend-bending induced by the applied potential across the NP heterostructure effectively decreases the barrier. By plotting the extracted barrier heights as a function of bias voltage, a zero bias barrier height can be extrapolated. This represents the conduction band offset between the two different materials and is approximated to be 420 meV, as shown in Fig. 4.4d. A conduction band offset of this magnitude is slightly lowered than that of planar InAs and InP in the <100> crystal direction (~600 meV). There are a few possible explanation to this discrepancy. First, the insert might not be purely InP and contain some As. Even though TBA is completely shut off during the insert growth, memory effect inside the chamber (i.e. As from the growth platter or chamber wall) can lead to As incorporation. It is also possible that the band

structure modification by wurtzite formation in the NP can cause a different conduction band offset[8,9].

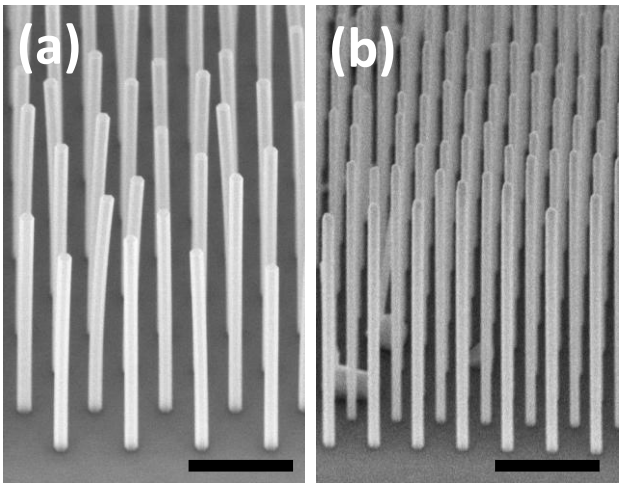

Figure 4.5: SEM images of nanopillar array of single barrier InAs/InP/InAs heterostructure grown at (a) higher InP growth rate and (b) lower InP growth rate. Scale bar denotes 1μm in length.

Even though purely axial InAs/InP single barrier structure has been demonstrated structurally by STEM and electrically by temperature-dependent measurement, the NP array appears to be non-uniform and "bendy," as shown in Figs. 4.3 and 4.5a. This is likely because of the uneven distribution of InP growth on the top of first InAs segment as the NPs only start to bend after mid-way through the length of pillar (Fig. 4.5a). To improve growth uniformity, the growth rate of the InP region is reduced by a factor of three by decreasing the TMIn flow rate from 90 sccm to 30 sccm. The growth time is multiplied by three to maintain the same InP barrier thickness. The resulting NP array is displayed in Fig. 4.5b with good uniformity. Furthermore, the NPs no longer bend, which means there is now an even distribution of InP insert during the heterostructure growth.

4.2.2 Double barrier tunneling structure

By repeating the two-temperature growth sequence twice, using slower growth rate for the InP regions, uniform NP array is demonstrated that contains a double InAs/InP heterostructure inside the NP.

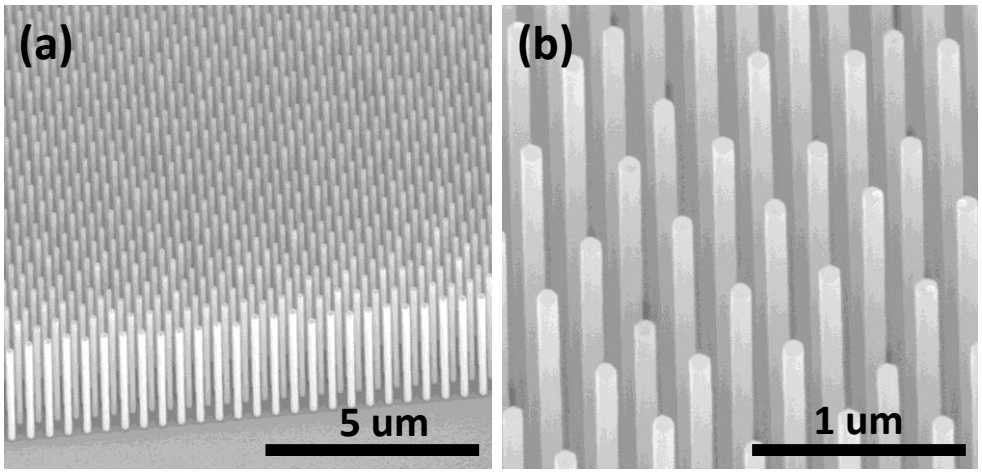

Figure 4.6: (a) A SEM image of a double InAs/InP heterostructure NP array showing good uniformity. (b) A close-up SEM image of the double heterostructure pillar array.

Figure 4.6a shows the NP array of the InAs/InP double barrier structures with an average length of 4.7 μm and diameter of 110 nm and a pitch of 500 nm. A close-up SEM image of the array is depicted in Fig. 4.6b. Structural analysis shows that the InP barriers range from 5 - 8 nm with the sandwiched InAs well in the 15 - 20 nm range. This well thickness is smaller than the InAs Bohr exiton radius[10], which should lead to quantization of discrete states inside the well. For electrical characterization, the same structure is repeated with an added InP passivation shell layer for better carrier confinement and transport properties[6]. The double InAs/InP NP heterostructures are fabricated as single-NP devices. A large number of devices are fabricated and measured. In some of the devices, when they are cooled down to cryogenic temperature, the

devices exhibit resonant tunneling behavior with somewhat symmetrical IV characteristics, as exemplified in Fig. 7. This particular device is measured at T = 77K and shows negative differential resistance (NDR) in both the positive and negative bias regimes. This is a signature of electron quantum tunneling through the InP barrier into one of the discrete states in the InAs well and out through another InP barrier when the electron wavefunctions inside and outside the well overlap under a certain bias condition.

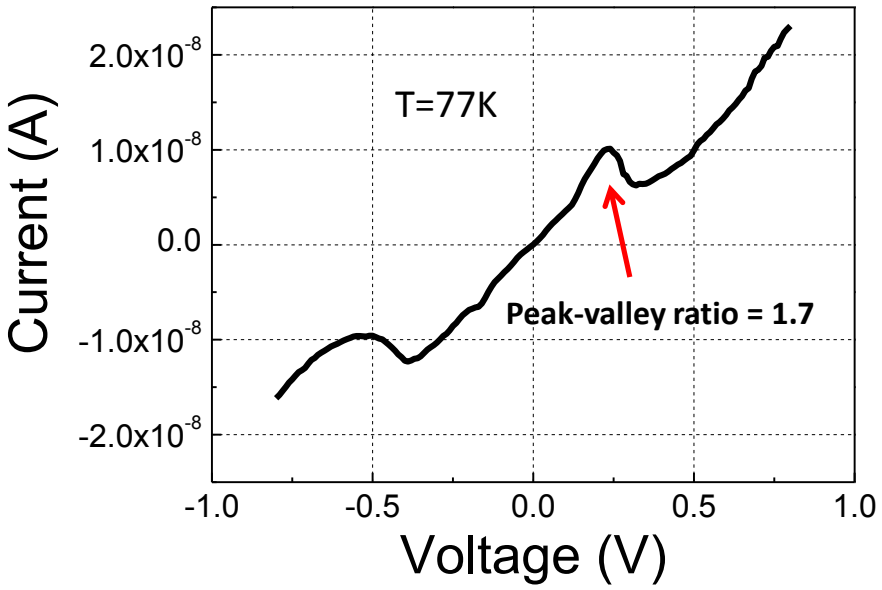

Figure 4.7: Current-voltage behavior of an InAs/InP double heterostructure with an InP shell showing the resonant tunneling behavior, measured at 77K. The peak-to-valley ratio is measured to be 1.7.

When the device is biased further, the potential across causes the bands to bend even more and the electron wavefunctions inside and outside the well no longer overlap[1,7]. This causes a decrease in current conduction and hence the negative differential resistance seen in Fig. 4.7. This device shows a peak-to-valley ratio of 1.7.

4.3 Single-temperature growth

Even though double heterostructures in InAs/InP materials system can be achieved using the two-temperature approach, the uniformity of the heterostructure formation still lacks consistency as not all the single-NP devices measured exhibit such resonant tunneling behavior. Some possible reasons for this include the inherent temperature control instability of the system or local temperature variation from NP to NP. Furthermore, with increasing number of heterostrcuture layers, the uniformity will further decrease and the growth time and materials use will therefore increase. As a result, developing a single-temperature growth technique to realize purely axial heterostructures is thus a very attractive alternative. To ease the development process, instead of growing pure InP inserts, InAsP is used as the barrier material.

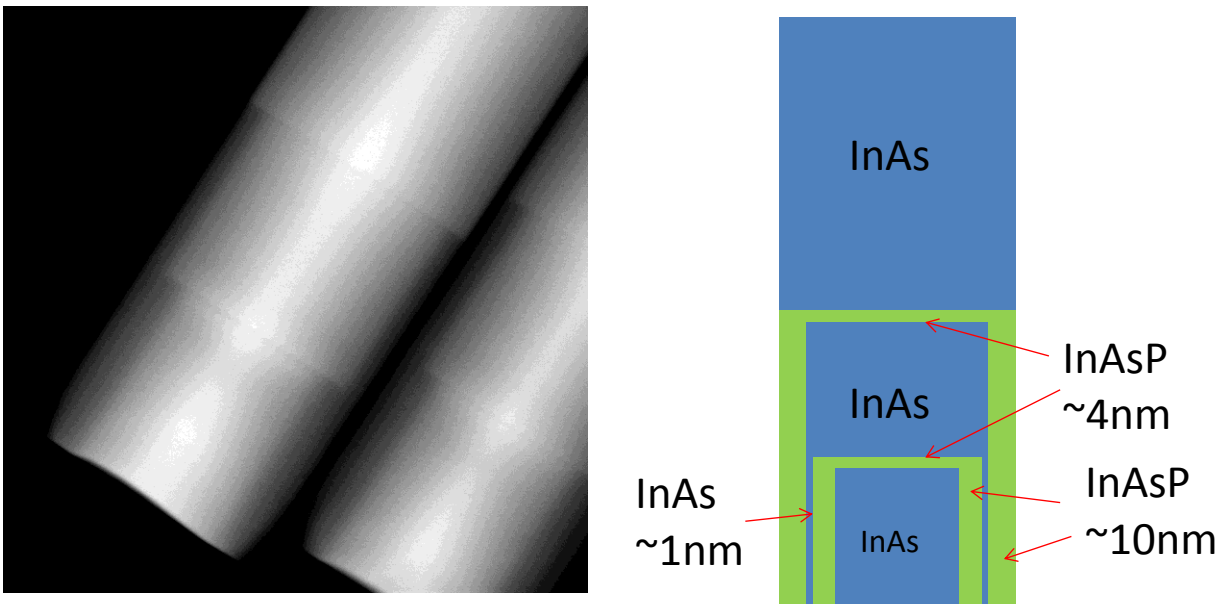

Figure 4.8: A STEM image of the InAs/InAsP double heterostructure grown at a single temperature at 620°C and a schematic detailing the resulting structure.

When the InAs/InAsP double barrier structure is grown under one temperature at 620˚C without any temperature change, the InP grows both axially and radially, as shown by the STEM image in Fig. 4.8, which clearly shows two layers of axial InAsP regions as well as two layers of InAsP shells, separated by an extremely thin InAs layer (1 nm). The illustration in Fig. 4.8 outlines the complicated structure. For each layer of InAsP insert, the radial growth rate is roughly 2.5 times the axial one, judged by the thickness difference of 4 nm (axial) versus 10 nm (radial). In order to get rid of the shell growth, an in-situ etching technique using Tertiarybutylchloride (TBCl) is employed[11,12].

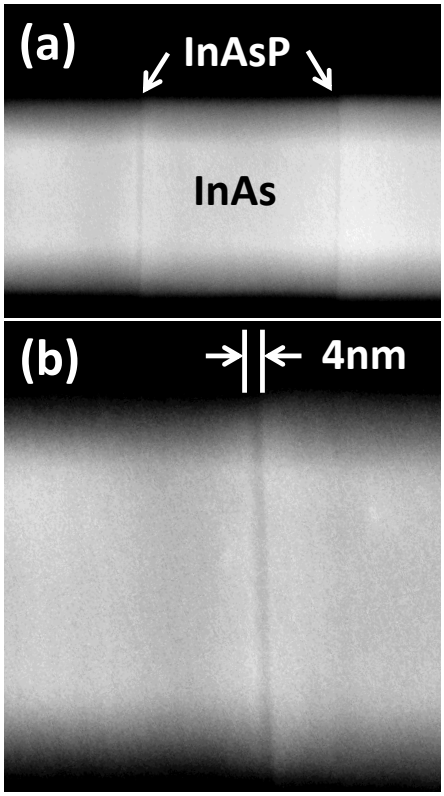

Figure 4.9: (a) A STEM image showing the InAs/InAsP double heterostructure with in-situ TBCl etching to realize purely axial heterostructure. (b) A close-up STEM image to show the highly-abrupt heterostructure interface between InAs and InAsP. The InAsP barrier is measured to be roughly 4 nm thick.

Similar in-situ etching technique using HCl has been reported to successfully achieve purely axial NP growth in the phosphide materials[13,14]. In the case of InAs/InAsP double barrier structures presented in this dissertation, TBCl is introduced after the completion of NP growth to ensure etching occurs only at the exposed sidewalls. After 5 minutes of TBCl flow, the samples are cooled down under both As and P overpressures. The resulting growth is shown in the STEM image in Fig. 4.9a, which clearly contains two purely axial InAsP inserts. The close-up STEM image in Fig. 4.9b shows the first InAsP insert with a measured barrier thickness of 4 nm and interface roughness and abruptness below the image resolution (< 1nm) on either side of the insert. To determine the actual P content in the barrier, the difference in contrast is compared in the InAs and InAsP regions; contrast is proportional to the square of atomic number in this imaging mode. The P content is found to be 25% in the InAsP barriers, resulting in a conduction band barrier height of approximately 150 meV. This band offset is more than enough to realize interesting quantum structures in the InAs/InAsP materials system.

4.4 Summary

In this chapter, different methods to achieve purely axial InAs/In(As)P heterostructures are presented. First, using a two-temperature growth, both single and double InAs/InP barrier structures are realized and confirmed structurally be STEM and electrically by temperature-dependent measurements. Based on the thermionic emission model, a conduction band offset is estimated to be 420 meV. By repeating the two-temperature growth twice, tunnel barrier structures are realized and proven by cryogenic electrical measurement, which shows the resonant tunneling diode characteristics of negative differential resistance in both positive and

negative bias conditions. It is very difficult, however, for the heterostructures grown using the two-temperature approach to result in practical, viable quantum device structures because they inherently possess too much variation and non-uniformity from NP to NP within the same array. As a result, a single-temperature is developed to achieve purely axial InAs/InAsP heterostructures by in-situ TBCl etching of the unwanted sidewalls. Very thin barrier thicknesses down to 4 nm with excellent interface quality have been demonstrated. This approach appears to be a very promising pathway to achieve well defined, well controlled quantum structures in III-V NP growth, which can lead to novel device structures with immense potential.

4.5 References

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Chapter 5

In(As)Sb nanopillars

5.1 Overview

Historically, InSb related materials have attracted special attention for its potential in the field of high-speed electronics[1] and mid-IR emitters and detectors[2,3] because it has the highest bulk electron and hole mobilities (μ_e of 77000 cm^2/V-s and μ_h of 850 cm^2/V-s) and the smallest band-gap (0.17 eV) in all the III-V semiconductors[4]. Furthermore, having a large Bohr exiton radius (> 60 nm) and a high electron magnetic moment (g* ~ 51)[5,6], InSb nanostructures are viewed as an ideal vehicle to experimentally study quantum physical phenomena and spin-orbit systems[7,8,9]. Despite these attractive properties, advanced development in InSb-based technology has been difficult because of a lack of semi-insulating, lattice-matched substrates, and convoluted epitaxial constraints. Recent progress in nano-heteroepitaxy, however, has enabled high-quality III-V nanopillars (NPs) to form on highly lattice-mismatched substrates[10,11]. This advancement opens the door for heterogeneous integration of high-performance InSb NP devices on cheaper and more readily available platforms.

Exploration of InSb in the NP community is a growing research interest, with the first reports appearing in 2005. InSb NPs have been grown using Au-assisted chemical beam epitaxy[12,13], Au-catalyzed metal-organic chemical vapor deposition (MOCVD)[14,15,16], thermal CVD[17], electrodeposition in porous templates[18], and self-nucleation[19]. Almost all recently

published methods are based on epitaxial techniques that generally use Au catalysts and an initial formation of InAs NP segments to assist the InSb NP formation. However, there has been evidence of Au atom contamination in the NPs using Au-catalyzed growth[20]; Au is known to create recombination centers in III-V semiconductors. This can significantly reduce the minority carrier lifetime and increase scattering, therefore hampering the device performance.

In the first part of this chapter, a thorough study of Au-free, direct InSb nanostructure formation on patterned InAs (111)B substrates, by MOCVD is provided. Various growth conditions that result in different types of InSb nanostructures are probed, including the conditions required to achieve NP growth. These observations are then explained by first-principles calculations using density-function theory (DFT). This paper provides a basic ground work for potential optoelectronic and electronic devices based on Au-free InSb NPs. The second part of this chapter focuses on the discussion on Au-free, selective-area InAsSb NPs, in which the growth mechanism, structural and spectral properties are studied in detail.

5.2 InSb nanopillars

5.2.1 Growth of InSb nanopillars

InSb nanostructures are grown on patterned InAs (111)B substrates with a low-pressure (60 torr) vertical Emcore MOCVD reactor, using trimethylindium (TMIn) and trimethylantimony (TMSb) as precursors. The InAs substrates are patterned with a SiO_2 mask (20-nm thick) using e-beam lithography and reactive ion etching, with a nanohole opening of 70 nm and a pitch of 500 nm. The patterned growth allows for a precise control over the position of nanostructure formation, leading to simpler device fabrication and enabling interesting new device functionalities such as bottom-up photonic crystals and plasmonic gratings using these

patterned nanostrctures[21,22]. The growth temperature in this study is limited by the low melting temperature of InSb (530˚C) at one side and the cracking temperature of TMSb source (> 450˚C) at the other one. Different growth temperatures ranging from 460˚C to 500˚C show no discernible impact on the growths. All the InSb growths presented in the study are carried out at a substrate temperature of 470˚C by flowing TMIn and TMSb under varying V/III ratios. The V/III ratio is controlled by fixing the TMIn flow while changing the TMSb flow. It is noted that the supplied Sb adatoms tend to form Sb clusters at the growth surface and these clusters need to be dissociated before being incorporated into InSb growth. Because this dissociation ratio is not perfect, the effective reacting V/III ratio is different from the supplied V/III ratio. In the interest of simplicity, the V/III ratio addressed in this chapter refers to the supplied V/III ratio. After MOCVD growth, the samples are cooled down under Sb overpressure to prevent InSb desorption. The resulting structures are studied by scanning electron microscopy (SEM) using an FEI Nova SEM/FIB system to determine the InSb nanocrystal formation and morphology. Further structural properties and chemical analyses are examined by transmission electron microscopy (TEM) and energy dispersive X-ray spectroscopy (EDS) using a FEI Titan 300 kV S/TEM system. Cross-sectional TEM samples are prepared by the FIB, using Ga ion beam for sample thinning.

The InSb growths by MOCVD are extremely sensitive to the local environments. A series of growths using V/III ratios ranging from 0.3 to 2 with a growth time of 7 minutes is depicted in the tilted SEM images in Fig. 5.1. Evidently, the resulting InSb morphologies can be controlled by tuning the V/III ratios.

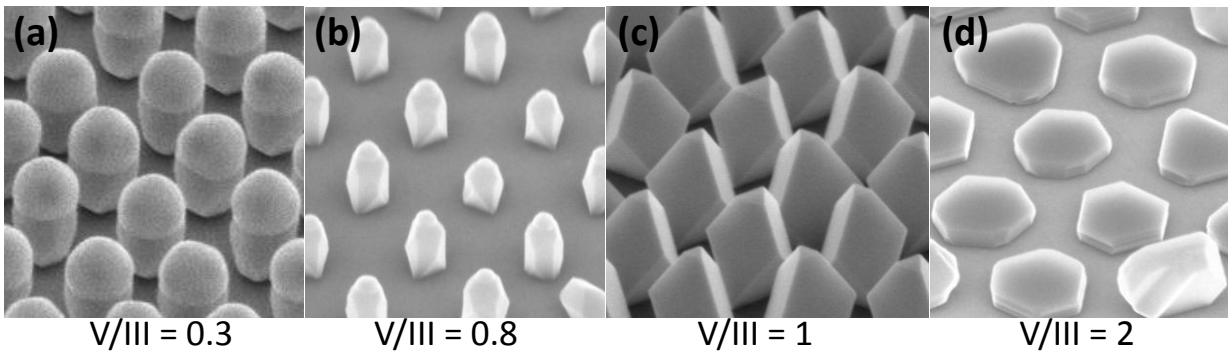

Figure 5.1: Tilted SEM images (52˚) of the resulting InSb growths at 470˚C using V/III ratios ranging from 0.3 to 2 and a growth time of 7 minutes.

Under a V/III of 2 (Fig. 5.1d), hexagonal pancake-like InSb structures with a flat (111)B top surface and {110} sidewalls are observed with minimal vertical growth with an average height and diameter of 80 nm and 400 nm, respectively. By lowering the V/III ratio, more vertical InSb structures start to form. Using a V/III of 1 (Fig. 5.1c) results in truncated InSb octahedrons with small, triangular (111)B top surfaces and inclined side facets. The average height of these truncated octahedrons is 300 nm. Lowering the V/III to 0.8 leads to yet another different structure resembling NP-like InSb formations (h = 250 nm, d = 140nm) with small In droplets on the top (Fig. 5.1b). The In droplets become more prominent using an even lower V/III of 0.3 (more In-rich), hence forming larger droplets and, consequently, InSb NPs with larger diameters (h = 410 nm, d = 290 nm), as shown in Fig. 5.1a. Typically, in other III-V semiconductors, catalyst-free, selective-area NPs take the shape of a hexagonal pillar with (111)B top surfaces and {110} sidewalls because {110} surfaces have the lowest surface energy. In the case of InSb, however, surfaces with the lowest energy appear to be different at the growth temperature under study. This discrepancy posts difficulty for purely catalyst-free InSb NP formation. Using low V/III ratios, or In-rich conditions, In droplets form and the vertical, self-catalyzed NP is initiated between the substrate and droplets. Without the In droplets, In and Sb

adatoms diffuse and relax based on the surface energetics to form the InSb equilibrium surfaces that result in non-NP growth.

Cross-sectional TEM is carried out on the InSb truncated octahedron formations shown in Fig. 5.1c to identify the preferred InSb surfaces and study the crystal structure. Figure 5.2a shows a TEM image of a single InSb truncated octahedron with side facets at different angles. The top flat facet is identified as a (111)B surface, being parallel to the InAs (111)B growth substrate.

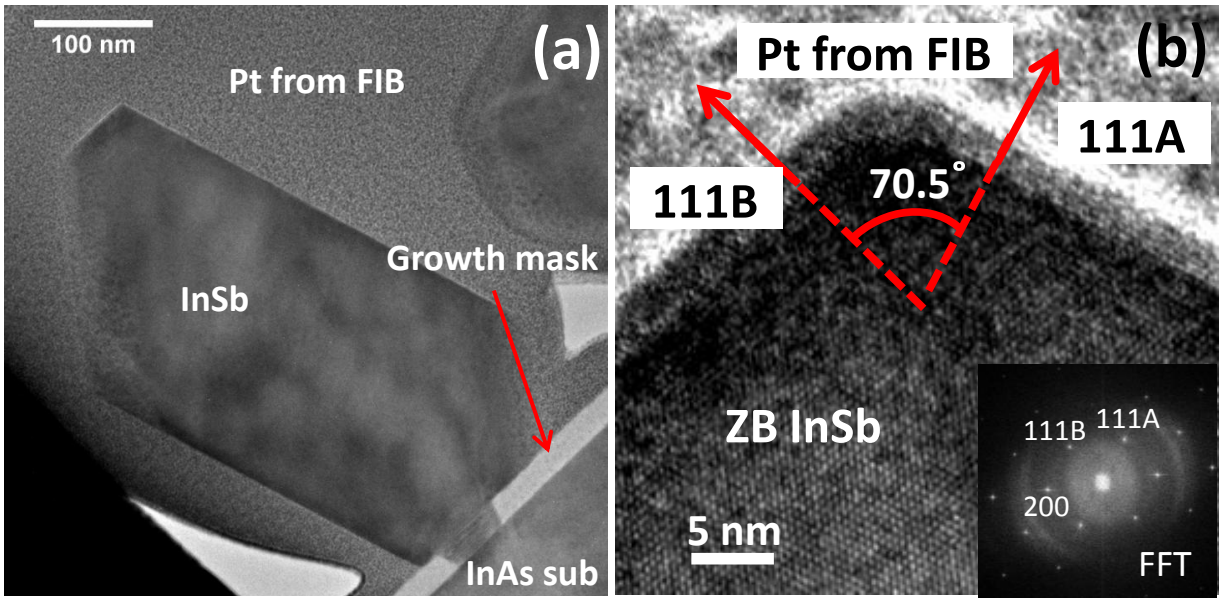

Figure 5.2: (a) cross-sectional TEM image of the InSb truncated octahedron grown at a V/III = 1, showing the different surfaces. (b) close-up of the TEM image showing purely ZB InSb and the (111)B top and (111)A side surfaces with an inset of the FFT to identify the crystal structure and different surfaces.

A close-up TEM image (Fig. 5.2b) shows that the truncated octahedron is single crystalline, zinc-blende (ZB) structure without any stacking fault or wurtzite (WZ) region. The latter is commonly observed in other NP material systems such as GaAs[23] and InAs[24]. This is likely because of the lower growth temperature (470˚C) and larger energy difference between

zinc-blende (ZB) and wurtzite (WZ) InSb. Indeed, the fast Fourier transform (FFT) image of this close-up region (inset of Fig. 5.2b) shows a purely ZB crystal structure. The normal angle between the top (111)B and the inclined side surfaces is measured to be 70.5˚, indicating the {111}A inclined surfaces. The TEM analysis concludes that this InSb nanostructure is dominated by the {111} surfaces, an indication that these are the preferred low-energy surfaces in the InSb material system.

5.2.2 Energy calculations of different InSb surfaces

To theorize the observed InSb nanocrystal formations, first-principles computations using density-functional theory (DFT) are carried out to determine the surface energies of different InSb surfaces. These calculations are performed with the software package FHI-AIMS[25]. The Perdew-Burke-Ernzerhof (PBE) parameterization of the generalized gradient approximation is used for the exchange-correlation functional[26]. The surface energy of important surface reconstructions of the (111)A, (111)B and {110} surfaces of InSb are computed using DFT. The total energy of each surface reconstruction is computed using a slab geometry 6 layers thick with a minimum of 64 equivalent k-points per 1x1 unit cell. The software FHI-AIMS is an all-electron DFT code that uses atom-centered electron-orbital like basis functions and includes a relativistic correction for heavy atoms ($Z > 30$). For these calculations, the PBE exchange-correlation functional is used, and 3s,3p,3d and 4f like basis functions are used to satisfy convergence criterion for In atoms; 3d, 5s, 5p, and 4f basis functions are used to satisfy convergence criterion for Sb atoms. The surface energy for the unrelaxed polar (111)A/(111)B surface is computed using a wedge geometry as described in Ref. [27]. The total energy of an infinitely long wedge composed of a 110, 100, and 111 surface is evaluated. The energy

contribution of the corners of the wedge is eliminated by subtracting a smaller wedge from a larger wedge. The remaining contributions are from bulk InSb, which can be easily subtracted, and from the three surfaces, two of which are computed using traditional slab techniques. The values for the non-symmetric polar surfaces computed using this technique are 0.038 eV/A^2 for (111)A and 0.028 eV/A^2 for (111)B. The values of $E_{111A/B}$ calculated using the wedge construction are scaled proportionally to γ_{111A} = 0.053 eV/$Å^2$ and γ_{111B} = 0.038 eV/$Å^2$ so that their sum equals the total surface energy of an unrelaxed polar 111A/B slab $E_{111A} + E_{111B}$ = 0.091 eV/$Å^2$. These scaled values are then used as the surface energy of the bottom unrelaxed surface for all other slab calculations.

Following the work of Ref. [28], the surface free energy is computed from the equation,

$$(\gamma_{top} + \gamma_{bot})A = E_{slab} - N_{In}\,\mu_{InSb} - (N_{Sb} - N_{In})\mu_{Sb}\,, \qquad \mu_{Sb(bulk)} - \Delta H < \mu_{Sb} < \mu_{Sb(bulk),}$$

where γ_{top} and γ_{bot} are the top and bottom surface energies, A is the surface area, E_{slab} is the total energy computed for the slab, N_{In} is the number of In atoms, N_{Sb} is the number of Sb atoms and μ_{Sb} is the Sb chemical potential. The enthalpy of formation of InSb is computed to be $\Delta H = \mu_{Sb(bulk)} + \mu_{In(bulk)} - \mu_{InSb}$ = 0.58 eV using bulk trigonal Sb and tetragonal In.

The {110} surface does not reconstruct, but In atoms in the surface can be replaced by Sb atoms and still satisfy the electron counting model. At the extreme limit, the surface is 100% terminated by Sb leading to the Sb-Sb chain structure. The surface energy if only 50% of the In are replaced by Sb is also calculated and labeled as the 50% Sb-Sb chain in Fig. 5.3.

Figure 5.3 shows the surface energy, γ, versus the calculated Sb chemical potential, μ_{Sb}, for the lowest energy reconstructions of the (111)A and (111)B, and for the 110 terminated with In-Sb chains, Sb-Sb chains, and an equal mix of the two chains.

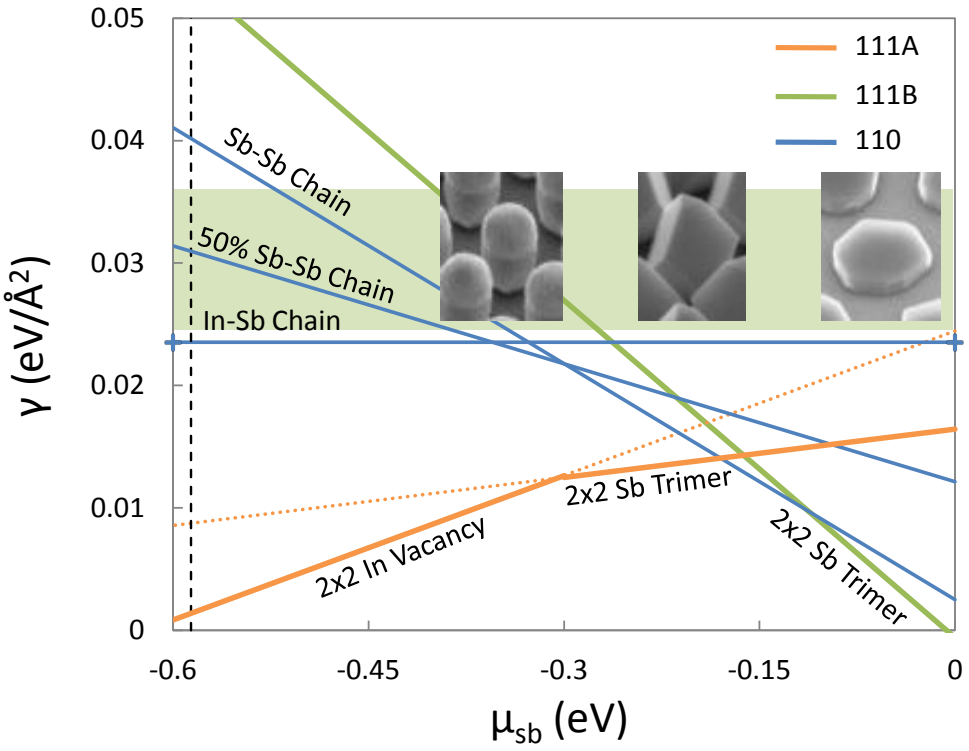

Figure 5.3: A phase diagram of surface energy for the 111A (orange), 111B (green), and 110 (blue) surface vs. chemical potential of Sb. Important surface reconstructions for each surface are shown as solid lines where they are dominant and as dashed lines otherwise. SEM images of nanocrystals are approximately positioned along the x-axis where the calculated surface energies can produce the observed shape.

Top views of the atomic surfaces are shown in Fig. 5.4. Also shown in Fig. 5.3 are the cropped SEM images of InSb nanocrystals grown at different V/III ratios. Their position along the x-axis roughly corresponds to the surface energies required to reproduce the observed morphology, and the color of the shaded background corresponds to the dominant surface. Large values of μ_{Sb} represent Sb-rich conditions and high V/III ratios, and small values of μ_{Sb}

represent In-rich conditions and low V/III ratios. The vertical dashed line at $\mu_{Sb} = -0.58$ is the calculated enthalpy of formation of InSb, which represents the lower bound of possible values for μ_{Sb}. Comparing the observed crystal structure with the calculated surface energies, it is possible to determine an empirical relationship between V/III ratio and the chemical potential, and ultimately learn the range of crystal morphologies for InSb.

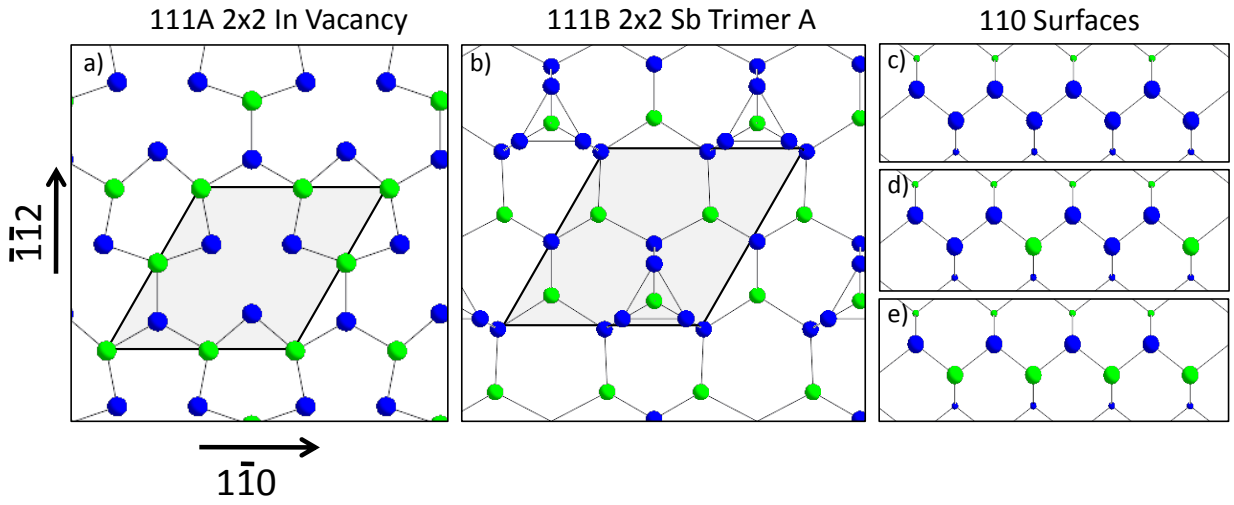

Figure 5.4: (a) The 111A In Vacancy surface reconstruction. (b) The 111B Sb Trimer surface reconstruction. (c) The 110 Sb-Sb Chain. (d) The 110 50% Sb-Sb Chain. (e) The 110 In-Sb Chain. The unit cell is outlined and shaded for the 111A and 111B surfaces. In atoms are green, and Sb atoms are blue.

The SEM images are correlated to ranges of μ_{Sb} on the phase diagram in Fig. 5.3 by inspection. At the far right is a nanocrystal whose shape is dominated by a large (111)B surface and flanked by {110} surfaces. This shape is consistent with the right of the phase diagram when $\gamma_{111B} < \gamma_{110} < \gamma_{111A}$. The intermediate nanocrystal shape is dominated by (111)A surfaces with small (111)B surfaces in a truncated octahedron and with no evidence of (110) surfaces. Such a shape will be observed if $\gamma_{111A} < \gamma_{111B} < \gamma_{110}$, however this inequality cannot be satisfied unless the (110) surface is <100% terminated with Sb-Sb chains. For example, a small region

from $-2.1 < \mu_{Sb} < -1.6$ can satisfy the inequality if the (110) surface is 50% terminated with Sb-Sb chains. At the left side of the figure, the {110} surfaces become visible and the (111)B surface area shrinks indicating $\gamma_{111A} < \gamma_{110} < \gamma_{111B}$. This situation occurs easily because of the steep rise in the (111)B surface energy as μ_{Sb} decreases.

These calculations verify that surface energy plays an important role in determining the shape of a nanocrystal grown by selective-area-epitaxy, but simultaneously indicate that there are other important physical effects driving the crystal growth. In particular, the apparent ability of the {110} surfaces to reconstruct in less energetically favorable configurations where the surface is only partially terminated with Sb reinforces the need to consider kinetic effects such as adatom diffusion and exchange with surface atoms. Nevertheless, this phase-diagram permits us to make some predictions and control over allowed and disallowed InSb nanocrystal morphologies. For instance, it is very unlikely to observe an InSb pillar shape with large {110} surface area, a small (111)B surface, and no (111)A surfaces using only selective-area, catalyst-free epitaxy.

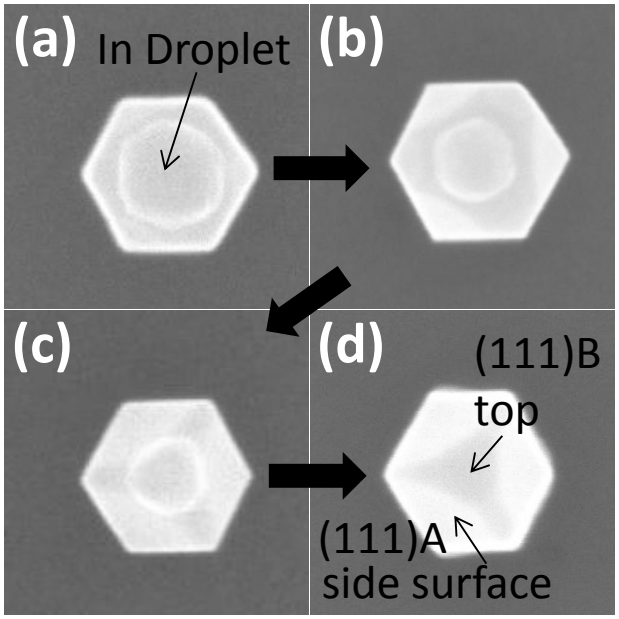

Figure 5.5: Top view SEM images of InSb NPs grown at 470˚C using a V/III ratio of 0.8 showing the progression of the inclined sidewall formation with disappearing In droplet.

With the In droplets, vertical InSb growths can be achieved; thus, if the droplets are not maintained throughout the growth, the preferred {111} facets will form, inhibiting vertical NP growth. Taking a closer look at the InSb NP growth with a V/III ratio of 0.8 from Fig. 5.1b, one can see that there are In droplets with varying sizes. This is likely because the V/III ratio of 0.8 is near the transition from purely selective-area epitaxy to self-catalyzed conditions that form In droplets. Figure 5.5 shows several top-view SEM images of these InSb NPs with different In droplet dimensions to show the progression of InSb NP formation with diminishing In droplets. The NP formation appears to follow closely with In droplet, leading to hexagonal NPs with {110} side facets (Fig. 5.5a). When the In-rich condition is not maintained, the In droplet gets incorporated into InSb NP and the three inclined {111}A surfaces start to form (Fig. 5.5b). As the In droplet shrinks, different InSb facets start to form (Fig. 5.5c) and eventually the entire droplet is absorbed by the InSb NP that result in three inclined {111}A side facets and a small

top (111)B surface (Fig. 5d). From these observations, it is concluded that In droplets are necessary to maintain vertical InSb NP growth. Under constant In-rich conditions, however, the In droplets also grow in size as growth time increases and larger droplets lead to NPs with much larger dimensions. A 15-minute InSb NP growth using a constant V/III ratio of 0.7 result in NPs with 500 nm diameter (SEM not shown). To accomplish taller NPs with smaller diameters, another approach must be developed.

5.2.3 Two-step growth to achieve high-aspect ratio InSb nanopillars

In order to achieve NPs with higher aspect ratio, we implement a two-step growth technique. The growth starts with self-catalyzed growth under a low V/III ratio of 0.7 for 7 minutes. This initial V/III ratio is chosen because any lower ratios would result in larger droplets rather quickly. Then, the V/III is raised to 0.9 for another 7 minutes in order to maintain the droplet size to achieve taller NPs, while keeping the NP diameter reasonably small.

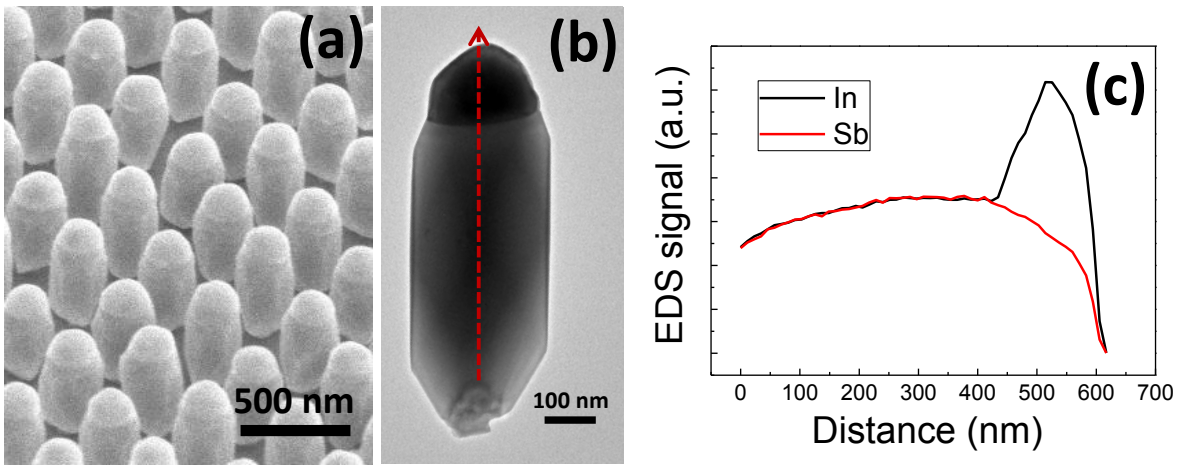

Figure 5.6: (a) A tilted SEM image showing InSb NPs resulted from the two-step growth. (b) A TEM image of a purely ZB InSb NP. (c) EDS of an InSb NP showing the In-rich droplet.

The SEM of the resulting growth is depicted in Fig. 5.6a, showing InSb NPs with an average height and diameter of 780 nm and 250 nm, respectively. The TEM image (Fig. 5.6b) shows a purely ZB InSb NP with an In droplet on the top. The twin-free, self-catalyzed InSb NPs have several advantages to avoid potential problems posted by stacking faults. The energy difference between ZB and WZ structures can lead to increased carrier scattering and reduced transport properties. The twinning can also further complicate band structure design in homo- or heterostructures. The InSb NP has flat {110} sidewalls with small (111)A and (111)B inclined surfaces near the base and the NP-droplet interface. An EDS scan along the length of the NP is used to analyze the chemical composition of the NP. The scan indicates an In droplet formation on the tip of NP and an equal amount of In and Sb atoms in the NP. We note that the scan shows that there are Sb atoms in the droplet, which is likely an artifact from the scan because the In and Sb energies have some overlap in the EDS spectrum. Using such a two-step growth mode, we have realized vertical, pure ZB, self-catalyzed InSb NPs on patterned InAs (111)B substrates without the use of any Au catalysts or initial InAs NP growth. We believe by further fine-tuning this approach, such as different combinations of V/III ratios in the two-step growth or multiple two-step cycles in one growth, taller and smaller InSb NPs can be achieved.

In summary, the growth conditions for InSb NPs directly on patterned InAs (111)B substrates are investigated. From the observed growths and DFT computations on different InSb surfaces, it is shown that the InSb nanocrystal morphologies can be controlled by tuning the V/III ratios. At higher V/III ratios (>1), pancake-like and truncated octahedron InSb structures form because the energetically favorable surfaces are the {111} facets as opposed to the {110} facets. Therefore, vertical InSb NP cannot be achieved via the selective-area, catalyst-free method. Using lower V/III ratios, In droplet forms in the mask opening that results in vertical InSb self-

catalyzed NP growth. Constant In-rich conditions, however, lead to increasing In droplet sizes that forms NPs with large dimensions. A two-step growth mode is then used to attain InSb NPs with higher aspect ratio and smaller dimensions.

5.3 InAsSb nanopillars

Even with such the successful demonstration of InSb NPs, the growth still lacks uniformity and controllability. As a result, InAsSb growths are investigated. Furthermore, it is found that the TMSb precursor decomposition rate changes dramatically in the temperature range of interest (400 - 500 ˚C)[29]. Therefore, to improve uniformity, Sb source is replaced by another precursor trisdimethylaminoantimony (TDMASb), which decomposes at a much lower temperature[30].

5.3.1 Growth of InAsSb nanopillars

InAsSb NPs are synthesized on patterned InAs (111)B substrates with and without following an initial InAs growth. The growths are carried out using a low-pressure (60 torr) vertical Emcore MOCVD reactor. TMIn, TBA and TDMASb are used as precursors. The growth substrates are, again, patterned with a SiO_2 mask (20-nm thick) with varying nanohole diameters ranging from 100 nm to 250 nm and pitches from 0.5 μm to 2.5 μm. First attempts of InAsSb NP are by growing them directly on InAs (111)B substrates for 5 minutes, despite the lattice mismatch. The resulting growths at different temperature, using a V/III of 1.3 with 20% Sb in the gas phase, are depicted in Fig. 5.7.

Clearly, at a growth temperature of 590˚C, InAsSb NPs are formed and some clusters on the growth mask with an average height of 2.5 μm (Fig. 5.7a). Some NPs are misshapen, leading

to relatively poor uniformity. When decreasing the growth temperature to 560˚C, only very short InAsSb stubs form with increasing cluster density on the growth mask, as shown in Fig. 5.7b. Further decreasing the growth temperature to 530˚C leads to even more clustering and noncrystalline InAsSb formations in the mask openings (Fig. 5.7c). In order to improve uniformity and decrease clustering, an initial InAs stub is implemented as a seeding layer to better collect the adatom collection and incorporation.

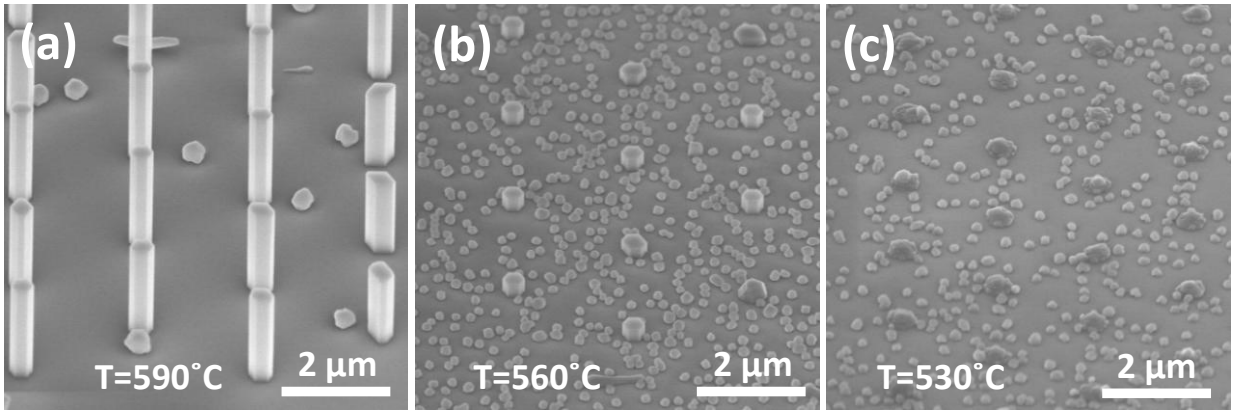

Figure 5.7: SEM images of direct InAsSb NPs on InAs (111)B substrates using a V/III of 1.3 grown at (a) 590˚C, (b) 560 ˚C, and (c) 530 ˚C with 20% Sb in the gas phase during growth.

The initial InAs stub growth is carried out by flowing TMIn and TBA for 30 seconds. The subsequent InAsSb NP growth is accomplished by simultaneously turning on TDMASb for 5 minutes at the same temperature as the initial InAs growth temperature. After growth completion, the samples are cooled down under Sb and As overpressures to prevent materials desorption. An illustration of the InAsSb NP with a short InAs stub is depicted in Fig. 5.8a. Figure 5.8b shows the SEM image of the initial InAs stub formation after 30 seconds of growth. These InAs stubs have an average height of 35 nm and are of hexagonal shape. Figure 5.8c shows the SEM image of the InAsSb NP array, with an Sb content of 63% in the gas phase, following the InAs stub formation. The average height and diameter are 1.4 µm and 180 nm,

respectively. Evidently, with the InAs seeding layer, the NPs are highly ordered with good uniformity. Furthermore, the clusters on the growth mask are no longer present even with an elevated 63% Sb percentage in the gas phase. This is likely because the initial InAs seeding layer helps the nucleation efficiency of Sb adatoms. Instead of having to diffuse around the growth mask to find exposed InAs wafer region, the extended InAs stubs provide an extra area for InAsSb nucleation.

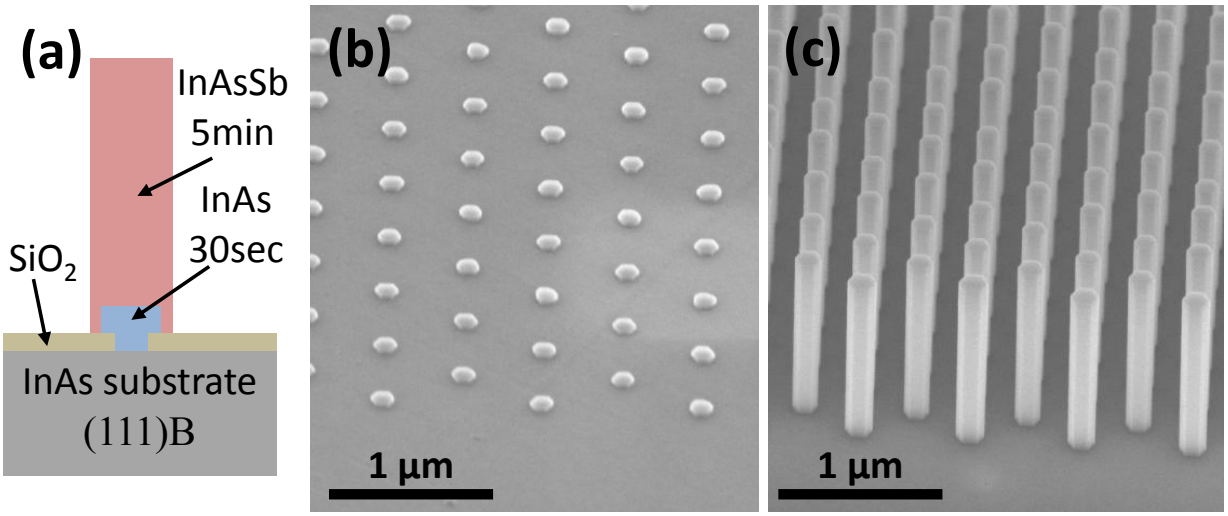

Figure 5.8: (a) An illustration showing an InAsSb NP grown on an initial InAs stub (not drawn to scale). (b) An SEM image showing the initial InAs stubs with a growth time of 30 seconds with an average height of 35 nm. (c) an SEM image showing the subsequent InAsSb NP growth on the InAs stubs with a growth time of 5 minutes and 63% Sb in the gas phase.

To probe the structural properties of these InAsSb NPs, TEM analysis is performed using a FEI Titan 300kV S/TEM. Figure 5.9 depicts the comparison between a pure InAs NP and an InAsSb NP. As shown in Figs. 5.9a and 5.9b, both types of NP contains stacking fault formation that is perpendicular to the growth direction, indicated by the contrast change in the images.

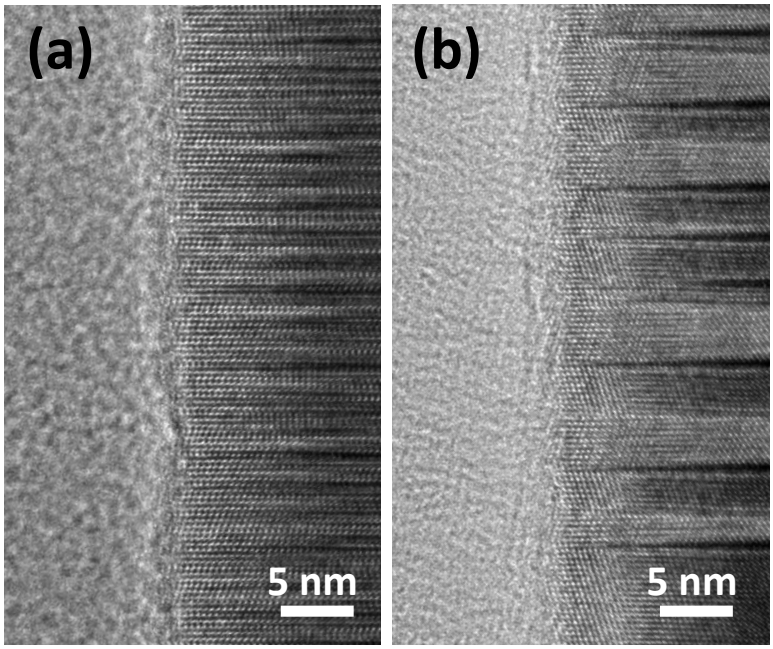

Figure 5.9: HRTEM images of (a) an InAs NP segment and (b) an InAsSb NP segment with 63% Sb in the gas phase. The InAs NP has much a higher stacking fault density compared to the InAsSb NP.

From such TEM images, the number of stacking faults can be counted. For the InAs NPs, the number of stacking fault, counted and averaged over several TEM images, is approximately 61 over 100 nm. For the InAsP NPs, on the other hand, this number is only about 28 per 100 nm. This decrease represents a reduction less than 50%. Because stacking fault formation in NP can lead to another type of crystal structure (WZ) which has different band structure, the carrier transport can be significantly modified because of carrier trapping and enhanced scattering, given a high stacking fault density[31,32]. Therefore, this significant reduction in stacking fault formation can potentially improve the NP properties.

5.3.2 Spectral analysis of InAsSb nanopillars

In order to further confirm Sb incorporation and determine the composition of InAsSb NPs, spectral analysis is performed by reflectivity measurement in the mid-IR wavelength range.

Reflectivity measurement is done by focusing the IR light onto the NP array through an IR microscope that is connected to a fourier transform infrared spectrometer (FTIR) with a KBr beam splitter and a liquid nitrogen cooled MCTA detector. The spot size is adjustable and can be as small as 10 μm^2, which is smaller than the size of the NP array (50 μm^2), hence ensuring accurate measurement. All the measurements are performed using an InAs substate as reference.

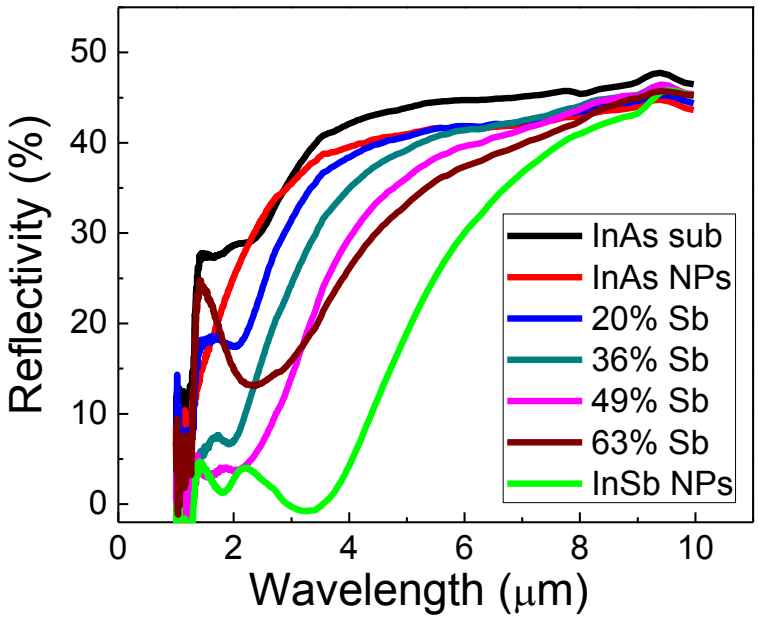

Figure 5.10: Reflectivity measurement of an InAs substrate and different NPs to determine the absorption cutoff of each NP.

The resulting reflectivity measurements, done at room temperature and in a nitrogen gas purged environment, are shown in Fig. 5.10. Also included in the same figure are the reflectivity measurements from an (111)B InAs substrate, pure InAs NPs and InSb NPs for comparison. The Sb% shown in the figure represents the percentage in the gas phase during growth. Clearly, the InAs substrate and NPs exhibit similar cutoff just above 3 μm, corresponding to the InAs band-

gap. When Sb is introduced to form InAsSb NPs, the cutoff wavelength increases from around 3.5 μm (20% Sb) to 4 μ (36% Sb) and saturates at just over 4.2 μm (49% and 63% Sb). This wavelength corresponds to a maximum Sb content of approximately 20% in the solid phase, even with further increase in the gas phase. This limitation is likely posted because of the relative high growth temperature at 590˚C. Since the melting temperature of InSb is 530˚C, a high Sb content in the InAsSb solid leads to material desorption. It is speculated that by lowering the growth temperature, higher Sb % should be attained.

5.4 Summary

Selective-area InSb nanostructures have been achieved using a self-catalyzed approach[33]. Without the In droplet, it is extremely difficult to form NPs because the energetically favored surfaces prefer other growth directions. With an initial In droplet formation, axial growth is achieved, and with a two-step V/III ratio growth to engineer the droplet size, InSb NPs with higher aspect ratio are demonstrated.

Even with such achievement, pure InSb growth still lack uniformity and controllability. As a result, InAsSb growths are investigated and the growth conditions to achieve high aspect ratio, uniform NP array is found. Structural analysis shows a dramatic reduction in stacking fault density even with only 20% Sb in the solid phase. Spectral analysis by reflection spectroscopy shows the tunability of Sb content up to 20% even with increasing percentage in the gas phase. This limitation is likely because of the high growth temperature used; InSb has a low melting temperature of 530˚C.

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Chapter 6

Conclusions and future outlook

6.1 Overview

This chapter summarizes the important and significant findings of this dissertation, which can be generalized into three sections. The first part focuses on the impacts surface states have on III-V nanopillar (NP) transport and the importance of a robust surface passivation technique. The second part discusses the efforts and outcomes of achieving different heterostrucutres in III-V NPs, including different growth methods. The third part presents the research effort towards antimonide-based NP development. Finally, building upon the work of this dissertation, the last section proposes some future research directions and outlook.

6.2 Surface passivation in nanopillars

The effects of surface states can play a prominent role in determining NP properties. In Chapter 2, the impacts of surface states on p-type GaAs NPs (Zn doping), are investigated by extracting the transport parameters from single-NP field-effect transistors (FETs) across different NP diameter[1]. It is found that the field-effect mobility and normalized resistance are both highly dependent on NP dimension. A semi-empirical model based on varying mobility is employed to extract the actual doping levels as well as the surface state density, which is found to be 5×10^{12} $cm^{-2}eV^{-1}$ without any surface treatment. Both ex-situ and in-situ passivation methods yield

similar results to improve the transport parameters as they become insensitive to dimension change after the treatment. Ex-situ chemical passivation by immersing the NPs in ammonium sulfide solution, however, shows device performance degradation after a few measurements. On the other hand, in-situ passivation by growing a thin InGaP shell around the GaAs core proves to be a reliable approach as the devices stay consistent. The same semi-empirical model is employed and the surface state density after passivation is found to decrease almost two orders of magnitude to 7×10^{10} $cm^{-2}eV^{-1}$ after passivation.

Similar to GaAs, InAs NP transport properties are investigated by studying single-NP FETs across different channel diameters[2]. The InAs channels, without any intentional doping during the NP growth, exhibit n-type channel characteristics. This is likely because the surface Fermi-level of InAs is pinned very close or even above the conduction band[3,4]. Again, without surface passivation, the field-effect mobility and resistivity are highly dependent on NP dimension. In-situ surface passivation is provided by growing a thin InP shell (~5nm), with an excellent crystal integrity despite the lattice mismatch. With the InP shell, the channel effective electron mobility becomes diameter independent and increases significantly to ~ 6,000 $cm^2/V\text{-}s$ with an unintentional doping level of 2×10^{17} cm^{-3}. The InAs/InP NP channels are then fabricated into vertical surround-gate FETs employing high-k Al_2O_3 dielectric and sputtered surround W gate. Such device geometry provides much better electrostatic gate control compared to the single-NP FET design. The vertical surround-gate FETs show good DC characteristics with On/off ratio of 10^6, transconductance of 1.3mS/μm and subthreshold swing of 80mV/dec at a relative low supply voltage of 0.5V.

Overall, it is shown that a robust surface passivation scheme is essential to achieve reliable and consistent NP materials properties. With good surface passivation, these III-V

semiconductor NPs show their potentials as next-generation electronic devices as the constant device scaling down inevitably faces the physical limitations posted by silicon[5].

6.3 Heterostructures in nanopillars

Heterostructures in NPs provide the ultimate control in nano-bandgap engineering in all three dimensions and are of great interests for new types of devices and exploring novel device physics[6,7]. Because of the dimension of these structures and the precision required, an excellent control over the heterostructure formation and direction is of necessity. Achieving radial heterostructures has been demonstrated in the previous section for surface passivation. Having the same controllability and interface abruptness for axial heterostructures, however, has been historically elusive for selective-area epitaxy[8]. First attempt to realize purely axial InAs/InP NP utilizes a two-temperature growth technique where the InAs and InP segments have different growth temperatures. Single barrier structures with one InP insert inside the InAs NPs are demonstrated to show good interface quality and abruptness. They are also fabricated into single NP device and measured at different temperature and the conduction band offset, based on the thermionic emission model, is extracted to be 420 meV. By repeating this two-temperature growth twice, double barrier structures are also developed and with another radial InP shell to passivation the surface, they exhibit resonant tunneling behavior at cryogenic temperature (77K) with a peak-to-valley ratio of 1.7.

The problems posted by the two-temperature growth, however, reside within the inherent temperature control instability of the system during growth, which ultimately leads to non-uniform NP array and heterostructure formation. This is further magnified when attempting multiple stacks of inserts as the temperature change increases. As a result, another approach to

realize purely axial heterostructure under the same temperature is investigated. First instead of using pure InP as barrier material, InAsP (P=20-60% in gas phase) is employed to promote more axial growth relative to radial growth. Then, after growth completion, in-situ chloride etching is introduced inside the growth chamber before cooling down. Because only the sidewalls are exposed, this effectively etches the undesirable shell formed during heterostructure growth to achieve purely axial structure[9]. The InAsP barrier can be as thin as only 4 nm with roughness (<1nm) below the measurement resolution. Overall, the in-situ chloride etching technique has proven to be a very attractive and viable solution to achieve purely axial heterostructures, which can lead to precise control over radial and axial heterostructures.

6.4 Antimonide-based nanopillars

Antimonide-based materials have always attracted a lot of attention because of their immense potential in high-speed electronics and mid-IR optoelectronics. Their development, however, has been hampered by a lack of suitable epitaxial platform. Advancement in NP heteroepitaxy has allowed them to be synthesized on other lattice-mismatched, yet readily available substrates. Selective-area InSb nanostructures have been achieved using a self-catalyzed approach[10]. Without the In droplet, it is extremely difficult to form NPs because the energetically favored surfaces prefer other growth directions. With an initial In droplet formation, axial growth is achieved, and with a two-step V/III ratio growth to engineer the droplet size, InSb NPs with higher aspect ratio are demonstrated.

Even with such achievement, pure InSb growth still lack uniformity and controllability. As a result, InAsSb growths are investigated and the growth conditions to achieve high aspect ratio, uniform NP array is found. Structural analysis shows a dramatic reduction in stacking fault

density even with only 20% Sb in the solid phase. Spectral analysis by reflection spectroscopy shows the tunability of Sb content up to 20% even with increasing percentage in the gas phase. This limitation is likely because of the high growth temperature used; InSb has a low melting temperature of 530˚C.

6.5 Future research and outlook

The work presented in this dissertation has set the foundation for some promising future research directions. First, because of the energy dissipation constraints, further Si transistor shrinking is approaching its physical limits as the leakage current inevitably increases, leading to higher supply voltage and more power consumption. One promising solution is to replace the channel material with a higher carrier mobility to achieve the same performance with lower power. The III-V vertical surround-gate FETs investigated here (InAs/InP) already show excellent DC device performance with a long gate length (~230 nm). developing a reliable method to control and scale down the gate length can improve the device even further. Other than n-type channel, realizing p-type channel in this material combination should also be explored to take advantage of the fully complementary logic device design. This can be potentially achieved by doping the InP shell to pin the Fermi-level of InAs core close to the valence band to make it p-type[11]. Furthermore, porting such a high-mobility device onto silicon platform can significantly decrease the fabrication cost and to make it compatible with other existing Si technology.

The in-situ etching technique also proves to be a viable pathway to synthesize purely axial InAsP/InAs heterostructures to make more intricate and interesting quantum structures in the NPs. Extremely thin InAsP barriers (3-4 nm) have already been achieved and by further

fine-tuning the InAs well thickness down to approach the Bohr radius of InAs, quantum well (QW) or even quantum dot (QD) in NP can be realized. Because this is a one-temperature growth with good control over uniformity and heterostructure formation, stacking multiple heterostructures should be an attainable goal. Some very promising devices that can benefit significantly from such NP heterostructures include NP avalanche photodetectors, QW- or QD-infrared detectors, and quantum cascade lasers (QCLs).

Historically, InSb and InAsSb have been very difficult materials to grow. With the framework established in this dissertation, however, some promising growth techniques to achieve high-quality antimonide-based NPs can be explored. In order to incorporate more Sb in the InAsSb NPs, a temperature decrease from the current one is inevitable. The growths, however, tend to become heavily clustered or deformed with decreasing temperature. A two-temperature growth, first to ensure good InAs seeding quality at a higher temperature followed by a subsequent InAsSb growth at lower temperature can be investigated. The preliminary results show a decrease in clustering density and NP growth with some non-uniformity. Fine tuning such an approach could be a possible direction.

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