Title
Silicon and Silicon Carbide Nanowires: Synthesis, Characterization, Modification, and Application as Micro-Supercapacitor Electrodes

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Silicon and Silicon Carbide Nanowires: Synthesis, Characterization, Modification, and Application as Micro-Supercapacitor Electrodes

By

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University of California, Berkeley

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Professor Liwei Lin

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Abstract

Silicon and Silicon Carbide Nanowires: Synthesis, Characterization, Modification, and Application as Micro-Supercapacitor Electrodes

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Doctor of Philosophy in Chemical Engineering

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Professor Roya Maboudian, Chair

For applications in mobile and remote sensing platforms, microsupercapacitors are attractive energy storage devices due to their robust lifetimes and high specific power capacity. Utilization of green electrolytes in these devices reduces environmental impact and simplifies packaging by avoiding the stringent oxygen and moisture free conditions required for organic and ionic liquid based electrolytes. Porous silicon nanowire based microsupercapacitor electrode materials are promising for on-chip applications using an environmentally benign aqueous electrolyte, 1 M KCl, however they are prone to oxidation. A silicon carbide coating was found to mitigate this issue. The fabrication techniques, involving low-temperature electroless etching of silicon, are compatible with current integrated circuit processing methods and may be readily integrated at the micro-device level. The electrode materials are in good electrical contact with the underlying substrate and require no additional current collector. The base porous silicon nanowires are coated with a thin silicon carbide passivation layer by low pressure chemical vapor deposition. The demonstrated capacitance of the electrode materials, ~1700 $\mu F/cm^2$ projected area, is comparable to other carbon based microsupercapacitor electrodes, remains stable over many charge/discharge cycles, and maintains capacitive behavior over a wide range of charge/discharge rates.

An improved passivation method for the porous silicon nanowires has also been developed. The selective coating procedure deposits an ultra-thin (~ 1-3 nm) carbon sheath over the nanowires and passivates them. The ultra-thin nature of the coating enables solvent access to the pore area and hence a large improvement of active specific surface over the SiC coated PSiNWs discussed above. The electrochemical performance of these coated nanowires is characterized in both an aqueous electrolyte and an ionic

liquid electrolyte. Specific capacitance values reaching 325 mF cm^{-2} are achieved in ionic liquid, and calculations indicate that the theoretical maximum capacitance of the pristine wires is reached. TEM studies confirm the coating thickness and its conformality. Raman spectroscopy indicates that the carbon in the coating is mainly sp^2 hybridized, with corresponding high conductivity. At the time of writing, these materials represent the largest specific energy microsupercapacitor electrode published. A test device is prepared and demonstrated powering an LED.

The testing results of silicon carbide (SiC) nanowires (NW) as an electrode material for micro-supercapacitors is described. SiC NWs are grown on a SiC thin film coated with a thin Ni catalyst layer via chemical vapor deposition. A specific capacitance of ~240 μF cm^{-2} is demonstrated. Charge-discharge studies demonstrate the SiC nanowires exhibit exceptional stability, with 95% capacitance retention after 2×10^5 charge/discharge cycles in an environmentally benign, aqueous electrolyte. Doping of the nanowires with nitrogen through the addition of 5 at% ammonia to the precursor gas flow rate improves the conductivity of the nanowire films by over an order of magnitude leading to increased power capabilities.

A method to transfer silicon and silicon carbide nanowire arrays to arbitrary substrates while maintaining electrical contact through the entire array is elucidated. The nanowires are grown on graphene sheets on SiO_2 coupons. The graphene acts as both the flexible material for maintaining structural continuity and electrical contact through the array during transfer. The SiO_2 acts as the sacrificial growth substrate which is etched after growth in order to release the nanowire/graphene hybrid. The nanowire/graphene hybrids are structurally characterized by XRD and electron microscopy. Good electrical contact is confirmed through testing of the SiCNW/graphene hybrids as supercapacitor electrode materials in an aqueous electrolyte. The specific capacitance, ~340 μF cm^{-2}, is similar to SiCNW arrays grown on oxide while the electrical conductivity is improved and cycling stability tests show less than a 1% decrease in capacitance after 10,000 cycles.

Acknowledgements

This document is the culmination of years of work during which I have had the good fortune to interact with many excellent researchers and teammates. I thank them all for their help in picking fruitful paths and spotting dead ends.

And for keeping me excited.

A special thanks to Roya, for believing I might just really like graduate school.

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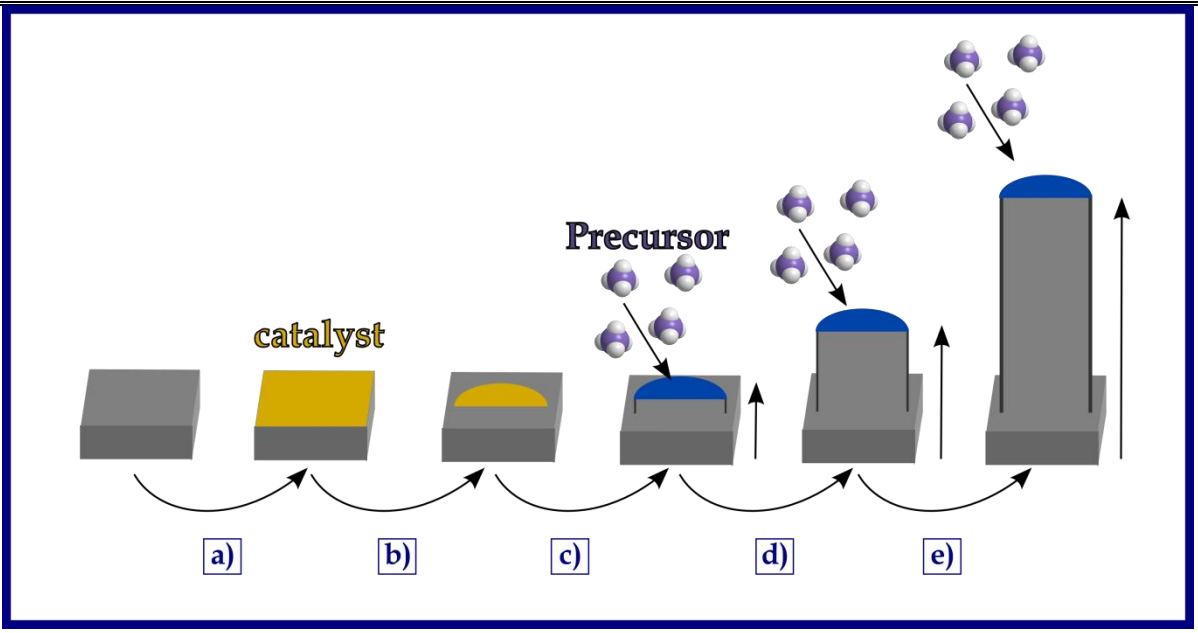
Chapter 1 – Overview: nanowires and supercapacitors

Introduction

Nano-materials represent a broad class of materials in which at least one dimension of the material is measured on the order of a nanometer. They may be characterized as 0-d (quantum dots) [1], 1-d (carbon nanotubes [2,3], nanowires [4]), 2-d (graphene) [5] or 3-d (buckminsterfullerene) [6] depending on the number of dimensions extending beyond the nanometer range. Over the past few decades nanomaterials have received much interest due to novel characteristics intrinsic to their nanoscale including magnetic, opto-electronic and thermal properties as well as increased reactivity [7]. For instance, quantum dots have been shown to exhibit size dependent band gap energies, resulting in size dependent coloration [8]. Nobler metals such as platinum have also been demonstrated to have size dependent reactivity and hence geometrically dependent catalytic properties [9]. Graphene exhibits ballistic electron transport and large scale sheets (~30 inch on the diagonal) can be produced with resistances as low as 125 $\Omega\ \square^{-1}$ [10]. Nanomaterials' geometries also results in high surface area to volume and surface area to mass ratios, termed specific surface area and measured described as either [area volume^{-1}] or [area mass^{-1}]. It is the latter characteristic of nanowires with which the following manuscript is mainly concerned, specifically for the high power density storage of electrical energy through capacitance. The results from the author's work on the synthesis, characterization and application of semiconductor nanowires as electrochemical double layer capacitor electrodes will be discussed. A hybridization scheme between graphene and semiconductor nanowires will also be described that takes the field a step closer towards integration of semiconductor nanowires with actual devices. This chapter will provide an overview as to what nanowires are and various methods of synthesizing them. Following that, electrochemical double layer capacitors will be described including their benefits and shortcomings as energy storage devices. Finally the driving forces behind their implementation on the microscale and the methods used to characterize them will be elucidated.

Nanowires

Nanowires are wire shaped materials 1-100's of nanometers in diameter, while being unconstrained in size in the axial direction. Due to their nanoscale, the properties of these materials may vary greatly from that of a bulk sample of the same material. At such scales, the surface states of the material begin to play an observable role in the electronic properties such as charge transport and trapping [11]. When one dimension of the nanowire approaches the wavelength of incident light, the material's optical response is affected [12]. Surface roughness approaching the order of the material's smallest dimension may have strong effects on reducing thermal transport [13]. Finally the extremely high aspect ratios which may be achieved with these materials, lead to



Scheme 1-1: A typical VLS based nanowire synthesis scheme. The process begins with a), the deposition of metal catalyst onto the growth substrate. In b) the substrate is heated to a temperature where the metal catalyst becomes molten. Precursors for the desired nanowire are added in c), which react on the catalyst surface and saturate the molten catalyst, forming a precursor/catalyst alloy. With continued addition of precursor the nanowire precipitates from the catalyst alloy and the nanowire extends in length through d) and e).

high surface area to volume ratios, difficult to obtain on the macroscale. As a result nanowires are an interesting area of study for a variety of applications including

catalysis [14], energy storage [15], energy generation [16] and sensing [17], where active materials' specific surface area plays a role in performance. The following work focuses on homogeneous semiconducting nanowires. For further reading on compound [18], metallic [19], metal oxide [20], and polymer [21] nanowires the reader is directed to relevant sources in the literature.

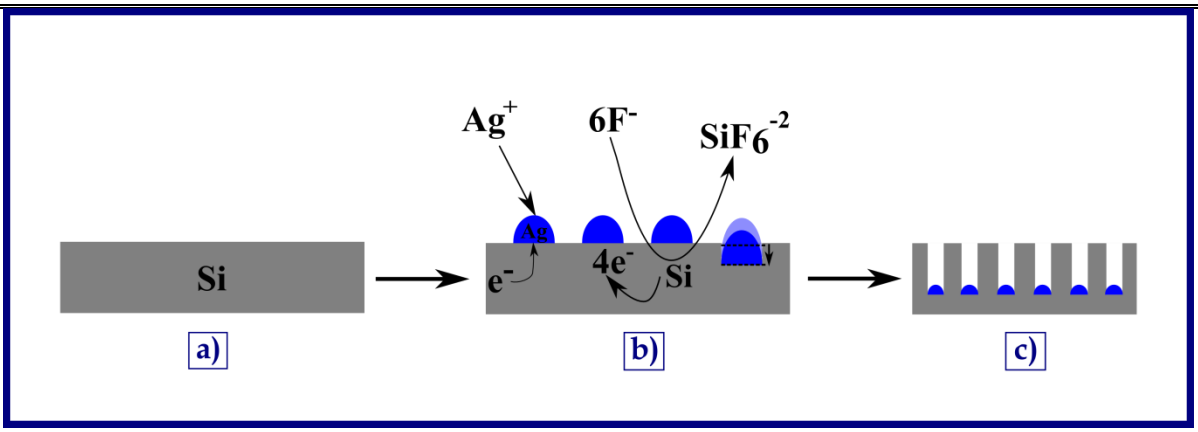
Nanowire synthesis - chemical deposition based

The growth of semiconductor nanowires began with the discovery of metal catalyzed growth from precursors in the vapor form in the 1960's [4]. The first step in this growth technique, known as vapor-liquid-solid (VLS) growth, is the deposition of nanoscale metallic films or droplets onto a growth substrate. The substrate is subsequently introduced into a furnace and heated to form nano-droplets of molten catalyst. A precursor containing the atoms of the desired nanowire's elemental composition is then introduced into the furnace. The precursor reacts on the surface of the molten catalyst, forming a semiconductor-metal alloy. Eventually with further addition of the precursor

the alloy droplet becomes supersaturated. Precipitation of the semiconductor nanowire then begins. Further addition of the precursor results in continued precipitation and growth of the nanowire structure. The process is summarized in Scheme 1-1. Visualization has confirmed VLS as the mechanism for growth through in situ electron microsopy [22]. To date the VLS method has been used to generate homogeneous semiconductor nanowires of numerous types with a variety of metal catalysts deposited through many techniques and employing a multitude vapor precursors. A summary of the rich variety of combinations used in VLS growth is provided by Werner et al. [23]. Since the initial discovery of VLS growth a number of other possible metal catalyzed chemical vapor nanowire synthesis mechanisms have been identified including vapor-solid-solid (where the catalyst remains solid), solution-liquid-solid (where the precursors are deposited from solution), and solid-liquid-solid (where the catalyst remains solid and the nanowire precursor material is in the solid phase) [24].

Control of nanowire arrangement on a surface is often desirable, rather than relying on the random arrangement obtained from blanket deposition catalyst deposition techniques. As the nanowires grow only from the metal catalyst in this mechanism, by patterning the catalyst onto the surface, control of the nanowire position and density is possible. For evaporated catalysts, lift-off techniques [25], nanosphere lithography [23], and shadow masking [26] are a few of the ways to control growth location and density. Catalysts deposited via electro- or electroless deposition have been patterned for both location and metal droplet spacing using membranes [27] and encapsulation of metal salt solutions in polymeric micelles [28] among other methods. Control of the electrical properties is also important for certain applications such as photovoltaics, and additional gases may be added to the vapor phase during growth for in situ doping [29], or post growth for ex situ doping [30]. Orientational control may also be achieved by judicious selection of the composition and crystallographic orientation of the underlying substrate [31,32], including epitaxial growth branching from other nanowires [33]. VLS is a truly versatile process which has yielded promising material for applications ranging from next generation transitors [26], to photovoltaics [34], and high frequency resonators [35]. One major drawback of the metal catalyzed VLS growth however is the incorporation of catalyst atoms into the final structure which may alter the electrical properties and hinder performance. For this reason a well thought out selection of the metal catalyst is important during initial process design, and is application dependent. In the following work silicon carbide nanowires have been studied using a single source precursor (methyltrichlorosilane, MTS) and a nickel catalyst film, which results in a dense array of nanowires with moderate electrical conductivity. In situ doping with ammonia has also been used to tune the electrical conductivity.

Nanowire synthesis - wet etch based



Scheme 1-2: A proposed mechanism for the wet etching of silicon nanowires with an in situ oxidant, Ag^+ ions. Silicon a), is immersed in a solution containing Ag^+ and F^- species in b). The Ag^+ ions extract electrons from the proximal silicon, oxidizing it and resulting in metallic Ag being deposited onto the surface. The F^- species react with the oxidized silicon, removing it from the wafer. The metallic Ag catalyzes further silicon oxidation resulting in continued etching of local silicon, and "sinking" of the Ag particles as shown in b). With time, a nanowire array is left, comprised of the unetched silicon, as in c).

Besides vapor deposition techniques, metal-catalyzed wet etching is another method for synthesizing silicon nanowires [36],[37]. Silicon is introduced into a bath containing an oxidant and a preferential silicon oxide etch, typically HF. Metal on the surface of the silicon catalyzes the oxidation reaction, increasing the local etch rate. The metal may be deposited ex situ (e.g. by evaporation, electro- or electroless deposition) or in situ using electroless deposition. In the former case the oxidant used during etching is typically H_2O_2 while in the latter case the oxidant is the metal salt and the arrangement of nanowires is based on the thermodynamics of the system. By varying oxidant and etchant ratios, silicon crystal orientation, silicon doping type (n- vs p-), and dopant concentration control of the resulting nanowires electrical properties, roughness, porosity, and tapering may be achieved [13], [36], [38], [39]. Templating methods, similar to those discussed above for chemical deposition based synthesis, are also viable options, however the negative of the metal pattern will be developed in the case of etching. As this work utilizes solely in situ catalyst deposition methods, that will be the focus of the rest of this discussion. For further reading on ex situ metal deposition and subsequent etching methods the reader is directed towards this helpful review [36].

Electroless deposition of metal onto silicon in the presence of HF to form large scale arrays of nanowires was first discussed in 2002 by Peng et al. [37]. Silver nitrate was utilized as the oxidant, resulting in Ag nanoparticles being deposited onto the surface and acting as a catalyst for further oxidation and subsequent etching, removing material in the immediate vicinity of the metal. A proposed mechanism is presented in Scheme

1-2, and adapted from [36]. As the etching continues, more silicon is removed from underneath the metal catalyst and thus the length of the wires may be controlled by total etching time. Finally, as the materials are exposed from the bulk of the substrate, they maintain the initial crystallography of the substrate. It should be noted that the exact mechanism and thermodynamics of the system have not yet been conclusively described in the literature.

Arrays of silicon nanowires formed in this way have been applied as photovoltaic structures [40], photocatalysts for water splitting [41], supercapacitor electrodes [15], field emission electrodes [42], and thermoelectrics [13]. Chapters 2 and 3 in this work will describe the synthesis of porous silicon nanowires from heavily boron doped p-type silicon with an in-situ metal catalyst/reductant etch bath, for application as supercapacitor electrode materials.

Supercapacitors

"Supercapacitor" is actually a term coined for a device storing electrical energy in the electrochemical double layer. Electrochemical double layer (ECDL) capacitor is the formal name of these devices. Based on the specific capacitance achievable with these devices in comparison to the standard parallel plate capacitor there is good reason to refer to them as supercapacitors or ultracapacitors (another common alternative). The first proposal of such a device came in the mid 20th century in the form of a patent awarded to Becker in 1957 in which was described a device storing energy in the ECDL formed at the interface between activated carbon in contact with an aqueous electrolyte [43]. Since then the use of organic electrolytes has been identified as a way of increasing the energy density of these devices by increasing the working voltage, as the total energy scales with the voltage (V) squared. Organic electrolytes with tetralkylammonium salts can operate in voltange ranges of 3.4-4 V vs. that of aqueous electrolytes with a working voltage range of ~1 V [43]. More recently focus has shifted to ionic liquids with even large stable voltage windows. Some may even approach 6V [44], although the toxicity and long term health hazards for these these novel electrolytes is still unknown.

While the reader is most likely familiar with the mechanism of electrical energy storage in batteries and parallel plate capacitors, the capacitance of the electrochemical double layer may be a new concept. It is thus worth comparing the operation of these various devices.

Comparison of batteries, parallel plate capacitors and supercapacitors

At the most fundamental level, in terms of purpose, batteries, parallel plate capacitors, and supercapacitors all function as electrical energy storage devices. Batteries do so

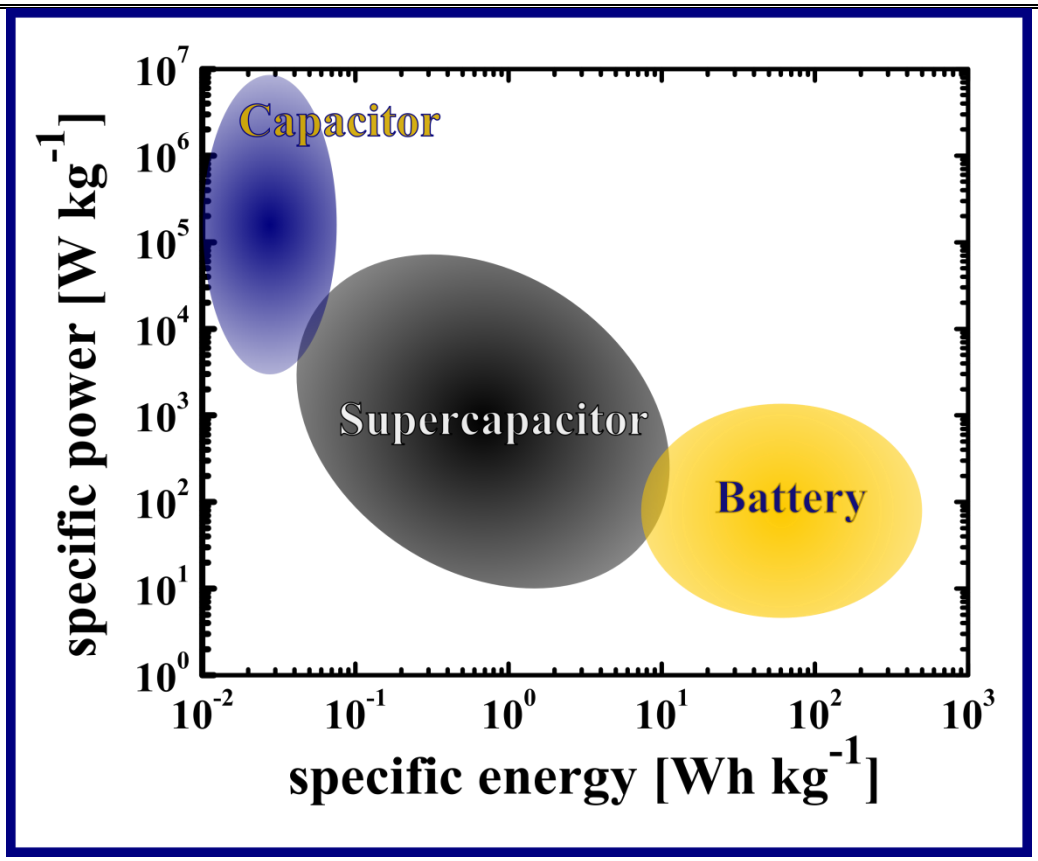


Figure 1-1: Ragone plot comparing the typical specific power and energy ranges of batteries, capacitors, and supercapacitors as extracted from [45].

through the pairing of electrochemical redox reactions, such as the well known Li-ion system, which occur at opposing electrodes. During discharge, metal species yield electrons to an external circuit, powering a load while traveling down the potential energy slope to the opposing electrode, where they recombine with metal ions in a thermodynamically favored arrangement. Charging is achieved by an external energy source forcing the reverse reaction. Thus electrical energy is stored in the chemical bonds of the charged electrode. Parallel plate capacitors on the other hand, store energy via electrostatics. Two plates, separated by a dielectric, are charged via an external energy source. Upon removal of the source, the charges are "stuck" on the plates until the circuit is completed by a load. The charges then recombine as they move down the potential energy slope, powering the load. In this case electrical energy is stored on the surface of the electrode, leading to more rapid discharge (higher power) than batteries, but lower total energy storage capabilities. ECDL capacitors are a bridging device, straddling the difference in energy and power density between capacitors and batteries, as depicted in the ragone plot in Figure 1-1. Supercapacitors are comprised of two

electrodes which are in contact with an electrolyte. Upon charging of the electrodes, the electrolyte becomes polarized, yielding a higher density of opposite charged ions at each electrode. In order to satisfy charge neutrality in the bulk of the solution, a second layer of counterions forms just outside of this region and this interphase between the electrode and the bulk is hence called the electrochemical double layer. Grahame's proposed model of 1947 is still used to describe this phenomena and the structure is

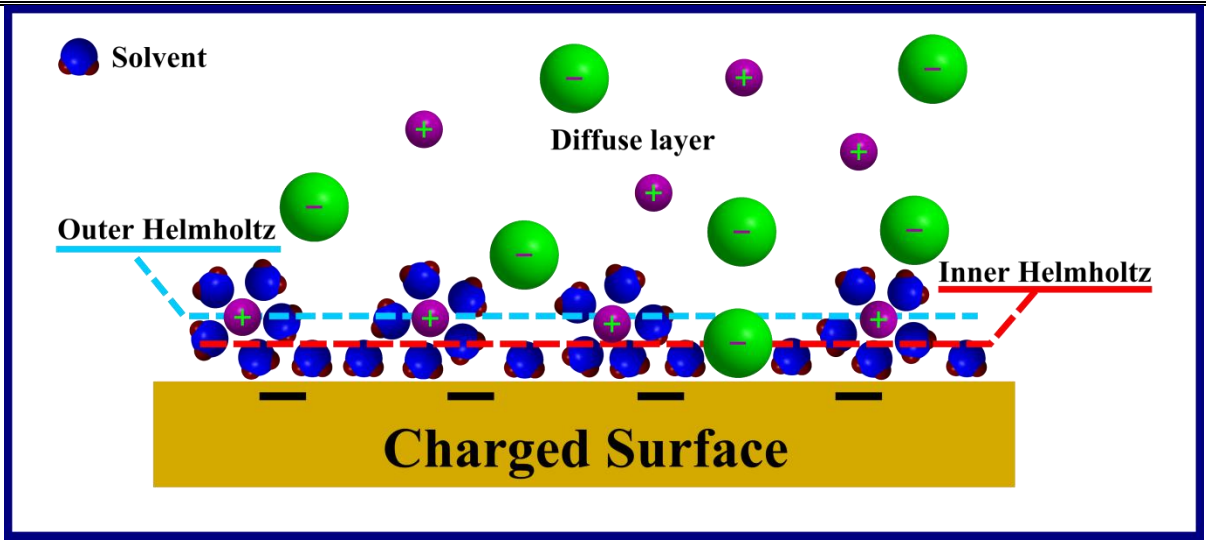


Figure 1-2: Visual description of the Grahame model for the electrochemical double layer, formed when a charged surface is in contact with an electrolyte solution [46]. Ions of the opposite charge are attracted to the surface. For charge neutrality an equal number of counterions form a second layer in close proximity, before the diffuse bulk is reached. The outer Helmholtz plane represents the closest approach for cations encapsulated by a solvation layer. The inner Helmholtz plane represents the plane of closest approach for specifically adsorbed anions. The solvent is not shown in the diffuse region for increased clarity.

depicted in Figure 1-2 [46]. The two labeled planes, inner and outer Helmholtz, refer to the plane of closest approach for the anion and cation respectively. Anions have a tendency to become specifically adsorbed onto electrode surfaces whereas cations are separated from the electrode at a further distance by a strong solvation layer. The plane of concentrated ions, opposing the charge on the electrode, represents a second "parallel plate" and gives rise to a capacitance which can be described in the same way as that of the double plate capacitor, given in Equation (1):

$$C = \frac{A}{d}\varepsilon\varepsilon_o \qquad (1)$$

Where C is the capacitance, A is the interfacial area, d is the separation distance between the two "plates", ε is the dielectric constant of the interlayer (or the adsorbed solvent

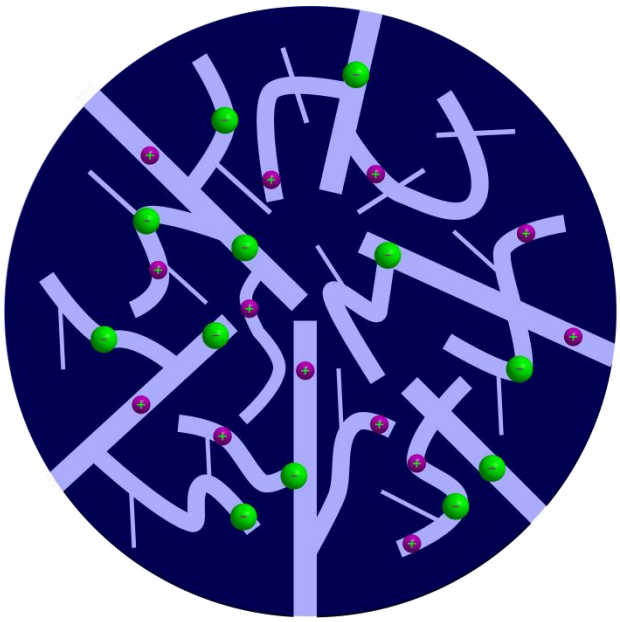


Figure 1-3: Depiction of magnified view into porous media typically utilized as supercapacitor electrode materials. Some pores are too small to allow ion penetration and thus will not actively participate in energy storage.

layer for a supercapacitor), and ε_o is the dielectric of a vacuum. Another important aspect of the supercapacitor design is that as the double layer forms at any surface which is wetted by the electrolyte. This enables the use of porous media with high specific surface areas. Various porous carbon materials, with specific surface areas ~1000 $m^2\ g^{-1}$, are typically employed due to their abundance, low cost, and reasonable conductivity [47]. It should be noted that the reported surface areas of these materials does not necessarily coincide with active area, as some pores will be too small to allow ion penetration, as depicted in Figure 1-3. The structure of the double layer has also been observed to change upon ion confinement in micropores (<1 nm in diameter), with substantial capacitance increases in capacitance measured in pores approaching the relevant ion's radius [48]. A rigorous new model to explain these phenomena has to date not been demonstrated.

By considering Equation (1), in comparison to a parallel plate capacitor, EDCL capacitors have a much larger potential area which is active and the distance between the "plates" is extremely small (~1 nm) [43]. For these reasons, supercapacitor is an accurate term, with specific capacitances reaching ~100x that of parallel plate capacitors. It may have occurred to the reader from this discussion, that a supercapacitor is actually two parallel plate capacitors in series. Indeed this is the case and the total capacitance is then given by equation (2):

$$1/C_{total} = 1/C_1 + 1/C_2 \qquad (2)$$

where C_1 and C_2 are the capacitances of the individual electrodes. This is an important point to remember and will be brought up again when the characterization methods for

these devices are discussed below. The total energy stored in a capacitor is proportional to the capacitance and is described by Equation (3):

$$E = 1/2CV^2 \quad (3)$$

where E is energy and V is the voltage window of discharge as limited by the electrochemical stability of the electrode material and electrolyte. Thus supercapacitors are able to store larger amounts of energy than parallel plate capacitors. However the charge and discharge cycles of supercapacitors require ion transport through porous media and results in added resistances. These are often modeled as set of series resistances (or transmission line resistance model) corresponding to the different size pores and these resistances result in real charge/discharge rate limitations [49]. The porous nature of supercapacitor electrodes then leads to lower power capabilities than those of parallel plate capacitors. A further discussion comparing the thermodynamics of the battery and supercapacitor systems may be found in Reference [45].

A final note in comparing these devices is that in capacitors and supercapacitors, all energy is stored via electrostatics and no degradation mechanism to the electrode is inherent to their operation as opposed to batteries which undergo chemical reactions and thus changes in electrode volume and morphology. Lifetimes of supercapacitors are subsequently ~1000x (in terms of number of charge/discharge cycles) that of batteries [43]. Due to their relatively high energy and power capabilities and their long cycle lifetimes, supercapacitors have been employed to date as backup power supplies, storage devices for regenerative braking systems and energy sources for fail-safe positioning devices [50].

Microsupercapacitors

Microelectromechanical system (MEMS) based remote sensors play an ever increasing role in human society including monitoring the structural health of major civil works, the physical health of human patients and the environmental presence of toxic or explosive compounds [51–53]. Integration of high power, robust, micro scale energy storage devices with these sensors is important in terms of device reliability, providing burst energy for data relay, and allowing for the continuing densification of components by reducing bulky external power sources. Micro-batteries based on 3-d architectures have been proposed for application in high-power devices and boast scalable energy capacity. However these devices have not yet been demonstrated to overcome typical battery failure modes resulting from material degradation during cycling [54]. Microsupercapacitors are attractive candidates to fill this important energy market due to their high specific power capacity and robust cycling stability (~10^6 cycles vs ~10^3 cycles for batteries) [55].

Microsupercapacitors typically utilize planar geometries and thus are able to achieve much smaller form factors than typical cylinder or box-like geometries. Several planar micro-supercapacitors have already been reported in the literature[15], [56–63]. A significant challenge to developing planar devices is integration of the electrode material. Activated carbon, which is the most common material used in macroscale supercapacitors, is difficult to integrate in planar technology, due to such issues as precise placement and the uniformity needed to pattern the electrode [57]. As a consequence, for on chip supercapacitor development, research has focused largely on nanomaterials. The development and testing of semiconducting nanowires synthesized via chemical deposition and wet etch methods microsupercapacitor electrodes will be discussed in detail in the upcoming chapters.

Supercapacitor performance characterization

The main figures of merit for supercapacitor materials are specific capacitance, specific energy, specific power, and cycling stability or lifetime. All may be tested utilizing straightforward techniques enabled by a basic electrochemical station. Namely the methods of cyclic voltammetry (CV), galvanostatic charge/discharge (GD) and impedance spectroscopy are used to quantify the performance metrics of supercapacitor materials. These tests may be performed in either a two-electrode or three-electrode configuration. In the latter a reference electrode is used to fix the potential over the working electrode (material being tested) while a current is applied or measured between the working and counter electrode (current sink). By having a separate reference, the electrochemical stability of the electrode/electrolyte can be probed at the same time as the specific capacitance of the electrode material under investigation. The two electrode configuration employs a symmetric (in this work) working and counter electrode, where the counter electrode acts a pseudo-reference, enabling the potential difference to be measured, but the true potential cannot be controlled. As an actual device is two electrodes it is the more accurate configuration for characterizing the energy and power characteristics of an actual supercapacitor comprised of the electrode materials being tested [64]. The two configurations are shown schematically in Figure 1-4.

Cyclic voltammetry

The method of cyclic voltammetry applies a constantly changing potential between the working and reference electrode, while monitoring the current between the working and counter electrode. The output is a plot of current vs. potential and the capacitance of the electrode material is calculated from Equation (4):

$$C = \frac{i}{dV/dt} \qquad (4)$$

where i is the measured current and dV/dt is the potential sweep rate. An ideal supercapacitor would thus result in a square wave current vs. potential plot. However in real ECDL capacitors the output deviates from this square wave in three typical ways [47]. The first is in current peaks at the high and low potential ranges, shown in Figure 1-5 a), which result from electrochemical instability of the electrode or electrolyte. Resistances in the material give rise to a skewing of the i-V relationship, depicted in Figure 1-5 b). If reversible redox reactions occur between the electrode and electrolyte,

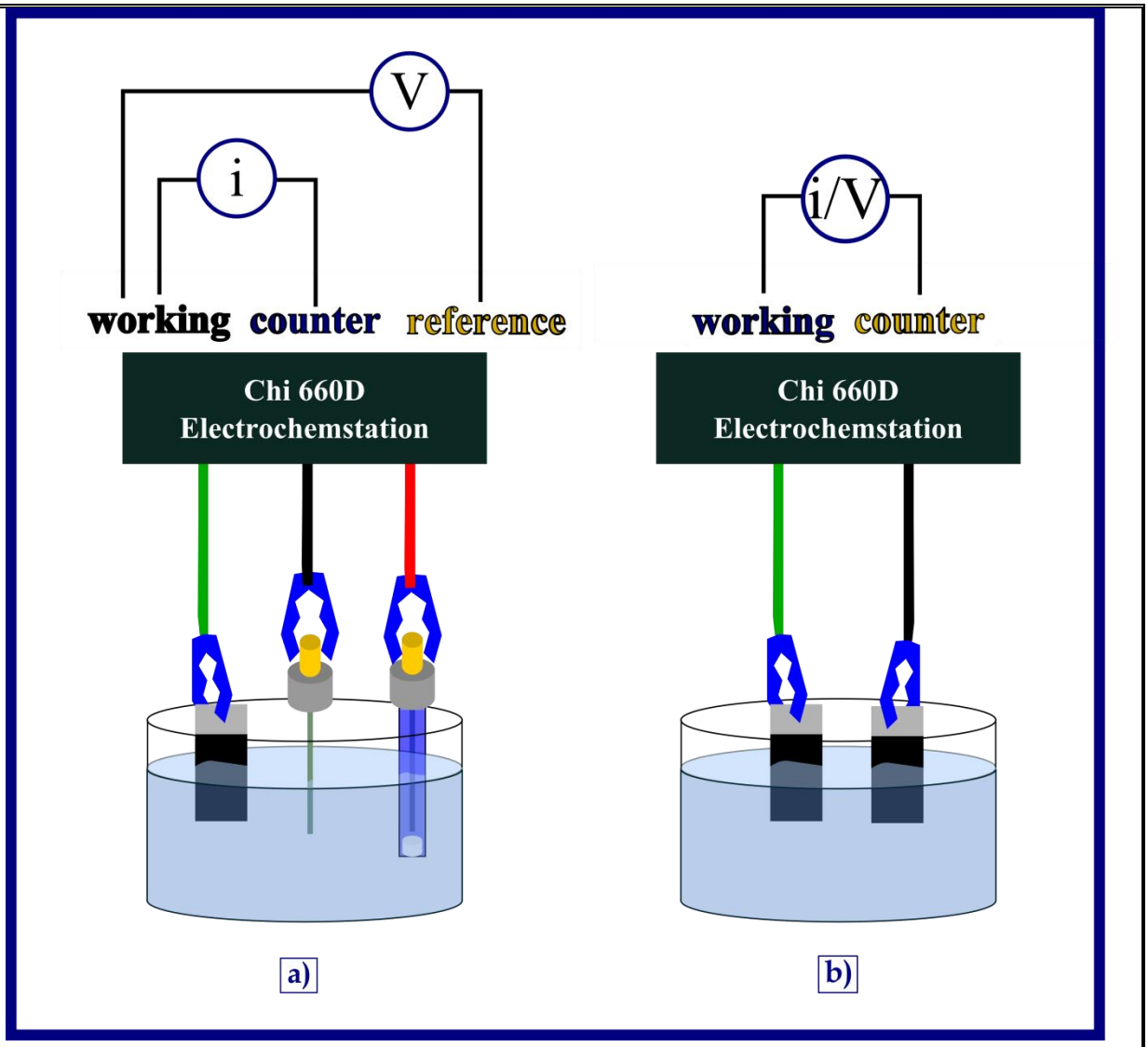


Figure 1-4: Comparison of three electrode a), and two electrode b), testing setups used for characterizing supercapacitor performance.

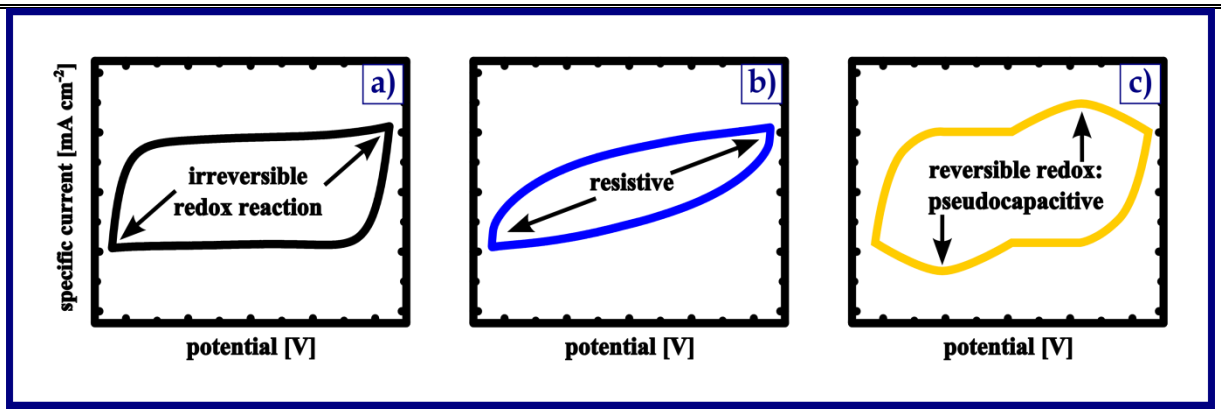


Figure 1-5: Description of different deviations from ideality typical during CV measurements of supercapacitors including a) Irreversible redox reactions, b) resistive behavior, and c) reversible redox reactions which contribute to energy storage.

this can result in a CV such as that in Figure 1-5 c), increasing the total energy storage capabilities of the system through the phenomenon called pseudocapacitance. Although this subject is not directly related to the work described herein, Conway's monograph contains a thorough discussion on the topic [43].

Analysis of CV results, in the face of non-idealities, may be performed with three different methods which can yield different results for capacitance. One may chose a single potential at which to analyze the current and through a judicious choice, avoid including contributions from faradaic reactions occurring during the voltage sweep. Averaging the current over the forward and reverse scans is a second choice and

averaging the current over the reverse scan direction (i.e., discharging) is a third. These are summarized in Table 1-1. In the following work, in an effort to characterize the pure double layer capacitance of the material, a single potential is chosen at which the current is used to determine capacitance.

It should be recognized that when performing this measurement in the three-electrode configuration, the capacitance measured is that for a single electrode. A device comprised of two of these electrodes would hence have a total capacitance, in the case that they are completely symmetric, of 1/2 that of a single electrode, based on Equation (2). Normalization of the capacitance calculated is important for being able to rationally compare different materials' performance. For microscupercapacitors, the typical metric utilized is capacitance per projected area, as the area occupied on a chip is the most relevant for on chip applications. It should be stated clearly whether the capacitance being reported is based on a three or two electrode method and whether the projected area is that of the total device or the active electrode material, so that accurate comparisons can be made.

Cycling stability may be determined utilizing CV. If CV is used, it should be conducted over the entire voltage window and at a relevant scan rate to operation. This will ensure that the results accurately represent the lifetime of the materials under expected use conditions.

Table 1-1

Method	Equation	Description
Current at a single potential	$C = \frac{i\|_{V=x}}{dV/dt}$	**Enables the calculation of capacitance based purely on double layer contributions.**
Average current over entire scan	$C = \frac{i_{forward\ avg} + i_{reverse\ average}}{2\ dV/dt}$	**Includes both pseudocapacitive and irreversible faradaic reactions**
Average over discharge scan	$C = \frac{i_{reverse\ average}}{dV/dt}$	**Includes both pseudocapacitive and irreversible faradaic reactions. May closer resemble capacitance achieved during discharge**

Galvanostatic charge/discharge

In GD a constant current is applied between the working electrode and the counter electrode, while the potential over the working electrode is measured. Threshold high

and low potentials are also set. When the system reaches these, the polarity of the current is reversed. The typical output for this technique is a plot of potential vs. time and an ideal supercapacitor yields a sawtooth potential-time relationship as shown in Figure 1-6 a). Common deviations from ideality include a vertical region upon reversal of the current polarity, shown in Figure 1-6 b), which is a result the sum total of resistances through the supercapacitor and is referred to as the IR drop accordingly. Analysis of this feature enables computation of the equivalent series resistance, or ESR, which includes the contributions from ionic resistance in the electrolyte, transport resistance in the porous media, electronic resistance in the electrode material and any resistances through the external circuit [43]. When determining the ESR from this method it should be calculated using Equation (5):

$$ESR = \Delta V_{IR}/I \qquad (5)$$

where I is the absolute current being applied and . This value should be checked for consistency by utilizing results from a variety of current values [65]. A second deviation from ideality is curvature in the potential-time relationship, depicted in Figure 1-6 c), which is a result of redox reactions occurring during charge or discharge [65].

Capacitance may be calculated from GD results utilizing Equation (4) where dV/dt is now the average over the entire discharge. GD is also the preferred method for calculating energy and power density as the ESR, and thus power limitations, are accounted for. Energy is calculated using Equation (3) and power may then be calculated by Equation (6):

$$P = E/t \qquad (6)$$

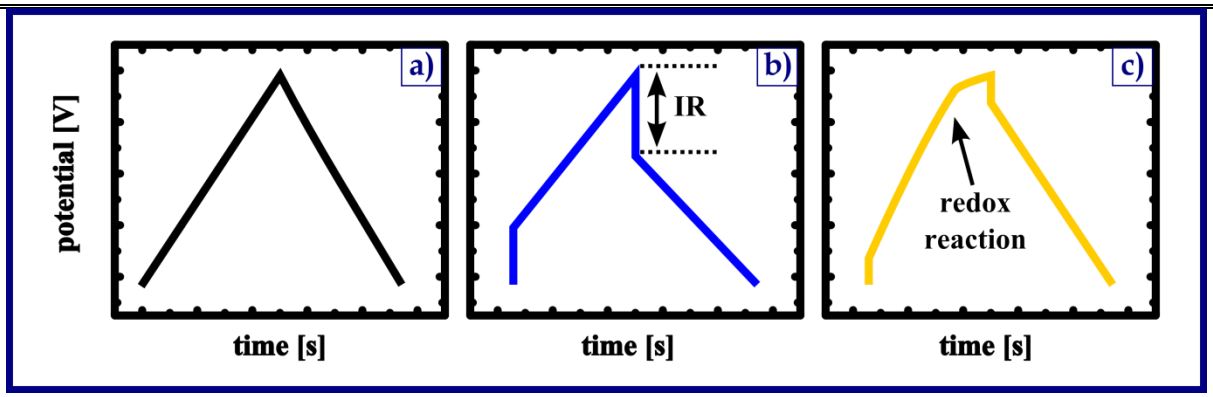


Figure 1-6: a) Ideal potential vs. time relationship obtained from galvanostatic testing of supercapacitors. b) Potential vs. time relationship obtained from galvanostatic testing of supercapacitors with resistive contributions. c) Potential vs. time relationship obtained from galvanostatic testing of supercapacitors with redox reactions occurring.

Where *P* is power and *t* is the time for discharge. Caution should be used when comparing the energy and power results for supercapacitor materials tested in two vs. three electrode systems as even the configuration of electrodes has been shown to effect these results [66]. As with normalized capacitance reporting energy and power "density" as per projected area of the device is typical in the literature.

GD may also be used to determine lifetime stability. During these tests the full voltage range should be utilized and the current applied should be relevant to expected operational conditions.

Impedance spectroscopy

This method applies an AC current between the working electrode and counter electrode over a narrow potential range. The results are then typically plotted as a nyquist or bode plot and various models have been proposed in order to relate the results to properties of the supercapacitor system including ionic resistance of the electrolyte and ESR. This method is not utilized in the current work as the relevant properties of the materials tested were well characterized by CV and GD. However it is mentioned for completeness as it is often reported in the supercapacitor literature. For more information on the technique and interpretation the reader is directed to the relevant literature [43].

Summary

Nanowire synthesis methods provide a wealth of new materials which are attractive for energy storage applications as a result of their geometrically dependent properties. Microsupercapacitors are extremely promising energy storage devices to bridge the energy and power gap between batteries and capacitors, and for implementation in distributed sensor networks and other MEMS applications where moderate energy, high power and high reliability are required. The following chapters will be concerned with the synthesis of nanomaterials and their characterization, both in terms of physico-chemical traits and energy storage performance.

References

[1] A. I. Ekimov, A. L. Efros, and A. A. Onushchenko, "QUANTUM SIZE EFFECT IN SEMICONDUCTOR MICROCRYSTALS," *Solid State Communications*, vol. 56, no. 11, pp. 921–924, 1985.

[2] L. V. Radushkevich and V. M. Lukyanovich, "O strukture ugleroda, obrazujucegosja pri termiceskom razlozenii okisi ugleroda na zeleznom kontakte," *Zurn Fisic Chim*, vol. 26, pp. 88–95, 1952.

[3] M. Monthioux and V. L. Kuznetsov, "Who should be given the credit for the discovery of carbon nanotubes?," *Carbon*, vol. 44, no. 9, pp. 1621–1623, Aug. 2006.

[4] R. S. Wagner and W. C. Ellis, "VLS mechanism of single crystal growth - Wagner and Ellis - APL - 1964.pdf," *Applied Physics Letters*, vol. 4, no. 5, pp. 89–90, 1964.

[5] K. S. Novoselov, "Electric Field Effect in Atomically Thin Carbon Films," *Science*, vol. 306, no. 5696, pp. 666–669, Oct. 2004.

[6] H. W. Kroto, J. R. Heath, S. C. O'Brien, R. F. Curl, and R. E. Smalley, "C60: Buckminsterfullerene," *Nature*, vol. 318, pp. 162–163, 1985.

[7] R. Vajtai, *Springer Handbook of Nanomaterials*. Dordrecht Heidelberg London New York: Springer, 2013.

[8] L. Brus, "Quantum crystallites and nonlinear optics," *Applied Physics A*, vol. 53, no. 6, pp. 465–474, 1991.

[9] R. K. Sharma, P. Sharma, and A. Maitra, "Size-dependent catalytic behavior of platinum nanoparticles on the hexacyanoferrate(III)/thiosulfate redox reaction," *Journal of Colloid and Interface Science*, vol. 265, no. 1, pp. 134–140, Sep. 2003.

[10] S. Bae, H. Kim, Y. Lee, X. Xu, J.-S. Park, Y. Zheng, J. Balakrishnan, T. Lei, H. Ri Kim, Y. I. Song, Y.-J. Kim, K. S. Kim, B. Özyilmaz, J.-H. Ahn, B. H. Hong, and S. Iijima, "Roll-to-roll production of 30-inch graphene films for transparent electrodes," *Nature Nanotechnology*, vol. 5, no. 8, pp. 574–578, Aug. 2010.

[11] T. Hanrath and B. A. Korgel, "Influence of Surface States on Electron Transport through Intrinsic Ge Nanowires," *The Journal of Physical Chemistry B*, vol. 109, no. 12, pp. 5518–5524, Mar. 2005.

[12] R. Agarwal and C. M. Lieber, "Semiconductor nanowires: optics and optoelectronics," *Applied Physics A*, vol. 85, no. 3, pp. 209–215, Oct. 2006.

[13] A. I. Hochbaum, R. Chen, R. D. Delgado, W. Liang, E. C. Garnett, M. Najarian, A. Majumdar, and P. Yang, "Enhanced thermoelectric performance of rough silicon nanowires," *Nature*, vol. 451, no. 7175, pp. 163–167, Jan. 2008.

[14] M. Wang, X. Wang, J. Li, and L. Liu, "In situ synthesis of 3D platinum nanoflowers on porous silicon for monolithic integrated micro direct methanol fuel cells," *Journal of Materials Chemistry A*, vol. 1, no. 28, p. 8127, 2013.

[15] J. P. Alper, M. Vincent, C. Carraro, and R. Maboudian, "Silicon carbide coated silicon nanowires as robust electrode material for aqueous micro-supercapacitor," *Applied Physics Letters*, vol. 100, no. 16, p. 163901, 2012.

[16] A. P. Goodey, S. M. Eichfeld, K.-K. Lew, J. M. Redwing, and T. E. Mallouk, "Silicon Nanowire Array Photoelectrochemical Cells," *Journal of the American Chemical Society*, vol. 129, no. 41, pp. 12344–12345, Oct. 2007.

[17] M. C. McAlpine, H. Ahmad, D. Wang, and J. R. Heath, "Highly ordered nanowire arrays on plastic substrates for ultrasensitive flexible chemical sensors," *Nature Materials*, vol. 6, no. 5, pp. 379–384, May 2007.

[18] X. Duan and C. M. Lieber, "General synthesis of compound semiconductor nanowires," *Advanced Materials*, vol. 12, no. 4, pp. 298–302, 2000.

[19] Z. L. Wang, *Nanowires and Nanobelts: Materials, Properties and Devices - Metal and Semiconductore Nanowires*. New York: Springer, 2003.

[20] E. Comini, C. Baratto, G. Faglia, M. Ferroni, A. Ponzoni, D. Zappa, and G. Sberveglieri, "Metal oxide nanowire chemical and biochemical sensors," *Journal of Materials Research*, vol. 28, no. 21, pp. 2911–2931, Nov. 2013.

[21] S. Chen, Y. Li, and Y. Li, "Architecture of low dimensional nanostructures based on conjugated polymers," *Polymer Chemistry*, vol. 4, no. 20, p. 5162, 2013.

[22] Y. Wu and P. Yang, "Direct Observation of Vapor−Liquid−Solid Nanowire Growth," *Journal of the American Chemical Society*, vol. 123, no. 13, pp. 3165–3166, Apr. 2001.

[23] H. J. Fan, P. Werner, and M. Zacharias, "Semiconductor Nanowires: From Self-Organization to Patterned Growth," *Small*, vol. 2, no. 6, pp. 700–717, Jun. 2006.

[24] K. Kolasinski, "Catalytic growth of nanowires: Vapor–liquid–solid, vapor–solid–solid, solution–liquid–solid and solid–liquid–solid growth," *Current Opinion in Solid State and Materials Science*, vol. 10, no. 3–4, pp. 182–191, Jun. 2006.

[25] S. Han, W. Jin, T. Tang, C. Li, D. Zhang, X. Liu, J. Han, and C. Zhou, "Controlled growth of gallium nitride single-crystal nanowires using a chemical vapor deposition method," *Journal of materials research*, vol. 18, no. 02, pp. 245–249, 2003.

[26] V. Schmidt, H. Riel, S. Senz, S. Karg, W. Riess, and U. Gösele, "Realization of a Silicon Nanowire Vertical Surround-Gate Field-Effect Transistor," *Small*, vol. 2, no. 1, pp. 85–88, Jan. 2006.

[27] K.-K. Lew, C. Reuther, A. H. Carim, J. M. Redwing, and B. R. Martin, "Template-directed vapor–liquid–solid growth of silicon nanowires," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 20, no. 1, p. 389, 2002.

[28] G. S. Doerk, C. Dhong, C. Politi, I. Laboriante, C. Carraro, and R. Maboudian, "Micellar block copolymer templated galvanic displacement for epitaxial nanowire device integration," *Journal of Materials Chemistry*, vol. 21, no. 24, p. 8807, 2011.

[29] H. Schmid, M. T. Björk, J. Knoch, S. Karg, H. Riel, and W. Riess, "Doping Limits of Grown in <i/> situ Doped Silicon Nanowires Using Phosphine," *Nano Letters*, vol. 9, no. 1, pp. 173–177, Jan. 2009.

[30] G. S. Doerk, G. Lestari, F. Liu, C. Carraro, and R. Maboudian, "Ex situ vapor phase boron doping of silicon nanowires using BBr3," *Nanoscale*, vol. 2, no. 7, p. 1165, 2010.

[31] A. I. Hochbaum, R. Fan, R. He, and P. Yang, "Controlled Growth of Si Nanowire Arrays for Device Integration," *Nano Letters*, vol. 5, no. 3, pp. 457–460, Mar. 2005.

[32] S. J. Rathi, D. J. Smith, and J. Drucker, "Guided VLS Growth of Epitaxial Lateral Si Nanowires," *Nano Letters*, vol. 13, no. 8, pp. 3878–3883, Aug. 2013.

[33] D. Wang, F. Qian, C. Yang, Z. Zhong, and C. M. Lieber, "Rational Growth of Branched and Hyperbranched Nanowire Structures," *Nano Letters*, vol. 4, no. 5, pp. 871–874, May 2004.

[34] T. Song, S.-T. Lee, and B. Sun, "Silicon nanowires for photovoltaic applications: The progress and challenge," *Nano Energy*, vol. 1, no. 5, pp. 654–673, Sep. 2012.

[35] X. L. Feng, R. He, P. Yang, and M. L. Roukes, "Very High Frequency Silicon Nanowire Electromechanical Resonators," *Nano Letters*, vol. 7, no. 7, pp. 1953–1959, Jul. 2007.

[36] Z. Huang, N. Geyer, P. Werner, J. de Boor, and U. Gösele, "Metal-Assisted Chemical Etching of Silicon: A Review: In memory of Prof. Ulrich Gösele," *Advanced Materials*, vol. 23, no. 2, pp. 285–308, Jan. 2011.

[37] K.-Q. Peng, Y.-J. Yan, S.-P. Gao, and J. Zhu, "Synthesis of large-area silicon nanowire arrays via self-assembling nanoelectrochemistry," *Advanced Materials*, vol. 14, no. 16, p. 1164, 2002.

[38] K. Peng, Y. Wu, H. Fang, X. Zhong, Y. Xu, and J. Zhu, "Uniform, Axial-Orientation Alignment of One-Dimensional Single-Crystal Silicon Nanostructure Arrays," *Angewandte Chemie International Edition*, vol. 44, no. 18, pp. 2737–2742, Apr. 2005.

[39] C. Chiappini, X. Liu, J. R. Fakhoury, and M. Ferrari, "Biodegradable Porous Silicon Barcode Nanowires with Defined Geometry," *Advanced Functional Materials*, vol. 20, no. 14, pp. 2231–2239, Jun. 2010.

[40] G. Fan, H. Zhu, K. Wang, J. Wei, X. Li, Q. Shu, N. Guo, and D. Wu, "Graphene/Silicon Nanowire Schottky Junction for Enhanced Light Harvesting," *ACS Applied Materials & Interfaces*, vol. 3, no. 3, pp. 721–725, Mar. 2011.

[41] Y. J. Hwang, A. Boukai, and P. Yang, "High Density n-Si/n-TiO_2 Core/Shell Nanowire Arrays with Enhanced Photoactivity," *Nano Letters*, vol. 9, no. 1, pp. 410–415, Jan. 2009.

[42] N. S. Das, D. Banerjee, and K. K. Chattopadhyay, "Enhancement of electron field emission by carbon coating on vertically aligned Si nanowires," *Applied Surface Science*, vol. 257, no. 22, pp. 9649–9653, Sep. 2011.

[43] B. E. Conway, *Electrochemical Supercapacitors: Scientific Fundamentals and Technological Applications*. New York: Springer, 1999.

[44] A. B. McEwen, H. L. Ngo, K. LeCompte, and J. L. Goldman, "Electrochemical properties of imidazolium salt electrolytes for electrochemical capacitor applications," *Journal of the Electrochemical Society*, vol. 146, no. 5, pp. 1687–1695, 1999.

[45] M. Winter and R. J. Brodd, "What Are Batteries, Fuel Cells, and Supercapacitors?," *Chemical Reviews*, vol. 104, no. 10, pp. 4245–4270, Oct. 2004.

[46] D. C. Grahame, "The electrical double layer and the theory of electrocapillarity," *Chemistry Reviews*, vol. 41, pp. 441–501, 1947.

[47] E. Frackowiak and F. Beguin, "Carbon materials for the electrochemical storage of energy in capacitors," *Carbon*, vol. 39, no. 6, pp. 937–950, 2001.

[48] J. Chmiola, "Anomalous Increase in Carbon Capacitance at Pore Sizes Less Than 1 Nanometer," *Science*, vol. 313, no. 5794, pp. 1760–1763, Sep. 2006.

[49] W. G. Pell and B. E. Conway, "Analysis of power limitations at porous supercapacitor electrodes under cyclic voltammetry modulation and dc charge," *Journal of Power Sources*, vol. 96, no. 1, pp. 57–67, 2001.

[50] R. Kötz and M. Carlen, "Principles and applications of electrochemical capacitors," *Electrochimica Acta*, vol. 45, no. 15, pp. 2483–2498, 2000.

[51] N. A. Tanner, J. R. Wait, C. R. Farrar, and H. Sohn, "Structural Health Monitoring Using Modular Wireless Sensors," *Journal of Intelligent Materials Systems and Structures*, vol. 14, no. 1, pp. 43–56, Jan. 2003.

[52] U. Kawoos, G. K. Mugalodi, M. R. Tofighi, S. Neff, and A. Rosen, "A permanently implantable intracranial pressure monitor - 2005.pdf," in *Proceeds of the IEEE*, 2005.

[53] T. K. Bhattacharyya, S. Sen, D. Mandal, and S. K. Lahiri, "Development of a wireless integrated toxic and explosive MEMS based gas sensor," in *VLSI Design, 2006. Held jointly with 5th International Conference on Embedded Systems and Design., 19th International Conference on*, 2006, p. 4–pp.

[54] D. R. Rolison, J. W. Long, J. C. Lytle, A. E. Fischer, C. P. Rhodes, T. M. McEvoy, M. E. Bourg, and A. M. Lubers, "Multifunctional 3D nanoarchitectures for energy storage and conversion," *Chemical Society Reviews*, vol. 38, no. 1, p. 226, 2009.

[55] P. J. Hall, M. Mirzaeian, S. I. Fletcher, F. B. Sillars, A. J. R. Rennie, G. O. Shitta-Bey, G. Wilson, A. Cruden, and R. Carter, "Energy storage in electrochemical capacitors: designing functional materials to improve performance," *Energy & Environmental Science*, vol. 3, no. 9, p. 1238, 2010.

[56] Y. Q. Jiang, Q. Zhou, and L. Lin, "Planar MEMS supercapacitor using carbon nanotube forests," in *Micro Electro Mechanical Systems, 2009. MEMS 2009. IEEE 22nd International Conference on*, 2009, pp. 587–590.

[57] D. Pech, M. Brunet, P.-L. Taberna, P. Simon, N. Fabre, F. Mesnilgrente, V. Conédéra, and H. Durou, "Elaboration of a microstructured inkjet-printed carbon electrochemical capacitor," *Journal of Power Sources*, vol. 195, no. 4, pp. 1266–1269, Feb. 2010.

[58] F. Liu, A. Gutes, I. Laboriante, C. Carraro, and R. Maboudian, "Graphitization of n-type polycrystalline silicon carbide for on-chip supercapacitor application," *Applied Physics Letters*, vol. 99, no. 11, p. 112104, 2011.

[59] C. Liu, Z. Yu, D. Neff, A. Zhamu, and B. Z. Jang, "Graphene-Based Supercapacitor with an Ultrahigh Energy Density," *Nano Letters*, vol. 10, no. 12, pp. 4863–4868, Dec. 2010.

[60] J. Chmiola, C. Largeot, P. L. Taberna, P. Simon, and Y. Gogotsi, "Monolithic Carbide-Derived Carbon Films for Micro-Supercapacitors," *Science*, vol. 328, no. 5977, pp. 480–483, Apr. 2010.

[61] M. Beidaghi and C. Wang, "Micro-supercapacitors based on three dimensional interdigital polypyrrole/C-MEMS electrodes," *Electrochimica Acta*, vol. 56, no. 25, pp. 9508–9514, Oct. 2011.

[62] J. W. Choi, J. McDonough, S. Jeong, J. S. Yoo, C. K. Chan, and Y. Cui, "Stepwise Nanopore Evolution in One-Dimensional Nanostructures," *Nano Letters*, vol. 10, no. 4, pp. 1409–1413, Apr. 2010.

[63] M. Beidaghi, W. Chen, and C. Wang, "Electrochemically activated carbon micro-electrode arrays for electrochemical micro-capacitors," *Journal of Power Sources*, vol. 196, no. 4, pp. 2403–2409, Feb. 2011.

[64] M. D. Stoller and R. S. Ruoff, "Best practice methods for determining an electrode material's performance for ultracapacitors," *Energy & Environmental Science*, vol. 3, no. 9, p. 1294, 2010.

[65] J. R. Miller and A. F. Burke, "Electric Vehicle Capacitor Test Procedures Manual." DOE, 1994.

[66] D. Pech, M. Brunet, T. M. Dinh, K. Armstrong, J. Gaudet, and D. Guay, "Influence of the configuration in planar interdigitated electrochemical micro-capacitors," *Journal of Power Sources*, vol. 230, pp. 230–235, May 2013.

Chapter 2 – Silicon carbide coated porous silicon nanowires as microsupercapacitor electrodes

Chapter Summary

For application in mobile and remote sensing platforms, microsupercapacitors are attractive energy storage devices due to their robust lifetimes and high specific power capacity. Utilization of green electrolytes in these devices reduces environmental impact and simplifies packaging by avoiding the stringent oxygen and moisture free conditions required for organic and ionic liquid based electrolytes. This chapter describes the development of silicon carbide coated porous silicon nanowire based microsupercapacitor electrode materials for on-chip applications using an environmentally benign aqueous electrolyte, 1 M KCl. The fabrication techniques described below, involving low-temperature electroless etching of silicon, are compatible with current integrated circuit processing methods and may be readily integrated at the micro-device level. The electrode materials are in good electrical contact with the underlying substrate and require no additional current collector. The base porous silicon nanowires, which corrode readily in an aqueous environment, are coated with a thin silicon carbide passivation layer by low pressure chemical vapor deposition. The demonstrated capacitance of the electrode materials, ~1700 $\mu F/cm^2$ projected area, is comparable to other carbon based microsupercapacitor electrodes, remains stable over many charge/discharge cycles, and maintains capacitive behavior over a wide range of charge/discharge rates.

Introduction

All silicon-based materials produced with low temperature methods using chemistries compatible with basic lithography techniques are promising in simplifying all aspects of processing and integration, making them an attractive electrode material for microsupercapacitors. As mentioned in the introductory chapter, high surface area and conductivity are two key requirements of an electrode material for use in these devices. Dense arrays of highly doped crystalline silicon nanowires (PSiNWs) in electrical contact with the underlying silicon meet both of these requirements. Previously PSiNWs produced via the well-established vapor-liquid-solid (VLS) mechanism were demonstrated as supercapacitor electrode material [1]. These were made porous by repeated Li-ion insertion and removal cycles, (i.e., Li-ion battery cycling) achieving specific surface areas of ~100 m^2/g. PSiNWs fabricated with a low-temperature, one-step electroless metal assisted etch technique discussed above [2], avoids the metal catalyst pre-seeding step and high temperature chemical vapor deposition growth

conditions required for VLS type wires, as well as the complexities associated with doping of bottom-up NWs. When the metal assisted etch is performed on a highly p-doped silicon wafer, the resulting nanowires are also porous with a specific surface area of ~340 m^2/g, a large improvement over the more complex VLS-battery cycling synthesis. Specifically here a wet etch using a one-step oxidant/etchant bath of $AgNO_3$ and HF respectively, at a bath temperature of 50 ^oC, is employed. It has been shown that this PSiNW production technique is compatible with standard lithography and patterning technologies [3]. Furthermore via increased etch time the nanowires are scalable to longer lengths and hence increased surface area and energy storage.

Experimental

PSiNW formation

The etching of the PSiNW arrays was performed using procedures previously published[2]. First p-type Si(100) coupons (single side polished, 1 cm x 1 cm, boron doped, 1 – 5 mΩ–cm), were pre-cleaned to ensure any contaminants such as dust, organic matter, and oxide would not be present. Surface contamination can lead to non-uniform etching by protecting the surface from the surrounding solution. The cleaning process follows a protocol where the coupons were first degreased through sonication for 10 minutes in acetone and then isopropyl alcohol. Subsequently the surface oxide was removed by a 10 minute immersion in 5 M HF. ***NOTE: HF is a highly toxic acid and should only be used after specific training on the hazards, protocol in case of spill or exposure, and safe working practices.** Residual organic matter removal by a 10 minute UV-Ozone treatment followed. A clean and oxide free surface was finally obtained by a second 10 minute immersion in 5 M HF. The unpolished sides were then protected from etching with a nylon based polymer resist. In addition, a thin strip at the top of the polished side was protected by the polymer resist for making later electrical contact. Electroless metal-assisted etching was performed in a 5 M HF/20 mM $AgNO_3$ (Fischer Scientific, >99.8%) aqueous solution, maintained in thermal equilibrium with a 50 ^oC water bath, for varying times. A clear plastic chemical splash guard was placed around the entire apparatus to mitigate any hazards of a spill during etching. The reaction apparatus is depicted in Figure 2-1. After etching the samples were dip rinsed in deionized water (DeIO, ~17.9 MΩ-cm) three times to wash off residual acid and metal salts. During the etching process a macroporous mat of Ag dendrites was deposited on the Si surface which was mechanically removed carefully by peeling. Samples were left free of residual Ag by immersion in ~3.5 M HNO_3. The end of this etching process was detected by a color change on the surface. Immediately after removal of the bulk silver, the nanowire arrays had a slight burnt orange color with

some silver spots. As soon as the surface was noticed to be uniformly dark grey, NO_3 etching was stopped. This point was of importance as continuing to expose the nanowire arrays to the nitric acid resulted in oxidation and dissolution of the array. Nanowire arrays were then washed with DeIO. The polymer resist was subsequently removed by acetone rinsing. Samples were held in acetone until subsequent cleaning and drying of the nanowires.

Cleaning and drying of the nanowires

Nanowires were cleaned of any oxide present in a dilute ~1.5M ethanolic HF solution (5:25 ethanol:DeIO by volume) for 10 minutes. This was done to ensure that the resulting nanowire arrays were in good contact electrical contact with the subsequent SiC coating, important in maximizing active surface area and resulting capacitance. The concentration of HF was chosen to reduce bubble formation on the surface and thus reduce delamination of the nanowire arrays. An ethanolic solution was utilized to ensure good wetting within the pores of the silicon nanowires which are superhydrophobic as shown in Figure 2-2.

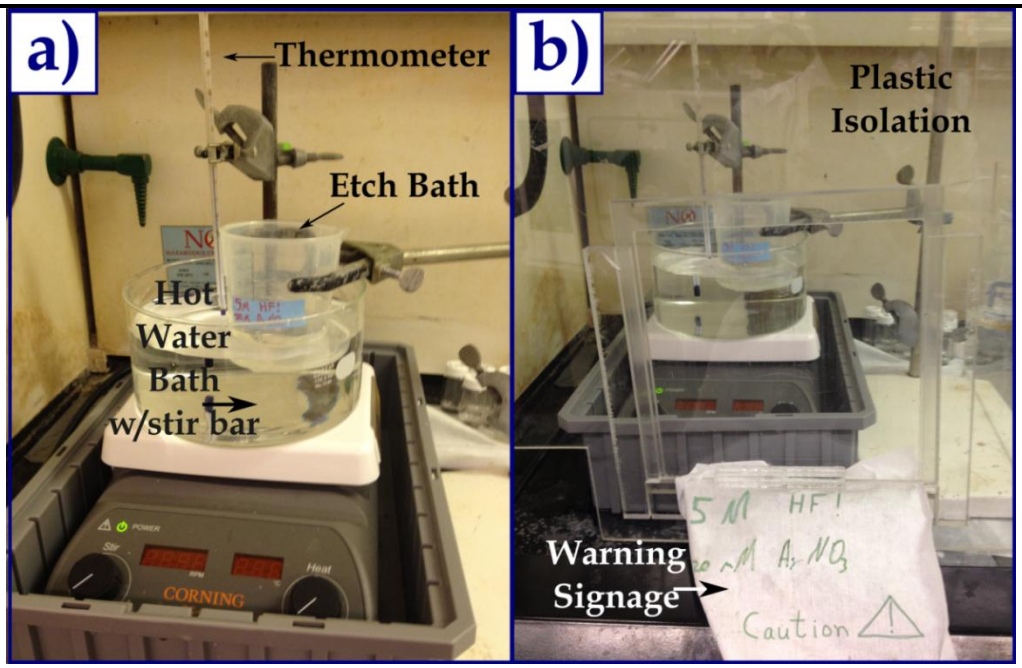


Figure 2-1: a) Image of etching reactor in hot water bath. A thermometer allows the hot water bath temperature to be monitored. b) Etching reactor behind plastic isolation with warning.

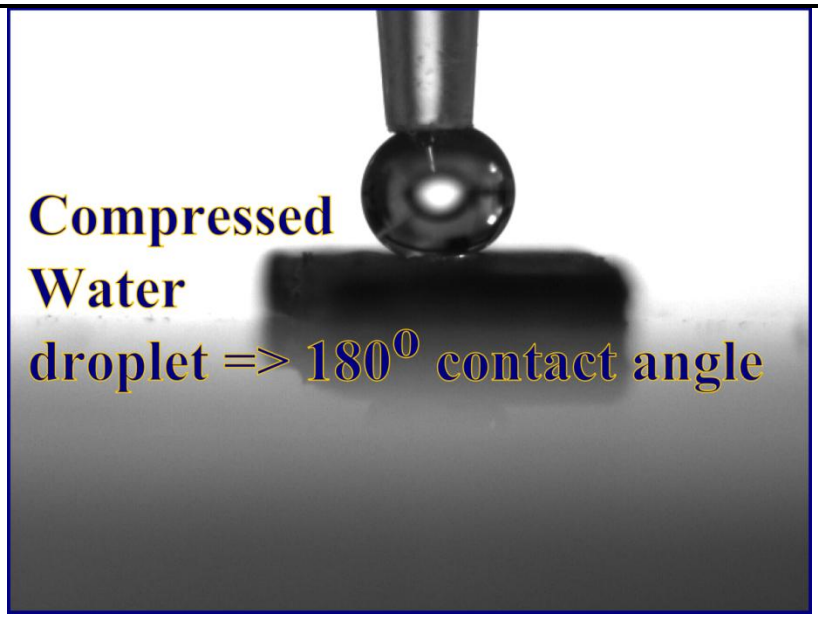


Figure 2-2: Image of water contact angle with PSiNW array. The drop would not transfer to the surface and compression of the drop against the array indicates superhydrophobicity.

After removal of the oxide, the nanowires were transferred into pure IPA and loaded into the critical point dryer. Critical point drying is the process of drying by going through the critical point of a liquid and into the supercritical fluid regime and then pumping out the critical fluid from the drying chamber. The purpose of CPD was to mitigate any meniscus formation during the drying process, as this can result in collapse of the nanowire structures into bundles. During standard drying, and subsequent meniscus recession between the nanowires, the resulting capillary forces pull the nanowires together, as observed in Figure 2-3 a). Critical point dried nanowires remain vertically aligned as shown in Figure 2-3 b). An excellent review of the mechanics underlying the collapse process may be found in Jansen, 1996 [4]. A tousimis AUTOSAMDRI®-815B, which utilizes CO_2 as the supercritical drying fluid at 1400 psi and 38 ^oC, was utilized for the critical point drying step.

SiC chemical vapor deposition

Polycrystalline SiC was deposited via a low-pressure chemical vapor deposition process utilizing a procedure described in detail elsewhere [5]. Growth was performed in a commercial LPCVD reactor (Tek-Vac CVD-300-M) utilizing 1,3 Disilabutane (DSB)

(Gelest Inc., >95% purity) as the SiC source. PSiNW samples were placed in the reactor immediately after oxide removal and drying. SiC deposition took place at 800 ^{o}C and 5 μTorr with a flow of 5 sccm DSB. Deposition time was varied from 30 seconds to 3 minutes corresponding to film thicknesses of 20 to 90 nm as measured on planar Si coupons coated alongside the PSiNW samples.

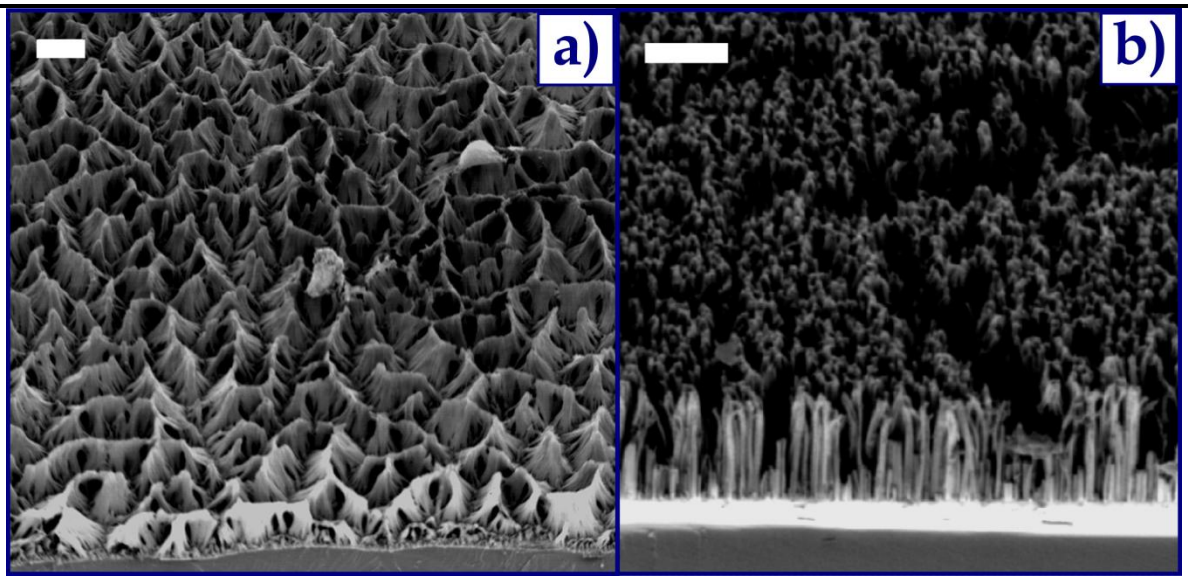


Figure 2-3: SEM images of PSiNW arrays. a) An array which was not supercritically dried. Visible clumping of the wires is due to collapse from capillary forces during drying. b) An array which was supercritically dried. Vertical alignment of the wires is maintained. Scale bars are 10 μm.

Physico-chemical PSiNW characterization

PSiNW morphology was characterized utilizing a NovelX mySEM scanning electron microscope. TEM images were acquired with a JEOL 2010 operated at 100 kV. Raman spectra were acquired with a HoribaJY LabRAM spectrometer in backscattering configuration with an excitation line provided by a HeNe laser (633 nm).

Capacitance testing

The electrical double layer capacitance of the resulting electrodes was analyzed utilizing cyclic voltammetry measurements in a 3 electrode configuration consisting of a

platinum wire counter electrode and an Ag/AgCl reference electrode. The nanowire arrays acted as the working electrode. Electrical connection was made directly to the sample in the planar region protected from PSiNW etching. Measurements were performed utilizing a Chi Instruments Electrochemical Analyzer 600D. Scans were taken between a voltage range of -0.2 to 0.6 V vs. Ag/AgCl electrode. 1 M KCl was used as the electrolyte. Electrodes were cycled at least 20 times prior to data recording to ensure removal of any adsorbed contaminants. Capacitance was calculated from Equation (1):

$$C = i\,\frac{dt}{dV} \qquad (1)$$

where i is the current density (A cm^{-2}) at V=0.2 V during the positive sweep and dV/dt is the scan rate used for the measurement. Choosing to read the current at 0.2 V leaves out any contribution from redox reactions which may be occurring at the extremes of the voltage range and is thus a good estimate of the pure double layer capacitance of the sample.

Results and Discussion

Electrochemical results – bare PSiNWs

The I-V response for the bare nanowires tested in aqueous solution, Figure 2-4 a), yields a specific capacitance is ~10 μF cm^{-2}, which is similar to values observed on planar silicon. An electrochemical reaction beginning during the positive potential sweep at around 0.5 V is also observed. The location and shape of this peak implies the oxidation of silicon to SiO_2 [6]. This was further confirmed by performing 500 charge-discharge cycles and subsequently immersing the PSiNWs in dilute HF, which selectively etches SiO_2, for 10 min. Total loss of the PSiNWs after this treatment, shown in Figure 2-4 b), confirms the conversion of PSiNW's to SiO_2 during cycling. Rapid oxidation explains the limited capacitance values as after oxidation the nanowires are no longer electrically active. Thus, these PSiNW's as formed, are not stable in an aqueous environment, preferable for environmental impact and device packaging considerations mentioned above. This is also consistent with the fact that the VLS-grown PSiNWs have only been reported as supercapacitor electrodes in non-aqueous electrolytes [1].

Physical analysis and electrochemical analysis - SiC coated PSiNWs

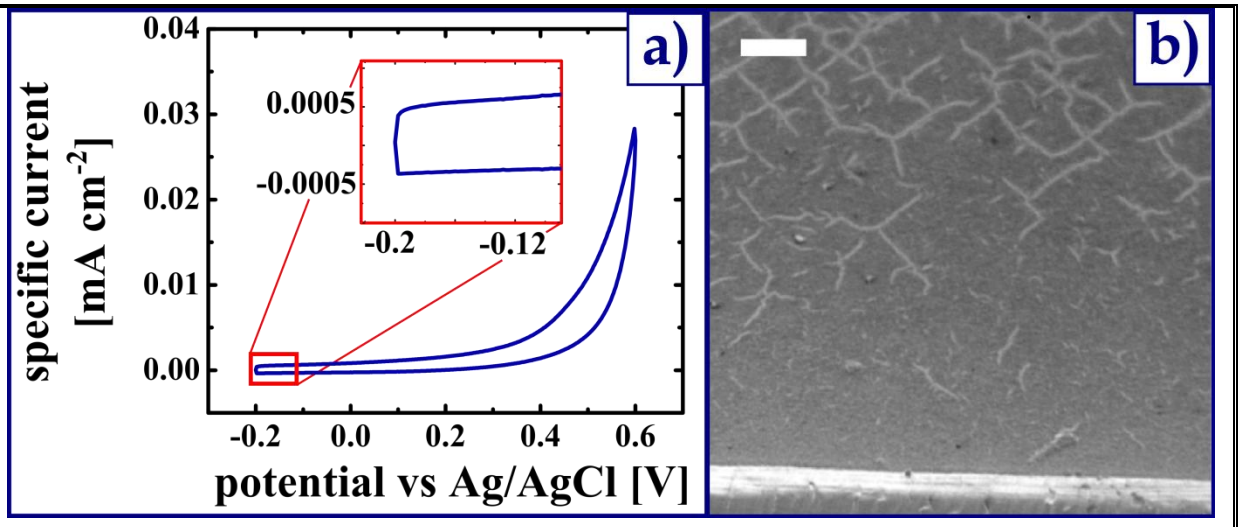


Figure 2-4: a) Cyclic voltammetry results for uncoated PSiNW array. Note large oxidation peak and low specific current during cycling. b) SEM image of bare PSiNW array after 500 charge discharge cycles and HF etch. Note complete loss of the nanowires. Scale bar is 10 μm.

It is well known that SiC coatings are stable in harsh chemical environments [7] and thus a thin SiC layer is selected for chemically passivating the PSiNWs. SiC films are deposited onto PSiNW arrays via low pressure chemical vapor deposition after removal of surface oxide by dilute HF rinsing as described above. The SiC films appear to coat the PSiNWs conformaly as indicated by a representative SEM image of a 3 minute coating provided in Figure 2-5 a), corresponding to a 90 nm coating on a planar silicon sample. It is interesting to note that the thickness of the coating on the nanowire surface is clearly thinner than the film as measured on the planar silicon surface. A 90 nm coating of SiC on the nanowire surfaces would bridge the gap between the nanowires and result in a dense film. The exact reason for the thinness of the nanowire coating is not known for sure. However, by comparing the cyclic voltammetry results for a ~32 μm and 40 μm SiC/PSiNW array, as seen in Figure 2-5 b), the increase in oxidation peak and decrease in specific capacitive current for the latter indicate that the longer nanowires are not completely coated. While the near ideal square wave result for the 32 μm array, exhibiting only a minor oxidation peak, suggests that the shorter nanowires are conformally coated. A similar cycling and HF etching was performed on the shorter coated array as that for the uncoated array discussed above. The negligible change in appearance of the array, as shown in Figure 3-5 c), also supports that the

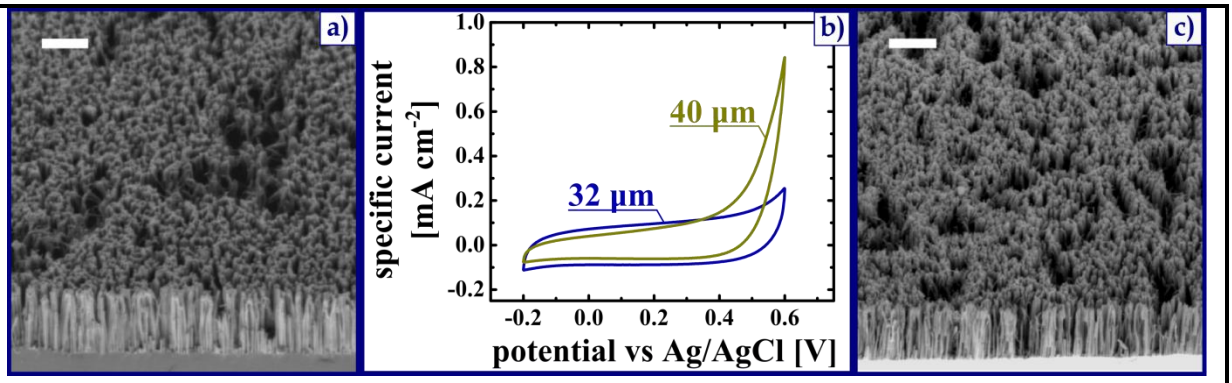


Figure 2-5: a) SEM image of SiC coated PSiNW array after a coating time of 3 minutes. b) Cyclic voltammetry results for SiC/PSiNW arrays of 32 and 40 µm in length. Scale bar is 10 mm. c) SEM image of SiC/PSiNW arrays after 500 charge/discharge cycles and HF etching. Scale bars are 10 µm.

shorter nanowire arrays are conformally coated. These facts support the proposition that transport limitations for the precursor gas into the array are a factor and may be the reason for the coating on the nanowires being thinner than that on a flat substrate. TEM analysis of the nanowires, see Figure 2-6 a), indicates a highly roughened surface which is expected for the SiC deposition parameters used [13]. Diffraction patterns for the coated wires also indicate polycrystalline material, as shown in Figure 2-6 b), in contrast to the single crystalline underlying PSiNWs expected from the etching conditions [2]. Raman analysis confirms the presence of SiC on the wires, as presented in Figure 2-6 c). The SiC coating also renders the surface hydrophilic, exhibiting a near 0° contact angle with water.

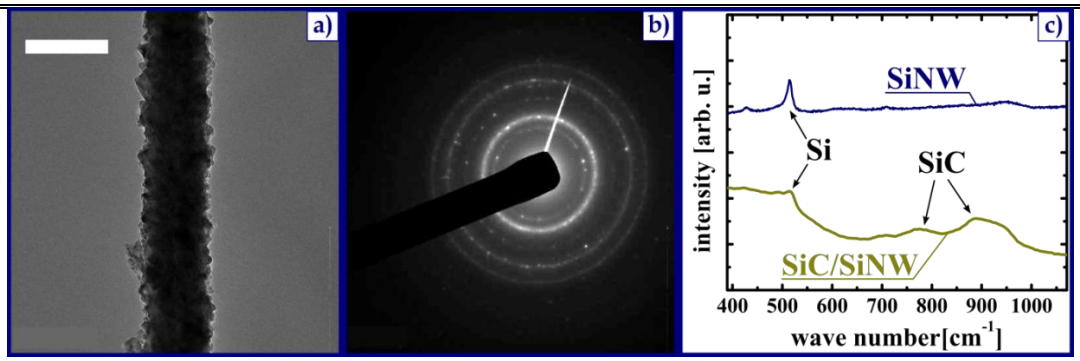


Figure 2-6: a) TEM image of SiC/PSiNW nanowire showing evidence of a rough exterior coating. b) Diffraction pattern for single SiC/PSiNW. Sharp dots are indicative of crystalline interior, while ring pattern indicates polycrystalline material, as expected in the coating from the deposition parameters. c) Raman spectra for bare PSiNW array and SiC/PSiNW array.

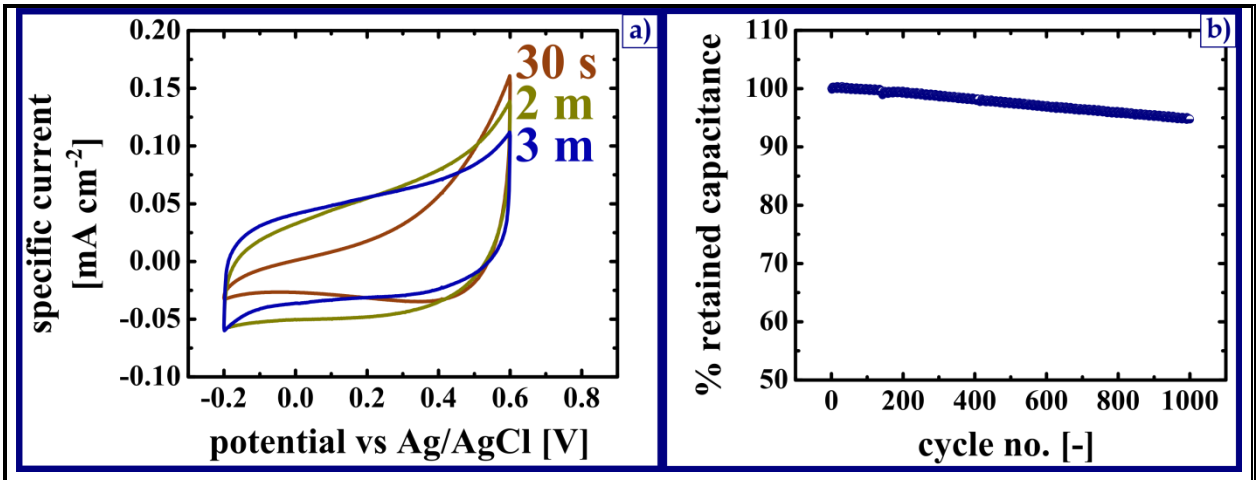


Figure 2-7: a) Cyclic voltammetry results for SiC/PSiNW arrays with coatings of varying thickness, as marked by different coating deposition times. b) Stability results from cycling of the SiC/PSiNW array indicating ~95% capacitance retention after 1000 complete cyclic voltammetry cycles.

Although 3 minute coatings appear to be sufficient for corrosion mitigation, thinner coatings are attempted in order to reduce processing time. All coated samples' CV results indicate improved capacitive behavior and some measure of passivation in comparison to the uncoated nanowires. However, the corrosion peak height, normalized to the projected area of the samples, increased with decreasing coating thickness, shown in Figure 2-7 a). These results suggest that thinner coatings lead to decreased robustness during cycling, an important aspect of supercapacitor energy storage devices. Thus, the longest coating time (3 minutes) used in the initial feasibility experiment is selected for use in all further work. This coating thickness is found sufficient to maintain 95% of the initial capacitance values over the course of 1000 charge-discharge cycles, see Figure 2-7 b).

The scalability of these materials, in terms of energy storage, is investigated by generating wires of various lengths, controlled by immersion time in the PSiNW etch bath, shown in Figure 2-8 a). As is clear from Figure 2-8 b), by increasing the length of the wires, the capacitance increases linearly. For a ~32 μm array, the longest nanowires to be conformally coated, the specific capacitance is determined to be ~1700 μF/cm^2 projected area at a 50 mV/s scan rate, comparable to carbon based microsupercapacitor electrodes [9]–[13]. This corresponds to an energy storage capability of ~850 μJ/cm^2 projected area. Beyond this wire length, the capacitance decreases and the corrosion peak height increases, as described above. This is most likely due to issues with mass transport along the length of the wires, hindering SiC deposition at the base of the NWs.

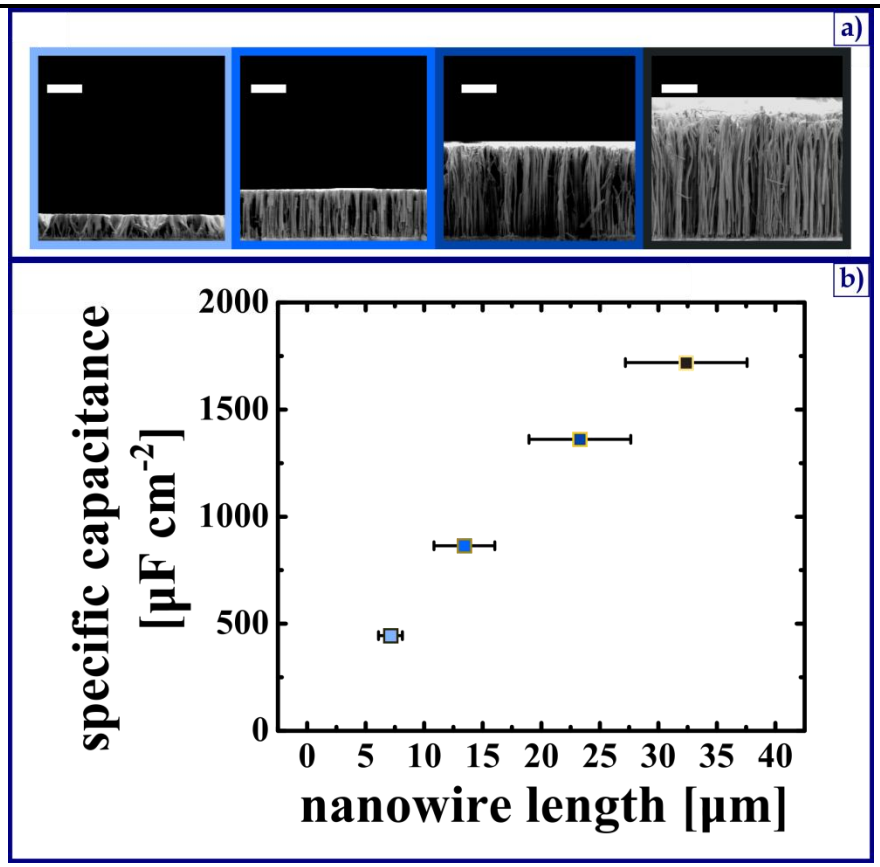


Figure 2-8: a) SEM images of SiC/PSiNW arrays of different lengths, achieved by etching for varying lengths of time. Scale bars are 10 μm. b) Specific capacitance vs. SiC/PSiNW array length. Specific capacitance scales linearly with increasing length, as expected.

It appears that this is a limitation to the utilized coating process, though not to the general principle presented. Theoretical calculations, described in a later chapter, imply that the electrolyte has been excluded from the pores resulting in capacitance values expected for non-porous nanowires. Application of alternative coating methods that work well for very high aspect ratio features and are controllable at thicknesses ~1 nm, such as atomic layer deposition or those described in a later chapter, may provide a solution to these issues and yield materials with even greater energy storage capabilities.

In addition to the advantages in terms of processing and scalability of these materials in comparison to typical microsupercapacitor electrodes, the aligned nanowire configuration may provide for enhanced transport of ions to the active surface area. As

opposed to porous carbons, which typically have tortuous pathways commonly viewed as a problem for ions accessing all the available active surface area, the presented aligned nanowires have spacing of ~100 nanometers, which allows for rapid ion transport during high charge-discharge rates. In order to investigate this, CV measurements are performed over a wide range of scan rates, from 10 mV/s to 5 V/s. The capacitive behavior of the materials is maintained over this range, see Figure 2-9, although a more tilted I-V response, characteristic of resistive behavior, is observed [14]. This may be mitigated through the use of doped SiC, films which are currently under investigation.

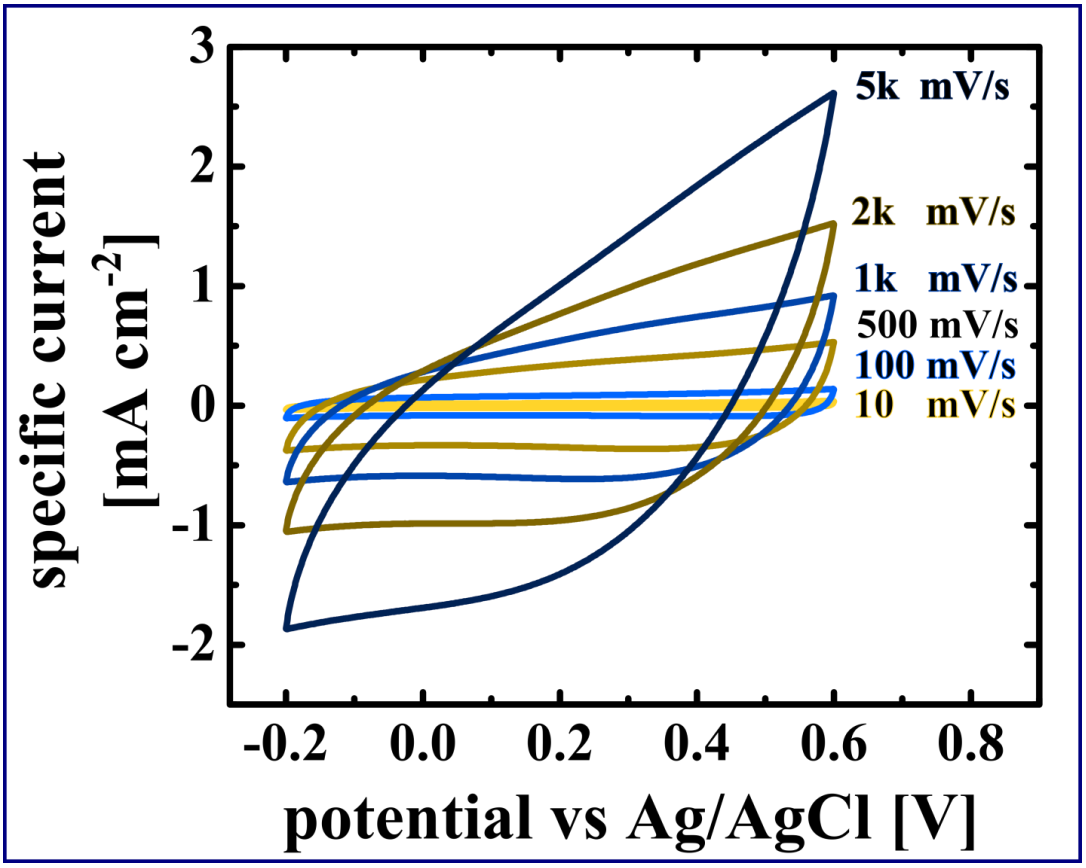


Figure 2-9: Cyclic voltammetry results for 32 μm long SiC/PSiNW array over a range of scan rates.

Conclusions

The application of SiC coated wet-etch formed PSiNWs as high-performance supercapacitor electrode materials for use with green electrolytes has been demonstrated. The materials are fabricated in a facile and IC compatible scheme. Capacitances of up to 1700 $\mu F/cm^2$ are achieved, and remain stable over 10^3 charge/discharge cycles. As well, the nanowires as formed are in electrical contact with the underlying substrate, mitigating the requirement of an additional current collector and implying straight forward integration with Si chip based devices. Limitations in the coating method include inability to coat wires of ~40 μm and above, limiting the total energy storage capability of the SiC/PSiNW structure. Furthermore the SiC coating method results in pore blockage, mitigating the added surface area resulting from the use of porous silicon nanowires. In the following chapter an improved coating method, resulting in an ultrathin protective barrier, will be discussed and the resulting materials' performance characterized.

Note:

Material from the previous chapter has been adapted in part from the publication:

J. P. Alper, M. Vincent, C. Carraro, and R. Maboudian, "Silicon carbide coated silicon nanowires as robust electrode material for aqueous micro-supercapacitor," *Applied Physics Letters*, vol. 100, no. 16, p. 163901, 2012.

References

[1] J. W. Choi, J. McDonough, S. Jeong, J. S. Yoo, C. K. Chan, and Y. Cui, "Stepwise Nanopore Evolution in One-Dimensional Nanostructures," *Nano Letters*, vol. 10, no. 4, pp. 1409–1413, Apr. 2010.

[2] A. I. Hochbaum, D. Gargas, Y. J. Hwang, and P. Yang, "Single Crystalline Mesoporous Silicon Nanowires," *Nano Letters*, vol. 9, no. 10, pp. 3550–3554, Oct. 2009.

[3] M. Zahedinejad, M. Khaje, A. Erfanian, and F. Raissi, "Successful definition of nanowire and porous Si regions of different porosity levels by regular positive photoresist using metal-assisted chemical etching," *Journal of Micromechanics and Microengineering*, vol. 21, no. 6, p. 065006, Jun. 2011.

[4] N. Tas, T. Sonnenberg, H. Jansen, R. Legtenberg, and M. Elwenspoek, "Stiction in

surface micromachining," *Journal of Micromechanics and Microengineering*, vol. 6, no. 4, p. 385, 1996.

[5] C. R. Stoldt, C. Carraro, W. R. Ashurst, D. Gao, R. T. Howe, and R. Maboudian, "A low-temperature CVD process for silicon carbide MEMS," *Sensors and Actuators A: Physical*, vol. 97, pp. 410–415, 2002.

[6] F. Jing, H. Tong, and C. Wang, "Cyclic voltammetry study of silver seed layers on p-silicon (100) substrates," *Journal of Solid State Electrochemistry*, vol. 8, no. 11, pp. 877–881, Oct. 2004.

[7] M. Mehregany, C. A. Zorman, N. Rajan, and C. H. Wu, "Silicon carbide MEMS for harsh environments," *Proceedings of the IEEE*, vol. 86, no. 8, pp. 1594–1609, 1998.

[8] R. Maboudian, C. S. Roper, C. Carraro, and R. T. Howe, "Silicon Carbide Thin Films using 1,3-Disilabutane Single Precursor for MEMS Applications - A Review," 2006, vol. 3, pp. 267–280.

[9] Y. Q. Jiang, Q. Zhou, and L. Lin, "Planar MEMS supercapacitor using carbon nanotube forests," in *Micro Electro Mechanical Systems, 2009. MEMS 2009. IEEE 22nd International Conference on*, 2009, pp. 587–590.

[10] F. Liu, A. Gutes, I. Laboriante, C. Carraro, and R. Maboudian, "Graphitization of n-type polycrystalline silicon carbide for on-chip supercapacitor application," *Applied Physics Letters*, vol. 99, no. 11, p. 112104, 2011.

[11] J. Chmiola, C. Largeot, P. L. Taberna, P. Simon, and Y. Gogotsi, "Monolithic Carbide-Derived Carbon Films for Micro-Supercapacitors," *Science*, vol. 328, no. 5977, pp. 480–483, Apr. 2010.

[12] P. Huang, M. Heon, D. Pech, M. Brunet, P.-L. Taberna, Y. Gogotsi, S. Lofland, J. D. Hettinger, and P. Simon, "Micro-supercapacitors from carbide derived carbon (CDC) films on silicon chips," *Journal of Power Sources*, vol. 225, pp. 240–244, Mar. 2013.

[13] D. Pech, M. Brunet, H. Durou, P. Huang, V. Mochalin, Y. Gogotsi, P.-L. Taberna, and P. Simon, "Ultrahigh-power micrometre-sized supercapacitors based on onion-like carbon," *Nature Nanotechnology*, vol. 5, no. 9, pp. 651–654, Sep. 2010.

[14] E. Frackowiak and F. Beguin, "Carbon materials for the electrochemical storage

of energy in capacitors," *Carbon*, vol. 39, no. 6, pp. 937–950, 2001.

Chapter 3 – Carbon coated porous silicon nanowires as microsupercapacitor electrodes

Chapter summary

In this chapter an improved passivation method for the porous silicon nanowires discussed above is demonstrated. The thrust of the chapter is the testing of a selective coating procedure for depositing an ultra-thin (~ 1-3 nm) carbon sheath over the nanowires to passivate them. The ultra-thin nature of the coating enables solvent access to the pore area and hence a large improvement of active specific surface over the SiC coated PSiNWs discussed above. The electrochemical performance of these coated nanowires is characterized in both an aqueous electrolyte and an ionic liquid electrolyte. Specific capacitance values reaching 325 mF cm^{-2} are achieved in ionic liquid, and calculations indicate that the theoretical maximum capacitance of the pristine wires is reached. TEM studies confirm the coating thickness and its conformality. Raman spectroscopy indicates that the carbon in the coating is mainly sp^2 hybridized, with corresponding high conductivity. At the time of writing, these materials represent the largest specific energy of any microsupercapacitor electrode published. A test device is prepared and demonstrated powering an LED.

Introduction

As discussed above, supercapacitors function by storing electrical charge (Q) in the electrochemical double layer at the interface between an electrode and an electrolyte. When the electrode is biased with a potential V, ions of the opposite charge are electrostatically attracted to the electrode surface, forming the ECDL and leading to a capacitance, C, described by the standard parallel plate capacitor Equation (1) [1]:

$$C = \frac{A}{d}\epsilon \qquad (1)$$

Here A is the interfacial area of the electrode, d is the distance between the electrode and the ECDL, and ε is the permittivity of the electrode-ECDL interphase. These devices are referred to as "super" capacitors in part because the electrodes are composed of materials with high specific surface area such as activated carbon [2] or exfoliated graphene [3], and the distance between the electrode and ECDL is very small compared to standard capacitors; this leads to ~100x greater specific capacitance over standard double plate capacitors [4]. Cycle lifetimes are typically orders of magnitude greater than battery electrodes as ideally there are no chemical reactions or volumetric changes within the active materials of supercapacitors during cycling [5]. Charge storage at the electrode surface also enables rapid charging and discharging characteristics and thus

high power capabilities [1]. Planar microsupercapacitors refer to a class of supercapacitors utilizing planar electrode geometries with small form factors, preferable for on-chip application [6]. These supercapacitors are attractive energy storage devices for integration with autonomous micro-sensor networks due to their high-power capabilities and robust cycle lifetimes [2]. Various methods have been used to fabricate carbon based planar microsupercapacitors and single-electrode specific capacitances of up to ~20 mF cm^{-2} projected area have been achieved [7].

Silicon-based supercapacitor electrodes synthesized via chemistries that are compatible with standard microfabrication processes are promising as on-chip power storage devices for autonomous microsystems applications due in part to their ease of integration with current microprocessor fabrication techniques. One such high surface area silicon synthesis method is based on a low temperature electroless etch process first described elsewhere [8,9]. This self-assembling synthesis method is well known to produce homogeneous arrays of porous silicon nanowires with an average pore diameter of ~10 nm and a high specific surface area of 342 $m^2 g^{-1}$ [10]. This is a large improvement in specific surface area over chemical vapor deposited silicon nanowires made porous by battery cycling (~100 $m^2 g^{-1}$) previously reported as supercapacitor electrode materials [11] while utilizing a simpler one step wet etch. However, these porous nanowires are highly reactive and dissolve rapidly when exposed to mild saline solutions [12]. As discussed in the previous chapter, silicon carbide (SiC) thin films have been used to protect the PSiNWs, yielding silicon carbide coated PSiNWs (SiC/PSiNWs) [13]. The SiC coatings were 10's of nm thick and while they successfully mitigated Si degradation during electrochemical cycling in aqueous electrolytes, they also resulted in pore blockage and a large decrease in the materials' energy storage potential. Here is described an improved coating method where by exposing the PSiNW arrays to a dilute methane environment in Ar at elevated temperatures, an ultra-thin carbon sheath is deposited over the wires, allowing full electrolyte access to the porous surface area while still mitigating Si degradation. The carbon sheath is also selective, forming only on the porous nanowires and not on planar silicon, making it even more attractive for the processing of integrated power supply materials. The capacitive characterization is also extended to an ionic liquid electrolyte which enables higher power and energy capabilities. A hydrophobic ionic liquid was selected to improve wetting of the hydrophobic carbon coated nanowires and performance of the material.

Experimental details

PSiNW synthesis

Porous SiNWs were synthesized following the previously published method [8]. 1x1 cm^2 (1-5 mΩ·cm, boron doped, single side polished) silicon (100) coupons were cleaned by successive sonication in acetone, isopropyl alcohol and de-ionized water. The coupons were then exposed to UV generated ozone for 5 minutes and any silicon oxide was subsequently removed by a 5 minute etch in 48% hydrofluoric acid (HF). ***NOTE: HF is a highly toxic acid and should only be used after specific training on the hazards, protocol in case of spill or exposure, and safe working practices.** The unpolished sides of the samples were coated with a thin nylon coating in order to protect them from etching. A ~2 mm wide strip of Si on the front side of the samples was also protected to provide an electrical contact point. Samples were then immersed in the oxidant/etchant bath consisting of 5M HF and 20 mM $AgNO_3$, equilibrated in a 50 ^oC heating bath, for various lengths of time to produce different length wire arrays. A clear plastic chemical splash guard was placed around the entire apparatus to mitigate any hazards of a spill during etching. Samples were then rinsed in de-ionized water and residual silver was removed by a HNO_3 (~3.5M) etch for 15-45 minutes. Drying was performed in a critical point dryer (Tousimis Autosamdri815B). For more detailed instructions and explanations of the steps, as well as a figure of the experimental setup used, the prior chapter on SiC coated PSiNW should be consulted.

Carbon coating

Carbon coating was performed in an atmospheric pressure chemical vapor deposition chamber (Lindberg Blue/m). Samples were heated to 900 ^oC at a rate of ~55 $^oC\ min^{-1}$ under 200 sccm of Ar (Praxair 99.995%). A flow of 4 sccm CH_4 (Praxair 99.993%) was then introduced to the chamber for 30 minutes. The CH_4 flow was then stopped and the sample cooled under Ar at a rate of ~15 $^oC\ min^{-1}$.

Physio-chemical characterization

SEM imaging was performed using an Agilent 8500 FE-SEM at a beam voltage of 1 kV. TEM/STEM imaging was performed using a JEOL 2200FS Field-Emission microscope with in-column W filter, operated at 200 kV. Elemental maps were obtained by energy-filtering on the Si L and the C K edges. Raman spectroscopy was conducted with a HoribaJY LabRAM confocal Raman microscope utilizing a 633 nm laser. Contact angle measurements were made with a Ramé Hart 290-F1 automated goniometer.

Electrochemical characterization

Electrochemical characterization was performed using a CHI 660D electrochemical station operating in a three-electrode configuration for single electrodes, and a two-electrode configuration for the device. For aqueous testing a Ag/AgCl reference and Pt

wire counter electrode were used. Characterizations performed in the ionic liquid 1-Ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide (EMIM-TFSI) utilized a Ag wire reference and a Pt wire counter electrode.

Results and discussion

Physio-chemical characterization

Scanning electron micrographs of the nanowires post carbonization (C/PSiNWs), as shown in Figure 3-1 a), reveal that their vertical orientation is maintained after carbonization and no significant structural damage is observed. A detailed transmission electron microscopy study was conducted in order to analyze the uniformity of the carbon sheath and the nanowire pore structure after carbon coating. A representative scanning transmission electron microscopy (STEM) analysis is presented in Figures 3-1 b),c) for a nanowire pre-carbonization and a nanowire post-carbonization, respectively.

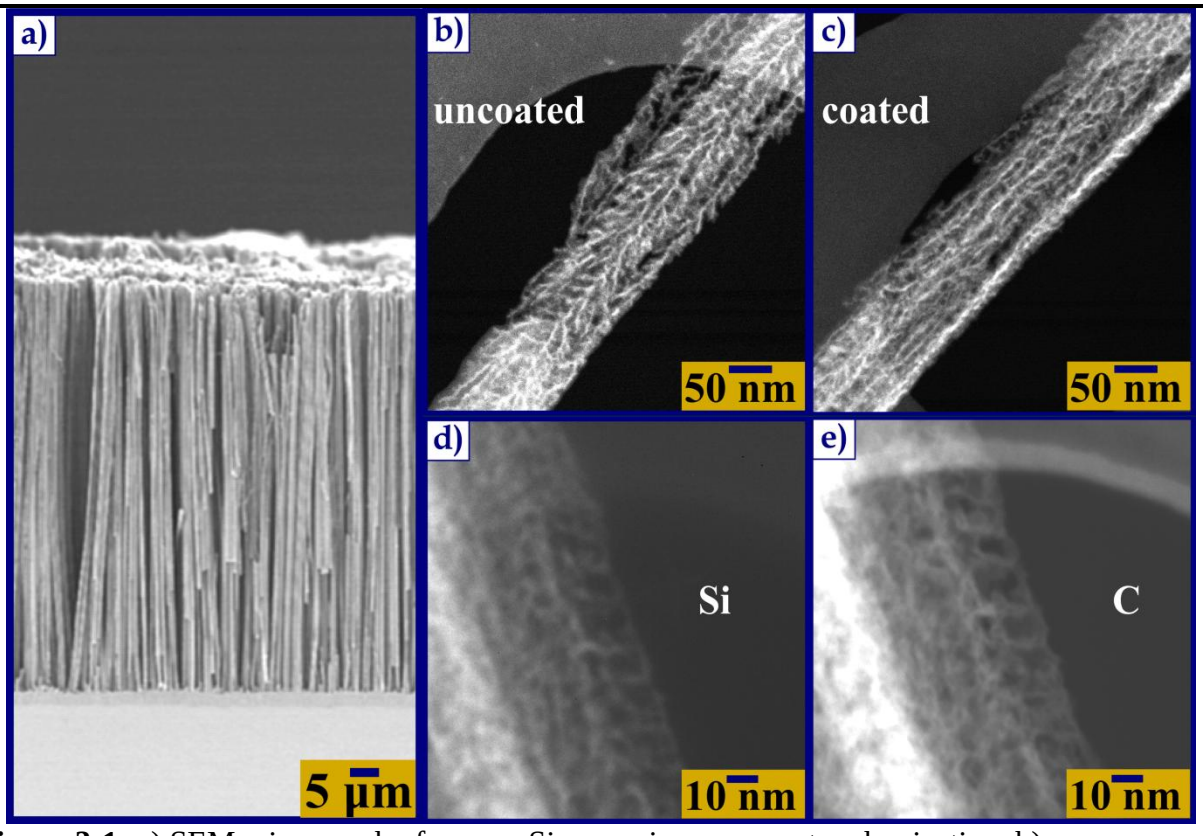


Figure 3-1: a) SEM micrograph of porous Si nanowire array post carbonization. b) Representative STEM image of a PSiNW. c) Representative STEM image of a C/PSiNW. d) Silicon elemental mapping realized through energy filtered TEM image of a C/PSiNW. e) Carbon elemental mapping of the same nanowire as in d), realized through energy filtered TEM.

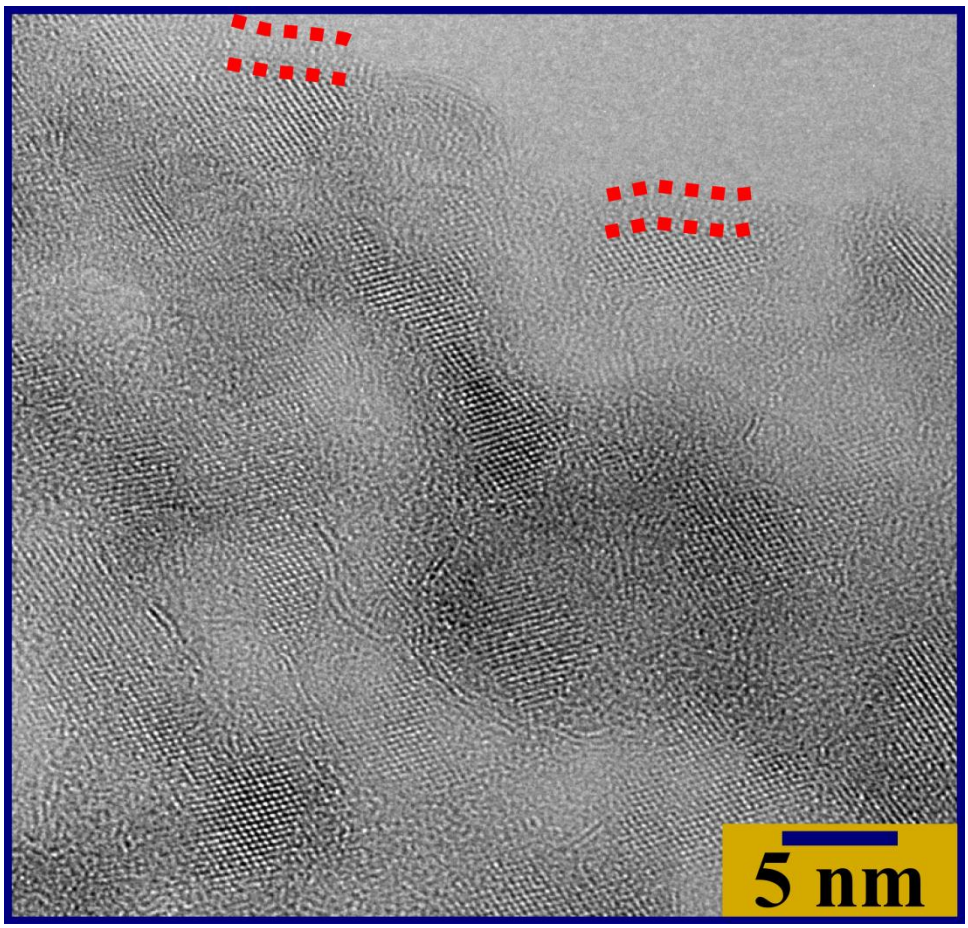


Figure 3-2: High resolution TEM micrograph of a C/PSiNW. Red dotted lines outline non-crystalline edge region used to define combined carbon and residual native oxide coating on PSiNWs.

The results indicate that the nanoscale pore structure of the PSiNWs is preserved, a key factor in realizing the full energy storage potential of these materials. Both the PSiNWs and C/PSiNWs samples exhibit a distribution of pore sizes; however, from these TEM images most openings are found to be ~10 nm in diameter, showing close accordance with previous reports on the PSiNW pore structure [10]. Elemental maps of C/PSiNWs generated from energy filtered TEM, shown in Figure 3-1 d),e), demonstrate complete overlap of the Si and C, which is important for successful passivation of the Si core. The pore openings also are clearly carbon free, strongly suggesting that the pore area remains solvent accessible. High resolution TEM micrographs of the C/PSiNWs , displayed in Figure 3-2, indicate a crystalline core and an amorphous sheath as outlined in Figure 3-2. By analyzing the sheath thickness post carbonization, attributed to the

carbon layer and residual native oxide, we estimate the carbon layer thickness to be between 1-3 nm. Micro-Raman measurements along a bundle of C/PSiNWs, presented in Figure 3-3, indicate the carbon sheath is axially continuous. The G peak position (1595 – 1596 cm^{-1}) and the D to G peak intensity ratios (1.34-1.42) both indicate a mainly sp^2 hybridized carbon film [14] with a correspondingly high electronic conductivity [15]. The lack of any carbon signal from the planar silicon exposed to the same carbonization conditions proves that the deposition chemistry is highly selective to the nanoporous form of silicon.

Electrochemical characterization – aqueous electrolyte

The capacitance characteristics of these materials are probed with the techniques of cyclic voltammetry (CV) and chronopotentiometry (CP) in a three-electrode configuration. As discussed above, during CV the potential over the working electrode is swept at a constant rate and the current is measured. During CP measurements, a constant current is applied to the working electrode and the potential over it is measured. The specific capacitance C (mF cm^{-2}) may be determined from either technique using the Equation (2):

$$C = i\,\frac{dt}{dV} \qquad (2)$$

where i is the current density (mA cm^{-2}) and dV/dt is the rate of change of the potential.

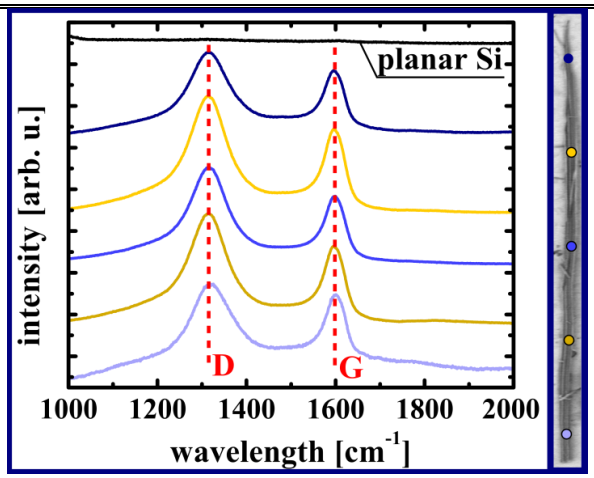


Figure 3-3: Raman mapping of a C/PSiNW bundle. The Raman spectrum of a planar silicon region, which was also exposed to the carbonization conditions, is included (top curve), demonstrating the selectivity of the carbonization process for the more highly reactive PSiNW surface. SEM micrograph outset is the nanowire bundle being analysed. Colored dots indicate locations where the Raman spectra were collected. The diameter of the colored dots represents 2 μm.

During CV, i is chosen at the midpoint of the voltage sweep in order to disregard any currents from redox reactions which may be occurring at the extremes of the voltage range and is thus a good estimate of the pure double layer capacitance of the sample. For CP, dV/dt is taken as the average rate of change during the entire discharge. Energy density is calculated from CP using equation (3):

$$E = 1/2CV^2 \quad (3)$$

where E is the energy per specific area (mJ cm^{-2})and V is the voltage window discharged over. Power density may then be calculated by equation (4):

$$P = E/t \quad (4)$$

where P is the power per specific area (mW cm^{-2}) and t is the total time for discharge.

For the aqueous system, both techniques are performed in a three-electrode system to specifically analyze the electrode material's performance. In Figure 3-4, the CV results

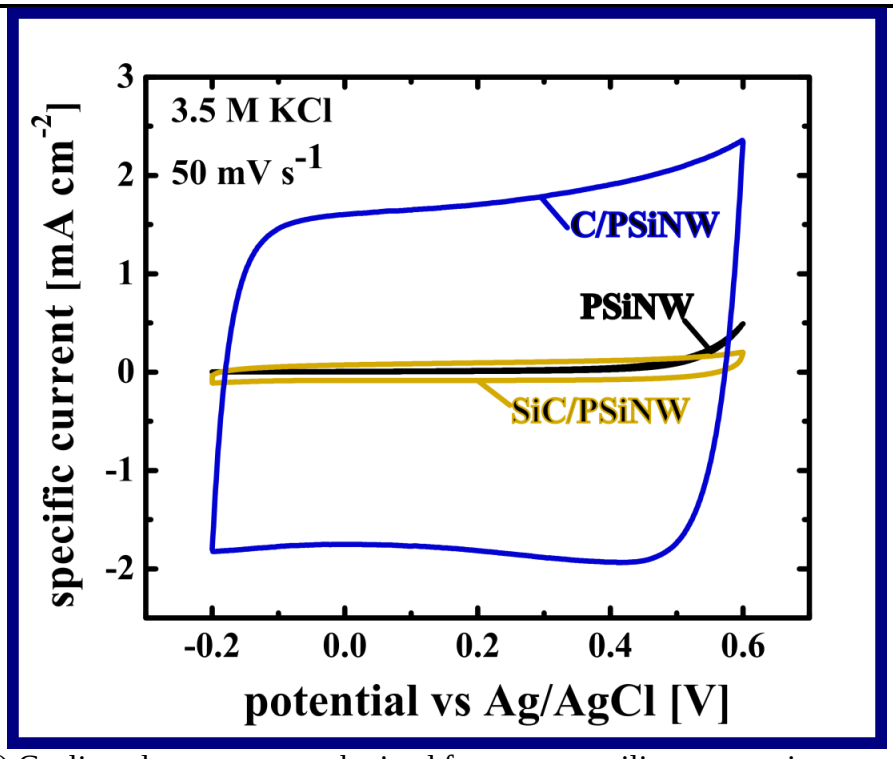


Figure 3-4: a) Cyclic voltammograms obtained from porous silicon nanowire array, SiC/PSiNWs and C/PSiNWs in 3.5 M KCl at a scan rate of 50 mV s^{-1}. All nanowire arrays had lengths of ~35 μm, achieved by matching the etching time.

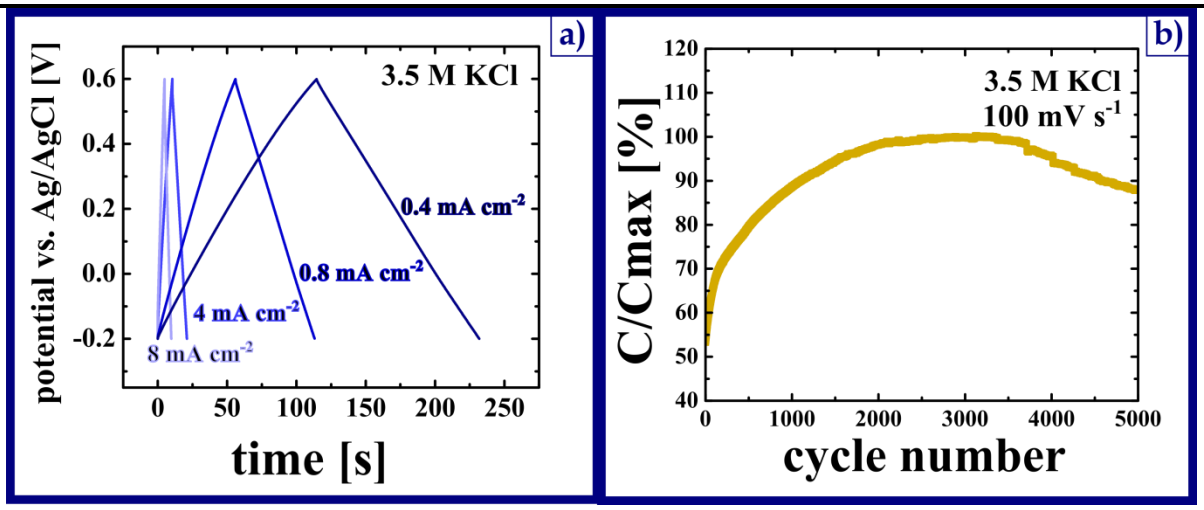


Figure 3-5: a) CP results for C/PSiNW over a range of scan rates in 3.5 M KCl. b) Results for extended CV cycling of C/PSiNW in 3.5 M KCl.

are presented in 3.5 M KCl for C/PSiNWs as well as PSiNWs and compared to those obtained previously for the SiC/PSiNWs discussed in a previous chapter [13]. All nanowires were ~35 μm in length, achieved by etching for the same amount of time. The large peak present in the PSiNW voltammogram near 0.8 V indicates oxidation of the PSiNWs as discussed in the previous chapter [13]. The rapid degradation of the PSiNWs upon exposure to aqueous solutions also greatly reduces the electrically active surface area and hence the small capacitive current. The oxidation peak is greatly suppressed in the C/PSiNW results indicating passivation of the surface. The small residual peak may be due to the oxidation of the Si, the carbon surface, or the electrolyte and it indicates that the stability window for the entire system is ~0.8V. The capacitive current measured on C/PSiNWs is ~17x that measured for SiC/PSiNWs. This result confirms that the thin carbon sheath passivates the nanowire surface while leaving the pore volume more accessible to the electrolyte and resulting in the surface of the pore participating in capacitive energy storage. The carbon sheath's extremely thin nature is key to the improved performance, as opposed to the relatively thicker SiC coating which results in solvent exclusion from the pores and prevention of the pore surface from being an active capacitive site.

Chronopotentiometry results, presented in Figure 3-5 a), demonstrate that the capacitive performance of C/PSiNWs is stable over a wide range of current densities. In aqueous electrolytes, carbonized nanowire arrays of ~38 μm in length have an energy density of ~19 mJ cm^{-2} and a power density of 0.081 mW cm^{-2} at a discharge current of 200 mA cm^{-2}. When the discharge current is increased to 8 A cm^{-2}, the energy density of

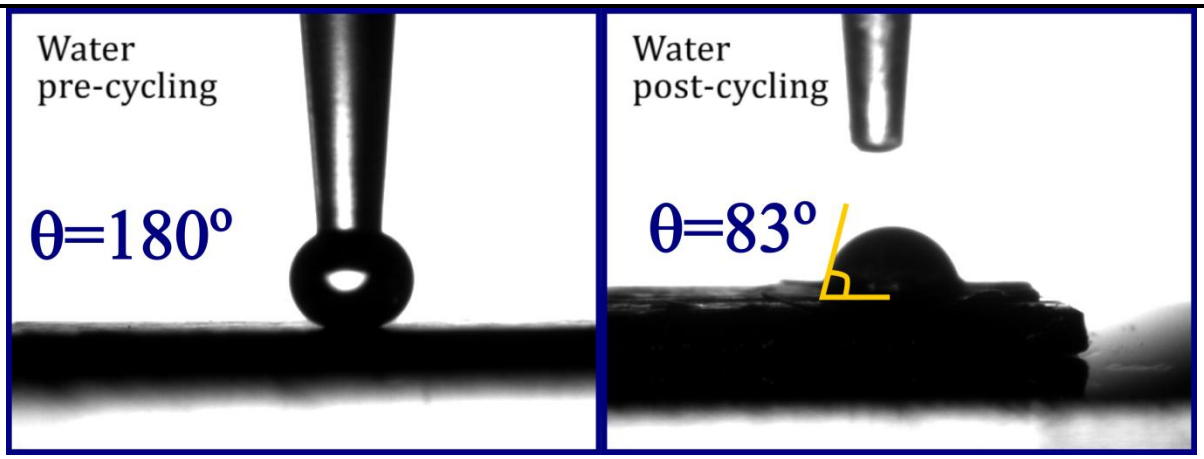


Figure 3-6: Contact angle of water with the sample tested in Figure 3-5 pre- and post-cycling.

the material decreases to ~16 mJ cm^{-2} and the power density increases to ~3.9 mW cm^{-2}. During these tests, a slow increase is observed in the capacitance for the C/PSiNWs with additional cycling. This behavior is further probed by extended CV cycling, results presented in Figure 3-5 b), and it is found that the capacitance does not peak until after ~2800 cycles, with an initial capacitance of ~55% of the maximum. This is attributed to poor initial electrode wettability. Water contact angle measurements of the carbonized surface indicate a hydrophobic surface with a water-C/PSiNW contact angle approaching 180°, as seen in Figure 3-6. After cycling, a contact angle of ~83° is observed, shown in Fig 3-6. This is most likely due to oxidation of the materials during cycling as evidenced by the slight peak observed in the CV at the high voltage range seen in Figure 3-4. The proposed explanation is that initially oxidation of the carbon increases the wettability, increasing the wetted pore area and hence capacitance. Subsequently the oxidation of the underlying PSiNWs results in a decrease of the material's capacity. The C/PSiNW arrays retain 88% of the maximum capacitance after a total of 5000 cycles, proving that the overall oxidative protection provided by the ultrathin carbon sheath is robust.

Electrochemical characterization – ionic liquid

While mild aqueous electrolytes are attractive due to their environmentally benign nature, biocompatibility and low cost, the stable operating voltage window is limited to ~1 V due to the electrolysis of water. In contrast, ionic liquids are stable over a much larger window, leading to improvements in the theoretical maximum energy and power densities, which scale with V^2. With this motivation, different length carbonized nanowire arrays (from 25 to 120 μm in length) were tested in an ionic liquid electrolyte, 1-Ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl) imide (EMIM-TFSI), and the

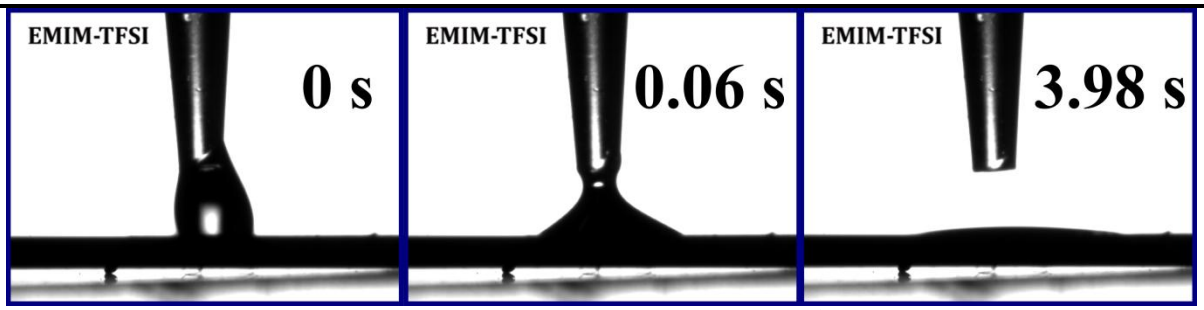


Figure 3-7: Time series of contact angle results showing a near 0^{o} contact angle of EMIM-TFSI with C/PSiNW surface.

scaling of capacitance with wire length was investigated. If the entirety of the wire is electrochemically active and wetted by the electrolyte, capacitance should scale linearly with nanowire length, as total surface area does. A near 0^{o} contact angle was measured for EMIM-TFSI on the C/PSiNW surface, as indicated by the time series shown in Figure 3-7, thus well wetted pores are expected. Figure 3-8 presents the capacitance results from the chronopotentiometry testing of the nanowire arrays in EMIM-TFSI at a current density of 1 mA cm^{-2} and a potential range of -1.0 – 1.7 V vs. Ag. These results demonstrate that the capacitance does indeed increase in a linear fashion with nanowire length. For arrays 120 μm in average length, a capacitance of ~325 mF cm^{-2} is obtained, the highest specific ECDL capacitance for planar electrode materials reported to date. We find that this value corresponds well to the theoretical maximum expected for the uncoated porous SiNWs, confirming that the complete pore area is likely being utilized for charging; details of the calculation may be found in the Appendix. The chronopotentiometry curves used to calculate the capacitance shown in Figure 3-9 indicate that there are some charge transfer reactions from the non-ideal nature of discharge results. However they contribute negligibly to the calculated capacitance and robust cycle-lifetime results, discussed later, imply these reactions neither appreciably improve nor hinder performance. It is also found that the initial volumetric capacitance of the nanowires in EMIM-TFSI closely matches the maximum value measured in aqueous electrolytes during extended cycling, due to the excellent wettability of the carbonized C/PSiNWs by EMIM-TFSI.

In order to compare device performance metrics to other planar microsupercapacitor electrode materials, two samples of C/PSiNWs, with specific capacitances of ~75 mF cm^{-2}, were implemented in a planar device configuration utilizing EMIM-TFSI as the electrolyte. A Ragone plot comparing our device performance to other planar microsupercapacitor materials [7, 13, 16, 17–20] is presented in Figure 3-10 a). The C/PSiNW device exhibits energy densities in ionic liquids that are the highest published to date for planar supercapacitor electrode materials, while maintaining

power densities which are comparable to carbon nanotube-reduced graphene oxide composites (RGO-CNT) [7]. This moderate power limitation is a result of the total ESR through the electrodes, ~376 Ω for a ~0.8 cm^2 total device area, as calculated from the IR drop in the GD results at 3 mA cm^{-2}. C/PSiNW lifetime behavior in EMIM-TFSI, shown in Figure 3-10 b), demonstrates that the materials are moderately robust compared to the other materials discussed in this work, with ~83% capacitance retention after 5,000 complete CP cycles at a 3 mA cm^{-2} charge discharge current. As a demonstration of the device function, Figure 3-11 shows that it can successfully power a white LED.

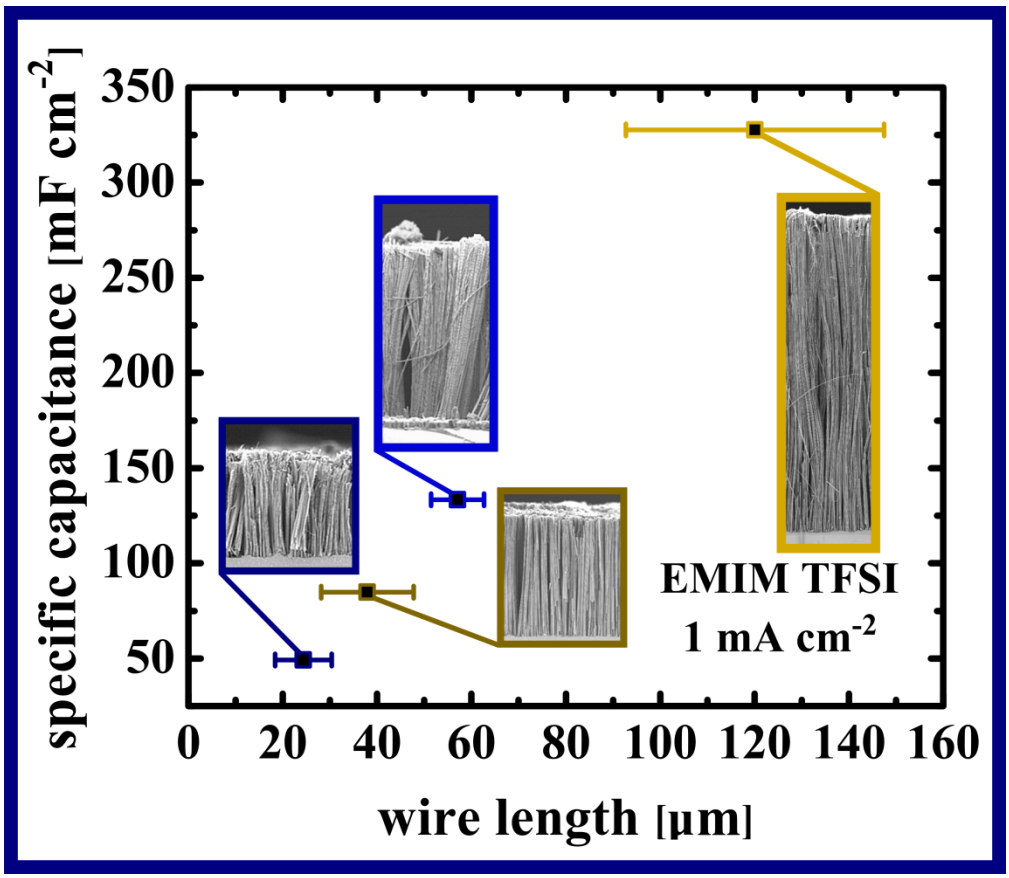


Figure 3-8: Plot of specific capacitance vs. average wire length for various CPSiNWs calculated from galvanostatic discharge data in EMIM-TFSI electrolyte at a current density of 1 mA cm^{-2}. Error bars are two standard deviations of the average value obtained from 10 cross sectional SEM images (representative SEM micrographs are inset for the different length arrays).

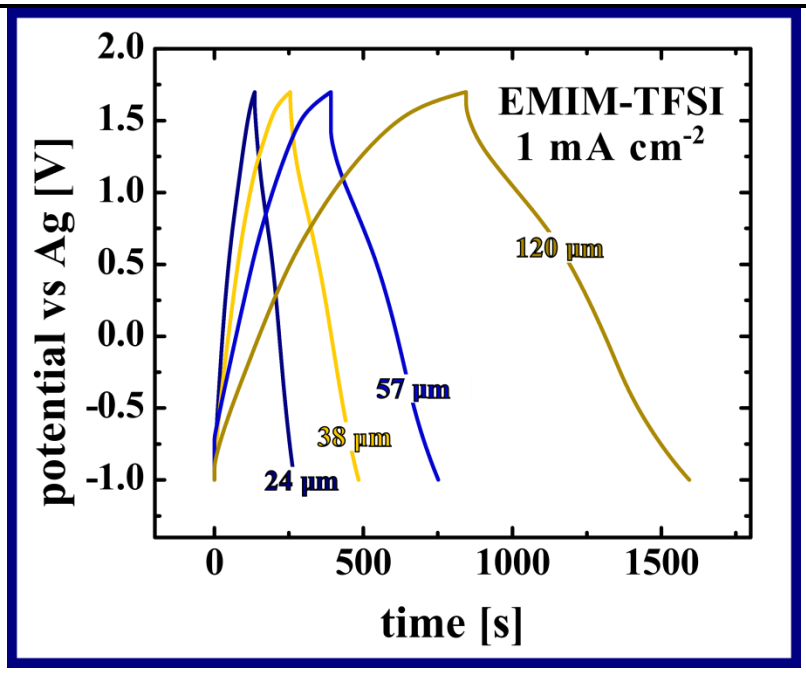


Figure 3-9: CP curves over a variety of discharge rates for C/PSiNW in EMIM-TFSI.

Conclusion

The results presented highlight that C/PSiNWs are quite promising as an extremely high energy density planar microsupercapacitor electrode material, which may enable smaller form factors for microsensors and microsystems devices. These results are also interesting as they indicate that the entirety of the porous structure is conformally coated, protected, and electrochemically active by the graphitic carbon sheath and hence the vastly improved performance over the SiC/PSiNWs discussed in the previous chapter. Due to their high surface area, electro-chemical stability, and the ultra-thin nature of the carbon coating, these materials may very well prove enabling to a variety of applications benefiting from high surface area, nanostructured Si based materials. Fuel cell energy generation [21], photoelectrolysis [22], and sensing [23] are a few such examples. The facile nature of the process should encourage further study of these promising materials. A possible shortcoming for these materials is the poor wettability in aqueous electrolytes which are favorable for certain applications as previously discussed. As well, the stability, while robust in comparison to battery electrodes, may not be optimal for application in systems which require sustained performance over ~100k cycles. These issues will be addressed by a novel electrode system presented in the following chapter.

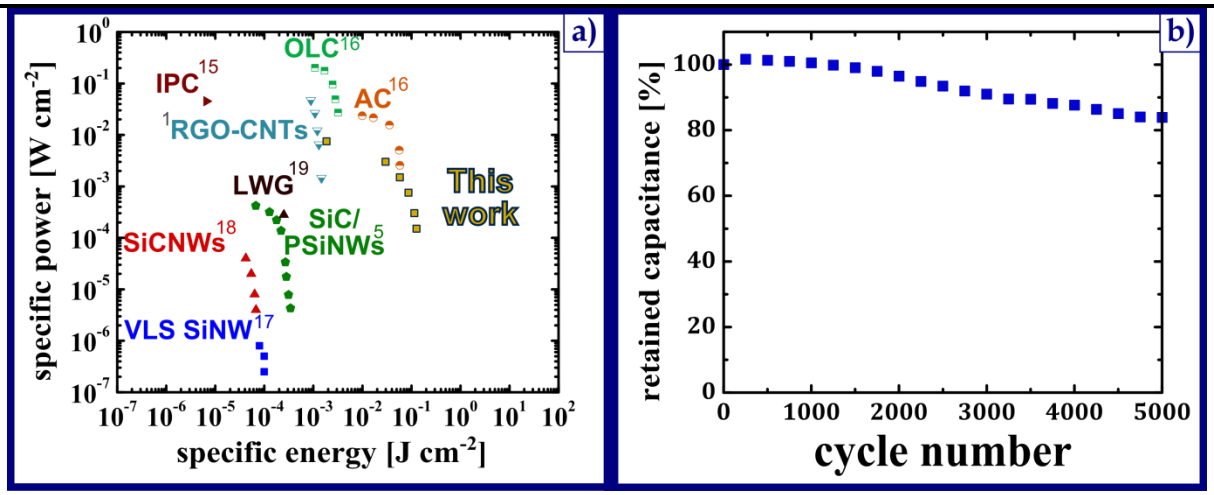


Figure 3-10: a) Ragone plot comparing the energy and power density of the C/PSiNW device tested in this work to other planar microsupercapacitor electrode materials: activated carbon (AC) [15], inkjet printed carbon (IPC) [14], laser written graphene (LWG) [18], onion like carbon (OLC) [15], reduced graphene oxide - carbon nanotube hybrid (RGO-CNT) [7], silicon carbide coated porous silicon nanowires (SiC/PSiNW) [11], silicon carbide nanowires (SiCNWs) [17], and vapour-liquid-solid grown silicon nanowires (VLS-SiNW) [16]. b) Results of extended cycling C/PSiNW device at charge-discharge current of 3 mA cm^{-2}.

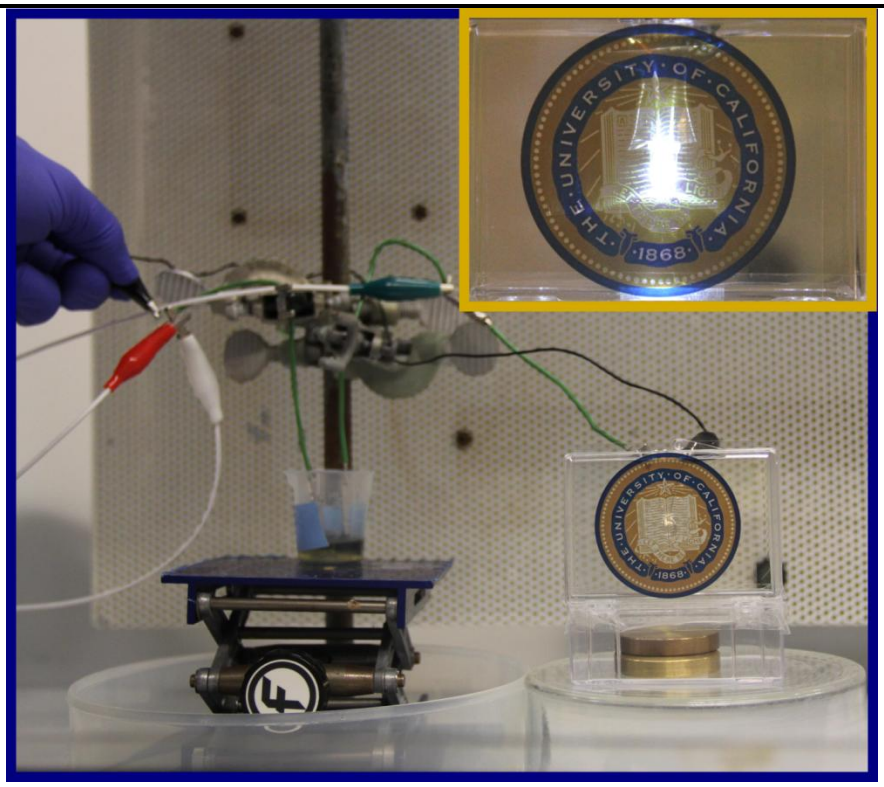


Figure 3-11: Photograph of C/PSiNW array device setup used to power a white LED during discharging of the device. The inset is an image of the LED during discharge.

References

[1] B. E. Conway, *Electrochemical Supercapacitors: Scientific Fundamentals and Technological Applications*. New York: Springer, 1999.

[2] P. Simon and Y. Gogotsi, "Materials for electrochemical capacitors," *Nature materials*, vol. 7, no. 11, pp. 845–854, 2008.

[3] Y. Zhu, S. Murali, M. D. Stoller, K. J. Ganesh, W. Cai, P. J. Ferreira, A. Pirkle, R. M. Wallace, K. A. Cychosz, M. Thommes, D. Su, E. A. Stach, and R. S. Ruoff, "Carbon-Based Supercapacitors Produced by Activation of Graphene," *Science*, vol. 332, no. 6037, pp. 1537–1541, Jun. 2011.

[4] M. Winter and R. J. Brodd, "What Are Batteries, Fuel Cells, and Supercapacitors?," *Chemical Reviews*, vol. 104, no. 10, pp. 4245–4270, Oct. 2004.

[5] E. Frackowiak and F. Beguin, "Carbon materials for the electrochemical storage of energy in capacitors," *Carbon*, vol. 39, no. 6, pp. 937–950, 2001.

[6] J. Chmiola, C. Largeot, P. L. Taberna, P. Simon, and Y. Gogotsi, "Monolithic Carbide-Derived Carbon Films for Micro-Supercapacitors," *Science*, vol. 328, no. 5977, pp. 480–483, Apr. 2010.

[7] M. Beidaghi and C. Wang, "Micro-Supercapacitors Based on Interdigital Electrodes of Reduced Graphene Oxide and Carbon Nanotube Composites with Ultrahigh Power Handling Performance," *Advanced Functional Materials*, vol. 22, no. 21, pp. 4501–4510, Nov. 2012.

[8] K.-Q. Peng, Y.-J. Yan, S.-P. Gao, and J. Zhu, "Synthesis of large-area silicon nanowire arrays via self-assembling nanoelectrochemistry," *Advanced Materials*, vol. 14, no. 16, p. 1164, 2002.

[9] M. Zahedinejad, M. Khaje, A. Erfanian, and F. Raissi, "Successful definition of nanowire and porous Si regions of different porosity levels by regular positive photoresist using metal-assisted chemical etching," *Journal of Micromechanics and Microengineering*, vol. 21, no. 6, p. 065006, Jun. 2011.

[10] A. I. Hochbaum, D. Gargas, Y. J. Hwang, and P. Yang, "Single Crystalline Mesoporous Silicon Nanowires," *Nano Letters*, vol. 9, no. 10, pp. 3550–3554, Oct. 2009.

[11] J. W. Choi, J. McDonough, S. Jeong, J. S. Yoo, C. K. Chan, and Y. Cui, "Stepwise Nanopore Evolution in One-Dimensional Nanostructures," *Nano Letters*, vol. 10, no. 4, pp. 1409–1413, Apr. 2010.

[12] C. Chiappini, X. Liu, J. R. Fakhoury, and M. Ferrari, "Biodegradable Porous Silicon Barcode Nanowires with Defined Geometry," *Advanced Functional Materials*, vol. 20, no. 14, pp. 2231–2239, Jun. 2010.

[13] J. P. Alper, M. Vincent, C. Carraro, and R. Maboudian, "Silicon carbide coated silicon nanowires as robust electrode material for aqueous micro-supercapacitor," *Applied Physics Letters*, vol. 100, no. 16, p. 163901, 2012.

[14] A. C. Ferrari and J. Robertson, "Interpretation of Raman spectra of disordered and amorphous carbon," *Physical review B*, vol. 61, no. 20, p. 14095, 2000.

[15] A. Grill, "Electrical and optical properties of diamond-like carbon," *Thin Solid Films*, vol. 355, pp. 189–193, 1999.

[16] D. Pech, M. Brunet, H. Durou, P. Huang, V. Mochalin, Y. Gogotsi, P.-L. Taberna, and P. Simon, "Ultrahigh-power micrometre-sized supercapacitors based on onion-like carbon," *Nature Nanotechnology*, vol. 5, no. 9, pp. 651–654, Sep. 2010.

[17] D. Pech, M. Brunet, P.-L. Taberna, P. Simon, N. Fabre, F. Mesnilgrente, V. Conédéra, and H. Durou, "Elaboration of a microstructured inkjet-printed carbon electrochemical capacitor," *Journal of Power Sources*, vol. 195, no. 4, pp. 1266–1269, Feb. 2010.

[18] W. Gao, N. Singh, L. Song, Z. Liu, A. L. M. Reddy, L. Ci, R. Vajtai, Q. Zhang, B. Wei, and P. M. Ajayan, "Direct laser writing of micro-supercapacitors on hydrated graphite oxide films," *Nature Nanotechnology*, vol. 6, no. 8, pp. 496–500, Jul. 2011.

[19] J. P. Alper, M. S. Kim, M. Vincent, B. Hsia, V. Radmilovic, C. Carraro, and R. Maboudian, "Silicon carbide nanowires as highly robust electrodes for micro-supercapacitors," *Journal of Power Sources*, vol. 230, pp. 298–302, May 2013.

[20] F. Thissandier, A. Le Comte, O. Crosnier, P. Gentile, G. Bidan, E. Hadji, T. Brousse, and S. Sadki, "Highly doped silicon nanowires based electrodes for micro-electrochemical capacitor applications," *Electrochemistry Communications*, vol. 25, pp. 109–111, Nov. 2012.

[21] M. Wang, X. Wang, J. Li, and L. Liu, "In situ synthesis of 3D platinum nanoflowers on porous silicon for monolithic integrated micro direct methanol fuel cells," *Journal of Materials Chemistry A*, vol. 1, no. 28, p. 8127, 2013.

[22] A. P. Goodey, S. M. Eichfeld, K.-K. Lew, J. M. Redwing, and T. E. Mallouk, "Silicon Nanowire Array Photoelectrochemical Cells," *Journal of the American Chemical Society*, vol. 129, no. 41, pp. 12344–12345, Oct. 2007.

[23] S. E. Lewis, J. R. DeBoer, J. L. Gole, and P. J. Hesketh, "Sensitive, selective, and analytical improvements to a porous silicon gas sensor," *Sensors and Actuators B: Chemical*, vol. 110, no. 1, pp. 54–65, Sep. 2005.

Chapter 4 – Silicon carbide nanowires as highly robust electrodes for microsupercapacitors

Chapter summary

In this chapter the effectiveness of silicon carbide (SiC) nanowires (NW) as an electrode material for micro-supercapacitors has been investigated. SiC is interesting as an electrode material as it is more thermally and chemically resistant than silicon or carbon and may be applied in harsh conditions which are found in various chemical process industries which these other electrode materials cannot withstand. SiC NWs are grown on a SiC thin film coated with a thin Ni catalyst layer via chemical vapor deposition. A specific capacitance of ~240 μF cm^{-2} is demonstrated, which is comparable to the values recently reported for planar micro-supercapacitor electrodes. Charge-discharge studies demonstrate the SiC nanowires exhibit exceptional stability, with 95% capacitance retention after 2×10^5 charge/discharge cycles in an environmentally benign, aqueous electrolyte. Doping of the nanowires with nitrogen through the addition of 5 at% ammonia to the precursor gas flow rate improves the conductivity of the nanowire films by over an order of magnitude leading to increased power capabilities. While these studies were performed under ambient conditions, they serve as an important baseline for future studies in harsh environments such as high temperature or highly oxidizing conditions.

Introduction

As discussed above, with the development of autonomous micro-sensors and actuators and distributed sensor networks, there has arisen a need for compact microscale, integrated, and reliable power sources. Micro batteries are under development for these applications; however, they are still susceptible to typical battery failure modes leading to lifetimes of ~10^3 cycles [1]. This aspect is especially unattractive for remote sensors in locations which are difficult to service such as those embedded in civil structures, oil wells or living bodies. Batteries also suffer from the potential for overheating during operation under high charge/discharge rates [2], which is problematic for uses which require frequent high-power energy bursts for data relay. In this context, supercapacitors offer advantages as mentioned above, specifically their high power ratings and long cycle lifetimes [3].

Several planar micro-supercapacitors have already been reported in the literature [4–12] and discussed in earlier chapters. A major challenge of developing such planar devices is the device-level integration of the electrode material. Activated carbon, which is the most common material used in macroscale supercapacitors, is difficult to integrate

in planar technology, due to such issues as precise placement and the uniformity needed to pattern the electrode [5]. As a consequence, for on chip supercapacitor development, research has focused on nanomaterials such as carbon nanotubes [4], graphene [8], or silicon nanowires (NWs) [7], which are by nature high surface area materials and compatible with standard microfabrication techniques. However, carbon based nanomaterials are hydrophobic, and hence present electrode wetting issues with aqueous electrolytes. While, as discussed in an earlier chapter, porous silicon NW electrodes corrode readily in aqueous electrolytes [7]. These are major shortcomings, given that aqueous electrolytes provide higher ionic mobility than non-aqueous alternatives (e.g., organic or ionic liquid based electrolytes), are environmentally benign and may be biocompatible. Due to the corrosion issue, bare Si NW supercapacitors have only been demonstrated in non-aqueous electrolytes [11]. Microfabricated carbon post interdigitated electrodes generated from photoresist pyrolysis have also received attention [10,12]. These materials are much larger in scale with heights of ~100 μm and diameters of ~50 μm. After electrochemical activation they are hydrophilic and demonstrate higher specific capacitance than the nanomaterials discussed above. However this is due in part to pseudocapacitive contributions and at best they show capacitance fade of over 10% after only 1000 charge/discharge cycles.

In this chapter the performance of silicon carbide nanowires as electrode materials in aqueous electrolyte for micro-supercapacitors is discussed. SiC is known to be a wide-bandgap semiconductor material with excellent physico-chemical stability, and is compatible with standard microfabrication techniques [13]. The results in this chapter show that the SiC NWs exhibit specific capacitance values in aqueous electrolytes that are comparable to published carbon nanomaterial-based microsupercapacitors mentioned above [4,7,8]. The SiC nanomaterials here are less than 10 μm thick and can withstand 2×10^5 charge/discharge cycles in aqueous electrolyte while maintaining over 95% of their initial capacitance value. Through the addition of ammonia to the precursor gas flow, the electrical conductivity of the nanowires can be improved by over an order of magnitude. Together these properties make SiC NWs a promising candidate for aqueous micro supercapacitor applications which require extremely robust performance and thin form factors. This work also serves as an important baseline for future work on the development of these materials as harsh environment supercapacitor electrodes. While the growth kinetics, mechanism, and resulting structure of these materials have not been conclusively determined at the time of this writing, preliminary results collected are provided in Appendix II.

Experimental

Intrinsic silicon carbide nanowire growth

Intrinsic silicon carbide nanowires are grown on n-doped 3C-SiC thin (2 μm) films on a Si(100) substrate with a SiO_2 (1.5 μm) isolation layer or a Si(111) substrate. The 3C-SiC thin films are deposited in a low-pressure chemical vapor deposition (LPCVD) reactor, employing methylsilane as the precursor and in-situ doped using ammonia [14]. The SiC NWs are grown by a Ni-catalyzed CVD process similar to that reported in Ref. [15]. A thin layer of nickel (~2.2 nm) is deposited by e-beam evaporation on the SiC/SiO2/Si(100) substrates. This layer acts as the catalyst for the SiC NW growth [15]. Samples are placed inside a LPCVD reactor and the temperature is increased to 950 °C at a rate of about 55 °C min^{-1} under 10 sccm of H_2. When the growth temperature is reached, methyltrichlorosilane (MTS) is introduced to the tube at a flow rate of 0.5 sccm while the H_2 flow rate is reduced to 5 sccm. The growth step proceeds for varying durations to achieve nanowire arrays of different lengths. At the end of the growth, the H_2 flow rate is increased to 10 sccm while MTS flow is stopped. Samples are then cooled down to room temperature at a rate of about 15 °C min^{-1}. The pressure is maintained at approximately 5 Torr throughout the growth process.

Doped silicon carbide nanowire growth

Doped silicon carbide nanowires are synthesized on ammonia doped SiC films (~300 nm) on an aluminum nitride substrate. The films are grown with the same NH_3 concentration as that used in the nanowire synthesis. SiC nanowires are grown as above except ammonia (5% in H2) is added to the reactor during growth at a flow rate between 1-5 atomic %. As well, the MTS flow rate during growth is 1 sccm and the total H_2 flow rate (including the contribution from the 5% ammonia) is 20 sccm during the entire synthesis.

Nanowire physico-chemical and electrochemical analysis

Nanowire morphology is characterized by scanning electron microscopy (SEM) using a LEO 1550. Crystal structure is determined using a Siemens D5000 automated X-ray diffractometer (XRD) operated in θ-2θ geometry. For the XRD analysis, the nanowires are grown directly on a Si(111) substrate to avoid interference with signal obtained from the underlying SiC thin film. High resolution transmission electron microscopy (HRTEM) is performed using the FEI Tecnai monochromated transmission electron microscope (TEM) operating at 200 kV.

Capacitive performance of the nanowires is evaluated using an electrochemical workstation (CH Instruments Inc., 660D) in a 3-electrode configuration. Electrical connection to the nanowire samples is made through the n-doped SiC thin film on which the nanowires are grown. During catalyst evaporation, a part of the sample is

masked in order to create a nanowire-free area which is used for this connection. A platinum wire is employed as the counter electrode and a Ag/AgCl electrode is used as the reference electrode. All measurements are performed in an aqueous electrolyte solution of 3.5 M KCl. Prior to acquisition, samples are cycled ten times to ensure removal of any adsorbed contaminants.

Results and discussion

Physical characterization

Figure 4-1 a) shows a representative SEM image of the nanowire arrays grown with a 30 minute growth time. A dense film of NWs is achieved with an average thickness of ~6 μm and the nanowires appear tapered. An XRD spectrum of nanowires grown on a Si(111) substrate is shown in Figure 4-1 b). Two peaks are noticeable in the range 20-90°, namely the Si(111) peak at 28.5° and the SiC peak at 35.7°. A strong peak near 35.7° corresponds to the lattice spacing between SiC bilayer stacks along the <111> growth direction of α-SiC or <0001> direction of β-SiC, and does not allow one to distinguish between cubic and hexagonal phases [16]. The full width-at-half-maximum values for Si and SiC peaks, at 28.5° and 35.7° respectively, after subtracting the Kα2 peak, are 0.1° and 0.43°, with 0.1° being the minimum resolution of the XRD system. This is indicative of the good crystalline quality of the SiC nanowires. The XRD results are confirmed by high resolution TEM characterizations performed on single NWs dispersed in ethanol by sonication (see Figure 4-2). These micrographs show that the SiC nanowires grow along the <111>-3C axis with a high density of stacking faults associated with the presence of 2H SiC polytypes. Lines on each side of the <111>-3C axis in the Fourier

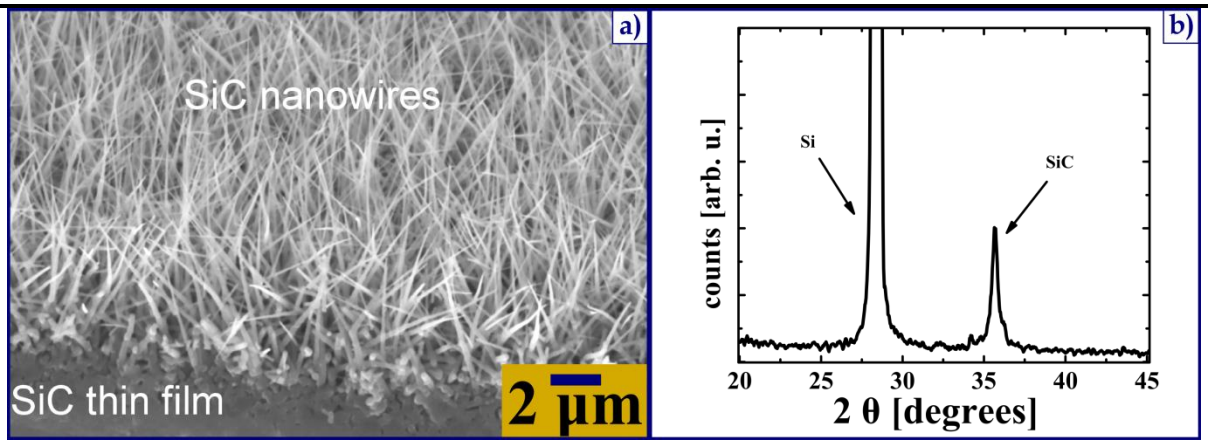


Figure 4-1: a) SEM image of intrinsic SiC nanowire film. b) XRD spectra taken of SiC nanowire film grown on Si substrate**.**

transform of the image confirm the presence of stacking faults (see Figure 2 inset). Preliminary evidence indicating an axial (hexagonal or rhombic form of SiC) is provided in Appendix II.

Intrinsic electrochemical characterization

Supercapacitors store energy at the interface between the electrodes and the electrolyte, in what is called the electric double layer (EDL) [3] as discussed above. The capacitance of such devices is then directly proportional to the surface area of the electrodes' material. Thus, by using high surface area materials such as nanowires, high capacitance values are expected. Cyclic voltammetry (CV), in the voltage range of -0.2 to 0.6 V vs. Ag/AgCl reference, is employed to determine the contribution of the nanowires to the total measured capacitance of the sample (see Figure 4-3 a).

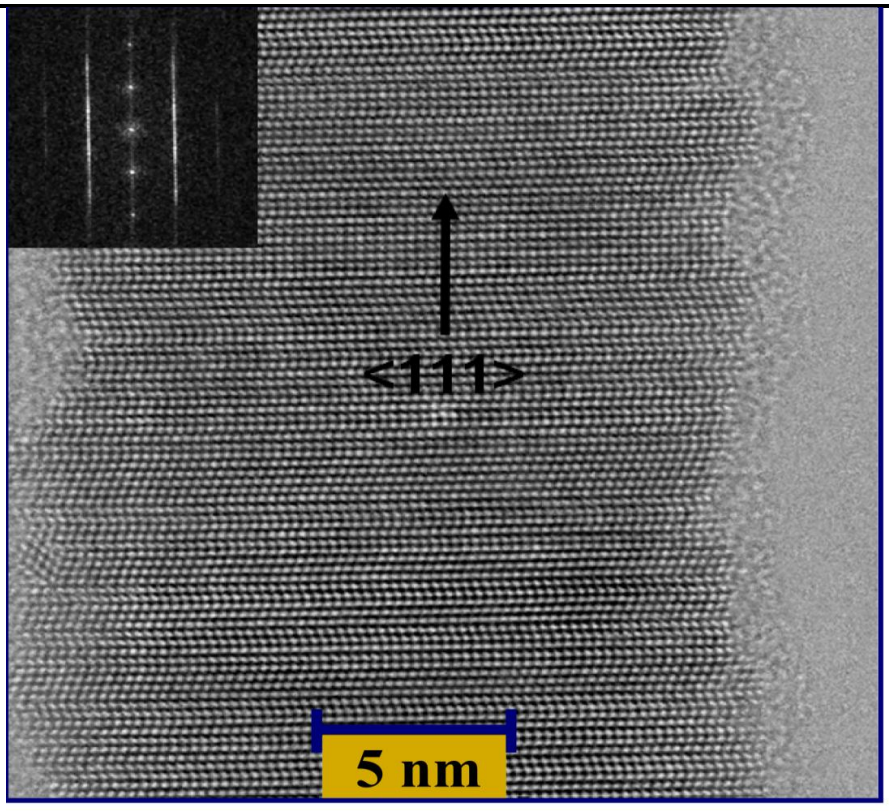


Figure 4-2: representative TEM image of single nanowire. Inset is the fourier transform of the image.

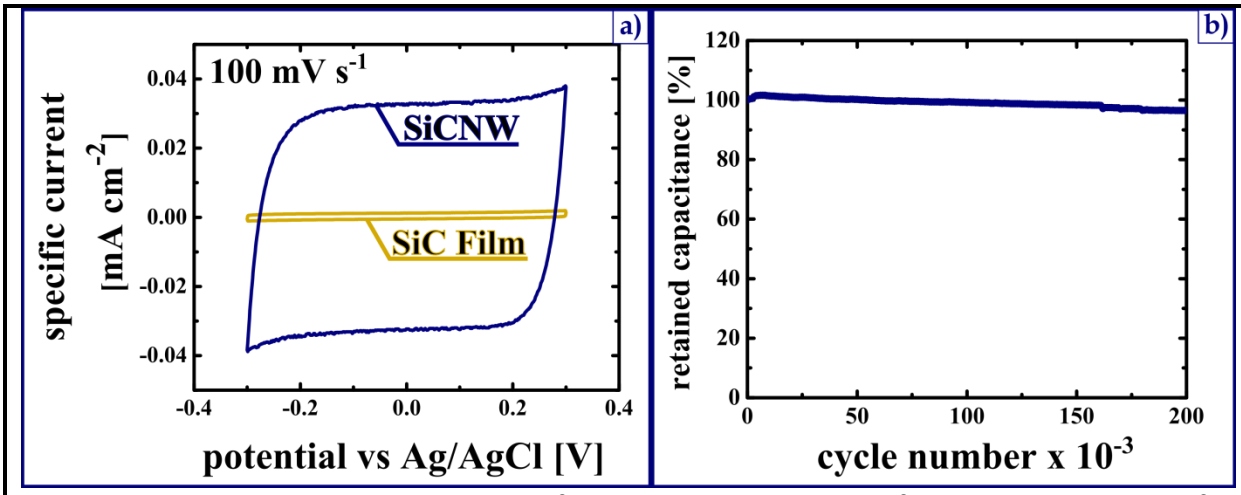


Figure 4-3: a) Cyclic voltammetry results for intrinsic SiC nanowire film compared to that of a SiC planar film. b) Extended cycling results for SiC nanowire film.

Capacitance per projected area is calculated by Equation (1):

$$C = i\,\frac{dt}{dV} \qquad (1)$$

where i is the current density (A cm^{-2}) at V=0.2 V during the positive sweep, dV/dt is the scan rate used for the measurement. Choosing to read the current at 0.2 V leaves out any contribution from redox reactions which may be occurring at the extremes of the voltage range and is thus a good estimate of the pure double layer capacitance of the sample. Figure 4-3 a) shows a comparison of CV results between the SiCNW-on-SiC/SiO_2/Si and the SiC/SiO_2/Si samples. The measured capacitance of the NW sample at 100 mV s^{-1} is ~38 times higher than the SiC thin film alone. This corresponds to SiC NWs exhibiting a specific capacitance value of ~240 µF cm^{-2} projected area, comparable to the results obtained using carbon nanotubes [4] or carbide-derived carbons [6].

In order to evaluate the cycle life of the nanowires, 2×10^5 charge/discharge cycles have been performed on a sample using cyclic voltammetry at a scan rate of 5 V s^{-1}. The samples are cycled over the whole charge/discharge voltage window of -0.2 to 0.6 V. This is important to note as degradation via redox reactions may not occur in a voltage window limited to be smaller than the operational voltage window. Figure 4-3 b) reports the percent retained capacitance as a function of the cycle number. This test reveals an extremely stable behavior, with less that 5%capacitance fade after 2×10^5 charge discharge cycles. This is superior to carbon based electrodes, such as in Ref. [12], which show >12% capacitance loss after one thousand cycles. In this regard, SiC

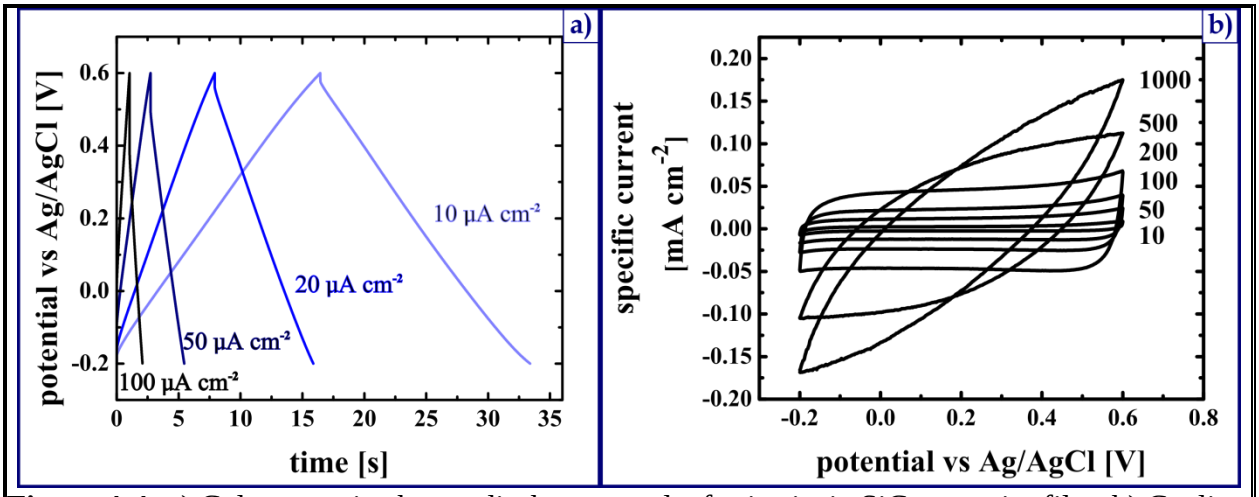


Figure 4-4: a) Galvanostatic charge-discharge results for intrinsic SiC nanowire film. b) Cyclic voltammetry results for SiC nanowire film over a wide range of scan rates, listed in the graph in mV s^{-1}.

nanowires are also superior to earlier discussed silicon NW arrays that are found to corrode readily during cyclic voltammetry under the same conditions [7]. The one step processing of these materials is also favourable compared to the two step silicon NW formation followed by SiC coating in order to mitigate aqueous corrosion discussed above [7]. The capacitance values of the SiC nanowires presented here are comparable to SiC coated silicon NWs of similar length.

Galvanostatic discharge studies have been performed to analyze the energy and power characteristics of the SiCNWs. A constant charge and discharge current is utilized to cycle the electrodes between -0.2 to 0.6 V. Figure 4-4 a) reports the charge/discharge data obtained. The initial vertical voltage drop region during discharge cycling may be attributed to the electrode series resistances. With increasing current this voltage drop increases as expected. By analyzing the slope of the discharge curve, the capacitance may be calculated from equation (2). The specific energy stored in the electrode is determined from the calculated capacitance by:

$$E = 1/2CV^2 \qquad (2)$$

where E is the energy per specific area and V is the voltage window discharged over. Specific power may then be determined by:

$$P = E/t \qquad (3)$$

where P is the power per specific area and t is the total time for discharge. The useable stored energy drops off as the current is increased due to an increasing voltage drop from the series resistances in the system. Hence it is important to report the specific power achieved at a specific energy stored. From the galvanostatic discharge results, the electrodes tested here exhibit a specific energy of ~68 μJ cm^{-2} and specific power of ~4 μW cm^{-2} at the discharge current of 10 μA cm^{-2}, the lowest current tested. At the highest current tested, 100 mA cm^{-2}, the electrodes yield a specific energy of ~41 μJ cm^{-2} and specific power of ~40 μW cm^{-2}. This power value is limited by the total resistance through the electrode. The resistance also affects the capacitance as discharge rate is increased which can be observed from the results of cyclic voltammetry performed over a wider range of scan rates presented in Figure 4-4 b). As the scan rate exceeds 200 mV s^{-1}, the resulting current-potential graph becomes less rectangular and more skewed, implying uncompensated internal resistances. The capacitance drops from ~240 μF cm^{-2} at 100 mV s^{-1} to ~135 μF cm^{-2} at 1 V s^{-1}.

Doped silicon carbide electrochemical analysis

The addition of ammonia to SiC film growth gases has previously been demonstrated as

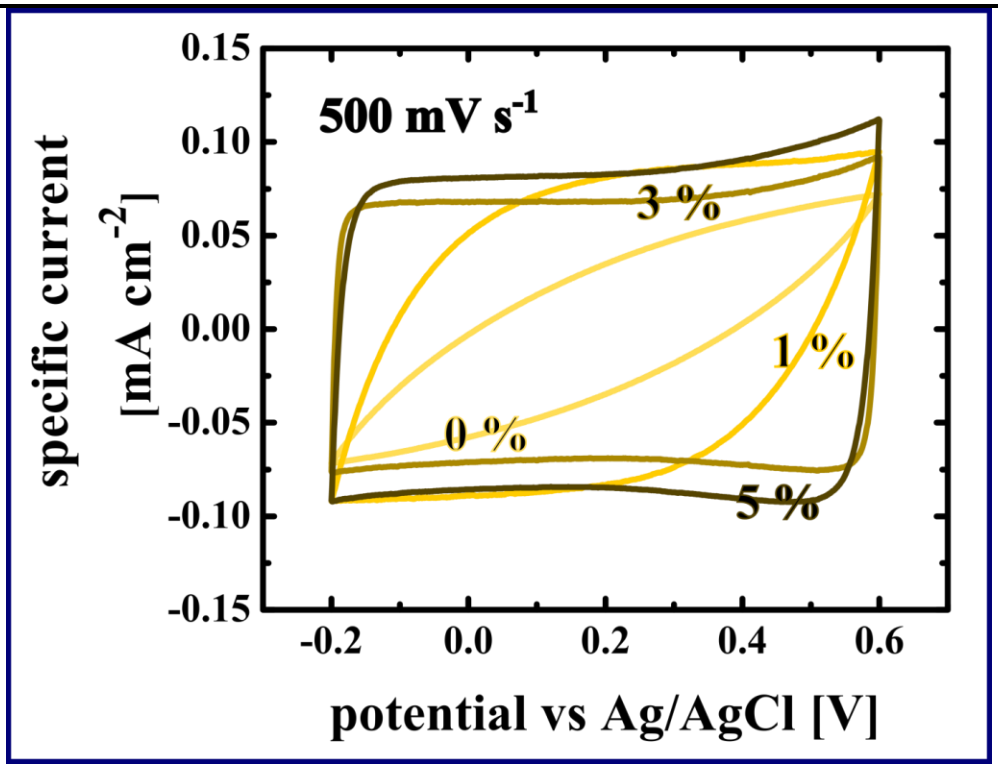


Figure 4-5: Cyclic voltammetry results for different percentages, in at%, of ammonia in precursor gas flow rate during SiCNW synthesis.

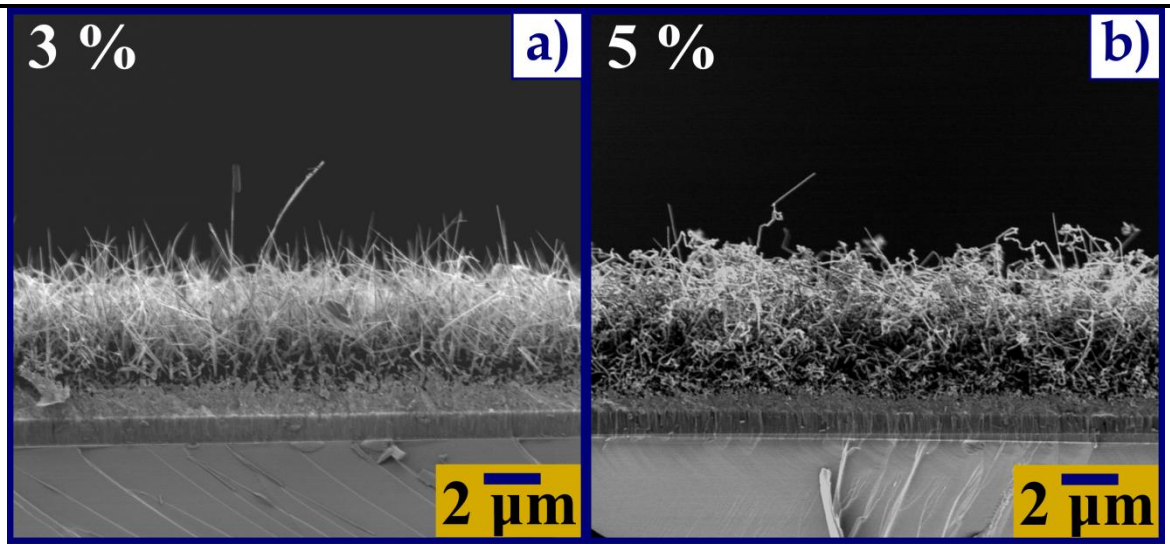


Figure 4-6: a) SEM image of SiCNWs with 3 at% ammonia added to precursor gas flow. b) SEM image of SiCNWs with 5 at% ammonia added to precursor gas flow.

an effective method for improving the conductivity resulting films [17]. Resistivity of the thin films was decreased by three orders of magnitude through the addition of 2.5 at% ammonia for SiC films grown at 800 ^{o}C using 1,3-disilabutane as the SiC precursor. In this work concentrations of ammonia in the reactor gas mixture were varied from 1-5 at% and the resulting nanowire films were characterized using similar methods as those discussed above for intrinsic SiCNWs. Cyclic voltammetry results for the doped films, as shown in Figure 4-5, immediately indicate that doping improves the conductivity of the wires as the I-V relationships at high scan rates (500 mV s^{-1} is displayed) maintain a more ideal square shape with increasing doping level. A small increase in capacitance is also observed for 5% doping sample which implies an increase in the electrochemically active surface area for these wires. Strong differences in nanowire morphology between the 3% and 5% doped samples, shown in Figure 4-6, offer a potential explanation for the observed increase in capacitance. The NW films, while being similar in terms of thickness, in the 3% sample are tapered, similar to the intrinsic SiCNWs. The 5% doped nanowire film appears more densely packed with the wires exhibiting random growth directions, a curly-cueish shape and no apparent tapering.

Analysis of the galvanostatic discharge results from the different films enables a more numeric analysis of the total resistance through the samples as well as their power and energy capabilities. A representative result for the doping series, at a discharge rate of 100 µA cm^{-2}, is shown in Figure 4-7 a). The IR drop portion of the discharge cycle, or the vertical region upon switching the current polarity, decreases in magnitude with increasing doping level. The total resistance value for the samples at this discharge rate

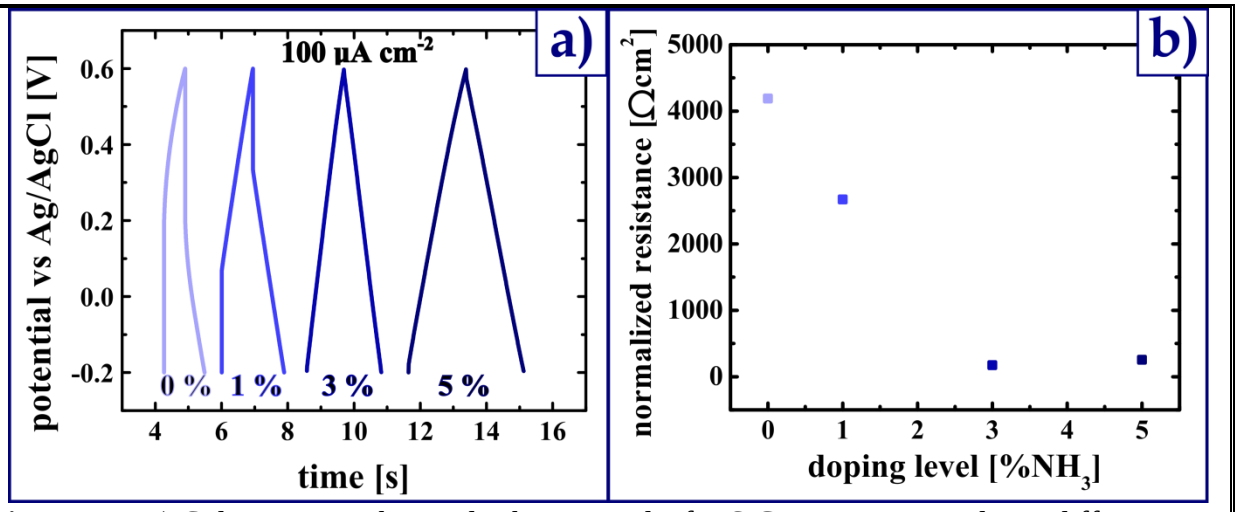


Figure 4-7: a) Galvanostatic charge-discharge results for SiC nanowire samples at different doping levels. b) Plot of normalized resistance for the nanowire film at different doping levels.

is plotted in Figure 4-7 b). Through the addition of ammonia into the reactor gas flow, the normalized resistance of the nanowire films decreases from ~4200 Ω cm at 0% doping, to ~230 Ω cm at 5%. The Ragone plot, shown in Figure 4-8, demonstrates the increase in power and energy capacity of the doped electrodes. As well the trend is clear that with increasing discharge rate (i.e., increasing power) the decrease in energy density occurs at a slower rate for the 5% doped samples as a result of decreased IR drop. The demonstrated doping method is promising for improving the performance of these materials as supercapacitor electrode materials.

Conclusion

The effectiveness of SiC nanowires as aqueous supercapacitor electrodes has been analyzed. The nanowires exhibit specific capacitance values that compare well to the state-of-the-art carbon based electrode values. Furthermore the SiCNWs have been demonstrated as extremely robust in the aqueous system by cycling 2×10^5 times without significant capacitance loss. The intrinsic materials' capacitive behavior begins to degrade as the rate of charge/discharge exceeds 200 mV s^{-1} due to internal resistances. Doping of the nanowires with nitrogen through the addition of ammonia to the precursor flow rate has been evaluated as a technique to reduce the nanowires resistance with over an order of magnitude drop in total resistance achieved at a 5 at% nitrogen. Single nanowire four point probe studies are proposed as a method of quantitatively measuring the change in conductance of individual nanowires, something not possible with the current analysis methods employed in this work. The excellent stability of SiC in harsh environments is attractive for high-temperature

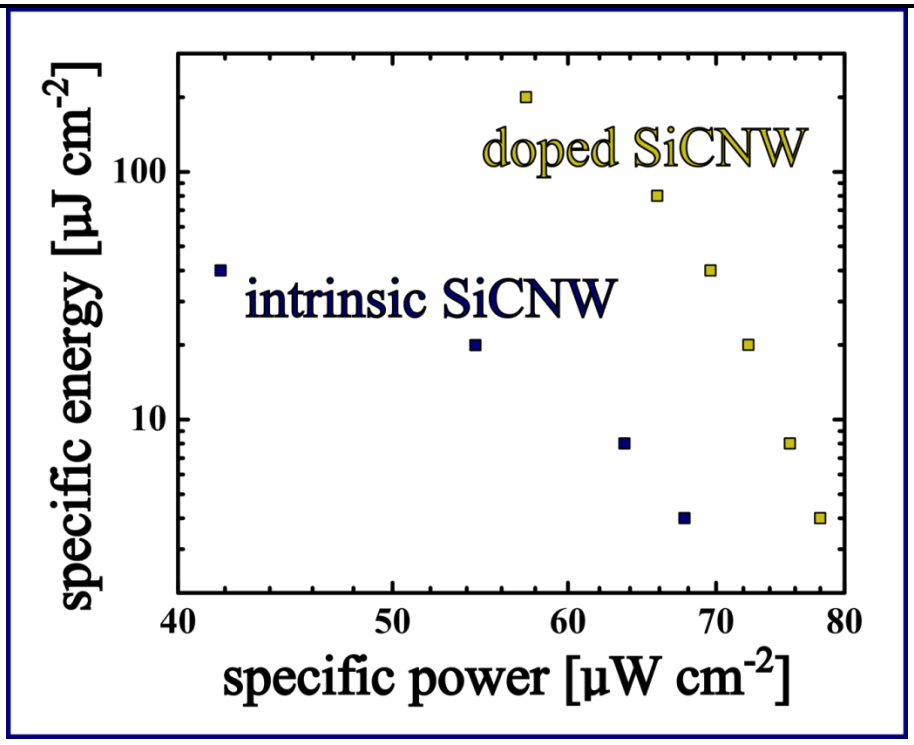


Figure 4-8: Ragone plot comparing the specific energy and power for intrinsic SiC nanowire films and 5 at% nitrogen doped SiC nanowire films.

energy storage applications. These, however, require solid electrolytes with new coating methods for nanowires and are currently under investigation. This work does provide an important basis of comparison for performance of the materials in future harsh environment studies.

Note:

Material from the previous chapter has been adapted in part from the publication:

J. P. Alper, M. S. Kim, M. Vincent, B. Hsia, V. Radmilovic, C. Carraro, and R. Maboudian, "Silicon carbide nanowires as highly robust electrodes for micro-supercapacitors," *Journal of Power Sources*, vol. 230, pp. 298–302, May 2013.

References

[1] J. W. Long, B. Dunn, D. R. Rolison, and H. S. White, "Three-Dimensional Battery Architectures," *Chemical Reviews*, vol. 104, no. 10, pp. 4463–4492, Oct. 2004.

[2] K. Amine, I. Belharouak, Z. Chen, T. Tran, H. Yumoto, N. Ota, S.-T. Myung, and

Y.-K. Sun, "Nanostructured Anode Material for High-Power Battery System in Electric Vehicles," *Advanced Materials*, vol. 22, no. 28, pp. 3052–3057, Jun. 2010.

[3] P. Simon and Y. Gogotsi, "Materials for electrochemical capacitors," *Nature materials*, vol. 7, no. 11, pp. 845–854, 2008.

[4] Y. Q. Jiang, Q. Zhou, and L. Lin, "Planar MEMS supercapacitor using carbon nanotube forests," in *Micro Electro Mechanical Systems, 2009. MEMS 2009. IEEE 22nd International Conference on*, 2009, pp. 587–590.

[5] D. Pech, M. Brunet, P.-L. Taberna, P. Simon, N. Fabre, F. Mesnilgrente, V. Conédéra, and H. Durou, "Elaboration of a microstructured inkjet-printed carbon electrochemical capacitor," *Journal of Power Sources*, vol. 195, no. 4, pp. 1266–1269, Feb. 2010.

[6] F. Liu, A. Gutes, I. Laboriante, C. Carraro, and R. Maboudian, "Graphitization of n-type polycrystalline silicon carbide for on-chip supercapacitor application," *Applied Physics Letters*, vol. 99, no. 11, p. 112104, 2011.

[7] J. P. Alper, M. Vincent, C. Carraro, and R. Maboudian, "Silicon carbide coated silicon nanowires as robust electrode material for aqueous micro-supercapacitor," *Applied Physics Letters*, vol. 100, no. 16, p. 163901, 2012.

[8] C. Liu, Z. Yu, D. Neff, A. Zhamu, and B. Z. Jang, "Graphene-Based Supercapacitor with an Ultrahigh Energy Density," *Nano Letters*, vol. 10, no. 12, pp. 4863–4868, Dec. 2010.

[9] J. Chmiola, C. Largeot, P. L. Taberna, P. Simon, and Y. Gogotsi, "Monolithic Carbide-Derived Carbon Films for Micro-Supercapacitors," *Science*, vol. 328, no. 5977, pp. 480–483, Apr. 2010.

[10] M. Beidaghi and C. Wang, "Micro-supercapacitors based on three dimensional interdigital polypyrrole/C-MEMS electrodes," *Electrochimica Acta*, vol. 56, no. 25, pp. 9508–9514, Oct. 2011.

[11] J. W. Choi, J. McDonough, S. Jeong, J. S. Yoo, C. K. Chan, and Y. Cui, "Stepwise Nanopore Evolution in One-Dimensional Nanostructures," *Nano Letters*, vol. 10, no. 4, pp. 1409–1413, Apr. 2010.

[12] M. Beidaghi, W. Chen, and C. Wang, "Electrochemically activated carbon micro-electrode arrays for electrochemical micro-capacitors," *Journal of Power Sources*, vol. 196, no. 4, pp. 2403–2409, Feb. 2011.

[13] R. Cheung, *Silicon Carbide Micro Electromechanical Systems for Harsh Environments*. Imperial College Press, 2006.

[14] F. Liu, C. Carraro, A. P. Pisano, and R. Maboudian, "Growth and characterization of nitrogen-doped polycrystalline 3C-SiC thin films for harsh environment MEMS applications," *Journal of Micromechanics and Microengineering*, vol. 20, no. 3, p. 035011, Mar. 2010.

[15] H.-J. Choi, H.-K. Seong, J.-C. Lee, and Y.-M. Sung, "Growth and modulation of silicon carbide nanowires," *Journal of Crystal Growth*, vol. 269, no. 2–4, pp. 472–478, Sep. 2004.

[16] A. L. Ortiz, F. Sanchez-Bajo, F. L. Cumbrera, and F. Guiberteau, "X-ray powder diffraction analysis of a silicon carbide-based ceramic," *Materials Letters*, vol. 49, no. 2, pp. 137–145, 2001.

[17] M. B. J. Wijesundara, D. Gao, C. Carraro, R. T. Howe, and R. Maboudian, "Nitrogen doping of polycrystalline 3C-SiC films grown using 1,3-disilabutane in a conventional LPCVD reactor," *Journal of Crystal Growth*, vol. 259, no. 1–2, pp. 18–25, Nov. 2003.

Chapter 5 – Growth of semiconducting nanowires on graphene

Chapter summary

Arrays of semiconducting nanowires have promise for application as electron sources and in energy harvesting and storage. Currently nanowire arrays which are grown at high temperature and harsh conditions require growth on rigid substrates and subsequent transfer to flexible substrates and making good electrical contact is non-trivial. In this chapter a method to transfer silicon and silicon carbide nanowire arrays to arbitrary substrates while maintaining electrical contact through the entire array is described. The nanowires are grown on graphene sheets on SiO_2 coupons. The graphene acts as both the flexible material for maintaining structural continuity and electrical contact through the array during transfer. The SiO_2 acts as the sacrificial growth substrate which is etched after growth in order to release the nanowire/graphene hybrid. The nanowire/graphene hybrids are physically characterized by XRD and electron microscopy. Good electrical contact is confirmed through testing of the SiCNW/graphene hybrids as supercapacitor electrode materials in an aqueous electrolyte. The specific capacitance, ~340 $\mu F\ cm^{-2}$, is similar to SiCNW arrays grown on oxide while the electrical conductivity is improved and cycling stability tests show less than a 1% decrease in capacitance after 10,000 cycles.

Introduction

The field of nano-electronics is rapidly evolving as new and useful scale-dependent properties associated with nano-materials are discovered. Arrays of semiconducting nanowires are particularly attractive for a number of applications as discussed earlier. In secondary battery technology, silicon nanowires (SiNWs) have been shown to reduce the mechanical stresses associated with lithium insertion and extraction [1]. This may enable rechargeable batteries with over ten times the specific capacity of current graphite anodes. SiNW arrays also exhibit greatly enhanced broadband light absorption due to decreased reflectance and transmittance as compared to solid films [2], and are promising in the field of thin film photovoltaics. In addition to Si, the nanoscale electrical and morphological properties of silicon carbide NWs (SiCNWs) including high aspect ratio and low electron affinity make them excellent candidates for field emission cathodes [3]. To date, SiCNW electron emitters have been demonstrated with a lower turn-on field and higher current densities than Si based devices [4]. SiCNWs also show promise as stable materials in electrochemical environments as encountered in aqueous supercapacitors, described in an earlier chapter [5].

Often these semiconducting nanowire arrays are grown from rigid conductive substrates which provide electrical contact to the array, as described above. A flexible conductive substrate however provides many advantages in terms of the applications previously mentioned. Batteries and supercapacitors both benefit from smaller form factors such as the typical rolled cylinder cell. The labor and mounting materials for solar panel installation, ~15% of the total cost per Watt [6], may be significantly reduced by "roll out" light-weight modules. Flexibility also provides greater opportunities for integration of energy storage and harvesting technologies with fabric for use in clothing or lightweight building supplies. In order to realize these benefits, methods must be developed for transferring arrays of nanowires to flexible substrates while maintaining good electrical contact.

Considering the latter issue first, forming electrical contact to nanomaterials is a non-trivial task which has received much attention. Optical lithography [7], electron beam lithography [8], dip-pen nanolithography [9], and focused ion beam methods [10], have been used to contact individual nanowires, nanorods, and nanotubes; however, these are not applicable to arrays of nanomaterials at scale. Evaporation of conductors onto the tips of nanowires is a method which addresses a larger array of nanomaterials, but requires a polymer deposition to prevent shorting, and partial removal of the polymer to expose the nanowires [11].

The post-growth transfer of nanomaterials arrays has been as well the subject of much study. Polymers have been utilized to form a supportive matrix around vertically aligned nanowire arrays which are then transferred to a secondary substrate after mechanical removal from the initial growth substrate. The resulting nanowires may be in a vertical [12,13], or horizontal orientation [14]. Electrical contact is then made to the array by metal evaporation. However, the application of polymer may require a later polymer removal step unless the polymer is incorporated into the device architecture. Wet approaches such as the Langmuir-Blodgett technique are an alternative method of depositing arrays of nanomaterials on substrates [15,16]. This obviates the need to stabilize the entire array prior to transfer, as the materials need only to be dispersed on the surface of a deposition liquid. Still the resulting material lacks precision control of electrical contact points and thus it is not favorable for scalable, array-based devices.

In this chapter a simplified route for the transfer of electrically contacted semiconductor nanowire arrays is described, wherein dense arrays of semiconducting nanowires are grown directly on graphene which may then be transferred to an arbitrary substrate. Graphene was selected due to its flexibility, excellent electrical and optical properties

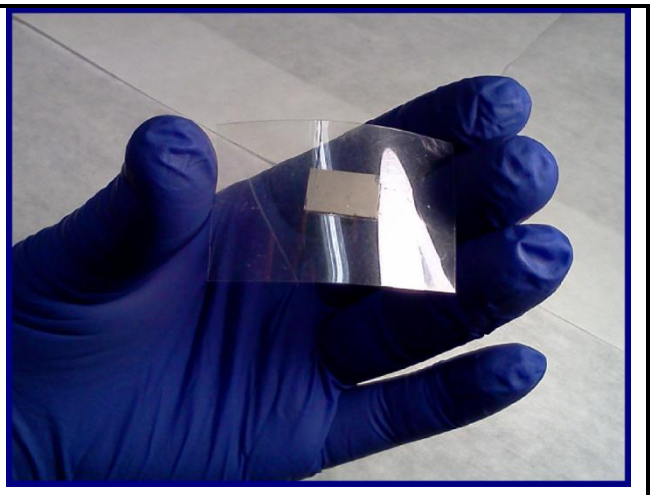


Figure 5-1: SiCNW on graphene transferred onto a flexible plastic substrate.

[17,18], as well as its thermal stability at the utilized nanowire growth temperatures [19]. Transfer techniques for graphene have also been previously developed [20,21], which provided a process framework which has been further optimized in this work. Two catalyst-seeding techniques are utilized to prepare the graphene for the metal catalyzed chemical vapor deposition growth of silicon carbide and silicon nanowires, which indicate that the technique may be extended to a wider array of semiconducting nanomaterials grown with similar methods.

In the case of SiNWs, Au nanoparticle catalysts are deposited via electroless deposition [22], while thin films of evaporated Ni are used to catalyze the SiC nanowires [23]. Prior to nanowire growth, graphene is transferred to a sacrificial support which enables a subsequent transfer of the nanowire/graphene hybrid (NW/G) to any arbitrary substrate post growth, such as a flexible plastic film as shown in Figure 5-1. In this work a 100 nm SiO_2 layer on Si is used as the sacrificial film and later etched in hydrofluoric acid, releasing the NW/G hybrid and allowing it to be floated on a deionized (DI) bath for transfer. The entire process is summarized in Scheme 5-1. While SiO_2 is chosen here as the sacrificial layer, the method can be extended to the use of any number of other growth substrates so long as they withstand the growth conditions for the nanowires and may be etched in a facile manner while not attacking the desired synthesized materials.

The hydrophobic nature of graphene is exploited in floating the NW films on top of the DI rinse bath after HF etching. This method works most consistently with the SiCNW arrays, which are themselves hydrophilic as synthesized (water contact angle of ~0^o). The SiNWs however, being quite hydrophobic after exposure to the HF etching solution, have a tendency to self-associate. This results in the SiNW/G hybrid curling up on itself when placed into the DI rinse bath. It is found that these hybrids are most consistently transferred intact if the SiNW array is not allowed to dry in between removal from the HF bath and placement in the DI rinse bath.

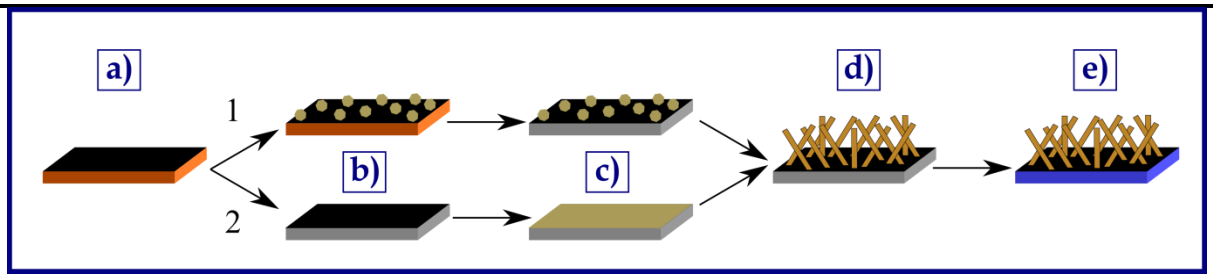
Experimental

Graphene growth

Graphene is grown by chemical vapor deposition on copper as described previously [19]. In short, an 8x2 cm^2 99.998% copper foil of 0.025 mm thickness (Alfa Aesar, USA) is introduced into a quartz tube and heated under vacuum to 1000 ^oC at a rate of ~55 ^oC min^{-1} with a 10 sccm of H_2 flow (Praxair 99.999%). Cu foil is annealed under these conditions for 30 minutes. Then, 20 sccm of methane (Praxair 99.993%) is introduced and maintained for 15 minutes. The samples are then cooled at a rate of ~15 ^oC min^{-1} under the same ambient. When the temperature reaches 600 ^oC all gas flows are stopped and the samples are cooled to room temperature under vacuum (~20 mTorr). The graphene obtained by this method is typically monolayer with small areas of two or three layer patches.

Nanowire catalyst deposition

Graphene decoration with Au nanoparticles for the SiNW growth is performed on the copper/graphene foil via electroless deposition as described in a previous work [22]. In short, graphene on Cu foil is immersed in a 0.2 mM $KAuCl_4$ (Sigma-Aldrich, 98%) solution for 30 seconds, rinsed in de-ionized water and dried under N_2.
Nickel deposition on graphene for the SiCNW growth occurs after transfer of the graphene onto the sacrificial SiO_2 support. The thin film, ~2.2 nm of Ni, is deposited onto the graphene via e-beam evaporation using a Thermionics VE-700 Vacuum



Scheme 5-1: Graphene growth, decoration and transfer process followed by Si and SiC nanowire growth and final transfer. First, a) graphene is grown on a copper foil. For SiNW growth, b.1) graphene is then decorated with gold nanoparticles by galvanic displacement and c.1) transferred to a SiO_2 substrate. For SiCNW growth, b.2) graphene is transferred to a SiO_2 substrate and then c.1) coated with an evaporated Ni film. d) Nanowires are then grown on the graphene via metal catalysed vapor deposition. The nanowire/graphene film is then transferred to an e) arbitrary substrate.

Evaporator. The bare SiO_2 region surrounding the graphene is masked with Teflon tape to ensure it remains Ni free.

Graphene transfer to NW growth substrate

Graphene grown on Cu foil is transferred onto a 100 nm SiO_2 film on Si wafer using a method described previously [20]. Briefly polymethylmethacrylate (PMMA), 8% wt/wt in toluene, is spin coated onto the copper/graphene foil which is subsequently floated on a 1 M $FeCl_3$ (Cu etching) solution. After etching of the Cu, the graphene/PMMA composite is gently lifted out of the solution with a glass slide, rinsed with DI water and allowed to dry in air on the SiO_2 substrate. The PMMA is then removed by dissolution in toluene, an improvement from the referenced procedure. It was found that the slower etching rate of PMMA in toluene, as compared to acetone, reduces the incidence of the graphene film curling onto itself, which may be due to uneven stresses being released in a rapid manner during acetone dissolution.

Nanowire growth

SiNWs are synthesized via a vapor-liquid-solid mechanism as discussed above and elsewhere [24]. Briefly graphene/AuNP on SiO_2 are placed into an atmospheric pressure chemical vapor deposition (CVD) furnace and heated to 850 ^oC, at a rate of ~57 $^oC\ min^{-1}$, under a flow of 200 sccm 10% H_2 in Ar. Then 50 sccm of $SiCl_4$ (Strem Chemicals, 99.9999%) is added to the direct flow and held for 5 minutes. After growth, the $SiCl_4$ flow is stopped and the reactor is cooled down to ~200 ^oC before removing the graphene/SiNW sample.

SiC nanowires are grown from the graphene substrate as described above [23]. SiCNW's are grown from the Ni catalyst in a low-pressure CVD furnace. Samples are heated to 950 ^oC, at a rate of ~55 $^oC\ min^{-1}$ under 10 sccm of H_2. Upon reaching the growth temperature, the flow of hydrogen is reduced to 5 sccm and a 0.5 sccm flow of methyltrichlorosilane (MTS, Sigma-Aldrich, 99%) is introduced to the chamber. Growth is allowed to proceed for 30 min, at which point the MTS flow is stopped and the sample is cooled to room temperature. The entire process takes place at ~5 Torr. These conditions have been shown to result in a nanowire array of approximately 6 μm height [5].

Nanowire on graphene transfer to arbitrary substrate

The nanowire arrays are transferred onto an arbitrary substrate by a sacrificial etch transfer. The SiO_2 film is first etched in hydrofluoric acid (48%) for ~10 minutes. The samples are carefully removed from the solution with the NW/graphene oriented upwards to prevent slipping of the graphene from the Si substrate. The NW/graphene/Si substrates are then slowly introduced to a DI bath at a shallow angle. The interaction between the hydrophobic graphene and water surface results in the NW/graphene film floating on the surface. It is then removed from the surface of the water bath by an arbitrary substrate. In this study, sapphire is used as the substrate to place the SiNW/graphene samples for XRD analysis and a thin plastic film (3M AF4300 transparency film) is used to deposit SiCNW/graphene samples for optical imaging.

Characterization methods

Nanowire morphology is characterized by scanning electron microscopy (SEM) using a NovelX mySEM. Crystal structure is determined using a Siemens D5000 automated X-ray diffractometer (XRD) operated in θ-2θ geometry. Graphene quality determination is performed by confocal Raman spectroscopy (HoribaJY LabRAM, 633 nm laser). Electrochemical testing of the samples is performed by cyclic voltammetry (CHI 660D electrochemical station) in 1 M KCl utilizing a three-electrode cell consisting of an Ag/AgCl reference electrode, Pt wire counter electrode and the NW array as the working electrode. Electrical connection is made directly to the front face of the substrate by Ag epoxy paste deposited into a small region of the SiCNW array. Capacitance, C, is calculated as discussed above using equation (1)

$$C = i\,\frac{dt}{dV} \qquad (1)$$

where i is the current at V=0.2 V during the positive sweep, dV/dt is the scan rate used for the measurement, and A is the projected surface area of the sample immersed in the solution.

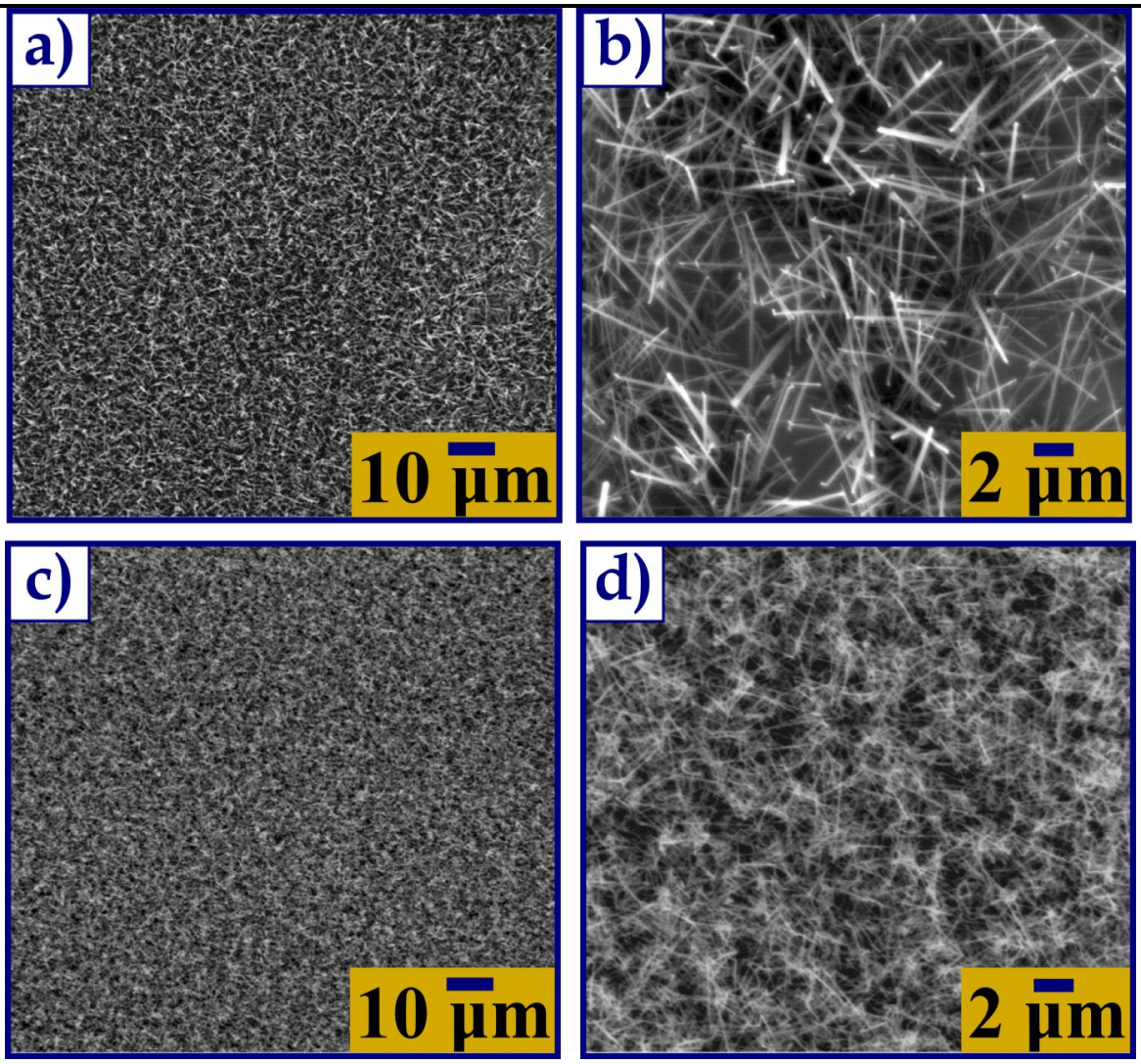


Figure 5-2: SEM of the obtained nanowires on graphene: silicon NWs -a) and b) and silicon carbide NWs - c) and d).

Results and discussion

Physical characterization

Scanning electron microscopy (SEM) analysis of both types of NW/G hybrids after transfer are presented in Figure 5-2. A very dense film of nanowires is achieved for both

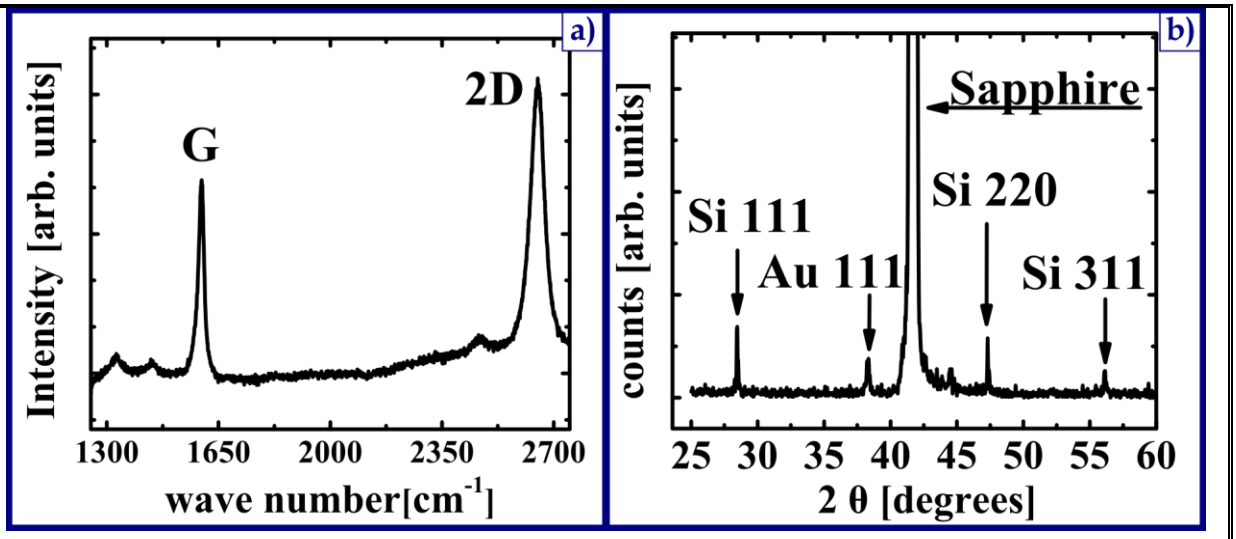


Figure 5-3: a) Raman spectrum of graphene after SiNW growth, using laser excitation wavelength 633 nm. b) XRD spectrum of the SiNW grown on graphene with final transfer on a sapphire substrate.

cases in contrast to previous work on InAs semiconductor nanowire growth from graphene [25]. This is a result of the catalyst seeding and NW growth technique used here whereas the previous work utilized a catalyst free method. Because the catalysts are on top of graphene on amorphous oxide, no preferential growth direction from the substrate is observed for either type of nanowire. The silicon nanowires are highly crystalline as observed from the sharp X-ray diffraction (XRD) spectrum (Figure 5-3 a) taken after transfer of the SiNW/G hybrid to a sapphire substrate. A Raman spectrum taken from the same sample in an Au-free region (Figure 5-3 b) indicates that the graphene is stable during the catalyst decoration process, secondary transfer and NW growth. Raman spectra acquisition of the underlying graphene on the SiC/G hybrid was not possible as broad carbon D and G peaks, indicating a large amount of disordered carbon, were observed and no 2D is peak is present. This is likely due to excess carbon residues in the reactor chamber reacting with the Ni during the nanowire growth and re-precipitating upon cooling, as these peaks are also observed in SiCNW samples grown in the absence of a graphene underlayer, as shown in Figure 5-4. Further TEM studies of the nanowire-graphene interface could resolve the final graphene quality and this work is currently under consideration. Due to the density of the nanowires on the surface of the graphene, transmission of the electrons through the carbon underlayer is not possible without prior removal of the nanowires. Techniques for selective removal of SiC nanowires from the surface are not yet developed.

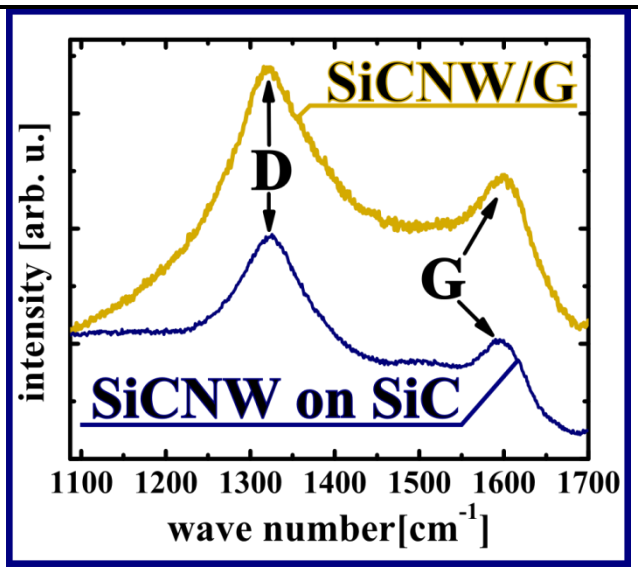


Figure 5-4: Raman spectra for both SiCNW/G and SiCNW/SiC. Note both have a prominent set of disordered carbon peaks.

Electrochemical characterization

As an example of the utility of the NW/G hybrid material, and to demonstrate that good electrical contact between the NW array and the underlying graphene support is achieved, the hybrid material is investigated as an electrode for aqueous supercapacitor applications. A SiC nanowire/graphene sheet on SiO_2 is probed using cyclic voltammetry (CV) over a wide range of scan rates. Results for a SiCNW array grown directly on a thin film of SiC on SiO_2 using the same technique and growth time are used as a comparison. Electrical connection is achieved by the application of epoxy-Ag paste on the arrays. Cyclic voltammetry results indicate that at a scan rate of 100 mV s^{-1} the SiCNW on graphene arrays have somewhat increased capacitance values, ~350 μF cm^{-2}, compared to SiCNWs grown on a thin film of SiC, ~240 μF cm^{-2}, discussed above. This strongly suggests that the entire array is electrically connected. The increase in specific capacitance may be due to the different morphology of the two types of SiCNWs clear from comparing Figure 5-2 to the SEMs presented in chapter 4. These SiCNWs appear to have a more "bird's nest" morphology as opposed to the "bed of needles" appearance of the earlier nanowires. The difference in structure is associated with growth on an amorphous substrate as opposed to a polycrystalline film in the earlier chapter. Figure 5-5 a) shows the cyclic voltammograms of the SiCNW arrays grown on graphene compared to those grown on SiO_2. A very different behavior at a scan rate of 0.5 V s^{-1} can be observed. While the SiCNW/graphene hybrid displays a near ideal capacitive rectangular-shaped current-voltage relationship, the SiCNW/SiO_2 results are quite skewed, indicative of higher internal resistances. These resistances arise from the resistance through the nanowires, the contact resistance between the wires and the substrate, the resistance through the substrate and the contact resistance where electrical connection is made between the testing station and the NW electrode. As the nanowires are grown from the same precursor and catalyst under identical conditions, and connection to the array is made via the same silver epoxy, it is concluded that the

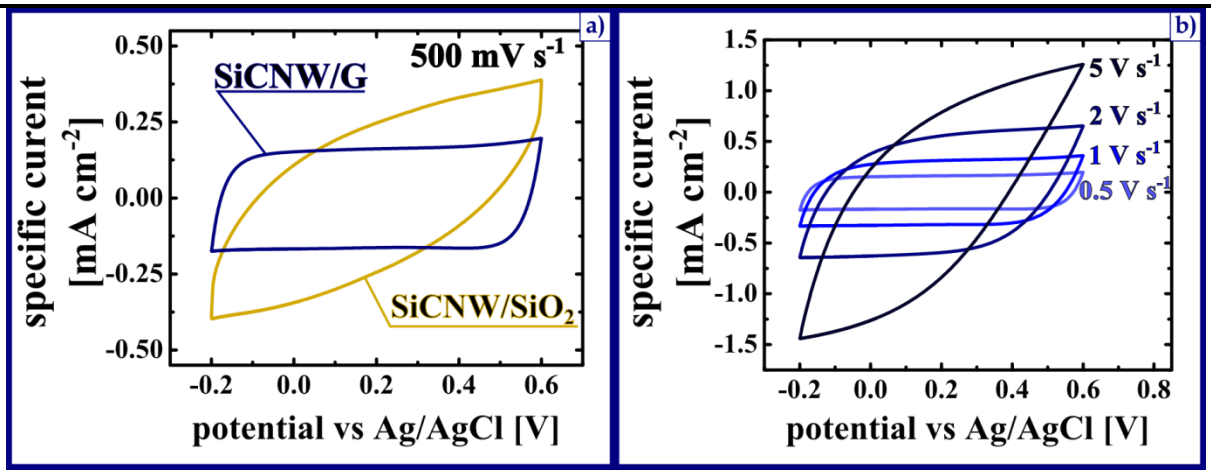


Figure 5-5: a) Comparison between cyclic voltammetry results for SiCNWs grown on graphene vs. those grown on oxide at a scan rate of 500 mV s^{-1}. b) Cyclic voltammetry results for the SiCNW/G hybrid material over a range of scan rates.

resistance at the wire-substrate interface and the resistance through substrate are the main contributing factors to the difference between the CV behaviors of the two tested materials. The contact between the nanowires grown in the absence of graphene may be due to the physical contact between the wires in the nest-like morphology. In contrast, the NW/graphene composite, with greatly enhanced conductivity through the array, is expected to be in contact through the graphene underlayer.

The extent of this difference can be qualitatively demonstrated with the same technique by considering the results for cyclic voltammetry on the SiCNW/graphene over a wider range of scan rates, as shown Figure 5-5 b). The SiCNW/graphene hybrid maintains near ideal performance through a scan rate of 2 V s^{-1}. It has been shown that graphitic interlayers can reduce the contact resistance between the deposited SiC thin films and metal contacts [26], and thus it seems reasonable that with improved graphene growth and transfer techniques, a graphene interlayer may be used to the advantage of the electronic materials engineer when designing hybrid conductive structures. The robustness of the NW/G hybrid material is confirmed by performing 10,000 complete charge/discharge cycles in an aqueous electrolyte at a scan rate of 5 V s^{-1}. Figure 5-6 shows the negligible reduction in capacitance measured after this time, indicating high stability during electrochemical cycling.

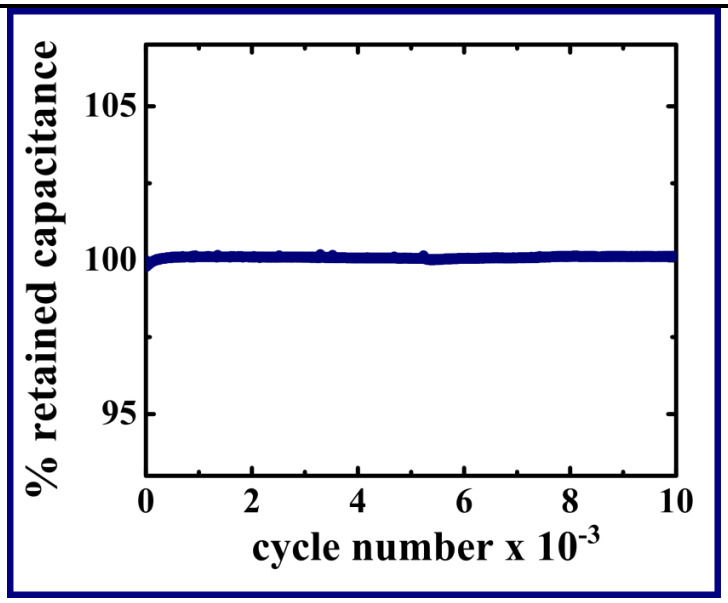


Figure 5-6: Capacitance rention of SiCNW with increasing cycle number.

Conclusions

In summary silicon and silicon carbide nanowires have been successfully grown directly on graphene and transferred onto arbitrary substrates. Silicon nanowires are grown by metal catalyzed CVD using gold deposited on graphene by an electroless deposition before PMMA transfer. SiC nanowires are synthesized with a similar process using evaporated nickel on top of graphene after PMMA transfer. SEM confirmed the nanowire structure of both semiconductors on graphene. Raman spectroscopy revealed graphene stability after SiNW growth while electrochemical measurements revealed the excellent contact between SiC nanowires and graphene, opening the possibility of using this new hybrid material for energy storage devices among others. Transfer of arrays of these semiconducting wires to arbitrary substrates is demonstrated. This general technique, which combines a number of previously published methods in a novel way, provides an important framework for future implementation of semiconducting nanowires into next generation devices.

Note:

Material from the previous chapter has been adapted in part from the publication:

J. P. Alper, A. Gutes, C. Carraro, and R. Maboudian, "Semiconductor nanowires directly grown on graphene – towards wafer scale transferable nanowire arrays with improved electrical contact," *Nanoscale*, vol. 5, no. 10, p. 4114, 2013.

References

[1] C. K. Chan, H. Peng, G. Liu, K. McIlwrath, X. F. Zhang, R. A. Huggins, and Y. Cui, "High-performance lithium battery anodes using silicon nanowires," *Nature Nanotechnology*, vol. 3, no. 1, pp. 31–35, Jan. 2008.

[2] L. Tsakalakos, J. Balch, J. Fronheiser, B. A. Korevaar, O. Sulima, and J. Rand, "Silicon nanowire solar cells," *Applied Physics Letters*, vol. 91, no. 23, p. 233117, 2007.

[3] K. Zekentes and K. Rogdakis, "SiC nanowires: material and devices," *Journal of Physics D: Applied Physics*, vol. 44, no. 13, p. 133001, Apr. 2011.

[4] E. Spanakis, J. Dialektos, E. Stratakis, V. Zorba, P. Tzanetakis, and C. Fotakis, "Ultraviolet laser structuring of silicon carbide for cold cathode applications," *physica status solidi (c)*, vol. 5, no. 10, pp. 3309–3313, Aug. 2008.

[5] J. P. Alper, M. S. Kim, M. Vincent, B. Hsia, V. Radmilovic, C. Carraro, and R. Maboudian, "Silicon carbide nanowires as highly robust electrodes for micro-supercapacitors," *Journal of Power Sources*, vol. 230, pp. 298–302, May 2013.

[6] R. Wiser, G. Barbose, and C. Peterman, "Tracking the Sun: The Installed Cost of Photovoltaics in the U.S. From 1998-2007." Lawrence Berkeley National Lab Internal Report, 2009.

[7] M. E. Toimil Molares, E. M. Hohberger, C. Schaeflein, R. H. Blick, R. Neumann, and C. Trautmann, "Electrical characterization of electrochemically grown single copper nanowires," *Applied Physics Letters*, vol. 82, no. 13, p. 2139, 2003.

[8] M. Bockrath, "Single-Electron Transport in Ropes of Carbon Nanotubes," *Science*, vol. 275, no. 5308, pp. 1922–1925, Mar. 1997.

[9] W. M. Wang, M. C. LeMieux, S. Selvarasah, M. R. Dokmeci, and Z. Bao, "Dip-Pen Nanolithography of Electrical Contacts to Single-Walled Carbon Nanotubes," *ACS Nano*, vol. 3, no. 11, pp. 3543–3551, Nov. 2009.

[10] T. W. Ebbesen, H. J. Lezec, H. Hiura, J. W. Bennet, H. F. Ghaemi, and T. Thio, "Electrical conductivity of individual carbon nanotubes," *Nature*, vol. 382, pp. 54 – 56, 1996.

[11] A. R. Abramson, W. C. Kim, S. T. Huxtable, H. Yan, Y. Wu, A. Majumdar, C.-L. Tien, and P. Yang, "Fabrication and Characterization of a Nanowire/Polymer-Based

Nanocomposite for a Prototype Thermoelectric Device," *Journal of Microelectromechanical Systems*, vol. 13, no. 3, pp. 505–513, Jun. 2004.

[12] M. C. McAlpine, H. Ahmad, D. Wang, and J. R. Heath, "Highly ordered nanowire arrays on plastic substrates for ultrasensitive flexible chemical sensors," *Nature Materials*, vol. 6, no. 5, pp. 379–384, May 2007.

[13] J. M. Spurgeon, S. W. Boettcher, M. D. Kelzenberg, B. S. Brunschwig, H. A. Atwater, and N. S. Lewis, "Flexible, Polymer-Supported, Si Wire Array Photoelectrodes," *Advanced Materials*, vol. 22, no. 30, pp. 3277–3281, Aug. 2010.

[14] Y.-K. Chang and F. C.-N. Hong, "The fabrication of ZnO nanowire field-effect transistors by roll-transfer printing," *Nanotechnology*, vol. 20, no. 19, p. 195302, May 2009.

[15] D. Whang, S. Jin, Y. Wu, and C. M. Lieber, "Large-Scale Hierarchical Organization of Nanowire Arrays for Integrated Nanosystems," *Nano Letters*, vol. 3, no. 9, pp. 1255–1259, Sep. 2003.

[16] L. Mai, Y. Gu, C. Han, B. Hu, W. Chen, P. Zhang, L. Xu, W. Guo, and Y. Dai, "Orientated Langmuir−Blodgett Assembly of VO_2 Nanowires," *Nano Letters*, vol. 9, no. 2, pp. 826–830, Feb. 2009.

[17] K. S. Novoselov, "Electric Field Effect in Atomically Thin Carbon Films," *Science*, vol. 306, no. 5696, pp. 666–669, Oct. 2004.

[18] R. R. Nair, P. Blake, A. N. Grigorenko, K. S. Novoselov, T. J. Booth, T. Stauber, N. M. R. Peres, and A. K. Geim, "Fine Structure Constant Defines Visual Transparency of Graphene," *Science*, vol. 320, no. 5881, pp. 1308–1308, Jun. 2008.

[19] X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo, and R. S. Ruoff, "Large-Area Synthesis of High-Quality and Uniform Graphene Films on Copper Foils," *Science*, vol. 324, no. 5932, pp. 1312–1314, Jun. 2009.

[20] A. Reina, H. Son, L. Jiao, B. Fan, M. S. Dresselhaus, Z. Liu, and J. Kong, "Transferring and Identification of Single- and Few-Layer Graphene on Arbitrary Substrates," *The Journal of Physical Chemistry C*, vol. 112, no. 46, pp. 17741–17744, Nov. 2008.

[21] K. S. Kim, Y. Zhao, H. Jang, S. Y. Lee, J. M. Kim, K. S. Kim, J.-H. Ahn, P. Kim, J.-Y. Choi, and B. H. Hong, "Large-scale pattern growth of graphene films for stretchable transparent electrodes," *Nature*, vol. 457, no. 7230, pp. 706–710, Feb. 2009.

[22] A. Gutés, B. Hsia, A. Sussman, W. Mickelson, A. Zettl, C. Carraro, and R.

Maboudian, "Graphene decoration with metal nanoparticles: Towards easy integration for sensing applications," *Nanoscale*, vol. 4, no. 2, p. 438, 2012.

[23] H.-J. Choi, H.-K. Seong, J.-C. Lee, and Y.-M. Sung, "Growth and modulation of silicon carbide nanowires," *Journal of Crystal Growth*, vol. 269, no. 2–4, pp. 472–478, Sep. 2004.

[24] G. S. Doerk, N. Ferralis, C. Carraro, and R. Maboudian, "Growth of branching Si nanowires seeded by Au–Si surface migration," *Journal of Materials Chemistry*, vol. 18, no. 44, p. 5376, 2008.

[25] Y. J. Hong, W. H. Lee, Y. Wu, R. S. Ruoff, and T. Fukui, "van der Waals Epitaxy of InAs Nanowires Vertically Aligned on Single-Layer Graphene," *Nano Letters*, vol. 12, no. 3, pp. 1431–1436, Mar. 2012.

[26] F. Liu, B. Hsia, C. Carraro, A. P. Pisano, and R. Maboudian, "Enhanced Ohmic contact via graphitization of polycrystalline silicon carbide," *Applied Physics Letters*, vol. 97, no. 26, p. 262107, 2010.

Chapter 6 – Looking forward

The previous chapters demonstrate that significant progress is being made towards harnessing the benefits of nanowires for energy storage applications. Deeper insight into the synthesis processes is enabling this progress along with a better understanding of how processing steps effects performance. But there is still much to learn and discover. New applications, simpler synthesis methods, improved parameters for better control of purity, orientation, and structure are all worthy pursuits. Hybridized structures, such as those discussed in chapter 5, open even more doors for nanomaterials to play a role in developing technology. Building upon these and implementing hierarchical designs which bridge length scales in three dimensions is another area deserving of interest as potentially enabling technology for putting nanotechnology to macro utility.

Specific applications beyond supercapacitors which appear poised to benefit from semiconducting nanowires' properties include other energy storage and generation technologies. Silicon anodes for Li-ion batteries have been shown to benefit from reduction of mechanical stress during Li insertion, which can result in up to a 300% volume expansion [1]. Arrays of silicon nanowires increase the light collection of thin film photovoltaics by ~30% when compared to planar silicon cells [2]. Etched silicon nanowires also show improved activity in photoelectrochemical water splitting [3]. Silicon carbide nanowires improve both the stability and performance of field emission electrodes due to their low electron affinity and high aspect ratios [4]. It is impossible to tell what other fields may find use for these materials, but it is quite possible there will be many.

As with any new technology, it is also important that study of the consequences resulting from the synthesis and application of these nanomaterials at scale is also attended to. It has already been shown that carbon nanotubes have size dependent cellular uptake rates [5] and silica nanowires exhibit aspect ratio dependent toxicity and tetrogenicity [6]. Transport and persistence of these materials in the environment are especially important to safe and sustainable application. Fundamental understanding of these material properties may even generate potential for new applications in medicine such as targeted drug delivery or implantable sensors.

References

[1] C. K. Chan, H. Peng, G. Liu, K. McIlwrath, X. F. Zhang, R. A. Huggins, and Y. Cui, "High-performance lithium battery anodes using silicon nanowires," *Nature Nanotechnology*, vol. 3, no. 1, pp. 31–35, Jan. 2008.

[2] M.-Y. Shih, S. F. LeBoeuf, M. Pietrzykowski, O. V. Sulima, J. Rand, A. Davuluru, U. Rapol, L. Tsakalakos, J. Balch, and P. J. Codella, "Strong broadband optical absorption in silicon nanowire films," *Journal of Nanophotonics*, vol. 1, no. 1, pp. 013552–013552, 2007.

[3] A. P. Goodey, S. M. Eichfeld, K.-K. Lew, J. M. Redwing, and T. E. Mallouk, "Silicon Nanowire Array Photoelectrochemical Cells," *Journal of the American Chemical Society*, vol. 129, no. 41, pp. 12344–12345, Oct. 2007.

[4] M.-G. Kang, H. J. Lezec, and F. Sharifi, "Stable field emission from nanoporous silicon carbide," *Nanotechnology*, vol. 24, no. 6, p. 065201, Feb. 2013.

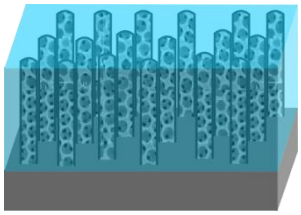
[5] H. Jin, D. A. Heller, R. Sharma, and M. S. Strano, "Size-Dependent Cellular Uptake and Expulsion of Single-Walled Carbon Nanotubes: Single Particle Tracking and a Generic Uptake Model for Nanoparticles," *ACS Nano*, vol. 3, no. 1, pp. 149–158, Jan. 2009.

[6] S. M. Nelson, T. Mahmoud, M. Beaux, P. Shapiro, D. N. McIlroy, and D. L. Stenkamp, "Toxic and teratogenic silica nanowires in developing vertebrate embryos," *Nanomedicine: Nanotechnology, Biology and Medicine*, vol. 6, no. 1, pp. 93–102, Feb. 2010.

Appendix I – Theoretical maximum capacitance for porous silicon nanowires

Theoretical maximum capacitance value of porous silicon nanowire array:

The total volume occupied by the porous Si nanowire array (VPSiNW) depicted in the blue box below, is equal to sum of the volume occupied by the pores (V_{pore}) and the silicon (V_{si}) divided by the fill factor 0.4, or fraction of total volume occupied by nanowires [1]:



or,

$$V_{PSiNW}\ \mathrm{cm}^3_{\mathrm{PSiNW}} = \left(V_{pore}\ \mathrm{cm}^3_{\mathrm{pore}} + V_{si}\ \mathrm{cm}^3_{\mathrm{si}}\right)/\ 0.4$$

The specific volume of the PSiNW, ($\tilde{V}_{\mathrm{PSiNW}}$) array is the volume divided by the total mass of silicon (m_{si}) in the array.

$$\tilde{\mathrm{V}}_{PSiNW}\ \frac{\mathrm{cm}^3_{\mathrm{PSiNW}}}{\mathrm{g}_{\mathrm{PSiNW}}} = \left(\frac{V_{pore}}{m_{si}}\ \frac{\mathrm{cm}^3_{\mathrm{pore}}}{\mathrm{g}_{\mathrm{si}}} + \frac{V_{si}}{m_{si}}\ \frac{\mathrm{cm}^3_{\mathrm{si}}}{\mathrm{g}_{\mathrm{si}}}\right)/\ 0.4$$

We can substitute the reported values for the density of silicon and the specific pore volume (Hochbaum, 2009) and calculate $\tilde{V}_{\mathrm{PSiNW}}$:

$$\tilde{\mathrm{V}}_{PSiNW}\ \frac{\mathrm{cm}^3_{\mathrm{PSiNW}}}{\mathrm{g}_{\mathrm{PSiNW}}} = \left(0.88\frac{\mathrm{cm}^3_{\mathrm{pore}}}{\mathrm{g}_{\mathrm{PSiNW}}} + \left(\frac{1}{2.31}\right)\frac{\mathrm{cm}^3_{\mathrm{si}}}{\mathrm{g}_{\mathrm{Si}}}\right)/\ 0.4 = 3.275\ \frac{\mathrm{cm}^3_{\mathrm{PSiNW}}}{\mathrm{g}_{\mathrm{PSiNW}}}$$

We can now calculate the expected value for the specific interfacial area for a film of PSiNWs ($\tilde{A}_{\mathrm{PSiNW}}$) with a known wire length (L [cm]) and capacitance per projected area (C [mF $\mathrm{cm}^{-2}_{\mathrm{projected}}$]):

$$\frac{\tilde{\mathrm{V}}_{PSiNW}}{L_{PSiNW}} \cdot \frac{C_{PSiNW}}{C_{Si}} = \tilde{\mathrm{A}}_{PSiNW}$$

where C_{Si} is the capacitance per projected area of planar silicon as measured in our laboratory (0.02 mF $cm^{-2}_{projected}$). We may then compare this to the actual area as measured for nanowires synthesized with this technique, 3.42 x 10^6 cm^2 g^{-1} [1].

Table AI-1: Summary of the specific capacitance and % theoretical interfacial area which is electrochemically active as calculated from above equations for various C/PSiNW array lengths. Error is two standard deviations calculated based on measurements made over 10 cross sectional SEM images.

Wire Length [µm]	specific capacitance [mF cm^{-2}] measured at 1 mA cm^{-2} discharge rate	% Theoretical Interfacial Area [-]
24 ± 6.0	**49**	**97 ± 19**
37 ± 10	**85**	**108 ± 22**
57. ± 6	**134**	**102 ± 10**
120 ± 27	**328**	**107 ± 24**

Reference

[1] A. I. Hochbaum, D. Gargas, Y. J. Hwang, and P. Yang, "Single Crystalline Mesoporous Silicon Nanowires," *Nano Letters*, vol. 9, no. 10, pp. 3550–3554, Oct. 2009.

Appendix II – Preliminary results: SiCNW growth kinetics, flow rate dependency, substrate dependent orientation, and crystal structure

This appendix presents data collected which does not constitute a completed study but is presented for the use of the reader. The general method presented in Chapter 4 has been further investigated to determine the kinetics of nanowire growth, precursor flow rate dependency of axial and radial growth rates, substrate dependent nanowire growth orientation, and SiCNW crystal structure. Catalyst thickness, pressure, temperature, and MTS:H_2 ratio were all kept constant and are consistent with the parameters found in chapter 4 for doped SiCNW growth. For more discussion of how these factors affect SiC nanowire growth utilizing similar systems, the reader is directed to the relevant literature [1], [2].

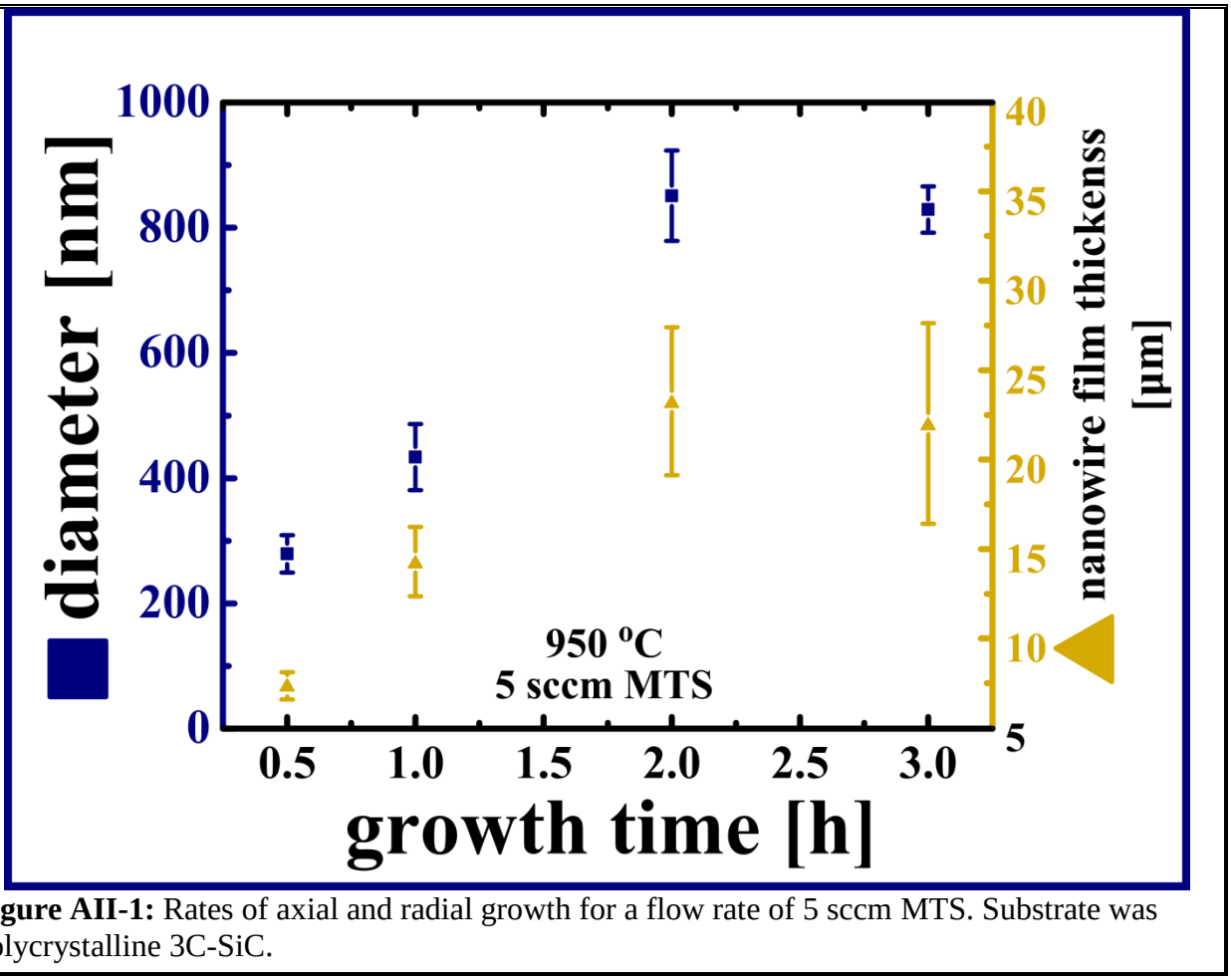


Figure AII-1: Rates of axial and radial growth for a flow rate of 5 sccm MTS. Substrate was polycrystalline 3C-SiC.

Appendix II – Preliminary results: SiCNW growth kinetics, flow rate dependency, substrate dependant orientation, and crystal structure

Growth kinetics for feed gas consisting of 5 sccm MTS, 100 sccm H_2

Figure AII-1 provides some insight into the growth kinetics. First it should be noted that the diameter of the nanowires increases with increasing growth time. This is contrary to what is observed in VLS growth of Si where the initial catalyst droplet determines the diameter of the resulting nanowire, with extended growth times only extending the SiNW length [3]. Secondly it appears that there is a plateau reached, sometime between 1-2 hours of growth, under these conditions. This may be due to catalyst loss through etching or incorporation into the nanowire structure.

In order to determine a conclusive kinetic model, more data is required at short and mid time points, and is the focus of current and future work.

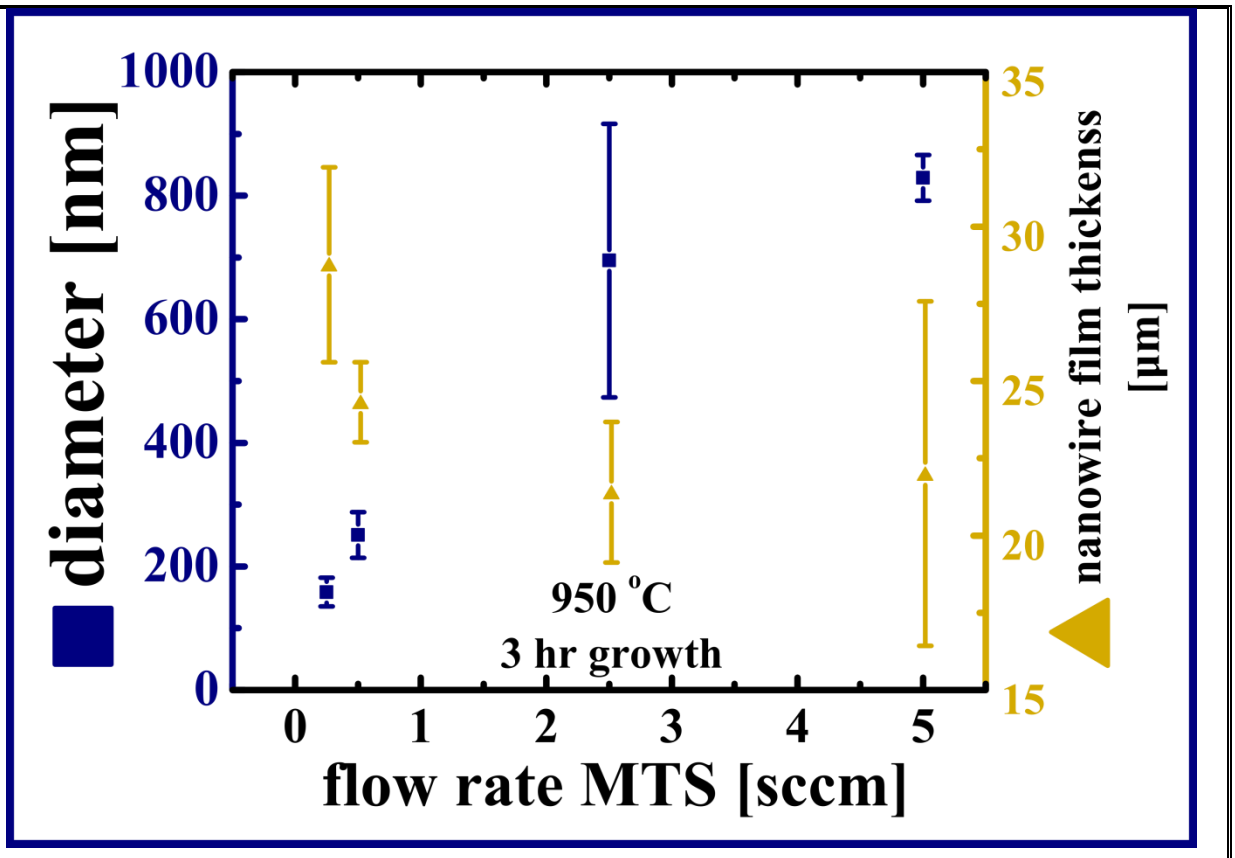


Figure AII-2: Effect of MTS flow rate on SiCNW axial and radial growth rate.

Appendix II – Preliminary results: SiCNW growth kinetics, flow rate dependency, substrate dependant orientation, and crystal structure

Effect of MTS flow rate on axial and radial growth rate

Considering Figure AII-2 there is an effect of MTS flow rate on radial growth rate. With increasing MTS flow rate, the resulting diameter of SiCNWs after a three hour growth rate tends to be greater. It also appears that a plateau for this phenomena may be occurring between 0.5 sccm and 2.5 sccm MTS. One theory for this behavior is that at lower flow precursor flow rates all of the MTS is consumed at the catalyst and only contributes to axial growth (and indeed the axial growth rate for 0.5 sccm and 5 sccm do not vary to a statistically significant amount) while at higher flow rates, MTS is present in excess and may react on the nanowire sidewalls and directly deposit SiC. However, that would imply that the axial growth should continue as long as MTS is present, while in figure AII-1 it is demonstrated that radial growth reaches a plateau as well. Further work to elucidate the exact mechanism of growth is required to develop a consistent theory for this behavior. An important first step will be to collect data for more flow rates of MTS and at shorter time points than 3 hours.

Substrate effect on wire orientation

The alignment of nanowires is important for field emission applications, however it was shown in chapters 4 and 5 that vertical orientation is not achieved when SiCNWs are grown from polycrystalline 3C or amorphous oxide. Figure AII-3 presents SEM images of SiCNWs grown with 1 sccm MTS for 45 minutes from single crystalline Si(100), 3C-SiC (111), and 4H-SiC substrates. Preferential vertical orientation is observed for 4H substrates. Si(100) appears to exhibit the most disordered growth while 3C-SiC (111) substrates yield something intermediate.

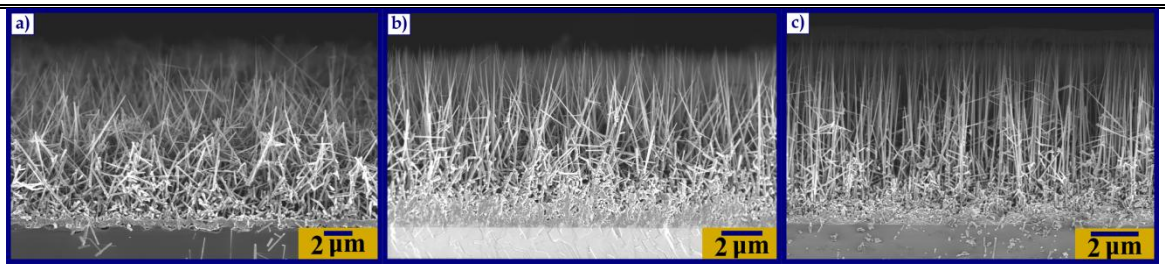


Figure AII-3: SEM results for SiCNWs grown on single crystal a) Si(100), b) 3C-SiC (111), c) 4H-SiC.

Appendix II – Preliminary results: SiCNW growth kinetics, flow rate dependency, substrate dependant orientation, and crystal structure

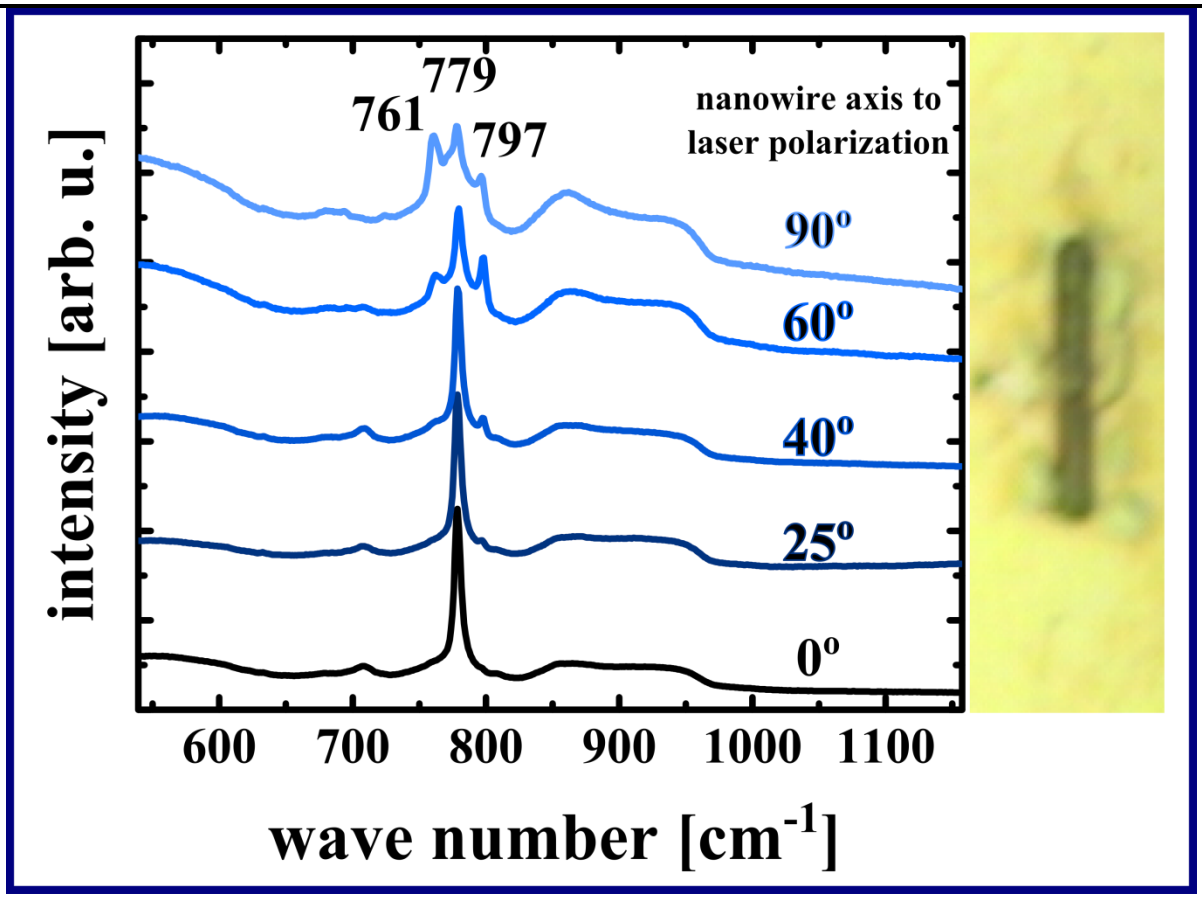


Figure AII-4: Single wire Raman spectroscopy results on SiC nanowire. Outset is optical image of nanowire.

Raman investigation of crystal structure

SiCNWs grown using this method have been claimed to be cubic based on XRD results [1]. However, as stated in chapter 4, the stacking of hexagonal and cubic forms of SiC have the same atomic spacing, and thus will yield identical primary XRD peak locations. Raman spectroscopy, a polytype sensitive analysis tool [4], has been employed in this work to probe the crystal structure of single nanowires. As shown in Figure AII-4, folded transverse optical modes exist which vary in intensity with nanowire orientation in respect to incident polarization. This is a clear indication of an axial structure, as opposed to an isostrpopic cubic structure [5]. The peak locations do

not conclusively point to a documented heaxagonal or rhombic structure [4], [6]. A determination of the best fitting structure may be possible with high resolution scanning transmission electron microscopy along the length of single nanowires. Work is currently ongoing to collect this information.

References

[1] H.-J. Choi, H.-K. Seong, J.-C. Lee, and Y.-M. Sung, "Growth and modulation of silicon carbide nanowires," *Journal of Crystal Growth*, vol. 269, no. 2–4, pp. 472–478, Sep. 2004.

[2] Y. F. Chen, X. Z. Liu, and X. W. Deng, "Factors affecting the growth of SiC nano-whiskers," *Journal of Material Science Technology*, vol. 26, no. 11, pp. 1041–1046, 2010.

[3] K. Kolasinski, "Catalytic growth of nanowires: Vapor–liquid–solid, vapor–solid–solid, solution–liquid–solid and solid–liquid–solid growth," *Current Opinion in Solid State and Materials Science*, vol. 10, no. 3–4, pp. 182–191, Jun. 2006.

[4] S. Nakashima and H. Harima, "Raman investigatino of SiC polytypes," *Physica Status Solidi.A, Applied Research*, vol. 162, no. 32, pp. 39–64, 1997.

[5] D. W. Feldman, J. H. Parker Jr, W. J. Choyke, and L. Patrick, "Phonon Dispersion Curves by Raman Scattering in SiC, Polytypes 3 C, 4 H, 6 H, 1 5 R, and 2 1 R," *Physical Review*, vol. 173, no. 3, p. 787, 1968.

[6] S. Nakashima, K. Kisoda, and J.-P. Gauthier, "Raman determination of structures of long-period SiC polytypes," *Journal of applied physics*, vol. 75, no. 10, pp. 5354–5360, 1994.

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