UNIVERSITY OF CALIFORNIA, SAN DIEGO

# Digitally Controlled Microwave Power Amplifier Design Techniques for Wireless Communications

A dissertation submitted in partial satisfaction of the
requirements for the degree Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

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2017

The dissertation of Varish Diddi is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

University of California, San Diego
2017

DEDICATION

*To my family*

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Chapter 3 is mostly a reprint of the material as it appears in "High Power Digital Doherty Polar Power Amplifier in CMOS SOI", V. Diddi, H. Gheidi, J. Buckwalter and P. Asbeck, submitted for publication in IEEE Transactions on Microwave Theory and Techniques and the material in "High-power, high-efficiency digital polar Doherty power amplifier for cellular applications in SOI CMOS", V. Diddi, H. Gheidi, J. Buckwalter and P. Asbeck, IEEE PAWR 2016. The author of this dissertation was the primary investigator and primary author for this material.

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ABSTRACT OF THE DISSERTATION

# Digitally Controlled Microwave Power Amplifier Design Techniques for Wireless Communications

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Professor Peter M. Asbeck, Chair

In order to meet the increasing demand of high data rate mobile broadband communication, newer standards increasingly employ spectrally efficient high order modulation schemes, which lead to large peak-to-average ratio (PAPR) of transmitted signals. To drive down the cost and form factor, a significant portion of the active circuitry in today's commercial handsets is implemented in silicon CMOS technology –

except for the power amplifier (PA). Silicon technology comes with low breakdown voltage, however, limiting the output power of the PA. Recent work has shown that series-connection of Si FETs (the "Stacked-FET" technique) can overcome the breakdown issue of silicon CMOS FETs to implement high power PAs. This can enable the use of scaled CMOS technology nodes which are optimized for digital logic circuits, to implement high performance PAs. The PAs, moreover, can make use of the digital circuits available to produce compact integrated circuits that are less dependent on microwave matching techniques than their counterparts. This work investigates the design and implementation of high output power, digitally-intensive PA CMOS architectures and their extensions for wireless transmitters that are highly efficient, even for signals with high peak-to-average ratio.

In the first part of this work, a digitally modulated PA (DPA) is implemented in polar architecture on 180 nm CMOS SOI technology. The amplitude modulation input signal is a 10-bit digital word controlling the number of active unit cells – each unit cell being a stacked FET PA. The DPA is also driven by a constant amplitude phase modulated (PM) signal centered at RF. The demonstrated DPA provides output power of 1.45 W at 900 MHz with drain efficiency of 65.9%. The power and efficiency are adequate for use in cellular handsets for 3G and 4G standards. The DPA can transmit WCDMA and LTE signals at 900 MHz and is functional from 800 MHz to 2.4 GHz with different matching networks. This DPA is a multi-band, multi-standard PA and is used as a building block for additional designs in this work.

The back-off efficiency enhancement of PA is critical to efficiently transmit signals of high PAPR from hand-sets. In the second part of the work, two identical DPAs

are used to implement a digitally modulated Doherty power amplifier (DDPA). This part of the work investigates the challenges and develops the techniques for achieving strong efficiency peaking in output power back-off for CMOS Doherty PAs at microwave frequencies. The output combiner needed within the Doherty architecture is realized using surface-mount components on a printed circuit board (PCB). Digital AM signals to both DPAs are independently provided as inputs. The phase difference between RF PM inputs of main and peaking DPAs can also be varied. The peak output power of CMOS DDPA at 900 MHz is >2 W (highest reported in the literature) with drain efficiency of 55.5%, while at 6 dB back-off the drain efficiency is 52.6%. The back-off efficiency and its improvement relative to class-B is highest reported in the literature for any CMOS Doherty implementation. The DDPA is demonstrated to transmit 5 MHz 64-QAM OFDM signal with very good linearity of ACPR better than -35.9 dB and EVM of 3.8%.

For applications like femto-cell base-stations, where the power needed is large, technologies like Gallium Nitride (GaN) work better than silicon because of superior voltage handling. The challenge here lies in efficiently driving the GaN FETs. The DPA developed in this work can provide large enough voltage to directly drive the input of GaN FET, thanks to the use of FET stacking. A novel architecture is demonstrated in which the CMOS DPA drives the GaN FET, which is connected as a common gate stage, with no inter-stage matching. The GaN FET in turn drives a 50 Ω load directly. The absence of any impedance matching network (with its associated bandwidth limitation) makes this PA wideband. Key design aspects of this architecture, including bandwidth limitation caused by circuit parasitics, are discussed in this work. A digitally controlled PA with a combination of CMOS and GaN (Mitsubishi Electric 0.75 μm process) is

demonstrated. The CMOS-GaN PA operates over a 2.4:1 frequency range for 1dB output power variation (500 MHz to 1.2 GHz); output power varies from 2.4 W to 3 W with efficiency between 48% to 74%. This PA is demonstrated to transmit 5 MHz, 64 QAM signal at various frequencies. These characteristics make this amplifier a candidate for application in femtocells and microcells.

# Chapter 1

# Introduction

Research interest in wireless communication can be traced back to the 19th century. In 1873 James Clark Maxwell published *A Treatise on Electricity and Magnetism*. Before 1890, Heinrich Hertz demonstrated the generation of electromagnetic waves and their properties similar to light [1]. In 1895 J. C. Bose gave a public demonstration of electromagnetic waves, using them to ring a bell remotely and to explode some gunpowder in Kolkata [2]. In 1986 it was reported that the distance of communication for Bose's apparatus was nearly a mile. During the same year, Alexander Popov demonstrated wireless transmission of Morse signals across 200 meters at St. Petersburg University [3]. On December 12th 1901 Marconi sent and received wireless signals across the Atlantic Ocean for the first time [3, 4]. For the contributions to the development wireless telegraphy, Marconi was awarded the Nobel Prize in 1909.

On April 3rd of 1973, Martin Cooper, a researcher at Motorola made the first call using the first cellphone in Manhattan, New York. This phone weighed more than a kilogram and would take 10 hours to charge while could be used to talk for 30 minutes. Several other technological advances fueled the birth and evolution of cellular

communication -- most notably, demonstration of PNP point-contact transistor in 1947 at Bell Labs and further advances in semiconductor device technology. A decade later, concepts of frequency reuse and hand-offs were developed. The first generation cellphones were initially analog systems operating at 850 MHz. During 1990s second generation cellphones were implemented using GSM/EDGE and CDMA standards. This generation of cellphones had superior digital transmission of signals compared to analog transmission of first generation. The second generation of cellphones provided simple internet connectivity which was not available in first generation. As the demand for mobile data increased standards like WCDMA/HSPA+ were implemented in third generation cellphones. The carrier aggregation in 3G led to mobile broadband data speeds above 60 Mbps [5].

With fourth generation (4G) cellular technology high data rates are achieved. The LTE standard, part of 4G, has higher bandwidth option than 3G. WCDMA has peak bandwidth of 5 MHz whereas LTE can go up to 20 MHz LTE UL (Up Link) uses higher order modulation like 16 QAM (Quadrature Amplitude Modulation) and 64 QAM compared to QPSK (Quadrature Phase Shift Keying) / HPSK (Hybrid Phase Shift Keying) of WCDMA. With 2 x 20 MHz carrier aggregation, LTE data rates can go beyond 300 Mbps.

A representative handset transmitter is shown in Figure 1.1. The baseband IQ data is upsampled, converted to the analog domain using DACs, and fed to an IQ modulator. The modulator output is then upconverted to RF using mixers. Band pass filters are needed to reject the image at the mixer output. The power amplifier amplifies this signal and feeds the antenna. In the commercial cell phones available, most of the circuitry

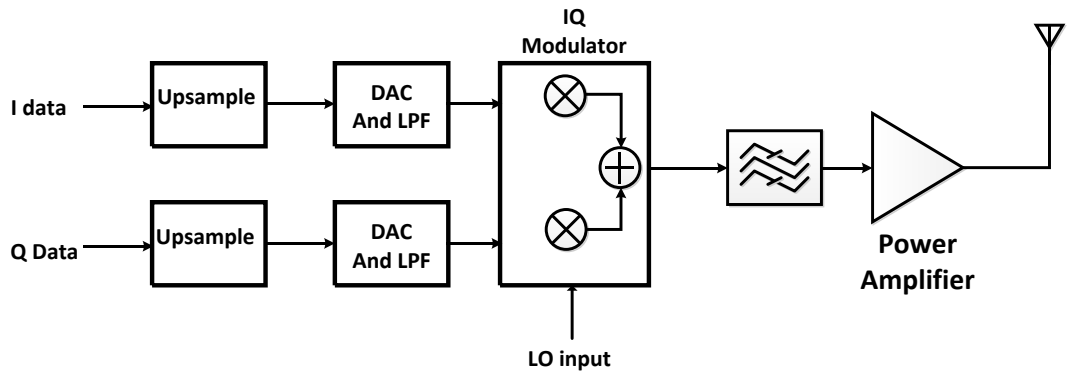


Figure 1.1. Block diagram of handset transmitter

except the PA is implemented in silicon CMOS technology. Silicon CMOS technology is generally ideal for digital circuits. Due to scaling, the $f_t$ of advanced CMOS technology is high enough (> 300 GHz) to design most of the RF and mm-wave circuits. The breakdown voltage for silicon technology goes down with technology scaling, however. The advanced node faster devices cannot handle large voltages or currents. The 180 nm CMOS SOI technology with $f_t$ of above 60 GHz handles a supply voltage of 1.5 V. Highly scaled 45 nm CMOS SOI technology with $f_t$ above 250 GHz handles a supply voltage of 1 V. Generating high output power from power amplifier becomes challenging with advanced CMOS technology. The CMOS FETs are generally non-linear compared to compound semiconductor (III-V) alternatives. The parasitics in silicon technology lead to lower efficiency in PAs. The passives on silicon substrate induce more losses than passives in III-V technology. The parasitics also manifest as non-linearities like AM-PM. This makes PA design difficult from efficiency and linearity stand point. Limited efficiency leads to lower battery life-time, which is crucial for handsets. Lower linearity leads limited data rates, as higher. But silicon has high yield, cost effective and enhances

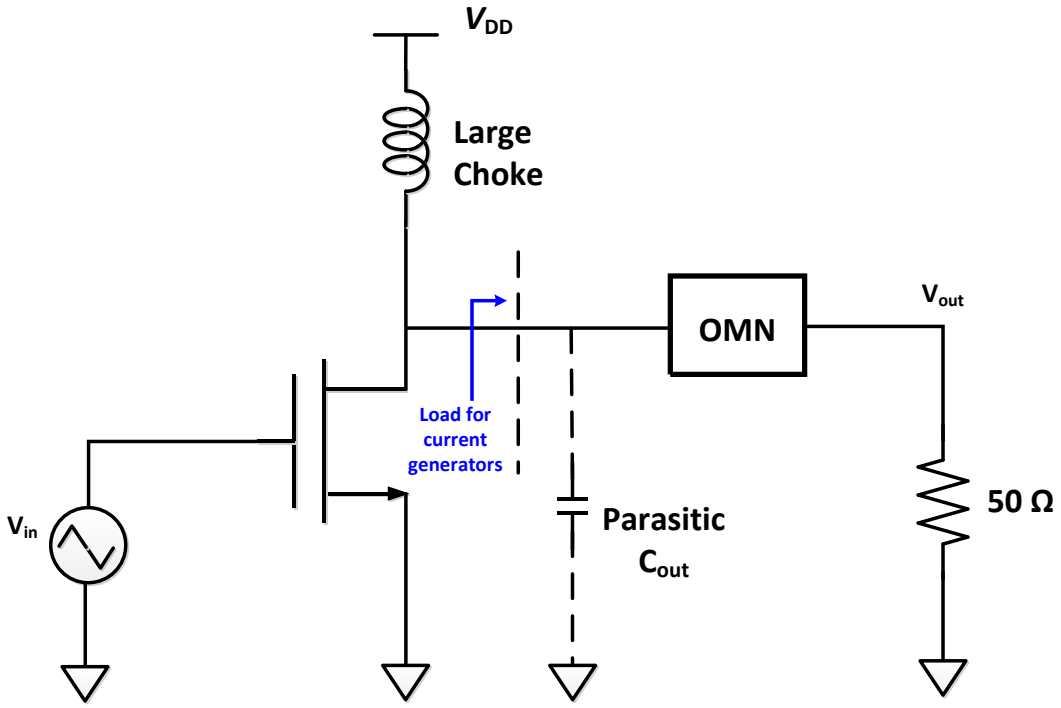


Figure 1.2. Schematic of basic power amplifier

integration. Typical PA modules (PAMs) used in handsets include peripheral circuits to control supply voltage (for implementing average power tracking), to generate bias voltages/currents, to perform band switching and various other functions. These are generally implemented in silicon CMOS technology. With CMOS PA, all the peripheral circuitry can be integrated on to a single substrate.

## 1.1 Power Amplifier Classes

Power Amplifiers can be used in various classes of operation [6]. The choice of class depends on various factors like efficiency, linearity, ease of implementation and others. Figure 1.2 shows a power amplifier with large inductor for drain biasing. The load seen by current generators and the conduction angle decide the PA behavior – output

power, gain, efficiency and linearity. In traditional biased PAs, class-A has 100% conduction angle, class-B has 50% and class-C has <50%. Class-AB has conduction angle between 100% and 50%. The linearity degrades with decreasing conduction angle mainly because of signal clipping. Efficiency improves with decreasing conduction angle because of reduced DC power dissipation in comparison to output power. The switching mode PAs like class-D, class-E and class-F give very good efficiency but do not offer good linearity. These classes are based on sharp rise and fall of current and voltage waveforms and reducing the overlap between them. This leads to good efficiency. The sharp waveforms lead to increased harmonics leading to degraded linearity.

Class-AB amplifiers exhibit behavior with good trade-off between linearity and efficiency. Ideally, the load seen by current generators of PA at the drain is real at fundamental frequency and short at all higher harmonics. The low impedance at higher harmonics is generally contributed by parasitic output capacitance of PA. In [6], author describes practical challenges involving PA output capacitance not being large enough to provide low impedances (relative to fundamental impedance) at harmonics. This is especially relevant when fundamental optimum resistance of high output power PA is low and significantly lower impedances are required at harmonics. In such cases, impedance matching networks can be designed to engineer voltage and current waveforms to achieve high efficiency operation by providing capacitive harmonic impedances. One such case is class-J PA and impedance levels needed for such operation are used in this work.

## 1.2 Power Amplifier Architectures for Back-off Efficiency Improvement

To enhance the spectral efficiency of wireless transmission, higher order QAM up to 64-QAM are currently being used in cellular communication. When such baseband signals are over sampled and filtered, the peak-to-average power ratio (PAPR) of resulting signals increase significantly. Also the use of OFDM increases the PAPR of transmitted signals. To efficiently transmit such signals, the PA needs to have good efficiency at peak output power as well as back-off. This can be achieved by load modulation – the load seen by PA is modulated with power back-off by varying certain parameter in the circuit. The most notable load modulation techniques for enhances back-off efficiency – Outphasing, Envelope tracking (ET) and Doherty—are briefly described.

### 1.2.1 Outphasing Power Amplifier

Idea of outphasing was introduced in 1935 [7]. Figure 1.3 shows block diagram for outphasing power amplifier [8]. This technique uses two saturated power amplifier whose output power is added through a combiner. The key idea is that the power at the

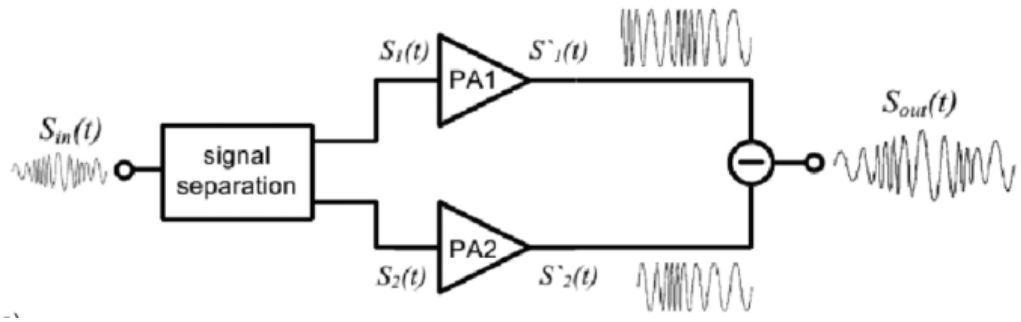


Figure 1.3. Block diagram of Outphasing power amplifier

output of ideal combiner can be varied by varying the phase difference between the outputs individual amplifiers (high efficiency switching mode amplifiers), without varying their output power amplitude. This keeps the PA operating at their peak output power in saturated state and hence at high efficiency. To achieve such behaviour at output, the signal at input is decomposed into separate drives of constant amplitude with appropriate phase difference to achieve needed output power.

Significant challenges in outphasing PA architecture arise in implementation of input signal component separator and output combiner. Input signal component separator, generally operated at baseband, imposes DSP overhead. Output combiner in practical implementation needs a balun, which is lossy at GHz frequencies. Obtaining output power for modulated signals with stringent linearity specifications is difficult as phases need to be added with good precision at output. In general outphasing amplifiers need memory correction in the predistortion to achieve good ACPR and EVM. This architecture has high efficiency at peak to certain back-off power, then leading to steep

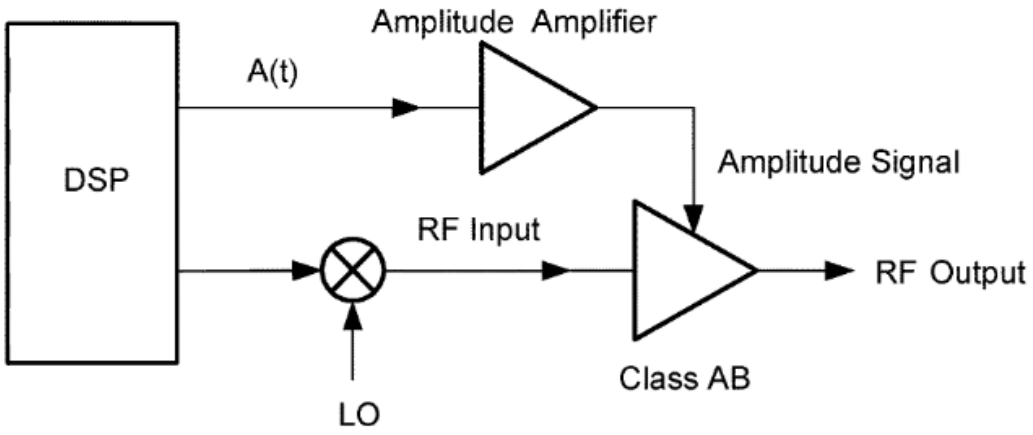


Figure 1.4. Block diagram of envelope tracking power amplifier

decrease in efficiency. There is also limitation in achievable dynamic range with acceptable efficiency.

### 1.2.2 Envelope Tracking (ET) Power Amplifier

Envelope tracking power amplifier (ETPA) system uses a RF power amplifier and supply modulator to vary its drain bias voltage. The drain bias of PA varies in accordance with input signal amplitude. Thus in back-off, the supply voltage is small. This reduces the DC power dissipated and enhances the efficiency. Another way to look at it is as follows: the drain bias is maintained at a level where transistor is saturation, where its efficiency is high, independent of input signal amplitude. Figure 1.4 shows the block diagram of an ET PA system [9].

The main challenge in operation of high efficiency ET PA system arises from supply modulator implementation. The total efficiency of the system is product of efficiencies of RF PA and supply modulator. The bandwidth of the envelope signal is higher than the bandwidth of IQ signal being transmitted. It is challenging to implement a highly efficient wideband supply modulator. The time-alignment between envelope signal and output RF signal of PA is crucial in linear reconstruction of signal at the output i.e. acceptable ACPR and EVM.

### 1.2.3 Doherty Power Amplifier

The Doherty power amplifier was introduced in 1936 [10]. This technique uses two power amplifiers – main and peaking – whose output is combined using an output combiner. Figure 1.5 shows a schematic diagram of the Doherty PA [11]. The output combiner uses a quarter-wave impedance inverter to bring about proper load modulation

for main power. At the input signal is split using a power divider. To combine output from main and peaking with proper phase at the junction of output combiner, a phase compensation network which mimics phase delay of impedance inverter is used. Main amplifier is biased in class AB and peaking amplifier is biased in class C. When input signal amplitude is small, the biasing arrangement ensures that main amplifier is active and peaking amplifier is not contributing any power to the output. As signal amplitude increases, the peaking amplifier starts pumping current to the load, resulting in lowering of impedance seen for main amplifier.

One of the important challenges in implementing Doherty PA comes from bandwidth limitation of impedance inverter. The traditional implementation is not area

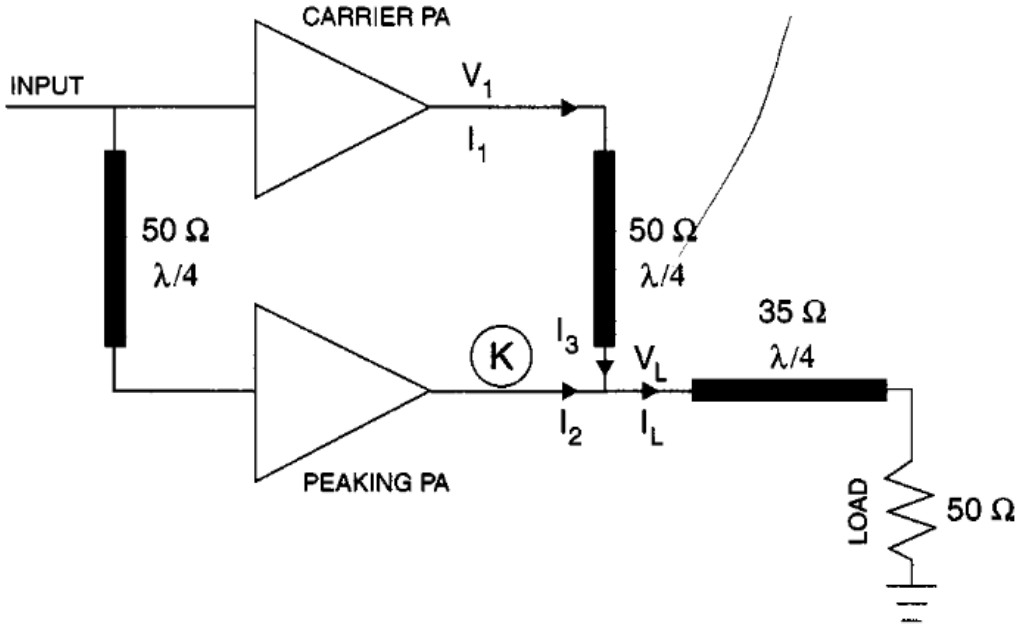


Figure 1.5. Schematic diagram of Dohety power amplifier

efficient – impedance inverter consumes large area at RF. To make Doherty PA viable for handset like applications lumped element implementation of output combiner and input networks are used.

## 1.3 Research Challenges and opportunities

Output power, efficiency, bandwidth and linearity are important parameters to evaluate PA performance. Apart from these, cost, form factor and ease of implementation also play influential roles in practical PA design. Choice of technology depends on cost, performance targets and various other factors. The most important challenge is to push the output power of PA to achieve the best possible efficiency for a given technology. The output power directly relates to distance of communication; more output power leads to increased distance of communication. Higher efficiency would lead to better power management – important especially for hand-held devices like handsets. Higher efficiency of PA also makes thermal management easier. A linear PA would be able to support complex modulation schemes – achieving high data rate communication. The research challenge is to explore, identify and demonstrate the design techniques which lead to highly linear, highly efficient and high output power PAs which would reduce cost, form factor and implementation overhead.

## 1.4 Scope of the Dissertation

The main focus of this dissertation is to explore design and implementation techniques of digitally intensive power amplifiers for wireless transmitters in silicon

CMOS technology. Two main issues addressed in this work are output power and efficiency, which are critical parameters of a wireless transmitter. The challenge is to demonstrate high efficiency operation for wireless transmission of high-order modulation signals having high PAPR, while maintaining the output power and linearity needs for handsets. The objective of this dissertation is to analyze the issues relating to digital power amplifiers and their extended designs from the standpoint of output power, efficiency and bandwidth. Based on the analysis and demonstrations, simple solutions are provided here to enhance the power amplifier performance.

As an extension of this work, the developed CMOS digital power amplifier is used as a driver to implement a CMOS-GaN power amplifier for femto-cell basestation applications. The challenge in this implementation is to achieve high power and large bandwidth, while maintaining good linearity. The frequency response of this power amplifier is analyzed and new approaches are suggested to enhance PA bandwidth.

## 1.5 Organization of the Dissertation

Chapter 2 describes the design of a digitally controlled power amplifier (DPA) in 180 nm CMOS SOI technology. The DPA is implemented in polar architecture with 10-bit digital AM and constant amplitude PM at RF. 10-bit AM controls active unit cells and use of stacked-FET PA for unit cells leads to large output power. An off-chip class-J like match is employed at output to achieve good efficiency. The design, layout and experimental results of CMOS DPA are discussed.

Chapter 3 describes a digitally controlled Doherty power amplifier implemented using two of the DPAs and off-chip combiner. The challenges in Doherty power

amplifier implementation are discussed and new approaches are proposed to enhance back-off efficiency behaviour. The advantage of using DPAs with sharp turn-ON characteristics to achieve sharp efficiency is described. The design of a Doherty combiner and the associated load modulation with back-off is discussed in detail. Various load modulation profiles are described and ease of implementing optimal modulation profile with digital control is brought about. Finally the implementation details and measurement results are described.

Chapter 4 describes a novel digitally controlled power amplifier implemented using a CMOS and GaN combination. The CMOS DPA is used to drive a 0.75 μm technology GaN FET to achieve high output power. The GaN FET is set in common gate configuration presenting suitable wideband output impedance for DPA. This design aims at making wideband PA by eliminating all impedance matching networks. The trade-off between bandwidth, efficiency and output power harmonic content is discussed in detail. A small-signal model is built for PA to analyse the factors limiting the bandwidth of CMOS-GaN PA. The role played by circuit parasitics in limiting the PA bandwidth is investigated. Based on such analysis, new approaches are suggested to enhance the PA bandwidth.

Chapter 5 concludes the thesis with summary of research and suggestions for future work.

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# Chapter 2

# Watt-class, High-Efficiency, Digitally-Modulated Polar Power Amplifier Implemented in CMOS SOI Technology

## 2.1 Introduction

Current cell phone handsets use many communication standards, which are part of the evolution of wireless communication technology. 2G communication was focused on voice only. The newer generation standards like WCDMA and LTE focus on high-speed wireless data transfer. The communication frequency and the power level change with the standard in use.

Digitally-controlled power amplifiers have been proposed [1-3] to provide a simple architecture for multimode and potentially multiband transmitters. In principle, they can be programmed for different modes of operation, and through the use of switching-mode output stages, they can achieve high efficiency. CMOS technology is a

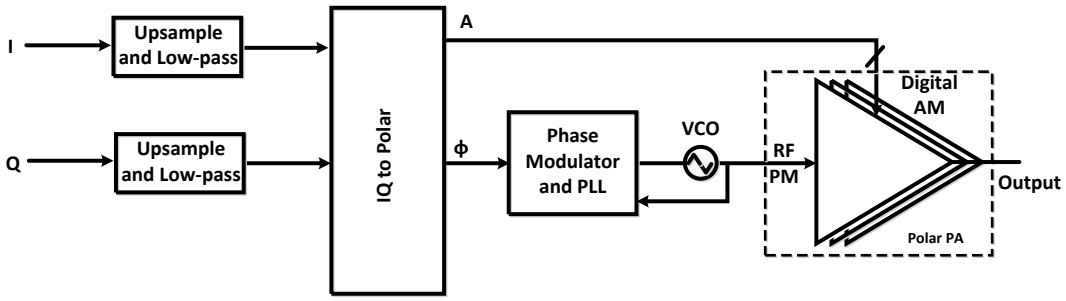


Figure 2.1. Schematic Digital Polar Transmitter

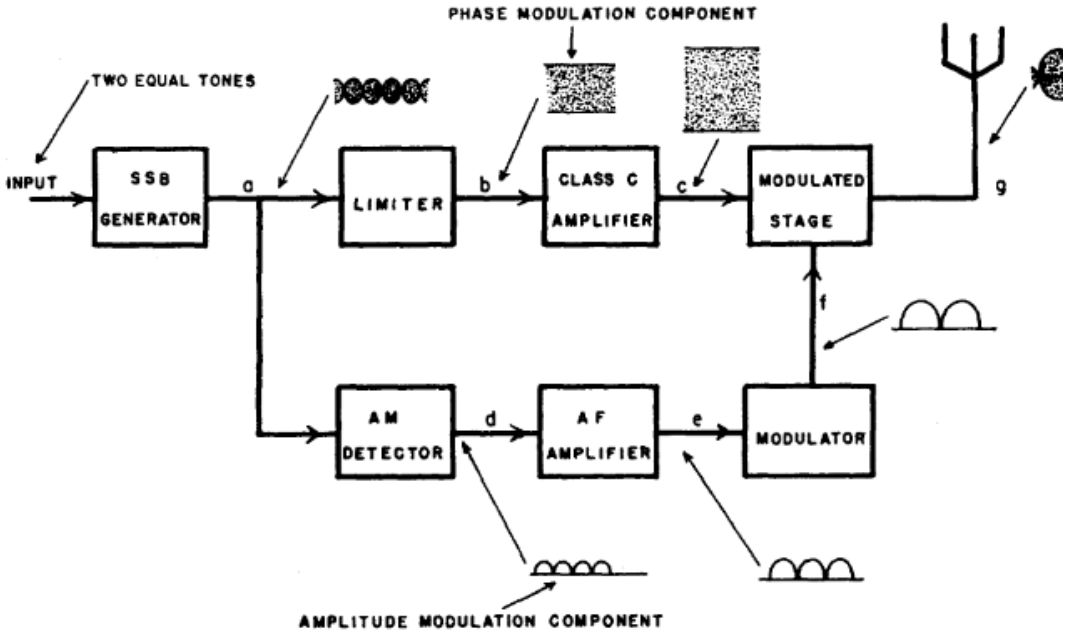


Figure 2.2. Schematic of original Kahn Transmitter

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preferred approach for integration of digital circuits and switching-mode devices with high frequency response.

The Digitally-controlled Power Amplifier (DPA) architecture was used as a part of Bluetooth transmitter in [1]. A 10-bit DPA was used to demonstrate the ability to transmit GSM signals in [2]. In [3] the 10-bit CMOS DPA was used to transmit 5 MHz WCDMA and WiMAX OFDM. The peak output power was 25.2 dBm with peak efficiency close to 47% at 1.85 GHz. In [4] peak power of 24.4 dBm was obtained at 43% efficiency at 800 MHz. The 10-bit DPA was used to transmit 5 MHz WCDMA. In [5], the DPA gives 30 dBm output power with 40.6% efficiency (including power consumed by buck converter). This PA was able to transmit 5 MHz WCDMA signal. The digital polar architecture has also been shown to work for WLAN application [6-7].

To date, CMOS Digital Power Amplifiers (digital PAs) have not generated high enough power levels for many applications, for example, cell phone transmitters. In this work, we demonstrate a CMOS digital PA with output power of 1.45 W, appropriate for WCDMA applications. A stacked FET configuration is used to increase the voltage handling capability of the CMOS output stage. The measured efficiency of the digital PA is high; drain efficiency of 65.9% is achieved at peak power; the corresponding peak system efficiency (which includes power dissipation in the digital logic and driver stages) is 60%. The digital PA output amplitude and phase are nonlinear functions of the input digital Amplitude Control Word (ACW) as expected for a high efficiency design. Input signals for modulated outputs are generated using Digital Predistortion (DPD). Results are shown here for WCDMA (PAPR=3.4dB) and LTE (PAPR=6.7dB) signals; drain efficiencies of 49.5% and 35.7% are achieved, respectively. The results are also shown

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for the following frequencies: 1.5 GHz, 1.6 GHz, 1.9 GHz and 2.5 GHz. Different output matching networks are used for different frequencies (so multiband operation can be with a tuneable output matching network, with no changes required at input and interstage. The CMOS DPA described here is also used as a building block for a high power, high efficiency digital Doherty amplifier for handset application and as a driver for GaN FET constituting a wideband CMOS-GaN power amplifier showing promise for micro-basestation application, as described in subsequent chapters.

## 2.2 Digital Power Amplifier (DPA) Architecture

In a polar architecture the IQ data is split into amplitude and phase. In the DPA designed in this work, the amplitude information corresponds to the fraction of active unit cells in the overall DPA. At maximum amplitude the full DPA is active and at back-off only a part of the DPA is active. The IQ to polar conversion is given by

$$A = \sqrt{(I^2 + Q^2)} \qquad \text{.....(1)}$$

$$\varphi = tan^{-1}\left(\frac{Q}{I}\right) \qquad \text{.....(2)}$$

A simple polar transmitter is shown in Figure 2.1. The IQ data is upsampled and low-pass filtered. The cordic converter transforms this data into amplitude and phase. The amplitude modulated signal (AM) is a baseband signal. The phase modulated (PM) signal has constant envelope and is centered at RF. This architecture is an evolved version of the transmitter discussed in Kahn's work, Figure 2.2 [8]. The Am and PM signal is reconstructed at the output by the power amplifier (PA). The AM signal can be provided to the output as supply voltage modulation of the PA. Such a PA is an analog polar PA

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[9]. This needs a supply modulator, which is not easy to implement in deep sub-micron technology. The newer silicon CMOS technology is optimized for digital circuitry and makes the design of RF circuits more complicated. This has encouraged the migration of Polar architecture towards digitally intensive implementations [1].

The digital PA developed in this thesis is implemented using a digital polar architecture, where amplitude modulation is realized with 10-bit input ACWs which govern the active fraction of the output cells. A constant amplitude RF input signal centered at the carrier frequency provides the phase modulation. The digital PA is composed of 31 unary and 5 binary weighted cells. The most significant 5 bits of the ACW input are processed by a binary-to-thermometer decoder (BTD) to activate suitable number of 31 unary cells. Each of the least significant 5 bits of the ACW drives a correspondingly weighted binary cell. All the cells are connected in parallel. When active, their currents get combined at the output. When inactive, the cells act as open with parasitic capacitance in parallel.

There at two extreme implementations of RFDAC design when cell distribution is considered. If all the cells are unary cell (equally sized), then we would need 1023 cells to create 1024 states (OFF being a state). This design would ensure monotonicity and minimize DNL error and dynamic switching error [17]. Such a design would need complex decoding logic which consumes significant area and power. From IC layout perspective, maintaining same phase for all ‘enable’ inputs of each cell would become challenging. On the other hand, if all the cells are binary weighted, and then we would need only 10 cells. The concern in this case is that the weighting is not precise due to cell

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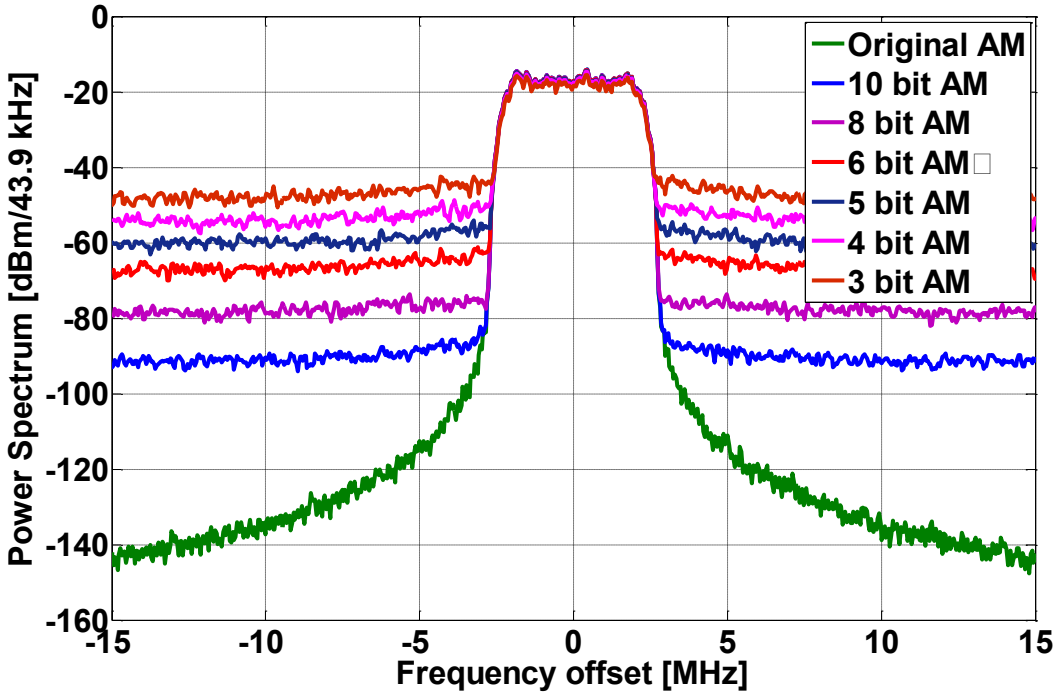


Figure 2.3. Spectrum of a LTE signal for various bit resolution in AM

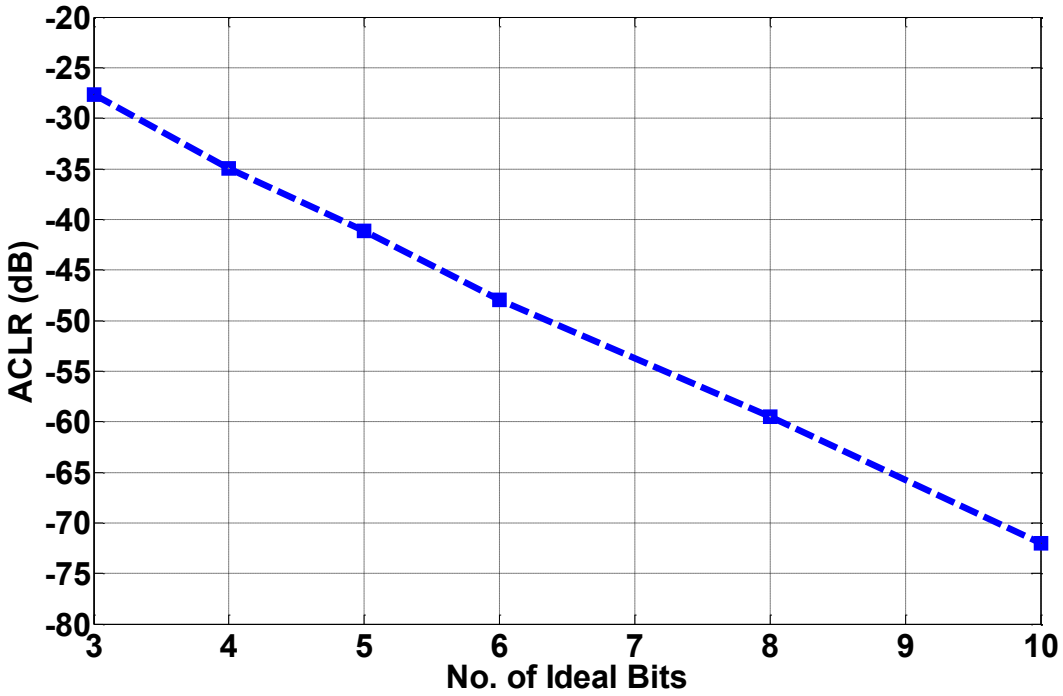


Figure 2.4. E-UTRA ACLR of LTE signal vs no. of bits of AM

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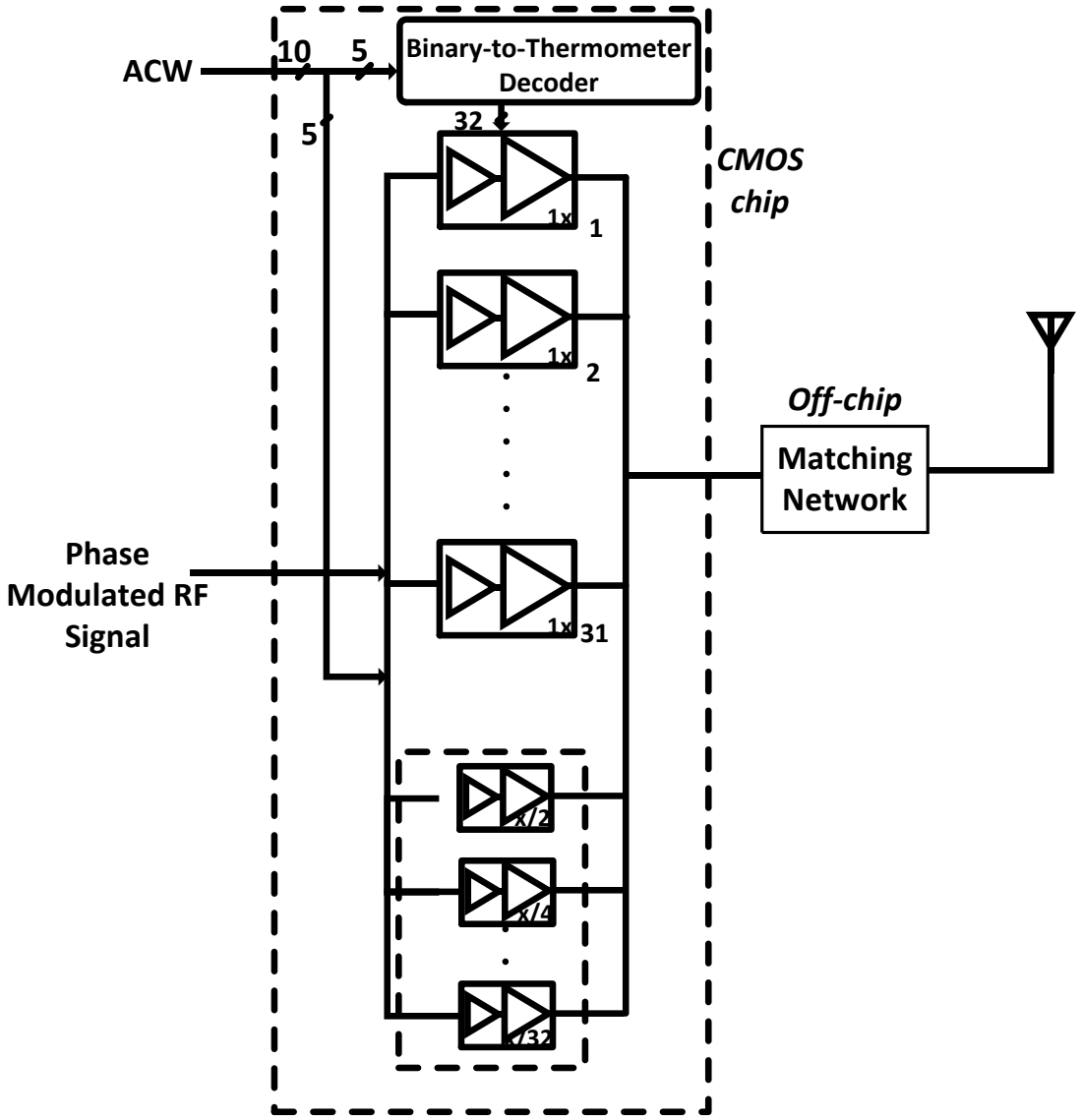


Figure 2.5. Architecture of Digitally controlled power amplifier (DPA)

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mismatches. This would lead to inaccurate states, resulting in loss of modulation accuracy.

For an idealized transmitter, 5 bits are enough to meet WCDMA ACPR and emission mask specs as shown in [3]. This is also enough to meet E-UTRA ACLR specification for LTE signal, considering the oversampling ratio for data is 10. This has to be better than -30 dB. 10-bit resolution for AM is used here to compensate for the AM-AM non-linearity of the digital PA and to provide power control (which can also be implemented with power supply voltage control). To study the effect of AM resolution a simple MATLAB code is used. Figure 2.3 shows the output spectra of polar transmitter for a 5 MHz LTE single-carrier signal as number of AM bits are changed. The finite amplitude resolution results in quantization noise; this elevates the noise floor of

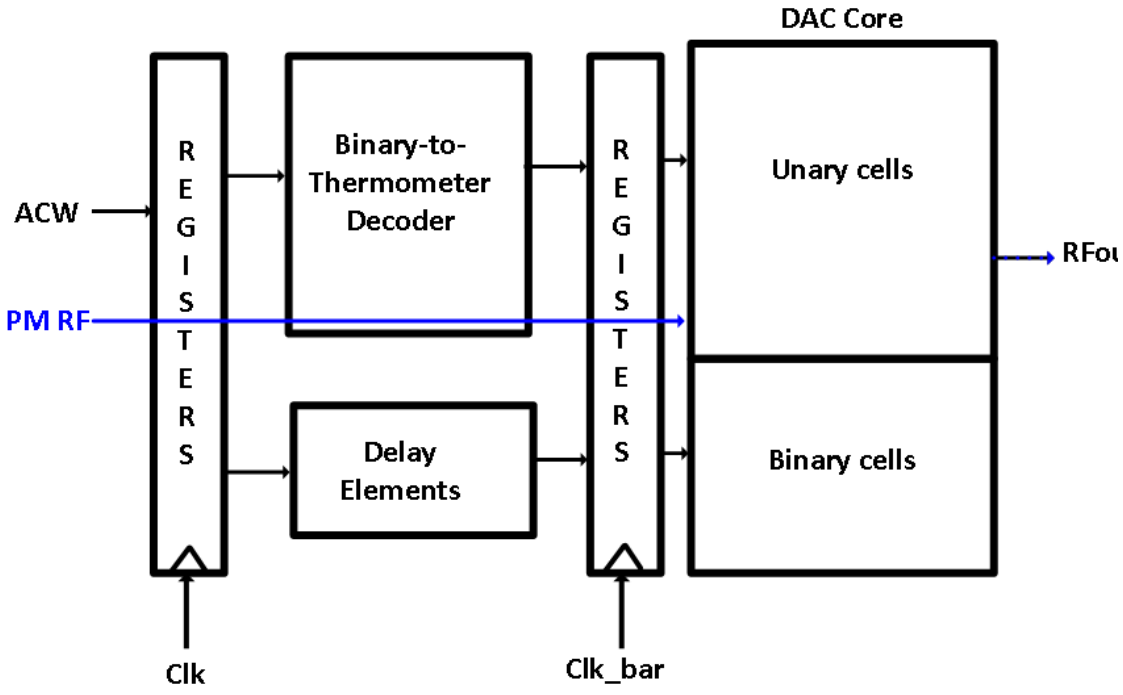


Figure 2.6. Block diagram of CMOS DPA chip

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transmitted signal. For close-in spectra, this results in inferior ACPR. Figure 2.4 shows improvement in ACLR as number of bits in transmitter is increased.

Figure 2.5 shows the block diagram of the implemented digitally controlled amplifier (DPA). The AM signal comes from binary to thermometer decoder (BTD) for unary cells and through delay blocks for binary cells. Figure 2.6 shows the block diagram of full-chip.

AM-PM time alignment is one of the critical issues in polar transmitters. Raab [10] discusses how the intermodulation distortion in two-tone test arises when there is delay between envelope (AM signal in our case) and carrier. To maintain carrier to intermodulation ratio better than 30 dB, the delay has to be less than (0.1/BW); BW being signal bandwidth. For small time mis-alignments, third order inter-modulation distortion (IMD3) for 2-tone signals varies as [19]:

$$IMD3 \approx \left(\frac{2}{\pi}\right)(B_{RF}\tau)^2$$

where BRF is bandwidth of two-tone signal and τ is time mis-alignment.

The time-misalignment between AM and PM signals results in inferior ACPR and EVM. In [3], effect of time misalignment on ACPR is studied in detail and shown for a 5 MHz WCDMA signal sampled at 200 MHz. To meet the ACLR specs of WCDMA, authors suggest time mis-alignment lower than 2.6 ns. This corresponds to around half a sample mis-alignment. For a 5 MHz LTE signal discussed before, the ACLR degradation with time mis-alignment can be studied. Figure 2.7 show the ACLR degradation as time mis-alignment between AM and PM path grows.

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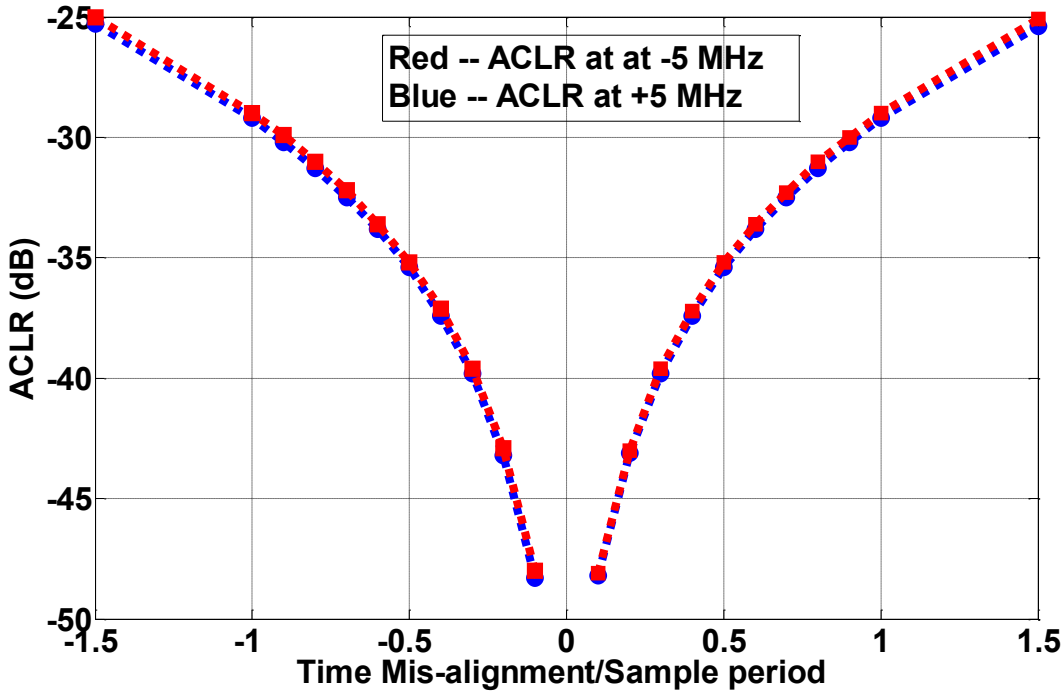


Figure 2.7. ACLR versus time mis-alignment between AM and PM paths

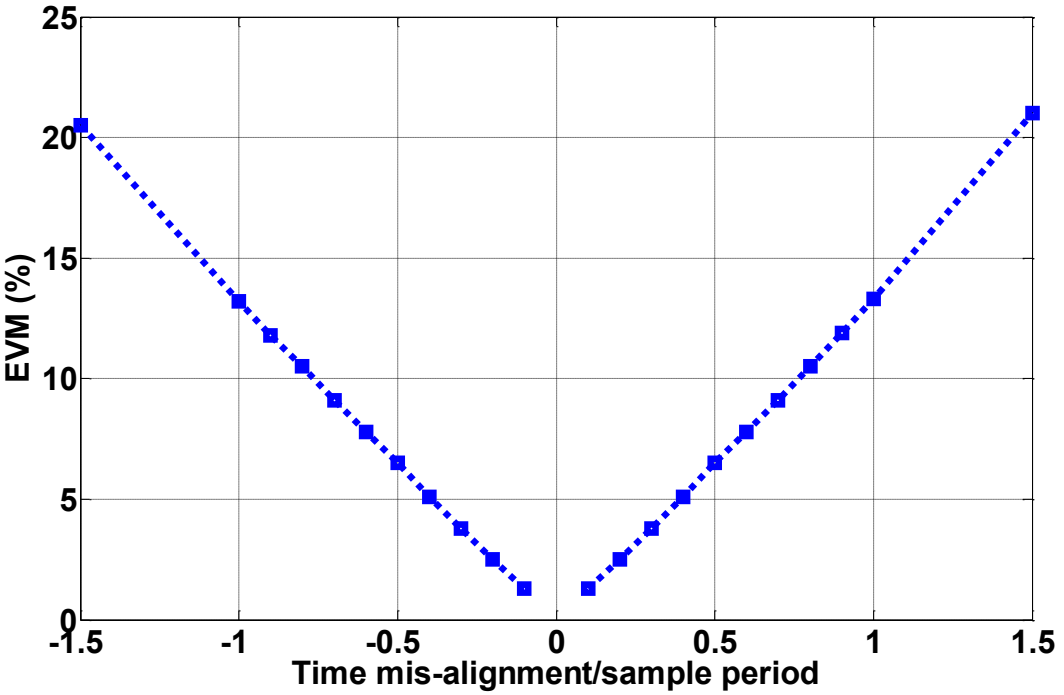


Figure 2.8. EVM in percentage versus time misalignment

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Time mis-alignment manifests as non-linearity for a transmitter. The IMD3 and ACLR study has been published [1,10]. The other parameter of importance is EVM; time mis-alignment between AM and PM paths in polar transmitter also affects EVM. Figure 2.8 shows the EVM degradation with AM PM time misalignment. In the presence of time-misalignment, phase data is off-set in time with respect to amplitude data. On IQ-plane, transmitter output, instead of reaching the ideal data reaches right amplitude but with different phase. This results in finite error vector, whose magnitude generally worsens with time-misalignment. In addition to this the DPA also shows clock images. These clock images are the characteristics of any sampled data systems like DPA. The DPA samples the data and has a zero-order hold filtering.

Because of non-linear operation of (1) and (2), the amplitude and phase signals

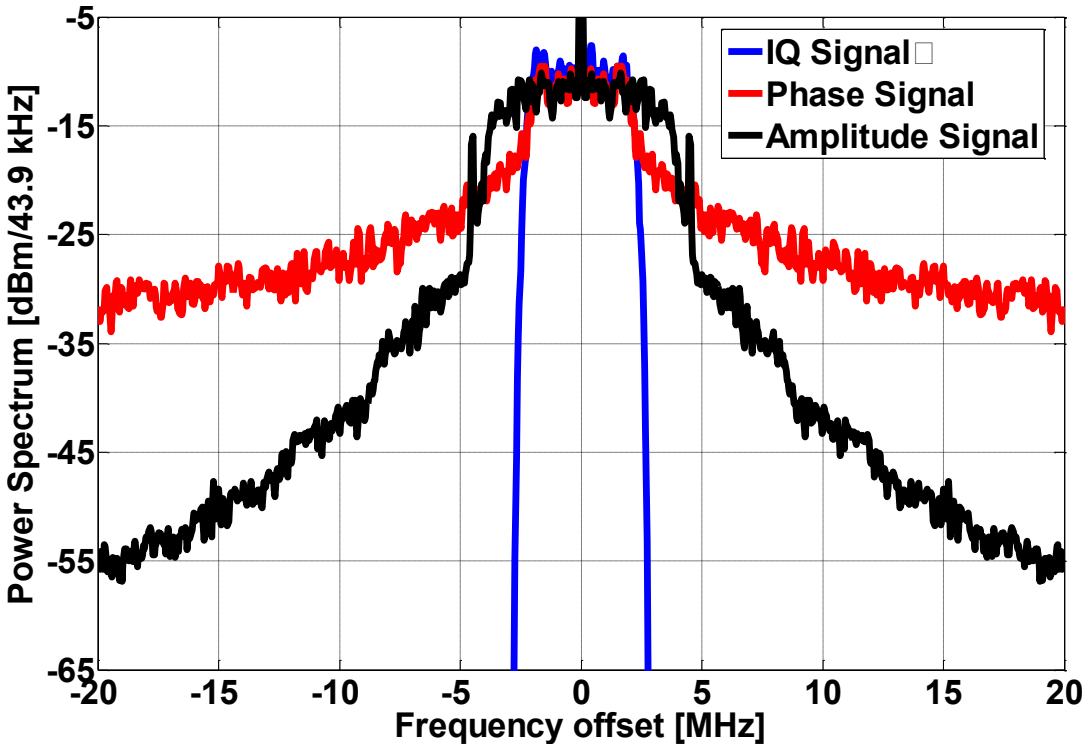


Figure 2.9. Amplitude and Phase signal bandwidth expansion in polat transmitters

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have much more bandwidth than the IQ signal. This is shown in Figure 2.9 for 5 MHz LTE single carrier signal. Looking at the close-in spectrum, the amplitude signal has larger bandwidth than phase signal. In far-out spectrum, the power of phase signal is higher than that of amplitude signal. To keep intact all the IQ information, a large bandwidth for phase signal has to be included. This would require wideband phase modulator to maintain good modulation accuracy, reduced spectral regrowth and improved broadband noise behaviour. A technique of using finite bandwidth amplitude and phase signals to improve broadband noise behaviour is discussed in [15].

The DPA has finite resolution in AM signal owing to quantization. This leads to quantization error, which shows up as noise spread over wide frequency range. This is of particular concern for handset application with FDD (frequency division duplex) operation; as this noise would fall on receive the band (RX band). The required noise level at receive band is -180 dB/Hz. The duplexers currently available have TX-RX isolation of the order of 50 dB – 60 dB. This required the RX band noise at the output of PA be lower than -120 dBm/Hz. This is difficult to achieve for DPA because of the quantization noise. However the noise can be reduced by filtering the inputs appropriately. This has been described in [11] where the input AM and PM signals are filtered to reduce out-of-band spectral images and quantization noise. In [7] a FIR filter is implemented on CMOS IC which achieves quantization noise suppression.

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# 2.3 DPA – Circuit Design

## 2.3.1 Technology

For circuit implementation, IBM 7RFSOI (180 nm CMOS SOI) technology is used. The substrate has high resistivity of 1000 Ω-cm. The technology offers thin-oxide SOI devices (NFET and PFET) with floating body and contacted body. The supply voltage for these devices is 1.5 V. The thick-oxide 2.5 V NFET and PFET devices in both floating body and contacted body flavours are also available. Diffusion and metal resistors are also available. The high density MIM capacitors with density of 2 fF/μm$^2$ are available. There are 4 metal layers; lower most M1 is copper and upper ones – M2, MT and AM – are aluminium. The thicknesses of metal layers are respectively 330 nm, 480 nm, 480 nm and 4 μm.

Thin oxide devices are used in implementing DPA as they present less parasitics compared to thick oxide devices. Thin oxide devices exhibit higher transconductance compared to thick oxide devices. The $f_t$ of body-contacted devices is 52 GHz and that of floating body devices is 76 GHz (These $f_t$ numbers are for an RC extracted model of 160 μm wide nominal device).

## 2.3.2 Logic Circuits

As shown in Figure 2.6, there are logic circuits used in implementing digital power amplifier system. As the digital bits come on to the chip, they are latched using registers. This helps to isolate the off-chip signal transients and maintain signal integrity on chip. A NAND gate based D flip flop is used to implement this circuit. The binary to thermometer decoder is a row column matrix decoder [2, 11]. The input bits are first split

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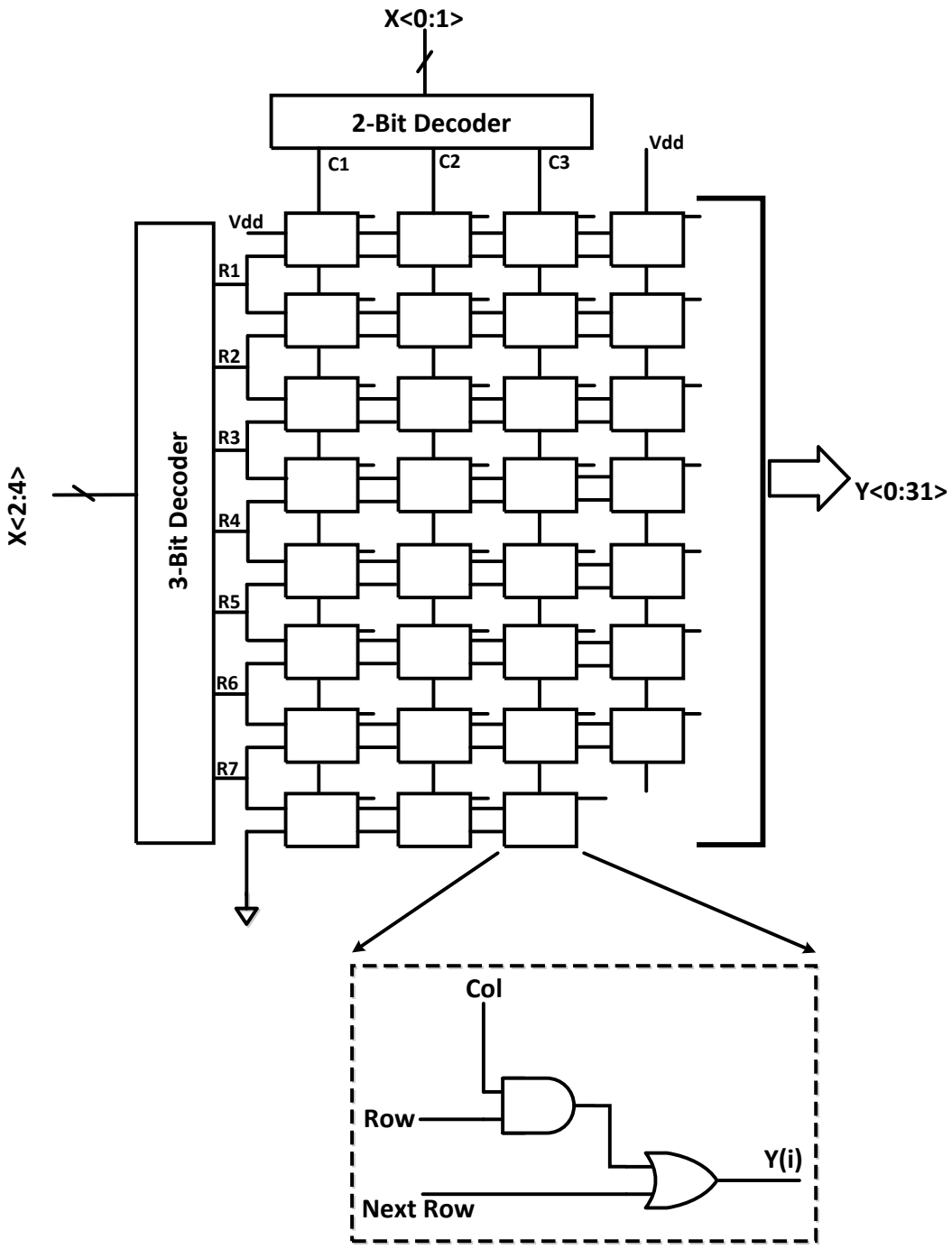


Figure 2.10. Block diagram of 5-to-32 Binary to Thermometer Decoder

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into two parts; 2-bits for column and 3-bits for row. These bits are decoded first using 2-to-3 decoder and 3-to-7 decoder respectively. The obtained 3 column bits and 7 row bits are used to activate appropriate number of thermometer bits at the output. Figure 2.10 describes the block diagram of full decoder with involved logic circuits. Thermometer coding helps reduce mismatch in DAC states. This also helps maintain monotonicity and avoid glitches. The delay elements are a cascade of inverters which mimic the delay of binary-to-thermometer decoder. The BTD and delay elements are followed by second set of registers, which helps isolate DAC core input from transients at output of binary to thermometer decoder. To implement all the logic circuits body contacted SOI FETs are used.

### 2.3.3 Driver Stages

Figure 2.11 shows the driver stages for final stack FET unit amplifier. To drive a final 160 um wide NFET, enable logic followed by 5-stages of inverters/class-D drivers are needed. Enable logic shown in Figure 2.11 takes phase modulated RF and enable (En) signals as input. The enable input is coming from binary to thermometer decoder followed by registers. The 50 Ω at the input of drivers helps get wideband resistive input impedance. This also helps to achieve good power transfer from measuring instruments. In an actual transmitter, the PLL drives the input of shown drivers – so no 50 Ω termination is needed. The supply voltage used is 1.7 V. Input DC is biased close to 1 V.

### 2.3.4 Stacked FET Power Amplifier

The stack FET power amplifiers in each unary cell use 4 NFETs. Figure 2.12 shows the stack FET unit power amplifier. The design of stacked FET PA is discussed in

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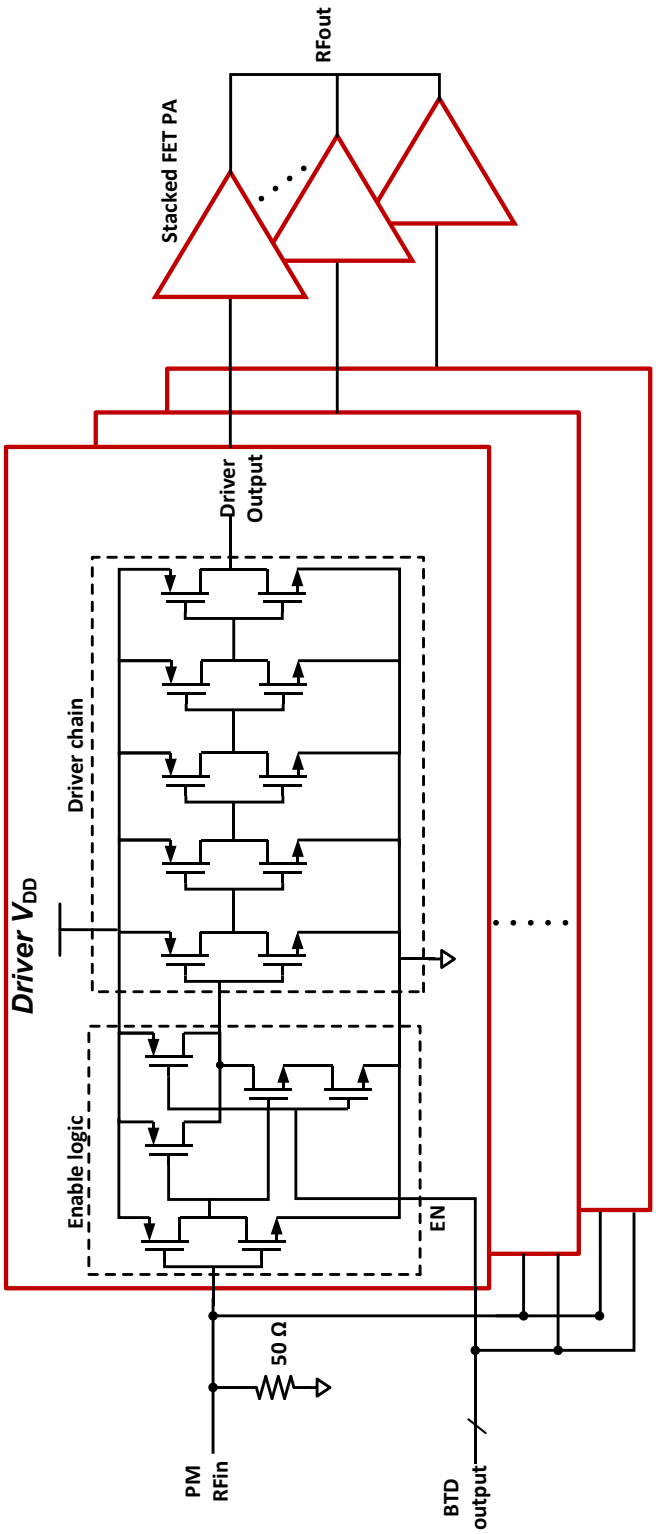


Figure 2.11. Schematic of driver stages of unit cell PA

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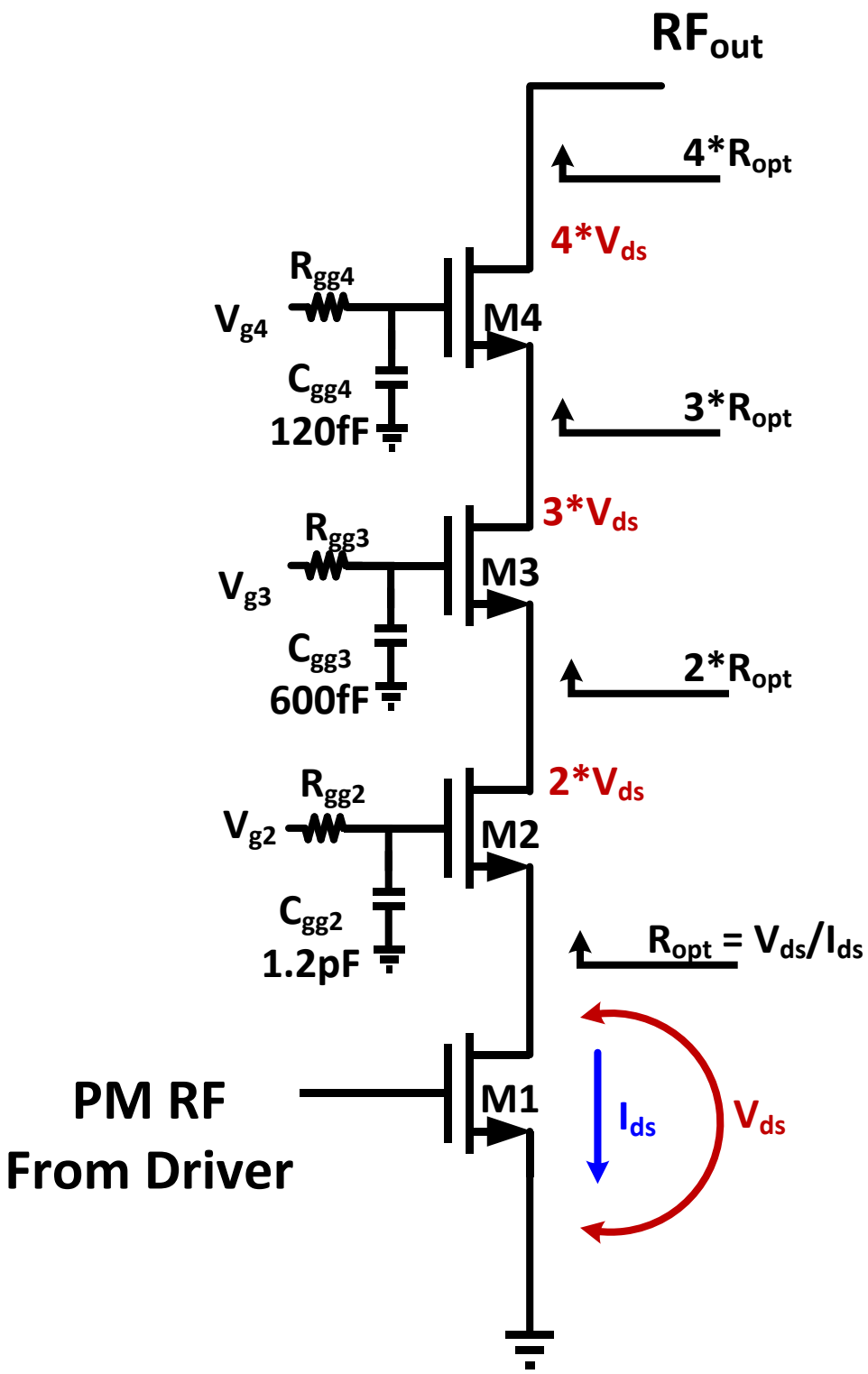


Figure 2.12. Schematic of unit stacked-FET PA

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[11-12]. In the 4-stack amplifier shown, the lower most transistor is driven by phase modulated RF signal. This common source stage M1 drives the source of next transistor M2. The transistor M2 is not in common-gate configuration. The finite capacitor Cgg2 at the gate of M2 does not provide RF ground. Thus the voltage swing at drain of M1 is split between parasitic $C_{gs}$ of M2 and $C_{gg2}$. This leads to voltage swing at gate of M2 helping create a reduced voltage swing between gate and drain of M2.

The impedance seen from drain of M1 should be set to $R_{opt}$ with the condition that size of M2 should be same as that of M1. The sizing has to be same as the current carried by both transistors is same. If M2 were common gate, then impedance looking into the source would be $(1/g_m)$. But in stacked FET finite $C_{gg2}$ plays a role in matching and helps bring the load impedance of M1 to $R_{opt}$. As we move up the stack, the load impedance required for transistor increases. This would require lower $C_{gg}$s for upper transistors.

A stack FET of four can handle four times the nominal voltage of a transistor. This would give four times more power than for a single transistor as used in stack, considering same current in both cases. FET stacking can be viewed as method of power combining. As the transistors are placed close to each other in stacking, this is very area efficient. This is very critical at higher frequencies as any on-chip routing would result in power loss [13-14].

Stacking of small transistors is beneficial compared to using a single large transistor to get higher power. Theoretically a large transistor can be designed to give same output power as the 4-stacked amplifier shown in Figure 2.12. But the optimum impedance needed for that large transistor would be much lower than is needed at drain of M4. The impedance matching needed in this case would be lossy, area-consuming and

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narrow bandwidth. Stacking helps increase the composite optimum resistance. This is very beneficial as the impedance matching to 50 Ω becomes much easier. In stacked-FET, for a given output power, the drive power needed is much smaller compared to single transistor.

## 2.3.5 Impedance Matching

The CMOS DPA has 31 unit cells and 5 binary weighted cells. Each unit cell has a final stage of 4-stacked -FET power amplifier. Each of the FET is 160 μm wide. This PA has to be matched to 50 Ω load to get best output power and efficiency. In the design stage the $R_{opt}$ of DPA is 8 Ω. The output capacitance of DPA is close to 7 pF. With such an output capacitance, it is more convenient to build a class-J like load for current generators of PA, than building a class-B like load.

An ideal class-B load is defined as $Z_{f_o} = R_{opt}$ at fundamental and shorts at all higher harmonics. Considering the frequency of operation to be 1 GHz and Ropt to be 8 Ω, the impedance provided by output capacitance at 2nd harmonics is 11.4 Ω. Using an inductor to resonate out the shunt capacitor at fundamental would further worsen the problem. Instead of resonating out the parasitic capacitance, it can be used to perform harmonic engineering and get better efficiency.

Ideally class-J load is defined as [16]:

$$Z_{f0} = R_{opt} + j * R_{opt}$$

$$Z_{2f0} = -j * \frac{3\pi}{8} * R_{opt}$$

$$Z_{nf0} = 0 \quad \ldots . . for\ n \geq 3$$

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The transient voltage peak for class-J load is higher than that for class-B load. This can be attributed to reactive part of fundamental load impedance. In order to limit the instantaneous voltage peaks across the stack, the load implemented here is not the ideal class-J load. The load instead is class-J like, considering that for full DPA $R_{opt}$ is close to 8 Ω. Figure 2.13 shows the harmonic load on smith chart for operating frequency of 900 MHz. The output network in composed of DPA output capacitance, wirebond inductance and two SMD components on the board.

With this load the gate and proper gate biasing, the voltage across each transistor

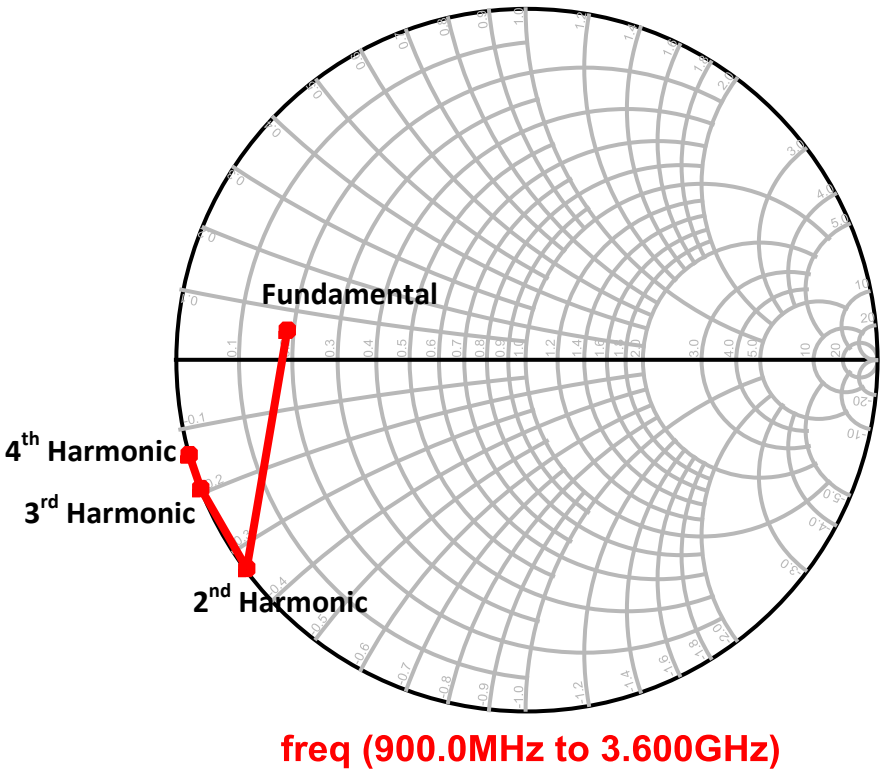


Figure 2.13. Harmonic load designed for Stacked FET PA

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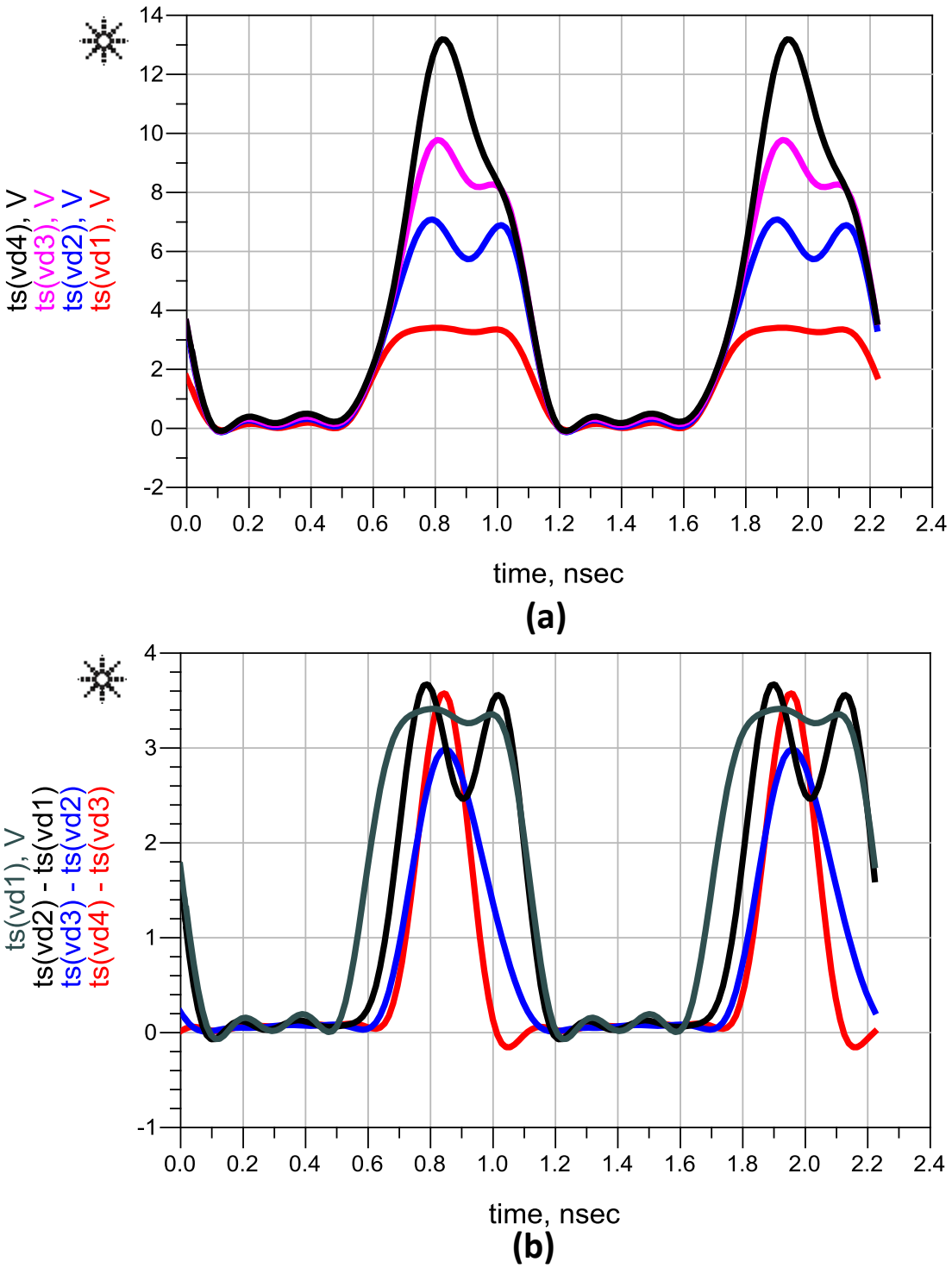


Figure 2.14. Time-domain waveforms for stacked FET PA (a) Drain Voltages (b) Drain to Source voltages

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of stack is made equal. Figure 2.14 (a) shows voltages at drains of each tansistor with supply voltage of 4.5 V when full DPA is operating. Figure 2.14 (b) shows the voltage distribution across different transistors. Looking out of the drain of top transistor, the load is aclass-J-like. Looking out of drain of 3rd transistor, however, the impedances not the same. So is also the case with 2nd and bottom transistor. This can be deduced by looking at the harmonic content of voltages and currents. The currents and voltages for top transistors have more 2nd harmonic content than 3rd. The currents and voltages of bottom transistors have more 3rd harmonic current – leading to flat top waveforms. This is seen in Figure 2.15 which shows drain current waveforms for transistors in stacked FET PA. The current from drain of lower transistors show higher 3rd harmonic content than 2nd harmonic, leading to sharp rising edge. This current behaviour is lost as we move up the

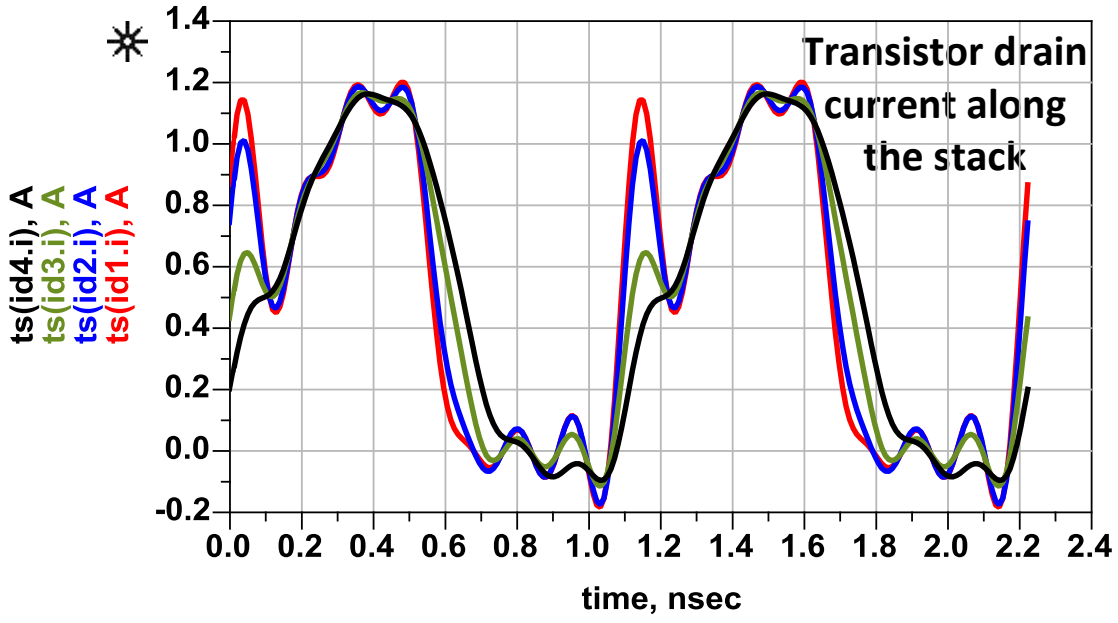


Figure 2.15. Drain current waveforms for four transistors of stacked FET PA

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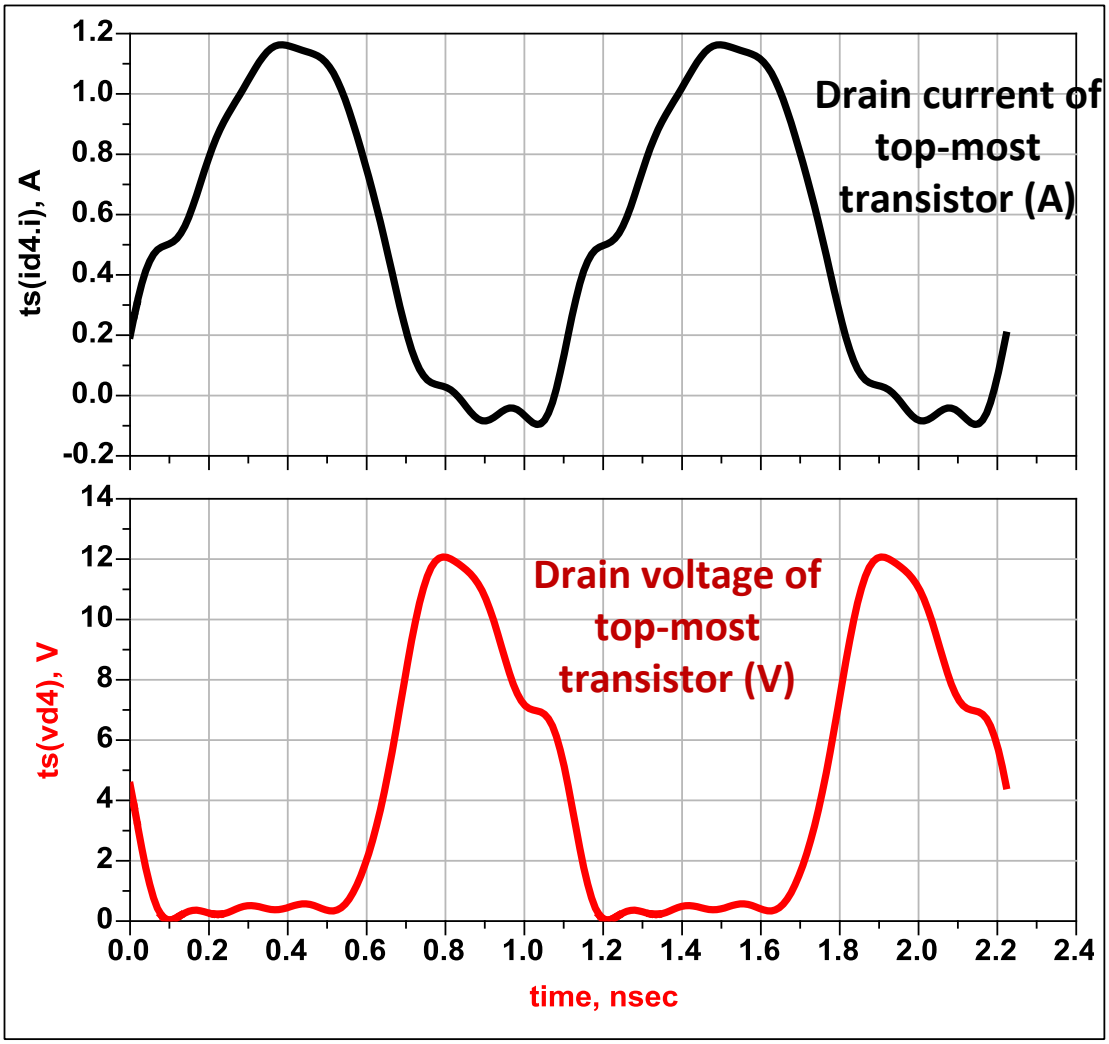


Figure 2.16. Drain voltage and current waveform of top transistor in 4-stack PA

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stack. Figure 2.16 shows the drain current and voltage of top transistor of stack at peak ACW. During the half-cycle when stack is ON, the current is high and voltage across stack is low. This indicates low impedance at the drain and behaviour like voltage source.

### 2.3.6 Layout

Stacked FET uses four 160 µm wide transistors. Each transistor is implemented with unit finger of 5 µm and has 32 fingers. The top layer is thickest and used to make traces carrying RF current. The gate capacitors are divided into two and placed at two

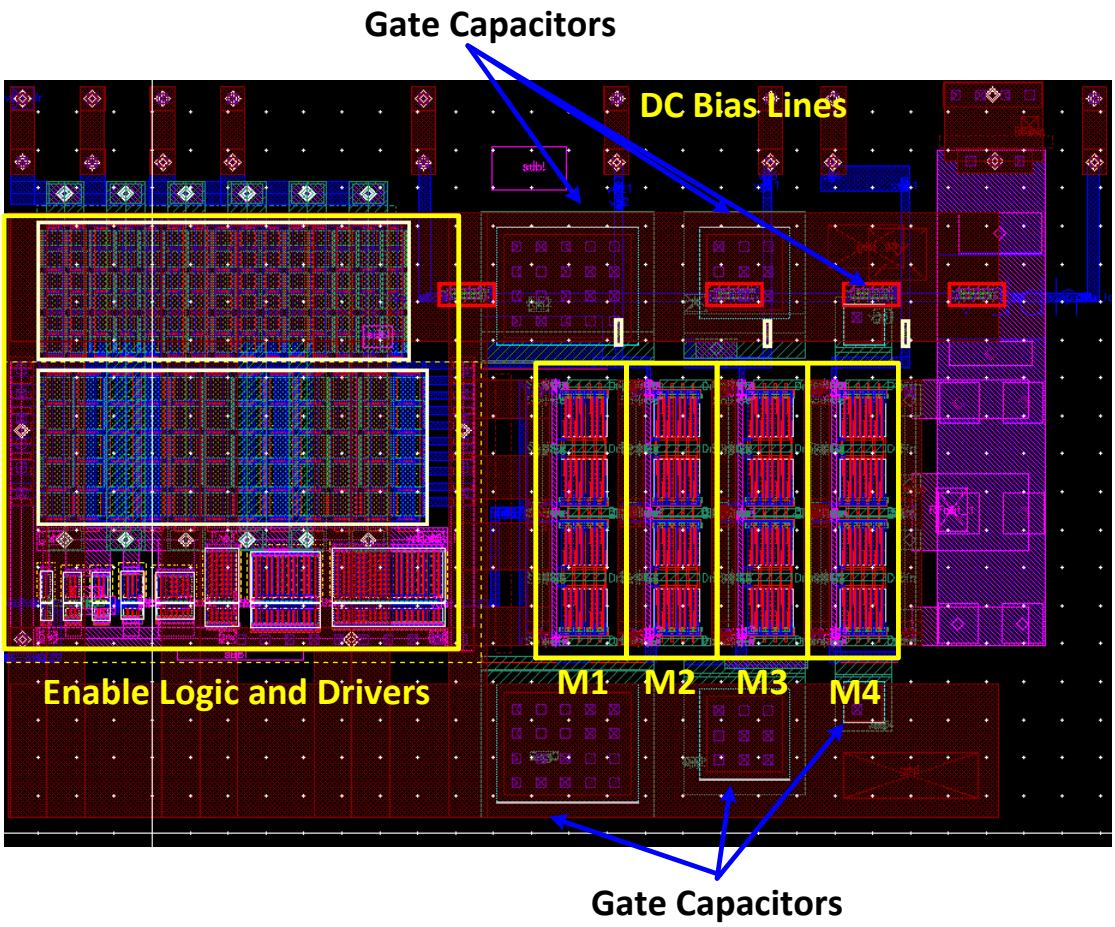


Figure 2.17. Layout of unit cell PA

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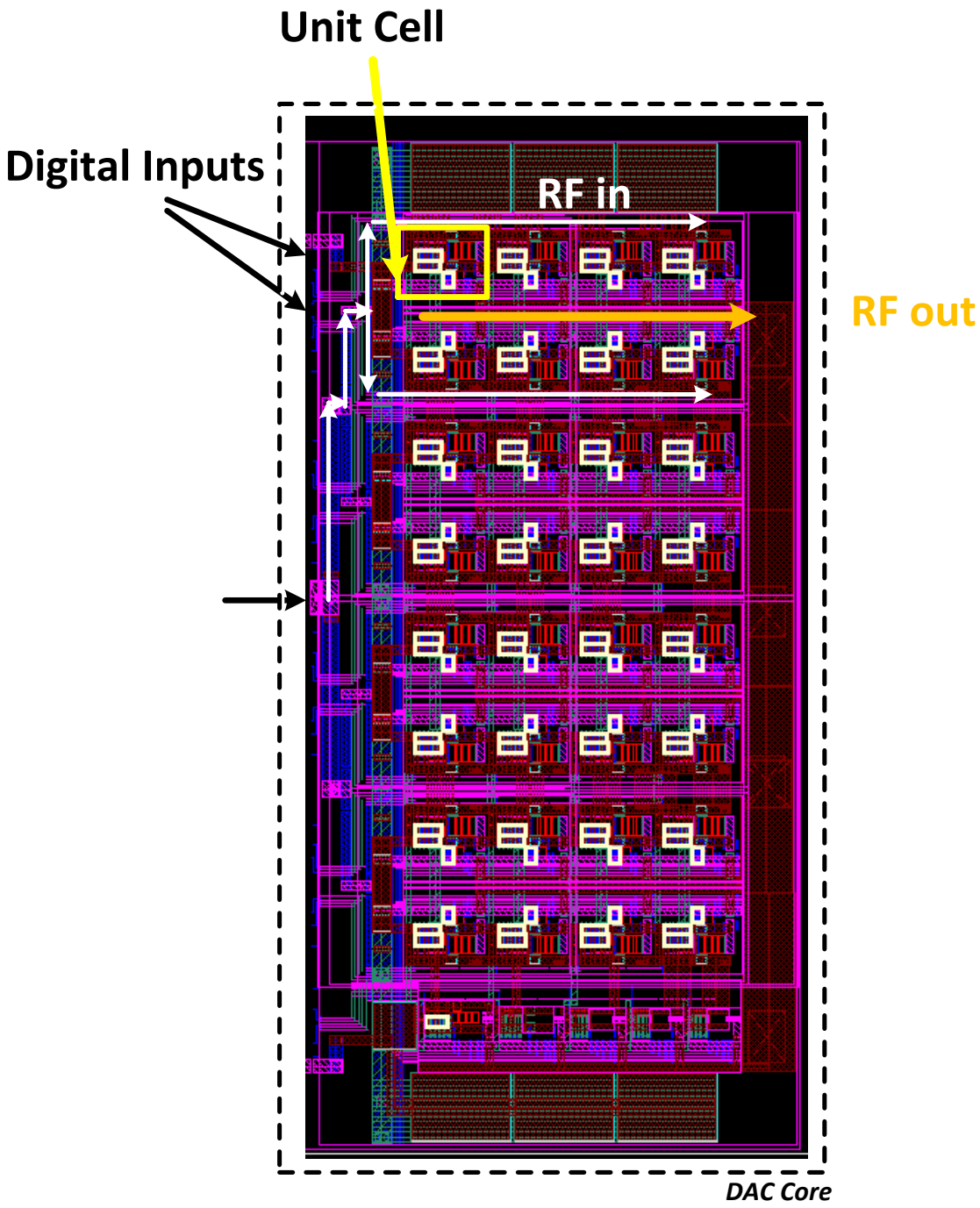


Figure 2.18. Layout of DAC Core

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ends of transistor, while DC bias is provided from one end of the gate line. Figure 2.17 shows the layout of unit stacked FET PA. The driver stages and the enable logic are also shown.

The input RF PM signal is fed to unit cells in corporate feed fashion to keep the phase similar. DAC core is made of 4 columns and 8 rows. Figure 2.18 shows the routing of input RF signal and output RF signal for top row of unit cell. Similar layout style is followed for a version of DPA with stacked FET PA built using floating body SOI transistors. Figure 2.19 shows the chip photograph of body contacted CMOS DPA.

## 2.4 Measurement Results

### 2.4.1 Measurement Set up

The CMOS DPA shown in Figure 2.19 was mounted on PCB with two metal layers and Rogers RO4003C substrate. The substrate thickness was 32 mils. Measurements were carried out at various frequencies with different matching networks. The PCB housed a single section *LC* match. The DC drain bias comes through a large Piconics conical inductor of 425 nH. A DC block is placed off the board. This constitutes the output bias-T.

The digital AM, RF PM, Gate biases and drain bias for stacked FET and RF output are all routed on board. The RF PM comes through a 50 Ω grounded CPW line.

The signal goes on chip through bond wire and sees a 50 Ω termination (Figure 2.11). This helps provide a wideband input matching and helps avoid frequency dependent matching network when test the DPA for wide range of frequencies. The 50 Ω

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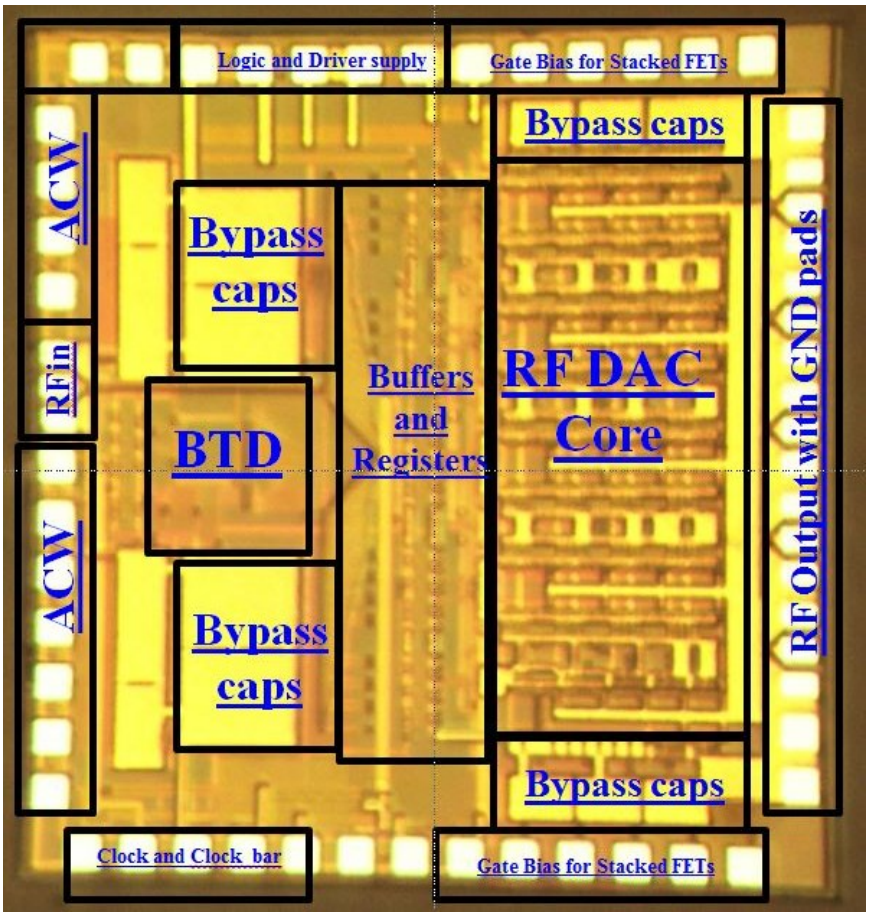


Figure 2.19. Chip Photo of CMOS DPA

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line (at input and output) on board was designed using sonnet EM simulation tool. The RF PM comes from Keysight ESG E4438C Vector Signal Generator.

The digital AM comes as 10-bit parallel word. This is fed from Keysight Logic Analysis System 16901A. The pattern generator module of 16901A provides 10-bit logic word with logic high of 3.3 V and logic low of 0 V. A set of resistive dividers are built on board with equal value SMD resistors. This brings the logic high down to 1.65 V.

Figure 2.20 shows the measurement set up. The ESG gives the phase modulated carrier signals, using data sampled at 45 MHz. The pulse pattern generator generates a clock of 45 MHz with LVPECL levels (high of 2.4 V and low of 1.6 V). This clock samples AM words from Logic analysis system.

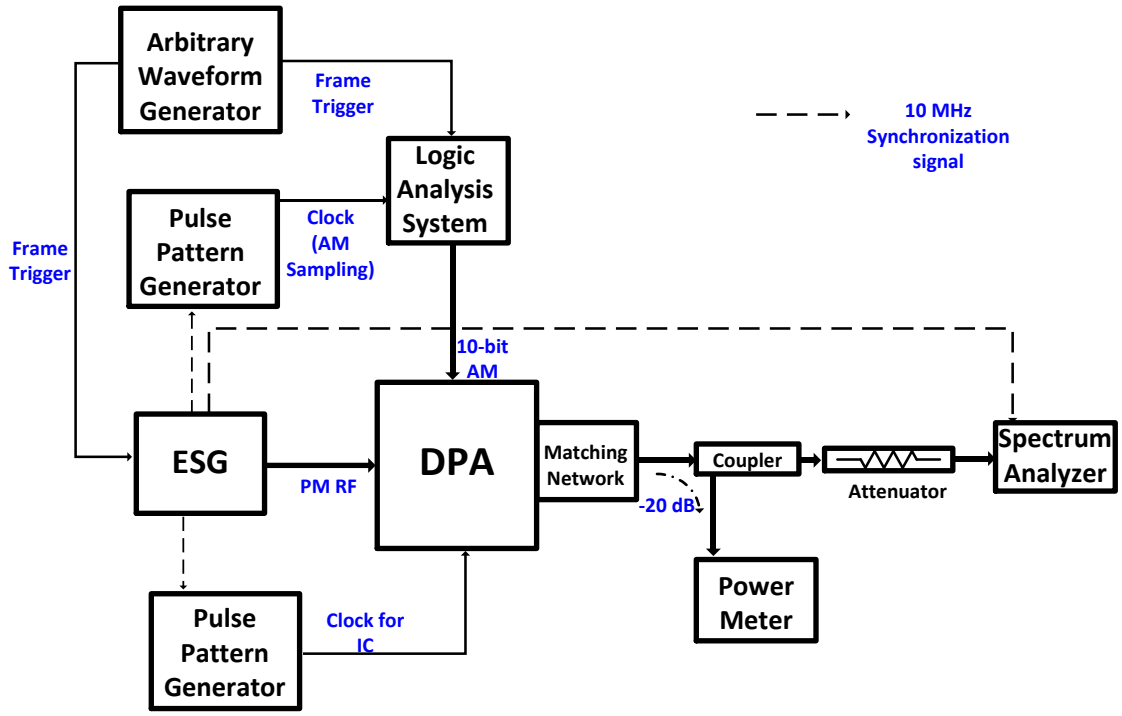


Figure 2.20. Block Diagram of Measurement Set up

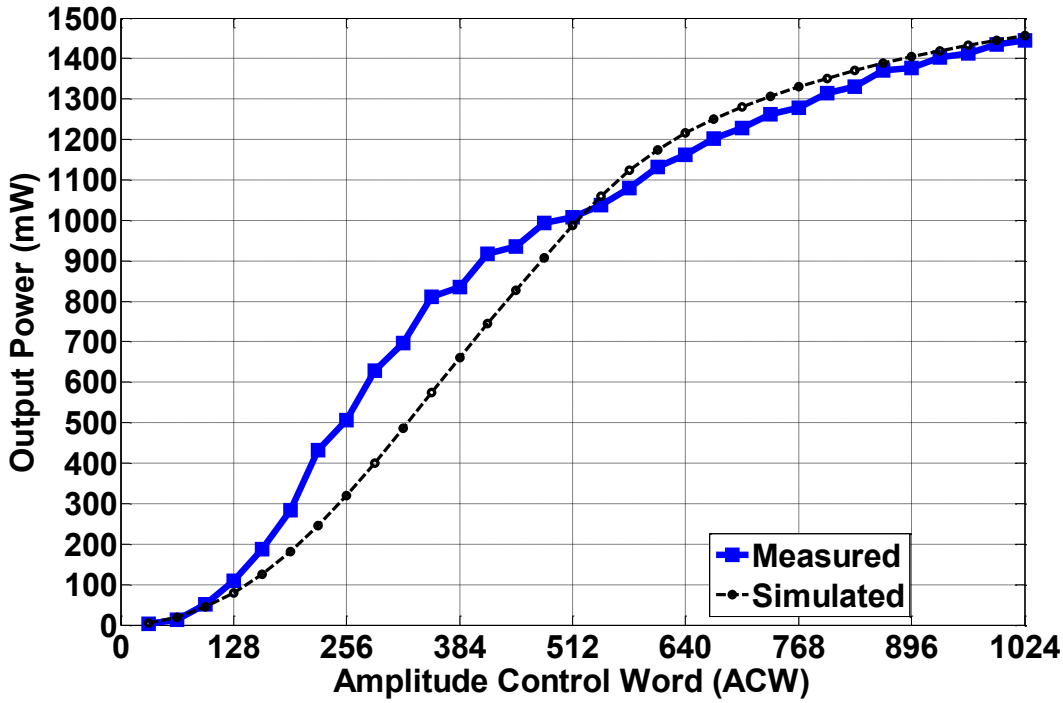


Figure 2.21. Output power of CMOS DPA at 900 MHz vs ACW

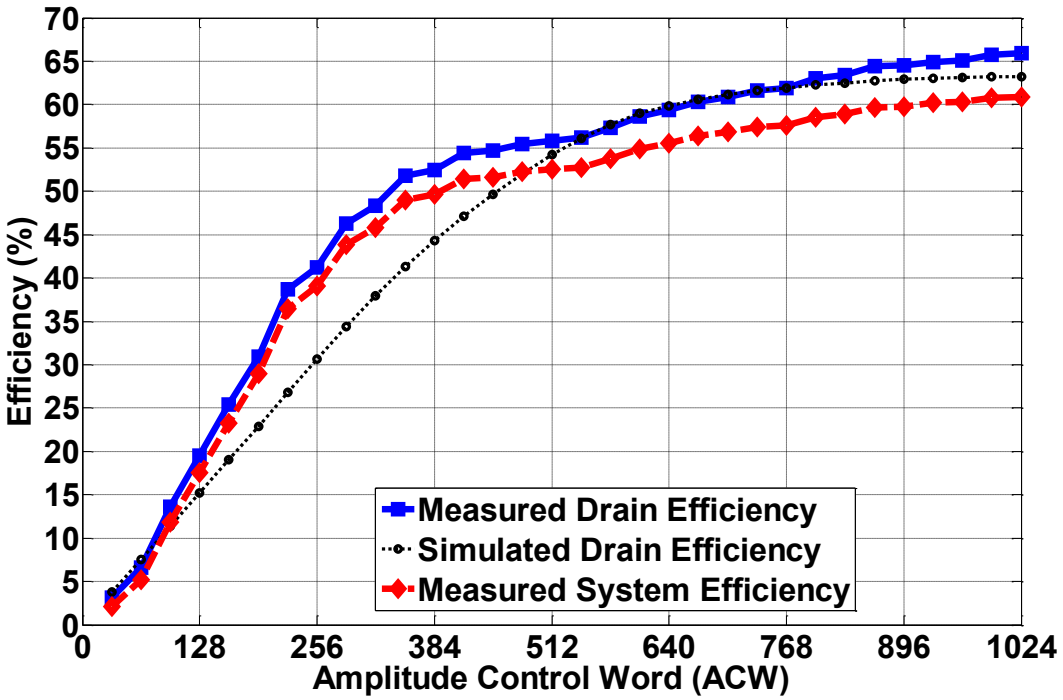


Figure 2.22. Drain and system efficiency of CMOS DPA versus ACW at 900 MHz

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Pulse pattern generator is also used to generate a 45 MHz clock for IC. This clock locks data in the registers shown in Figure 2.6. The needed clock and clock-bar are generated on the chip used set of inverters.

Time-alignment is a critical issue in polar transmitter. A frame trigger signal is needed to start the AM and PM data precisely at the same as PA input and may act as limiting factor for time-alignment accuracy.

On the output side a coupler is used to split the signal. Power meter measures power of coupled signal. An attenuator is used to bring power level down for spectrum analyzer. The down-converted IQ data is captured from spectrum analyser. The output spectrum 10 MHz reference signal is used to synchronize ESG, sampling clocks and spectrum analyser.

## 2.4.2 CW Measurement

The DC measurements show the triode region on-resistance of the DPA to be 500 mΩ. CW measurements are done with supply voltage of 4.5 V. Figure 2.21 shows measured and simulated output power versus ACW of body-contacted DPA at 900 MHz. The peak measured power is 1.45 W at 900 MHz. For low ACW, the power increases quadratic ally. This is because the current increases linearly with ACW. In this region, DPA acts like a current source. This is similar to adding current sources in parallel with ACW. At large ACW, the DPA acts as a switch. The effective width of DPA is large and impedance looking into drain is low. The DPA thus acts like a voltage source with relatively low source resistance. The output power gets compressed in this region with as the ACW is increased.

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Figure 2.22 shows the measured and simulated drain efficiency, and measured system efficiency versus ACW. The peak drain efficiency at 900 MHz is 65.9%. The system efficiency (SE) considers the power dissipated by driver stages and logic circuits.

$$SE = \frac{P_{out}}{P_{final-stage} + P_{driver} + P_{logic}}$$

The peak system efficiency at 900 MHz is 60.9%. The difference between drain and system efficiency at peak ACW is close to 6%. This difference goes down with ACW, the power consumed by drivers decrease with ACW because drivers are turned OFF in back-off. Figure 2.23 shows the efficiency behaviour in back-off. This matches

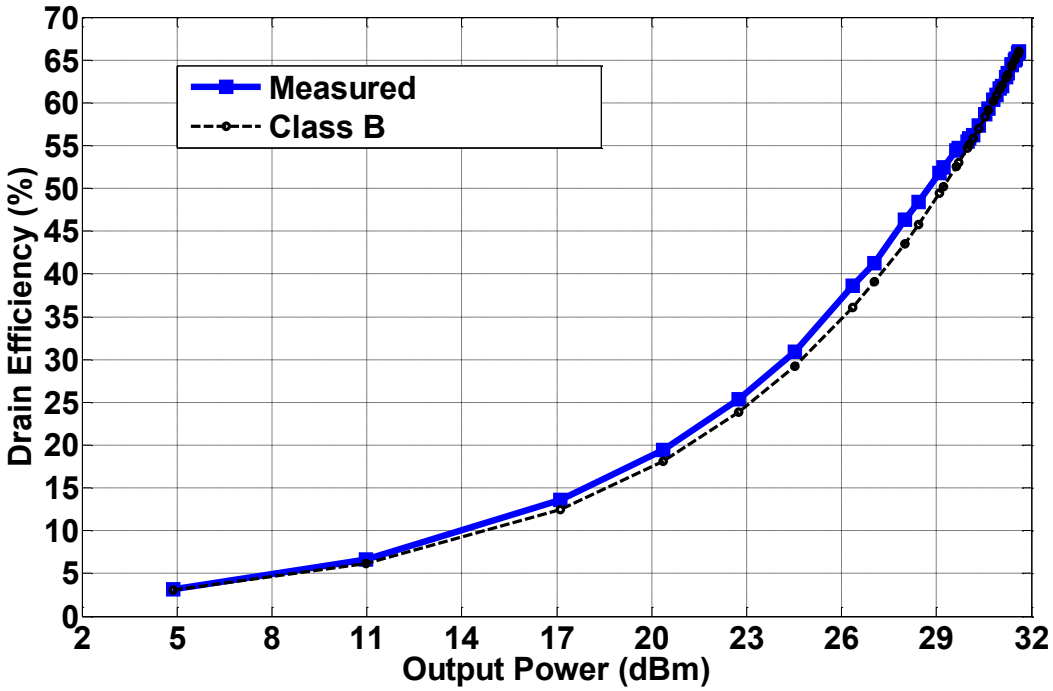


Figure 2.23. Measured drain efficiency of CMOS DPA versus output power at 900 MHz

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closely with class-B behaviour. Class-J amplifier is a class AB type PA with capacitive harmonic termination [19]. For half conduction cycle, this would lead to class-B like back-off behaviour.

Figure 2.24 shows the plot of measured and simulated normalized output voltage of DPA at 900 MHz versus ACW. This represents AMAM of CMOS DPA. For low ACW the output voltage increases linearly with ACW. This is region of linear operation DPA. For large ACW the out voltage shows compression. The measured AMAM behaviour is monotonous for unary cells. The non-monotonous behaviour exhibited is attributed to placement of binary cells in DAC core. Figure 2.25 shows the AMPM (or ACW-PM) behaviour of CMOS DPA at 900 MHz. The average phase distortion behaviour with ACW originates from active load-pulling as unit cells are gradually

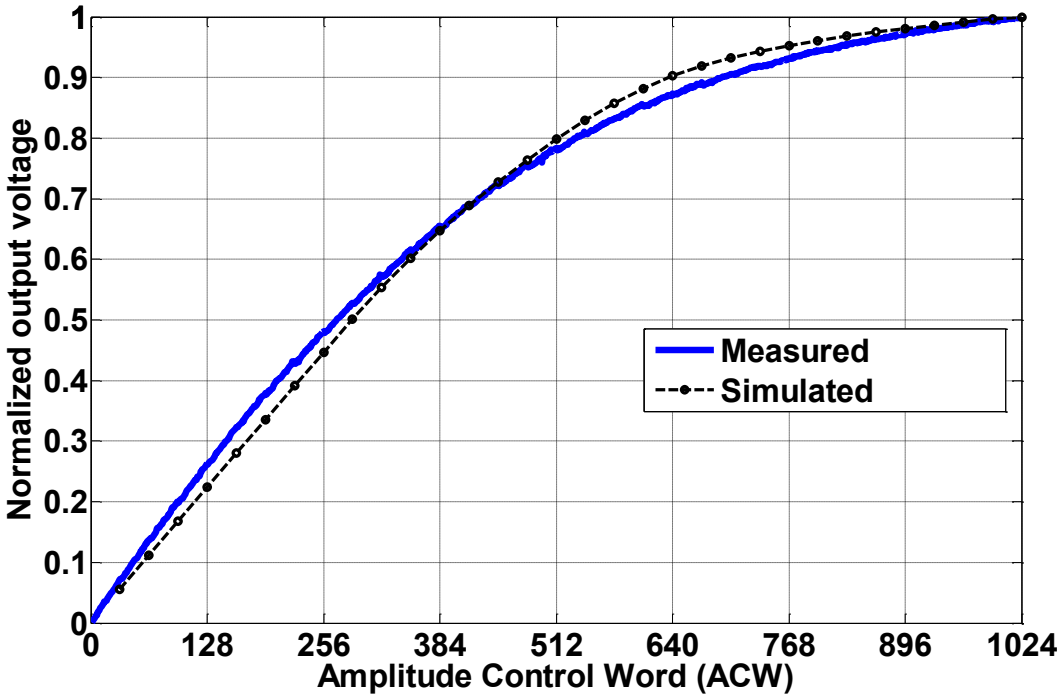


Figure 2.24. AM-AM behaviour of CMOS DPA at 900 MHz

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turned ON. Phase distortion is monotonic for unary cell variation, but exhibits non-monotonicity with binary cell variation. This effect is more visible for low ACWs and is attributed to the location of unary and binary cells in the DAC layout. In this design binary cells are placed as a separate block away from the first unary cell that turns ON. Placing the binary cells close to first unary cell limits the phase variation output for low ACW. Also, there are no significant glitches in ACW-PM behaviour; the RF input routing was done in "corporate-feed" fashion to mitigate this problem.

### 2.4.3 Modulated Signal Measurement

The digital PA was tested using a 5 MHz bandwidth uplink WCDMA signal with 3.4 dB PAPR. A LUT based DPD was used to achieve good ACPR as shown in Figure 2.26. The ACW and PM data were sampled at 45 MHz and digital PA used a 90 MHz

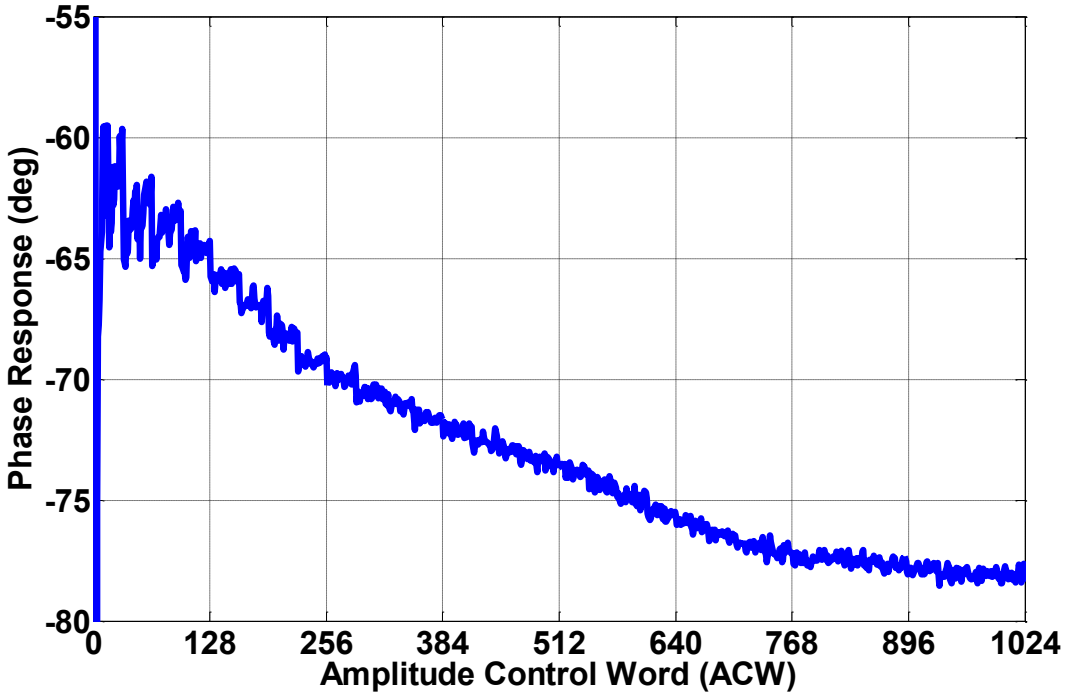


Figure 2.25. ACW-PM behaviour of CMOS DPA at 900 MHz

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clock for latching digital inputs. The digital PA yields an average output power of 28.3 dBm at an average drain efficiency of 49.5%. The ACLR1 at the output is 37.9 dBc and 37.3 dBc for low and high side of the band.

The digital PA was also tested using a 10 MHz bandwidth LTE signal with 6.5 dB PAPR with a look up table (LUT) based DPD. The digital PA gives average output power of 25.7 dBm at an average drain efficiency of 37.5%. The output spectrum is shown in Figure 2.27. Figure 2.28 shows the pre-DPD AMAM and post-DPD AMAM. Figure 2.29 shows the pre-DPD AMPM and post-DPD AMPM. The ACLR1 at the output is 33.7 dBc / 33.2 dBc for low / high side of the band.

The LUT developed is based on envelope enhanced memory polynomial (E2MP). The forward modelling of equation used is [18]:

$$y(n) = \sum_{m1=0}^{M1-1} \sum_{m2=0}^{M2-1} \sum_{k1=0}^{K1} \sum_{k2=0}^{K2} a_{m1m2k1k2} * x(n-m1) *$$

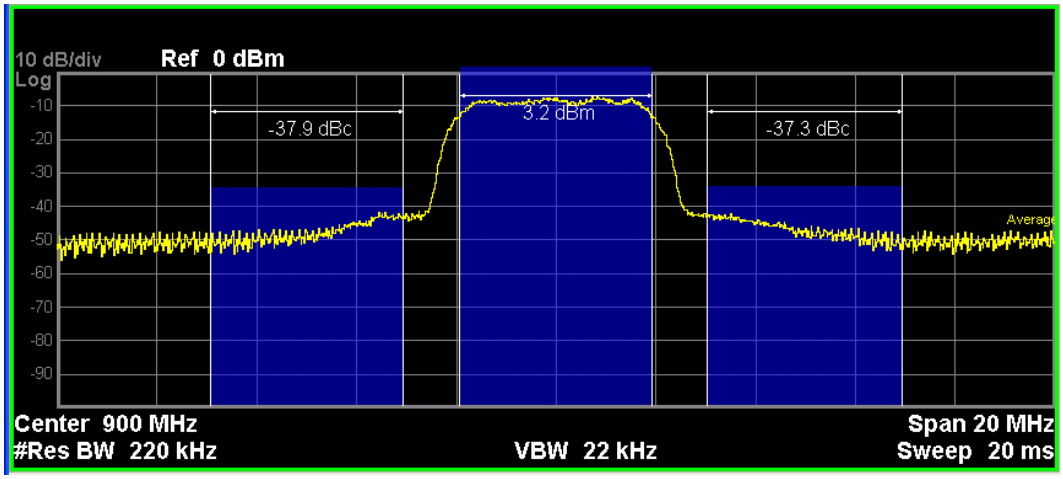


Figure 2.26. Measured output spectrum of 5 MHz WCDMA signal at 900 MHz

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$$|x(n-m1)|^{k1-1} * |x(n-m2)|^{k2-1}$$

where $a_{m1m2k1k2}$ are the model co-efficients with non-linearity order of K1 and K2 and memory depths of M1 and M2. This model helps address the non-linearity and memory effects emerging from interactions in AM and PM paths. In performing DPD for 10 MHz signal more than 100 co-efficients are needed.

To avoid computational overhead of memory polynomial, a memory-less LUT based pre-distortion is used. This method of linearization is apt for handset applications and more relevant for the designed DPA with handset level output power. The signal (16 QAM OFDM) has 5 MHz bandwidth and is centered at 836 MHz. The papr of

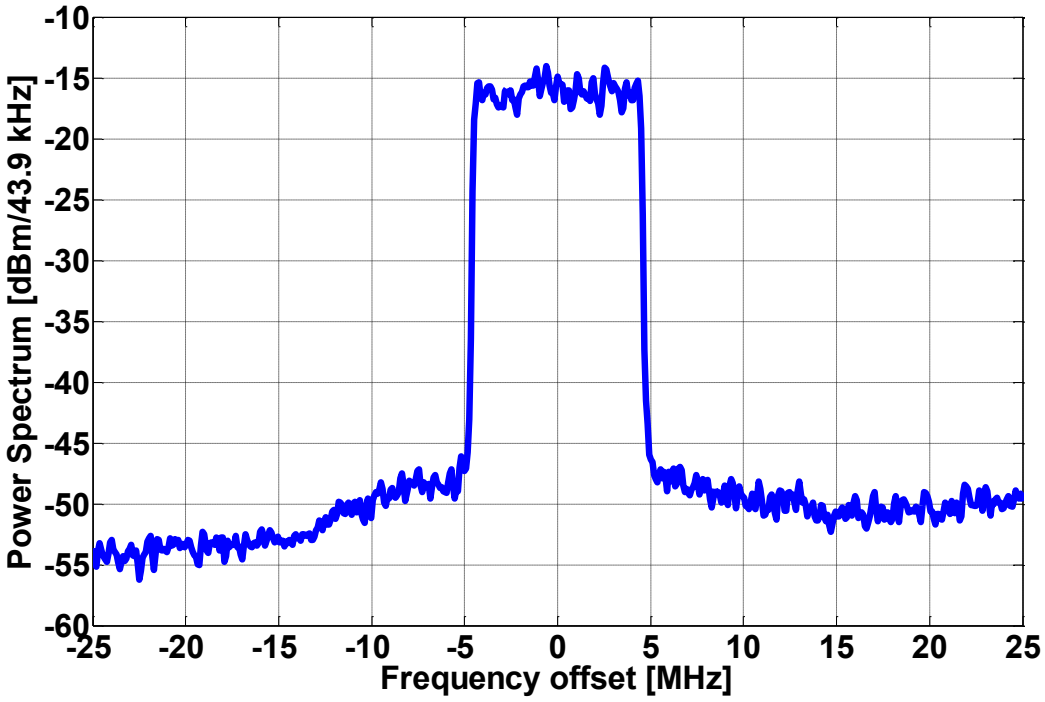


Figure 2.27. Measured output spectrum of 10 MHz LTE (16 QAM OFDM) signal at 900 MHz

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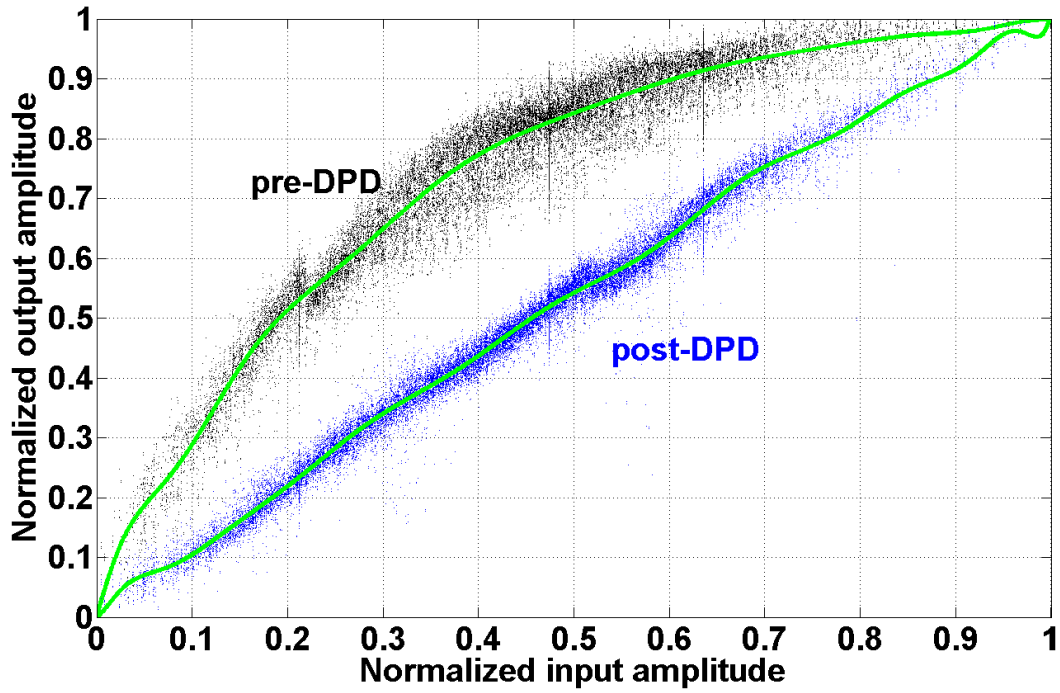


Figure 2.28. AMAM behaviour of CMOS DPA for 10 MHz LTE signal before and after E2MP

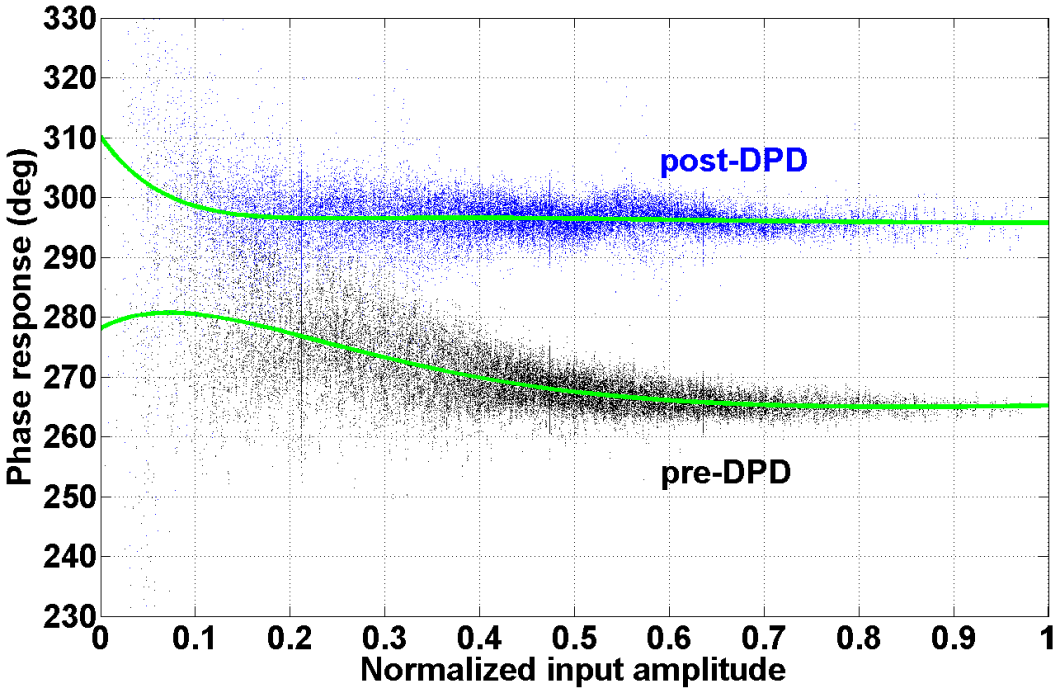


Figure 2.29. AMPM behaviour of CMOS DPA for 10 MHz LTE signal before and after E2MP

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signal is 7.6 dB and is sampled at 80 MHz. The output power is 22.3 dBm. The output spectrum is shown in Figure 2.30.

There are two reasons for the spread in AMAM and AMPM behaviour. The first is lack of enough decoupling for supply on and near the DPA chip; the second is time-mis-alignment between AM PM paths of DPA. The first one gets worse as sampling frequency of input data increases. The second one gets worse with signal bandwidth. The spread seen in Figure 2.31 and Figure 2.32 is due to increased sampling frequency of 80 MHz. The memory-less pre-distortion can correct the average line of AMPM behaviour in Figure 2.32; unlike the AMPM spread reduction in Figure 2.29. For circuits those are built using CMOS DPA, memory-less pre-distortion works well for 5 MHz wide signals.

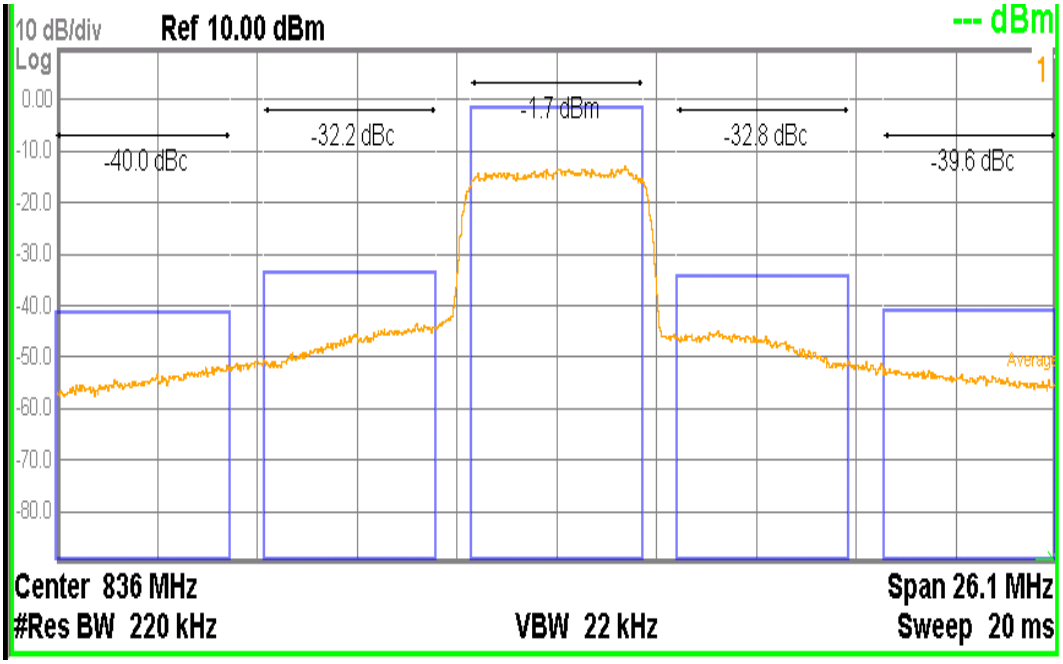


Figure 2.30. Measured output spectrum of 10 MHz LTE (16 QAM OFDM) signal at 900 MHz

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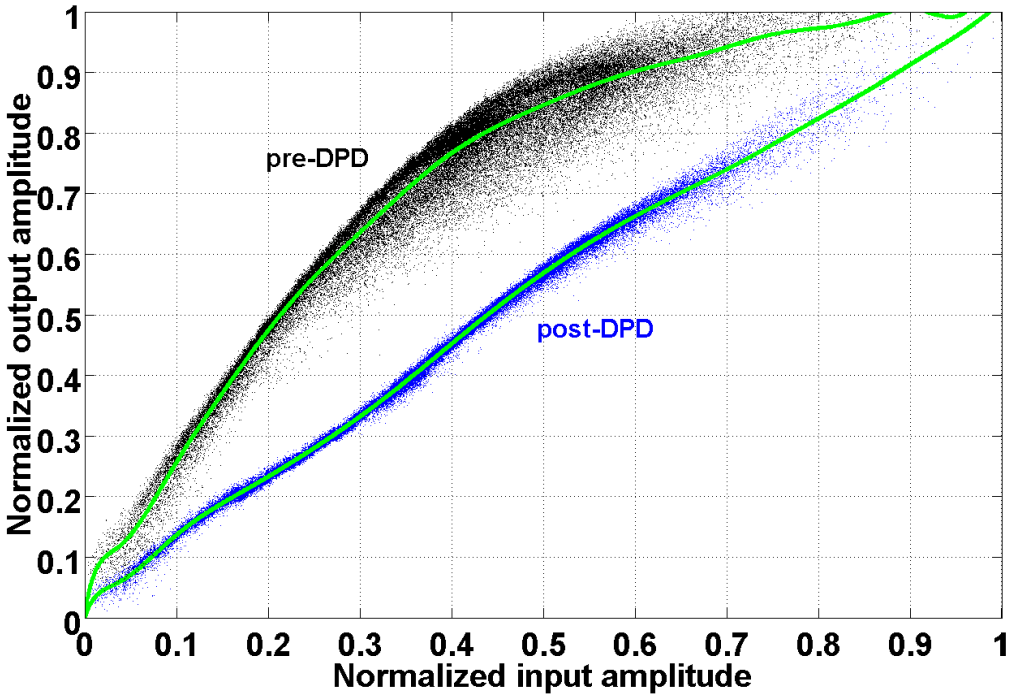


Figure 2.31. AMAM behaviour of CMOS DPA for 5 MHz LTE signal before and after memory-less predistortion

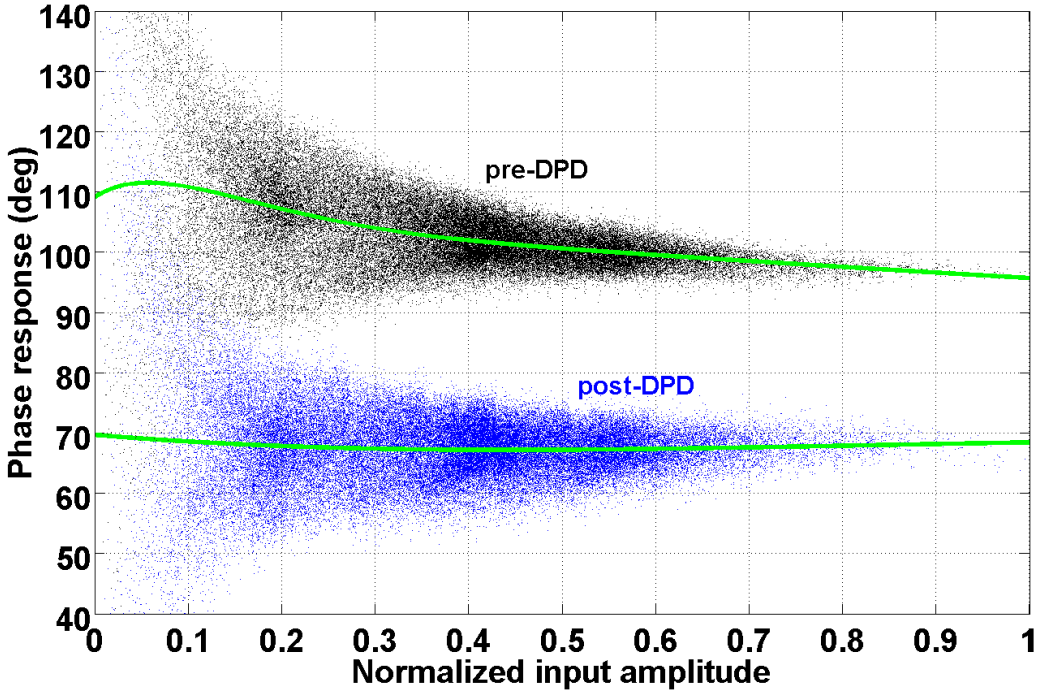


Figure 2.32. AMPM behaviour of CMOS DPA for 5 MHz LTE signal before and after memory-less predistortion

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Such correction is used in the coming chapters. Figure 2.33 shows the far-out spectrum for 5 MHz signal at output. The clock images are 40 dB lower than main band power. The noise floor is 40 dB lower to main band power.

### 2.4.4 Multi-frequency Operation

The CMOS DPA takes RF PM and digital AM as inputs to provide a reconstructed output with high efficiency. There are no frequency selective elements on CMOS DPA. The high efficiency is obtained by providing optimum load at the operating frequency by off-chip impedance matching network. By changing the matching network to provide optimum load at different frequencies, DPA can be made functional at different frequencies. Such an implementation would need a switchable matching

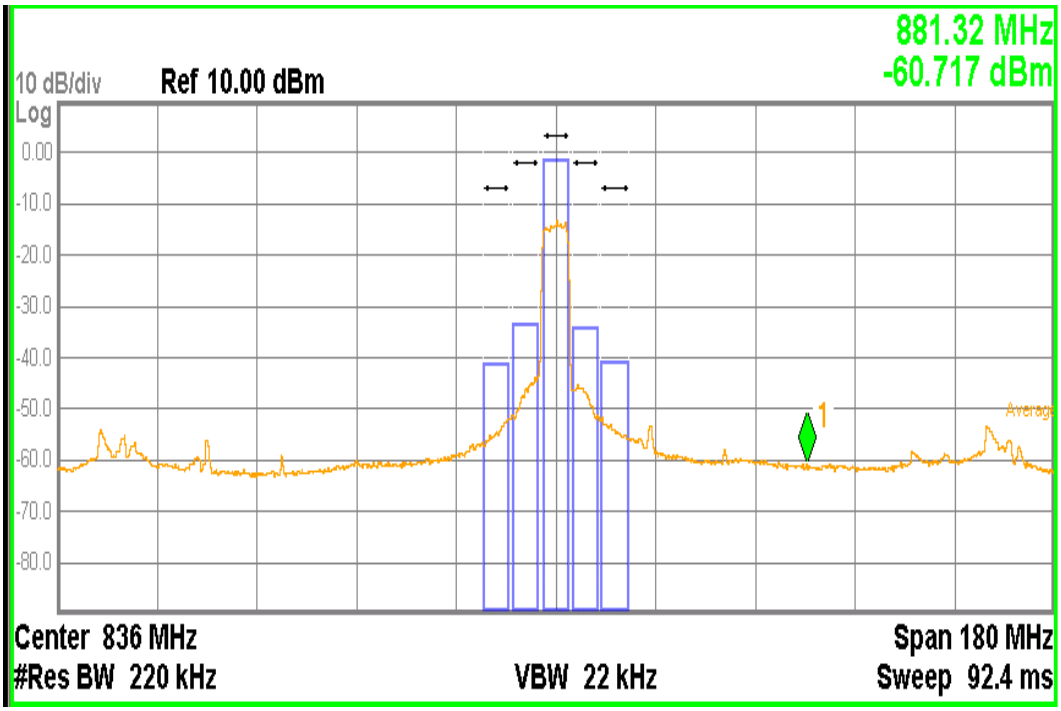


Figure 2.33. Far-out spectrum of 5 MHz LTE signal after memory-less pre-distortion

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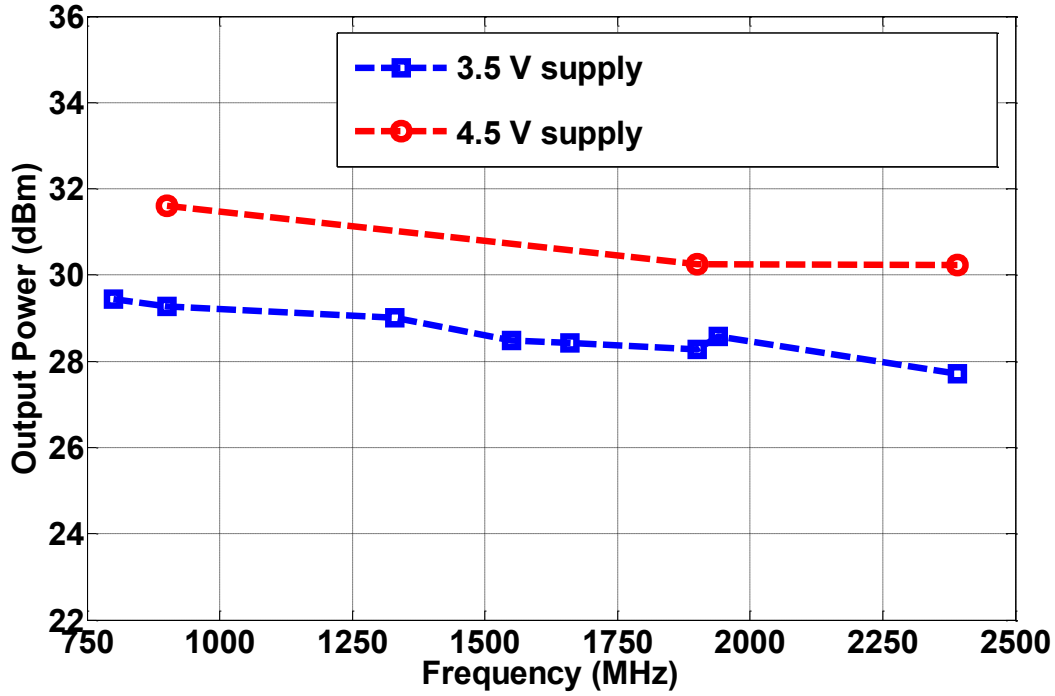


Figure 2.34. Multifrequency operation -- output power versus frequency of body-contacted CMOS DPA

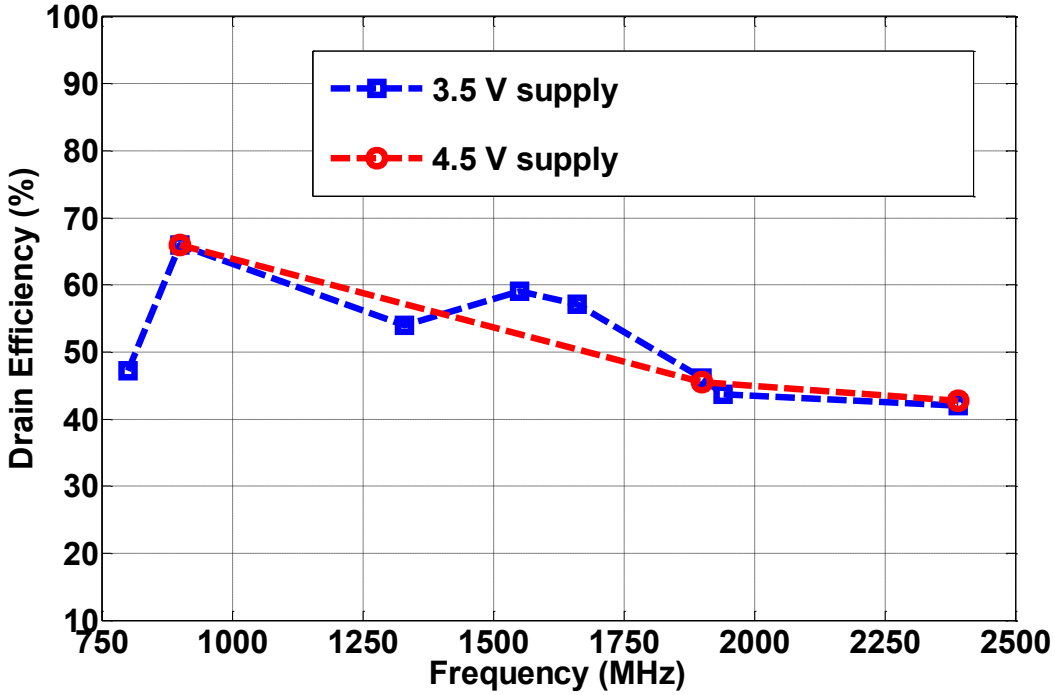


Figure 2.35. Multifrequency operation – drain efficiency versus frequency of body-contacted CMOS DPA memory-less predistortion

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network. Different matching networks in this work are implemented using SMD components on board, which are not switchable. Each network is a single section L-match. Figure 2.34 and Figure 2.35 show peak output power and peak drain efficiency at various frequencies of operation. The measurements indicate broadband performance of CMOS DPA of >50% drain efficiency.

Floating body devices are used to build ad different version of digitally controlled power amplifier. The FB devices come with lower parasitic capacitances. Lower Cgs leads to higher $f_t$ and lower drive power is needed. FB devices lead to lower parasitic capacitances at various nodes and help realizing output voltage and current signals with sharp edges. This leads to lower voltage and current overlap leading to high efficiency operation. Figure 2.36 shows the extracted capacitances between various nodes of body-contacted and floating-body FET with 160 µm width. The CW measurements are

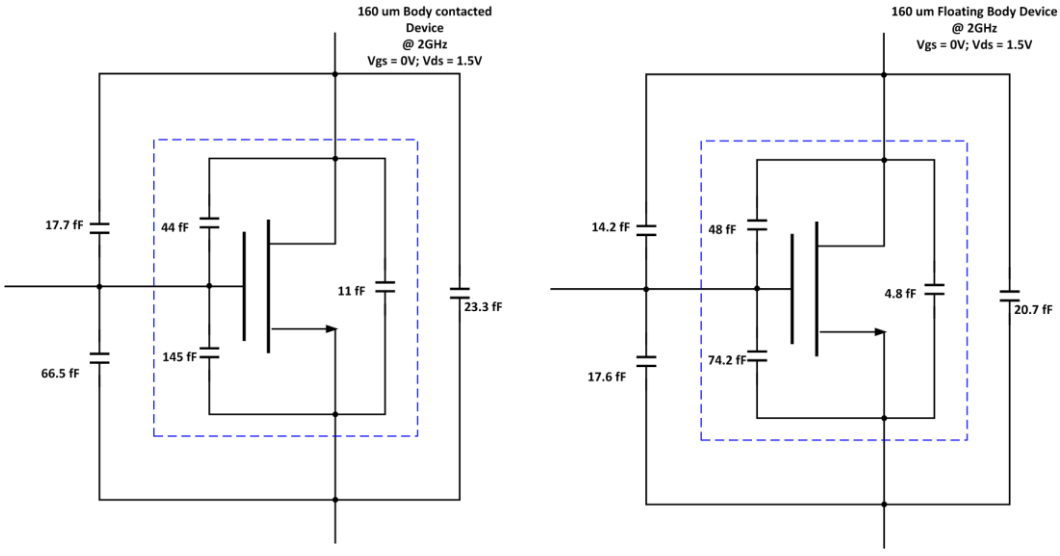


Figure 2.36. Parasitic capacitances of Body-contacted and Floating-body SOI FETs

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performed at various frequencies with 3.5 V supply. With the supply voltage of 4.5 V, FB-DPA gives output power of 1.35 W with drain efficiency over 65%.

Figure 2.37 shows the output power and drain efficiency of FB DPA at three operating frequencies. The efficiency at lower frequency – close to 900 MHz – is comparable for both BC and FB versions of DPA. At higher frequency – close to 2.5 GHz—FB DPA exhibits better efficiency.

## 2.5 Summary

A watt-class high-efficiency, digitally-controlled polar power amplifier has been demonstrated in 180 nm SOI CMOS technology. The 10-bit DPA is implemented in two

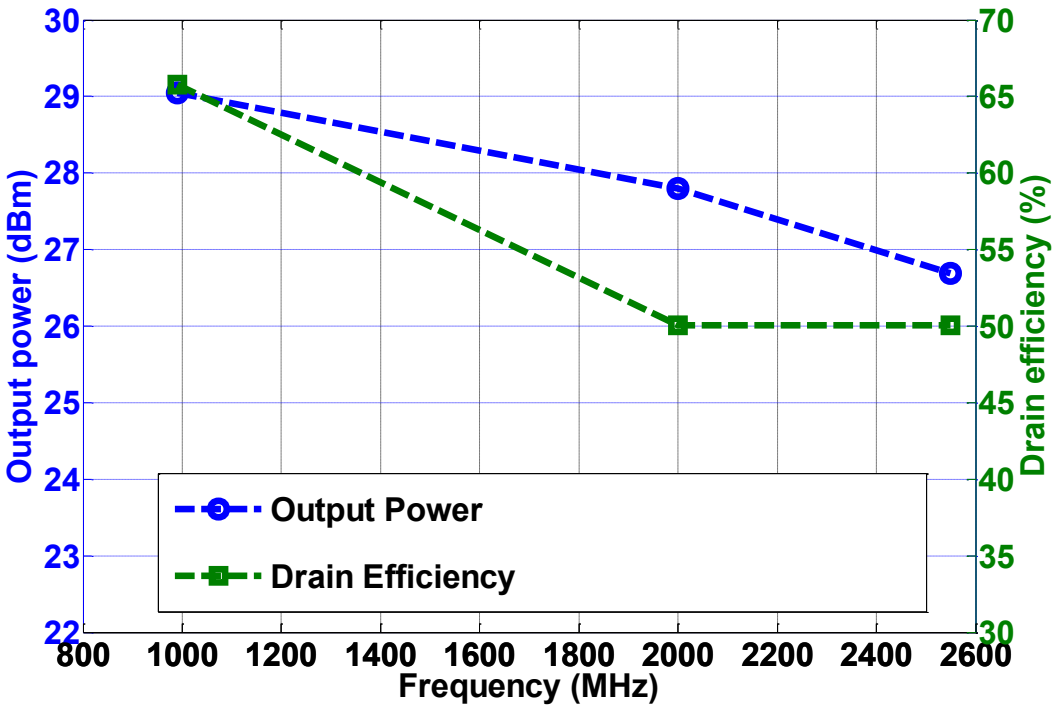


Figure 2.37. Multi-frequency operation of floating body DPA

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versions – one using body-contacted SOI devices and second using floating-body SOI devices. The body-contacted SOI version of this design achieves 31.6 dBm of output power at 65.9% drain efficiency with an external LC matching network. Both versions demonstrate multi-frequency operation. BC version of DPA is tested from 800 MHz to 2.5 GHz. The FB version of DPA shows improved efficiency at higher frequencies compared to BC version of DPA. The BC DPA design has been shown to work for WCDMA and LTE standards.

## 2.6 Acknowledgement

Part of the material in Chapter 2 appears in "A Watt-Class, High-Efficiency, Digitally-Modulated Polar Power Amplifier in SOI CMOS", V. Diddi, H. Gheidi, Y. Liu, J. Buckwalter and P. Asbeck, IEEE CSICS Symposium 2015. The author of this dissertation was the primary investigator and primary author for this publication.

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# Chapter 3

# High Power, High Efficiency Digital Doherty Polar Power Amplifier in CMOS SOI Technology

## 3.1 Introduction

Evolution of wireless technology has led to widespread use of spectrally efficient modulation methods such as higher order Quadrature Amplitude Modulation (QAM) and OFDM, leading to signals with high peak-to-average ratio (PAPR). To transmit such signals efficiently, a power amplifier (PA) with good back-off efficiency behavior is needed. This chapter addresses the development of a CMOS SOI power amplifier with better backoff efficiency than that of the amplifier described in Chapter 2.

To achieve improved backoff efficiency, multiple power amplifier architectures have been explored, including outphasing [2-5], envelope tracking [6-9], Doherty [10-13].The Doherty architecture was introduced in 1936 as a means of achieving high efficiency for modulated signals [1]. This architecture is one of the promising candidates

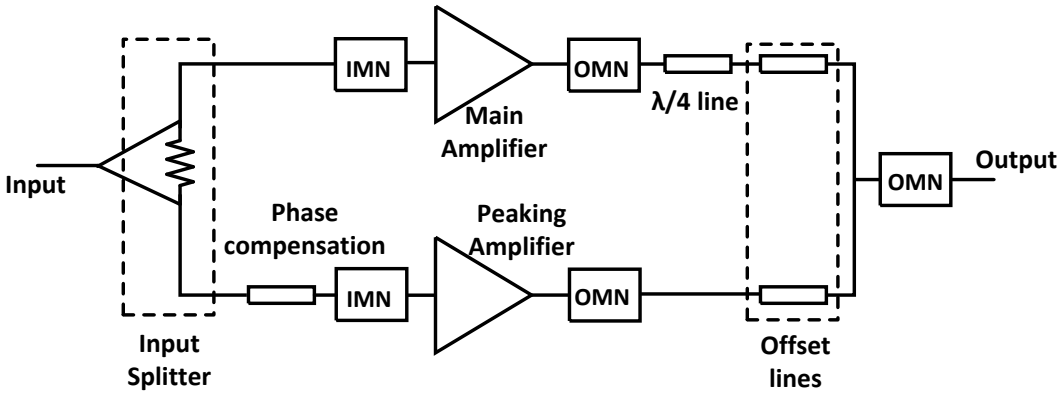


Figure 3.1. Block diagram of conventional Doherty power amplifier

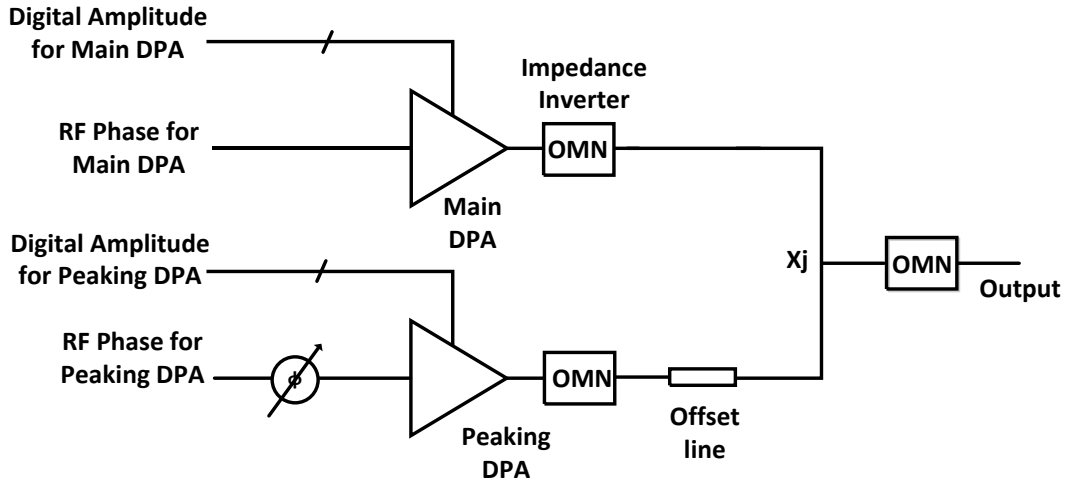


Figure 3.2. Block diagram of proposed digital Doherty power amplifier

for PAs for cellular handset applications [14-15], and is typically implemented as shown in Fig.1. In this chapter, a Doherty power amplifier implemented using CMOS SOI technology is described in which the unit amplifiers have amplitudes controlled by digital rather than analog inputs. The main PA (MPA) and peaking PA (PPA) utilize the polar architecture; each has digitally-controlled amplitude and can be considered as an RFDAC (RF Digital-to-Analog Converter). This architecture provides flexible and accurate control over turn-on power level and gain for the PPA relative to the MPA. In the traditional Doherty PA, the peaking amplifier goes from class-C to class-B with input power in gradual fashion. With the digital Doherty PA (DDPA), the PPA turn-on is ideal, leading to a sharp peak in back-off efficiency. Figure 3.2 shows the proposed architecture.

CMOS-based DDPAs have been previously reported [16]. In contrast to the prior work, a CMOS DDPA with output power levels that correspond to the requirements for handset PAs (maximum power of order 2W) has been designed in this work. We also demonstrate very high efficiency (above 50% at 6 dB backoff), which is of interest in mobile radio applications.

CMOS FETs have comparatively low breakdown voltage, making them less suitable for power amplifier design. In order to increase the voltage handling capacity, the stacked-FET technique [17] is used here, facilitated by implementation in SOI technology. An output combiner based on lumped elements is used to provide impedance inversion as well as impedance transformation. The input for DDPA is dual drive – two separate inputs for MPA and PPA with controllable phase difference between them.

## 3.2 Digital Doherty Power Amplifier Design

### 3.2.1 Practical Doherty Power Amplifier Design Challenges

The traditional Doherty amplifier architecture is shown in Figure 3.1. The main and peaking amplifier outputs are combined using a quarter-wave transmission line, which acts as impedance inverter. At low output power levels only the MPA is active; as the input power is increased, the MPA saturates for the load impedance it experiences, leading to high efficiency behavior. When input power is further increased, the PPA turns on, and its output current increases the voltage swing and effective load impedance at the combiner output. The impedance inverter translates this output load increase to a load decrease at the drain of MPA, moving it out of saturation. With further increases in input

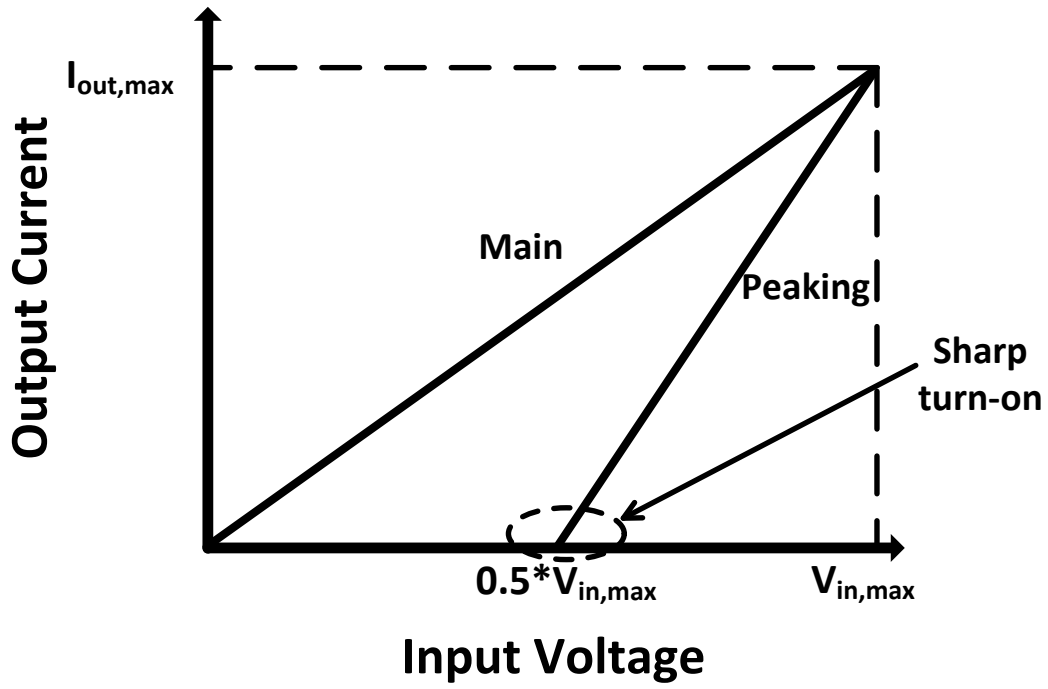


Figure 3.3. Current outputs of main and peaking amplifiers in ideal Doherty PA

power, both MPA and PPA saturate, giving also high efficiency behavior.

For high efficiency in backoff, it is critical that the MPA become saturated with PPA in OFF state. It is difficult to realize this in the traditional analog-Doherty which uses a PPA biased in class C. The gradual turn-on characteristics of the PPA do not allow sharp saturation of the MPA, and cause a related loss of power gain at the transition power level. The output current required of the PPA as a function of input amplitude is shown in Figure 3.3, which shows that, after turn-on, the PPA requires a gain twice that of MPA. Previously, this is implemented by using unequal sizes for MPA and PPA [19-20], unequal power division [21]. The precise control over the PPA characteristics available in the DDPA avoids this problem. In a digital PA, output current can be directly specified with the input digital code. This makes the DDPA a more attractive and simpler solution than an analog Doherty PA.

The implementation of the impedance inverter is another challenge in the Doherty architecture. Transmission-line impedance inverters commonly used in base-station amplifiers are too large for handset applications. Many works [14-15] have used lumped element equivalents, which reduce area, although these networks typically come with bandwidth limitations [15]. An output matching network is also needed to translate the final 50 Ω impedance to optimum impedances for both MPA and PPA. Offset transmission lines are typically employed to move the PPA impedance in back off to an appropriately high level [22]. In this work, output matching networks, impedance inverter and offset lines are implemented in hybrid fashion, with lumped elements on a PCB with straightforward design, as shown schematically in Figure 3.2. Impedance matching

external to an IC is commonplace for handset power amplifiers, and is conducive to high power handling with high efficiency.

At the input of the traditional Doherty there is a power splitter, to divide the inputs between the MPA and PPA. It is challenging to design an appropriate fixed power splitting ratio, since the PPA requires no input power in back off, while its overall gain should be twice that of the MPA at high input power, as noted above. The power splitting ratio in practice also depends on the input impedances of the MPA and PPA, which are biased differently and have power dependent input capacitances [14, 23]. This results in non-ideal back-off behavior of traditional Doherty PAs. Wilkinson power splitters are typically used at the input, although some works [14-15] have proposed direct connected power splitter for handset Doherty PAs. In the present design, the input power splitting function is carried out by selection of the appropriate digital inputs to the MPA and PPA, in straightforward fashion. At the input there is also a phase compensation network, to compensate for the phase lag of the impedance inverter at the output of MPA. The phase variation of signal through MPA and PPA is dominated by their respective AM-PM behaviors. This is a significant problem in analog Doherty PA where PPA path shows large AMPM response. One of the ways of mitigating this problem is to use dual-phase inputs [24]. In this work dual phase inputs are used; the relative phase between MPA and PPA can be controlled and varied at the modulation rate.

### 3.2.2 Doherty Combiner Design

The Doherty output combiner has three parts. One section goes from output of MPA to junction point (marked as Xj in Figure 3.2). The second section goes from the PPA output to the junction point. The third section goes from junction point to the final

50 Ω load. Traditionally all these sections are implemented using transmission line structures [27].

In this work, the third section is an L-match converting 25 Ω to 50 Ω. For both MPA and PPA, a class-J-like load is used. A class-J amplifier load is inductive at the fundamental and capacitive at second harmonic. The nominal Class J impedances correspond to:

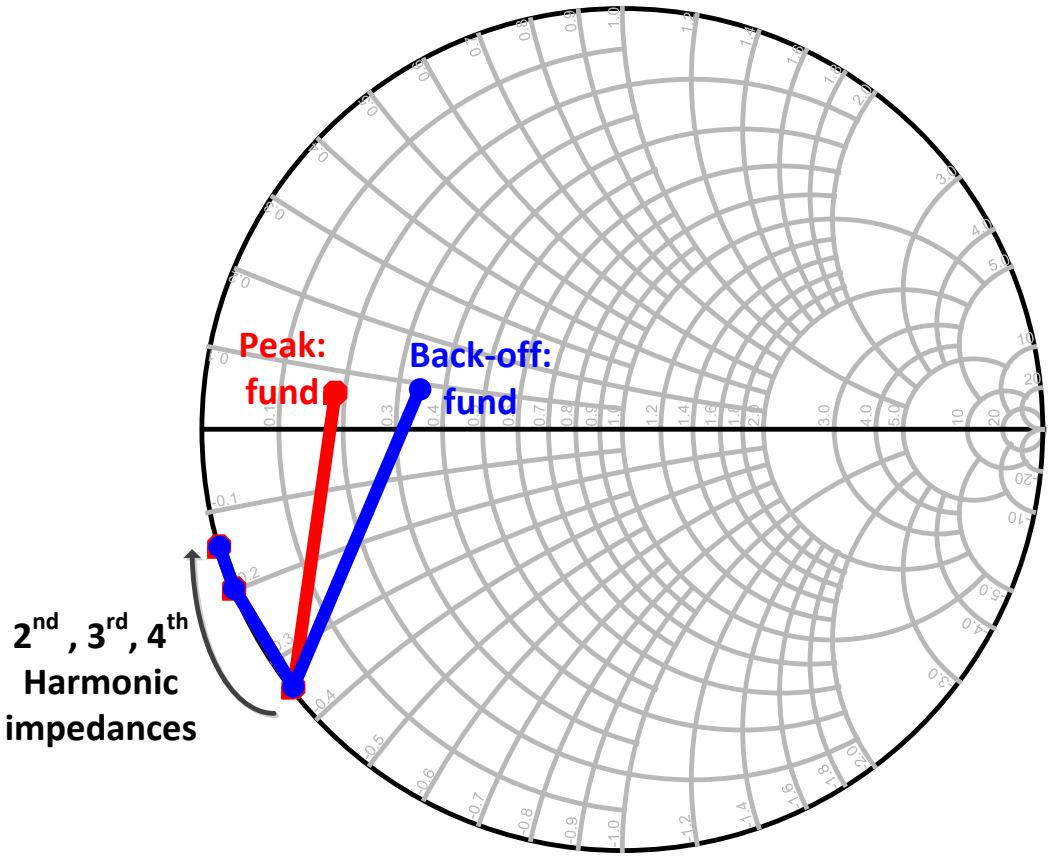


Figure 3.4. Simulated load seen by MPA current generators at peak and back-off at various harmonic frequencies

$$Impedance\ at\ Fundamental: Z_1 = \sqrt{2}R_{opt} \angle 45^0$$

$$Impedance\ at\ 2nd\ Harmonic: \ Z_2 = \frac{3\pi}{8} R_{opt} \angle -90^0$$

Impedances for all higher harmonics are zero.

In this work, the impedance presented to the current generators within the DPA is approximately 9 + j3 Ω for peak power operation for both the MPA and PPA (which is similar to what has been used with individual DPAs).

For the MPA in back-off operation, the load presented to the current generators is

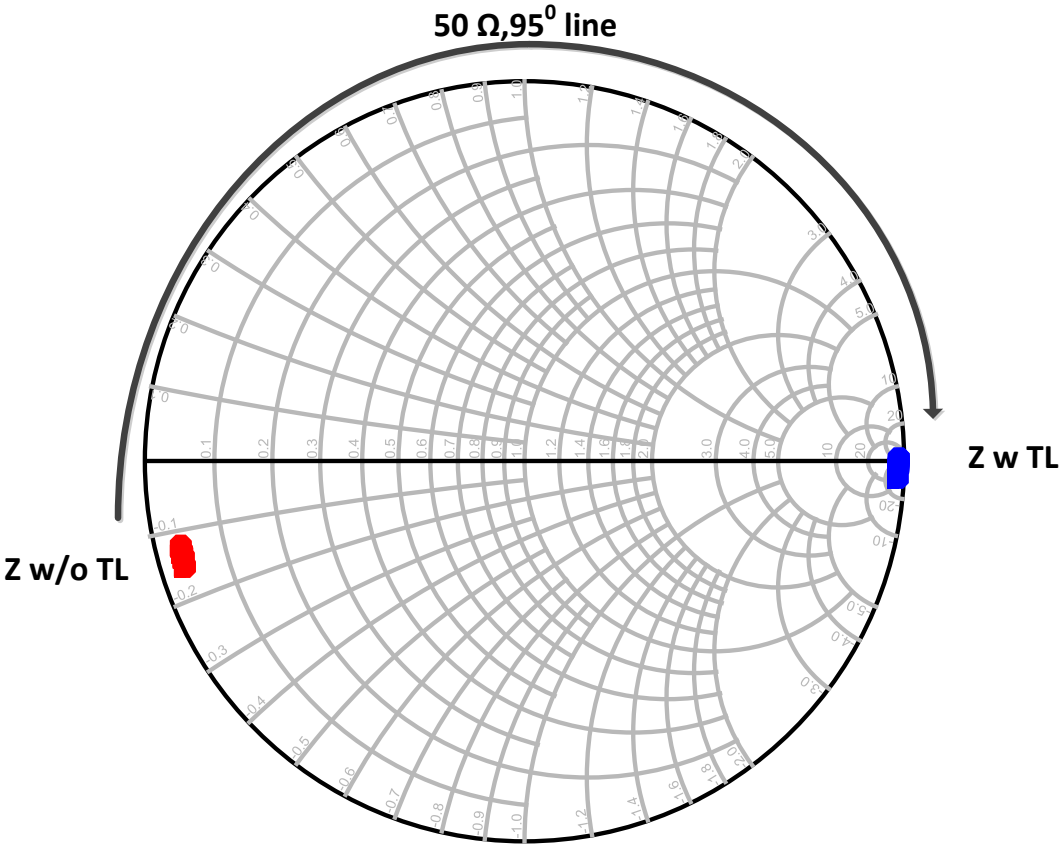


Figure 3.5. Simulated load looking into PPA at junction point with and without offset line.

17.1 + j4.3 Ω. In order to provide this increase in load impedance, the matching network also acts as impedance inverter [15]. The matching and impedance inverter are implemented with parasitic $C_{out}$, parasitic $L_{bw}$, and surface mounted components $L_{m1}$and $C_{m1}$ (shown in Figure 3.7). This circuit acts as a π-network equivalent to a λ/4 impedance inverter of $Z_0$ close to 21 Ω. Figure 3.4 shows the harmonic load seen by MPA at various harmonic frequencies, both at peak and back-off operation.

For the PPA, the output network must perform impedance matching. Additionally, in back-off when the PPA is off, the output network needs to ensure that the impedance seen from junction point towards the PPA is essentially an open. There is large parasitic capacitor at the output of PPA, however: Cout~ 6.8 pF. Without an offset line, the impedance looking into the PPA is 1.74 – j6.78. To transform this into an "open", an offset line of 50 Ω and 95° electrical length is used. Figure 3.5 shows the load impedance and its transformation using the offset line. Figure 3.6 shows the notional

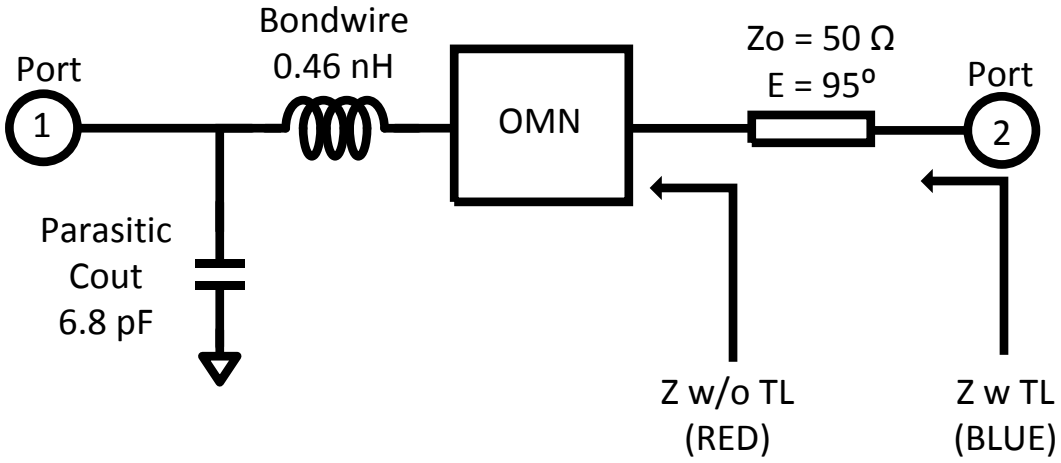


Figure 3.6. Load looking into PPA at junction point with and without offset line.

equivalent output network used for the PPA. Port 1 represents the PPA together with its parasitic capacitance of 6.8 pF. Port 2 represents the junction point in the Doherty combiner. The transmission line implementation shown in the figure, however, is not area efficient. The combination of output matching network and offset line is transformed into an equivalent T-network on the PCB. This network is implemented using parasitic $C_{out}$, parasitic $L_{bw}$, and surface mount components $L_{p1}$, $C_{p1}$ and $L_{p2}$. Figure 3.7 shows the Digital Doherty PA with Main and Peaking amplifiers along with output combiner.

### 3.2.3 Digital Doherty Load Modulation

In a manner similar to the traditional analog Doherty, in order to high efficiency

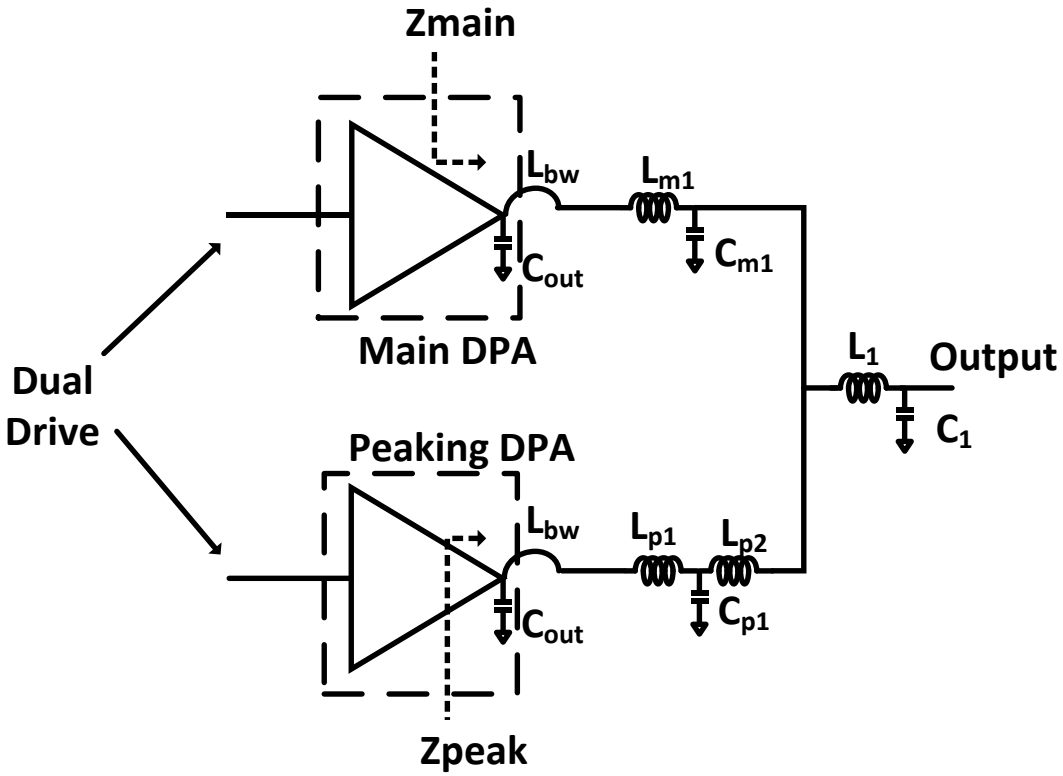


Figure 3.7. Output combiner for DDPA

peaking in back-off, the MPA needs to be saturated with the PPA OFF. Then the PPA needs to be turned ON in a manner that keeps the MPA in saturation for higher power levels. To achieve this, the digital codes for MPA are increased till half the full scale amplitude while the PPA is OFF. After this, the digital code for the PPA is increased so that the amplitude rises at approximately twice the rate as that of MPA. Figure 3.8 graphically depicts the baseline variation of digital codes (ACWs) of the MPA and the PPA, using this piecewise linear variation. Figure 3.9 shows the corresponding variation in the magnitude of the fundamental load impedance seen by the current generators of the MPA and the PPA.

Figure 3.10 shows the output currents of the MPA and the PPA. At the end of the

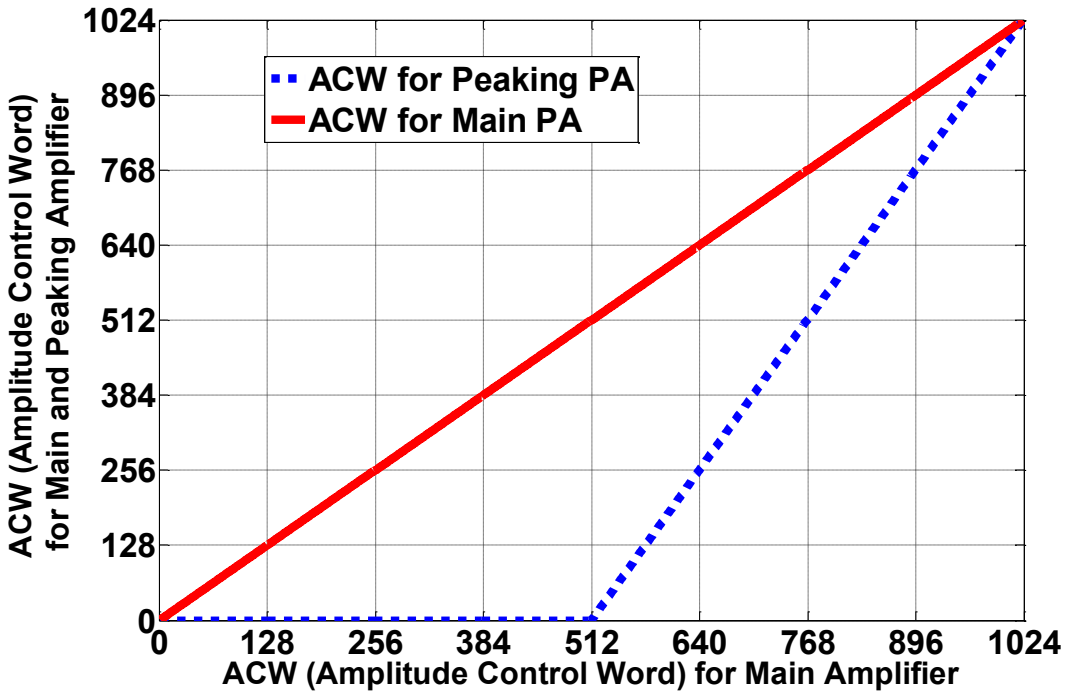


Figure 3.8. ACW profile for Main and Peaking PA

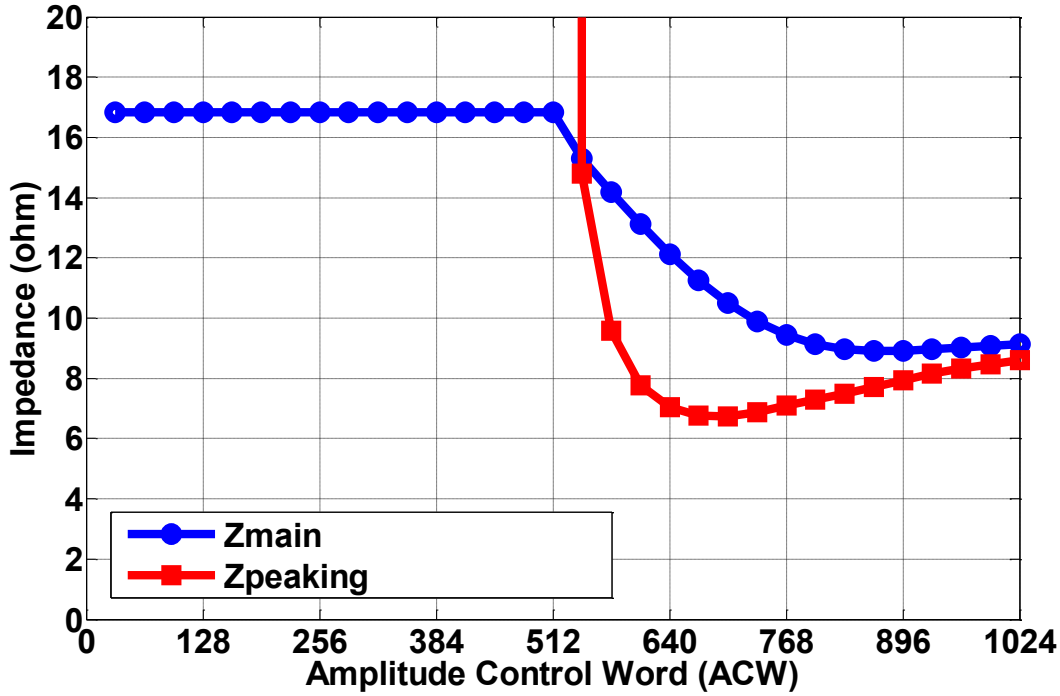


Figure 3.9. Simulated Load Impedance Modulation seen in Main PA due to Peaking PA

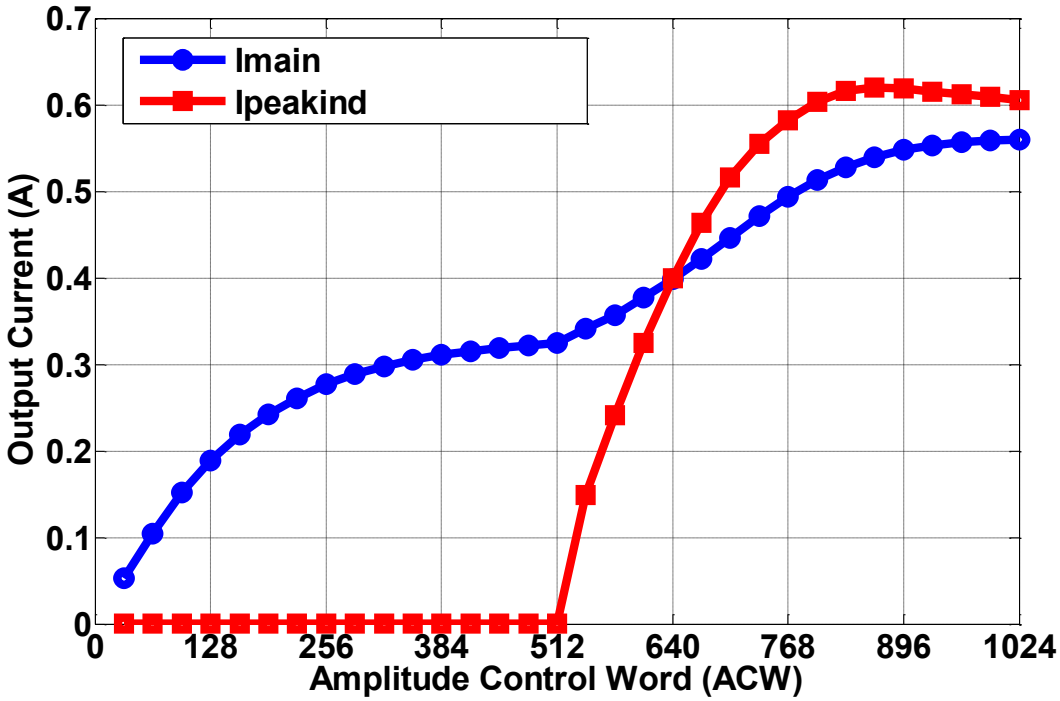


Figure 3.10. Simulated fundamental output current amplitudes of Main PA and Peaking PA with ACW

sweep to midrange ACW, the MPA saturates, as seen in its output current profile. The corresponding output power is approximately a quarter of the maximum power (6-dB back off) and a maximum efficiency point. During the second half of the sweep, the PPA is active and modulates the load seen by MPA as shown in Figure 3.9. During this phase the output current of MPA is increased as its load is decreased. To reach same final output current, the ACW of the PPA is increased at twice the rate as that of the MPA. At peak ACW, both MPA and PPA are saturated, and their output currents are similar. This corresponds to the peak power, high efficiency point of the DDPA.

Figure 3.11 shows the fundamental output voltage amplitude variation for MPA and PPA with ACW. For ACW less than 512, the voltage of the MPA saturates at the end

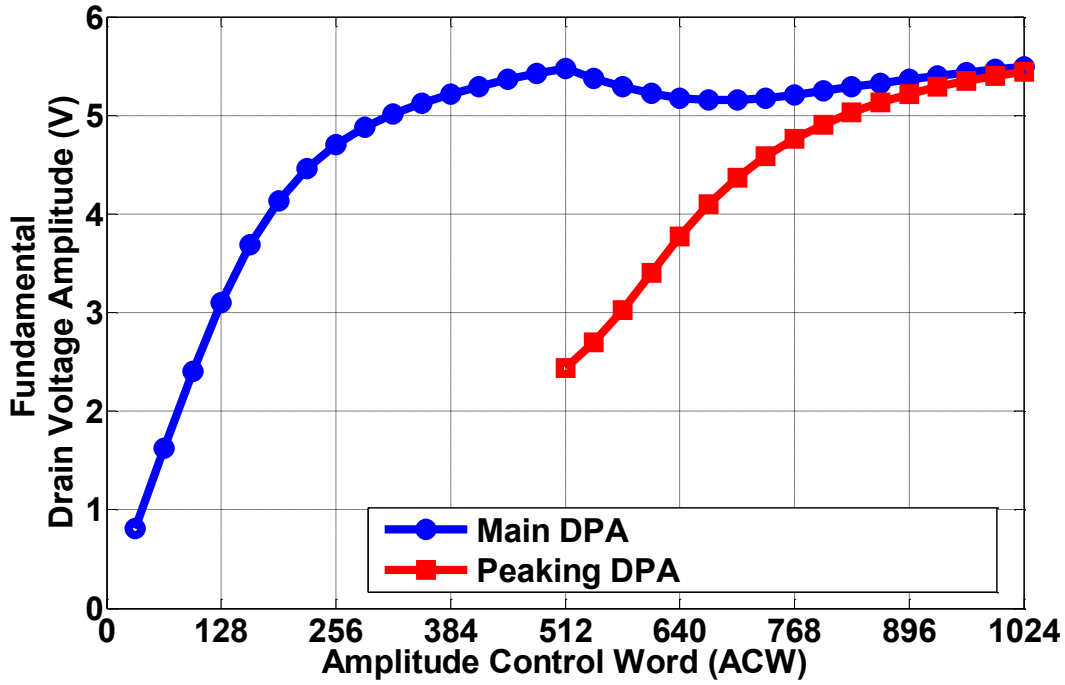


Figure 3.11. Simulated fundamental output voltage amplitudes Main PA and Peaking PA with ACW

of the first half sweep. In the second half of the ACW sweep, the output voltage of MPA remains close to saturation. During this region the MPA operates with high efficiency. The voltage output of PPA increases to reach the saturation value similar to the MPA.

Figure 3.12 shows the load modulation of the MPA by the PPA. When PPA is OFF, load seen by the MPA is high (17 + j4 Ω). The load seen by the PPA is a large capacitor, dominated by OFF-state output capacitance of the DPA. As the ACW increases

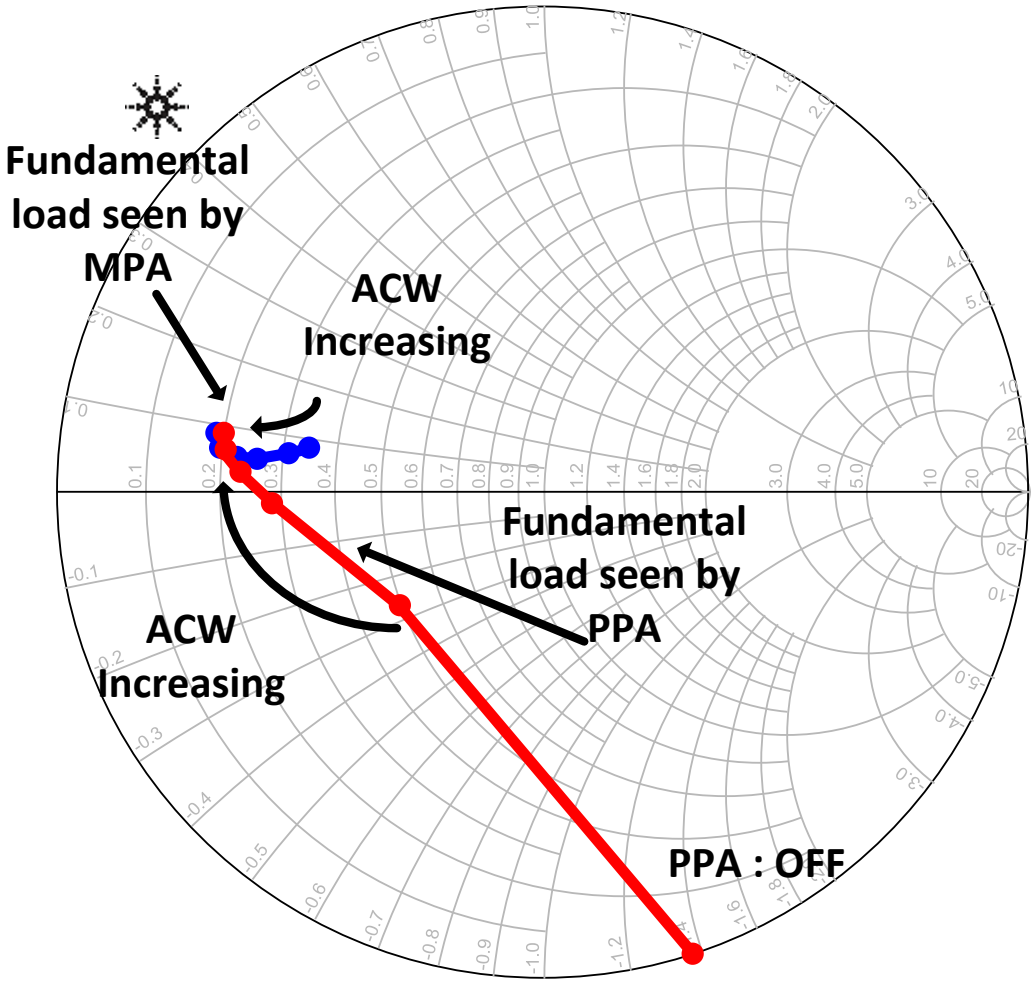


Figure 3.12. Simulated fundamental impedance seen by Main PA and Peaking PA with varying ACW

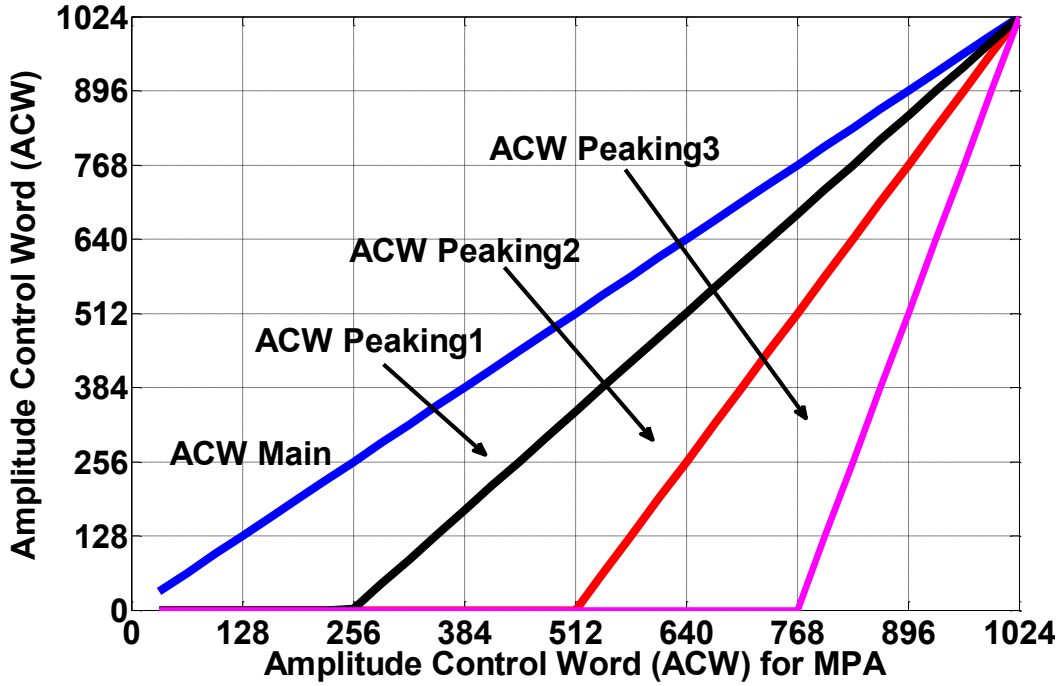


Figure 3.13. ACW profiles for MPA and PPA for various modulation profiles

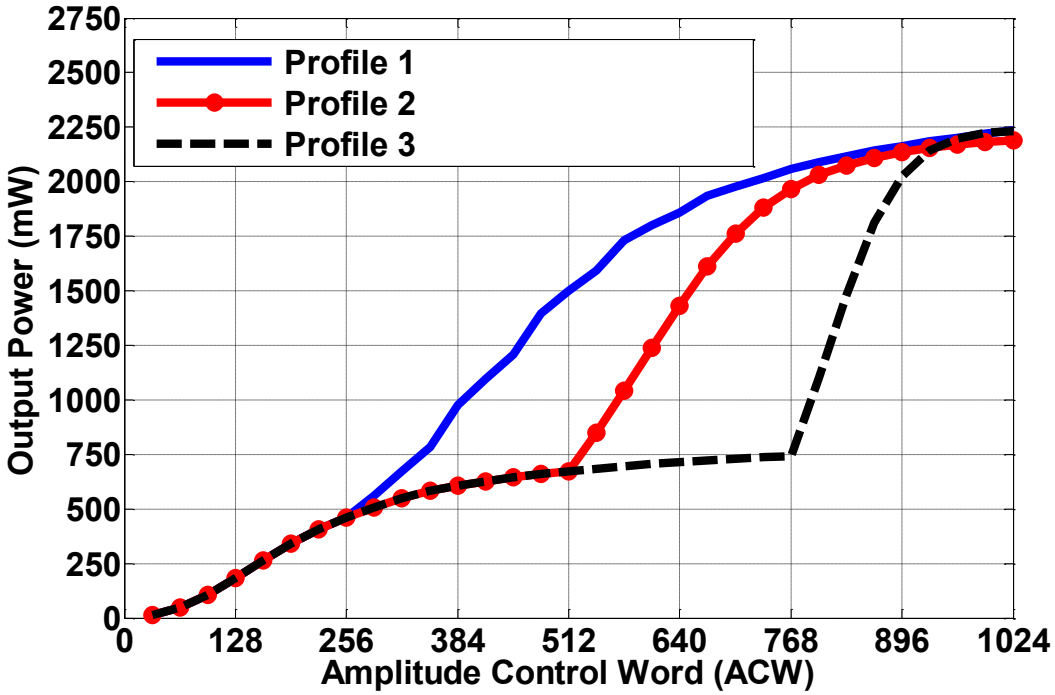


Figure 3.14. Simulated output power versus ACW for different profiles of load modulation

and reaches its peak, both MPA and PPA see an optimum impedance of (9 + j3 Ω).

### 3.2.4 Load Modulation Profiles

It is of interest to consider the possible trajectories of the PPA ACW in relation to the trajectory of the MPA ACW in order to optimize performance; with the flexible digital control of the DDPA, virtually any profile can be produced experimentally. Here, three profiles are considered as examples, shown in Figure 3.13. For each profile, the ACW for MPA varies from lowest to full-scale ACW. The PPA is made active at various points: 256 for profile 1, 512 for profile 2 and 768 for profile 3. Simulations are done to explore the dependence of efficiency vs output power for different trajectories.

Figure 3.14 shows the output power versus ACW for the different profiles of load

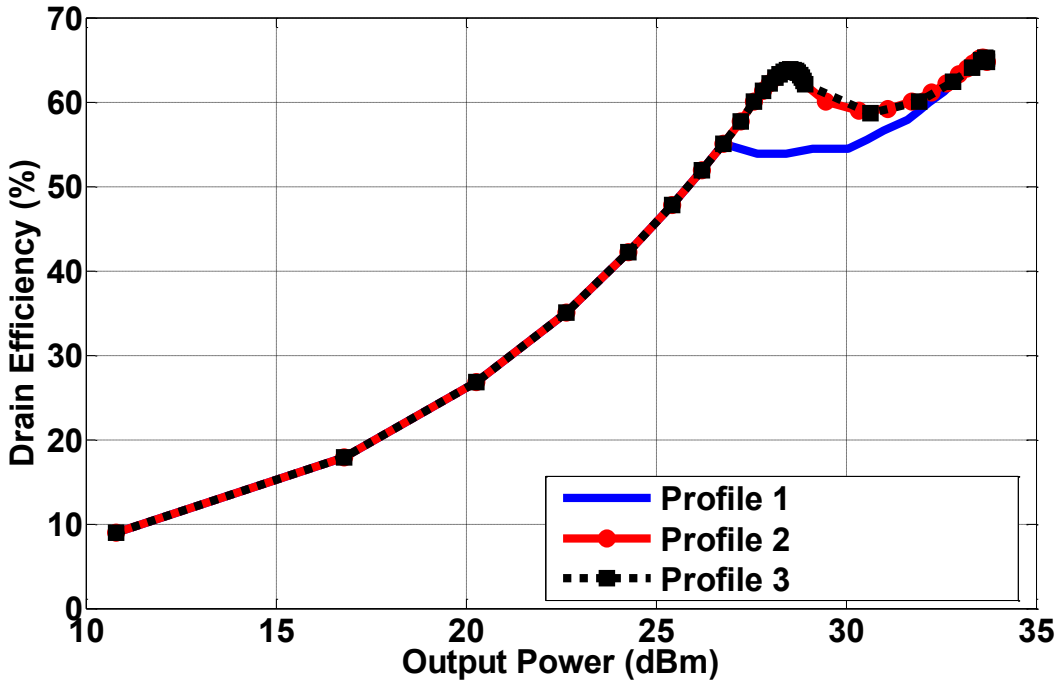


Figure 3.15. Simulated Drain Efficiency vs output power of DDPA for different profiles of load modulation

modulation. Profile 1 shows superior linearity of power vs ACW. This comes at the cost of efficiency, however. Figure 3.15 shows the drain efficiency versus output power for the different profiles. When the PPA is OFF, the MPA exhibits the same class-B behavior of efficiency vs output power in all cases. If the PPA turns on early, as in profile 1, the efficiency does not fully reach the peak achieved when the MPA is fully saturated. If the MPA is allowed to operate in very deep saturation before the PPA turns on, there is no improvement in back-off efficiency. However, there is a reduction in effective resolution of power control when the MPA is pushed into deep saturation. In profile 3, for example, the power increase from state 512 to 767 of the MPA is very small, as the MPA is in deep saturation. These states would not be of much use once predistortion is used for the MPA.

In addition to efficiency vs output power and effective resolution considerations, there are important considerations for the choice of ACW trajectory in regard to the AM-

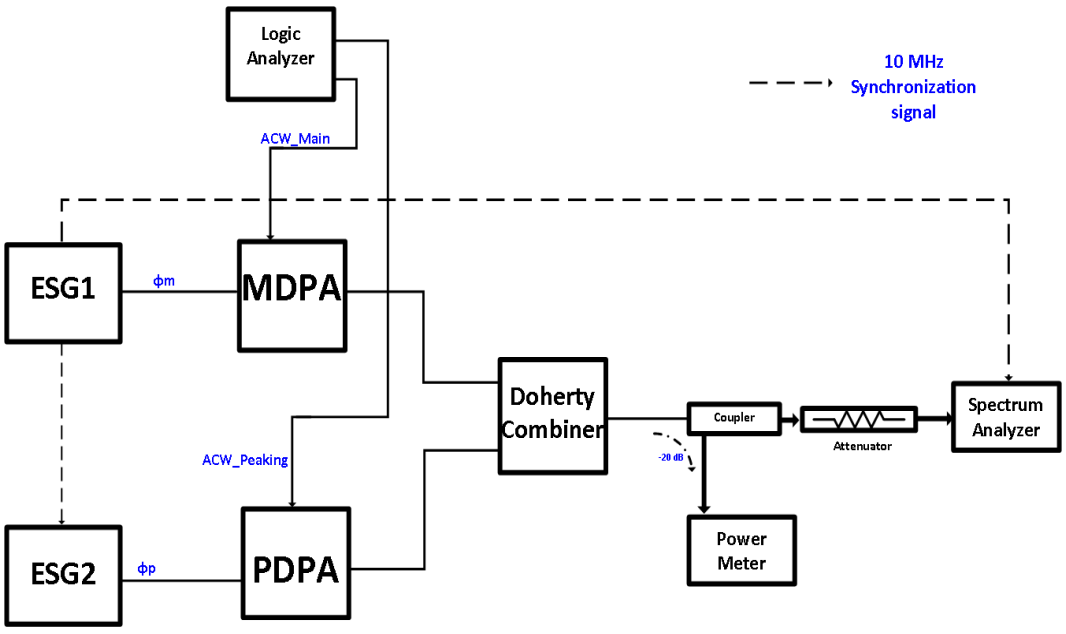


Figure 3.16. Measurement set up for DDPA

PM behavior of the output. It is desirable to pick a trajectory that minimizes the variations in phase vs ACW for both MPA and PPA in order to limit the bandwidth of the input phases that must be provided to the DDPA [16].

## 3.3 Measurement Results

### 3.3.1 Measurement setup

The PM (phase modulated) input centered at the RF frequency is fed from an Agilent ESG 4438C to the driver stages of both MDPA and PDPA. A 50 Ohm termination is provided on chip at the phase modulated RF input pad. The phase difference between these PM signals can be controlled using ESGs. The supply voltage used for drivers is 1.7 V. The supply voltage used for both MPA and PPA is 4.1 V.

The CMOS DPA used as MPA and PPA was implemented in 180 nm CMOS partially-depleted SOI technology with supply voltage 1.5 V. Body-contacted SOI were used. The technology offers 4 metal layers. Both DPAs were mounted on a PCB with Rogers 4003C substrate and wirebonded for appropriate connections, including 10 parallel amplitude control bits for each DPA.

Figure 3.16 shows the block diagram of the measurement set up. An Agilent Logic Analysis System 16901A was used to provide the input 10 bit words to both MPA and PPA. The pattern generator logic output levels are 0 V and 3.2 V, translated to 0 V and 1.6 V using resistive dividers on the PCB.

### 3.3.2 Continuous Wave Measurement Results

Figure 3.17 shows the output power versus ACW of the MPA, using the trajectory of Figure 3.8, when the ACW inputs are varied quasi-statically. Figure 3.18 shows, peak

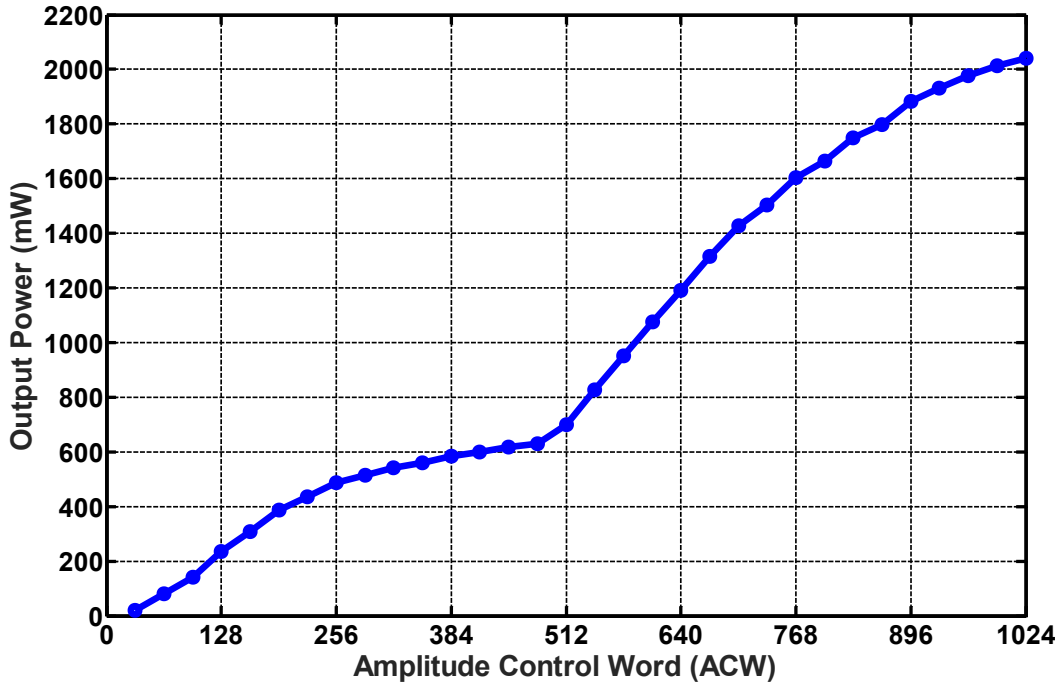


Figure 3.17. Measured output power versus ACW at 900 MHz

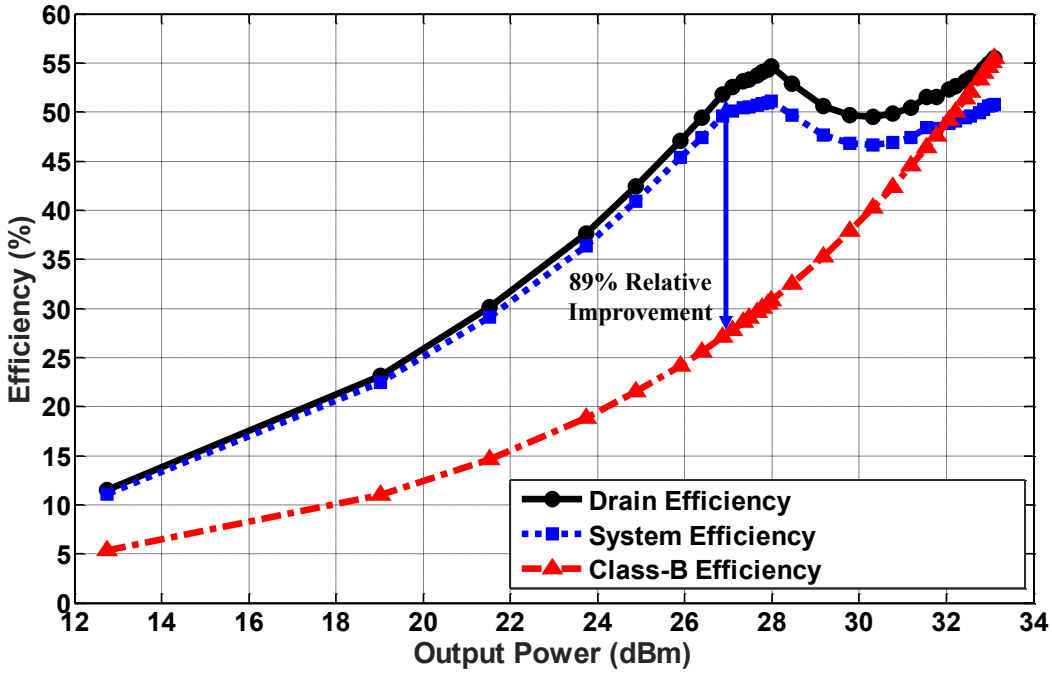


Figure 3.18. Measured efficiency versus output power at 900 MHz

power of greater than 2 W was obtained, with drain efficiency of 55.5%. The "system efficiency" is defined here as the RF fundamental output power divided by the dc power for digital logic on-chip, digital drivers on-chip and for the RF output stage; this was 50.8% at peak output power. A second efficiency peak occurs at output power of 28 dBm (at 5.1 dB back-off from the peak). The drain efficiency at this power was 54.6%. At 6 dB back-off the drain efficiency was 52.6% (which corresponds to 89% improvement relative to a normalized class-B PA efficiency roll-off). The system efficiency at 6-dB back-off was 50.1% (corresponding to improvement relative to class-B behavior of 97%; better numbers are measured than for drain efficiency since for the DDPA architecture, the driver stages are turned OFF with back-off).

In separate measurements, the ACW was varied dynamically following a linear ramp trajectory, with a dwell time of 1.1 μs at each input level. Figure 3.19 and Figure 3.20 show the resulting normalized AM-AM characteristics and AM-PM characteristics of the DDPA at 900 MHz. The AM-AM characteristics are in good agreement with the quasi-static measurements. The AM-PM is associated with changing output resistance and capacitance of both MDPA and PDPA.

### 3.3.3 Modulation signal Measurement

Modulation testing was done with two different signals. For a 5 MHz, single-carrier 16-QAM signal with PAPR of 6.6 dB, Figure 3.21 shows the output spectrum centered around 900 MHz. Figure 3.22 shows the IQ constellation of the demodulated signal. The EVM was measured to be 3.8%. The ACLR values were -38 dB and -38.1 dB on lower and higher sides of the band respectively, with the use of Digital Pre-Distortion (DPD). The average output power was 26.7 dBm with drain efficiency of 45.7%. Figure

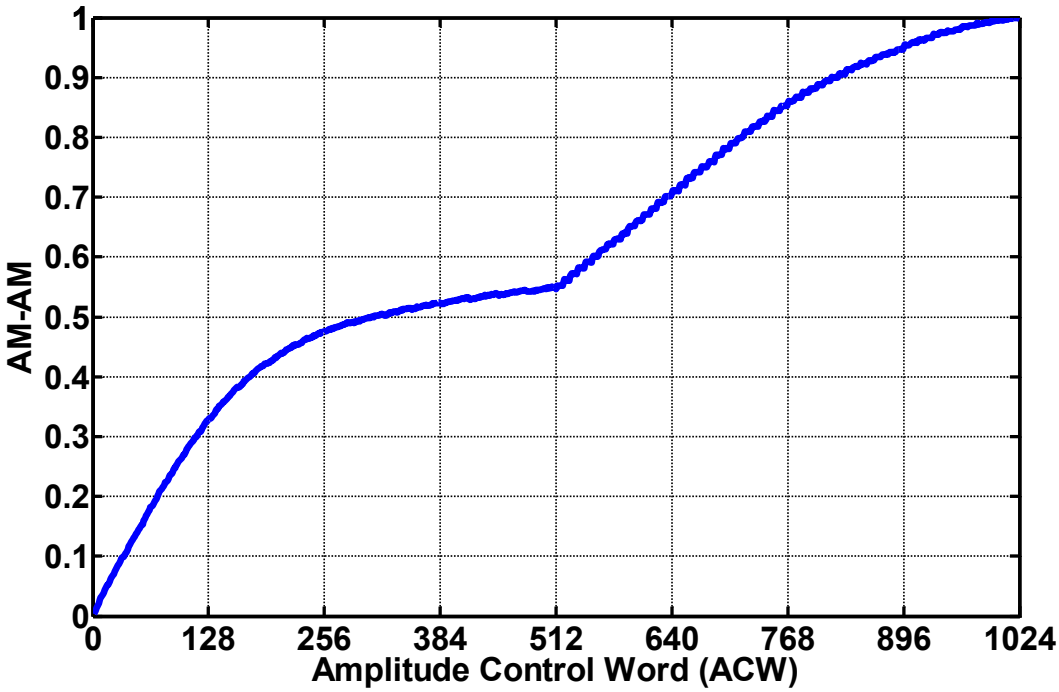


Figure 3.19. AM-AM of DDPA at 900 MHz

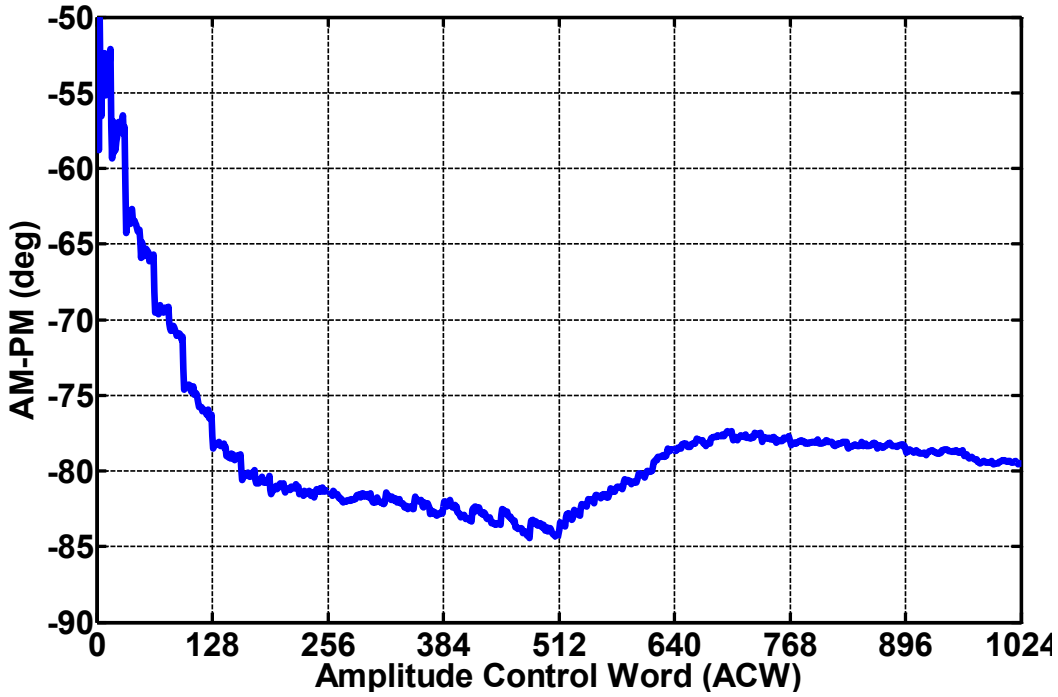


Figure 3.20. AM-PM of DDPA at 900 MHz

3.21 shows the ACLR1 and ACLR2 of the output spectrum. The estimated phase difference between MPA and PPA inputs is -95° (which was optimized to get best peak efficiency). In the measurement set up this was generated by setting phase delays in the two ESGs for the MPA and the PPA. This phase delay was varied in accordance with the instantaneous output power level for the modulated signal.

Memoryless, equation based, digital pre-distortion was performed to improve the output accuracy and meet the specifications for handset signals. The DDPA has two separate regions of operation, where only there MPA is active and where both MPA and PPA are active. The non-linear behavior of the AM-AM and AM-PM characteristics is different in these regions and cannot be modelled by a single equation. Accordingly, separate fitting equations were used for the two regions. Continuity of the modelled

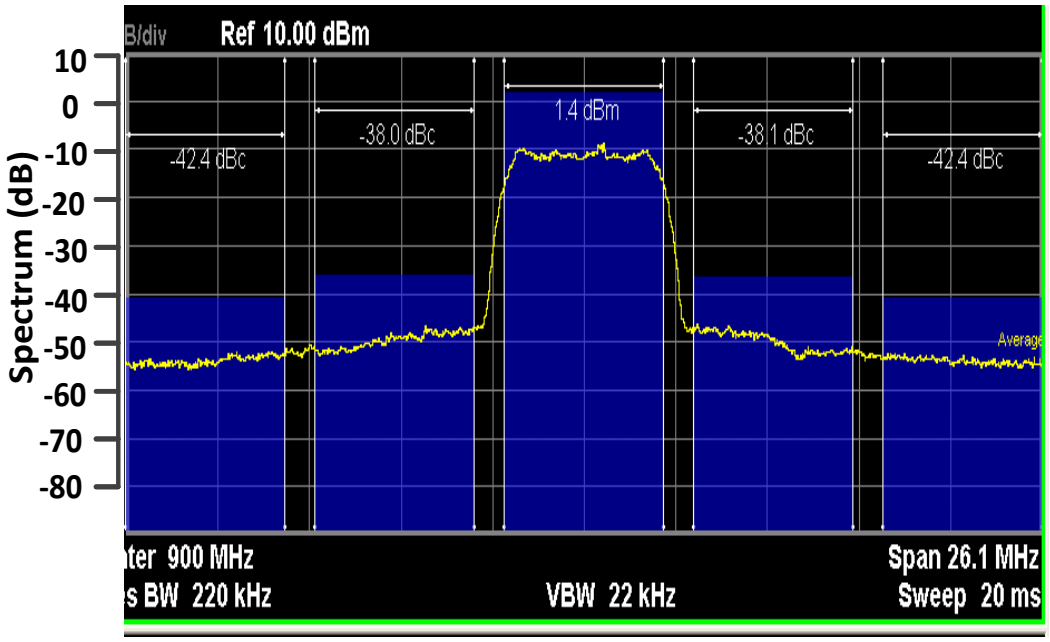


Figure 3.21. Measured DDPA output spectrum for 5 MHz single-carrier 16 QAM signal

equations was maintained, as needed to achieve low ACLR. Figure 3.23 shows the AM-AM behavior obtained from modulated signals, under pre-DPD and post-DPD conditions. The correction was done using an $8^{th}$ order polynomial for each region. Residual deviations from linear behavior show up in the AM-AM behavior at low input amplitudes in Figure 3.23, which in principle could be corrected by using a higher order fitting function. Figure 3.24 shows the AM-PM behavior under pre-DPD and post-DPD conditions. An exponential equation-based fitting was used for both regions, followed by a second level of polynomial-based correction. The spread in results for the AM-AM and AM-PM experimental curves can be attributed to memory effects. In this work, an important contribution to memory is likely to be the power supply decoupling for the

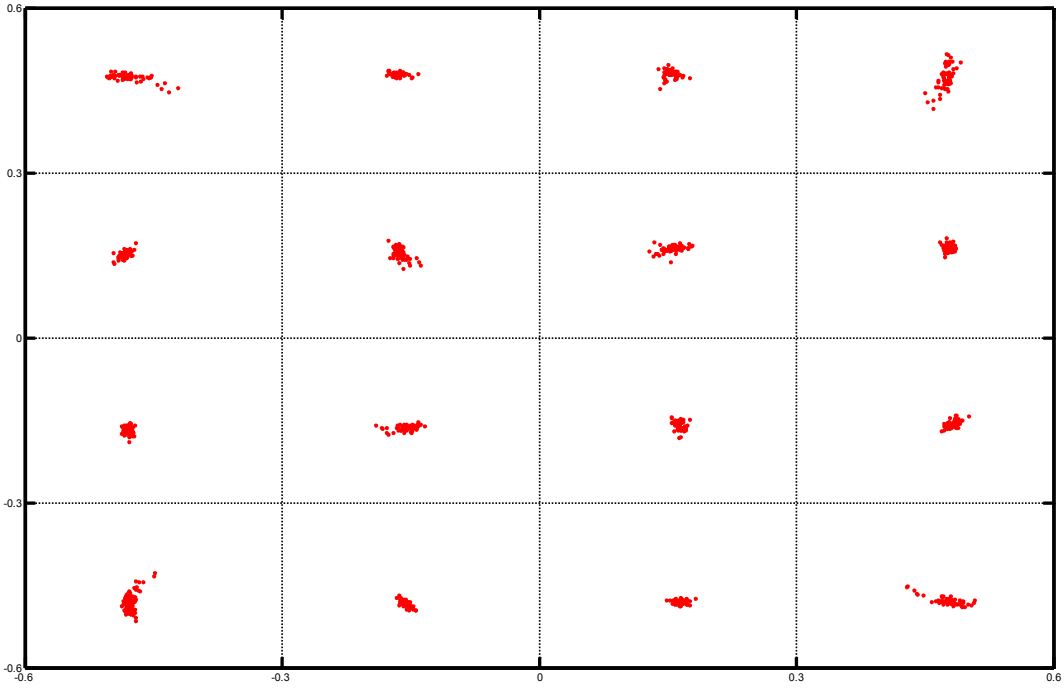


Figure 3.22. Measured IQ constellation of 16-QAM 5-MHz signal centered around 900 MHz (EVM = 3.8%)

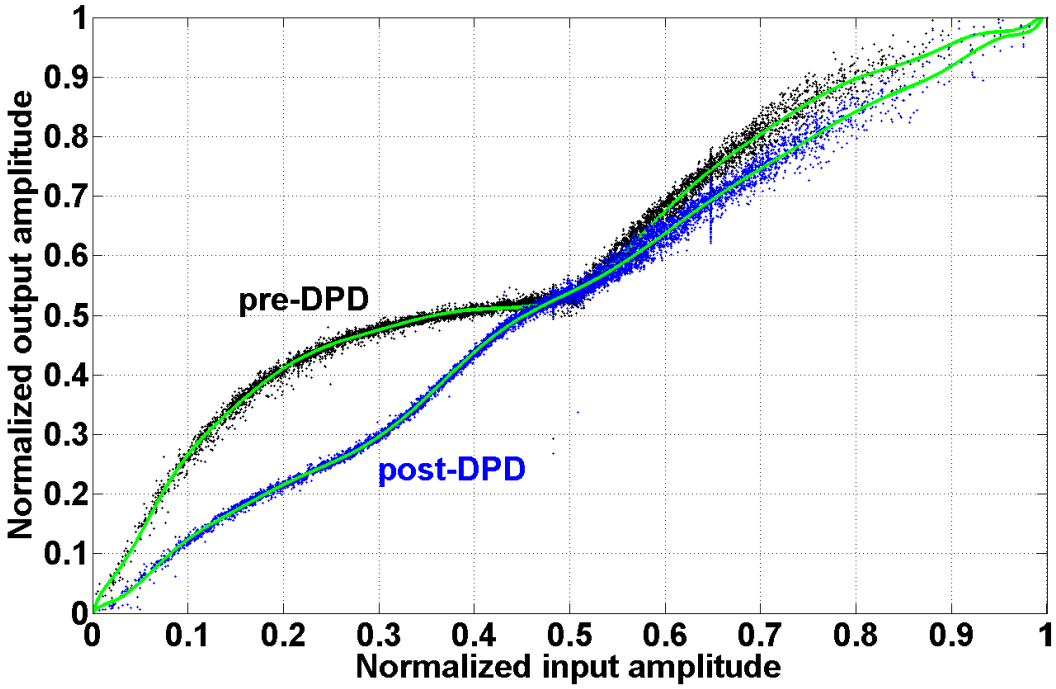


Figure 3.23. Measured AMAM behavior for 5 MHz 16-QAM signal : before and after equation based digital predistortion.

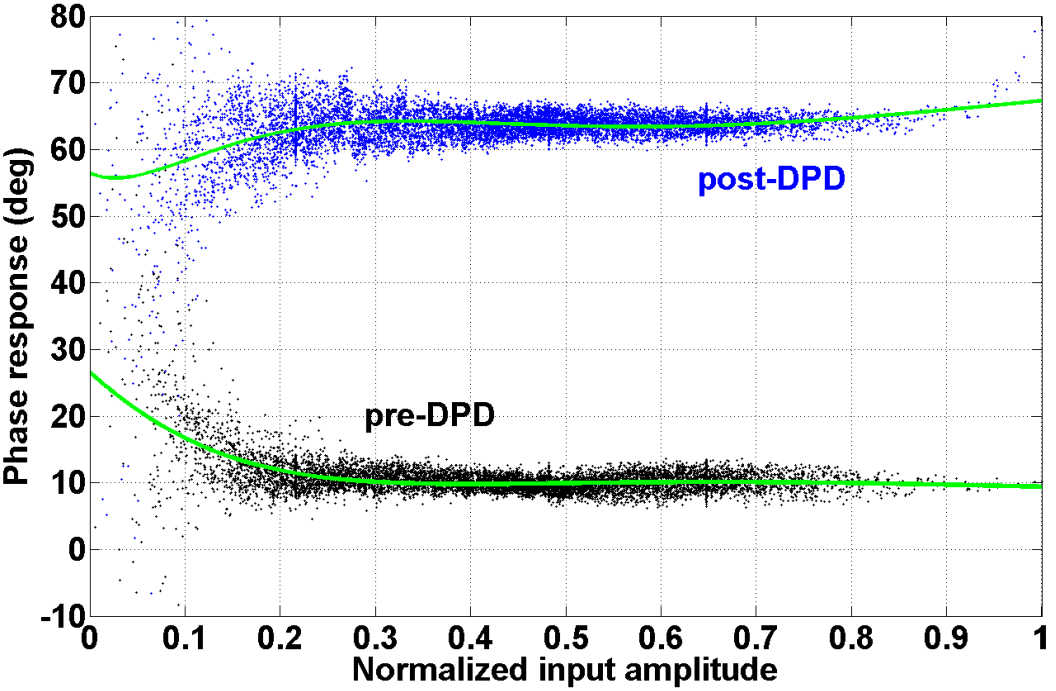


Figure 3.24. Measured AMPM behavior for 5 MHz 16-QAM signal : before and after equation based digital predistortion.

driver stages of the MPA and PPA. An improved supply decoupling (smaller bondwire and larger decoupling capacitor) would be needed to demonstrate larger bandwidth of modulated signals with memory-less DPD. Time alignment inaccuracies also show up as memory effect, and would need to be mitigated for use at larger bandwidth.

The DDPA was also tested with a 5 MHz 64-QAM OFDM signal centered at 900 MHz, whose PAPR was 7.4 dB. The output power was 25.7 dBm with a drain efficiency of 45.5%. Figure 3.25 shows the output spectrum. The normalized mean square error for OFDM signal was 4.1%. The ACLR values are 35.9 dB and 37 dB on lower and upper sides of the band. Figure 3.26 shows the far out spectra of DDPA with sampling frequency of 45 MHz. Clock images are visible at 45MHz offsets; these are lower than 33 dBc compared to signal.

The measured characteristics of the DDPA are compared in Table I with those of other reported amplifiers, including CMOS-based Doherty amplifiers with both analog and digital architectures. A Doherty power amplifier implemented in III-V technology for handset applications and a CMOS envelope tracking (ET) power amplifier are also shown for comparison.

Modulated RF signals corresponding to 16-QAM and 64-QAM OFDM were applied to the DDPA for measurement. The IQ data was transformed into AM and PM signals to feed the polar DDPA. As for CW measurements, the 20-bit digital AM signals were provided by the Agilent Logic Analyzer 16901A and the phase modulated RF signals came from Agilent ESGs. The data was sampled at 45 MHz. Accurate time alignment between different inputs is needed to achieve good modulation accuracy. Separate time-alignment delays were used for the two unit amplifiers, to compensate for

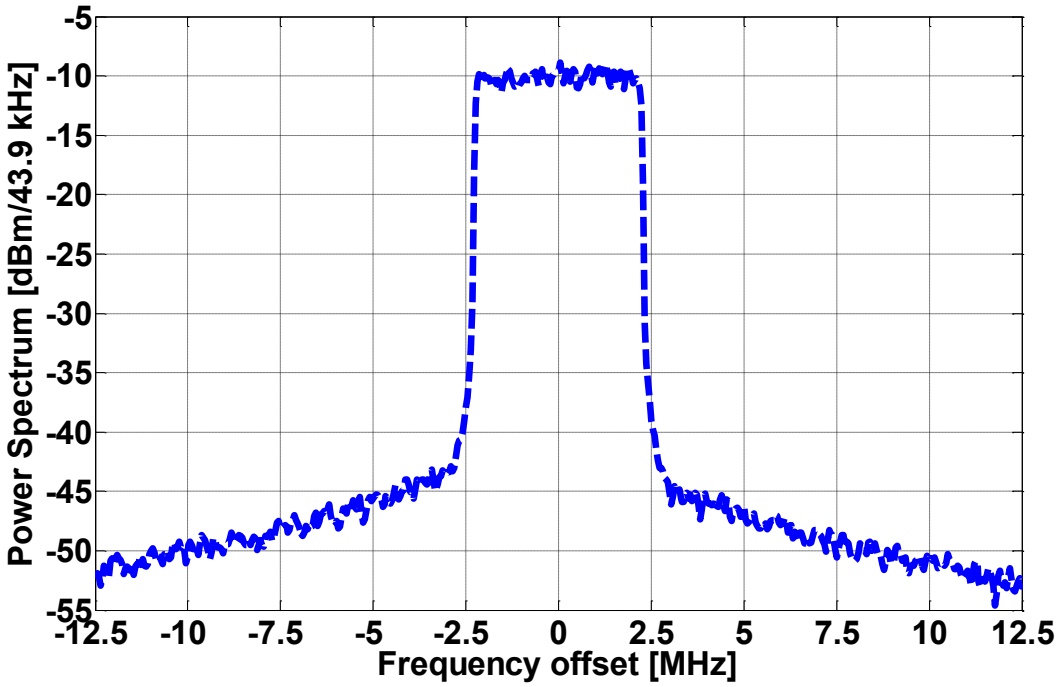


Figure 3.25. Measured DDPA output spectrum for 5 MHz OFDM 64-QAM signal

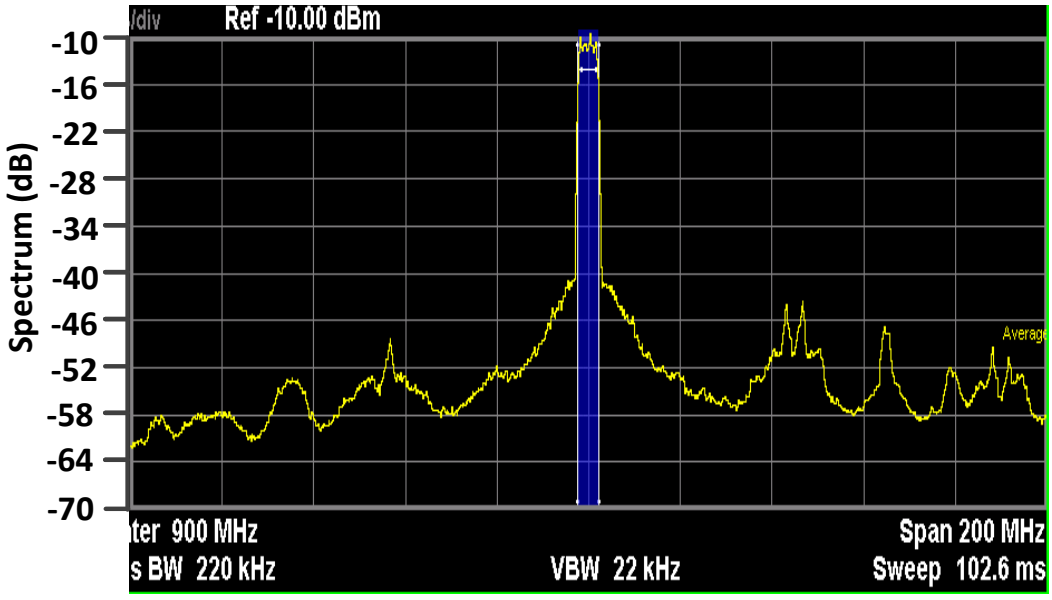


Figure 3.26. Measured spectrum of CMOS DDPA DPA output with sampling rate of 45MS/s, shown over a wide spectral range.

different interconnect delays. Sub-sample level time-alignment was performed and alignment accuracy of $1/10^{th}$ of a sample was achieved (limited by the measurement set up).

## 3.4 Circuit Limitations and Future Prospects

One of the challenges in a Doherty amplifier implementation is the matching bandwidth, particularly for handset-like applications where area is at a premium. When transmission lines are implemented using their lumped element equivalents for impedance inverters and matching networks, bandwidth limitations are generally experienced [15].

Figure 3.27 shows the simulated and measured frequency response of the DDPA at peak and at back off. At back off, when only the MPA is active, the DDPA has 1-dB power bandwidth of 300 MHz (fractional bandwidth of 40%). This bandwidth is governed by the impedance transformation from 50 Ω load to 17 + j4 Ω. At peak, the 1-dB power bandwidth is around 75 MHz, which is relatively narrow (and has dependence opposite to that of conventional Doherty amplifiers, for which bandwidth at peak power is broad because the λ/4 line is not doing any impedance inversion). To understand the bandwidth of the proposed DDPA, output power simulations were done at peak power from both the MPA and the PPA as a function of frequency (Figure 3.28). The output power of the PPA is relatively constrained in bandwidth, which can be traced to the lumped element implementation of the offset line. Alternative impedance matching networks can be expected to alleviate this constraint.

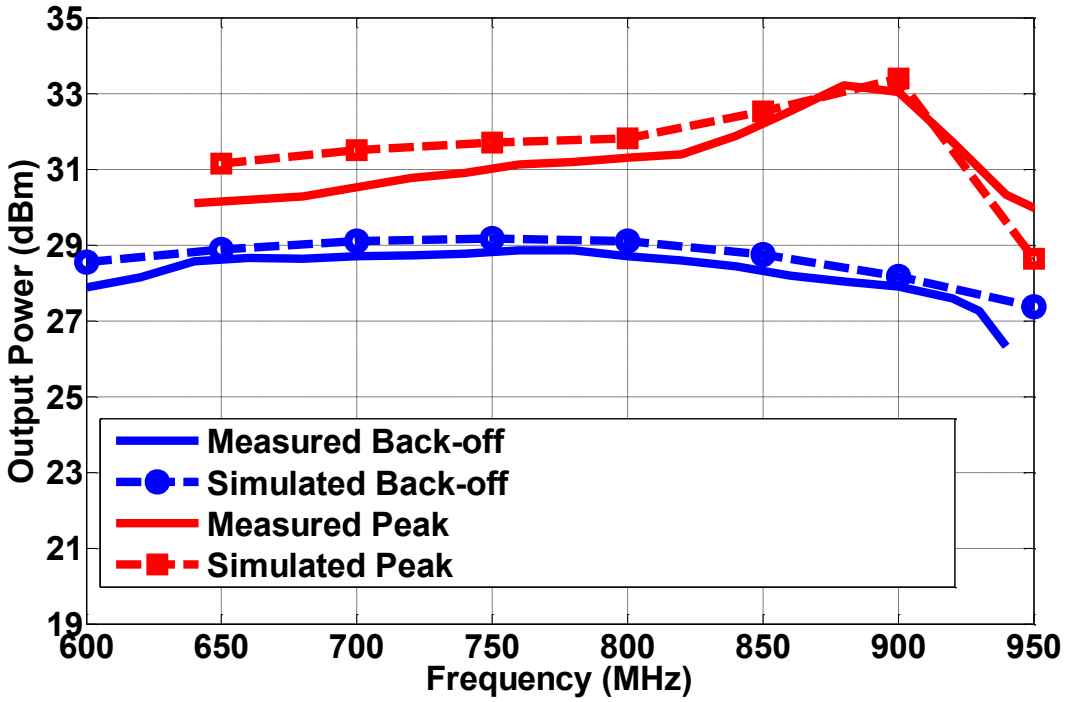


Figure 3.27. Measured and simulated output power of DDPA at peak and back-off ACW vs frequency

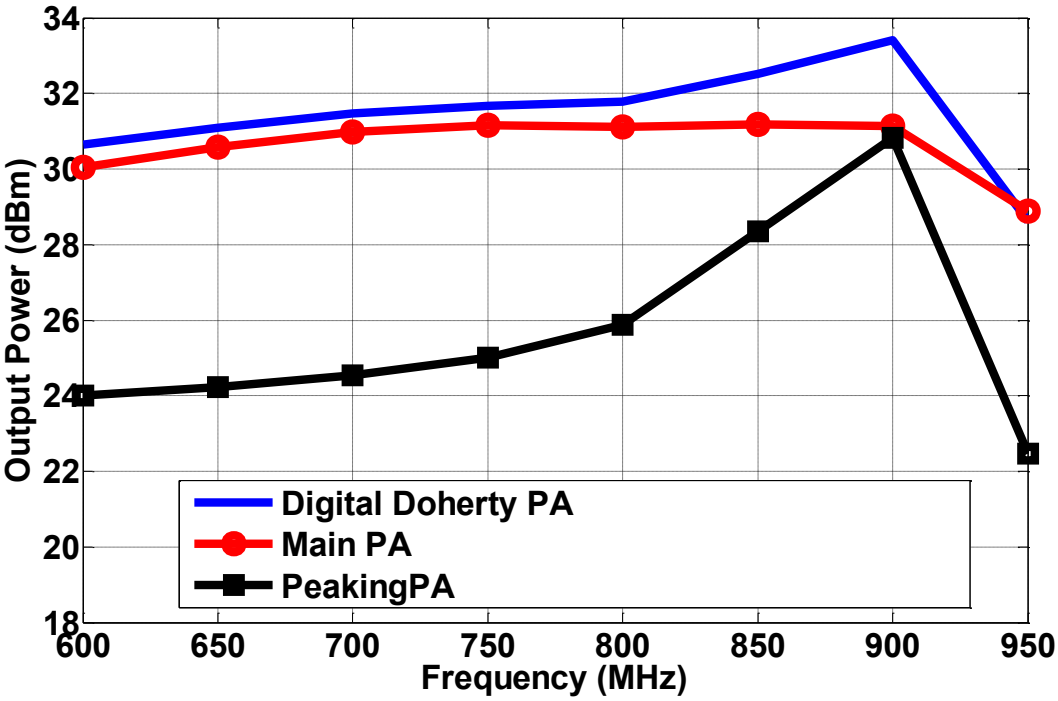


Figure 3.28. Simulated output power of DDPA, MPA and PPA at peak ACW vs frequency

Other challenges for digitally-controlled power amplifiers are related to quantization noise and to frequency replicas from the digital clock used. Figure 3.26 shows the measured output frequency spectrum over a wide spectral range, in which the clock images and quantization noise from DDPA can be seen. The spurious signals make it difficult to directly use the amplifier for frequency-division duplex (FDD) transceivers because of possible introduction of noise into the receive band. Clock images can be pushed far away from the carrier by increasing the sampling frequency of input data, either as supplied from off chip, or by oversampling and filtering on-chip [28]. This also reduces quantization noise since over-sampling ratio is increased. In the present system there are limitations for very high sampling rates by supply decoupling for driver amplifiers. Quantization noise can also be reduced by with higher bit resolution, and for specific frequency ranges, by DSP filtering methods [29].

## 3.5 Conclusion

A digitally-controlled Doherty polar power amplifier (DDPA) has been demonstrated in CMOS SOI technology. Stacked-FET technique has been used to achieve peak output power in the range of several Watts, as required for various mobile communication applications. The strong, controllable turn-ON/turn-OFF characteristics of DPA has been exploited to achieve a strong efficiency peaking at back-off power. The input of the DDPA has a dual-phase drives and shows no input impedance variation with power back-off.

The DDPA yielded peak output power of 33.1 dBm at 900 MHz with drain efficiency of 55.5% and system efficiency of 50.8%. To the authors' best knowledge, this

TABLE I

COMPARISON TABLE OF DDPA PERFORMANCE WITH PREVIOUSLY REPORTED WORKS

| | *Technology* | *Technique for BO efficiency improvement* | *Freq (GHz)* | *Peak Pout (dBm)* | *Efficiency @ Peak Pout (%)* | *Efficiency at 6-dB back-off (%)* | *Average Pout (dBm)* | *Signal/BW (MHz)/ PAPR(dB)* | *Average Efficiency (%)* | *EVM (%)* | *ACLR (dB)* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| [30] | 180 nm CMOS | ET | 1.85 | 30.2 | 48 (PAE) | 45.6$^{\zeta}$ | 26 | 16QAM/ 10 / 7.5 | 34.1 (PAE) | 2.8 | -34.2 |
| [31] | 65 nm CMOS | Doherty | 3.71 | 26.7 | 40.2 (DE) | 36.2 | 20.8 | 16QAM/ 1 / 5.4 | 28.8 (DE) | 6.3 | -21 |
| [14] | 2 um InGaAs/GaAs | Doherty | 1.88 | 33 | 51 (PAE) | 45$^{\zeta}$ | 26 | 16QAM/ 8.75 / 9.54 | 40.2 (PAE) | 3 | N/A |
| [32] | 180 nm CMOS | Doherty | 0.88 | 32$^{\zeta}$ | 56$^{\zeta}$ | 47.9$^{\zeta}$ | 27 | 16QAM/ 10 / 7.5 | 47.4 (PAE) | 3.85 | -33 |
| [33] | 180 nm CMOS | Doherty | 0.847 | 31.2 | 57.8 | 43.9$^{\zeta}$ | 25.2 | 3G LTE/ 10 / 7.6 | 43.6 (PAE) | N/A | -34 |
| [34] | 180 nm CMOS SOI | Doherty | 1.85 | 30.7 | 44.4 | 30.2$^{\zeta}$ | 27.2 | 16QAM/ 10 / 7.5 | 37.7 (PAE) | 4.78 | -30 |
| This Work | 180 nm CMOS SOI | Doherty | 0.9 | 33.1 | 55.5 (DE) 50.7 (SE) | 52.4 (DE) 49.9 (SE) | 26.7 | 16QAM/ 5 /6.6 | 45.7 (DE) | 3.8 | -38 |
| | | | | | | | 25.7 | 64QAM OFDM/5/ 7.4 | 45.5 (DE) | 4.1 (NRMSE) | -35.9 |

$^{\zeta}$estimated from plots

SE – System Efficiency

is the highest peak output power yet reported for Doherty PAs implemented in CMOS technology. At 6-dB back-off DDPA had drain efficiency of 52.6% (system efficiency of 49.9%), also the highest reported for CMOS Doherty PAs. For modulated signal testing, 5 MHz signals of single-carrier 16-QAM and OFDM 64-QAM have been used. The output power was 26.7 dBm and 25.7 dBm with drain efficiency of 45.7% and 45.5% respectively. The output signals had ACLR of better than -38 dBc and -35.9 dBc and EVM of 3.8% and Normalized Root Mean Squared Error (NRMSE) of 4.1% respectively. A memory-less, look-up table (LUT) based pre-distortion was used to achieve good linearity.

Results indicate that CMOS DDPAs are promising components for mobile wireless applications.

## 3.6 Acknowledgement

Chapter 3 is mostly a reprint of the material as it appears in “High Power Digital Doherty Polar Power Amplifier in CMOS SOI”, V. Diddi, H. Gheidi, J. Buckwalter and P. Asbeck, submitted for publication in IEEE Transactions on Microwave Theory and Techniques and the material in “High-power, high-efficiency digital polar Doherty power amplifier for cellular applications in SOI CMOS”, V. Diddi, H. Gheidi, J. Buckwalter and P. Asbeck, IEEE PAWR 2016. The author of this dissertation was the primary investigator and primary author for this material.

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# Chapter 4

# Broadband Digitally Modulated Polar Power Amplifier using CMOS SOI and Gallium Nitride Combination

## 4.1 Introduction

As described in Chapter 1, there is currently significant research interest in developing digitally intensive power amplifiers (PAs) for various applications. Digitally-controlled amplifiers are well-suited to multimode operation where output power can be controlled using digital input words. They are also favorable for increased levels of system integration. Digitally-controlled PAs (DPAs) such as RFDACs [1-5] have no inherent frequency sensitive components except for output impedance matching networks, thus a tunable matching/switchable matching network can allow PA operation over a wide range of frequencies.

Digital control can be implemented straightforwardly in silicon CMOS technologies which are well-suited to digital logic, as detailed in Chapters 2 and 3.

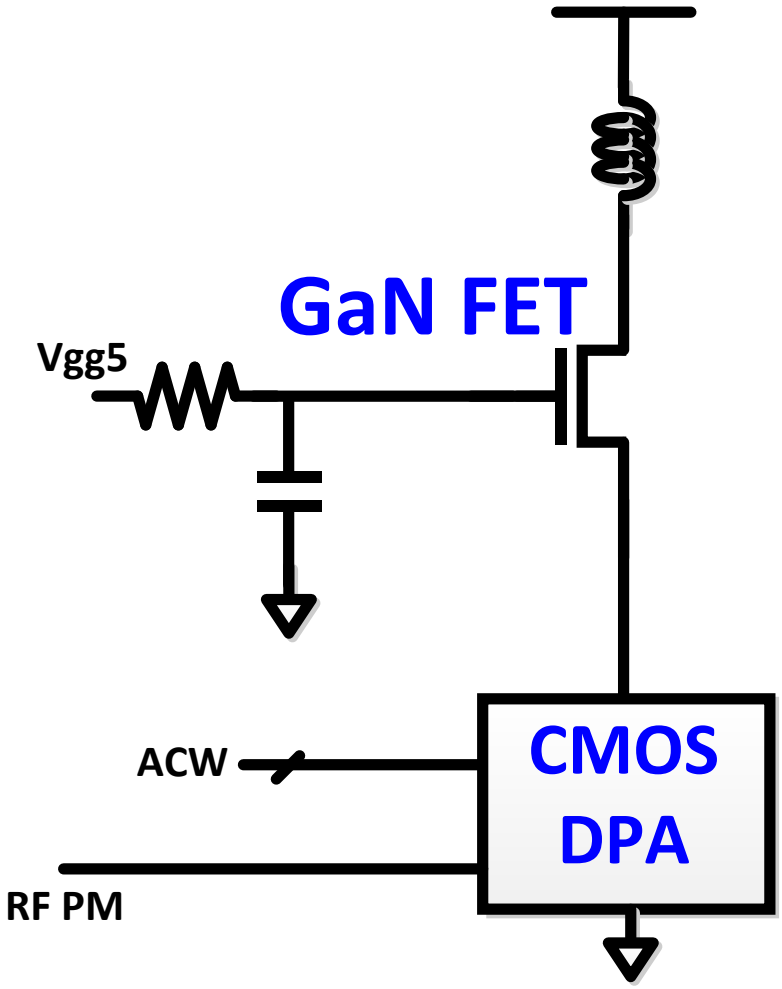


Figure 4.1. Schematic of CMOS/GaN PA

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Unfortunately, CMOS technology is not optimal for high power and high voltage PAs, due to relatively low voltage handling capability and high parasitic capacitances and resistances which limit output power and efficiency. One of the techniques that have been shown to be successful in overcoming this breakdown limitation in CMOS technologies is FET-stacking [5-6]. By stacking CMOS FETs, the output power of digitally-controlled CMOS PAs has reached the watt-level. Applications such as micro-basestations and hand-held peer-to-peer communication systems often require higher power, however. This chapter reports a combination of CMOS and GaN that can achieve higher power levels, while retaining straightforward digital control. The work can be viewed as an extension of the FET-stacking concept, from the use of only CMOS FETs to a combination of CMOS and GaN FETs.

One of the critical aspects in designing a broadband high power amplifier is the bandwidth limitation of impedance matching networks. This can appear both at the final stage and at interstage impedance matching networks. Implementing broadband multi-stage networks leads to significant losses, degrading the PA efficiency. In this work all impedance matching networks are eliminated; a CMOS DPA drives a common-gate-like GaN FET, which in turn directly drives a 50 Ω output load.

## 4.2 Circuit Design

### 4.2.1 Architecture

The CMOS-GaN power DAC circuit architecture is shown in Figure 4.1. The inputs to the CMOS DPA consist of 10 bit digital words to control the output amplitude, as well as a constant amplitude RF signal at the carrier frequency containing the desired

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phase modulation. The output of the DPA drives the source of GaN FET. A large capacitor of 180 pF is used to provide RF ground at the gate of GaN FET. An adjustable DC gate bias is connected to the gate of GaN FET through a 200 Ω resistor (this prevents significant de-biasing of the device while allowing small gate current to flow). The drain of the GaN FET is connected to a $V_{dd}$ supply and to a 50 ohm RF load through a bias-T on the associated printed circuit board. A large choke inductor of 425 nH (on the PCB) and a DC block (off the PCB) are used to build a bias-T, which operates to below 0.5 GHz.

An important design consideration for the CMOS DPA is that it must be capable of providing high enough current and voltage swings. The required current corresponds to the output current of the composite amplifier, together with the current needed to charge the capacitance at the intermediate node between the CMOS and GaN. The voltage required depends on the characteristics of the GaN FET used. For representative GaN threshold voltages of the order of -3V and forward gate-source voltages of 2V for full current operation, voltage swings in the range 6 - 8 V must be supported by the CMOS DPA. This requires specialized CMOS DPA design. Generally in past work, CMOS transistors designed to withstand high voltages (LDMOS and EDMOS) have been used to drive GaN devices [8-10].

## 4.2.2 DC Loadline Analysis

The CMOS DPA operates by alternately turning ON and OFF an appropriate number of amplifier cells at the RF frequency. When the CMOS is used in combination with the GaN FET, the overall ON current is determined, in low frequency operation and

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for high $V_{dd}$, by the relationship between the Id-Vd curves provided by the CMOS and the Id-Vgs curves provided by the GaN FET, as pictured in Figure 4.2. As shown in the figure, the Id-Vgs curve provided by the GaN FET is relatively linear for Vgs>Vt. The Id-Vds curves of the CMOS DPA (depicted for different values of ACW) exhibit significant nonlinearity. For low values of ACW, the Id-Vds curve has strong saturation, and the CMOS DPA acts approximately as an ACW-controlled current source. For high values of ACW, the Id-Vds curves are linear, and the DPA acts as a variable resistor.

For high values of the ACW, the relationship between output power and ACW can be approximately written assuming linear Id-Vd curves as

$$I_d = \left[\frac{g_m}{1 + g_m * R_{on}}\right] * (V_{gg} + |V_p|) \quad (1)$$

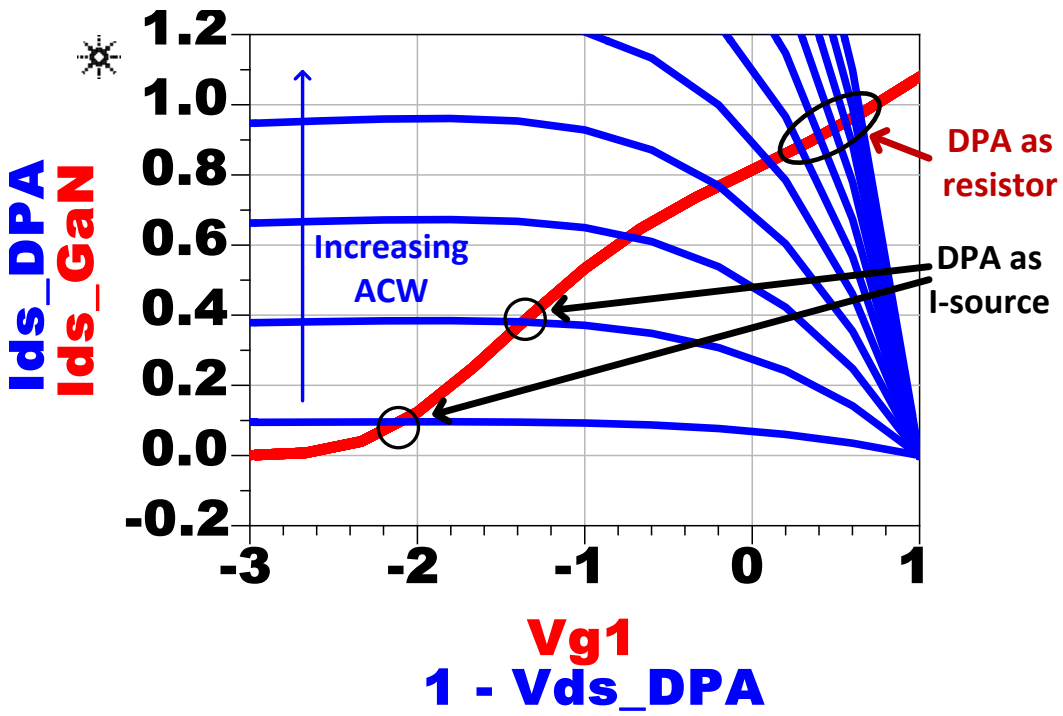


Figure 4.2. Load line analysis, showing relationship between GaN FET ON current and CMOS DPA characteristics.

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where $R_{on}$ is the on-resistance of the CMOS DPA, gm is transconductance of the GaN FET, $V_{gg}$ is the gate biasing voltage for GaN FET and $V_p$ is the threshold voltage of GaN FET. To a better approximation, for the DPA at very large ACW

$$R_{on} = {\beta}/{ACW} \tag{2}$$

where β is a proportionality factor, assuming the DPA is operating in triode region. Assuming normalized output voltage has the same behaviour as the output current we infer that

$$\frac{v_{out}}{v_{out,max}} = \frac{ACW}{ACW_{max}} \left[\frac{ACW_{max} + \beta * g_m}{ACW + \beta * g_m}\right] \tag{2}$$

The equation illustrates that as ACW approaches $ACW_{max}$ the output voltage

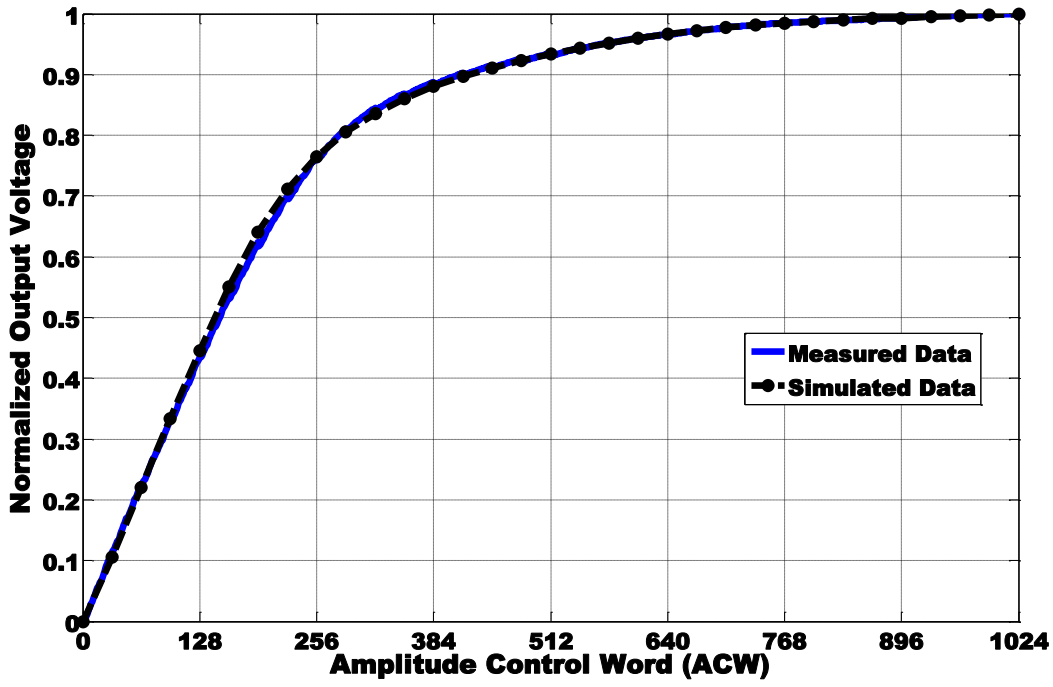


Figure 4.3. Measured and simulated relationship between output voltage amplitude and digital input word.

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saturates, and the onset of saturation is affected by the GaN FET $g_m$. In this regime the Id-Vd behaviour of the DPA looks like that of a digitally controlled resistor. Conversely, for low values of the ACW, the DPA begins to approximate a current source. This leads to a linear variation of overall current vs ACW. Figure 4.3 shows a comparison plot of measured and simulated normalized output, in which the linear and saturation regions are apparent. Detailed simulations provide very good agreement with experiment. It is important to note that, by the mechanisms just described, the impedance seen from the output of the DPA changes as a function of ACW.

The maximum output power of the CMOS-GaN combination is limited both by the ACW-governed output current discussed above, and also by the value of $V_{dd}$. For low values of $V_{dd}$ and high output currents, the current decreases as the GaN FET enters its triode regime; its $g_m$ decreases and the ON current saturates at near $V_{dd}/R_L$.

The sizing of the GaN FET with respect to the DPA is critical to achieve best performance. When overdriven, the maximum current carried by both GaN FET and CMOS DPA should be equal. Otherwise one of the elements will limit current at the peak power while the other is underutilized (thus providing higher capacitance than is necessary). To utilize the DPA to attain its highest output power as well as efficiency, the fundamental load seen should be close to 8 Ω [5]. The load seen by the DPA is predominantly determined by the large-signal transconductance of the GaN FET. The size and biasing of the GaN FET should be able to provide appropriate transconductance at the peak output power carrying similar current that of DPA. In our design the simulation suggests that the fundamental load is close to 10.5 Ω. A larger GaN FET would bring this closer to optimum value. The downside of such a FET would be

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increased gate-source capacitance, which might lead to degradation in frequency response of the PA. Using more advanced technology node for GaN FET can give better transconductance per width of the device. This would meet the fundamental load impedance requirement and potentially improve the frequency response at the same time.

### 4.2.3 AC Analysis and Circuit Parasitics

As for any cascode amplifier, the pole associated with the output node capacitance and the 50 ohm load resistance (pole $p_1$), and the pole associated with the node intermediate between the CMOS DPA and the GaN FET (pole $p_2$) are important determinants of the frequency response. For pole $p_1$, the equivalent parasitic capacitance at the drain of the GaN FET ($C_{d,gan}$) together with the 50 Ω load leads to an RC rolloff with corresponding 3dB bandwidth estimated to be above 2.5 GHz. For pole $p_2$, the overall capacitance associated with the floating intermediate node is large (of order 15 pF) but the associated impedance to ground is small (related to 1/gm of the GaN FET in parallel with the ACW-dependent output impedance of the DPA), leading to an

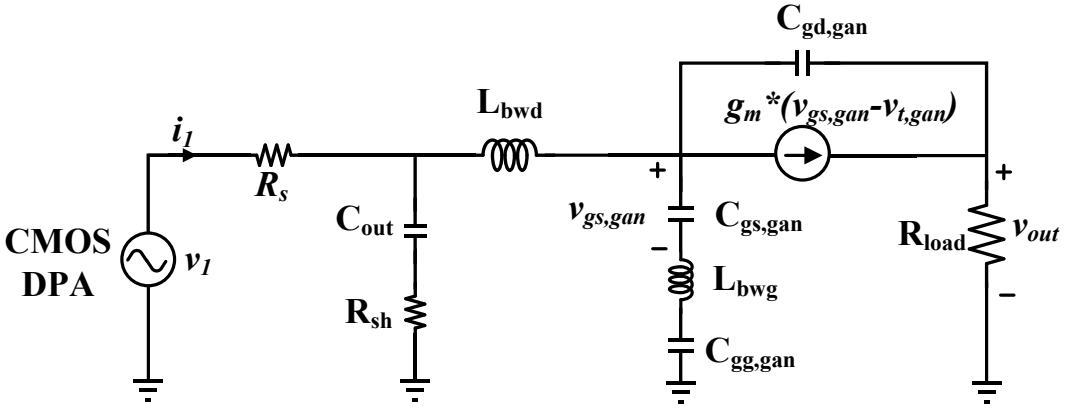


Figure 4.4. Small signal equivalent model for the CMOS-GaN DPA.

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associated 3 dB bandwidth above 5 GHz at peak ACW. This pole position changes with ACW, however, and is reduced to below 2 GHz for the lowest output powers.

In our experimental amplifiers, additional parasitic elements at the intrinsic node between CMOS DPA drain and GaN FET source also have an important influence. Bondwires are used to connect the DPA with the GaN FET, adding significant parasitic inductances. The DPA output capacitance ($C_{out}$) is measured to be 7 pF. The bondwires from CMOS DPA to GaN FET are modelled to have inductance $L_{bwd}$ of 1.1 nH. A wirebondable capacitor ($C_{gg,gan}$) of 180 pF is used at the GaN FET gate. The inductance of the gate bondwire ($L_{bwg}$) is modelled to be 0.2 nH.

Figure 4.4 shows the small-signal equivalent model for the circuit. The overdriven and saturated CMOS DPA acts as voltage source providing current $i_1$ with series resistance of $R_s$ (0.5 Ω). When backed-off, the DPA instead acts largely as a current source [6], increasing the value of $R_s$, which drives various parasitic elements along with the GaN FET. The shunt resistance $R_{sh}$ (6.5 Ω) models the finite quality factor of parasitic output capacitance $C_{out}$.

The transfer-function from $i_1$ to $v_{gs,gan}$ is

$$\frac{v_{gs,gan}}{i_1} = \left[\frac{1}{j\omega C_{gs,gan}}\right]\left[\frac{Z_4}{Z_3+Z_4}\right]\left[\frac{Z_1(Z_3+Z_4)}{(Z_1+Z_2)(Z_3+Z_4)+Z_3Z_4}\right] \tag{4}$$

where

$$Z_1 = R_{sh} + \left(\frac{1}{j\omega C_{out}}\right) \tag{5}$$

$$Z_2 = j\omega L_{bwd} \tag{6}$$

$$Z_3 = j\omega L_{bwg} + \left(\frac{1}{j\omega C_{gs,gan}}\right) \tag{7}$$

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$$Z_4 = \frac{1}{g_{m,gan}} \tag{8}$$

CMOS DPA output voltage and current are related by equation

$$\frac{v_1}{i_1} = R_s + Z_1 \left[\frac{Z_2(Z_3+Z_4)+Z_3Z_4}{(Z_1+Z_2)(Z_3+Z_4)+Z_3Z_4}\right] \tag{9}$$

where $R_s$ is on resistance of CMOS DPA.

From the equivalent model, the pole locations of the network can be derived. The dominant pole is significantly affected by $L_{bwd}$ and by $C_{gs,gan}$. The simulations indicate that by reducing these parasitic elements, the dominant pole will be pushed out, leading to enhanced bandwidth.

This simple model predicts frequency behavior which is similar to that obtained from FET model simulation as well as measurement. Figure 4.5 shows plots comparing

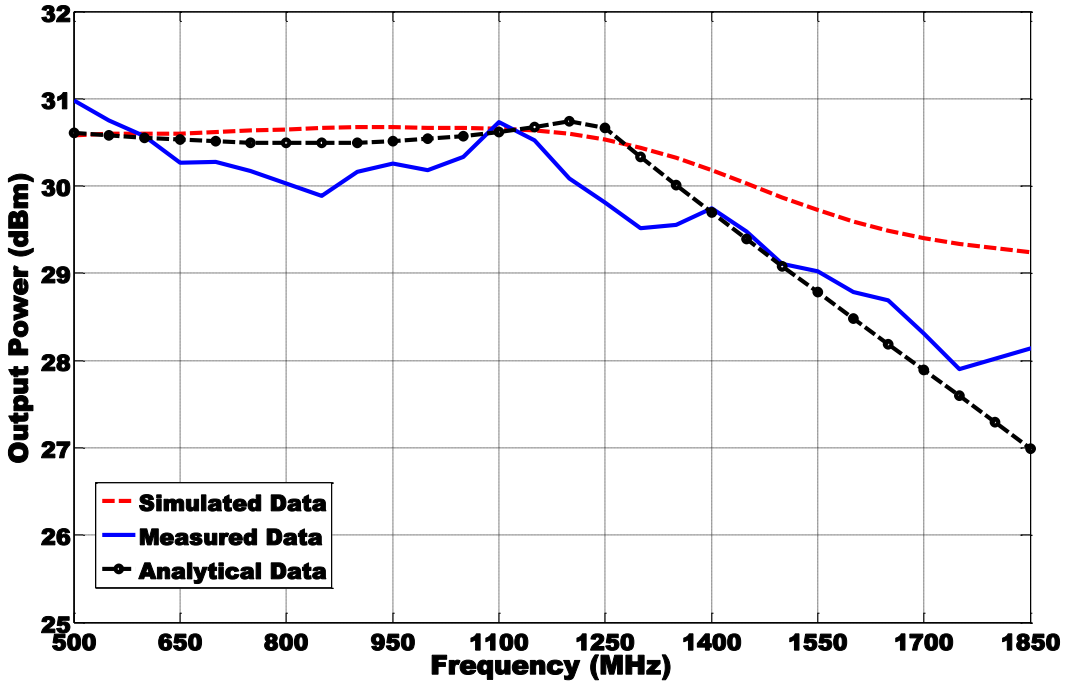


Figure 4.5. Measured and simulated output power (at backoff) versus frequency. Analytical model is also shown.

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the output power levels versus frequency from the above equivalent model; from a detailed FET-level simulation; and from measurement. The measured data shown corresponds to backoff operation, in which only a fraction (5/32) of the full DPA cells are active. This corresponds to the case of CMOS-drive limited operation. By contrast, at maximum output power, the output power is limited by the supply voltage and the load resistance, leading to a relatively frequency-independent result (broader band behavior). The measured data are in good agreement with simulation and analysis.

To model the output phase vs ACW (ACW-PM behavior), the circuit is approximated as a passive circuit consisting of a source, series resistance $R_s$, shunt elements $C_{out}$ and $R_{sh}$, and the impedance looking out of the CMOS DPA, which includes $Z_2$, $Z_3$ and $Z_4$. The phase at the output of the CMOS DPA is

$$\varphi = ang(Z_o) - ang(Z_o + R_s) \tag{10}$$

which can be simplified to

$$\varphi = \tan^{-1}\left(\frac{R_s * Im(Z_o)}{R_s * Re(Z_o) + |Z_o|^2}\right) \tag{11}$$

where

$$Z_o = Z_1\left[\frac{Z_2(Z_3+Z_4)+Z_3Z_4}{(Z_1+Z_2)(Z_3+Z_4)+Z_3Z_4}\right] \tag{12}$$

Choice of load is another critical aspect of power amplifier design. In our design a 50 Ω load is directly applied to the drain to avoid any bandwidth-limiting or lossy impedance matching network, as noted above. On the other hand, with this configuration, the harmonic impedances are non-optimal for high efficiency performance. No traps are present to suppress the output at various harmonics; harmonic amplitudes are controlled only by the parasitic capacitances within the network. It is important to note also that

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harmonics are present in the output both at high output powers (near the saturated power for the overall DPA) and for low output powers, since the unit amplifiers (which are turned ON or OFF in different numbers) are individually driven in hard-switched fashion. The output power has components at the fundamental and various harmonics, till the frequencies where the output capacitance starts presenting a low impedance path. Such a harmonically rich output power can be seen at various operating frequencies.

According to simulations, the resistance looking into the DPA changes by a factor of x35 as the ACW varies, which causes significant variation in the output phase. Additionally, the value of $C_{out}$ changes with output voltage swing, which in turn changes with ACW. The impedance looking into the source of the GaN FET also varies with voltage swing. With increasing ACW, the voltage swing at the source leads to a progressive change from class-B to class-AB biasing regime which causes the impedance to slightly decrease. The combined effect of changing series resistance, shunt non-linear

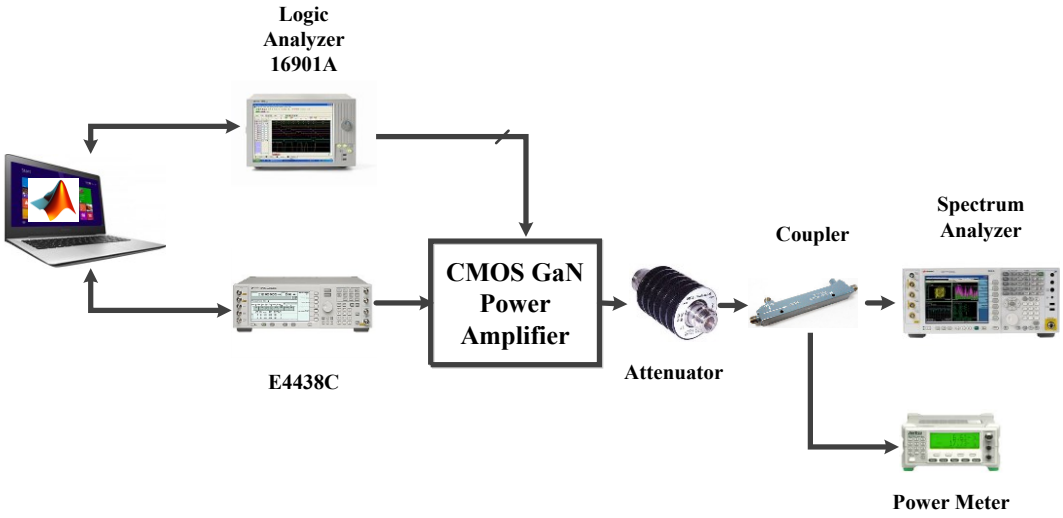


Figure 4.6. Block diagram of measurement set up.

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capacitance and load impedance provided by GaN FET leads to a complex phase behavior vs output power of the overall amplifier. Measured results are pictured below (Fig 18), showing an overall variation of about 25$^{o}$ as ACW is varied.

# 4.3 Measurement Results of CMOS-GaN Digital Power Amplifier

## 4.3.1 Measurement Setup

The CMOS DPA, with 10-bit digital control, was implemented in 180 nm CMOS partially-depleted SOI technology with supply voltage of 1.5 V [5]. Body-contacted SOI FETs were used. The 10-bit digital data were fed to the DPA in parallel fashion. The GaN

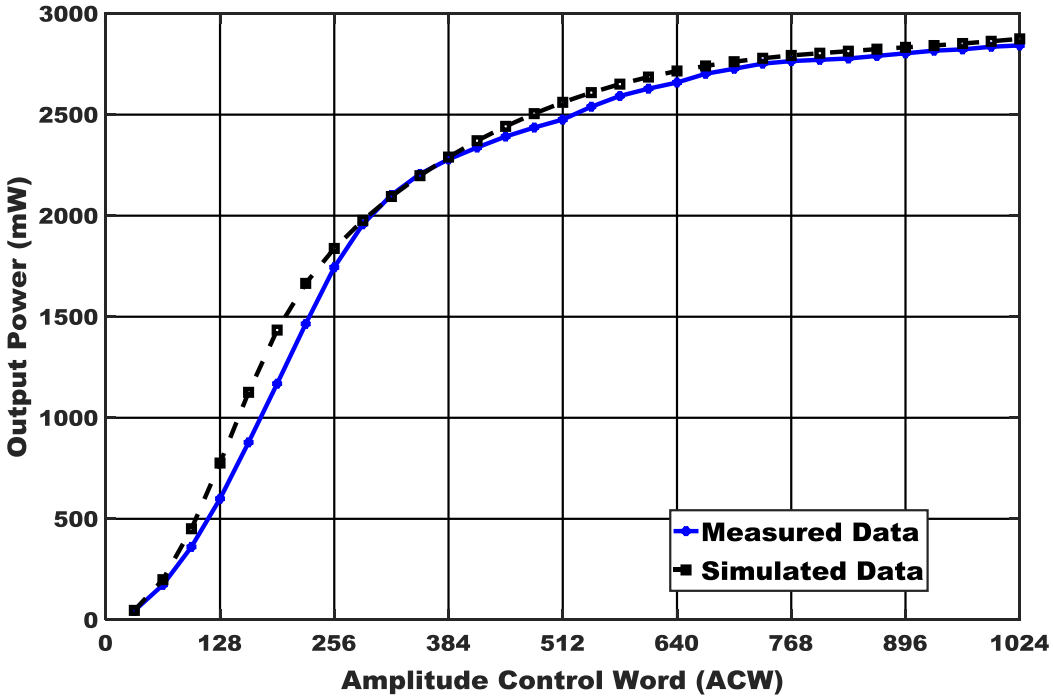


Figure 4.7. Measured and simulated output power versus amplitude control word at 900 MHz.

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HEMT driven by the CMOS DPA was implemented using Mitsubishi Electric's 0.75 um GaN HEMT process. The GaN FET used in this experiment was fabricated on a silicon substrate, and has a gate width of 2 mm, channel length of 0.75 um, $V_t$ = -3 V, $g_{m,max}$ = 400 mS, and $f_t$ = 16 GHz. Both chips were mounted on a PCB using Rogers RO4003C substrate and wirebonded for appropriate connections. The drain of GaN HEMT directly drives a 50 Ω transmission line on the PCB.

Figure 4.6 shows the block diagram of measurement set up used to characterize the CMOS-GaN DPA. The digital polar CMOS-GaN power amplifier needs amplitude and phase inputs. The digital amplitude input of 10-bit words is supplied to the amplifier from the pattern generator module of an Agilent Logic Analysis System 16901A. The pattern generator output levels of 0 V and 3.2 V are brought to needed levels of 0 V and 1.6 V using a network of resistive dividers on the PCB. These signals provide inputs to the on-chip binary-to-thermometer decoder whose supply voltage is 1.7 V.

The phase modulated input centered at RF frequency is fed from an Agilent ESG 4438C to the driver stages. A 50 Ohm termination is provided on chip at the phase modulated RF input pad. The supply voltage used for drivers is 1.7 V.

## 4.3.2 Continuous Wave Measurement Results

Figure 4.7 shows the output power versus the ACW (amplitude control word) of the CMOS-GaN DPA at 900 MHz. A peak power of 2.84 W is achieved with drain efficiency of 58%. The system efficiency in this case is 55.8%. The system efficiency considers DC power expended by the final stage, the driver stage and the digital logic

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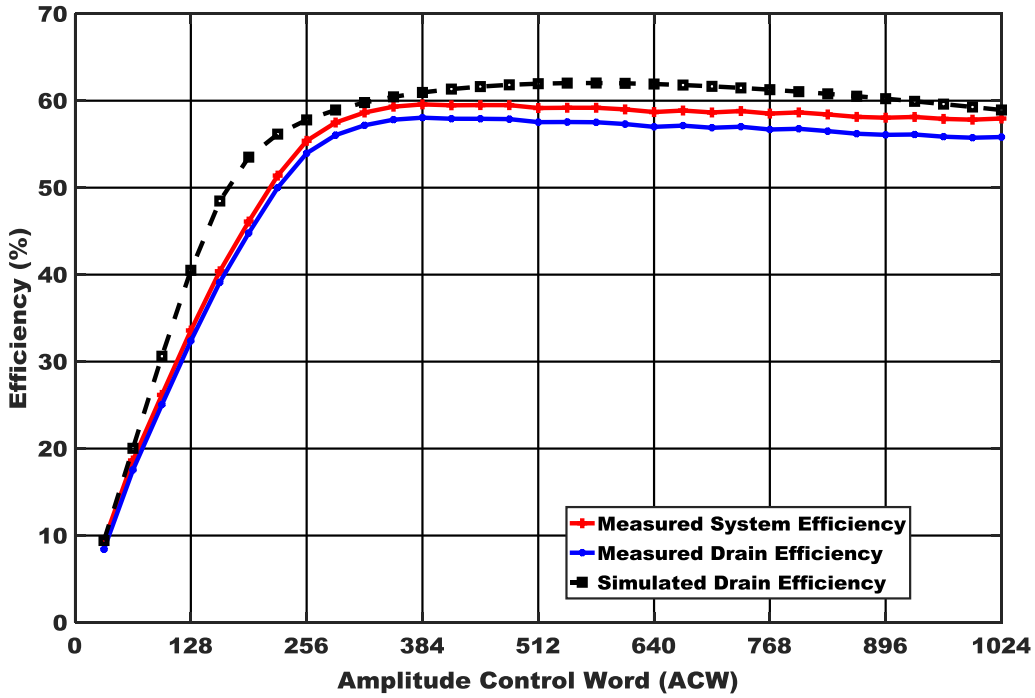


Figure 4.8. Measured and simulated efficiency versus amplitude control word at 900 MHz.

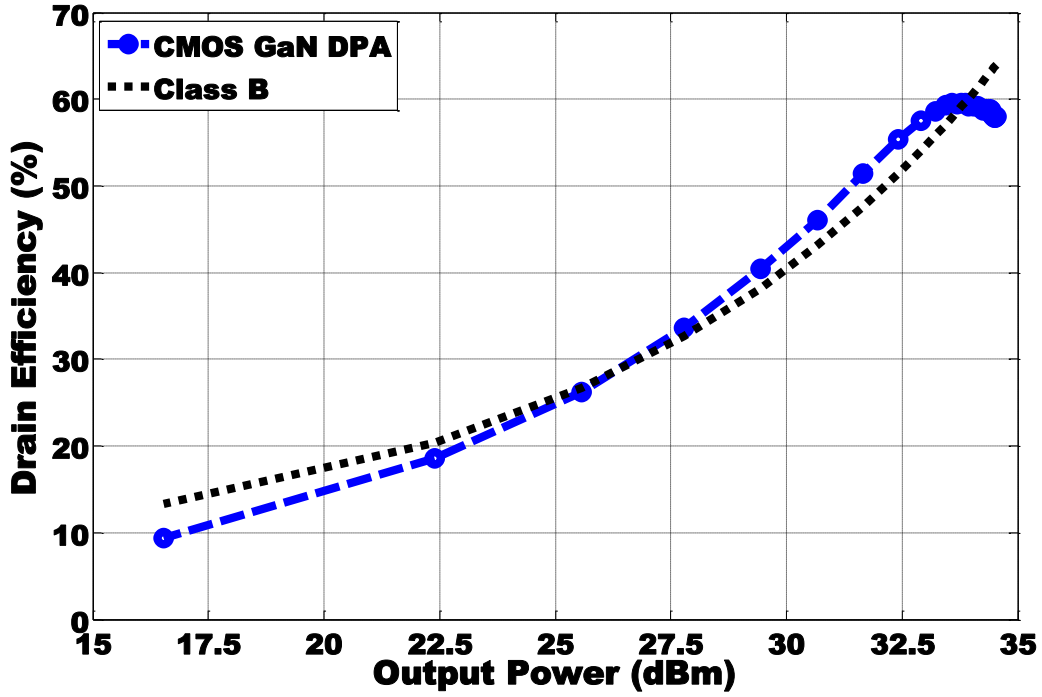


Figure 4.9. Measured drain efficiency versus output power at 900 MHz.

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circuit. The output power characteristics show quadratic increase for low ACW values (where the DPA acts like a linear current source) and compression at higher ACWs.

Supply voltage of 15 V is used in this case. The efficiency variation with ACW at 900 MHz is shown in Figure 4.8. The efficiency versus output power as the power is backed off is shown in Figure 4.9 at 900 MHz. At the maximum efficiency point the output power is 33.6 dBm with drain efficiency of 59.6%. At about 6 dB back-off the PA drain efficiency is 33.6%. This behavior is similar to that of Class-B power amplifier, as shown in the figure.

Figure 4.10 shows the measured frequency response for output power and drain efficiency. The maximum output power drops from 3.09 W to 2.48 W (34.9 dBm to 33.9

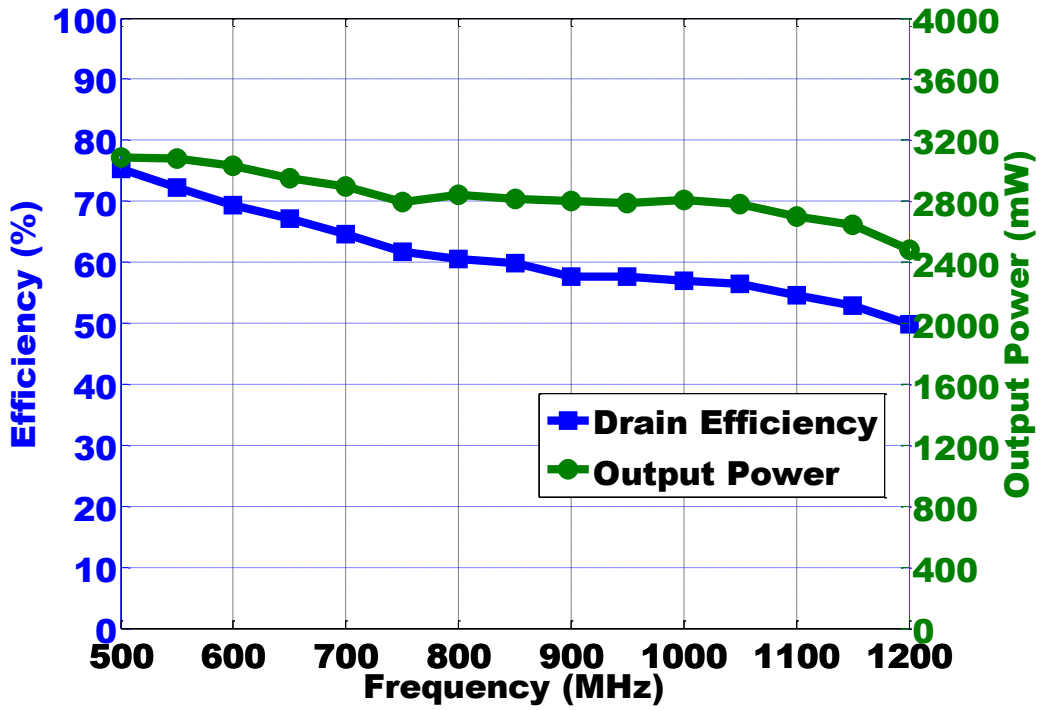


Figure 4.10. Measured efficiency and output power versus frequency

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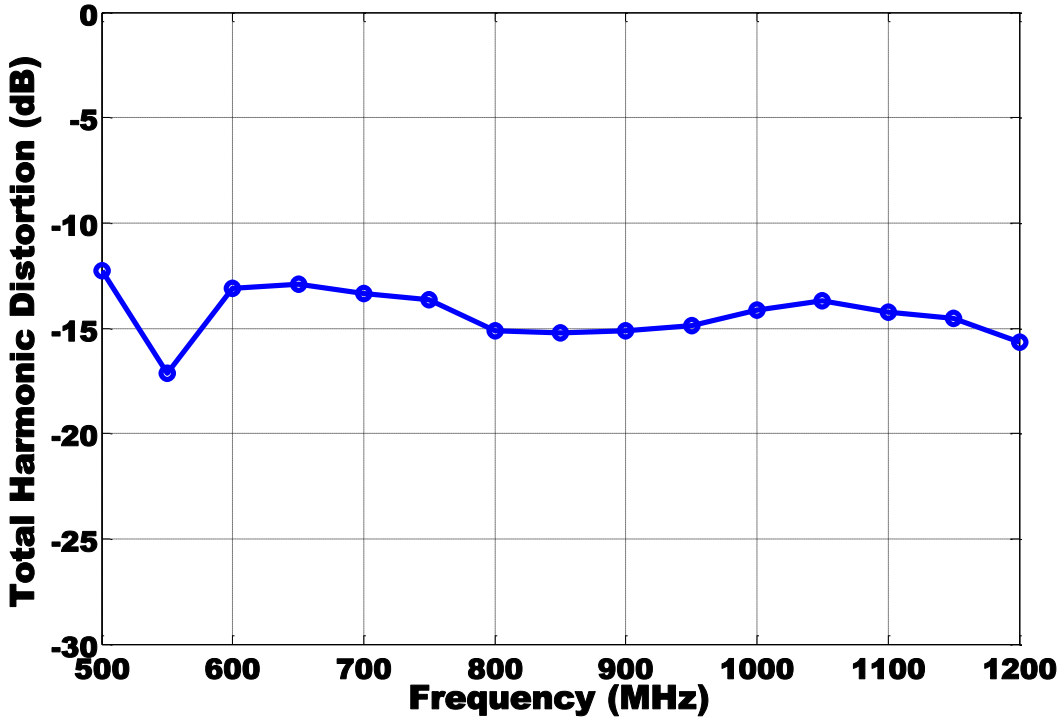


Figure 4.11. Total harmonic distortion of output power versus frequency

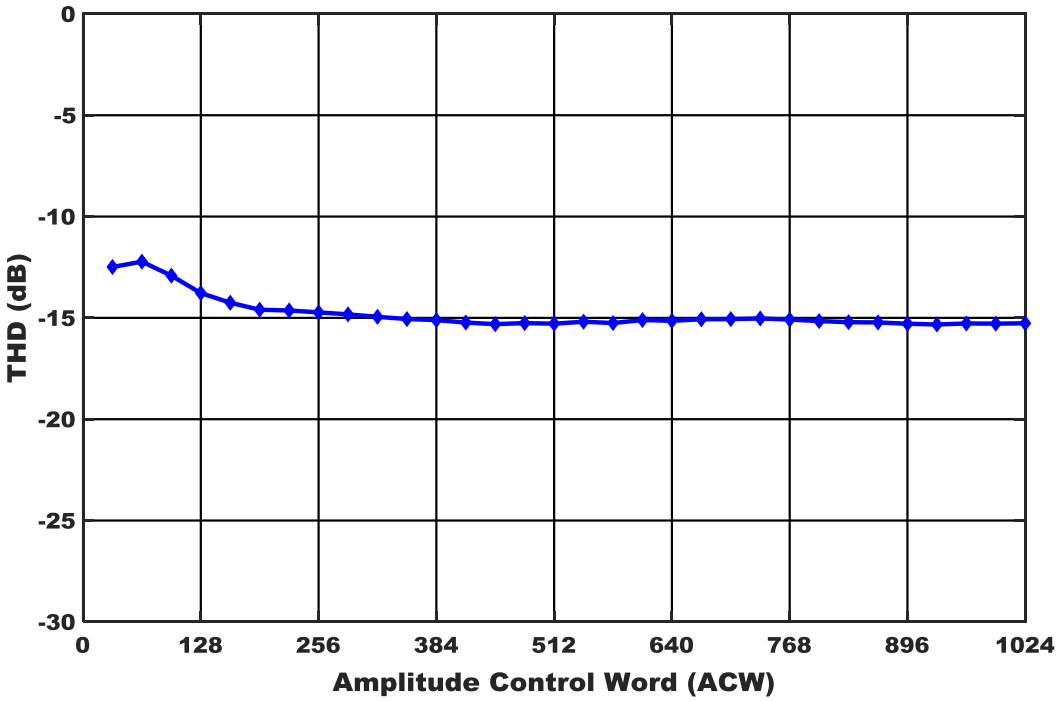


Figure 4.12. Total harmonic distortion of output power versus ACW at 900 MHz.

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dBm) from 500 MHz to 1.2 GHz. The corresponding drain efficiency drops from 75.3% to 49.9%. The 1-dB power bandwidth is 700 MHz centered around 850 MHz. Thus the power amplifier has very high fractional bandwidth of 82.3% (as expected from the absence of output matching network).

The load seen by the power amplifier has no intentionally placed harmonic termination. As noted above, this leads to wider bandwidth at the cost of reduced efficiency, and to the presence of output power at harmonic frequencies. Figure 4.11 shows the total harmonic distortion (THD) at various operating frequencies taking into account second and third harmonics (power at higher harmonics is generally much lower). For operating frequency of 900 MHz, second harmonic power is -21 dBc and third harmonic power is -17 dBc relative to the fundamental. Corresponding THD is -15.1 dBc. Fourth harmonic power is close to -30 dBc and does not significantly affect THD.

The drain current of the CMOS-GaN PA has sigificant harmonics at both peak power and at low ACW, as described above. Figure 4.12 shows the THD variation with ACW

at 900 MHz. The THD is seen to be elatively invariant with changing ACW.

### 4.3.3 Quantization Steps and Errors

The CMOS-GaN DPA can be regarded as an RF digital-to-analog converter (RFDAC) whose output voltage amplitude is the analog equivalent of the input digital word. The implemented RFDAC has 10 physical bits. This leads to 1024 output voltage amplitude states. Similar to a mixed-signal DAC, the DPA output has quantization steps as well as ingrained non-idealities. Apart from unintentional non-idealities, the output

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also has compressive behavior. To understand and quantify the overall non-ideal behavior, the output errors must be separated from the expected compressive non-linearity.

One of the several ways of doing this is to assume the DPA has a certain nonlinear relation between output RF amplitude and digital input, model this behavior and define error figures-of-merit based on the difference between measured data and modeled "ideal" behavior. In principle when digital predistortion (DPD) is used to linearize the output (for example, using a polynomial-based method) the "ideal" modelled compressive behavior can be accurately compensated.

To evaluate errors (deviation of measured value from modelled value) in our

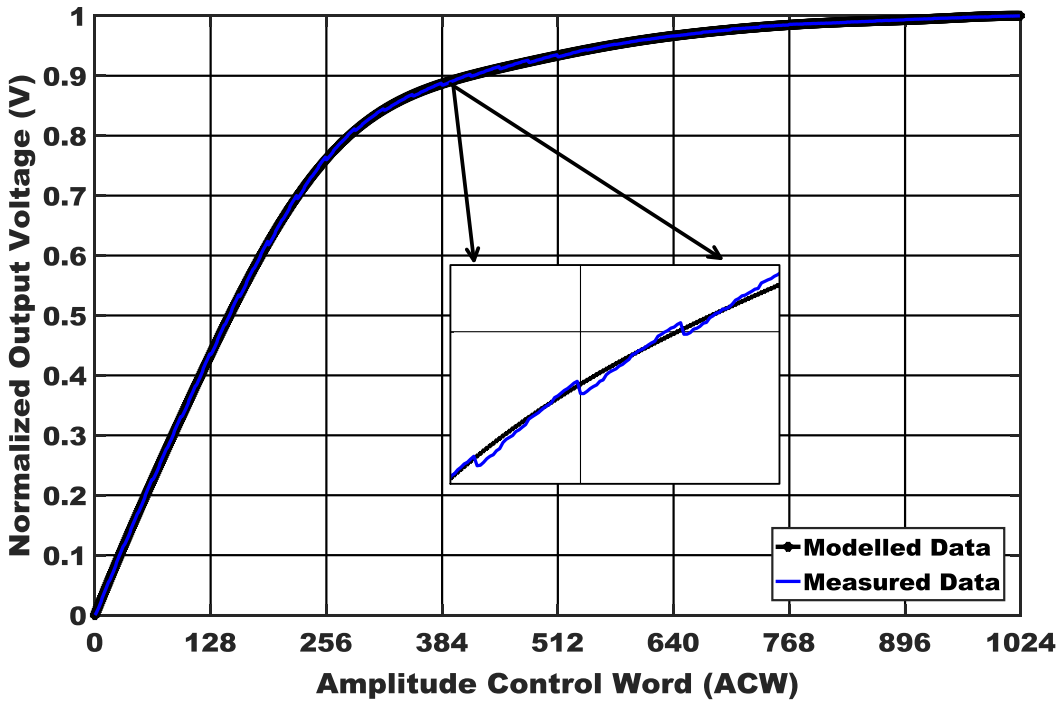


Figure 4.13. Measured and modelled quasi-static normalized output voltage at 900 MHz.

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work, measured voltage amplitude outputs for every state are compared to modelled outputs for that state. Both measured and modelled outputs are normalized to their peak values. Thus

$$error(i) = v_{measured}(i) - v_{modelled}(i) \quad (13)$$

Where $v$ corresponds to normalized voltage amplitude. Figure 4.13 shows $v_{measured}$ and $v_{modelled}$ vs ACW, corresponding to quasistatic measurements. The modelled curve employs a 15$^{th}$ degree polynomial. Figure 4.14 shows the error profile of the DPA vs ACW. With the given normalization, the LSB for a 10 bit system would correspond to 1/1024.

The measurements show error peaks that occur at particular codes. These codes

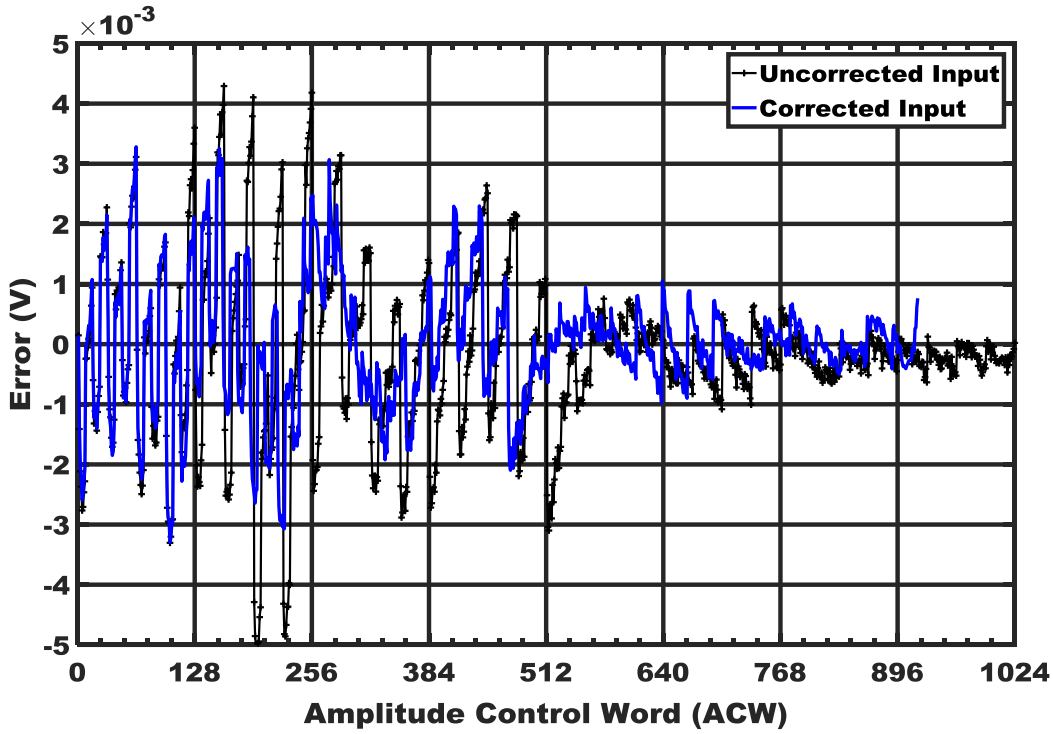


Figure 4.14. Measured normalized output error voltage amplitude vs input code word (with correction).

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correspond to transitions when a new unary bit is turned-on and all (previously on) binary weighted bits are turned off, as seen in Figure 4.13. Within our chip, there is a systematic difference between the aggregated values of the binary bits and the desired result based on the unary bits. While redesign and resizing binary transistors could potentially minimizing this problem, the error peaks can be partially mitigated by avoiding specific code states where the errors are largest. Such a scheme also makes the DPA output monotonous with ACW. Errors for this "corrected" ACW are also shown in Figure 4.14. The maximum deviation from modelled data on this basis is 3.3 $x10^{-3}$, which corresponds to a quasi-static error-based ENOB of 7.2.

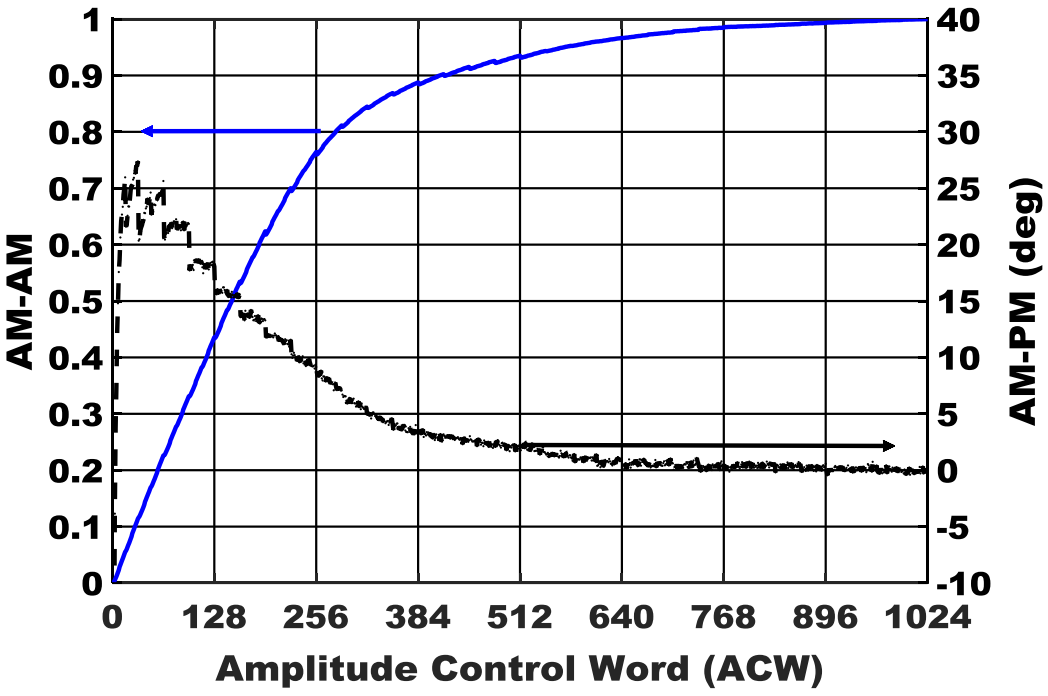


Figure 4.15. AM-AM and AM-PM of CMOS-GaN DPA at 900 MHz

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### 4.3.4 Modulated Signal Measurement Results

To produce modulated output signals, digital inputs corresponding to the amplitude, and a phase-modulated RF carrier input are required. These must be accurately time aligned. In the following, results for 5 MHz 16-QAM signals are presented. The 10-bit ACWs were derived from an Agilent Logic Analyzer 16901A and phase modulated carrier from an Agilent ESG 4438C, both sampled at the rate of 45 MHz. Sub-sample level time-alignment was performed to achieve best possible ACPR. Memory-less, equation-based digital pre-distortion was performed to meet the specifications.

Figure 4.15 shows the AM-AM and AM-PM characteristics of the power amplifier at 900 MHz. In this case the digital data is traversed from lowest ACW to highest in quasi-static fashion. The AM-PM behavior is dominated by the CMOS DPA; measurements of this circuit block alone show similar spread in phase response with back-off. The AM-PM behavior can be attributed to the effect of varying output resistance of the DPA vs ACW, together with the output capacitance of the circuit.

For the single-carrier 16-QAM signal of 5 MHz bandwidth measurements, the PAPR was 7.3 dB. Figure 4.16 shows the output spectrum centered at 900 MHz. Figure 4.17 shows the IQ constellation of the demodulated output signal. The EVM was measured to be 2.3%. The average output power is 27.7 dBm at drain efficiency of 38.1%. The ACLR values were -38.4 dBc and -38.2 dBc on lower and higher side of the band. Figure 4.18 and Figure 4.19 show the AMAM and AMPM behaviour of CMOS-GaN DPA before and after memoy-less correction (pre-distortion) is performed.

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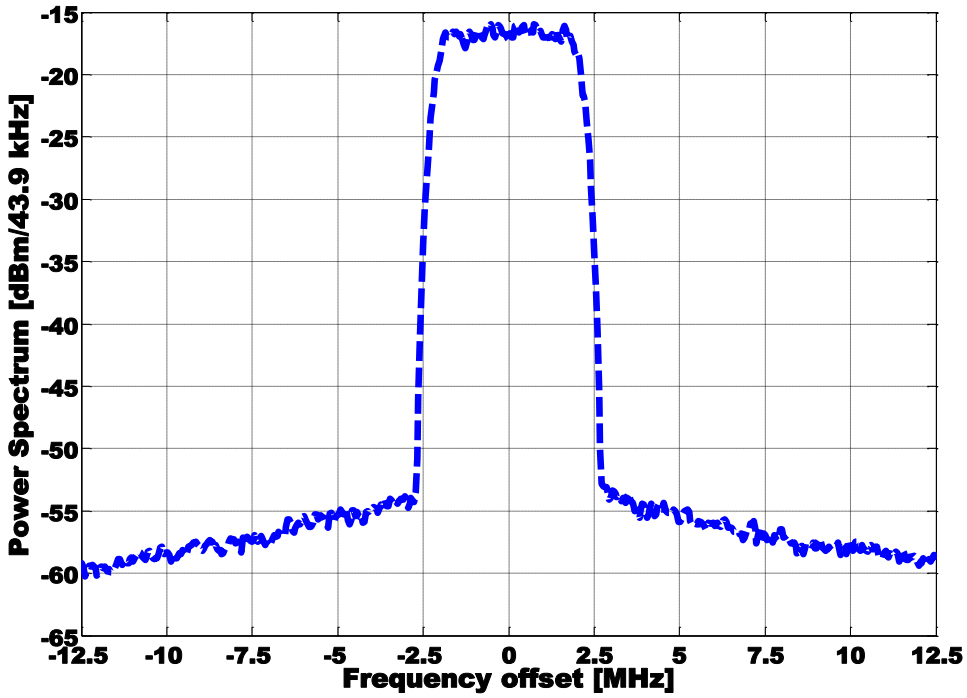


Figure 4.16. Output spectrum of 5 MHz 16-QAM signal at 900 MHz

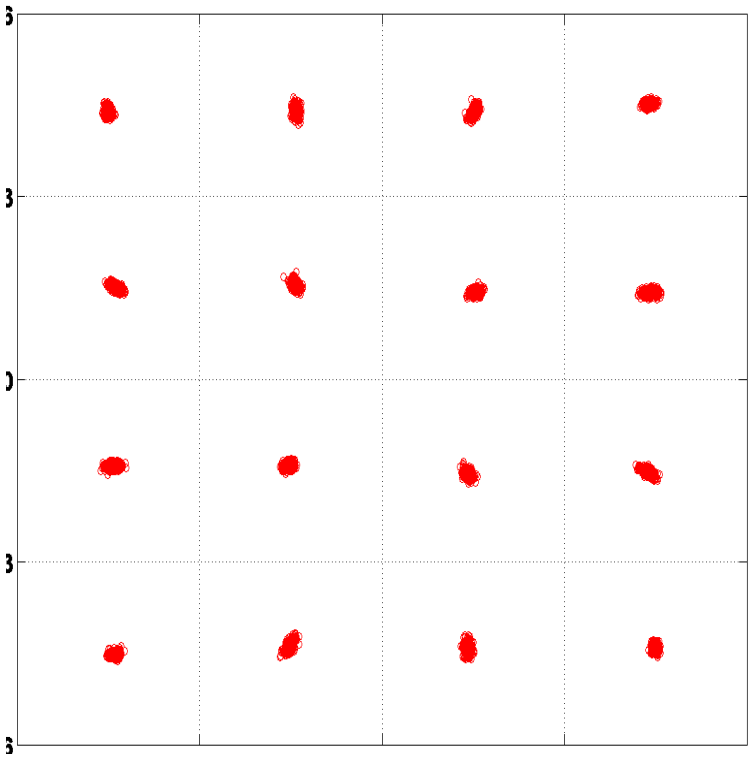

Figure 4.17. Measured IQ constellation of output for 5 MHz signal centered around 900 MHz (EVM = 2.3%)

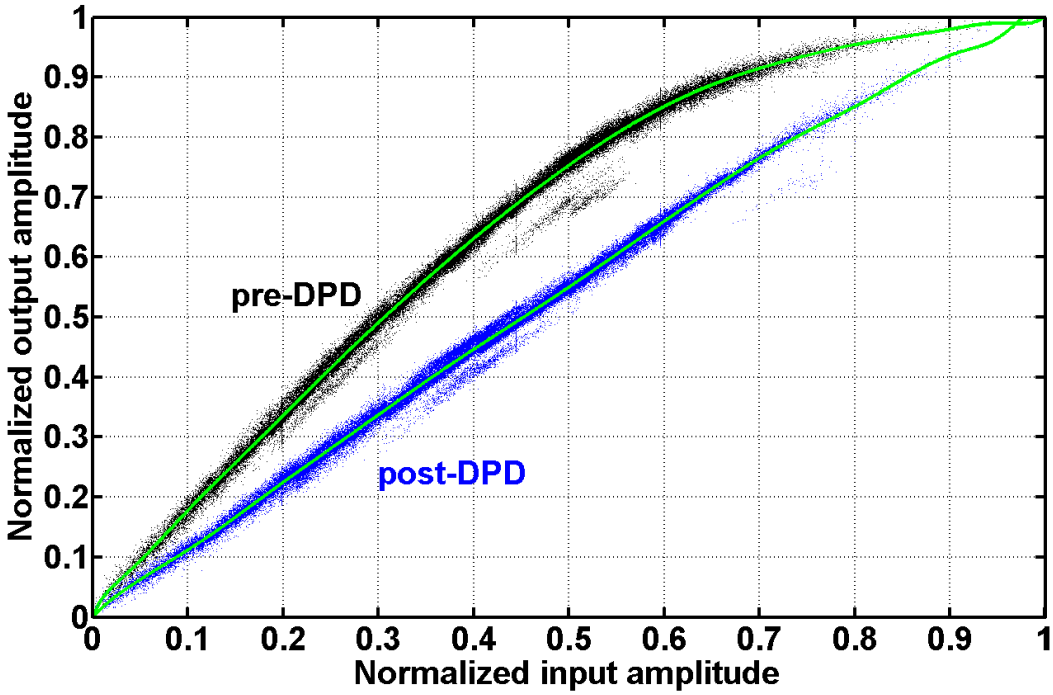


Figure 4.18. Measured AMAM behavior for 5 MHz 16-QAM signal : before and after equation based digital predistortion.

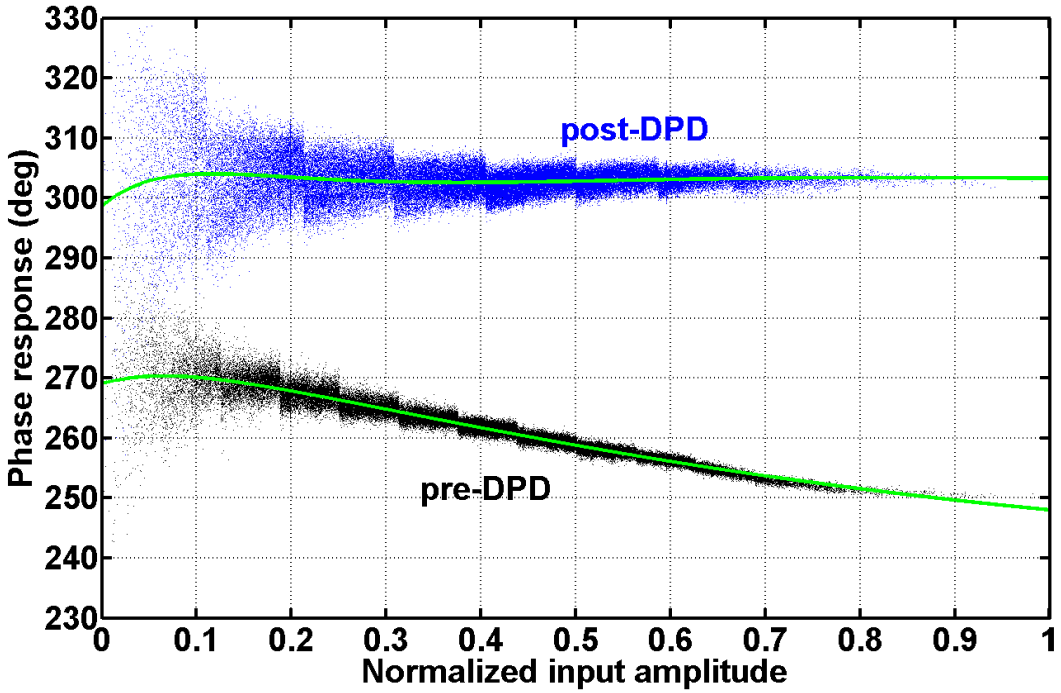


Figure 4.19. Measured AMPM behavior for 5 MHz 16-QAM signal : before and after equation based digital predistortion.

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The CMOS-GaN DPA was also tested with a single-carrier 64-QAM signal of 5 MHz bandwidth and 6.9 dB PAPR. Figure 4.20 shows the output spectrum centered at 900 MHz. Figure 4.21 shows the IQ constellation of the demodulated output signal. The EVM was measured to be 3.6%. The average output power was 27.72 dBm at drain efficiency of 38.3%. The ACLR were -36.2 dBc and -38.5 dBc on lower and higher side of the band.

Modulation signal testing using 5 MHz bandwidth 16 QAM signal was also performed at various frequencies from 500 MHz to 1.2 GHz. Figure 4.22 shows the average power and drain efficiency for various frequencies. Figure 4.23 shows the ACLR and EVM at these frequencies. The time-alignment and pre-distortion was performed separately at each frequency to achieve best linearity results.

## 4.4 Circuit Limitations and Opportunities

It can be expected that the proposed architecture will be capable of providing digitally-controlled power amplifiers over a broader bandwidth than was measured experimentally. In our analysis, we found that the parasitic inductance from the drain of the CMOS DPA to the source of GaN FET presented significant limitations to the bandwidth performance. These could be combated by more optimal design and assembly, even using distinct chips for the GaN and the CMOS as was done in this work. Eventual co-integration of GaN and CMOS on one substrate may also become possible, to achieve the highest bandwidths.

Bandwidth can be further enhanced by using an accelerating capacitor across the drain-source terminals of GaN FET ($C_{ds}$). In theory, this capacitor accelerates the

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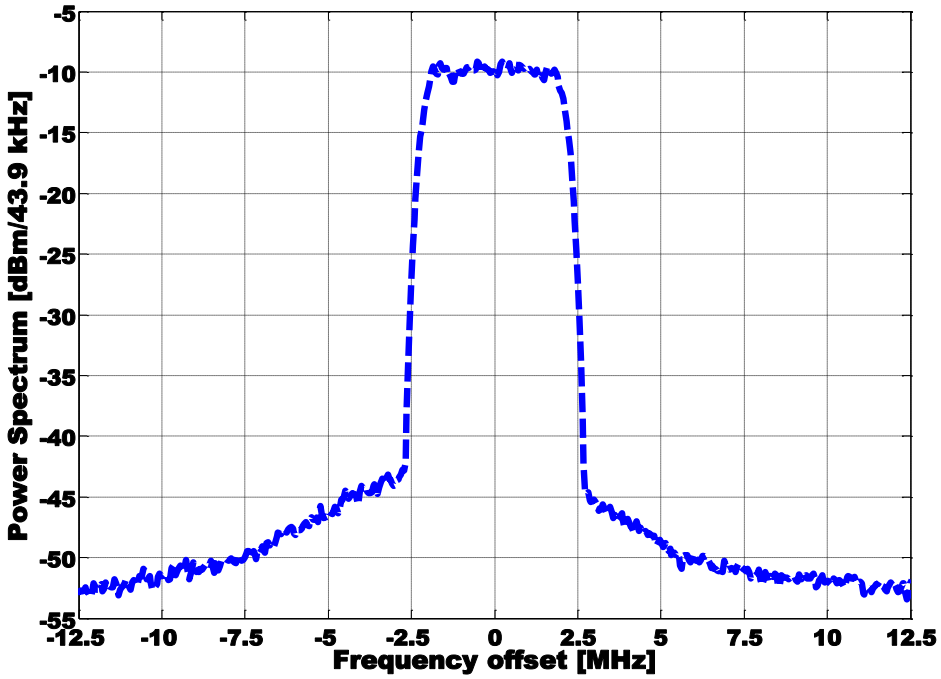


Figure 4.20. Output spectrum of 5 MHz 64-QAM signal at 900 MHz

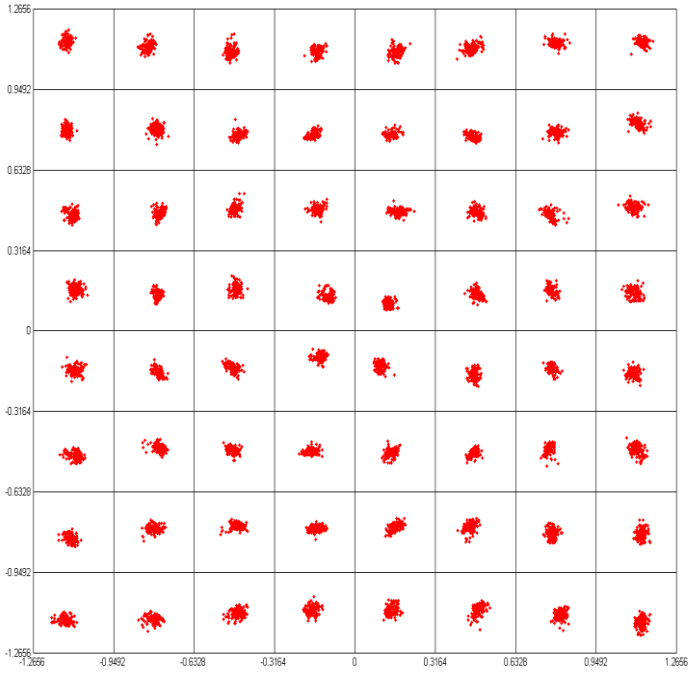


Figure 4.21. Measured IQ constellation of 64 QAM output for 5 MHz signal centered around 900 MHz (EVM = 3.6%)

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charging and discharging of floating node between the CMOS block and the GaN FET thus enhancing the circuit bandwidth (at the cost of extra capacitance at the GaN FET drain). Alternatively, this can be viewed as presenting a negative capacitance at the source node of GaN FET, leading to faster turn-on behavior. A simple simulation of frequency response of CMOS-GaN DPA with an appropriately chosen capacitor (2.6 pF) leads to enhanced bandwidth (on order of 10%). This capacitor should be as close to the FET as possible to minimize parasitic inductances.

One of the important aspects of broadband circuits is the $f_t$ of technology. In our implementation the $f_t$ of the CMOS SOI FETs is on the order of 65 GHz. The measured $f_t$ of GaN is close to 15 GHz. By implementing similar designs with faster transistors will

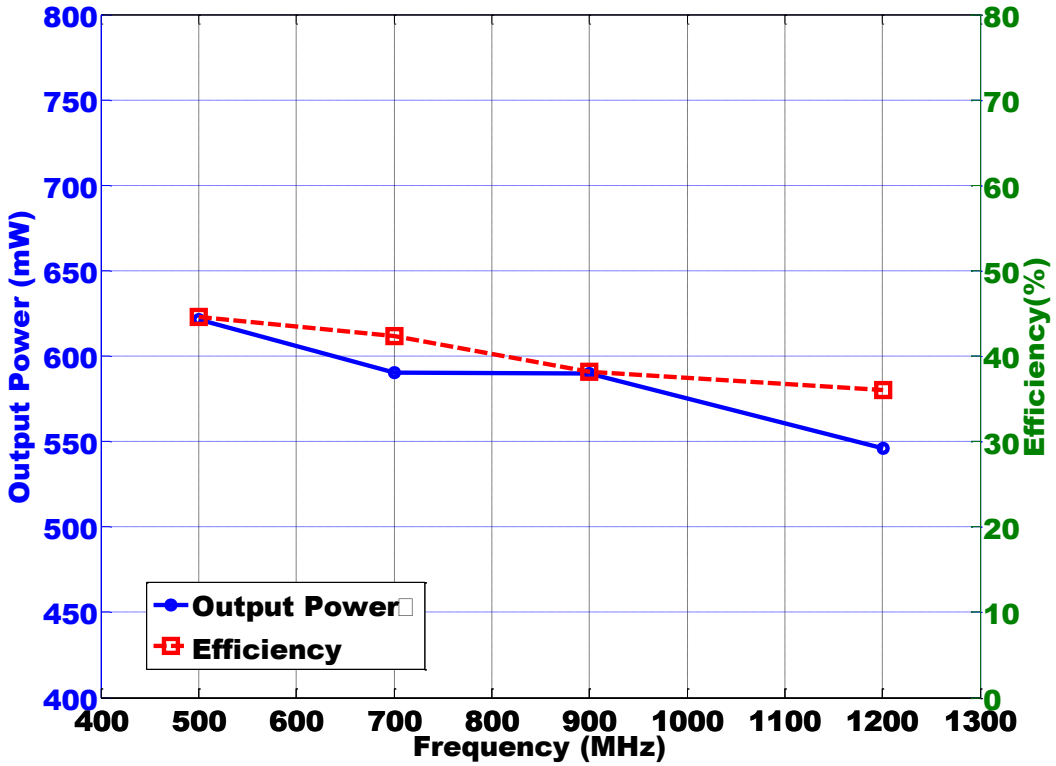


Figure 4.22. Output power and drain efficiency versus frequency for 5 MHz 16-QAM signal.

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lead to broader bandwidths.

The harmonic content of the output power is one of the concerns in the architecture. For a fixed frequency of operation, harmonic traps are part of traditional design. Designing harmonic traps to yield a harmonically clean output power over a broad band is very challenging. If the design is more than an octave in bandwidth, the preferred way to get clean output power across the band is by implementing tunable harmonic traps (although differential versions of the present design could achieve significantly lower second harmonic power at the output).

For cellular frequency division duplex (FDD) systems, receive band noise is also an important concern. Digital power amplifiers have major limitations due to quantization

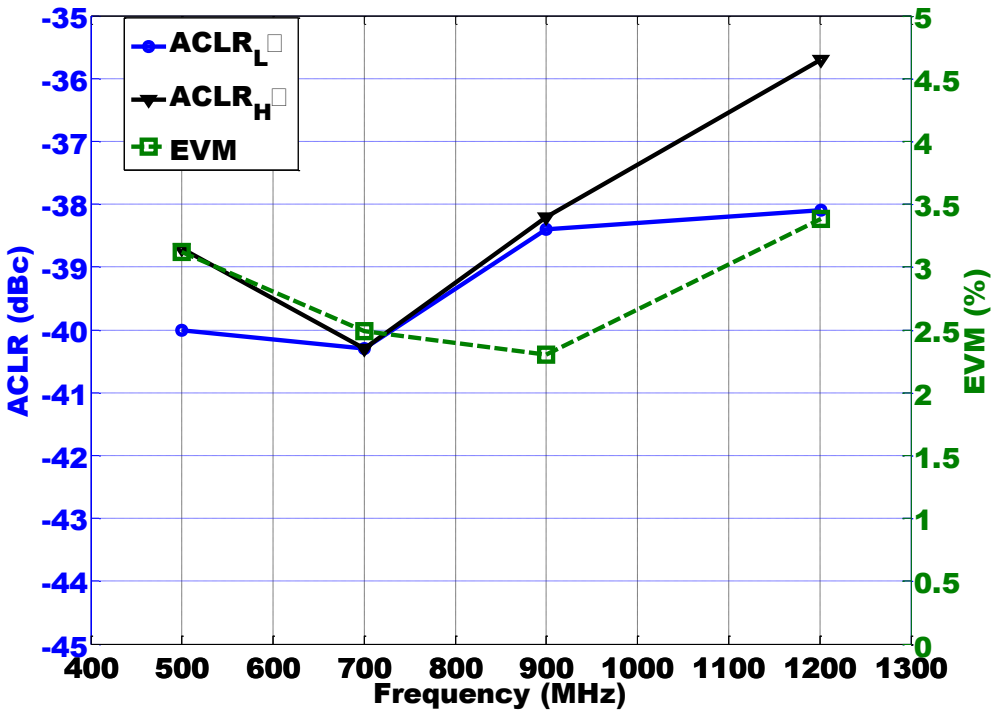


Figure 4.23. ACLR and EVM versus frequency for 5 MHz 16-QAM signal

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noise and code glitches, which can lead to out-of-band noise and non-linearity. The work shown here also has the added complication of time-alignment between AM and PM signals, which produces spurious outputs that affect close-in ACLR as well as broadband noise. Figure 4.24 shows the output spectrum over a wide range for a 5 MHz 16 QAM signal with a PAPR of 7.3 dB centered at 500 MHz. The quantization noise floor is found to be 48 dB lower than the main power spectral lobe, leading to an estimated ENOB of 6.9 using the equation 14,

$$SQNR = 12 * \frac{2^{2n}}{PAPR} * \frac{f_s}{RFBW} \tag{14}$$

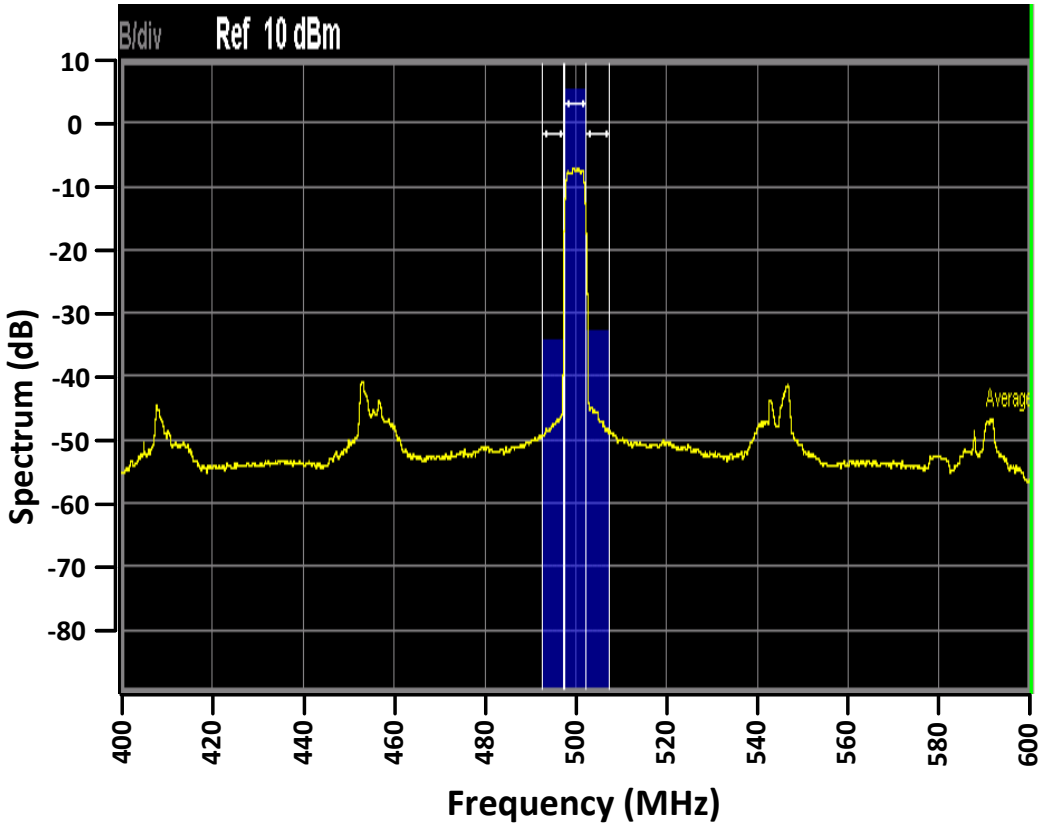


Figure 4.24. Far-out spectra of CMOS-GaN DPA output with sampling rate of 45MS/s

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where *SQNR* is main signal to quantization noise ratio, *n* is ENOB, *PAPR* is the peak-to-average ratio of output signal (output PAPR of 7.1 considered in calculation), $f_s$ is the sampling frequency of the data and *RFBW* is signal bandwidth. The clock images are found to be approximately 35 dB lower than main band. The ratio of $f_s$ to *RFBW* is 10 in our measurement. Increasing this ratio will reduce the quantization noise floor. This will also push the clock images further away from main signal. On-chip digital upsampling and filtering will help move these clock images to much lower levels [13] and suppress quantization noise [14].

## 4.5 Conclusion

A hybrid power amplifier using a CMOS-GaN combination achieving high efficiency and broad bandwidth has been presented. A stacked-FET design has been used to achieve CMOS output voltage sufficient to drive the GaN FET. The amplifier directly drives a 50 Ω load; absence of matching network increases the output bandwidth.

Amplifier operation has been shown from 500 MHz to 1.2 GHz. The peak power achieved ranges from 2.4 W (1.2 GHz) to 3 W (500 MHz) with peak drain efficiency from 48% to 74%. The CMOS-GaN PA has also been demonstrated to work for 5 MHz bandwidth signals with complex modulations including 64-QAM. The experimental results exploit polar architecture to achieve high efficiency, and digital controllability to perform pre-distortion.

This work shows the promise of combined CMOS-GaN amplifiers to implement digitally-controlled multiband RF PAs for applications such as micro-cell base stations, although issues such as Rx band noise remain to be addressed.

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## 4.6 Acknowledgment

Chapter 4 is mostly a reprint of the material as it appears in “Design of a Digitally-Controlled Broadband Polar Power Amplifier using a CMOS and Gallium Nitride Combination”, V. Diddi, S. Sakata, S. Shinjo, V. Vorapipat, R. Eden and P. Asbeck, submitted for publication in IEEE Transactions on Microwave Theory and Techniques and the material in “Broadband digitally-controlled power amplifier based on CMOS / GaN combination”, V. Diddi, S. Sakata, S. Shinjo, V. Vorapipat, R. Eden and P. Asbeck, IEEE RFIC Symposium 2016. The author of this dissertation was the primary investigator and primary author for this material.

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# Chapter 5

# Conclusions and Future Work

## 5.1 Dissertation Summary

Power amplifier design is going to pose significant challenges in next generation cellular communication. Cost, performance and integration are going to be critical parameters. From cost and integration perspective, silicon CMOS technology is attractive for PA implementation. As digital control can be easily implemented using digital circuits in CMOS, controlling PA output is also going to be easy. But CMOS technology has inferior breakdown voltage compared to compound semiconductor technology. This dissertation addresses the problem and details design and implementation techniques for power amplifiers in silicon CMOS SOI technology. FET stacking technique is used to combat lower breakdown voltage of CMOS SOI FETs and provide high output power. Digital circuits are designed to control the effective width of active PA; thus establishing digital control over PA output power. Making sure that the designed IC has no frequency sensitive components, yields a working PA that can be used at multiple frequencies. PA implementation in polar architecture leads to high efficiency performance.

A building block digitally modulated polar power amplifier (DPA) was presented in Chapter 2. This PA takes constant amplitude phase modulated (PM) signal at RF and 10-bit digital amplitude modulation (AM) signal to provide output signal of needed amplitude and phase. 10-bit digital input controls 31 unary cells with 5 MSB bits (using a binary-to-thermometer decoder) and 5 binary weighted cells with 5 LSB bits. Each cell is a 4-stacked FET PA, drains of all are connected together. An off-chip matching network in the form of single-section L-match is implemented using SMD components to provide class-J-like load to the overdriven CMOS DPA. At 900 MHz, CMOS DPA designed using body-contacted CMOS SOI FETs yields >1.4 W of output power with >65% drain efficiency. The multi-frequency operation with high efficiency was demonstrated for CMOS DPA. Modulation signal measurements show good performance for 10 MHz 16-QAM OFDM (25.7 dBm output power at 37.5% drain efficiency) using a memory polynomial based digital pre-distortion. Using a memory-less equation based pre-distortion was used for 5 MHz 16-QAM signal to meet the cellular specs of ACLR better than -30 dBc with output power of 22.3 dBm and drain efficiency of 24%.

To transmit signals of high PAPR, PA needs to have good back-off efficiency. Doherty amplifier uses peaking amplifier to perform load modulation for main amplifier leading to improved back-off efficiency. The CMOS DPA was used to digitally controlled Doherty power amplifier as described in Chapter 3. The main and peaking amplifier are independently digitally controlled and are realized using identical CMOS DPAs. A lumped-element, off-chip Doherty combiner is designed using SMD components to provide required impedances for both power amplifiers at peak and back-off power levels. The digital Doherty PA yields high peak output power of >2 W at 900

MHz with peak drain efficiency >55%. At 6-dB back-off the drain efficiency is >52%. This efficiency improvement in back-off is because of strong ON/OFF characteristics of digital PAs and careful design of Doherty combiner to make sure that peaking amplifier presents an open in OFF state (rather than looking like a capacitor). CW measurements show a strong efficiency peak at 5.1 dB power back-off reaching 54.6% drain efficiency. The digital Doherty amplifier gives 25.7 dBm average output power with 45.5% average drain efficiency with transmitting a 64-QAM OFDM signal of 7.4 dB PAPR.

The CMOS DPA employs stacked FET topology leading to very high output power. There are many ways of increasing higher output power – more stacking or increasing total width size of DPA. Former leads to lower efficiency, while later reduces optimum impedance making impedance transformation difficult. Large sized PAs generally have lower bandwidth – both due to impedance transformation and increased parasitic drain capacitance. In Chapter 3, CMOS-GaN DPA design is described. This uses large output power of CMOS DPA to drive a GaN FET. The GaN FET then drives a straight 50 Ω load. This yields large output power. Any impedance transformation networks are avoided to make achieve broadband performance (leading to lower efficiency as no harmonic termination is employed). Such a PA would find application in femto-cell or pico-cell transmitters. More than one octave of carrier bandwidth (500 MHz to 1.2 GHz) was obtained. The CMOS-GaN DPA was tested with 16-QAM signal over wide frequency range and good efficiency was obtained, while meeting good linearity numbers.

## 5.2 Future Work

The DPA (and all other circuits built from it) show elevated noise floor owing to quantization errors inherent in a digitally controlled PA. Such high noise floor is not observed in classical biased Pas with analog inputs. This leads to significant noise in receive band of transceiver. This is problematic for FDD systems, as the TX signal corrupts RX signal. Clock images are also seen in the output spectrum. Both of these issues can be solved by implementing a programmable FIR filter on-chip [1-2]. Clock images can be moved out by using higher sampling rate for transmitter. A novel technique of cancelling TX noise in RX band on receiver side has also been developed by Mr. N. Rostomyan. This system shows promising results by pushing noise floor from TX leakage to below -180 dBm/Hz while employing a commercially available duplexer for the FFD transceiver. Even without this correction, the architectures of the CMOS DPA and its extensions are very suitable candidates for TDD systems. The 5G sub-6GHz cellular communication is a potential application for these circuits, if standards evolve to be TDD.

The CMOS DPA uses digital AM while PM comes from a laboratory instrument in the experiments conducted. A CMOS digital phase modulator [3-4] can be used to implement a fully digital PA. Such a PA will have all digital inputs, generating controllable output power with complex modulation formats.

The modulation bandwidth can be increased by using memory-polynomial DPD as seen in Chapter 2. This indicates that the DPA currently exhibits memory effect and, based on experiments performed, it is concluded that the decoupling of driver stages

determines the AM-AM and AM-PM "cloud". For high sampling rate the decoupling becomes critical. Future work should focus on better decoupling to enhance modulation bandwidth while using memory-less DPD.

The DPA / RFDAC architecture as developed in this thesis is attractive from the system stand-point because the circuits are carrier frequency agnostic. A single DPA with switchable matching network can work for very wide range of frequencies. This is demonstrated by the results of multi-frequency of CMOS DPA in Chapter 2. The future work should attempt in making this design more flexible by using digitally switchable matching networks. Such networks can be implemented on integrated passive device technology which offers high Q passive components. The digitally controlled switches can be implemented in CMOS SOI technology. This design can be very flexible and can be used to solve the issue of non-optimum drain load seen by PA for non-50 Ω post impedance transformation load.

To improve the bandwidth of digital Doherty PA, an improved output network for peaking PA needs to be designed. A simple π-network implementation of offset transmission line leads to reduced impedance excursion on smith chart, which in turn leads to improved bandwidth. Figure 5.1 and Figure 5.2 show the circuit implementation and impedances on smith chart respectively. The future work should also focus on using digitally switchable matching networks to vary load impedance seen by main PA in back-off. This would lead to digital Doherty with digitally controllable back-off powers where efficiency peaks.

The technology and assembly improvement would, in future, lead to bandwidth enhancement of CMOS-GaN DPA. Future designs should focus of making back-off

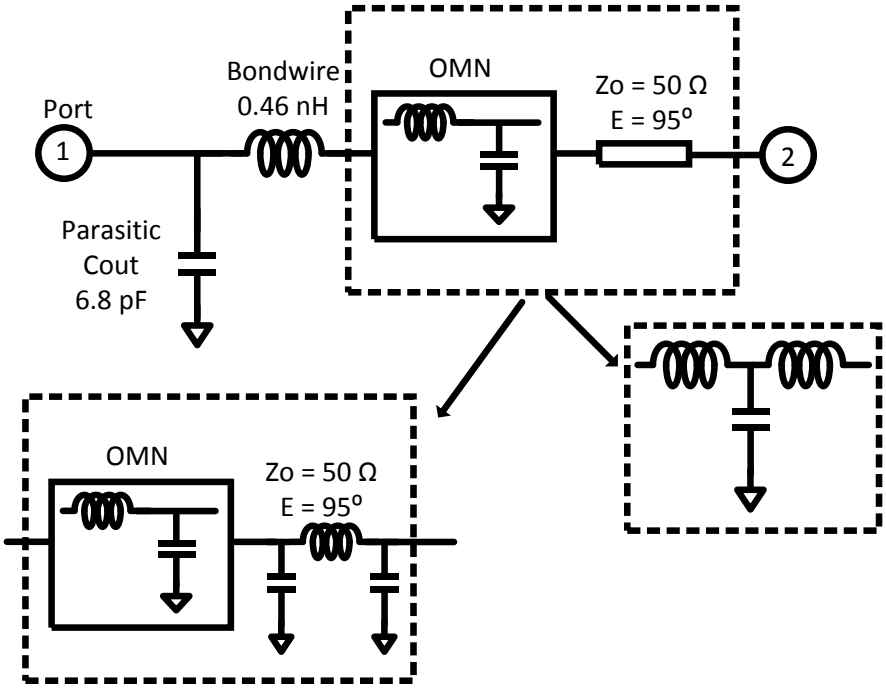


Figure 5.1. Output network for PPA, using OMN and transmission line, T-equivalent network used experimentally, and OMN and lumped equivalent of transmission line.

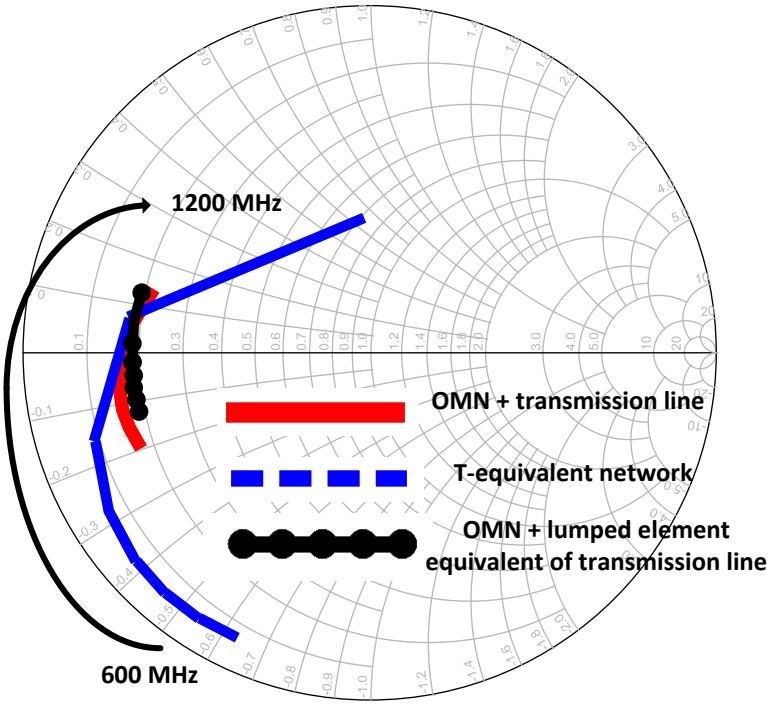


Figure 5.2. Impedance excursion on smith chart for different implementations of output network for PPA.

efficiency improvements in CMOS-GaN DPA by implementing a CMOS-GaN Doherty PA. In general, Doherty PA imposes bandwidth limitation of its own. Doherty combiner at the output would become the bandwidth limiting factor, instead of impedance transformation limit. In femto-cell applications, implementation area is not as stringent a limitation as handset application. Complex low-loss output combiners can be designed and implemented on PCB/laminate. Future work should look at architectures like Doherty-Outphasing continuum [5] which offer very wideband performance.

## 5.3 References

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