Wireless Powering of mm-scale Fully-on-chip Neural Interfaces

(Invited Paper)

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***Abstract*—This paper presents guidelines for the design and optimization of on-chip coils used for wirelessly-powered mm-scale neural implants. Since available real estate is limited, on-chip coil design involves managing difficult trade-offs between the number of turns, trace width and spacing, proximity to other active circuits and metalization, quality factor, matching network performance/size, and load impedance conditions, all towards achieving high power transfer efficiency. To illustrate the design optimization procedure, a 3×3 mm^2 on-chip coil is designed, and measurement results reveal a 3.82 % power transfer efficiency for a 1.6 kΩ load that mimics a 100 μW neural interface.**

I. Introduction

Miniaturized implantable microchips featuring on-chip electrodes, amplifiers, stimulators, and wireless power transfer (WPT) and telemetry capabilities can offer electrical access to the cortical surface at high electrode density. If the fully-on-chip neural interfaces are smaller than the radius of curvature of the cortical surface (i.e., at mm-scales), many such chips can be arrayed across the curves of the cortical surface (Fig. 1), potentially enabling higher global electrode density than ECoG or μECoG [1]. As fully wireless modular devices, interconnect problems that burden conventional approaches are eliminated.

However, for several reasons, the achievable quality factor (Q) of mm-scale on-chip coils is low, which, when coupled with the small physical size and relatively large transcutaneous separation between the implant and an external driving coil, results in low power transfer efficiency (PTE) [2]. Unfortunately, conventional Q-enhancement techniques such as patterned ground planes cannot be applied to the interior of fully-on-chip neural interfacing devices, as other active circuitry must exist there. Design rules limit area and trace width/spacing that, coupled with finite metal heights, finite conductivity of p-type silicon (p-Si) substrates, and peripheral circuits within the center of the coil, all serve to limit achievable Q and degrade the coil's self-resonant frequency (SRF). As a result, optimization of on-chip coils for powering mm-scale neural interfaces features unique design challenges not typically encountered in conventional RFIC design.

This paper presents guidelines for design and optimization of on-chip WPT coils to overcome and alleviate the challenges described above with reporting the results of an on-chip coil optimized for a 100 μW neural interfacing system.

Work supported by the University of California Multicampus Research Programs and Initiatives (MRPI) and the UCSD Center for Brain Activity Mapping.

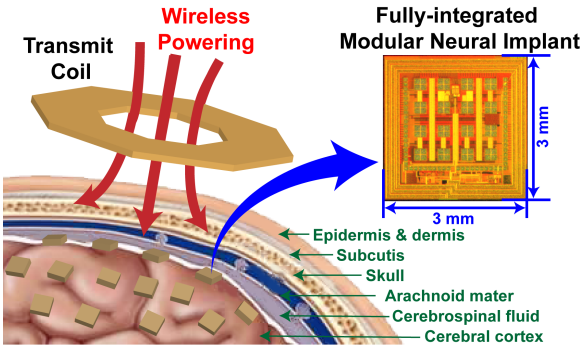


Fig. 1. Overview of fully-on-chip modular neural implants. The inset die photo illustrates the on-chip coil and interior active circuitry.

II. On-chip Coil Optimization

A. Model parameters

Power transfer efficiency in an inductive link is given by:

$$PTE = \frac{k^2 Q_{TX} Q_{RX,loaded}}{1+k^2 Q_{TX} Q_{RX,loaded}} \frac{R_L}{R_L+R_{P,RX}} = \frac{K_{coupling}\eta_{RX}}{1+K_{coupling}\eta_{RX}} \eta_{load} \quad (1)$$

where $Q_{TX} = \omega L_{TX}/R_{TX}$, $Q_{RX} = \omega L_{RX}/R_{RX}$, $Q_{RX,loaded}=\eta_{RX}Q_{RX}$, $K_{coupling} = k^2 Q_{TX} Q_{RX}$, $\eta_{RX} = R_{P,RX}/(R_L + R_{P,RX})$, $\eta_{load} = R_L/(R_L + R_{P,RX})$ and $R_{P,RX}$ is the effective parallel resistance of the RX coil ($R_{RX}(Q_{RX}^2+1)$), assuming capacitors are used to resonate both the transmitter (TX) and receiver (RX) coils [3].

Here, $K_{coupling}$ is largely dominated by the TX and RX coil design and their physical separation, which is difficult to optimize on the RX side under anatomical constraints. Instead, optimizing on-chip coils for mm-scale neural implants is typically an exercise in maximizing $\eta_{RX}\times\eta_{load}$, both of which depend on the load impedance. To illustrate the proposed design procedure, in this paper, a 100 μW load is considered in a total chip area of 3×3 mm^2 with 2.4×2.4 mm^2 of area available for inner active circuitry (Fig. 1).

In this paper, optimization is performed based on 3D Finite Element Method (FEM) simulations using Ansys HFSS v15. Figure 2 shows a cross section of the employed $10\times10\times10$ cm^3 model. All of the tissue layers include frequency-dependent dielectric properties reported in [4]. The RX chip is placed on gray matter (10 mm implant depth) and covered with 200 μm of Parylene C, while the TX is positioned above tissue with various air gap distances (1 to 10 mm).

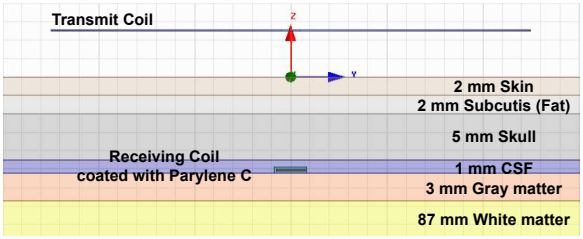


Fig. 2. Cross section of the employed FEM simulation model.

B. Optimizing the number of turns

Figure 3(a) depicts the simulated Q_{RX} of on-chip coils with the varying number of turns in the same layout area, and with a 1:1 width-to-space ratio. Here, fewer turns results in higher Q_{RX}, as resistance increases quadratically with trace length and width, while inductance increases only linearly in the same layout area. This analysis concludes that a single turn coil offers the largest possible $K_{coupling}$.

However, PTE is not determined solely by $K_{coupling}$; η_{RX} and η_{load} are also important, and depend on both the load impedance and $R_{P,RX}$. As illustrated in Fig.3(b), $R_{P,RX}$ increases with the number of turns. In contrast to optimizing $K_{coupling}$, a larger number of turns is desired to achieve a high $R_{P,RX}$ in order to better match to the impedance of a low-power load. These competing trade-offs equalize for various frequencies and load conditions, resulting in an optimal number of turns for maximum PTE. Figure 4 illustrates this for k = 0.005 and Q_{TX} = 250, assuming a 1.6 kΩ AC load that models a 100 μW 0.8 V DC loads, given a rectifier with 50% power conversion efficiency (PCE) and 100% voltage conversion efficiency (VCE) [5]:

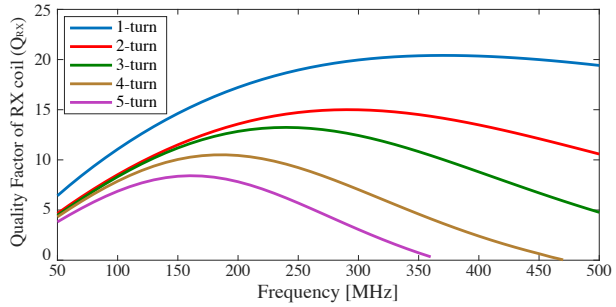
$$R_{AC.load} = \frac{1}{2}\frac{PCE}{VCE^2}R_{DC.load} = \frac{1}{2}\frac{PCE}{VCE^2}\frac{V_{DC.load}^2}{P_{DC.load}}. \quad (2)$$

This analysis shows a 3-turn coil is optimal for a 100 μW neural implant with other specifications described above.

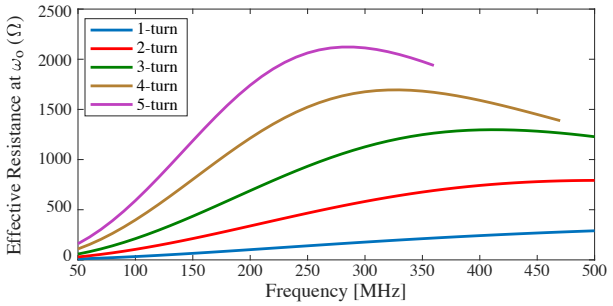
C. Optimizing trace width/spacing

The next step for RX coil design is to size the coil wire width and spacing. Wider trace widths achieve lower resistance but reduce the spacing between turns in a fixed area. Proximity effects between turns result in not only additional effective resistance but also increased parasitic capacitance that reduces SRF, both of which ultimately serve to degrade Q_{RX}. Unlike when optimizing for the number of turns, it is appropriate to try to maximize Q_{RX} when optimizing coil trace/space specifications, as at large load resistances, η_{RX} and η_{load} are not strongly affected by coil trace size. To select optimal trace width and spacing, a parametric sweep was performed in HFSS with 5 μm trace width steps from 60 to 90 μm for a fixed total coil width (280 μm). Representative results from this parametric sweep are shown in Fig. 5. Here, HFSS simulation results suggest an optimal ratio of 30:11 (75 μm : 27.5 μm for Q = 14 at 200 MHz).

Interestingly, a tapered sizing approach where outer turns are wider than inner turns can further improve Q under the same total coil width constraint by minimizing the proximity effect and p-Si substrate losses. To find the optimal tapering rate, a further parametric sweep was performed in HFSS by



(a)



(b)

Fig. 3. (a) Quality factor (Q_{RX}), and (b) effective resistance ($R_{P.RX}$) at resonance for various turn-number configurations.

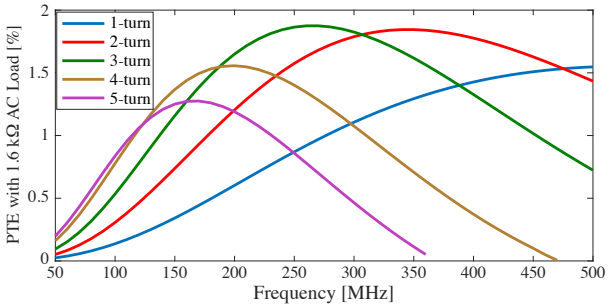


Fig. 4. Power transfer efficiency for k=0.005, and Q_{TX}=250 for AC loads of 1.6 kΩ.

increasing the outer-turn trace with 1 μm steps from 80 to 90 μm, while decreasing the inner trace width by the same amount and maintaining the middle trace width and relative spacing. Simulation results reveal an improved Q of 14.6 for a 10 μm tapering rate with 27.5 μm spacing. Figure 5 illustrates Q of the optimized on-chip coil in comparison to the 1:1 width-to-space 3-turn coil.

D. Internal circuit routing considerations

In fully-on-chip neural implants, the RX coil is typically positioned along the perimeter of the chip to maximize its area and inductance. However, unlike conventional inductors in RFICs, the inner area of the RX coil in fully-on-chip neural implants is filled with active circuitry, electrodes, metalization, etc. [6]. The presence of conductors within the inner area of the coil can potentially adversely affect Q_{RX} (and potentially interfere with sensitive internal analog circuits). Figure 6(a) shows simulated power loss densities of two representative chip implementations with a conventional grid-based internal power distribution and routing scheme (left) and a fractal H-tree-based routing scheme (right). As shown, grid-based routing schemes introduce additional on-chip eddy current

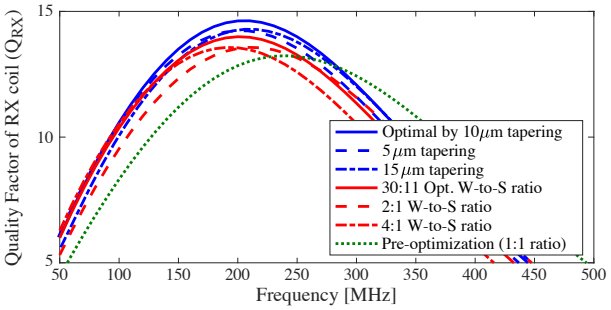


Fig. 5. Optimizing Q_{RX} through trace width/spacing engineering.

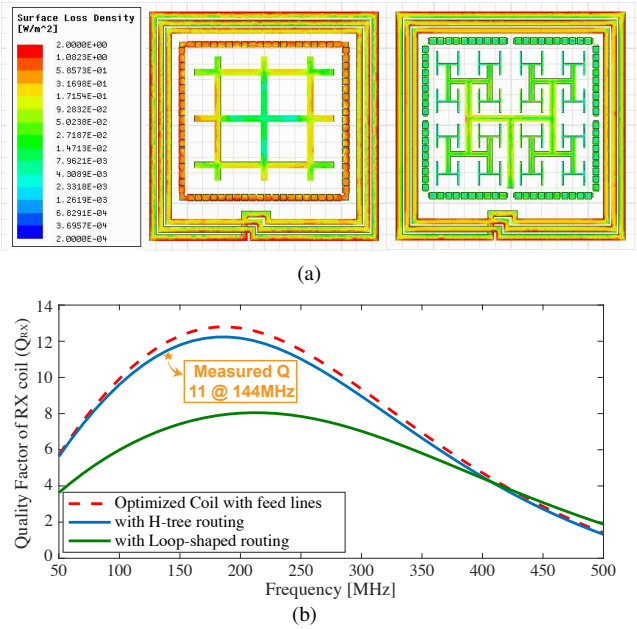


Fig. 6. (a) The loss density on metal surfaces indicating the amount of receiving power from a 1 W transmitting coil and neighboring traces and (b) the Q degradation by inner routing and its measured value of the fabricated IC implementing the H-tree routing scheme.

loops that cause significant additional losses. Figure 6(b) shows how Q_{RX} is degraded from a maximum of 12.8 with no internal routing (including feed line losses), to 8.0 under grid-based routing. To minimize the degradation of Q_{RX}, it is recommended to design on-chip power distribution and routing networks to follow a fractal geometry, to minimize the number of eddy current loops. Measurement results at 144 MHz, chosen not because it is optimal for the RX coil's Q, but rather due to characteristics of the TX coil, reveal a Q_{RX} of 11, validating simulations at that frequency.

III. Transmit Coil Optimization

To maximize PTE, the TX coil should be designed to maximize k^2Q_{TX} at the frequency where the RX coil was optimized. At the frequencies where mm-scale RX coils are optimal (∼100s of MHz), a single-turn TX coil offers superior Q_{TX} compared to multi-turn coils (due to higher SRF), and is thus employed in the following analysis. Generally, k increases with both frequency and TX coil size, until the SRF or for a radius $\sqrt{2}$ larger than the TX-RX coil separation distance, respectively. However, too large of a coil size decreases Q_{TX} at the optimal RX coil frequency. Figure 7 illustrates the effects of this trade-off vis-a-vis PTE, showing an optimal PTE of

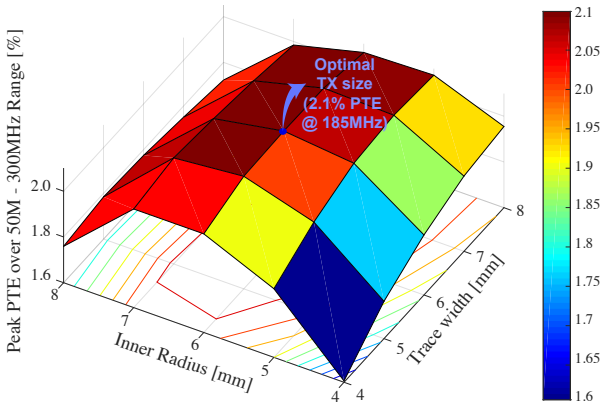


Fig. 7. Transmit coil optimization for 1 oz copper (35 μm thickness) on a PCB, for 15 mm coupling distance (5 mm of air and 10 mm of tissue).

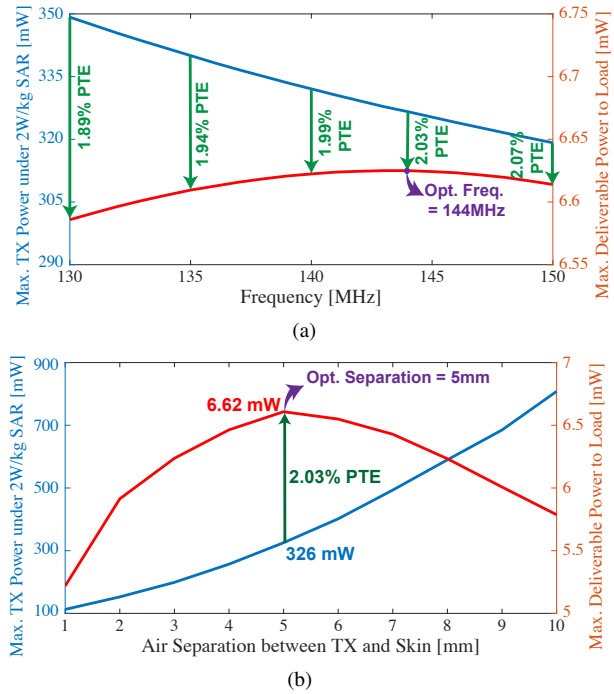
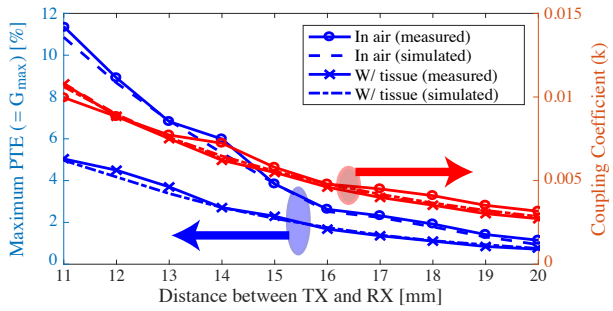


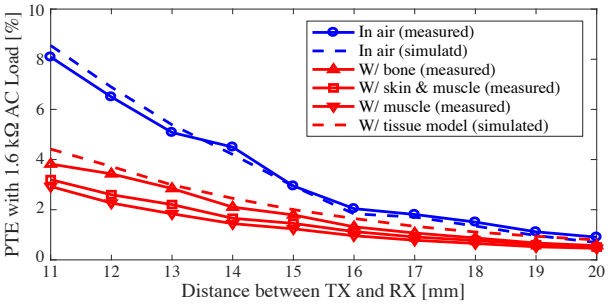
Fig. 8. (a) Operating frequency selection with 5 mm air gap and (b) optimal air separation from tissue when considering SAR at 144 MHz.

2.1% for a 6 mm inner radius and 6 mm trace width at 185 MHz. Here, the proposed octagon-shaped TX coil realizes up to 10.5% PTE improvement over a circular coil.

In high power applications that flirt with specific absorption rate (SAR) limits, it may be beneficial to not necessarily optimize for maximum PTE, but instead for maximum delivered power to the RX under SAR limits. For example, the TX coil described above can transmit more power under SAR limits at lower frequencies, where PTE is deteriorated. As shown in Fig. 8(a), an optimal frequency of 144 MHz balances SAR-limited TX power with PTE to maximize power delivered to the RX load. Interestingly, placing the TX coil away from the skin increases TX power under SAR limits as depicted in Fig. 8(b), yet does so with decreased PTE. In this example, the power delivered to the RX load is maximized for an air separation distance of 5 mm. At an RX load power of 100 μW, it is better to optimize for maximum PTE, as SAR limits are not reached. However, if the implant enters a



(a)



(b)

Fig. 9. (a) Maximum PTE under optimal load conditions, along with estimated k. (b) Measured and simulated PTE with a 1.6 kΩ AC load in air and galline tissue.

constant stimulation mode, where power can be as high (∼mW level), the SAR-informed optimizations described above may be appropriate. Assuming a peak power as high as 6 mW, a 144 MHz frequency was selected in this work.

IV. Measurement Results

In order to validate the described optimization methodology, a 3×3 mm^2 fully-on-chip neural interfacing device and a 24 mm octagonal TX coil were fabricated. WPT measurements were taken with a Keysight E5071C vector network analyzer. To ensure accurate PTE measurements, extensive calibrations and port extensions were performed to de-embed the effects of all SMA connectors and feed lines. Unlike conventional WPT systems, which often estimate important quantities such as k by removing the tuning capacitor and measuring Z-parameters [7], [8], it is difficult to remove on-chip tuning capacitors used in mm-scale neural implants, and thus an alternative analytical technique is required.

The maximum PTE with an optimal load, $PTE_{max.opt.load}$, is defined approximately as $k^2Q_{TX}Q_{RX}/4$ when $K_{coupling}$ is smaller than 1. This is exactly the same as the definition of maximum available gain (G_{max}), and thus k can be estimated by measuring Q_{TX}, Q_{RX}, and G_{max} derived from the following equation:

$$G_{max} = \frac{|S_{21}|}{|S_{12}|}(S - \sqrt{S^2 - 1}), \quad (3)$$

where S is the stability factor derived from S-parameters. Figure 9(a) shows the measured $PTE_{max.opt.load}$ and k results in air, and across 10 mm of galline tissue (with the rest of the coil separation distance occurring in air). Coil Qs were measured separately, revealing Q_{TX} = 416.8 and Q_{RX} = 11 at 144 MHz in air. Since Q_{TX} is severely degraded in the presence of biological tissue, Q_{TX} was measured at every data point in order to estimate k. Simulated $PTE_{max.opt.load}$ based on the models described above agree with all shown measurements to within 0.6 %.

TABLE I. Table of comparisons to recent mm-scale WPT links for implants under in-vitro conditions

Parameters		This work	[2]	[7]	[8]
TX	Type	Oct. PCB	Square PCB	Hex. PCB	Cir. PCB
	Diameter [mm]	24	20.5	24	28
	No. of turns	1	3	1	5
RX	Type	On-chip	On-chip	Wirewound	Wirewound
	Volume [mm^3]	0.036 (3×3×0.004)	0.048 (2×2.18×0.011)	0.785 ($\pi\times0.5^2\times1$)	0.785 ($\pi\times0.5^2\times1$)
	No. of turns	3	4	7	7
TX-to-RX distance [mm]		11† \ 15‡	10	12	12
Tissue thickness [mm]		10	7.5	10	10
Frequency [MHz]		144	160	200	20
AC load [kΩ]		1.6	Optimal	5	0.25
PTE [%]		3.82* \ 1.83	0.8	0.56	1.4
Max. Del. Power (2W/kg SAR) [mW]		5.22° \ 6.62°	Not reported	0.275°	2.75°

Note : † for the maximum PTE and ‡ for the maximum delivered power under 2 W/kg SAR
* 5.04 % with optimal load. ◇ based on HFSS SAR simulation. ○ converted from 1.6 W/kg SAR.

While Fig. 9(a) shows the maximum PTE given an ideal load, Fig. 9(b) shows measured PTE for a more realistic fixed 1.6 kΩ AC load. Here, the WPT achieved 3.82 %, 3.2 %, and 2.93 % PTE at 11 mm WPT channel distance (1 mm air gap, and 10 mm of either galline chest bone or muscle tissue with and without skin). Simulations with the brain implant model described in Fig. 2 achieves 4.25 %. For reference, the WPT link achieved 8.1 % measured PTE and 8.6 % simulated PTE across 11 mm in air.

Table I summarizes the results of this work while contrasting to other recent work on mm-scale implantable coils. As a result of the proposed optimization procedure, the designed on-chip coil WPT link achieved higher PTE than previously-reported on-chip WPT solutions, while achieving comparable PTE to mm-scale wirewound coils.

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