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UNIVERSITY OF CALIFORNIA
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MATERIALS GROWTH AND CHARACTERIZATION OF THERMOELECTRIC AND RESISTIVE SWITCHING DEVICES

A dissertation submitted in partial satisfaction
of the requirements for the degree of

DOCTOR OF PHILOSOPHY

in

ELECTRICAL ENGINEERING

by

Kate J. Norris

June 2015

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Tyrus Miller
Vice Provost and Dean of Graduate Studies

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Abstract

MATERIALS GROWTH AND CHARACTERIZATION OF THERMOELECTRIC AND RESISTIVE SWITCHING DEVICES

by

Kate J. Norris

In the 74 years since diode rectifier based radar technology helped the allied forces win WWII, semiconductors have transformed the world we live in. From our smart phones to semiconductor-based energy conversion, semiconductors touch every aspect of our lives. With this thesis I hope to expand human knowledge of semiconductor thermoelectric devices and resistive switching devices through experimentation with materials growth and subsequent materials characterization. Metal organic chemical vapor deposition (MOCVD) was the primary method of materials growth utilized in these studies. Additionally, plasma enhanced chemical vapor deposition (PECVD), atomic layer deposition (ALD),ion beam sputter deposition, reactive sputter deposition and electron-beam (e-beam) evaporation were also used in this research for device fabrication. Scanning electron microscopy (SEM), Transmission electron microscopy (TEM), and Electron energy loss spectroscopy (EELS) were the primary characterization methods utilized for this research. Additional device and materials characterization techniques employed include: current-voltage measurements, thermoelectric measurements, x-ray

diffraction (XRD), reflection absorption infra-red spectroscopy (RAIRS), atomic force microscopy (AFM), photoluminescence (PL), and raman spectroscopy.

As society has become more aware of its impact on the planet and its limited resources, there has been a push toward developing technologies to sustainably produce the energy we need. Thermoelectric devices convert heat directly into electricity. Thermoelectric devices have the potential to save huge amounts of energy that we currently waste as heat, if we can make them cost-effective. Semiconducting thin films and nanowires appear to be promising avenues of research to attain this goal. Specifically, in this work we will explore the use of ErSb thin films as well as Si and InP nanowire networks for thermoelectric applications. First we will discuss the growth of erbium monoantimonide (ErSb) thin films with thermal conductivities close to or slightly smaller than the alloy limit of the two ternary alloy hosts. Second we consider an ex-situ monitoring technique based on glancing-angle infrared-absorption used to determine small amounts of erbium antimonide (ErSb) deposited on an indium antimonide (InSb) layer, a concept for thermoelectric devices to scatter phonons. Thirdly we begin our discussion of nanowires with the selective area growth (SAG) of single crystalline indium phosphide (InP) nanopillars on an array of template segments composed of a stack of gold and amorphous silicon. Our approach enables flexible and scalable nanofabrication using industrially proven tools and a wide range of semiconductors on various non-semiconductor substrates. Then we examine the use of graphene to promote the growth of nanowire networks on flexible copper foil leading to the testing of nanowire network devices for thermoelectric

applications and the concept of multi-stage devices. We present the ability to tailor current-voltage characteristics to fit a desired application of thermoelectric devices by using nanowire networks as building blocks that can be stacked vertically or laterally. Furthermore, in the study of our flexible nanowire network multi-stage devices, we discovered the presence of nonlinear current-voltage characteristics and discuss how this feature could be utilized to increase efficiency for thermoelectric devices. This work indicates that with sufficient volume and optimized doping, flexible nanowire networks could be a low cost semiconductor solution to our wasted heat challenge.

Resistive switching devices are two terminal electrical resistance switches that retain a state of internal resistance based on the history of applied voltage and current. The occurrence of reversible resistance switching has been widely studied in a variety of material systems for applications including nonvolatile memory, logic circuits, and neuromorphic computing. To this end we next we studied devices in each resistance state of a TaOx switch, which has previously shown high endurance and desirable switching behavior, to better understand the system in nanoscale devices. Finally, we will discuss a self-aligned NbO2 nano-cap demonstrated atop a TaO2.2 switching layer. The goal of this device is to create a nanoscale RRAM and selector device in a single stack. These results indicate that ternary resistive switching devices may be a beneficial method of combining behaviors of different material systems and that with proper engineering a self-aligned selector is possible.

To my grandfather,

Harold Cozad,

Who instilled a love of technology and learning in me while teaching me I could do anything I set my mind to

To Edward Cremata,

Who cheered me on the whole way and sacrificed in the name of science for this thesis

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During my time as a student at UCSC I have been taught by so several and collaborated with many fine persons. I would like to express my appreciation to Dr. Andrew Lohn who took the time to train me in MOCVD and thermoelectric theory, his discussions and brain challenges are appreciated and cherished. Elane Coleman grew all Silicon nanowire samples discussed in this work. Mike Oye has been a consistent supporter.

I am thankful to Dr. Stanely Williams and all of Hewlett Packard Labs for the ability to work alongside some of the best researchers in the nation and be trained in their image. Max Zhang, Xuema Li, Katy Samuels, and Steven Barcelo thought me fabrication techniques and built many samples in this work with me. Jiaming Zhang has graciously trained me in EELS and improved my TEM abilities. Perhaps most of all I learned how to design resistive switches from Dr. Jianhua Yang, a wonderful teacher and mentor.

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The research performed for this thesis would not be possible without my fine co-authors; Andrew J. Lohn, Takehiro Onishi, Elane Coleman, Vernon Wong, Ali Shakouri, Gary S. Tompa, Nobuhiko P. Kobayashi, Junce Zhang, David M. Fryauf, Gary A. Gibson, Steven J. Barcelo, Matthew Garrett, and J. Joshua Yang.

Chapter 1

Introduction

1.1 Thermoelectric Devices

Thermoelectric devices are composed of materials that create an electrical potential when placed under a temperature gradient. This phenomena is caused by a net diffusion of charge carriers from the hot to the cool side as shown in Figure 1.1. The dimensionless figure of merit ZT breaks down the qualities that make good thermoelectric materials, $ZT=S^2\sigma T/\kappa$ where S is the Seebeck coefficient, σ is electrical conductivity, T is absolute temperature, and κ is thermal conductivity. Essentially, for thermoelectric materials to work effectively, the material needs to be a poor thermal conductor but also a good electrical conductor. Metallic materials have desirable electrical thermal conductivity levels however they have high thermal conductivity and therefore are a poor thermoelectric material. Insulators have the opposite problem of natural low thermal conductivity levels as is ideal however their low thermal conductivity levels make them poor candidates. Innately optimizing ZT is a difficult problem as σ and κ are inherently related in a manner not suitable for ideal thermoelectric devices. Therefore semiconductors are the best option for thermoelectric materials, as they can achieve reasonable values of ZT. To compete with the current industry standard, Bismuth Telluride, a minimum ZT of 1 is required[1].

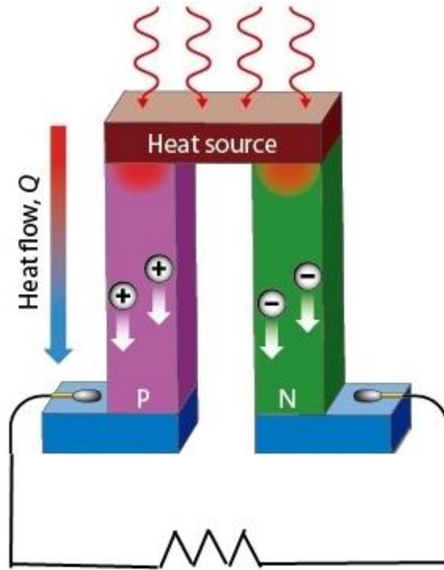

Figure 1.1 Basic schematic of how a thermoelectric device operates.

1.2 Nanowires Networks

Material properties change significantly at the nanoscale. When semiconducting materials are controlled at the nanoscale, the wavefunction describing the charge carriers of the device are confined and an altered density of states is observed. This creates a separation in the energy states of the material making the band gap tunable. Quantum confinement occurs in structures with dimensions comparable to the De Broglie wavelength of their carries, on the scale of tens of nanometers. This correlates to limited motion in the confined dimension(s) with infinite motion in the unconfined dimension(s) introducing quantization of energy states. Therefore quantum wells, or thin films, have one dimension of confinement, nanowires have two dimensions of confinement, and quantum dots have three dimensions of confinement.

Theoretical analysis has been reported to show that the Seebeck coefficient for quantum well (QW) structures increases linearly with decreasing QW thickness. Therefore when the thickness becomes less than a few nanometers based on the assumption that the enhancement of Seebeck coefficient arises mainly from an increase in the density of states near the conduction band edge when the carrier electrons are confined in such a narrow space[2], [3]. It has been shown that due to quantum confinement, nanowires also exhibit a large reduction in thermal conductivity compared with their bulk materials which would considerably increase the dimensionless figure of merit, $ZT=S^2\sigma T/\kappa$ [4], [5]. The reduced dimensions of nanowires cause the scattering of phonons at the surface because charge carriers have much smaller wavelength than the majority of the phonon spectrum. Therefore thin films and nanowires are promising forms of semiconductors for thermoelectric applications.

In the study presented here nanowire networks were strongly considered. Specifically the intersections of nanowire networks are of interest, creating thick mesh like structures. The Boltzmann transport equation (BTE), utilized for transport theory in solids, treats electrons and phonons as particles but overlooks the wave nature with its well known scattering mechanisms [6]. Nanowires can experience strong quantum confinement and have dimensions comparable to the phonon wavelength, especially in nanowire networks with a large number of intersections. Previously it has been suggested that a Coulomb blockade model can explain the electron transport through an intersection [7]. An electron wave can experience a finite reflection at a potential barrier created by a different environment at the fused portion[7] . We hypothesize that

a phonon could also be reflected at the fused portion, as the crystal structure through which a phonon travels may vary suddenly, resulting in a reduction in thermal conductivity at intersections in a nanowire network. Furthermore, if phonons see the intersection as a virtual surface different from a continuous bulk material, surface phonon modes could be excited, which results in many different phonon polarizations than those found in bulk semiconductors[6]. Our current comsol multi-physics modeling described above is purely geometrical, therefore microscopic factors cannot be ruled out in thoroughly describing electrical and thermal properties of nanowire networks. Figure 3 shows transmission electron microscope (TEM) images collected at the center of an intersection where two indium phosphide nanowires are fused. Two fringe directions crossing according to the lattice of the two nanowires prior to fusing can be seen here. There also appears to be some distortion in atomic arrangement. Phonon waves could potentially experience the atomic arrangement distortion at the intersection as the electrons experience the potential barrier. If this is in fact occurring, it could result in decreased thermal conductivity at the intersection.

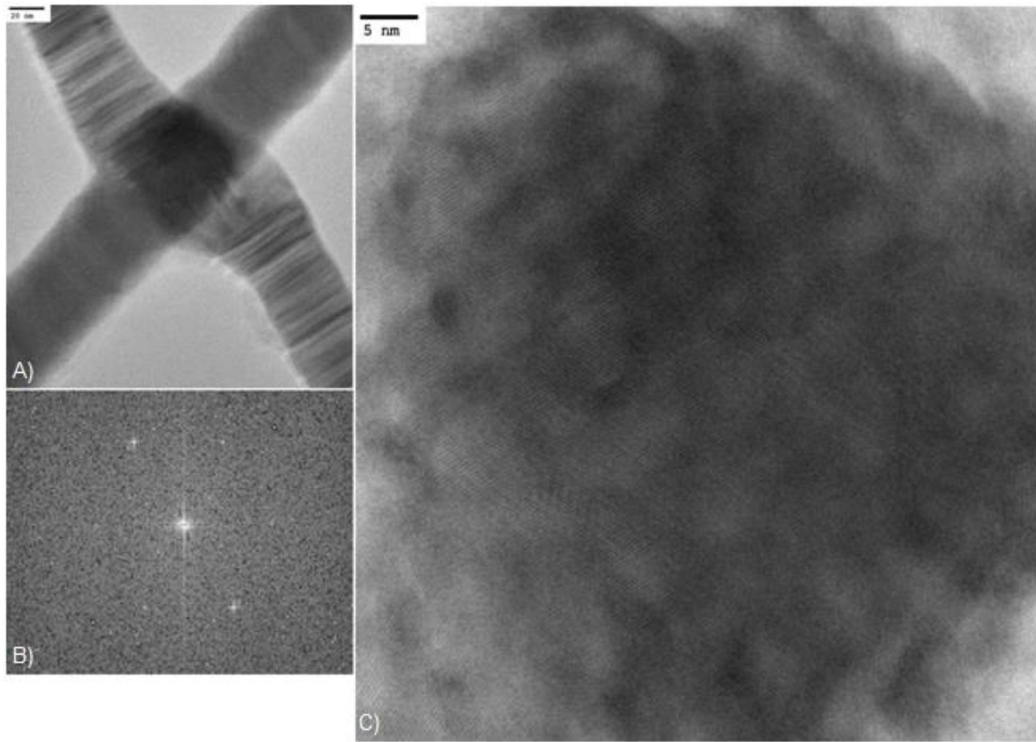

Figure 1.2: A) Lower magnification bright field image of the intersection illustrating the fused quality of the nanowires, B) associated selected area Fast Fourier Transform with points, not rings, indicating a high level of crystallinity, C) Bright field TEM image of a nanowire intersection at higher magnification.

1.3 Metal Organic Chemical Vapor Deposition

Metal Organic Chemical Vapor Deposition (MOCVD) started in 1968-9 with the work of Manasevit and Simpson though the growth of single crystal GaAs on lattice mismatched substrates [8]. MOCVD is an interesting material growth method because it is scalable, economical for high quality semiconductor production, flexible, high purity, and can produce abrupt interfaces. The drawbacks to utilizing this method of growth is the required precursors are expensive and hazardous. Additionally, this method has the most parameters to control, a disadvantage inherent to desirable flexibility.

For the MOCVD growth of III-V nanowires the vapor-liquid-solid (VLS) method was used. VLS is a bottom up method of fabrication requiring a catalyst. Au was used as the catalyst material in our studies. In this process a vapor, the carrier gas with precursor, flows over the surface of the substrate. Once the organic bonds are thermally cracked near the substrate from heat, the metal atoms are free to react on the substrate. A small "diffusion layer" is present over the surface of the substrate causing the precursors to diffuse to the surface of the substrate. The Au catalyst turns to liquid as the substrate is heated and is a preferred site for the vapor to condense, supersaturating the catalyst. Once supersaturated, the nucleation of small clusters within the liquid alloy droplet align with the substrate interface. As the cluster grows out of the droplet forcing the droplet upward with the precipitation of the compound. Generally crystal growth requires a single crystalline substrate as the nanowire will align to the crystallographic direction of the substrate. However, single crystalline substrates are expensive, thick, and inflexible. Therefore, we explore the use of thin film a on flexible metallic substrates to allow the growth of nanowire networks with the requirement that the polycrystalline grains of the thin film exceed the diameter of the nanowires growing aligned with them.

1.4 Transmission Electron Microscopy

Knoll and Ruska first developed Transmission Electron Microscopy as a characterization technique in 1932 [9]. A current heats a filament emitting electrons that are accelerated down the column, then focused by lenses and transmitting through the sample. The electron beam is both transmitted through the thin specimen and

diffracted. The wavelength of the accelerated electrons allow for imaging of a single column of atoms. This creates a diffraction pattern when the Bragg conditions are met. The resultant pattern allows you to determine the material you are imaging as well as which plane of the material we are observing. This is confirmed through fringe spacing. Figure 1.3 a) shows the bright field TEM image of a Si wafer aligned to the zone axis, or the electron beam, while b) depicts the diffraction pattern created by the [100] Si wafer along the [110] zone axis. Image contrast is affected by sample thickness and composition. The heavier, higher atomic number, the material is, the darker it will appear.

The specimen must be thin enough for the electron beam to transmit through the sample limiting the thickness to ~100nm maximum. This requirement makes the sample preparation for TEM experiments time consuming and difficult. The simplest method used in these studies was drop casting of nanowires which were ultrasonicated. To cross section a device for a TEM study an ion beam was used to remove the region of interest and polish it to less than 100nm for viewing. Platinum and Carbon were used as protective layers to prevent the region of interest from ion damage. A cross sectional TEM view of a nanowire or semiconductor device can yield important information about crystal growth and device fabrication. TEM is a useful method when atomic resolution is required. This method can shed light on device behavior and actual structure.

TEM equipment can be equipped with electron energy loss spectroscopy (EELS) measurement tools. EELS is a very powerful form of spectroscopy because it

can take spectra with the same area of a STEM probe, down to ~.5nm in diameter. In EELS the specimen is exposed to the beam of electrons with a narrow range of kinetic energy as it was accelerated at a set energy to form the beam. Some of the electrons will transmit without any interaction and will form the zero loss peak as they have lost no energy passing through the specimen. A strong zero loss peak without secondary peak indicate a good quality, thin specimen, likely around 30nm thick. Some electrons however experience inelastic scattering passing through the specimen, meaning that the electron beam interacts with an electron and lose energy deflecting their path slightly in a random direction. The amount of energy lost in the interaction can be measured by a spectrometer and interpreted to yield extensive information about the specimen. The possible events that an electron can experience correlate to the various regions of the EELS spectra. First the zero loss peak represents the transmitted beam that loss no energy as it did not interact. Then we have the plasmonic region, energy losses up to 50eV that reflect plasmon excitations, resonance of valence electrons, and interband transitions, outershell electron interactions. The shape of the plasmonic region is directly related to the band structure of the material. Finally, we have the core loss region reflecting interactions with inner shell electrons, the excitation to unoccupied higher level shells above the Fermi level creating a characteristic 'edge' of the energy to transition to that shell. The fine structure of the core loss peaks can yield information about bonding. Therefore EELS is capable of measuring atomic composition, chemical bonding, as well as valence and conduction band electronic properties. EELS is most

effective with low atomic numbers where the excitation edges are sharp and relatively easy to measure.

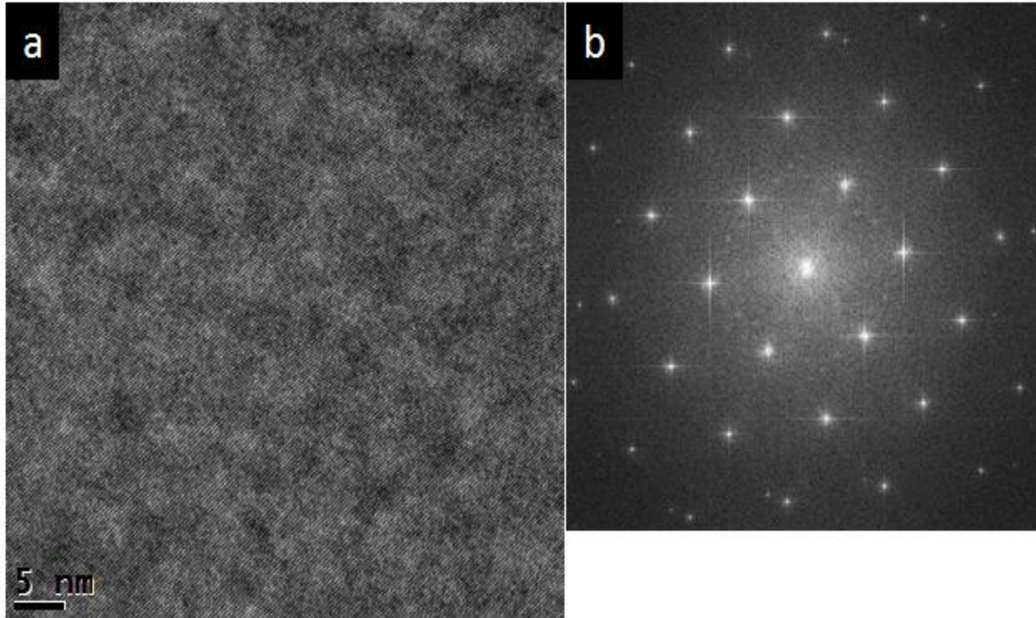

Figure 1.3 a) bright field image of a crystalline Si substrate and b) the diffraction pattern of the Si aligned to the [110] zone.

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Part I Thermoelectric Materials Growth and Characterization

Chapter 2

MOCVD growth of erbium monoantimonide thin film and nanocomposites for thermoelectrics

Kate J. Norris[1,2], Andrew J. Lohn[1,2] ,Takehiro Onishi[1], Elane Coleman[3], Vernon Wong[1,2], Ali Shakouri[1], Gary S. Tompa[3], and Nobuhiko P. Kobayashi[1,2]

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Abstract

We report the growth of erbium monoantimonide (ErSb) thin films on indium antimonide(100) substrates by low-pressure metal organic chemical vapor deposition. The growth rate of ErSb thin films shows strong dependency on the growth

temperature and the Sb/Er precursor molar flow rate ratio. Scanning electron microscopy, energy dispersive x-ray spectroscopy, and x-ray diffractometry (XRD) were employed to study the ErSb thin films grown under the growth conditions that gave the maximum growth rate in the range we investigated. We also report the growth of two types of nanocomposites in which ErSb nanocolumns or nanoslabs with lengths ~500 nm and diameters 20-30 nm are embedded in Zn doped InGaSb (ErSb/InGaSb:Zn) and ErSb nanoparticles with diameters of ~30 nm are embedded in Zn doped InSbAs (ErSb/InSbAs:Zn). These nanocomposites were intended to increase phonon scattering in a mid-to-long phonon wave length range to reduce lattice thermal conductivity. We used time domain thermo reflectance to measure total thermal conductivity for the two types of nanocomposites, and we obtained 4.0 ± 0.6 and 6.7 ± 0.8 W/m.K for the ErSb/InAsSb:Zn and ErSb/InGaSb:Zn nanocomposites, respectively, suggesting that the thermal conductivity was close to or slightly smaller than the alloy limit of the two ternary alloy hosts. The two nanocomposites were further studied with transmission electron microscopy to reveal their microscopic features and XRD to assess their crystalline structures.

Introduction

Demand for green energy has spurred the search for carbon free energy sources by harvesting wasted energy. Thermoelectrics are environmentally friendly power sources under growing investigation that convert a temperature gradient into electric power. The standard guideline of efficient thermoelectric materials search for low-temperature applications is to identify narrow band gap semiconductors with

high carrier mobility [1]. The efficiency of a thermoelectric material is a function of the dimensionless figure of merit ZT, where $ZT=S^2\sigma T/\kappa$; S is the Seebeck coefficient, σ is electrical conductivity, T is absolute temperature, κ is thermal conductivity [2]. A ZT~1 for bismuth telluride, BiTe, alloys near room temperature discovered in the 1950s is necessary for practical applications. However due to the interdependence of the components of the dimensionless figure of merit it has been difficult to achieve a $ZT>1$[3]. To improve ZT, one can increase the power factor, $S^2\sigma$, and/or reduce thermal conductivity, κ. There are various approaches to achieve higher ZT, such as: introducing peaks in the density of states [4], phonon scattering with "guest atoms"[5], one-dimensional nanostructures[3], and superlattices [6]. A record high ZT of 2.65 and a thermal conductivity of 0.031 W/mK was measured for a Bi_2Te_3 single thin layer prepared by laser ablation [7]. Additionally, a ZT of ~2.4 has been reported for a Bi_2Te_3/Sb_2Te_3 superlattice by Venkatasubramanian [6].

We focused on reducing thermal conductivity. Thermal conductivity, κ, is broken into the contribution from lattice vibrations (i.e., phonons) and from charged carriers. The lattice contribution can be suppressed by using the concept of "nanocomposites", semimetallic nanoparticles embedded in an alloy host semiconductor. Recent advances utilizing ErAs semimetallic nanoparticles embedded in an alloy host semiconductor made of one of group III-V compound semiconductors have shown that the lattice thermal conductivity can be reduced to near its theoretical limit[8, 9, 10, 11]. Much remains to be explored in the understanding of phonon transport in nanostructured materials despite attempts [12].

To further enhance the thermoelectric properties of nanocomposites we designed nanocomposites with ErSb nanostructures embedded in two types of alloy host semiconductors; $In_xGa_{1-x}Sb$ and $InSb_{1-y}As_y$. Embedded semimetallic nanoparticles, for instance, can maintain electrical properties and optimize heat transport properties of the host semiconductors by working as mid to long-wavelength phonon scattering sources[13, 14], along with dopants [15]. The thermoelectric power factor ($S^2\sigma$) is also enhanced by nanoparticles [9]. It was also reported that *ZT* increased with the reduction in embedded nanoparticle size [8].

While ErSb has been grown exclusively by molecular beam epitaxy [9, 16, 17], we demonstrated the growth of ErSb by metal organic chemical vapor deposition (MOCVD) on InSb(100) substrates. In our demonstration, ErSb was deposited in the form of either thin films or nanostructures in a host semiconductor as mentioned earlier. Two types of ErSb nanostructures have been identified; nanoparticles and nanocolumns embedded in a host ($In_{1-x}Ga_xSb$ or $InSb_{1-y}As_y$) ternary alloy. Our research has demonstrated the potential of nanocomposites that would reduce thermal conductivity below the alloy limit, practically improving *ZT* and providing a method to grow ErSb-based nanocomposites by MOCVD for a wide range of viable applications.

Experimental Procedure

<u>ErSb thin films on InSb(100) substrates</u>

Low-pressure MOCVD was used to grow ErSb thin films on epi-ready InSb(100) substrates. An InSb(100) substrate was placed on a susceptor held in a reaction chamber made of quartz. The surface of InSb(100) substrate was thermally deoxidized before the deposition of an InSb buffer layer and a subsequent ErSb thin film. The precursors; triethylantimony(TESb) and tris-isopropylcyclopentadienyl erbium (iPrCp 3Er), were carried by purified hydrogen gas to the reaction chamber. The growth temperature, pressure, molar flow rates were 485°C, 180 Torr, $5.58x10^{-5}$ moles/min of TESb, and $1.37x^{-5}$ moles/min of iPrCpEr, respectively. The growth was performed with plasma assisted deposition.

Fig. 2.1 shows the deposition rate of ErSb thin films on InSb(100). As clearly shown in Fig. 2.1, the growth rate of an ErSb thin film was found to be strongly dependent on both the growth temperature and the Er/Sb precursor flow rate ratio. Fig. 2.1 indicates a sharp peak of .0833 nm/sec at a substrate temperature of 485 °C and a precursor V/III molar flow rate ratio of 2.25. An interesting feature is that the deposition rate falls off slower at lower precursor flow rates and higher growth temperatures while reducing faster at higher flow rates. The incorporation of Er on initial InSb surfaces in the high temperature regime in Fig. 2.1 may have been reduced by significant preferential desorption of Sb from InSb expected at temperatures close to the melting temperature of InSb, 527°C. In addition, the growth rate is most likely suppressed at lower precursor ratios because of a deficiency of Sb. Once formed the ErSb should be thermally stable within the growth temperatures investigated in Fig. 2.1 as the melting temperature of ErSb is above 2000 °C.

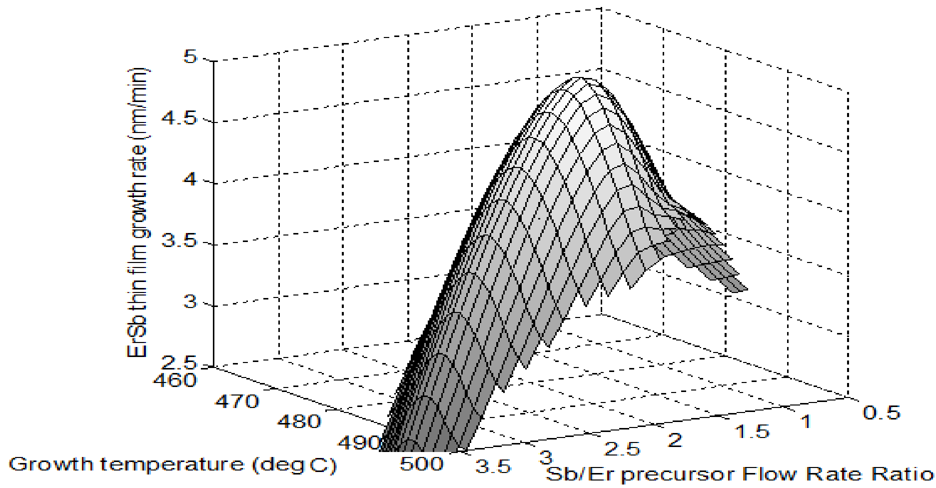

Figure 2.1 - ErSb thin film deposition rate on InSb(100) substrates.

<u>Nanocomposite: ErSb nanostructures embedded in a ternary alloy host</u>

After completing the calibration of ErSb thin film growth, we conducted epitaxial growth of nanocomposites in which ErSb nanostructures were embedded in either Zn-doped InGaSb or Zn-doped InSbAs host grown on InSb(100) substrates by low-pressure MOCVD. For both hosts, MOCVD growths were conducted at a substrate temperature of 485° C and a reactor pressure of 200 Torr. The precursors; trimethylindium, triethylantimony, and triethylgallium were used for the InGaSb:Zn host with molar flow rate ratio of 1.05:1.49:0.92, respectively. The precursors for the InSbAs:Zn host were trimethylindium, triethylantimony, and triethylarsine with a molar flow rate ratio of 1.05:1.49:0.89. Diethylzinc (Zn) was flowed at 1.93×10^{-6} moles/min for both host materials. For both host materials, the erbium precursor, tris-

isopropylcyclopentadienyl-erbium, was injected to the reaction chamber at $1.70x10^{-4}$ moles/min.

Results and Discussion

ErSb thin films on InSb(100) substrates

Even at the highest growth rate, the grown ErSb thin films showed smooth surface morphology. Energy dispersive x-ray spectroscopy (not shown) confirmed that both Er and Sb were present in the thin films as well as the In and Sb from the substrate. The XRD profiles collected from the grown ErSb thin film on an InSb(100) substrate is shown in Fig. 2.2. Based on multiple diffraction peaks present in the InSb(100) substrate and InSb buffer layers, the buffer layers are likely to be polycrystalline, at best, highly-oriented textured films. As indicated in Fig. 2.2, we were unable to index some peaks even though these unidentified peaks did not impact relevant analyses. Two distinct peaks indexed ErSb(422) and ErSb(511) or ErSb(333) indicate that the ErSb thin film has two preferential growth orientations over [100] direction expected for a simple epitaxial growth on InSb(100) substrates. This suggests that the grown ErSb thin film has crystallographic registry with rotated and/or tilted with respect to the substrate as previously reported by Palmstrøm, et al.[18]. The polycrystalline nature of the buffer layer could also explain why ErSb takes on these unusual orientations.

To further investigate the microscopic crystal structure of the ErSb thin film we referred to the structure factor of the rock salt crystal structure to obtain

$F(422)$=280 and $F(511)$=34 [19-20], therefore; the intensity of the ErSb(422) peak should have been $(280/34)^2 = 67.8$ times stronger than the ErSb(511) peak if two types of crystallites having these two planes as preferential orientations had the same volume fraction. In Fig. 2.2, we obtained the ratio of the two diffraction peak intensities; $I(511)/I(422)$ =16670/826= 20.18, then we calculated the ratio of the number of unit cells that would result in the obtained ratio of the diffraction peak intensities. ; $N(511)/N(422)$ ~37 [19]. Therefore the grown ErSb thin film has volume ratio of approximately 97.4 % ErSb(511) majority orientation and 2.6 % ErSb(422). These results indicates that, in an ErSb thin film grown on an InSb(100) substrate, ErSb(511) oriented phases dominate with the small fraction of ErSb(422) phases. In contrast, peaks associated with ErSb(n00) families did not appear in Fig. 2.2 suggesting that the grown ErSb thin film does not have a crystallographic registry typically expected from epitaxial thin films.

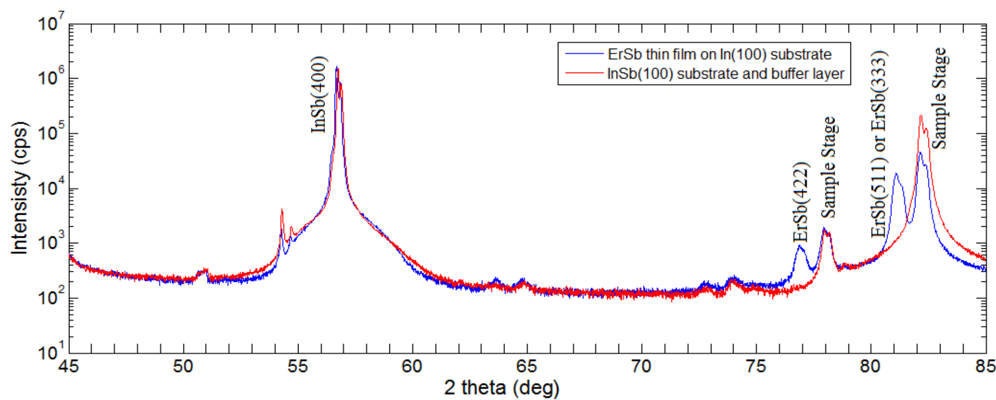

Figure 2.2 - XRD profile of an ErSb thin film grown on an InSb buffer layer on an InSb(100) substrate compared to that of an InSb(100) substrate.

<u>Nanocomposite: ErSb nanostructures embedded in a ternary alloy host</u>

The XRD profiles in Figs. 2.3 and 2.4 were collected from two types of nanocomposites; ErSb/InGaSb:Zn nanocomposite and ErSb/InSbAs:Zn nanocomposite, respectively. Embedded ErSb nanostructures did not appear on the XRD profiles presumably because the volume of each nanostructure spatially isolated from others is too small to make up sharp and intense diffraction peaks. While the grown InSb buffer layer are likely polycrystalline based on the XRD profile in Fig 2.2, it is possible a selection process of a dominant crystallographic orientation can induce epitaxial growth of a subsequent layer during the growth of the InGaAs/ErSb and InAsSb/ErSb nanocomposites[21]. From the (004) and (002) peak shifts in Figs. 2.3 and 4, alloy compositions were obtained for the In_{1-x} Ga_xSb:Zn (x=0.975) and the $InSb_{1-y}As_y$:Zn (y=0.406). There is a possible compositional variation in the InGaSb host material that would be overlaid onto the contrast created by the host and embedded ErSb.

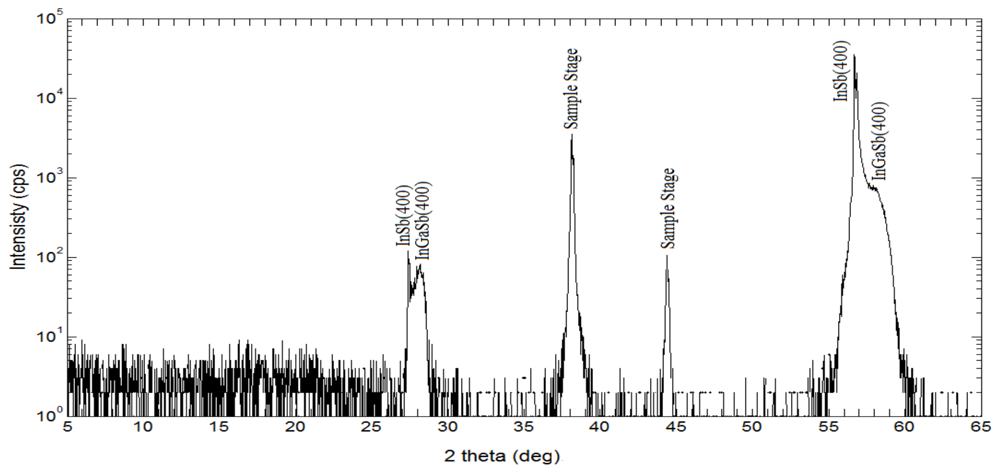

Figure 2.3 – XRD profile of the $ErSb/In_{1-x}Ga_xSb$:Zn (x=0.975) nanocomposite.

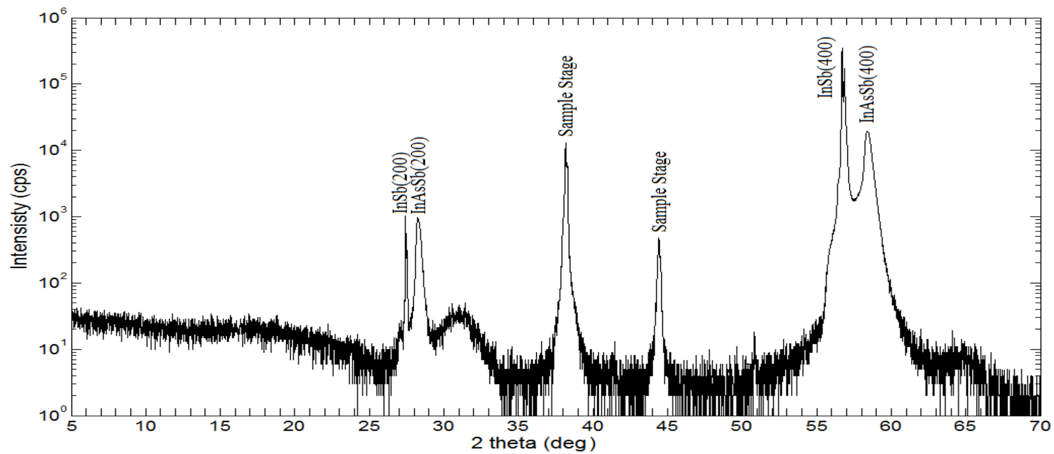

Figure 2.4 – XRD profile of the ErSb/$InSb_{1-y}As_y$:Zn (y=0.406) nanocomposite.

Cross-sectional TEM was used to analyze structural characteristics of the two types of nanocomposites; ErSb/InGaSb:Zn and ErSb/ InSbAs:Zn as shown in Fig. 2.5 and 6, respectively. The TEM images were collected with [110] zone-axis. Fig. 2.5 reveals that a group of 20-30 nm diameter ErSb nanocolumns or nanoslabs formed in the InGaSb:Zn host. These nanometer scale structures seen in Figure 2.5 could be "nanoslabs", long-range periodical structures such as ErSb/InGaSb lateral super lattice, or nanocolumns, or nanocolumns. However the nanocolumn arrangement has been reported elsewhere [22]. Most of the nanocolumns appear to be parallel to each other. This would indicate that the ErSb nanocomposites grew with preference to the InSb(100) substrate's crystallographic orientation. Fig. 2.6 shows a large number of ~30 nm diameter ErSb nanoparticles formed in the InAsSb:Zn host. The nanoparticles appear to be distributed throughout the sample. The formation of ErSb nanoparticles is likely to be spontaneous [8]. Higher concentrations of erbium along with a

relatively high erbium diffusion rate on the surface could have allowed larger ErSb nanoparticles to gradually grow into ErSb nanocolumns [22].

As described earlier, one of the key thermoelectric characteristics that directly influence *ZT* is thermal conductivity of a material. We used time domain thermo-reflectance (TDTR) [23] to determine thermal conductivity of the two types of nanocomposites at room temperature. TDTR measurements provide total thermal conductivity (i.e., the sum of the lattice and the electronic contributions to thermal conductivity). Surface roughness on the Al layers affects the TDTR results through the variation in the Al layer thickness. The Al layers were measured with an acoustic echo in the TDTR measurement. This systematic error is estimated to be ± 5% reflecting the fact that the variation in the Al thickness. Other sources of error include the uncertainties of the laser beam sizes and the layers heat capacities. The thermal conductivities obtained for the ErSb/InSbAs:Zn at room temperature was 4.0± 0.6 W/mK. This is slightly lower than ~5 W/mK obtained for the InSbAs alloy limit at the composition we experimentally examined [24]. We also determined the thermal conductivity of the ErSb/InGaSb:Zn at room temperature to be 6.7 ± 0.8 W/mK, which is slightly higher than the alloy limit of ~5 W/mK [25]. We would have seen observable reduction in the lattice contribution as theoretical predictions expect the nanocomposites to behave as mid to long-wavelength phonon scattering sources [13, 14] if the size of the embedded ErSb nanostructures were appropriately tuned.

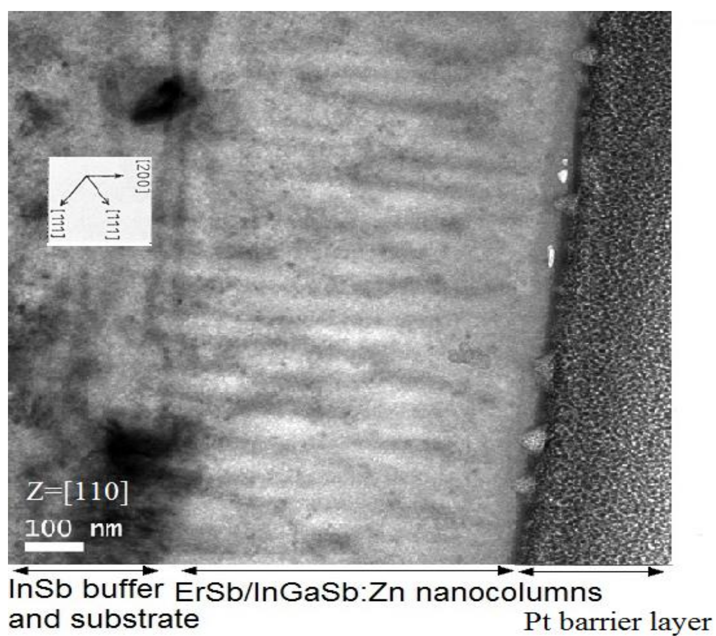

Figure 2.5– TEM image of the ErSb/InGaSb:Zn nanocomposite showing a group of 20 ~ 30 nm diameter nanocolumns or nanoslabs.

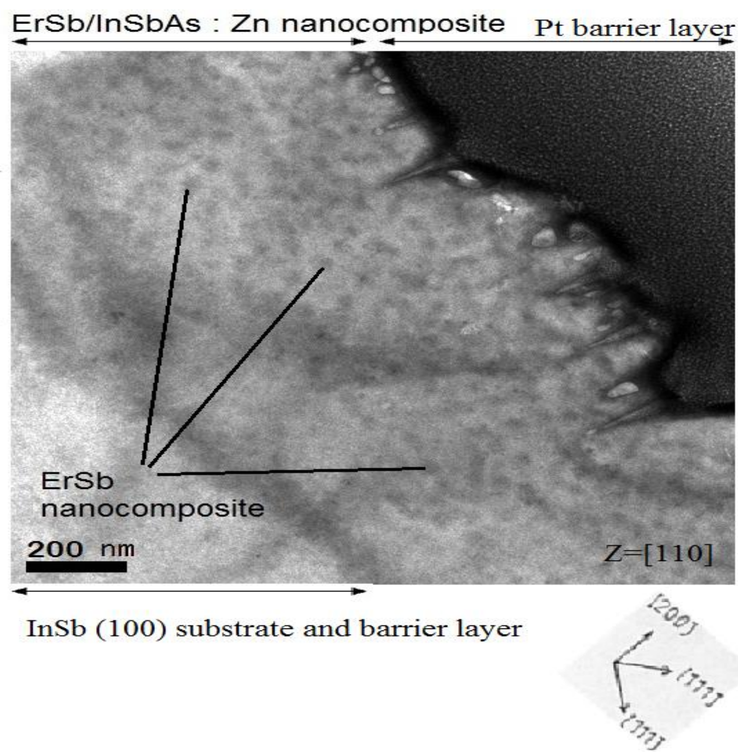

Figure 2.6 – TEM image of the ErSb/InSbAs:Zn showing a large number of 20 ~ 35 nm diameter nanoparticles.

Summary

We demonstrated MOCVD growth of ErSb thin films on InSb(100) substrates. While the EDX analysis confirmed the grown ErSb thin films are made of all expected chemical elements, the XRD profile suggested that ErSb(511) or ErSb(333) phase dominates the thin film. We also demonstrated the growth of two types of nanocomposites; ErSb/$In_{1-x}Ga_xSb$:Zn and ErSb/$InSb_{1-y}As_y$:Zn by low-pressure MOCVD. In the InGaSb:Zn host, the TEM analysis revealed that ErSb grew as nanopillars with ~500 nm length and 20-30 nm diameter almost vertical to the substrate while ErSb nanoparticles with diameter of ~30 nm were identified in the InSbAs:Zn host. The measured thermal conductivities of the two types of nanocomposites showed promising results, however further tuning (e.g., size and volume fraction of ErSb nanostructures) is necessary to validate the concept of nanocomposites within the context of thermoelectric materials and further investigation is required to address specific growth mechanisms that have resulted in the two types of ErSb nanostructures (i.e., nanocolumns/slabs and nanoparticles) depending on the types of hosts.

Acknowledgment

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Chapter 3

Reflection absorption infrared spectroscopy analysis of the evolution of ErSb on InSb

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Abstract

We discuss an ex-situ monitoring technique based on glancing-angle infrared-absorption used to determine small amounts of erbium antimonide (ErSb) deposited on an indium antimonide (InSb) layer epitaxially grown on an InSb (100) substrate by low pressure metal organic chemical vapor deposition (MOCVD). Infrared absorption from the indium–hydrogen (In—H) stretching mode at 1754.5 cm^{-1} associated with a top most surface of an epitaxial InSb layer was used to compare varying levels of surface coverage with ErSb. Among four samples of varying coverage of ErSb

deposition (7.2 to 21.5 monolayers), detected infrared absorption peaks distinct to In—H weakened as ErSb surface coverage increased. In the early stage of ErSb deposition, our study suggests that outermost indium atoms in the InSb buffer layer are replaced by Er resulting in increase in absorption associated with the In—H mode. Using this simple ex-situ technique, we show that it is possible to calibrate the amount of ErSb deposited atop each individual InSb substrate for depositions of few to tens of monolayers.

Keywords: ErSb; InSb; Infrared absorption; MOCVD; AFM; Evolution; Island; Surface coverage

Introduction

Combining nanometer-scale materials of particular chemical composition within a bulk host material of differing chemical composition often leads to unique modifications of the bulk host material's physical properties [1], [2] and [3]. This phenomenon has been especially studied to optimize the thermoelectric figure-of-merit *ZT* – an indicator of thermoelectric material performance – of a bulk thermoelectric material. A material's *ZT* can be enhanced with an increase in electrical conductivity or Seebeck coefficient, or with a decrease in thermal conductivity at a given temperature. Thermoelectric properties of ternary group III–V compound semiconductor host materials such as indium gallium antimonide (InGaSb) and indium antimony arsenide (InSbAs) are expected to be largely improved by embedding nanometer-scale semi-metallic particles such as erbium antimonide (ErSb)

nanoparticles into the aforementioned host materials [2]. The inclusion of these semi-metallic nanoparticles with an appropriate diameter creates desirable scattering centers for mid-wavelength phonons and provides additional charge carriers to the host material [3]. Therefore, the host material's thermoelectric figure-of-merit ZT is enhanced because of decreased thermal conductivity by the reduced contribution from lattice thermal conductivity and increased electrical conductivity at a given doping concentration by supplying additional charge carriers available for conduction. In addition, the Schottky barriers created at the interface between a host material and embedded semi-metallic nanoparticles can be tuned to alter the electron energy distribution around the Fermi level, which can result in an increased Seebeck coefficient [4].

It is predicted that an optimal nanoparticle size and volume density exist where thermal conductivity is minimized and electrical conduction properties of the host material are improved [1]. This prediction illuminates the need for accurate control of the size and volume density of ErSb nanoparticles deposited and formed atop an InSb surface. Unlike molecular beam epitaxy equipped with an in-situ growth monitoring system (e.g., reflection high-energy electron diffraction) that works in ultra-high vacuum, an in-situ growth monitoring system capable of estimating the presence of a small amount of a material on a growth front is not generally available in metal organic chemical vapor deposition (MOCVD). Yet, the great success in growing high-quality III–V compound semiconductors by MOCVD is indisputable. Therefore, we explore an ex-situ calibration technique, reflection absorption infrared

spectroscopy (RAIRS), based on glancing-angle infrared-absorption used to collect information on vibrational modes of chemical species that make up a surface and to obtain the amount of a small quantity of ErSb delivered onto InSb surfaces. RAIRS has proven to be a particularly useful technique in catalyst surface characterization for its ability to evaluate surface vibrational modes and resolve closely positioned absorption peaks due to high spectral resolution [5]. Metal nanoparticles such as Au supported by Al_2O_3, SiO_2, FeO (111), CeO_2, and TiO_2 thin films have been extensively studied with great success using RAIRS [6]. In addition to RAIRS, atomic force microscopy (AFM) is also used to further evaluate the surface morphology and concentration of ErSb nanoparticles formed on the InSb surface.

Experiment

When exposed to vapor phase chemicals, solid surfaces can serve as a growth platform for crystal formation. ErSb deposited atop an InSb surface forms ErSb nanoparticles largely due to thermodynamic differences in the enthalpy of formation between the two materials [7]. Four samples with four different amounts of ErSb deposited on InSb surfaces were made on InSb (100) substrates by low-pressure MOCVD [8] and [9]. Prior to ErSb deposition, a 500 nm unintentionally doped InSb buffer layer was grown on an InSb(100) substrate, creating a smooth surface that served as a growth platform for ErSb deposition. Tris(isopropyl-cyclopentadienyl) erbium and trimethyl-antimony were used for the growth of ErSb on the InSb buffer layer. Shown in Fig. 3.1 is a deposition rate of ErSb plotted against temperature and

molar flow rate ratio between Sb and Er precursors. The figure shows a deposition rate peak of 4.9 nm/min at a temperature of 485 °C and precursor molar flow rate ratio of 2.25. Fig. 1 clearly shows that the ErSb deposition rate is very sensitivity to both temperature and molar flow rate ratio. The peak deposition rate shown in Fig. 3.1 was used for each of the four samples hosting different amounts of ErSb deposited on the InSb buffer layer. By varying the ErSb growth time, each sample yielded a specific amount of deposited ErSb ranging from 7.2 to 21.5 monolayers (ML).

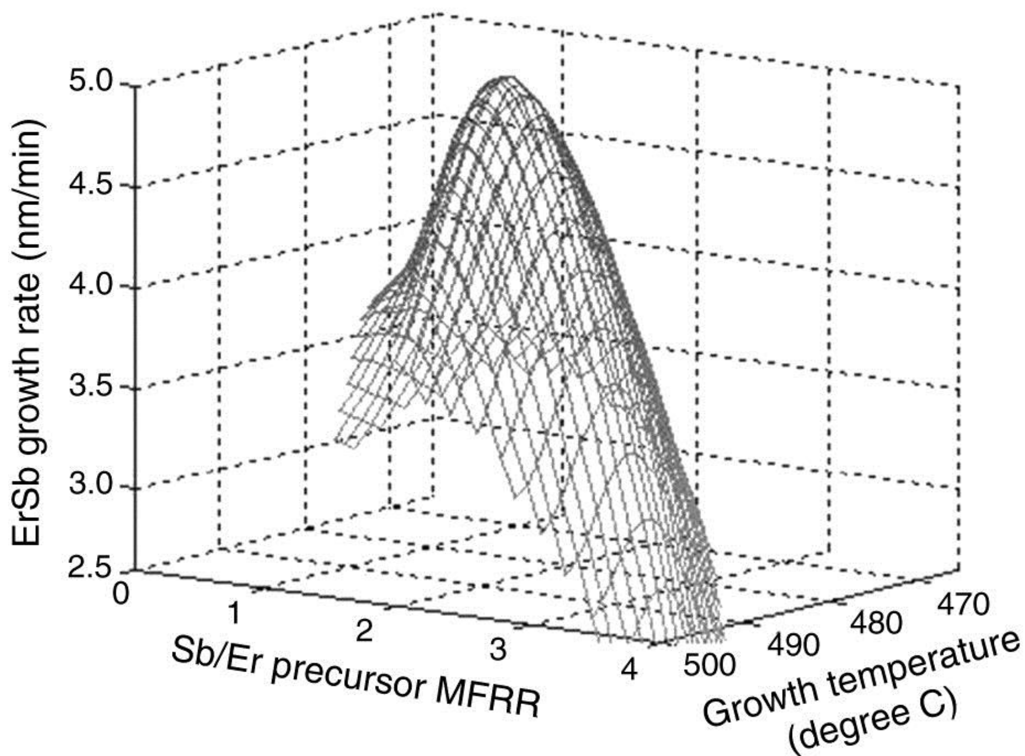

Figure 3.1. The deposition rate of ErSb on InSb(100) surfaces plotted as a function of deposition temperature and the Sb/Er precursor molar flow rate ratio (MFRR). A peak deposition rate of 4.9 nm/min was obtained at 485 °C and molar flow rate ratio at 2.25.

Fig. 3.2 illustrates the configuration of our RAIRS measurement. An infrared beam is collimated onto the surface of the sample at an approximate incident angle of 8°. A portion of the emitted infrared beam is absorbed by the vibrational modes associated with In—H bonds present on InSb surfaces partially covered by ErSb deposition. The remaining unabsorbed incident infrared light is reflected and collected by a detector. Detection of the reflected infrared spectrum reveals absorption peaks characteristic to the stretching mode of exposed In—H bonds present on the surface of the InSb buffer layer. In our RAIRS measurement, absorption spectra were obtained with respect to a reference sample that provided a surface of an InSb buffer layer without ErSb, therefore the RAIRS spectrum collected from the 0 ML sample shows no spectroscopic features associated with In—H bonds.

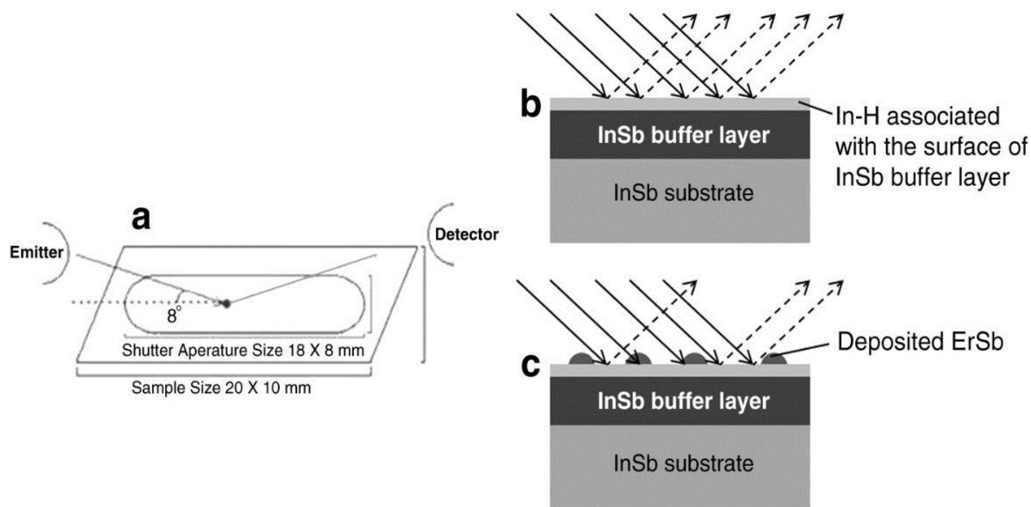

Figure 3.2. (a) Reflection absorption infra-red spectroscopy (RAIRS) configuration. (b) and (c) Schematics showing that an increase in surface coverage of ErSb results in

a decrease in the number of detected In—H bonds exposed on the InSb buffer layer surface.

Results and discussion

Considerable amounts of hydrogen and hydrogen radicals are present in our low-pressure MOCVD growth environment. This is, in particular, expected because we use rather low V/III ratio, 15/1, for the growth of InSb in contrast to typical growth conditions for group III-arsenide and –phosphide for which much higher V/III ratio is used. Prior to ErSb deposition, In—H surface bonds are formed and characterized by their distinct vibrational modes. These vibrational modes are capable of infrared absorption in the 1660–1682 cm^{-1} range reported for hydrogen-terminated indium phosphide (InP) surfaces [10] and 1754.5 cm^{-1} range reported for the In—H stretching mode of InH_3[11]. Based on this information, we studied chemical and morphological evolution of the surface of the InSb buffer layers upon ErSb deposition.

Fig. 3.3 shows RAIRS spectra obtained from the four samples with different growth times at a given deposition rate as calibrated in Fig. 3.2. Each sample is covered with a specific amount of ErSb ranging from 7.2 to 21.5 ML. In Fig. 3.4, the peak absorption intensity is plotted as a function of ErSb deposition showing linear correlation between these two quantities based on the trend seen in the range of ErSb deposition of 7.2–21.5 ML. It is apparent in Fig. 3.3 that as the amount of deposited ErSb increases and covers the InSb surface, the RAIRS absorption peaks associated

with the In—H bonds decrease. This simple picture, however, does not appear to describe the evolution from 0 ML (i.e., the reference sample) to 7.2 ML ErSb sample. As mentioned earlier, our RAIRS measurement is a comparative measurement done on the four InSb surfaces covered with different amounts of ErSb using an InSb surface with 0 ML ErSb deposition (i.e., the reference sample). If we assume that the surface of the reference sample was completely occupied by In—H bonds, the In—H absorption on the 7.2 ML ErSb sample would have shown reduced absorption, in other words, in our RAIRS measurement, the absorption of the 7.2 ML ErSb sample should have been recorded as "negative" absorption. Therefore, the positive absorption of the 7.2 ML ErSb sample seen in Fig. 3 suggests that the number of In—H bonds on the 7.2 ML ErSb sample is indeed larger than that on the reference sample. Qualitative description for the evolution from 0 ML to 7.2 ML ErSb sample is as follows; under our specific growth conditions, the surface of the InSb buffer layer (i.e., the reference sample with 0 ML ErSb) is covered predominantly with antimony. It is also highly likely that a small number of In—H bonds coexist. The heat of formation of Er—Sb and In—Sb is − 286.8 kJ/mol and − 34.1 kJ/mol, respectively [12] and [13], thus, upon the deposition of 7.2 ML ErSb, at least during the early stage of ErSb deposition, there is a strong thermodynamic driving force for indium atoms in the InSb buffer layer being replaced by Er to form ErSb. This replacement process creates more free indium atoms available to form additional In—H bonds on the 7.2 ML ErSb sample leading to the "positive" absorption as seen in Fig. 3. Further deposition of ErSb results in complete coverage of the InSb buffer

layer and the number of In—H bonds that participate in the absorption decreases as nominal thickness of ErSb increases. Also notable in Fig. 3.3 is the capability of RAIRS to clearly distinguish a 2.3 ML difference of deposition between a 9.5 ML ErSb sample and 7.2 ML ErSb sample.

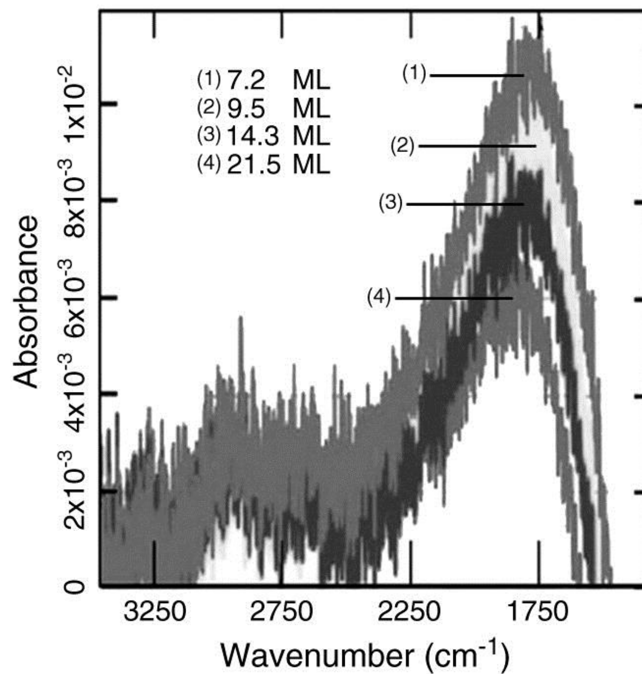

Figure 3.3. RAIRS spectra of the four samples with varying coverage of ErSb on In—H terminated InSb surfaces. Detected infrared absorption peaks distinct to the In—H stretching mode at 1754.5 cm^{-1} weakened as ErSb surface coverage increased.

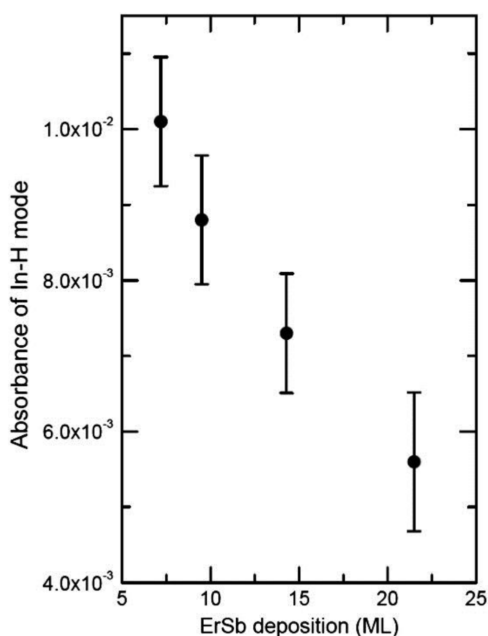

Figure 3.4. Peak absorbance at 1754.5 cm^{-1} of In—H vibrational mode plotted as a function of ErSb deposition.

To further assess the small amount of ErSb deposition profiled by the RAIRS experiments, we evaluated the samples by atomic force microscopy (AFM). The two samples representing the upper and the lower bounds of ErSb deposition range we studied; 7.2 ML (a) and 21.5 ML (b) are shown in Fig. 3.5. Clearly seen are ErSb islands covering the surfaces of the InSb buffer layers. Surface coverage of ErSb was also obtained by AFM and plotted in Fig. 3.6. Extrapolating to 0 ML does not seem to traverse 0%, which may indicate the significance of the replacement process occurring between erbium and indium as described earlier. The 7.2 ML sample surface is approximately 29% covered and the 21.5 ML sample surface is approximately 55% covered. These AFM results are qualitatively consistent with the

RAIRS results and further qualify RAIRS as a competent ex-situ calibration technique for evaluating the deposition of few to tens of ML surface coverage.

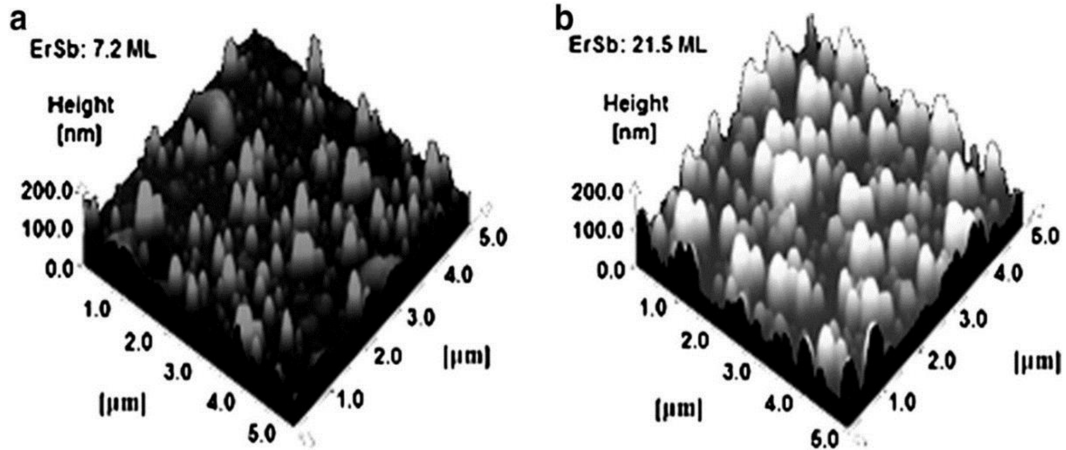

Figure 3.5. AFM images collected on two of the samples with varying coverage of ErSb on In—H terminated InSb surfaces. ErSb covers approximately 29% of the InSb surface for the 7.2 ML sample (a) and approximately 55% of the InSb surface for the 21.5 ML sample (b).

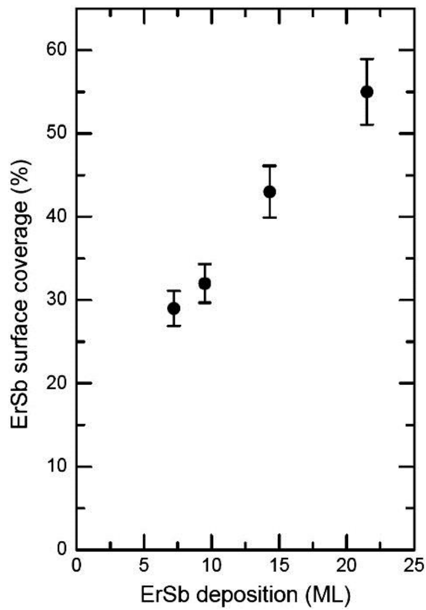

Figure 3.6. ErSb surface coverage on the InSb buffer layer.

RAIRS offers two main advantages over alternative characterization techniques. First, it can be performed in non-vacuum environments since it is an optical technique. Second, even at adsorption as low as 0.01%–2%, the RAIRS signals associated with the number of surface adsorbing molecules is generally recorded at relatively high resolution using modern FTIR spectrometers. Also, while the technique is not surface-specific, it can be shown theoretically that the best sensitivity for IR measurements on metallic surfaces is obtained using grazing-incidence reflection of the IR light [5]. Our studies take advantage of these benefits of RAIRS and use the reflection IR technique to measure mono-layer amounts of ErSb on In—H terminated InSb surfaces. The technique can also be used to measure mono-layer amounts of materials other than ErSb deposited on similar surfaces, making material deposition rates of differing materials easy to compare.

Summary

In developing enhanced thermoelectric materials with embedded nanoparticles, it is necessary to monitor the size and volume density of grown nanoparticles. An optimal nanoparticle size and volume density may exist where the figure-of-merit *ZT* of the host thermoelectric material is optimized. Therefore, we discuss an ex-situ monitoring technique based on glancing-angle, infrared-absorption called RAIRS used to measure the amount of ErSb nanoparticles deposited atop InSb substrates. After exposing the surface of the InSb substrates to a shallow angle infrared beam, we

detected distinct absorption peaks associated with In—H surface bonds found on the substrate surface before and after ErSb deposition. The difference in the absorption peaks measured before and after ErSb deposition revealed the amount of ErSb deposited atop the substrate surface. We used AFM to visualize the surface topology of the InSb substrates with grown ErSb nanoparticles. Results from both RAIRS and AFM correlated well with one another, qualifying RAIRS as a competent ex-situ monitoring technique for evaluating the deposition of mono-layer amounts of ErSb on In—H terminated InSb surfaces.

Acknowledgments

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Chapter 4

Nanoimprint Lithography based Selective Area Growth of Indium Phosphide Nanopillar Arrays on Non single-crystal Templates

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ABSTRACT

Selective area growth (SAG) of single crystalline indium phosphide (InP) nanopillars was demonstrated on an array of template segments composed of a stack of gold and amorphous silicon. The template segments were patterned by UV nanoimprint lithography on a silicon substrate covered with a natural oxide, and the SAG was achieved by metal organic chemical vapor deposition. Our SAG is different from conventional SAG in one critical aspect. In our SAG, growth of InP takes place selectively on a pre-defined array of template segments made of non-single crystal materials on a foreign substrate. The grown InP nanopillars were

studied for their structural, chemical and optical properties. The new SAG process is not limited to the specific materials such as InP nanopillars and silicon substrate used in this demonstration; our approach enables flexible and scalable nanofabrication using industrially proven tools and a wide range of semiconductors on various non-semiconductor substrates.

Keyword: A3. Metalorganic chemical vapor deposition; A1. Nanostructures; B1. Oxides; B2. Semiconducting III-V materials

Introduction

Arrays of semiconductor nanostructures fabricated by selective area growth (SAG) have gained interest as a platform for many applications [1-3]. Conventional SAG of semiconductor thin films achieved by growing materials within openings pre-defined by a mask on a single-crystal semiconductor substrate was demonstrated decades ago [4]. Conventional SAG has further evolved and is currently used for growing semiconductor nanostructures [5]. Two limitations of conventional SAG of semiconductor nanostructures are: (1) a single-crystal semiconductor substrate is required for epitaxial growth and (2) semiconductor nanostructures grown in an array are epitaxially connected to a single-crystal semiconductor substrate[5]. These two aspects restrict the choice of nanostructure and substrate materials and the design of devices that employ these nanostructures [6-8]. Use of single-crystal semiconductor substrates in conventional SAG rules out device fabrication on glass or metal substrates. To address this issue, a group has used a poly-Si substrate with a Silicon

dioxide mask to produce nanowires in selected areas to reduce the need for a single crystal substrate[9]. Furthermore, the fact that nanostructures in an array are all connected to a single-crystal substrate makes it difficult to electrically access a specific nanostructure within the array. In this paper, we present a new type of SAG of semiconductor nanostructures. Our SAG process is unique in that growth of nanostructures is initiated on an array of template segments formed on non-single crystal foreign substrates. Our SAG approach on non-crystal substrates could open the door for many applications not feasible through the conventional SAG. For example, individual nanostructures fabricated on an array of metallic template segments on an insulator substrate can be individually electrically addressed through the associated metallic template segment. Also, our method uses only proven, cost effective industrial techniques: nanoimprint lithography and metal organic chemical vapor deposition (MOCVD).

Experiment

Figure 4.1 illustrates the steps for growing an array of nanopillars on template segments. For this demonstration we chose three materials, silicon (Si) with native oxide, a stack of gold (Au) and amorphous silicon (a-Si), and indium phosphide (InP) for non-single crystal substrate, template segment, and nanopillar. The substrate preparation process utilized UV nanoimprint lithography (NIL) to transfer a pattern of template segments to a polymeric reverse tone mold using a custom-designed nanoimprint machine [10]. A four inch wafer mold was used to template the substrate with 130-150 nm diameter segments in a repeating hexamer pattern, as seen in Figure

2a. The NIL process depicted in Figure 4.1 is summarized as follows: (a) a mask is made on a four inch silicon wafer using deep UV lithography - this mask is subsequently used to make a daughter mold by NIL as shown in (b); (c) the daughter mold is used to imprint the array pattern into UV resist prepared on a PMMA layer based on the bilayer structure model [11] on a Si substrate with native oxide; UV irradiation forms a polymer mask shown over the PMMA. The UV resist is then etched using Reactive Ion Etching (RIE) to expose the pattern in PMMA, as shown in (d). A second RIE step removes the PMMA revealing the pattern on the substrate as shown in (e). Next, a layer of a-Si with a nominal thickness of 10 nm followed by a layer of Au with a nominal thickness of 5 nm are deposited by electron beam evaporation at normal incidence to form the a-Si/Au template segments in (f) and an acetone lift off process is used to leave the a-Si and Au segments, as shown in (g). Because the patterns can be precisely defined by the initial deep UV lithography and reproduced faithfully by NIL, an array of the template segments with an arbitrary geometrical pattern can be fabricated uniformly over a large area. Figure 1(h) illustrates the InP nanopillars grown from the a-Si/Au template segments. The processes described in Figure 4.1 were implemented on a four inch n-type silicon (100) wafer. A native silicon dioxide layer (~1.5nm thick) was intentionally left on the wafer, to allow later release of the InP nanopillars from the Si substrate, if desired, and to inhibit InP growth outside of the a-Si/Au template segments. While the native oxide suppressed the growth of InP in unwanted regions, it is certainly possible a small amount of InP was deposited in these regions. Metal organic chemical vapor

deposition (MOCVD) was used to grow InP nanopillars on the template segments. Typical growth conditions were; growth pressure 75 torr, V/III ratio of ~5 and temperature 505°C. The precursors for the MOCVD growth were ditertiary butylphosphine (DTBP) and trimethylindium (TMIn) at molar flow rates of 40.12 $x10^{-5}$moles/min) and 8.34x*10^{-5}moles/min, respectively, for 20 minutes.

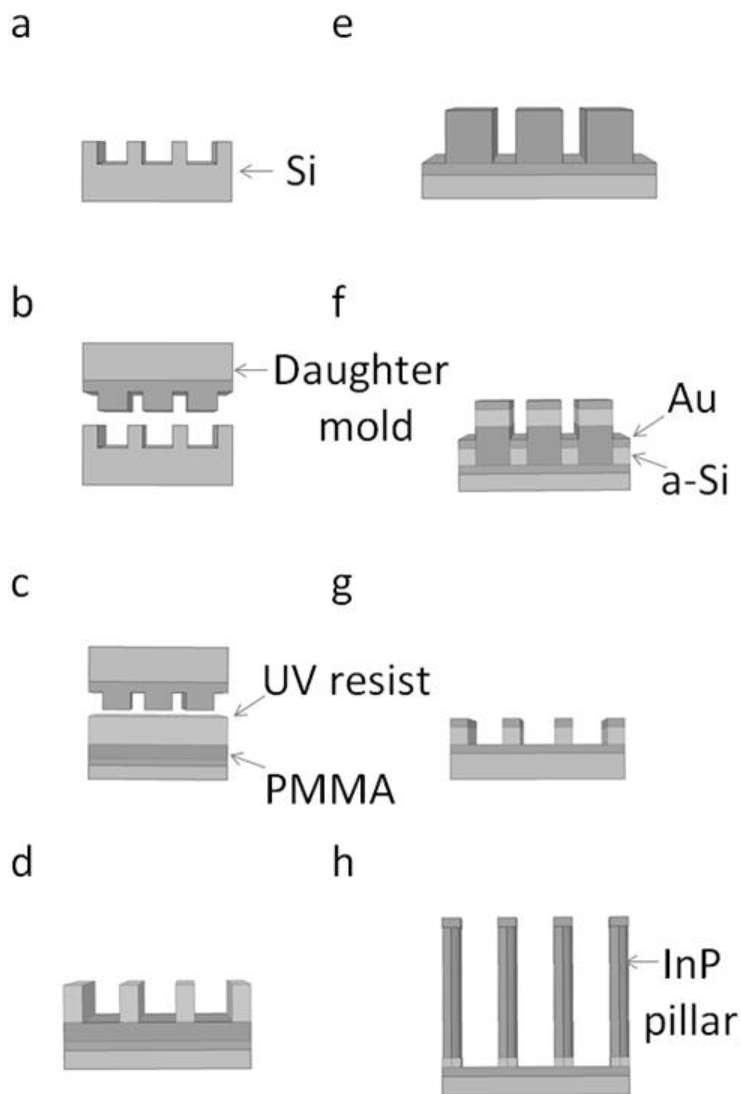

Figure 4.1: Fabrication procedure for the nanopillars: (a) The fabrication of the nanopillar array silicon mold using deep UV lithography. (b) The making of the daughter mold using nanoimprinting, (c, d) The fabrication of the seed layers from the polymer d The fabrication of the seed layers from the polymer daughter mold using nanoimprinting. (e) the negative of the array pattern in pmma is left to (f) deposit the seed layer for growth using e-beam deposition, 10nm of amorphous Silicon and 5nm of gold, shown after lift off in (g). (h) After the substrate preparation shown in a-g the InP pillars are grown by mocvd.

Results and Discussion

Figure 4.2 shows scanning electron microscope (SEM) images of representative InP nanopillars. Figure 4.2(a) shows InP nanopillars grown out of an array of hexamer clusters of a-Si/Au template segments and illustrates the consistency achieved. Shown in Figure 4.2(b)-(e) are magnified images of the pillars in different stages of growth. Figure 4.2(b) depicts the beginning stage of a nanopillar in the form of a circular cone with gold on top. Next a spherical tip begins to develop in 4.2(c), and expands in 4.2(d), which continues until the pillar resumes vertical growth with nearly constant radius as in 4.2(e). The majority of fully developed pillars shown in Figure 4.2(e) are ~300 nm in length with an average maximum diameter of ~140nm, of which the diameter can be tuned by controlling the size of the template segments [5]. The nanopillar height is a reflection of growth time and parameters, should a longer nanopillar be desired a longer growth time or an increase in temperature should be employed.

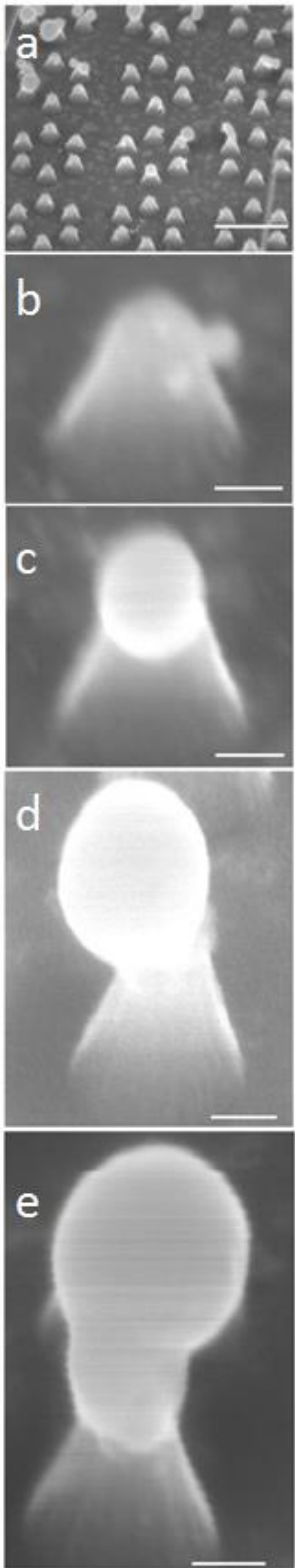
a
b
c
d
e

Figure 4.2: Scanning electron microscope (SEM) images of indium phosphide nanopillars grown by MOCVD a) showing the repeating pattern, scale bar is 500nm, and b-e) showing the progression of pillar growth, scale bar is 50 nm.

Elemental chemical analysis of the pillars via energy dispersive x-ray spectroscopy (EDX) performed in the SEM, not shown here, confirmed that indium and phosphorus are two dominant elements and that a small amount of Au is present. In addition to the EDX measurements, it is also found that the nominal volume of the deposited Au for a single template segment is roughly that of the measured volume of Au at the tip of a single pillar seen in the SEM images, therefore, the SAG of nanopillars on a-Si/Au template segments appears to progress via Au catalysis as in the vapor-liquid-solid (VLS) mode[12]. It is worth pointing out that the dimension of the a-Si/Au segments (130-150nm in diameter) is much larger than typical sizes of Au catalysts (~10nm in diameter) used in our past experiments [13-20], except when doped with boron[21], and even larger than seen in other's VLS mode at 50 nm [22], indicating that the VLS mode can operate at a large length scale when growth is geometrically confined as in the case of our SAG. It should be noted however, that the relationship of the pillar size and tip size is dependent on the growth parameters. We would merely like to note that with this beginning template size and growth parameters, a large length scale was seen for the VLS growth mode.

To assess the crystallographic properties of the nanopillars, we performed x-ray diffraction (XRD) as shown in Figure 4.3. In Figure 4.3, the black and grey lines represent a Si substrate with an array of a-Si/Au template segments without and with InP nanopillars, respectively. Wide and narrow range scan profiles are shown in

Figure 4.3(a) and (b), respectively. The difference between these two profiles is small overall, and is only noticeable when looking at the section shown in Figure 4.3(b). This is probably because the total volume of nanopillars involved in the XRD profile is ~$1.4x10^{15}$ nm^3, which is approximately equivalent to an 18nm thick film if spread over the area of the x-ray beam, making it difficult to detect in XRD measurement. In addition, unlike an epitaxial thin film, it is highly likely that the nanopillars do not have a specific crystallographic registry with respect to the Si (100) substrate, making them more difficult to detect in our XRD measurement.

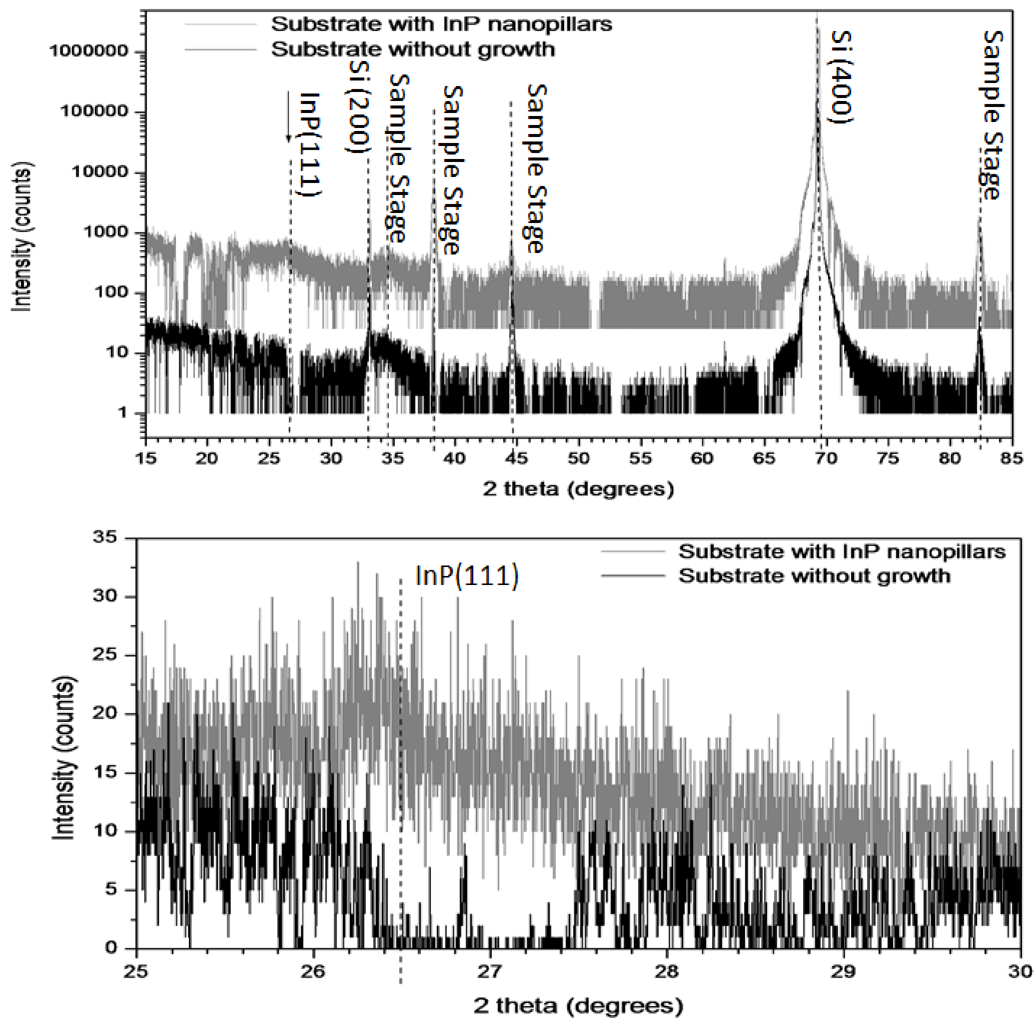

Figure 4.3: (a) X-ray diffraction profiles of a substrate with indium phosphide nanopillars and an as-prepared substrate by NIL prior to MOCVD growth. (b) a closer look at scattering angles where the substrate with indium phosphide nanopillars differs from the as- prepared substrate.

The presence of the small broad peak in the InP nanopillar sample at ~26.2 degrees seen in Figure 4.3(b) is most likely associated with InP (111) indicating that the (111) plane is dominant. The growth of the InP nanopillars in our experiment cannot simply be viewed as ordinary epitaxial growth from a substrate because the substrate is not single-crystal, but rather it is characterized by the a-Si/Au template

segments that intrinsically develop random crystallographic orientation as they crystallize through heat treatment during the growth of the InP. Typical III-V nanowires grow along the direction perpendicular to the lowest energy plane[23], which is generally the (111) plane. In our case, it is likely that the a-Si crystallized at a reduced temperature due to metallic impurities. This then initiated InP(111) growth, and is consistent with the observation that many of InP nanopillars grew nearly vertically with respect to Si(111)[24,25]. The amount of silicon that would need to crystallize is negligible as in principle the nucleation of a nanowire only requires short range crystallographic order and the template that provides this order can have a significantly different lattice constant[26,27].

Cross sectional transmission electron microscopy (TEM) was performed to examine the interface between an InP nanopillar and an Au/a-Si template segment as well as the structure of the pillar. Figure 4.4 shows cross-sectional TEM images of a nanopillar from the same sample shown in Figure 4.2. Figure 4.4(a) shows the entirety of the pillar examined here. In a series of sample preparation processes, a 2µm thick Pt was deposited utilizing a gallium ion beam as a protection layer on top of a 10nm carbon coating. The ion beam was held at 30kV and 27pA for cleaning of the sample at a 1.8° tilt to remove the damaged top layers for both surfaces to achieve a final thickness below 100 nm. This process was performed on a FEI Nova Nanolab dual beam system. The darker sections seen within the tip of the pillar indicate the presence of elements with higher atomic numbers suggesting non-uniform distribution of the Au in the tip. The diameter of the spherical tip is much larger than

that of the “neck" formed between the tip and stem. This feature is unique to our SAG pillar growth - the size of the metal catalyst is typically comparable to that of the nanowire in conventional VLS growth processes.

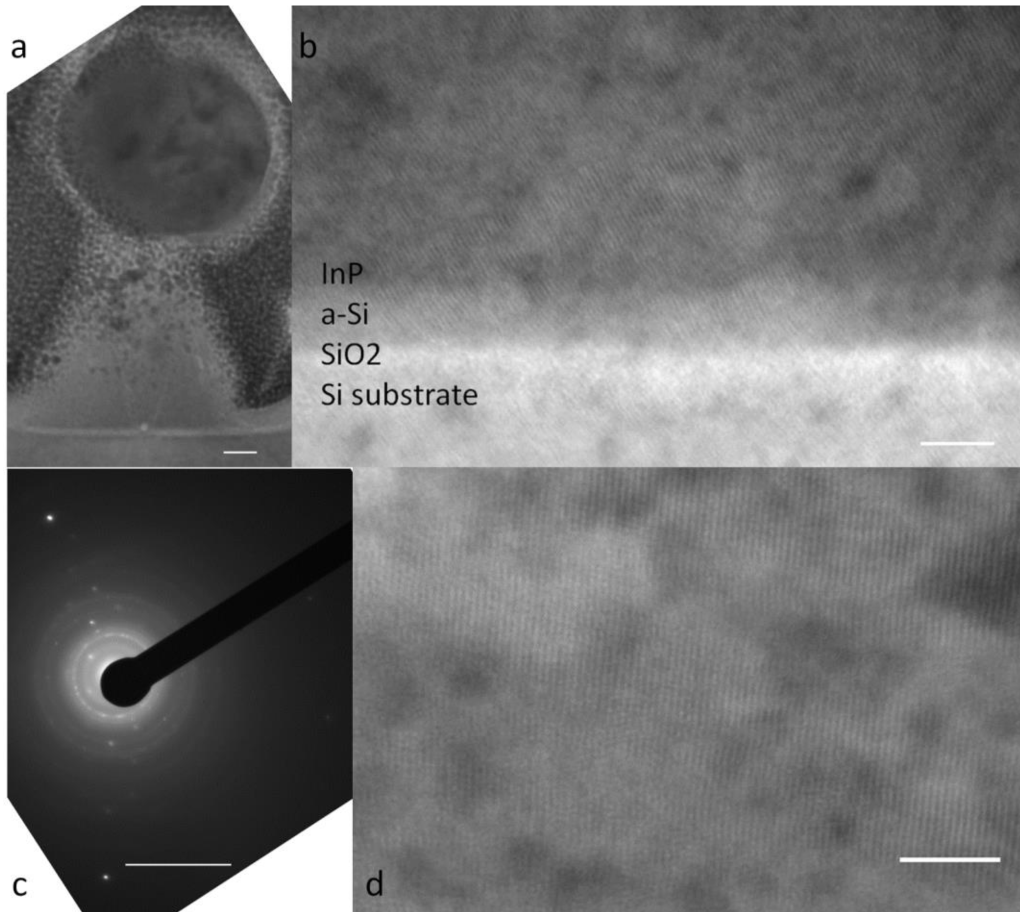

Figure 4.4: (a) Bright field transmission electron microscopy of InP nanopillars as seen in Figure 2, the scale bar is 20 nm. (b) Bright field of the interface between the substrate and growth, the scale bar is 5nm (c) Selected area diffraction shows single crystallinity of the silicon with the diffraction spots directly below the beam stop and indium phosphide to the left and to the bottom right of the beam stop while the rings show the polycrystallinity of the platinum protection coating. The zone axis appears to be [011] and the scale bar is 1nm Dif (d) BF TEM images of the fringes present in the InP further along the pillar that were aligned with the bottom fringes, the scale bar is 1nm. The spots correspond to the platinum protection layer surrounding the InP pillar that was cross sectioned.

Figure 4.4(b) shows a magnified image of the interface between the a-Si template segment and the pillar. The silicon substrate, a ~1.5 nm native oxide layer, an a-Si layer, and InP are seen. The original a-Si layer appears to have partially crystallized, most likely due to heating during the MOCVD InP growth process as observed previously [24,25]. The measured thickness of the remaining Silicon layer is ~4nm which is significantly less than the original 10nm and a reduction in layer thickness is consistent with the a-Si layer undergoing partial crystallization. The glass transition temperature of a-Si has been estimated to be ~1266K, which is much higher than our MOCVD growth temperature [28]. However we believe that the transformation from 10nm a-Si occurred through multiple processes; crystallization to form 4nm Si (111) and the incorporation of some Si atoms into the Au-In-P droplet used in nanopillar vertical growth through the VLS mode. Apart from the crystallization of the a-Si layer, the Au-Si system is known to form an eutectic alloy with an eutectic temperature of 363°C [29] well below the MOCVD growth temperature. Furthermore, Si atoms loosely bound to the Si layer would migrate through Au even at temperatures lower than the eutectic temperature and form Au silicide. The structure of Si-Au template segments that undergo the MOCVD growth needs to be further investigated to address how InP nucleates on the template.

As Figure 4.2 and 4.4(a) indicate, the tip consisting of Au, In and P that drove the growth of the pillars through the VLS growth mode, which would indicate the a-Si layer thinned as Si atoms were incorporated in the Au-In-P tip. Figure 4.4(b) also reveals that the InP took the same crystal direction as the silicon seed layer through

the fringes seen here. Figure 4.4(c) shows a selected area diffraction (SAD) pattern collected from the interface shown in (b). The SAD pattern indicates that there are two single crystalline components co-existing within the selected area based on the distances between diffraction spots. Analysis on the SAD pattern identified two different sets of diffraction spots that were overlaid; that of Si and of InP, which are presumably associated with the silicon substrate and InP nanopillar, respectively. The rings are related to the polycrystalline platinum protection coating that surrounds the pillar and not intrinsic to the sample. Figure 4.4(d) is a magnified image of (a) that shows fringes running continuously throughout the InP pillar suggesting that it is in fact epitaxial growth of InP on crystallized a-Si although the role played by the Au-In-P spherical tip is not clear at this point. The spacing of the fringes confirms that the zone axis is the [011] of a f.c.c. lattice. Therefore we believe that the a-Si formed a Si (111) crystal seed for the nanopillar formation through the vls growth mode, where the Au layer became an Au droplet taking with it a small amount of Si.

Optical properties of the InP nanopillars were characterized by photoluminescence (PL). PL spectra were collected over 2cm x 2cm area on the samples to ensure consistent results, which indicates that combining NIL and MOCVD SAG has a potential of offering a uniform material platform over a large area. A 532nm CW laser of 6.7 mW, with a nominal spot size of ~2mm diameter was used to excite the samples at room temperature. Figure 4.5 displays the collected PL spectra from an template area of growth clearly showing that the InP nanopillars grown on the array of a-Si/Au template segments are optically active while also showing the PL emission

from an area of growth without templates that is not optically active, therefore indicating that any InP growth in this area is not optically active or is below our detection capabilities. The peak emission wavelength is ~893nm which corresponds to a 1.389eV, approximately 50meV larger than that of a bulk InP, 1.344eV. This is consistent with the finding that blue-shifts in the range of 50meV to 110meV are found depending on geometrical and strain level of an ensemble of nanowires, influencing bad gap energy as well as the location of radiative recombination[30] When one compares lattice fringe spacing at the base of the nanopillar with that within the nanopillar further away from the base, as shown in Figure 4a and 4b, respectively, it is found that there is an approximately 6% relaxation toward the tip. The strain relaxation suggests the presence of non-uniform strain field along the nanopillar and the strain is expected to be largest at the bottom of the pillar where InP conforms to the Si lattice, compressing the lattice at the bottom of the nanopillar whereas further along the pillar, the lattice relaxes to that of bulk InP. It has been shown elsewhere that PL is very sensitive to strain and that growing InP on Si can cause a significant blue-shifts due to large lattice mismatch[31]. Also that the strain in an InP nanowires can cause blue shifts of this magnitude[32]. The large FWHM of the PL peak would also indicate that radiative recombination is occurring over the nanopillars as the strain is released and associated bandgap continuously changes [31] .

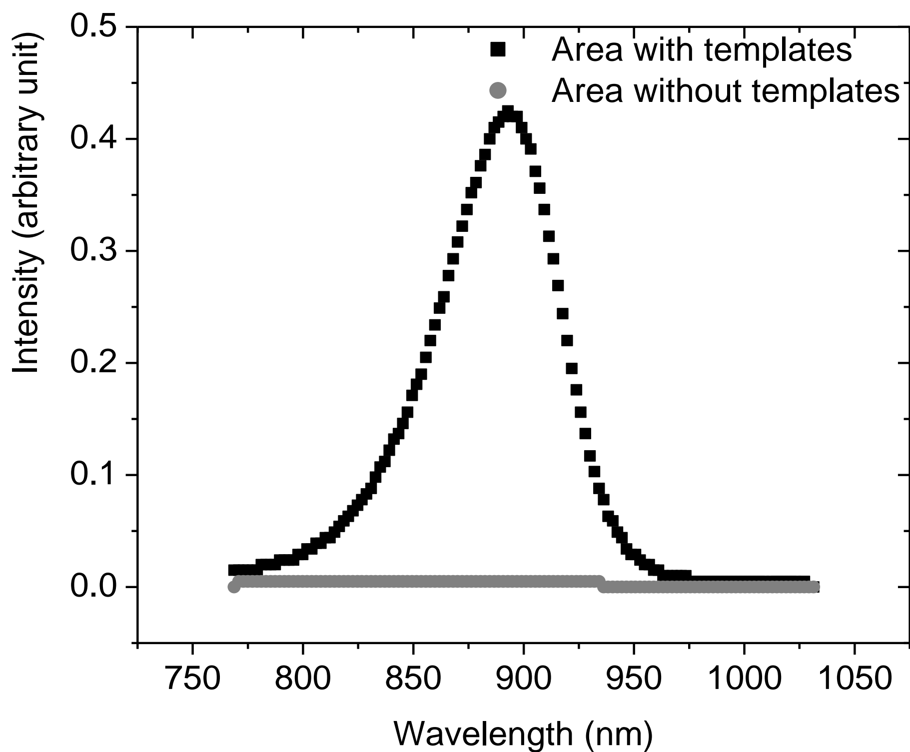

Figure 4.5: Room temperature photoluminescence of the InP nanopillars and the substrate with no templates to compare any substrate contribution.

Conclusion

We have demonstrated an unique SAG to grow InP nanopillars on an array of a-Si/Au template segments. The templates were created through UV NIL and the nanopillars were grown by MOCVD. The growth progression for a nanopillar from the template was shown along with TEM showing the crystallinity of the pillars continues along the entirety of the structure starting from the crystallized Silicon seed layer. (111) directionality was difficult to detect by XRD due to the small volume equivalent to a thin film ~18 nm thick, however all data points to growth in this

direction. Our SAG technique allows for precise control on location of nanometer-scale semiconductor single-crystals while enabling the use of non-single crystal substrates that are often low-cost.

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Chapter 5

Graphene Mediated Growth of Polycrystalline Indium Phosphide Nanowires and Monocrystalline-Core, Polycrystalline-Shell Silicon Nanowires on Copper

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ABSTRACT

Two types of semiconductors, indium phosphide (InP) and silicon (Si), were separately grown on polycrystalline copper foils with the presence of gold colloidal particles. InP was grown with and without carbon deposition by metal organic chemical vapor deposition, and Si was grown with and without plasma enhanced chemical vapor deposition of carbon. While InP and Si grew as films on untreated copper foils, they were found to grow in the form of nanowires when copper foils were pre-treated with carbon. Structural analysis revealed that the grown InP nanowires were polycrystalline. In contrast, the grown Si nanowires were found to

have core-shell structures with a monocrystalline core and a polycrystalline shell. Further analysis suggested that graphene was formed on the copper foils during the carbon deposition. Therefore, we concluded that the presence of graphene promoted the growth of InP and Si in the form of nanowires. The demonstration of growing semiconductor nanowires on copper foils could be a new path to integrate semiconductor and metal to provide a unique material platform for a wide range of devices.

Keywords: MOCVD, indium phosphide, silicon, copper, polycrystalline, nanowire, graphene

Introduction

There are many potential applications, such as optoelectronic and thermoelectric devices, which would benefit from utilizing low cost metallic substrates, such as flexible metal foil substrates, for the growth of semiconductors. Aluminum and copper, for instance, are low cost materials with excellent electrical and thermal conductivity, making them suitable electrode materials for devices. Heteroepitaxial growth of metal on semiconductor surfaces has been extensively studied to develop high performance electrodes [1] although it is also been demonstrated that polycrystalline, rather than single-crystal, metal films simply deposited on semiconductor surfaces serve as acceptable electrodes [2,3]. In contrast, growth of semiconductor materials directly on metallic surfaces has been limited to non-single crystal (i.e., polycrystalline and amorphous) semiconductor films, [4,5] presumably

because of the lack of demand for epitaxially grown single-crystal semiconductors on metallic surfaces. For this reason, even emerging semiconductor nanostructures such as quantum dots and nanowires are almost exclusively grown on single-crystal semiconductor substrates, [6,7] with a few exceptions demonstrated on non-single crystal semiconductor surfaces [8,9,10]. InP nanowires grown using copper seeds have been demonstrated, however, the demonstration involved a single crystalline InP substrate [11]. New demonstrations were recently reported, in that, graphene enabled epitaxial growth of InAs nanowires on copper and InGaAs nanowires on MoS_2 surfaces [12,13].

One of the main fields that would benefit from the growth of semiconductor nanostructures, such as our nanowires on polycrystalline copper, is thermoelectric devices. One of the key reasons for designing semiconductor nanowire thermoelectric devices is to utilize the electron transport properties of nanowires to maintain a preferred electrical conductivity via quantum effects, i.e., ballistic transport [14,15]. More importantly, rough surfaces of nanowires allow the scattering of phonons, therefore reducing thermal conductivity, which is another important aspect to increasing thermoelectric efficiency [16,17]. In fact, phonon scattering has proven so essential to thermoelectric efficiency that polycrystalline materials, which scatter phonons with a much higher efficiency than that in monocrystalline materials, show promise as a viable thermoelectric material platforms [18,19]. In polycrystalline materials containing grains with various size ranging from 3nm to 1μm, phonons with a wide range of wavelengths may be scattered efficiently, therefore increasing

thermoelectric efficiency [19]. Additionally, grain boundaries can scatter phonons [20]. From these preliminary demonstrations and design considerations, we concluded that it is logical to use polycrystalline materials in the form of nanowires for thermoelectric devices, in order to combine the benefits provided by both polycrystalline films and nanowires to achieve maximum phonon scattering.

In this study, InP and Si were chosen to further study graphene's role in promoting the growth of semiconducting nanowires, including group IV semiconductors. In pursuing the growth of semiconductors on metallic surfaces, our study explores a method to grow semiconductors in the form of nanowires on polycrystalline copper foils, using graphene as an intermediate layer. InP nanowires are entirely polycrystalline while the Si nanowires have monocrystalline-core polycrystalline-shell structures. These material platforms could offer unique benefits to engineer thermal and electrical conductivity for thermoelectric devices.

Experiment

Four samples were prepared on mechanically flexible, non-single crystalline copper (Cu) foils, two of which were used for InP growth and the other two were for Si growth. The preparation of the two InP growth samples consisted of one Cu foil with carbon deposition and the other without carbon deposition. A Cu foil was cleaned with acetic acid, rinsed with DI water, and dried in air. Subsequently, carbon deposition was conducted by annealing the Cu foil in hydrogen at 990℃ and 270 mTorr for 20 minutes followed by flow of methane/hydrogen mixture for 10 minutes,

also at 990℃ and 270 mTorr. Following the carbon deposition, the Cu foil was allowed to cool in hydrogen, and then it was purged with argon before removal from the carbon deposition reactor. Another Cu foil was rinsed with acetone, isopropanol, methanol, rinsed in DI water, and dried in air. The two Cu foils, one with and the other without the carbon deposition, were further coated with Au colloidal nanoparticles with nominal diameters of 10 nm by drop casting and allowed to dry in air. Metal organic chemical vapor deposition (MOCVD) was used to deposit InP on the two Cu foils. The MOCVD growth conditions for InP were a growth time 20 minutes at 300 Torr, 550°C, and a 4.3 V/III molar flow rate ratio. The precursors were ditertiary butyl phosphine (DTBP) and trimethylindium (TMIn).

The preparation of the two Si growth samples also consisted of one Cu foil with carbon deposition and the other without carbon deposition. Two Cu foils were cleaned with acetic acid, rinsed with DI water, and dried in air. Subsequently, one Cu foil underwent the carbon deposition described earlier. Following the carbon deposition, the Cu foil was allowed to cool in hydrogen then purged with argon before removal from the reactor. The other Cu foil did not undergo the carbon deposition. The two Cu foils, one with the carbon deposition and the other without it, were coated with colloidal gold. Plasma enhanced chemical vapor deposition (PECVD) was utilized to deposit silicon. The PECVD for Si included a pre-growth annealing process performed at 400℃ for 5 min in hydrogen, which was followed by a nanowire growth step at growth temperature of 500°C. Disilane (Si_2H_6) hydrogen

mixture was used as the silicon precursor and the flow rate was 10 sccm with a reactor pressure of 0.3 Torr and a growth time of 15 minutes. After the growth, the reaction chamber was evacuated and the sample was cooled to 50℃ in argon.

In summary, we have four samples in total in this experiment; InP with carbon on Cu, InP without carbon on Cu, Si with carbon on Cu, and Si without carbon on Cu. All four samples, InP on Cu foils with/without carbon deposition, and Si on Cu foils with/without carbon deposition, were characterized by various analytical tools including scanning electron microscopy (SEM) and energy dispersive x-ray spectroscopy (EDX), transmission electron microscopy (TEM), Raman spectroscopy, and x-ray diffraction (XRD).

Results and Discussion

The Cu foils prepared with the carbon deposition were characterized prior to semiconductor (i.e., InP and Si) growth using Raman spectroscopy, in order to determine the nature of the grown carbon layer. Figure 5.1 shows the Raman spectrum taken from the Cu foil that underwent the carbon deposition. Two peaks marked with "G" and "2D" are clearly seen and identified as two types of vibrational modes [21,22,23], suggesting the presence of graphene on the Cu foil. The "2D" mode appears to be sharper and more intense than the "G" mode indicating that the graphene is a single layer [24].

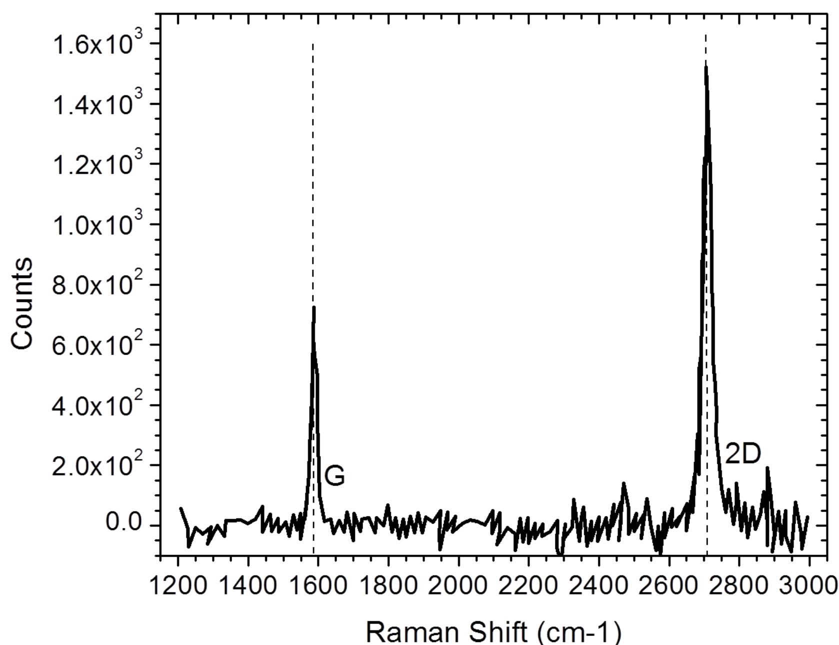

Figure 5.1. Raman spectroscopy data taken on the carbon-treated copper substrate, showing the distinct graphene peaks, G and 2D with the background PL signal removed.

Figure 5.2 investigates the InP growths using SEM. The SEM image shown in Figure 5.2a, taken from the InP sample deposited on the Cu foil without carbon deposition, shows that a granular film was grown. The EDS confirmed that the grown film is composed of stoichiometric InP. While InP grew as films on Cu foils without a graphene intermediate layer, InP grew as nanowires only on the Cu foil with a graphene intermediate layer, as seen in Figure 5.2b-d. Multiple nanowires appear to form from a central location in Figure 5.2b. EDS indicates that their elemental composition consists of indium and phosphorus with a chemical composition approximately stoichiometric InP. Figure 5.2b demonstrates that a high

density growth of InP nanowires can be grown on polycrystalline Cu foils by using a graphene intermediate layer. The image highlighted in Figure 5.2c shows details of the rough surface morphology of the grown InP nanowires. A rough morphology of nanowires has been shown to reduce thermal conductivity, which is advantageous in thermoelectric applications [16]. The image shown in Figure 5.2d depicts a nanowire at its early stage of development with an Au metallic cap at the tip.

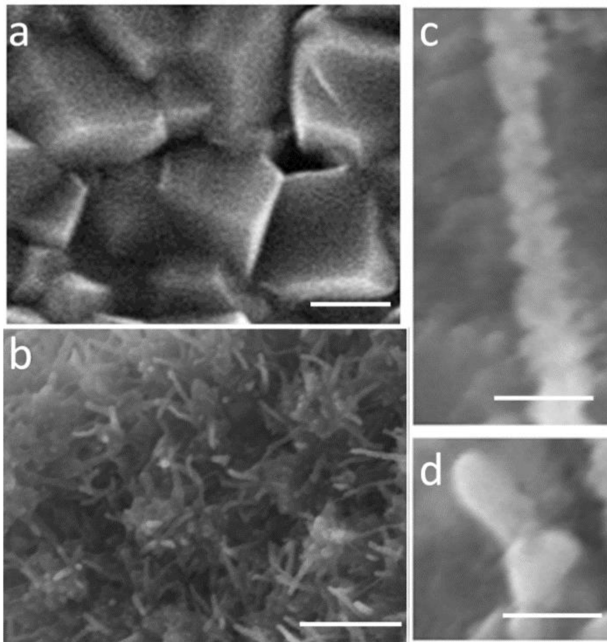

Figure 5.2. SEM images of indium phosphide grown by MOCVD, (a) in the form of a polycrystalline layer grown directly on copper. The scale bar is 1000nm, and (b) in the form of polycrystalline nanowires grown carbon-treated copper. The scale bar is 2500nm. (c) Polycrystalline nanowire in the initial stages of growth. The scale bar is 250nm. (d) Developed poly-crystalline nanowire showing the unique morphology. The scale bar is 250nm.

TEM images of a representative InP nanowire are exhibited in Figure 3 to explore microscopic structural characteristics of the nanowire. Figures 5.3a and 5.3b, collected at two different magnifications, show granular features that indicate that the

nanowire is not single phase. It appears to consist of larger grains with size of 40-120 nm likely to be formed by aggregation of small grains with size of 2-11nm. Figure 5.3c presents a corresponding selective area diffraction (SAD) pattern of the nanowire shown in Figures 5.3a and b. The SAD pattern depicts several rings confirming that the nanowire is polycrystalline. The SAD pattern also displays bright spots on those rings associated with {111}f.c.c. InP crystalline planes.

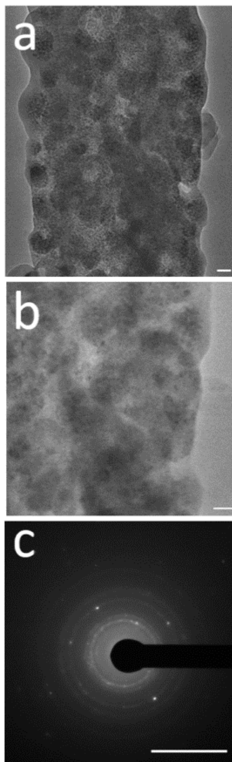

Figure 5.3. (a) TEM image of a poly-crystalline InP nanowire grown on a copper substrate treated with carbon. Multiple single-crystal grains ranging 20-40nm are seen. The scale bar is 20nm. (b) magnified image of the nanowire in (a) showing amorphous regions around the grains. The scale bar is 20nm. (c) diffraction pattern of the nanowire suggesting that the nanowire can be described as polycrystalline, however multiple spots on the rings indicate that a set of specific planes {111} are more prevalent in the nanowire. The scale bar is 1.0nm Dif.

As expected from the observation of InP films grown on Cu foils without a graphene intermediate layer (Figure 5.2a), the growth of silicon on copper without a graphene intermediate layer also resulted in the formation of silicon films with rough surfaces as shown in Figure 5.4a. In contrast, as shown in SEM images in Figure 5.4b-c, a network of Si nanowires were grown on a graphene intermediate layer on Cu foils. Figure 5.4b illustrates a high density nanowire network over an area greater than 2 cm^2 of consistent coverage. A nanowire network has the advantage that charge transport can utilize many paths to maximize electrical conductivity [25]. A low magnification image in Figure 5.4b shows that nominal length of the nanowires exceeds 10μm and the nanowires are randomly orientated. The image depicted in Figure 5.4c indicates that the nanowire diameter is approximately 130nm.

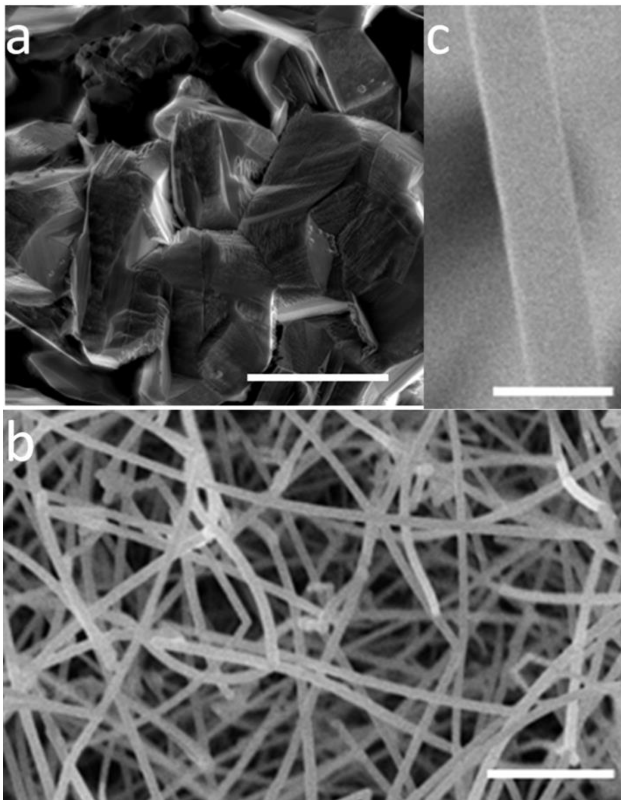

Figure 5.4. SEM images of Silicon grown by PECVD, (a) in the form of a polycrystalline layer grown directly on copper. The scale bar is 25µm. (b) Network of monocrystalline-core, polycrystalline-shell Si nanowires grown on carbon-treated copper. The scale bar is 2000nm. (c) Magnified image of the nanowire. The scale bar is 200nm.

Figure 5.5a illustrates the internal structure of a representative Si nanowire. There appears to be substantial surface roughness with magnitude ~5nm that is not obvious in the corresponding SEM images in Figure 5.4. The TEM indicates that the Si nanowires consist of two distinguishable sections that form a core-shell structure. The core is magnified in Figure 5.5b, revealing that the core diameters range from 10nm to 20nm across the nanowire. A SAD pattern taken on the Si nanowire shown in Figure 5.5a and 5.5b is displayed in Figure 5.5c, which indicates that there is a monocrystalline portion and a polycrystalline portion within the nanowire. The zone axis is [110] f.c.c. and the core was found to be single crystal and oriented f.c.c. [111] direction. The shell is further magnified in Figure 5.5d, which, with the SAD pattern, confirms that it is polycrystalline.

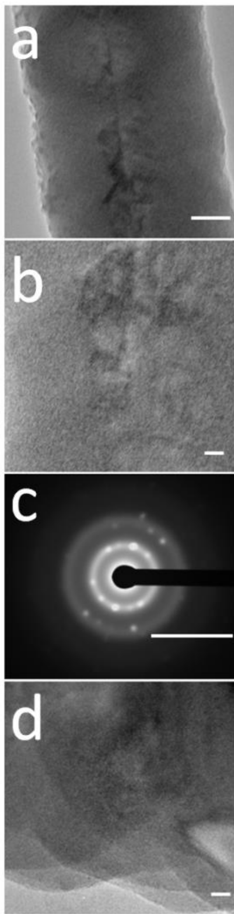

Figure 5.5. (a) TEM image of a Si nanowire grown on a carbon-treated copper substrate. The scale bar is 20nm. (b) Magnified image of the nanowire core, suggesting that the core is monocrystalline. The scale bar is 5nm. (c) Diffraction pattern of the nanowire shown in (a), indicating the presence of both monocrystalline and polycrystalline regions. The zone axis is [111]. The scale bar is 1.0nm Dif. (d) TEM image collected from the shell of the nanowire showing various fringe patterns, which suggests that the shell is polycrystalline. The scale bar is 5nm.

In summary, the growths of InP and Si on Cu foils yielded films on Cu foils, as seen in Figures 5.2a and 5.4a respectively. In contrast, the Cu foils covered with a graphene intermediate layer yielded InP and Si nanowire networks, which suggests that the presence of a graphene layer was a necessary condition for nanowires to form on Cu foils.

XRD was also performed on the nanowire samples, as well as a Cu foil covered with a graphene intermediate layer, to obtain further insights. As shown in Figure 5.6a, XRD taken on a Cu foil covered with a graphene intermediate layer reveals several peaks. Figure 5.6a, collected from a Cu foil covered with a graphene intermediate layer, shows Cu(111) as well as Cu(200), confirming that the copper used in our experiment was polycrystalline. Interestingly, Cu(110) was also seen on Cu foils covered with a graphene intermediate layer in the two nanowire samples (i.e., InP and Si nanowire samples shown in Figure 5.6b and6c).

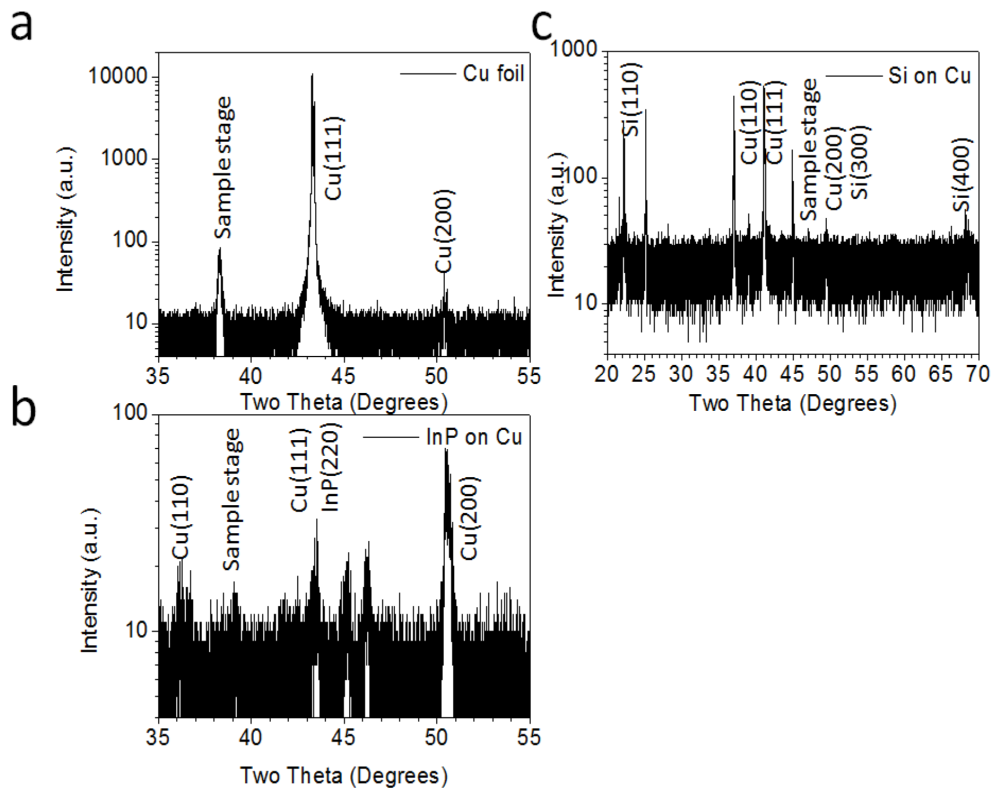

Figure 5.6. X-ray diffraction on the (a) carbon-treated copper, (b) Indium Phosphide nanowires grown on carbon-treated copper, and (c) Silicon nanowires grown on carbon-treated copper.

In figure 5.6b, collected from the InP nanowire sample, Cu(111) and InP(220) peaks located closely each other appear to be a broad peak. The weak InP(220) signal can be attributed to the fact that total InP volume containing InP(220) planes that satisfy the Bragg condition is a small fraction of what it would have been for a single-crystal InP film with the same nominal thickness as that of an ensemble of InP nanowires. In addition, the InP nanowires are polycrystalline, which further reduces the peak intensity compared to that expected for a InP single-crystal film For instance, based on an estimated maximum of 11% spatial coverage by the nanowires and average nanowire length of ~10μm, there would be ~$4x10^{14}nm^3$ total volume or a thin film with thickness of approximately only ~7 nm.

As indicated in Figure 5.6c, collected from the Si nanowire sample, Cu(110), Si (110), Cu(200), Si(300), and Si(400) diffraction peaks suggest that Cu and Si nanowires are preferentially oriented along [100] and [110] direction of each of their respective f.c.c. lattice. It is unsurprising that the [110] contributor from InP and Si went unseen in the TEM diffraction as the zone axis were aligned with that family of planes. The XRD analysis presented here supports the TEM SAD data indicating a polycrystalline nature of Si nanowires and of the Cu foils. Additionally, Cu and Si interdiffuse at their interface, possibly suppressing the formation of nanowires when a graphene intermediate layer was absent [26]. Cu and Si would have also formed a wide range of silicides, which could prevent nanowires from forming. A graphene intermediate layer may have prevented the formation of the silicides, as the XRD profile in Fig. 5.6(c) does not suggest that such silicides are present.

Conclusively determining the cause of polycrystalline formation is difficult, due to the many aspects of growth that can affect the resulting structure, such as the substrate material's chemical interactions, the substrate's surface energy, or the growth's chemical and structural relationship with the orienting layer. Firstly, in epitaxial growth of a thin film on a dissimilar thick substrate, there is, in general, a limit of how much mismatch strain can be accommodated by the thin film. The large mismatch between InP and Cu (62%) prevents epitaxial growth of thin film InP on Cu [27]. To solve this problem, a "buffer" layer can be employed to allow the formation of semiconductor atop a substrate unsuitable for epitaxial growth [28]. For example, previously, InAs nanowires were epitaxially grown by utilizing graphene as an intermediate orienting layer or a "buffer" on copper [12]. In that method, Zinc blende InAs orients along the <110> direction on (111) plane (the nearest-neighbor atomic distance of 0.428 nm). This allows the InAs to be symmetrically well-matched with the carbon honeycomb lattice along <1210> direction on the (0001) plane in the graphene of 0.426 nm spacing. This creates only a ~0.5% misfit between InAs and graphene [12]. The previously reported InAs nanowires were possible through symmetry-based van der walls epitaxial growth on the graphene layer, where the InAs f.c.c. lattice finds the closest matching arrangement of carbon bonds in the honeycomb graphene lattice [12]. The method of growth here with InP and Si on graphene, as well as the previously reported InAs and GaAs on graphene, are unlike traditional heteroexpitaxial growth where the lattice mismatch arises from a small difference in atomic spacing, but rather from asymmetrical arrangement as well as

spacing. Both InAs and InP have an f.c.c. lattice, but their bond lengths are significantly different; 0.428nm for InAs and 0.415nm for InP, respectively, along the <110> direction. Therefore a misfit of ~2.6% is present between InP and graphene, which is much larger than that between InAs and graphene. 2.6% is a significant misfit for a symmetry based growth, which is expected to contribute to substantial strain that could lead to polycrystalline InP nanowires, as we observed. The "natural" crystalline orientation of several semiconductors on graphene has been previously calculated [29]. The large variation in lattice constants forces the different semiconductors to mate to the graphene honeycomb in different ways. For example, Munshi [29] reports that the InP f.c.c. lattice (111) at 0.415nm would conform to the 0.426 nm lattice of graphene. Essentially InP would naturally assume the same alignment on graphene along the (0001)/(111) registry.

Additionally, in the formation of InGaAs on graphene, a core-shell structure was formed creating an InAs core and an InGaAs shell, suggesting strain accommodation can cause the formation of core-shell structures with a type of spinodal decomposition [13]. However, Si and InP cannot break into multiple monocrystalline materials, thus they would simply break into mono-core poly-shell and/or polycrystalline materials. In our case, the Si nanowires may have exhibited a monocrystalline core with a polycrystalline shell structure due to a large in-plane lattice mismatch of ~9.6% between Si (111) and (0001) of graphene or, more likely, of ~4% between graphene (0001) and 30% rotation with respect to the [110] direction of Si (111), creating sufficient strain to force defect creation in the form of a polycrystalline shell. With

this large mismatch, nanowires can still grow, however [30], large mismatch would yield significant strain within nanowires, possibly causing spontaneous creation of a core-shell structure [13].

Another consideration is the use of DTBP in our MOCVD growth of InP, which would have increased the carbon interaction with the Cu substrate during the growth, possibly affecting the pre-existing graphene, while InAs and InGaAs were demonstrated using AsH_3 which would have no effect on the graphene surface [31]. Additionally, Cu is a fast diffuser that interacts strongly with P and Si, which could be affecting the InP growth formation and crystalline nature of Si [32,33]. The previously reported InAs nanowire growth was monocrystalline, despite the substrate being amorphous, which can be largely explained because the lattice mismatch with graphene is only ~0.5% and mild chemical interaction between the substrate and growth material [12]. Additionally, monocrystalline GaAs was grown on graphene, despite a 6.3% lattice mismatch [29]. However, the original substrate was crystalline and a less reactive than the Cu used in our experiments. Here, we present materials grown on a polycrystalline substrate with lattice mismatch of 2.6% for InP and 4% for Si. In addition to the substrate's polycrystallinity, the surface energy of the intermediate graphene layer used in our experiments also plays a role in the polycrystalline nature of formation in this study.

Conclusion

The utilization of graphene to form nucleation sites for the growth of InP and Si nanowires on Cu foils was demonstrated. Based on a series of studies with two different materials (i.e., Si and InP), we concluded that the graphene intermediate layer serves as a template on polycrystalline Cu, facilitating the growth. The InP nanowires exhibit grains with a wide range of sizes, which would allow the grains to be engineered for optimum scattering of phonons. The Si nanowire networks exhibit large polycrystalline shells that would scatter phonons with rough surfaces, and a large number of grain boundaries and monocrystalline cores would be advantageous for transport of electrons or holes. These two types of material platforms on mechanically flexible Cu foils could be ideal for thermoelectric devices. This technique allows for the use of flexible, metallic substrates for large area growth of semiconductor nanowires.

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Chapter 6

Silicon Nanowire Networks for Multi-stage Thermoelectric Modules

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ABSTRACT

We present the fabrication and characterization of single, double, and quadruple stacked flexible silicon nanowire network based thermoelectric modules. From double to quadruple stacked modules, power production increased 27%, demonstrating that stacking multiple nanowire thermoelectric devices in series is a scalable method to generate power by supplying larger temperature gradient. We present a vertically scalable multi-stage thermoelectric module design using semiconducting nanowires, eliminating the need for both n-type and p-type semiconductors for modules.

Keyword: Nanowire Network; Plasma enhanced chemical vapor deposition (PECVD); Silicon; TiN nucleation layer; copper substrate

Introduction

Most of the energy produced commercially in the United States is lost to the environment in the form of waste heat [1]. Some of this lost energy can be recovered by mechanical heat engines via the Rankine cycle, but much of this waste heat, especially low grade (<230°C) heat, is not considered practical to recover due to low conversion efficiencies [2]. Thermoelectric (TE) devices, which convert heat into electricity via the Seebeck effect, are an attractive option for recovering waste heat [3]–[5]. A range of emerging materials, expected to increase the Seebeck coefficient (S) and decrease thermal conductivity (κ), have propelled the field of TE research at the nanometer scale. While significant materials advances have been made with superlattices[6], [7] , nanowires [8]–[10], nanocomposites [11], [12], thin films [13], and layered films[14], [15] there seems to be many aspects left for further advancement. In additional to material advancements the field is turning toward larger device design advancements such as p-n leg geometry[16], Fresnel lenses to intensify heat [17], as well as sandwiched traditional devices to optimize cross flow [18], [19] . In this paper, by forming randomly oriented nanowire networks onto flexible metallic substrates, rather than semiconductor substrates, we build on a new concept for fabricating a TE module[20]. In this demonstration, Silicon was chosen for the TE material because of its abundance and nontoxicity. Silicon also demonstrated reduced thermal conductivity when formed into nanowires, which was beneficial to TE power generation [21]–[23]. Our design concept is not limited to Silicon; thus other semiconductors suitable for the desired range of temperatures,

such as Indium Phosphide (InP) and Indium Antimonide (InSb) [24], which our lab has also used to demonstrate viable TE devices can be similarly implemented. As a substrate, copper was selected due to its low cost, mechanical flexibility, and high electrical and thermal conductivities. More importantly, the metallic substrate allows us to design a TE module with simple electrical connections either vertically or laterally to obtain desirable open circuit voltage (V_{oc}) and short circuit current (I_{sc}).

Conventional TE modules use a large number of small legs made of both n and p-type semiconductor to cover required device area, adding significant manufacturing costs associated with materials and assembly [25]. In these devices, V_{oc} increases as multiple p- and n-type semiconductor legs are connected in series; however, I_{sc} is limited by a narrow current path defined by the cross-sectional area of each semiconductor leg and the contact resistance associated with metal-semiconductor junctions, thus; in these devices, the series resistance increases as the number of semiconductor legs increases, limiting I_{sc} that can be achieved for a given electrical power. The concept of multi-stage TE modules presented in this paper offers additional unique design elements by incorporating only one type of semiconductor and a large cross sectional area as a current path into the device.

Additionally, from TE module design perspective, there is an inherent vertical scaling limitation with traditional TE modules because conventional TE modules cannot be easily stacked on top of one another to increase overall module thickness, which is partly because of heat and electrical current flowing orthogonally to each other (i.e., current flows laterally while heat flows vertically). In the multi-stage TE

modules presented in this paper, heat and current flow parallel to each other, allowing for the modules to have large effective thickness that can create a large temperature gradient for a given heat source. Our approach also allows us to fabricate a TE module that is built by laterally assembling single modules made of both n-type and p-type materials, as in a conventional TE module, which is suitable for applications that require high voltage for a given power. This choice of assembling several modules allows a high current or high power module is not readily attainable with traditional TE modules.

Experiment

Copper (Cu) foils (approximately 50µm thick) with area of $2cm^2$ were prepared with acetic acid, rinsed with Deionized water, and air dried. A 40nm thick Titanium Nitride (TiN) layer was deposited onto the prepared Cu foils using an atomic layer deposition system with an inductively coupled plasma source. The TiN layer was deposited at 300°C with N_2 carrier gas. N_2 plasma and Titanium tetrachloride, TiCl4, were utilized as the Nitrogen and Titanium precursors, respectively. Subsequently, 4nm of gold (Au) was deposited by electron-beam evaporation onto the TiN layer.

Four samples were made for this study. All four were boron doped p-type Silicon (Si) nanowires grown in the form of three-dimensional network to promote electrical conduction while reducing thermal conductivity[26]. The Si nanowire networks were deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) with plasma generated by a 180-250kHz 12.6 kW power source using a two-step process to form

first a nanowire network and secondly a continuous semiconducting layer [27]. Precursors for the B-doped Si nanowire networks were disilane diluted in hydrogen and diborane. The PECVD process consisted of a pre-growth annealing step performed at 400°C for 5 min in hydrogen, which was followed by a nanowire growth step at 500°C. The disilane flow rate was 10 sccm with a reactor pressure of 0.3 Torr. The growth time for each of the four samples was different: 45, 15, 30, and 90 minutes for Samples 1, 2, 3, and 4, respectively. After the growth step was completed, the reaction chamber was evacuated and then the sample was cooled to 50°C in argon.

Samples 1 and 3 were also topped with an additional p-type Si layer, referred to as "Second Si layer", which served as a top contact layer and prevented electrical and thermal shorting. This top contact Si layer was deposited by PECVD at 500°C and 0.5 Torr for 15 minutes with the same precursors used for the nanowire growth. The four samples, Sample 1-4, are selectively combined to fabricate three different modules schematically shown in Figure 6.1a-c. The module depicted in Figure 6.1a is composed of Sample 3 and will be referred to as Module 1. The multi-stage device depicted in Figure 6.1b is composed of Sample 3 and 4, referred to, from here forward, as Module 2. Samples 1, 2, 3, and 4 were used to create the device depicted in Figure 6.1c and will be referred to as Module 3. The three modules, Module 1-3, were tested to obtain current-voltage characteristics, and to measure the generated electrical power output. Heat was supplied by a Joule heater to one side of the device while an active heat sink removed heat from the other side, maintaining a constant temperature gradient, regardless of different overall thickness of the three modules, at

around a desired temperature. Sample 3 in each module was consistently applied to the actively cooled side of the three modules. Current–voltage measurements were made using a HP 4155A Semiconductor Parameter Analyzer parameter analyzer at a range of temperatures in the direction as heat flow, the direction normal to the Cu foil surfaces. The voltage drop measured across the stack was made with respect to the cold side as the positive terminal and the hot side as the grounded end of the stack. A 3D printed holder is utilized to hold the samples in place while ensuring good thermal contact and thermocouples are imbedded in the holders to measure the temperature at each side of the stack. The thermocouples are connected to a 24 bit national instruments thermocouple input module to a labview program to record 4 thermocouple's reading's through time.

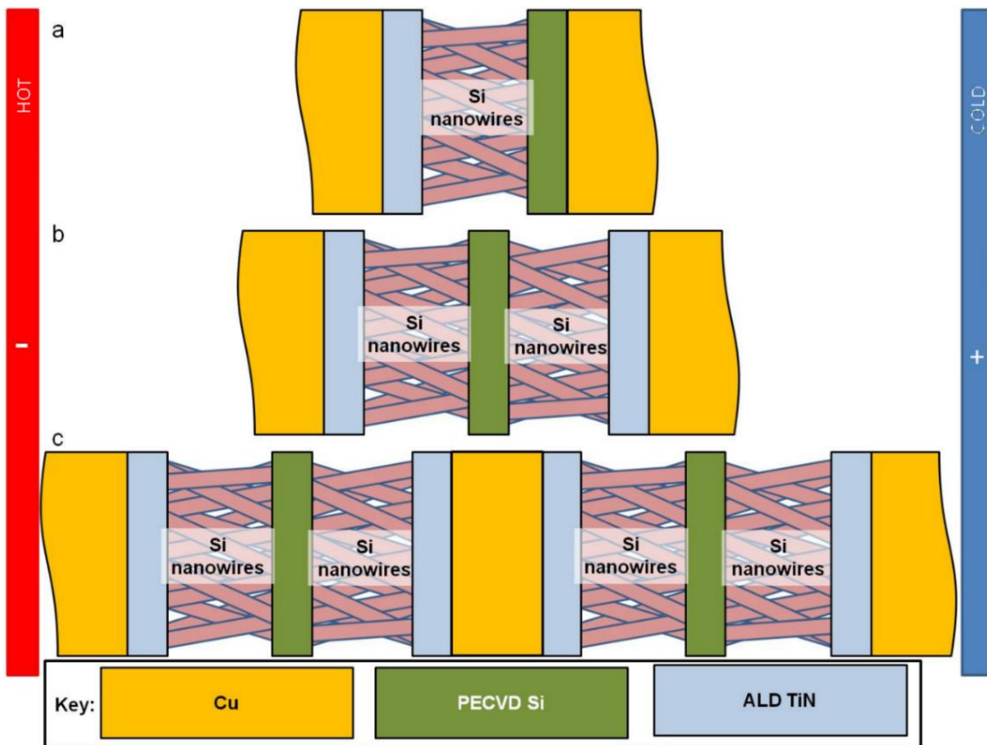

Figure 6.1. Schematic of the three TE modules made of stack of Si nanowire network combined with Si and TiN layers integrated on Cu foils.; a) single stack module (Module 1), b) double stack module (Module 2), and c) quadruple stack module (Module 3).

Results and Discussion

Scanning electron microscopy (SEM) was used to inspect characteristic growth habits of Si nanowires in Sample 1-4 as shown in Figure 6.2. All four samples have nanowires with uniform high areal density and lengths exceeding 30µm, establishing characteristic nanowire networks with a large number of interconnects. The SEM images also reveal a large variation in nanowire diameter between and within samples. Additionally, the nanowires in all samples appear to have a noticeably smooth surface. The four samples, Sample 1-4, are summarized in Table 6.1.

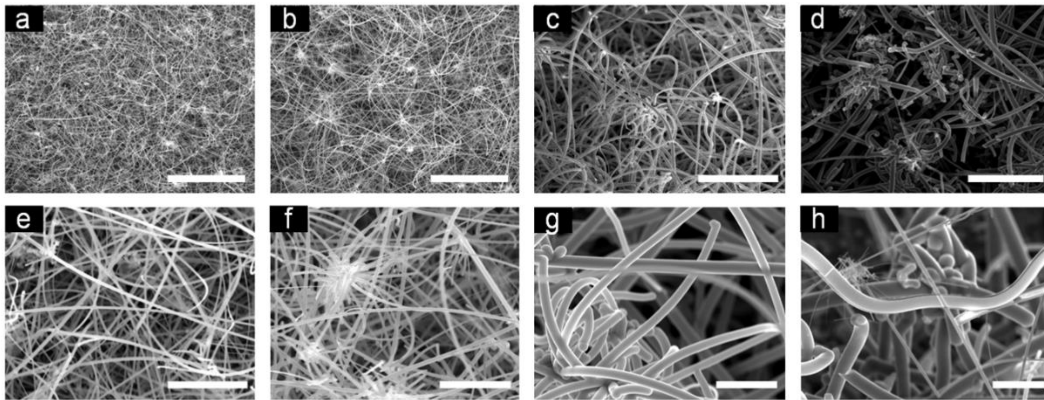

Figure 6.2. Scanning electron microscope (SEM) image of p-type (B doped) silicon nanowire networks grown by PECVD on Cu foils. Panels (a)-(d) are at low magnification (30µm scale bar), revealing high density networks. Panels (e)-(h) are at high magnification (5µm scale bar), revealing the diameter range of the nanowires. Samples 1-4 correspond to Figure 2a-d and Figure 2e-h respectively.

Table 6.1. Nanowire diameter range and growth time for each sample

Sample Number	Diameter Range (nm)	Growth Time (min)	Second Si Layer
1	50-190	45	Yes
2	40-300	15	No
3	900-1400	30	Yes
4	17-1600	90	No

Current-voltage (I-V) measurements at three different temperature differentials, ~ Δ0 ˚C, ~Δ35 ˚C, and ~ Δ67 ˚C, were done on Module 1-3 as shown in Figure 6.3. All I-V curves are straight lines, indicating that ohmic contacts are made through the modules. The measured current for any given applied voltage increases as the temperature gradient increases, as is expected from the presence of the Seebeck effect. The slope of the I-V curves (i.e., conductance) for Module 1 and 2 appears to change as the average temperature changes. In Module 1, the conductance increases as the temperature gradient increases, whereas in Module 2, the conductance decreases as the temperature gradient increases. Unlike Module 1 and 2, the conductance of Module 3 remained unchanged upon increasing the average measurement temperature. The dependence of the conductance on the average measurement temperature can be explained qualitatively as follows. For semiconducting Si, the conductance is expected to increase with increasing

temperature. For metallic Cu and TiN, on the other hand, the conductance is expected to decrease with increasing temperature. Therefore, the dependence of the conductance on the average measurement temperature in Fig.6.3 suggests; Module 1 is dominated by the semiconducting portions, while Module 2 is dominated by the metallic portions, and, in Module 3, the conductance is equally contributed from both the semiconducting and metallic portions. The conductance of Module 3 being insensitive to the magnitude of the temperature gradient indicates that stacking multiple devices, and therefore creating additional metal-semiconductor interfaces, does not pose problems with maintaining conductance, making this architecture a vertically scalable option for building a thick TE module. The fact that the electrical conductance of Module 3 remains constant also suggests the module efficiency can be maintained through a wide range of temperatures by implementing this module architecture. The constant electrical conductance of Module 3 as the average measurement temperature increases, along with the ohmic behavior at ΔT=0, also indicates that electrical transport is not being inhibited significantly by various interfaces present in the module. As such, many nanowire networks could be stacked together, allowing for a large ΔT, as thicker devices can maintain larger temperature gradients for a given heat source. In this case, then different materials assigned for each stage of a multi-stage TE module could be utilized to take advantage of the fact that different materials have specific temperature ranges where heat is optimally converted into electricity [28], [29]. Figure 6.3 also shows that the Voc of each device at ΔT ~67 doesn't scale with the number of Si nanowire stacks because the

temperature difference was set to be approximately the same for each stack in the three modules. This is reflected in that, regardless of the number of Si nanowire stacks, the effective Seebeck coefficient was comparable for all three modules. To further investigate how each Si nanowire network stack contributes to the overall module performance, we compared the power output of the three modules by setting a specific temperature gradient for each module so that the temperature gradient per stack in a module was approximately equal for all the modules.

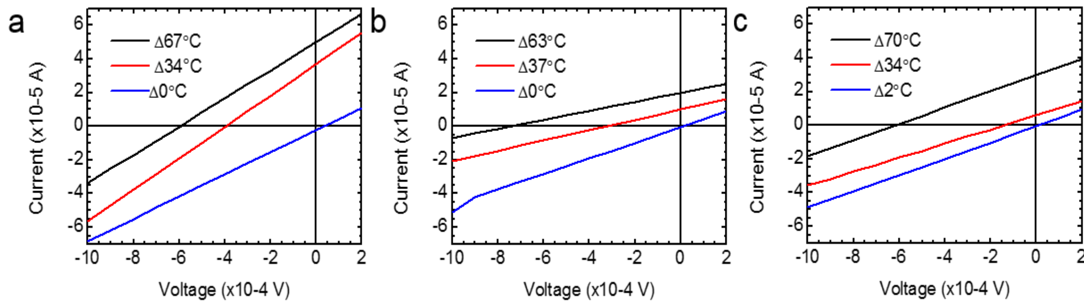

Figure 6.3. Current versus voltage curves are shown for (a) Module 1, (b) Module 2, and (c) Module 3 with varied temperature differences across the two devices.

Figure 6.4 shows I-V and power curves for the three modules. The measurement was done by providing ~ ΔT=18°C across a single stack within each module. For example, a four-stack device with a 70°C gradient across the device provide a gradient of ~17.5°C across each stack. Table 6.2 gives the maximum generated power P_{max} for each module and P_{max} per stack, as illustrated in Figure 6.4, along with V_{oc} and I_{sc}. P_{max} obtained from these modules were comparable to those found in earlier studies[30], [31]. Figure 6.4 and Table 6.2 clearly demonstrate that the total power generation of multi-stage TE modules scale with the number of stacks,

whereas the P_{max} per stack remains relatively constant. Additionally the η measured with these devices is expectedly low as they were tested out of their optimal conversion range however here we are presenting a new design and we are currently optimizing our devices to improve η. V_{oc} increases as the number of stacks increases, as expected from a set of voltage sources connected in series. As expected, the P_{max} per stack appears to be relatively constant because *ΔT*/stack was the same and conductance/stack for all three modules, signaling that having multiple stacks didn't hamper the modules' ability to produce power. Based on the constant *Pmax*/stack for a given overall ΔT, as well as the increase of *Pmax*/ΔT from Module 2 to Module 3, we have shown that the addition of stacks does not inhibit the ability of a multi-stage TE device to produce increasing amounts of power as stacks are added. Therefore, a semiconductor nanowire network on a metallic substrate is a viable material platform for multi-stage TE modules that can be scaled vertically through stacking, and can accommodate large temperature gradients.

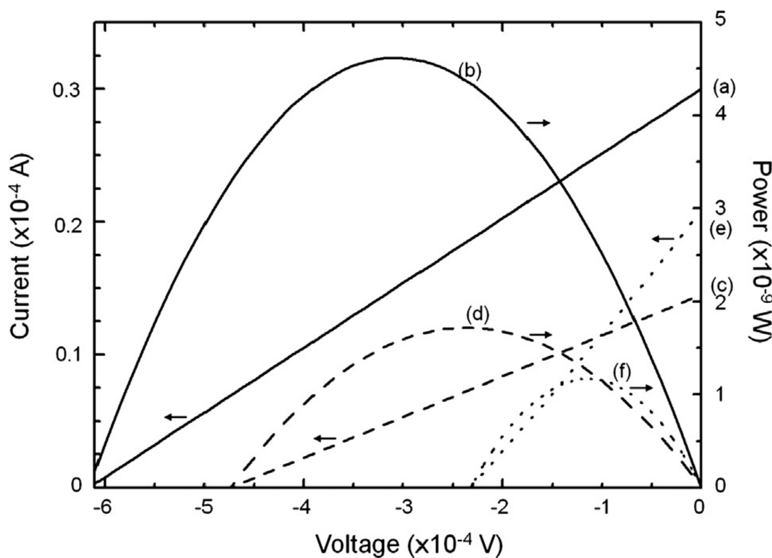

Figure 6.4. Power curves and current versus voltage curves. (a),(b): ~Δ70˚C across Module 3 (quadruple stack module). (c),(d): ~Δ37˚C across Module 2 (double stack module). (e),(f): ~Δ19˚C across Module 1 (single stack module). In all Modules, the temperature gradient across each stack is the same, 18˚C±1˚C

Table 6.2. Values of P_{max}, I_{sc}, and V_{oc} for each Module and per stack, for a temperature gradient of ΔT = 18˚C±1˚C per stack

P_{max} (x10^{-9}W)	ΔT (˚C)	number stacked	ΔT/stack (˚C)	P_{max}/stack (x10^{-9}W)	I_{sc} (μA)	V_{oc} (mV)	η (=P_{max} /P_{in}) (μ%)
4.7	70	4	17.5	1.2	30	6.2	.47
1.7	37	2	18.5	.85	14.5	4.7	.27
1.1	19	1	19	1.1	20	2.3	.32

Conclusion

We have presented the concept of multi-stage TE module using semiconductor nanowire-based TE devices directly fabricated on Cu foils. Given the concept, we demonstrated ~2cm^2 flexible, multi-stage TE modules that are laterally and vertically scalable. As inherently expected, V_{oc} and P_{max} for a given temperature difference per stack increased as the number of stacks vertical mounted in series increases. The fact that power output scales with the number of stacks suggests that the concept of multi-stage TE module is a viable option for applications where vertical scalability is appropriate for a large thermal gradient. In addition, individual modules can be assembled laterally to fabricate a TE module that can accommodate a large area heat source applications that require high current for a given power. The

TE module architecture presented in this paper is directly built on flexible Cu foils that have potential of providing usable area much larger than that of single-crystal semiconductor substrates commercially available. Our module architecture being mechanically flexible accommodates heat sources of arbitrarily shape and size. The concept of multi-stage TE modules is not limited to the specific choice (i.e. Si) we used as a nanowire material for the demonstration, and another semiconductor or a combination of various semiconductors within a stack or for different stacks can be selected for specific temperature ranges that need to be covered. The TE module architecture presented here allows for the tailoring of TE modules for specific current-voltage characteristics required for a target application through various avenues for optimization.

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Chapter 7

Nonlinear Current-Voltage Characteristics of Semiconductor Nanowire Network based Double-stage Thermoelectric Devices

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ABSTRACT

This paper presents the concept of a unique thermoelectric devices experimentally demonstrated. One of the multiple design factors for electrical power generation that this concept utilizes is non-linearity in the current-voltage characteristics of the studied devices. In this particular study, the thermoelectric devices were made of two thermoelectric cells that employed silicon and indium phosphide nanowire networks grown on a mechanically flexible copper substrate. The use of two dissimilar materials, silicon and indium phosphide, was intended to increase energy conversion efficiency by taking advantage of each of the two materials that perform well at different temperature ranges (i.e. double-stage

thermoelectric device). The demonstrated concept suggests the presence of a new pathway to increase maximum electrical power generation for a given temperature gradient under specific electrical load conditions.

Keyword: Nonlinear current-voltage, Nanowire, thermoelectric, flexible substrate

Introduction

Thermoelectric (TE) power generation is an attractive method of generating electrical power from various heat sources [1]. In the past, progress in this field has resulted from focusing on TE materials engineering aspects, rather than TE device designs. For instance, a range of emerging nanomaterials expected to increase the Seebeck coefficient (S) and decrease thermal conductivity (κ) have propelled the development of exotic TE materials controlled at the nanometer scale; advances have been made with superlattices [2]–[4], thin films[5]–[7] , organic semiconductors[8], and nanowires [9]–[12]. Nanowires have stood out as an especially desirable option due to their reduced thermal conductivity while maintaining electrical conductivity and the Seebeck coefficient[13]–[16]. The collective properties of nanowires forming a network, rather than a collection of a large number of discrete nanowires, are further beneficial in TE applications, as heat has to travel over a distance much longer in a nanowire network than in a single nanowire [17].

Various TE materials are routinely evaluated by the dimensionless figure of merit (ZT), which is defined as $ZT= S^2\sigma T/\kappa$ where T is an operating temperature. ZT is often used to scale the Carnot efficiency to obtain power conversion efficiency, however

such power conversion efficiency deduced from *ZT* often does not provide a practical way of optimizing device performance; thus, in this paper we present a new concept. We suggest that rather than rely on performance improvements, electrical power generated at various temperatures capitalize on the practical benefit of the concept of double-stage TE devices with non-linear current-voltage characteristics. Traditionally, TE materials are appropriately doped to ensure highly-efficient ohmic contacts in a TE device; as a result, given a conventional TE device architecture, the current-voltage characteristic is linear. In contrast, the device presented in this paper takes advantage of non-linearity explicitly introduced in current-voltage characteristics to increase electrical power generation. It is conceivable that this new concept in TE, if designed and implemented properly, adds another knob to optimize TE devices in the same way that non-linear current-voltage characteristics has been known to be one of the keys performance factors in photovoltaics[18], [19]. Non-linearity in current-voltage characteristics of TE devices can be established, for instance, through the introduction of a rectifying layer, interface, or inducing space-charge region without substantially destructing overall charge transport [20], [21].

The new device architecture presented in this paper is made possible by our unique processes of growing single-crystal semiconductor nanowire networks on non-single crystal copper substrates [22]. The metal/semiconductor nanowire/metal building block (i.e. TE cell) without a thick semiconductor substrate can be put on top of each other to fabricate multi-stage TE devices (Note: two TE cells are stacked in this paper), which generates a thermal gradient, for a given heat source, much larger

than that generated by a single-stage TE device; in other words, multi-stage TE devices can be physically much thicker than a single-stage TE device[11]. In addition, multi-stage TE devices allow different semiconductor materials to be used; thus, in this demonstration, Si and InP, two representative materials available in our laboratory, were chosen for the nanowire materials.

Experiment

InP and Si nanowire networks were separately grown on flexible copper (Cu) foils that were ~50μm thick over 2cm^2 in area. The Cu foils served as bottom electrodes to fabricate two discrete TE devices, as shown in Figure 7.1, for which two distinctive preparation processes were developed. Cu foils utilized for InP nanowire networks were treated with acetic acid, rinsed with acetone, methanol, and di water then air dried. Next, electron-beam evaporation was used to deposit a 30nm Si layer directly on the prepared Cu foils. Subsequently, the Cu foils were coated with colloidal gold particles with diameters approximately 10-50 nm and allowed to dry in air. A two-step metal organic chemical vapor deposition (MOCVD) growth process, specifically developed for the prepared Cu foils, was used to grow the InP nanowire network [22], [23]. The two-step MOCVD growth, consisting of a nanowire growth mode (step 1) followed by a film growth mode (step 2), formed a continuous layer on the tips of the nanowires ensuring that a good Ohmic contact (i.e., a top electrode) could be formed on the nanowires without electrical shorting between the top electrode and the Cu foil (i.e., the bottom electrode). In the two-step MOCVD growth for InP nanowire networks, growth conditions were as follows: in step 1, growth pressure: 150 Torr, a

molar V/III ratio: 3.8, growth time: 45 minutes, and growth temperature: 560°C, and in step 2, growth pressure: 150 Torr, a molar V/III ratio: 1.5, growth time: 55 minutes, and growth temperature: 500°C. The precursors for the two-step MOCVD growth of InP nanowire network were ditertiary butylphosphine (DTBP) and trimethylindium (TMIn) at molar flow rates of 5.0×10^{-4} moles/min and 1.3×10^{-4} moles/min, respectively, for step 1, and 5.0×10^{-4} moles/min and 3.3×10^{-4} moles/min, respectively, for step 2. InP nanowires were doped unintentionally due to phosphorous loss from their surfaces during the growth, causing the InP nanowires to become slightly p-type. In the MOCVD growth, the InP nanowire network layer in the InP TE device was treated with indium during the final step of the growth to increase the surface area on which the PECVD Si top layer was deposited, thus it is likely that the InP nanowires lost a certain amount of phosphorus from their surfaces. Following the InP nanowire network growth, an n-type (Sb doped) Si layer was deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) onto the nearly continuous InP layer resulted from the two-step MOCVD growth. The PECVD deposition was conducted at 500°C, 0.5 Torr, for 15 minutes with 180-250 kHz plasma generated by a 12.6 kW power source. Precursors for the Sb-doped Si layer were 15,000ppm disilane diluted in hydrogen and triethylantimony introduced as an n-type dopant. This Si layer, referred to as "PECVD Si", in addition to the InP layer grown in step 2 of the two-step MOCVD growth, provided a doped semiconductor surface for a top electrode and prevented shorting when a top electrode was applied. The fabricated TE device, referred to as "single-stage InP TE device", made of Cu

bottom electrode/Evaporated Si/InP nanowire network/PECVD Si/Cu top electrode, is schematically shown in Figure 7.1a.

The Cu foils utilized for Si nanowire network growth were prepared with acetic acid, rinsed with DI water, and air dried. Subsequently, carbon deposition was performed on the prepared Cu foil. The process of depositing a carbon layer on Cu foils and the role graphene plays within the context of growing Si nanowires have been described and studied using Raman spectroscopy [22]. The study showed that growing Si on Cu without a graphene layer results in a poly-crystalline Si layer rather than nanowires. After the graphene deposition, the Cu foils were further coated with colloidal gold prepared from a 1mMolar hydrogen tetrachloroaurate and 1% trisodium citrate solution. Plasma enhanced chemical vapor deposition (PECVD) was utilized to grow silicon nanowire networks at a growth temperature of 500°C. The disilane flow rate was 10sccm with a reactor pressure of 0.3Torr and a growth time of 15 minutes. After the growth of Si nanowire network, the reaction chamber was evacuated and the sample was cooled to 50℃ in argon. The resulted TE device based on Si nanowire networks, referred to as "single-stage Si TE device" was coupled with the single-stage InP TE device shown in Figure 1a to fabricate a two-stage TE device, referred to as "double-stage Si/InP TE device", schematically shown in Figure 7.1b. We discovered with the testing of the single-stage Si TE device that the second stage of layer growth is essential to the application of a top contact without shorting the devices.

TE measurements of the resulting two devices, single-stage InP TE device and double-stage InP/Si TE device, schematically shown in Figure 7.1a and b and described above, were performed. Heat was supplied by a Joule heater to the top electrode of the device while a heat sink removed heat from the bottom electrode, maintaining a constant temperature gradient. Current–voltage measurements were made in the same direction of heat flow. Current–voltage measurements were made at a range of temperatures by applying electrical voltage to the top electrode while the bottom electrode was grounded.

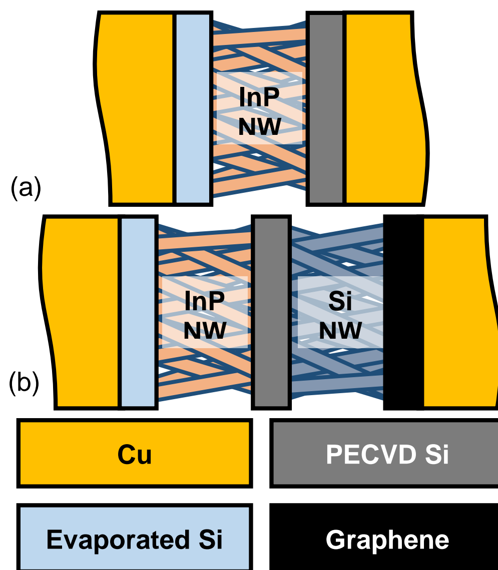

Figure 7.1. Schematic of two TE devices (a) a single-stage InP TE device composed of an InP nanowire network and a PECVD Si layer, and (b) a double-stage InP/Si TE device composed of InP and Si nanowire networks and a PECVD Si layer.

1. Results and Discussion

Scanning electron microscopy (SEM) was used to investigate the InP nanowire growths on Cu coated with an evaporated Si layer before and after a PECVD Si layer

was deposited. Figure 7.2a illustrates as-grown InP nanowires from the two-step MOCVD growth described earlier. The two-step MOCVD growth promoted the formation of large, up to ~1µm in diameter, spherical tips from 50nm colloidal Au and ~250nm caps stemming from 10nm colloidal Au. These features provided an effective large surface area for the formation of a top electrode. As seen in Figure7.2b, the InP nanowire network and spherical tips grew up to 10µm long. The InP nanowires grew uniformly across the area of 2cm x 2cm with areal density (total length/area) in the range of 10-50μm^{-1}. The InP nanowires are oriented in the direction the non-single crystalline evaporated Si layer deposited on the Cu substrate obtained when it became poly-crystalline therefore the InP nanowires are not in an array. The evaporated Si layer served as a nucleation layer that promoted the formation of InP nanowires on a Cu substrate, which was validated by the fact that InP grew as a poly-crystalline film when deposited directly on a Cu substrate [22]. In Figure 7.2c and 7.2d, SEM was further used to characterize morphology of the InP nanowires after having been covered with a PECVD Si layer. This layer prevents shorting upon the application of a top electrode. Interestingly, the large nanowire tips formed in the second step of the two-step MOCVD growth of InP nanowire networks appear to have been coated during the Si growth and reveal a more uniform, thicker diameter.

Structural information of nanowires is also vital for TE designs; therefore transmission electron microscopy (TEM) was performed on the InP nanowire network covered with the PECVD Si layer in the single-stage InP TE device (i.e.

Figure 7.1a) and is shown in Figure 7.2e. Shown in Figure 7.2f is a selected area diffraction (SAD) pattern collected with a diffraction aperture that covered a large number of InP nanowires. Based on unique features, fringe spacing, and pattern symmetry of multiple diffraction spots present in Figure 7.2e, it appears that the core of each nanowire is composed of single crystalline InP oriented along its respective <111> directions. The PECVD Si layer appears to have formed a rough Si shell around the InP nanowire. The core-shell structure is theoretically expected to be beneficial in simultaneously providing a transport path for charged carriers and a scattering mechanism for phonons [24], [25]. Additionally, rough surface morphology has been shown to benefit TE properties of nanowires[15], [26]. Diffraction rings slightly offset from each other were found to be associated with poly-crystalline nature of the Si shell, therefore, the nanowire network used in the single-stage InP TE device is made of a large number of single-crystalline InP nanowire cores each of which is surrounded by a poly-crystalline Si shell.

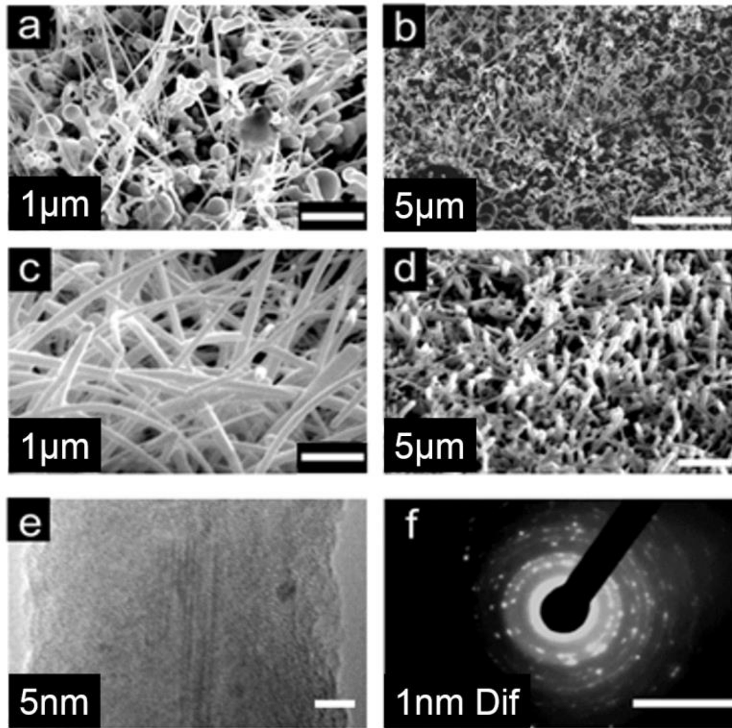

Figure 7.2. Scanning electron microscope (SEM) images of InP grown by the two-step MOCVD growth prior to the PECVD Si layer deposition a) at high magnification and b) at low magnification. Scanning electron microscope (SEM) images of the same sample after PECVD Si layer was deposited (c) at high magnification and (d) low magnification. (e) TEM imaging of the sample imaged in (c-d). There appears to be an InP crystalline core with a Si shell. The diffraction pattern of the nanowire shown in (f) indicates the presence of single-crystal InP and poly-crystal Si.

Figure 7.3a-b show SEM images of Si nanowires used in the single-stage Si TE device. Figure 7.3a shows a high magnification image depicting interconnections formed by multiple nanowires fused during the growth, forming a 3D nanowire network. Previously, it was found that a nanowire network allows for the transport of electrical charges further than the length of an individual nanowire [17]. With many conduction paths, electrical current will be able to flow easily through the network, whereas the interconnections may limit the propagation of phonons through the

network [27]. Figure 7.3b reveals that the average length of the nanowires exceeds 15μm. The Si nanowires grew fairly uniformly across the area of 2cm x 2cm with areal density (total length/area) in the range of 20-100μm^{-1}. A bright field TEM image of a representative nanowire is shown in Figure 7.3c. The nanowires exhibited a core shell structure with the core being single-crystal silicon and the shell being poly-crystalline silicon. The Si crystalline cores observed ranged from 10-20nm in diameter. Nanowires with a crystalline core and poly-crystalline shell could potentially reduce thermal conductivity by scattering phonons in the poly-crystalline shell while the single-crystalline core provides a conduction path for electrical charges. The SAD pattern in Figure 7.3d indicates that there are both single and poly-crystal phases in the analyzed area. It appears that the zone is [110] with bright (111) spots of single-crystal Si with a slight rotation due to off tilt and the surrounding shell is poly-crystal.

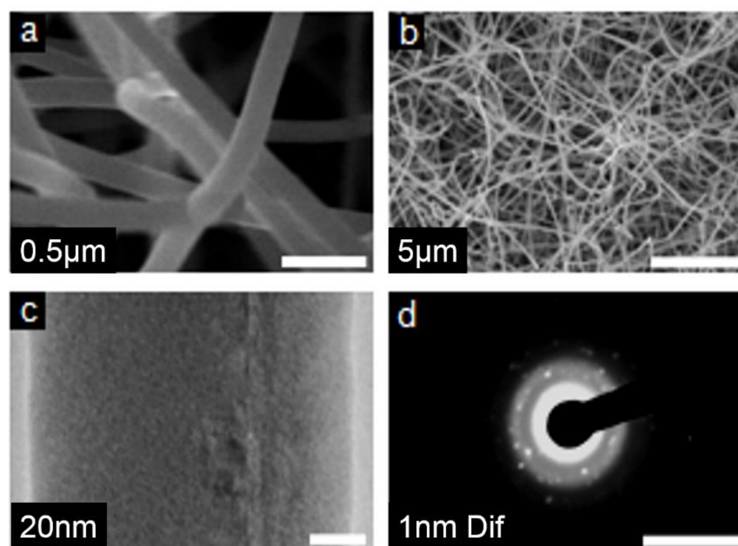

Figure 7.3. Scanning electron microscope (SEM) image of an unintentionally doped Silicon nanowire network a) at high magnification and b) at low magnification. (c) TEM image of the same growth, showing a single-crystal core in the nanowire and in (d) the diffraction pattern of the nanowire shown in (c) indicates the presence of both single-crystal and poly-crystal regions.

Current-voltage (I-V) measurements at various temperatures were done on both the single-stage InP TE device and the double-stage InP/Si TE device, and are shown in Figure 7.4. In Figure 7.4, curves (a)-(d), the single-stage InP TE device, reveal n-type characteristics with the I-V curve shifted into second quadrant, while curves (e)-(g), the double-stage InP/Si TE device, reveal characteristics of a p-type semiconductor device, with the I-V curve shifted into the fourth quadrant. An n-type Si reference sample was used to confirm that n-type semiconductor produces power in the second quadrant. Power produced by the single-stage InP TE devices in the second quadrant suggests that the n-type PECVD Si top layer combined with an unintentionally p-doped InP nanowire network dominates the power production, in other words, electrons in the n-type PECVD Si top layer would easily dominate transport properties of the entire device, regardless of the presence of an unintentional doping of the InP nanowire network. Therefore, it is unsurprising that the overall device characteristics are aligned with that of the sole doped layer (i.e. n-type PECVD Si layer).

Curves (a)-(d) show that as the temperature differential increases, so does V_{oc} and I_{sc}, along with the area under the curve. This indicates that the maximum thermoelectric output power found on each I-V curve increases. Curves (e)-(g) of the double-stage InP TE device also indicate that, as the temperature difference increases,

so does the maximum output power found on each I-V curve. The double-stage device demonstrates significant increases in power production compared to those of the single-stage InP TE device at Δ50˚C (i.e., curve (d)). In contrast to the linear I-V curves (a)-(d), the I-V curves of the double-stage InP/Si device present non-linear characteristics, which resemble I-V characteristics of photovoltaic (PV) cells at different illumination levels. Such non-linear I-V curves at various temperatures, based on its analogy to power production in PV cells, can be viewed as a way to increase overall electrical power production in TE devices in comparison to conventional TE devices that show linear I-V characteristics.

The nonlinear characteristics seen in the double-stage TE device poses an interesting concept that could be applied to semiconductor TE devices. Therefore, we explore how this feature arose, by a rectifying layer or interface or possibly the undoped nanowires operated in the space charge limited transport regime. There are many possible causes for nonlinearity as there are many interfaces present in this device. The non-linear I-V curves (i.e., rectifying I-V curves) could indicate the presence of a Schottky barrier in the double-stage InP/Si TE device. As non-linearity is not exhibited by the single-stage TE device in Figure 1a, it is unlikely that a rectifying junction (e.g. PN junction) is present at the interface between the PECVD Si layer (n-type) and the p-type InP nanowires. Additionally, the nonlinearity must not have been caused by the undoped 30nm Si evaporated directly on Cu as the identical interface is also present in the single-stage InP TE device, which does not exhibit non-linearity. This barrier could therefore have been created by forming a PN

junction when the n-type PECVD Si layer formed a contact with the p-type Si nanowire network. In the double-stage InP/Si TE devices shown in Figure 7.1b, a Schottky barrier could form when the graphene formed on the copper foil. It has been previously reported that a Si/graphene interface creates a Schottky barrier with rectifying behavior [28]–[30]. Finally it has been reported that undoped semiconductor nanowires experience space-charge-limited transport with characteristic nonlinear IV curves, which dominates over Schottky barriers [20]. Additionally, space-charge-limited transport theory indicates that efficiencies will scale with temperature and conductivity squared and the Seebeck coefficient cubed, with the ability to exceed 10% when nanowire diameters are reduced to 20nm[20]; thus our results presents a possible path to achieve electrical power generation via TE devices with non-linear current-voltage characteristics. As nonlinearity, or the fill factor often used for PV, increases so does efficiency. Therefore it would be desirable to have high enough doping for low resistance contacts while keeping the doping low enough that the nanowire networks still operate in the space-charge-limited transport regime.

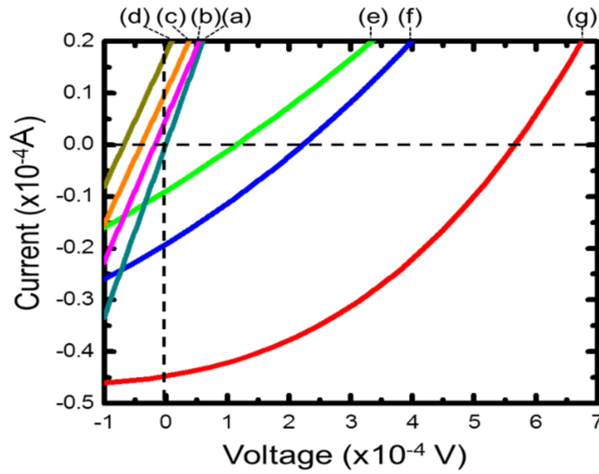

Figure 7.4. Current versus voltage curves are shown for the single-stage InP TE device (a-d) and the double-stage InP/Si TE device (e-g); with varied temperature differences across the two devices; a) Δ0 ˚C, b) Δ30 ˚C, c) Δ41 ˚C, d) Δ50 ˚C; and e) Δ5˚C, f) Δ20˚C, g) Δ51˚C.

Table 7.1 Values of P_{max}, I_{sc}, and V_{oc} for each TE device at ~ Δ50 ˚C,

	I_{sc} (μA)	$V_{oc}(mV)$	P_{max} (nW)	Normalized power (nW/°C)	FF (fill factor)
InP	20	0.08	.4	.08	0.025
InP/Si	-40	.6	10.4	.2	0.433

The power output along with current-voltage characteristics for the single-stage InP TE device at Δ50˚C is shown in Figure 7.5a. Figure 7.5a shows the maximum power output of this device is ~0.4nW, a normalized power of $8x10^{-11}$W/˚C. The small power output is attributed to the weak doping of the p-type InP nanowires. When this weakly doped p-type InP nanowire layer is covered with the

intentionally doped n-type PECVD Si layer, the overall electrical conduction results in n-type behavior, as seen in the I-V curves (a)-(d) in Figure 7.4, suggesting that these two semiconductors, InP and Si, having Seebeck coefficients with opposite signs work against each other. Therefore, using the same conduction type (i.e. either n-type or p-type) for both the InP nanowires and the PECVD Si layer could have worked complementarily. In other words, having a consistent doping type for the two materials that need to be combined in this device architecture is critical to increase the power output by increasing the combined Seebeck coefficient.

Figure 7.5b reveals that the double-stage InP/Si TE device produced a maximum power of ~10.4nW at $\Delta 51^{\circ}C$ (i.e., normalized power ~$2x10^{-10}$W/°C). The normalized power increased approximately 25 times compared to that of Figure 7.5a, with the addition of the Si nanowire network layer. V_{oc}, I_{sc}, and other TE characteristics for the two devices are summarized in Table 7.1, showing that the addition of the extra layer of nanowires increases the magnitude of I_{sc} by a factor of two, and increases V_{oc} by a factor of 7.5.

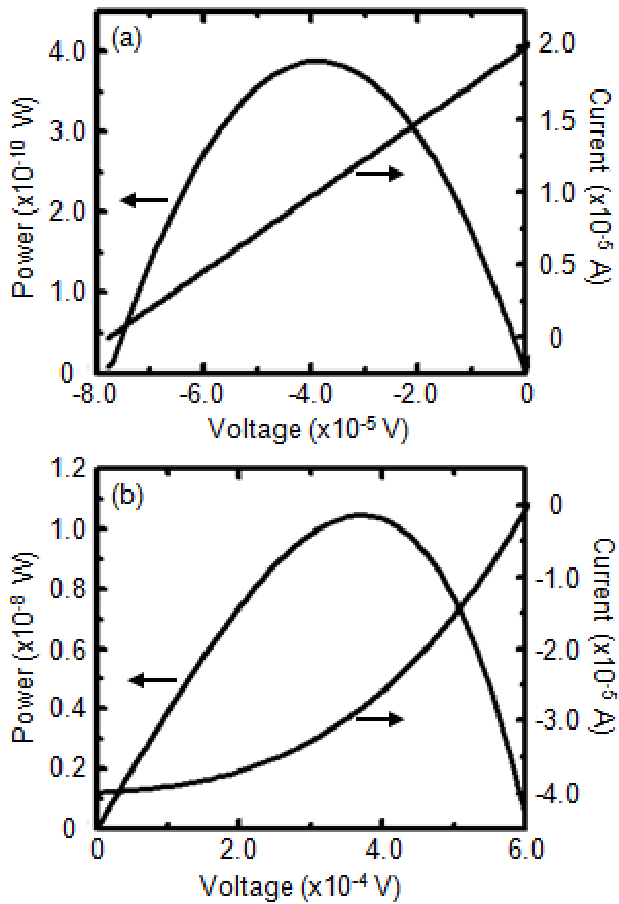

Figure 7.5. Power and Current versus voltage curves at ~50˚C temperature differences are shown a) for the single-stage InP TE device and b) for the double-stage InP/Si TE device.

Power output of these samples are low; however the major cause is identified and can be alleviated by, for instance, properly doping nanowires and semiconductor layers (e.g. PECVD Si and Evaporated Si in Figures 7.1a and 7.1b) present in a TE device. Despite significant performance limitations associated with doping and combining nanowires having opposite conduction types in the studied TE devices, the potential anticipated for the concept (i.e. multi-stage TE devices with non-linear current-voltage characteristics) presented here is clearly seen in producing electrical

power within a non-linear current-voltage curve with a fill factor much larger than that obtained for a linear current-voltage curve found in conventional TE devices. Additionally, with the other attributes of mechanical flexibility and resulting scalability given in the studied TE devices, the concept could present a viable option for specific applications for heat sources with a large area and/or an odd shape. For instance, with consistently doping different materials, a multi-stage TE device can be optimized for a large temperature gradient, utilizing specific materials with bandgaps [31] appropriate for different temperature ranges. Furthermore, our device architecture allows to build a TE device that has a thickness much larger than that can be obtained by conventional thin film deposition technologies or bulk semiconductor technologies, offering a new pathway to create a large temperature gradient.

Conclusion

We presented a new concept that can be applied for TE devices for electrical power generation. The concept is built upon multiple-stage TE cells that are made of different semiconductor materials and that exhibit non-linear current-voltage characteristics. The origin of the nonlinearity has not been conclusively identified in the current study and is the focus of continuing study; however, several possible sources were considered; the presence of a Schottky barrier and/or the space-charge-limited transport regime, either of which (or both of which) could be built in the double-stage InP/Si TE devices presented in this paper.

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Part II Resistive Switching Materials Growth and Characterization

Chapter 8

Investigation of a Nanoscale TaOx Resistive Switching Device

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ABSTRACT

Resistive switching, a reversible change in electrical resistance of a dielectric layer through the application of a voltage bias, has propelled a field of research to form improved non-volatile memory device. Tantalum oxide has been investigated as the dielectric component of resistive switching devices as a leading candidate for a few years. Presented here is a structural and chemical investigation of TaOx devices with 55nm in diameter in the virgin, forming on, and switched off (reset) states for

comparison using cross sectional TEM techniques including HRTEM, and EELS to gain further understanding of this material system. The nanodevices imaged in this study were switched below 100uA. Unique features found in this study are in agreement with previous hypotheses made by various researchers based on X-ray fluorescence microscopy of micron-scale devices, indicating a variation in oxygen concentration around the switching area.

Keyword: resistive switch, memory, memristor, Tantalum oxide, nanovia

Introduction

Resistive random access memory (RRAM) is a type of nonvolatile random-access memory that has gained significant attention as a potential next generation memory device[1], [2]. RRAM operates by the change in resistance across a dielectric solid state material such as TiO2, TaO2, HfO2, Al2O3 etc[3]–[5]. Many studies have been performed on various switching materials to understand the switching mechanisms [6]–[9]. It has been found consistently that the drift/diffusion of oxygen vacancies controlled through an electric field and/or a thermochemical reaction is believed crucial to our understanding of these systems[6], [7], [9], [10]. Visualizing the actual active region is critical to understand the details of the microscopic picture of the switching [9], [11]. For example TaOx has an amorphous conduction channel where switching occurs through compositional modulation of the channel whereas it has been observed that TiOx has a crystalline conductive channel where switching is performed through gap modulation of the channel. Tantalum oxide

has shown excellent performance with reports of endurance exceeding 10^{10} open loop cycles [12], [13]. Titanium oxide produces desirable nonlinear current-voltage characteristics[7], [11]. Ti is a very reactive metal and a strong oxygen-getter, and therefore likely to interact with the TaO2 switching layer. With these devices it is intended to take advantage of TiOx switching behavior along with the endurance characteristics of TaOx. This design is investigated here using current-voltage characteristics as well as transmission electron microscopy (TEM) and electron energy loss spectroscopy (EELS) analysis.

Experiment

Figure 8.1 depicts the schematic of the as deposited devices studied here. The bottom electrode is a 55nm TiN via bottom electrode, connected to a 150nm W line fabricated on a Si wafer. To ensure a clean bottom electrode prior to the deposition of the switching layer the substrate is ultrasonically cleaned with acetone and IPA, then reactive ion etched (RIE) with oxygen plasma for 30 seconds and finally ion milling etched at 400Watts for 90 seconds in Ar gas. The TiN via is surrounded by 20nm SiO2 / 15nm SiN isolation layers. A TaO_2 switching layer (4nm thick) was deposited by reactive RF sputtering using a tantalum oxide target (nominal composition to be TaO_2) with an Ar gas flow of 6 sccm and an O2 gas flow of 0.26 sccm. Metallic Ti and Pt top electrode layers were defined by photolithography and deposited by electron beam deposition at ambient temperature to thicknesses of 10nm and 20nm, respectively at 0.45µmBar and a rate of 1Å/s.

Current-Voltage measurements were performed on the fabricated switching devices using an Agilent 4156c parameter analyzer. An FEI NOVA dual beam was utilized for cross sectioning, where the devices was protected with e-beam Pt followed by i-beam Pt prior to trench and cleaning. HRTEM and EELS were taken using a FEI Titan at 300kV. HRTEM was utilized to study the three devices in the three different states: the virgin, ON, and OFF states.

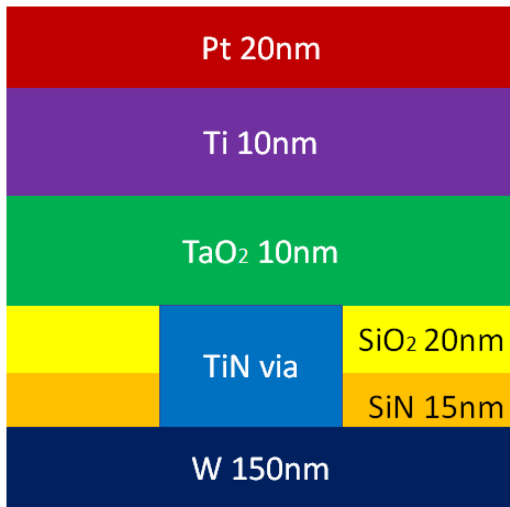

Figure 8.1: a) Schematic of memristive device (not drawn to scale). In frame from bottom up: W bottom electrode line, 55nm diameter TiN via surrounded by a SiO_2, SiN isolation layers, 10nm TaO_2, 10nm Ti and 20nm Pt top contact.

Results and Discussion

Current−voltage (I−V) curves from three 55nm-diameter devices are shown in Figure 8.2. Figure 8.2a depicts the I-V curve of the device in the virgin state (i.e. it was as fabricated). Figure 8.2b shows the I-V characteristics obtained from a device being turned to the ON state for the first time, showing the transition from the virgin state to the ON state. After being set to the ON state for the first time, this device was

prepared for TEM imaging. Figure 8.2c depicts the I-V characteristics obtained from a device being turned OFF after a single cycle voltage sweep and left in the OFF state, representing a device that underwent the ON state and was set to the OFF state. It should be noted that the following analysis was done on three separate devices, as described above, explicitly set to the virgin, ON, and OFF states. Since all studied devices had comparable I-V characteristics when at the virgin state, we strongly believe that the variations seen in the analysis were intrinsic and resulted from controlled specific operations (i.e. virgin, ON, and OFF) individually done on a specific device.

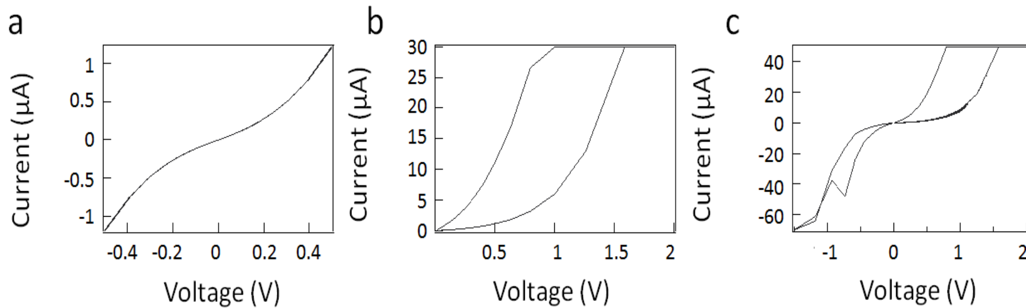

Figure 8.2: Current−voltage (I−V) of the three cross sectioned devices presented in this study; a) the virgin state, b) the transition from the virgin state to the ON state, and a cycle of a device from the virgin state to the ON state and from the ON state to the OFF state.

Cross-sectional TEM images in Figure 8.3(a),(b), and (c) show prepared devices set to the virgin, ON, and OFF states, respectively. In Figure 8.3(a) representing the virgin state, a test structure was prepared as was for TEM imaging to compare several as deposited devices. The test structure as deposited device shown in Figure 8.3a is 75nm in diameter. The TaO_2 layer appears to contain granular formations in the as deposited switching layer. The TaO_2 layer is followed by a Ti layer. Noticeably, the

Ti top electrode layer appears to be much thinner than the nominal fabrication thickness, 4nm rather than 10nm. Since the deposition rate of Ti routinely calibrated for its highest accuracy and precision further investigation is required. It is unlikely that the entirety of this discrepancy can be attributed to inaccuracy of the e-beam evaporator as the as deposited Pt is ~19nm, effectively the nominal fabrication expected value of 20nm. Therefore it is likely that the Ti layer has partially oxidized upon the establishment of a contact with the underlying TaO2 layer, adding TiOx to the top of the TaO2 layer, which provides a reason for the TaO2 layer that appears to be much thicker than its intended thickness of 10nm.

Core-Loss EELS relative mapping for the three cross sectioned devices studied here are shown in Figure 8.4. The as deposited test structure device is shown in Figure 8.4a. The core-loss EELS quantification indicates there is twice as much oxygen as tantalum in the as deposited film. Notably, the EELS map of the virgin state also shows that the Ti top electrode is slightly oxidized and that some Ti has migrated into the TaO2 switching layer. This would confirm chemically that when Ti contacted the TaO2 switching layer it began to react, diffusing and attracting oxygen away from tantalum. The core loss EELS of the as deposited device shows the as deposited structure and that the cross section is only partially nanovia and substantially isolation layer.

Figure 8.3b shows the device in the ON state. Figure 8.3b shows TEM of the device whose electrical testing is shown in Figure 8.2b. The TaO_2 has developed three features above the 55nm TiN nanovia, this will be referred to as the active

region. This region appears to be amorphous. The active region appears to be contained within the TaO_2 layer, below the Ti layer, and the Pt layer which appear to have thinned at the location of the device. The EELS compositional mapping of the same device is shown in Figure 8.4b. The EELS mapping, along with lateral core loss compositional line scans, indicate there are three tantalum and titanium rich regions in the ON state cross sectioned device with corresponding drops in oxygen concentration. In the ON state the core loss composition averages approximately 1 Ta : 1 Ti : 2 O over the active region. However in the metallic rich regions that drops to Ta : Ti : O. Therefore core-loss EELS indicates that is a highly metallic rich device. The low resistance ON state of a TaO_2 resistive switch has metallic and oxygen rich sections creating a compositional filament like structure whereas the ON state of a TiO_2 device is a gap modulated mechanism [6], [7], [10]. Therefore this data would indicate that this device is more consistent with a TaOx switch as the active region is amorphous and there is significant compositional modulation. Additionally in the core loss EELS map shown in 8.4b, it can be seen that there is very little isolation layer contained in the cross section aligned with the nanovia indicating the majority of the signal from the active region is from above the via, quantitatively ~95% of the cross section.

Bright field TEM of the Off state device is shown in Figure 8.3c. This is a different device from the on state device shown in Figure 8.3b as this was an ex-situ study and therefore cannot be compared quantitatively. However, the active regions of both devices are observed to be contained within the TaO2 layer with similar

contrast. Again the Ti layer appears to accommodate the deformation while the Pt thinned above the activated region. Due to time limitations a lower resolution EELS map shown in Figure 8.4c was taken however it allowed us to determine that only ~70% of this cross section was device therefore further making any numerical data from the device incomparable to the ON state. Rather Figure 8.4c tells us that again the Ti top electrode was oxidized and that there is Ti in the TaO2 layer. However TEM of this device shows that the active region is a permanent deformation present in both states of the device after forming. Core Loss data shows that in the area of the active region the nitrogen levels extend past the via and could have contributed to the deformation seen in the active region.

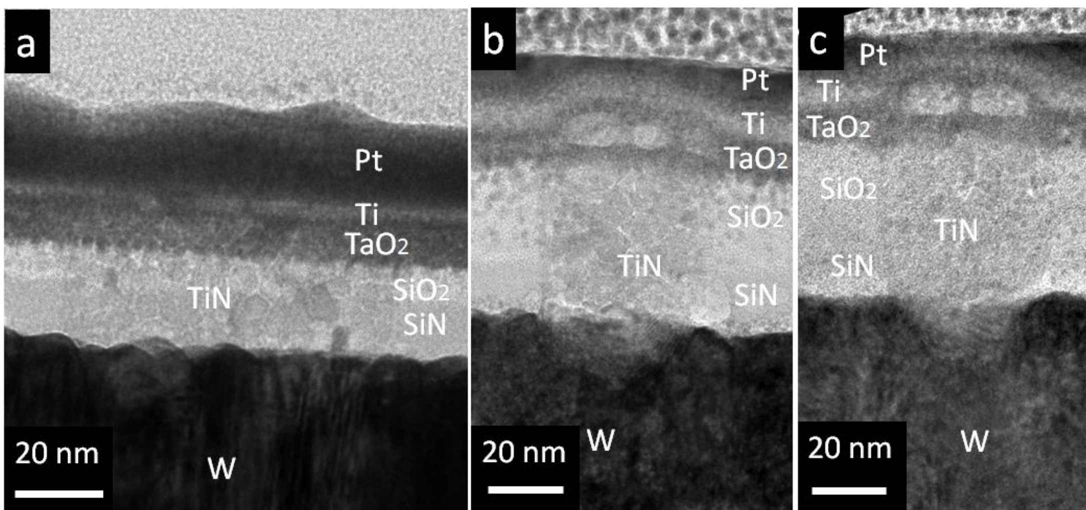

Figure 8.3: High-resolution TEM images of three TaO2 devices cross-sectioned in a) the virgin state, b) the ON state and c) the OFF state corresponding to the IV curves shown in Figure 8.2 a-c.

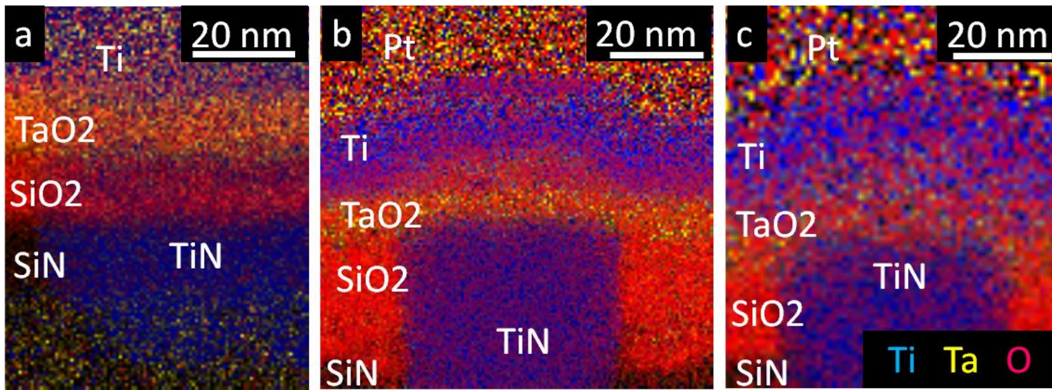

Figure 8.4: EELS elemental mapping of three cross-sectioned TaO2 devices to determine the locations of Ti, Ta, and O in a) the virgin state, b) the On state and c) the Off state.

Conclusion

Here we have presented the study of resistive switch designed to take advantage of the high endurance of TaOx with a TaO2 switching layer and the current-voltage attributes of TiOx with a Ti top electrode which would oxidized on contact with TaO2. Core loss EELS mapping and linescans as well as TEM contrast indicate metallic rich areas within the active region of the cross sectioned device in the ON state. The presence of similar amorphous active regions in the On and Off states but modulated composition indicate the switching mechanism is similar to TaOx in those respects. This device study illustrates how various materials can combine to create devices utilizing the strengths of each material. This study also demonstrates the importance of top electrode material selection in the behavior of a resistive switching devices as interface interactions and mobile species play a key role in the actual behavior of devices. The comparison study has also revealed that the

biggest morphology change inside the device is typically caused by the very first electrical operation while the change is very subtle between ON and OFF states.

Acknowledgements

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Chapter 9

Self-Aligned NbO2 nano-cap for Negative Differential Resistance Resistive Switching Devices

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ABSTRACT

Resistive switching devices with highly non-linear current-voltage characteristics are required for memory arrays based on the cross-bar architecture to minimize electrical cross-talk among a large number of resistive switching devices at different memory states. In this paper, a self-aligned fabrication process of a NbO2 "nano-cap" is explicitly developed and successfully integrated atop a TaO2.2 switching layer to fabricate a resistive switching device with highly non-linear negative differential resistance (NDR) current-voltage characteristics.

Keyword: resistive switching, nonlinear, memristor, selector, nonlinearity, insulator-to-metal transition

Introduction

Resistive Random Access Memory (RRAM) devices are two terminal electrical resistance switches that retain a state of internal resistance based on the history of applied voltage and current. The occurrence of reversible resistance switching has been widely studied in a variety of material systems for applications including nonvolatile memory, logic circuits, and neuromorphic computing [1]–[3]. These devices can be used for computing by both storing and processing information. These cross point devices are usually used in a crossbar array for real applications[4], [5]. Most RRAM devices including those based on TaO2 and TiO2 switching materials have a linear or slightly nonlinear ON state current-voltage relations [6]–[9]. Consequently, when reading or writing a bit of a switch all the other switches connected to the common line are partially selected, which further results in sneak path currents [10]. Therefore, for large memory array applications, nonlinearity is desired to mitigate the sneak path leakage issue, which severely limits the size of the crossbar arrays and thus the density of the memory. This can be achieved with the utilization of a nonlinear selector in series with a resistive switch at each cross point. To address this here we investigate a stack that has been designed to combine resistive switching with a built-in selector.

Experiment

Figure 9.1a depicts the schematic of the as deposited device studied here. The bottom electrode is a TiN via with a diameter of 75nm, connected to a 150nm W line

fabricated on a Si wafer. To ensure a clean bottom electrode prior to the deposition of the switching layer the substrate is ultrasonically cleaned with acetone and IPA, then reactive ion etched (RIE) with oxygen plasma for 30 seconds and finally ion milling etched at 400Watts in Ar gas for 90 seconds. The TiN via is surrounded by 20nm SiO2 / 15nm SiN isolation layers. A TaO2.2 switching layer (4nm thick) was deposited by reactive RF sputtering using a tantalum oxide target (nominal composition to be TaO2.2) with an Ar gas flow of 273 sccm and an O2 gas flow of 77 sccm. Metallic Nb and Pt top electrode layers were defined by shadow masks and deposited by electron beam deposition at ambient temperature to thicknesses of 30nm and 10nm, respectively at 2.2μTorr and a rate of 1Å/s.

Figure 9.1b shows a device structure intended to exhibit highly non-linear resistive switching. NbO2 is a negative differential resistance (NDR) material, resulting in a highly nonlinear I-V relation in a device stack [11], [12]. This is because when NbO2 is heated by Joule heat it undergoes an insulator to metal transition once the temperature is over the insulator-metal-transition (MIT) temperature, i.e., 1081K for NbO2 [11]–[15]. During the initial electrical conditioning described later, the device structure in Figure 9.1b is expected to result from the as-fabricated device structure shown in Figure 9.1a. The electroforming process creates a conduction channel (nanofilament) in the TaOx layer. The conduction channel consists of Ta-O solid solution with oversaturated O, which is a strong oxidizing agent and oxidize the part of the Nb metal on the tip of the conduction channel when the channel experiences a local high temperature induced

by a high current during the subsequent operations. Either NbO_2 or Nb_2O_5 may form thermodynamically. However, under high electric field an electrically conducting phase is preferred. The reason is that if a nonconducting phase forms, a large voltage drop will be concentrated on this phase and electroform this phase into a conducting phase eventually. The local temperature during electroforming might be over the MIT of NbO_2 and thus make NbO_2 an electrically conducting phase during electroforming. Therefore, NbO_2 is naturally formed just within the local region of the conduction channel tip. This approach can be used to form a self-aligned NbO_2 nano-cap on the filament for nonlinear resistive switching. Current-Voltage switching curves were performed using an Agilent 4156c parameter analyzer. Helium ion microscope was used to locate the devices studied and marked with 1µm crosses 1µm away from the devices for identification in a FEI NOVA dual beam for cross sectioning, where the device was protected with e-beam Pt followed by i-beam Pt prior to trench and cleaning. HRTEM and EELS were taken using a FEI Titan at 300kV.

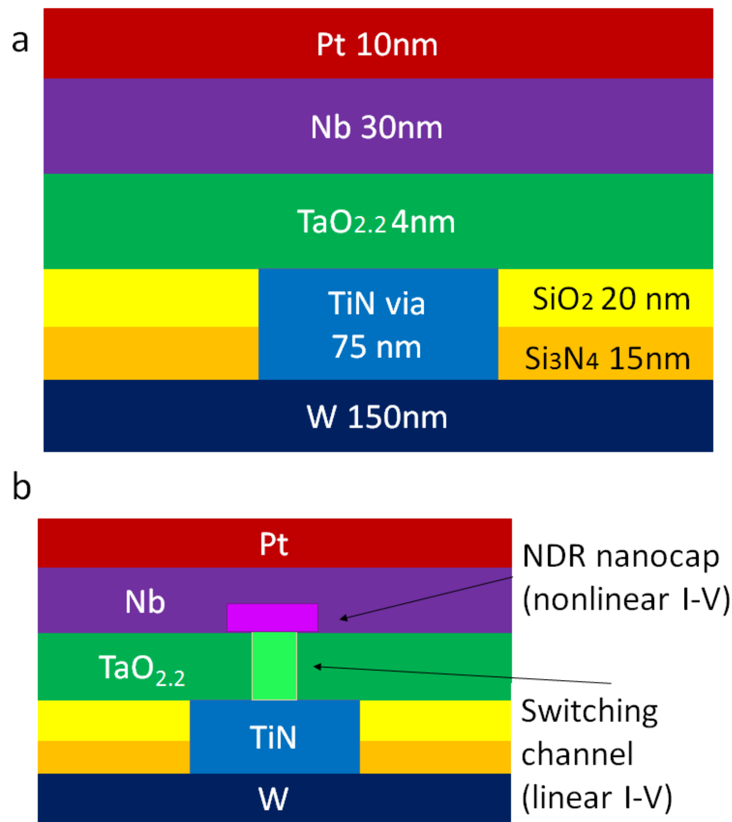

Figure 9.1: a) Schematic of memristive device (not drawn to scale). In frame from bottom up: W bottom electrode line, 75nm diameter TiN via surrounded by SiO2 and SiN isolation layers, 4nm $TaO_{2.2}$, 30nm Nb and 10nm Pt top contact. b) post activation schematic showing how the nonlinearity arises, with $TaO_{2.2}$ behaving as a resistive switch and NbO_2 behaving as a selector.

Results and Discussion

I-V curves collected from the device schematically shown in Figure 9.1a are shown in Figure 9.2. Figure 9.2 a) shows that the device at the virgin state (e.g. as-fabricated device) was highly resistive. The device was then switched twice a 1µA with linear behavior consistent with a TaO_x switch and turned off with relatively large current level as shown in Figure 9.2b). This electrical operation induces the designed NDR behavior in this device, shown in Figure 9.2c. This would indicate the desired

NbO_2 region present in this device near the active TaO_x region as it has an insulator to metal transition when heated known to show NDR behavior. Figure 9.2d) depicts c) in semi-log.

HRTEM of the cross sectioned device in the Off state is presented in Figure 9.3a. The image shows the formation of two new regions (i.e. two regions that did not obviously exist in the designed device shown in Figure 9.1a). These two new regions (I) and (II) appeared to form on a region of the $TaO_{2.2}$ layer immediately above the TiN via and have distinguishable phases, labelled NbO_2 and Nb_2O_5 respectively. EELS relative compositional mapping shown in Figure 9.4 allows us to visualize the composition of the cross-sectioned device. Region II is shown to be oxygen rich. The fringe spacing and diffraction pattern of region II are consistent with monoclinic Nb_2O_5 and its diffraction pattern was consistent with the family of (111) planes. Figure 9.4 indicates that region I is a Nb rich region located above the TaO_x switching layer. Figure 9.3b, a HRTEM image of region I corresponds to the Nb rich region in figure 9.4. This region is consistent with NbO_2 through EELS quantification analysis, TEM fringe spacing and the diffraction pattern. The diffraction pattern and fringe spacing of Figure 9.3b, shown in 9.3c, indicates the region is NbO_2 with (222) and (400) planes. Within region I dark contract shows a metal rich path between two nitrogen regions below the NbO_2 nano-cap, this is a possible conduction path. The amorphous TaO_x switching region cannot be easily identified due to the disruption above the TiN via during the activation. Additionally as this device is in the OFF state the TaO_x region that become Ta rich in the ON state

will have experienced compositional modulation in being turned OFF making the detection of the active linear switching region impossible. Core loss EELS quantification indicates the presence of Ta and O beneath the Nb rich region, however with such a small region confirmation of the phase is not possible however previous experiments would indicate the presence of Ta2O5 [7]. Therefore it is possible that NbO2 is forming after TaOx switches, creating an oxygen saturated Ta-O solid solution region from which Nb can attract oxygen and form NbO2. The Nb rich "nanocap" can be seen in the HRTEM images and EELS elemental mapping. Therefore scientifically, this shows that even though Nb oxides are less stable than Ta_2O_5 thermodynamically, the formed Ta-O solution filament can oxidize Nb. Technologically, this approach can be used to form a self-aligned NbO2 nano-cap on the filament for nonlinear resistive switches.

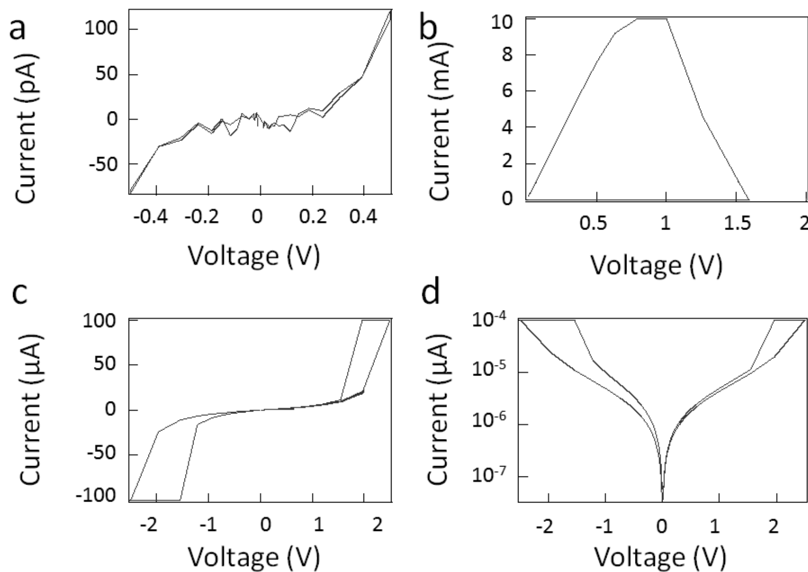

Figure 9.2: Current−voltage (I−V) of the cross-sectioned device in a) the virgin state, b) the hard switch on state, c) the following switching cycle showing NDR behavior, and d) in semilog scale.

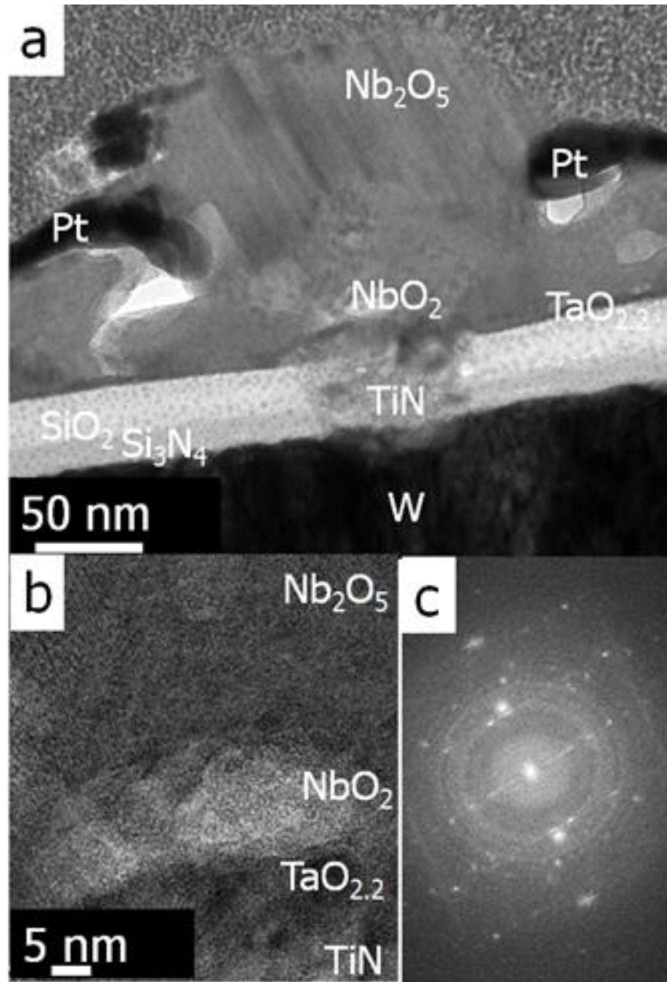

Figure 9.3: High-resolution TEM images of the OFF state cross sectioned device a) at low magnification, b) at high magnification in the location of the NbO2 nanocap with c) the corresponding diffraction pattern that shows the presence of 222 and 400.

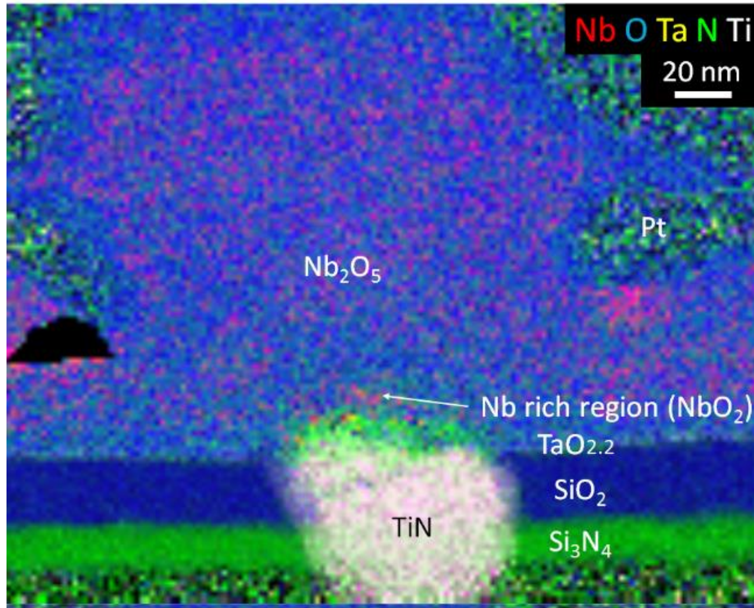

Figure 9.4: EELS elemental mapping of cross-sectioned TaO2.2 device to determine the locations of Nb, Ta, N, and O in the OFF state.

Conclusion

In summary, we have succeeded in creating a self-aligned nano-cap for nonlinear switching of RRAM devices. This nano-cap is composed of NbO2 and the deformed region surrounding the nano-cap is composed of Nb2O5. With the use of EELS composition mapping we were able to identify the non-linear element right above the TaOx switching layer centered atop the TiN nanovia. This study shows that even though Nb oxide is less stable than Ta_2O_5 thermodynamically, the formed Ta-O solution filament can oxidize Nb.

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The authors are grateful to HP labs, Stanford Nanocenter, and the MACS facility (Moffett Field, California) at Advanced Studies Laboratories, University of California

Santa Cruz, and NASA Ames Research Center for continuous support on analytical equipment. This material is based upon work supported by the National Science Foundation Graduate Research Fellowship under Grant No. DGE-0809125. Support by Semiconductor Research Corporation CSR fund (Dr. Victor Zhirnov) is also highly appreciated. This work would not be possible without the bottom electrodes provided by SK Hynix. We would like to acknowledge Jiaming Zhang, Max Zhang, Bill Thompson, and Katy Samuels for their contributions toward this work.

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Chapter 10

Future Work

10.1 Thermoelectric Devices

In chapters 2-7 I presented my work on thermoelectric materials. Nanowire networks are truly amazing forms of nature. Growth of these nanowire networks on various surfaces for optimal device configuration was extensively studied. This study gave me an deep appreciation for crystal structure and quantum effects. Additionally nanowire networks have the potential to be dense and thick. I believe that by recoating with Au additional layers can be created to form networks thick enough for direct top electrode deposition without electrical shortage. One of the areas of mystery I have yet to have fully studied is the intersection of nanowire networks. This is perhaps the most challenging aspect of a nanowire network to study and the most important to understanding whether it is truly beneficial to thermoelectric devices to form nanowires as networks rather than arrays. Previously it has been shown by Nobuhiko P. Kobayashi and Andrew J. Lohn that at room temperature quantum conductance can occur at these points, possibly affecting both electrical and thermal transport. However it is still not understood experimentally how phonons are affected by these intersections. I showed in the introduction TEM of a intersection and how the lattice changed where the nanowires grew together, fusing. Without experimentation it is unconfirmed and only theoretical how phonons are affected by intersections. I plan to create a TEM sample using an aduro protochip that will allow me to heat one arm of the four connected to an intersection at a time and observe how

the sample changes. Additionally scanning thermal microscopy could be utilized to investigate how phonons truly interact with the fused nanowire intersections in a network.

One aspect of my research that I found especially intriguing is nonlinear thermoelectric devices. I would like to form a nanowire pellet with an undoped semiconducting binding agent to test how the space-charge-limited transport regime behave on a large scale. I would also like to alter the doping concentration to find the sweet spot when the charge carriers still operate in the space-charge-limited transport regime and where they still make reasonable electrical contact to the applied electrodes. This test would help show how the fill factor can be turned by doping concentration in nanowires when this regime is used to maximize efficiency.

10.2 Resistive Switching Devices

Chapters 8 and 9 discussed resistive switching of TaOx devices. Each study shows the importance of top electrode materials. In both studies the top electrode participated in the device switching; in chapter 8 the Ti top electrode diffused and we observed TaTiOx switching while in chapter 9 we saw how the Nb top electrode interacted with the filament forming a self-aligned resistive switch and selector. In-situ study of these systems for complete understanding is my next steps, as with separate cross sectioned devices quantification of elements can't be directly compared. In situ studies would allow for conclusive evidence of the chemical and physical changes in each state.

The behavior of the TaTiOx system is intriguing in many ways. I would like to explore at what occurs as the composition of each material is altered. I plan to explore how TaTiOx behaves when TaOx and TiOx are co-sputtered rather than formed into a bilayer structure. Additional I believe this opens a whole new area of materials to explore for resistive switching when we move into ternaries and multi-layered structures for the switching region. Therefore if we liked the behavior of different aspects of specific materials they could be combined in a manner to take advantage of different material aspects. This could be applied not only to TaTiOx but to HfAlOx or TaSiOx, for example, in both bilayer and co-sputtered material systems.

An aspect of resistive switching that draws my attention is still the problem of sneak paths. As we have determined a method of forming a self-aligned selector atop a linear switching filament I feel this should be explored further. NbO_2 has too high of a insulator-metal transition temperature, 1081k. Unenclosed here for length reasons, VO_2 was also explored however its insulator-metal transition occurs at too low of a temperature. Therefore I plan to form a multi-layer structure so that V and Nb combine to form a phase of VNbOx with the hope that it will contain a insulator-metal transition as both of its component parts do. If that is unsuccessful I plan to investigate additional materials such as Cr and Ti4O7 that are known to display nonlinear current-voltage characteristics. Another possible route I plan to explore is the use of these materials as dopant in a linear switch such as SiO2 or TaOx to determine if the selectivity can be provided as part of the switching filament.