LBNL-41784
Preprint

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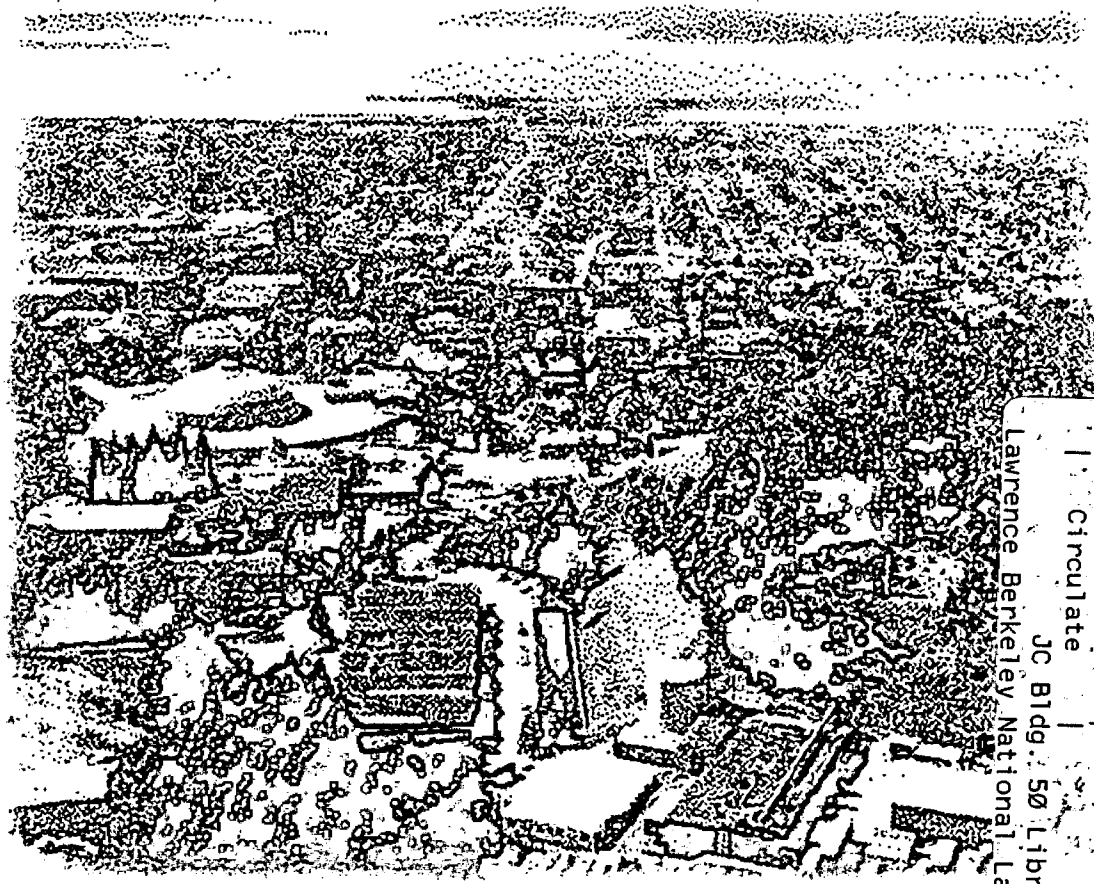
Engineering Division

May 1998

Submitted to
Nuclear Instruments and Methods in Physics Research A



DISCLAIMER

A Fast, Compact Solution for Low Noise Charge Preamplifiers[1]

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Abstract

A new structure for low noise charge sensitive preamplifiers, implemented using a transconductance gain stage plus a voltage gain stage, has been thoroughly investigated. Uniquely high values of open-loop gain have been demonstrated, together with good low noise performance and high load driving capability. Implementation of this scheme uses only a minimal number of commercial parts, resulting in a very compact and relatively low power circuit.

A detailed theoretical analysis of the dynamic response and noise performance of the circuit is given. Several tests and measurements have been performed to validate the theory and the results are presented.

[1] This work was supported by the Director, Office of Energy Research, Office of Basic Energy Sciences, of the U.S. Department of Energy under Contract No. DE-AC03-76SF00098.

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Introduction

Nuclear instrumentation has become a mature discipline, where the engineering challenge is often reduced to the selection of the most appropriate adaptation of an existing solution. Not surprisingly, charge sensitive preamplifiers often fall into this category of engineering challenge. The design of very low noise charge sensitive preamplifiers can be very demanding. For instance, the lowest noise preamplifiers commonly have noise floors ≤ 5 e^- [1-3]. More often, charge sensitive preamplifiers can have substantially higher noise floors without causing any significant consequence to the measurement. The design of these higher noise floor preamplifiers is addressed in this paper.

Theory of operation

The fundamental elements necessary to construct a low noise charge sensitive preamplifier are shown in Fig. 1, in block diagram form. A transconductance gain stage (implemented by the three terminal device T_{TD}) converts a small input voltage into a current that is then converted back into a larger voltage on the high impedance Z_1, thereby creating open loop gain. An output voltage buffer B_1 simultaneously drives both the feedback capacitor, establishing the closed loop transfer function, and the external load.

The low frequency open-loop gain is proportional to the product of the voltage-to-current gain of the input device (transconductance) and the value of the impedance Z_1.

The frequency behavior is dictated, as a first order approximation, by Z_1 (which may also include some parasitic elements of T_{TD}). Usually a small fixed capacitor is shunted to Z_1, to establish a controlled frequency response and thereby improve circuit stability, a technique known as "dominant pole compensation".

Many preamplifiers designed using this topology have shown excellent performance and are widely used. However, there are some limitations in the ratio of size/performance for these circuits, no matter which technology is used to build them. In fact, to achieve high values of low frequency open loop gain, wide bandwidth, high load driving capabilities and low noise, many modifications must be made to the simple scheme depicted in Fig.1, each adding several components. Such issues have always been a limitation in applications where high density is required but a fully integrated approach is not viable.

The technique discussed here constitutes one solution to these problems, offering high performance while using the lowest number of parts possible. Our idea is to combine the best features of commercially available operational amplifiers and low noise junction field effect transistors (JFETs) in a simple, cost effective, though Spartan manner. If an additional gain stage were interposed between the high impedance node Z_1 in Fig.1 and the output buffer B_1 the open loop gain could conceivably be increased without sacrificing the noise performance of the circuit. One possible implementation of such a gain stage is through the use of discrete components, the other is to use an operational amplifier. The approach with discrete components is known and documented [4], while the approach that uses an operational amplifier has not been investigated thoroughly. However, once realized, it would allow the instrumentation community to take advantage of all the features built into commercial operational amplifiers such as the capability to drive low impedance cables, short circuit proof output, low quiescent power etc. To realize this solution, the operational amplifier must satisfy the following criteria:

a) Its input voltage noise must be adequately low, i.e. must add little or no contribution to the total noise.

b) Its input current noise must also be low to ensure little or no contribution to the total noise.

c) The structure of its open loop gain must be such that the pole(s) added to the total open loop gain function ensures a condition of stability when the loop is closed.

d) Its slew rate must be adequately high for stability and linearity reasons (usually >1000 V/us).

To find such an operational amplifier that satisfies all criteria simultaneously is not a trivial task.

With the most recent improvements in operational amplifiers it has been possible to identify a few good candidates. We have fabricated and analyzed two preamplifiers with this topology.

In the circuit shown in Fig.2, the JFET (J_1) is the input device, the resistor R establishes proper biasing, as does the voltage source V_B. The loop is closed through the capacitor C_F. The speed of this circuit is limited; in fact, a pole is created by the presence of the parasitic capacitance between gate and drain of the input device (C_{GD}). This capacitance is amplified at the drain of J_1 by the Miller effect (expressed by 1+ the voltage gain between the gate and the drain of J_1 - $MG = g_m \cdot R$), therefore the pole, given by the product $R \cdot (1+MG) \cdot C_{GD}$, is placed at low frequency. A typical value for the frequency of the pole, when J_1 is an InterFET NJ450 at I_D=3 mA, is ~6 MHz. To reduce this effect, a simple solution has been adopted

(see Fig.3). The JFET J_1 has been cascoded with another field-effect transistor (J_2). The JFET J_2 is a selected device with a high pinch off voltage and a large I_{DSS}, we used a commercially available U311. The selection criterion of J_2 establishes the drain voltage of J_1. This small modification pushes the pole (now at the drain of J_2) to a much higher frequency, as the Miller term is no longer present (typically 60MHz). This solution has the additional benefit of wider choice of drain currents through J_1 (therefore on its transconductance) because it is possible to add the resistor R_2 directly to the drain of J_1 without significant degradation of the noise performance.

The cascode transistor could be a bipolar junction transistor, but in this case an additional voltage would be required to bias its base and the logarithmic impedance of its base-emitter junction could also introduce an undesired instability in the loop.

The cascode JFET J_2 introduces a high frequency pole and a zero in the open-loop transfer function due to its gate to drain capacitance. However, for practical values of the parameters, the pole and the zero fall in the same position, therefore no high frequency shift is introduced and the only pole is given by the product between R_1 and the parasitic gate to drain capacitance of J_2. This means that at high frequencies the capacitance between the source and the drain of J_2 has a feed-forward effect on the signal, compensating for the additional delay introduced by J_2 and thereby stabilizing the circuit.

When the previous configuration is adopted, the open loop gain DC value of the system is defined by the product of the voltage gain from the gate of J_1 to the input of the operational amplifier and by the open loop gain of the operational amplifier itself. In other words, if A_0 is the DC open loop gain of the operational amplifier, g_{m1} is the transconductance of J_1 and $A_{v,0}$ is the open loop gain of the whole circuit:

$$A_{v,0} = g_{m1} \cdot R_1 \cdot A_0$$

In practice, for g_{m1}=30mA/V, R_1=1kΩ and A_0=80 dB, $A_{v,0}$=110 dB. As stated before, the pole set by R_1 and the gate to drain capacitance of J_2 create the high frequency limitation. When it is necessary to further limit the high frequency behavior, this is easily done by splitting R_1 for the AC signal such that $R_{1a}+R_{1b}=R_1$, as shown in Fig.4.

This technique of setting the dominant pole by changing the DC value of the open loop gain has the drawback that, as will be demonstrated later, the noise can be increased if too low a value of R_{1a} is needed.

Noise Analysis

A noise analysis of the circuit is straightforward once the main noise sources are introduced in the general scheme of Fig.3. The dominant sources of noise are the JFETs, the operational amplifier and the load resistor R_1. The contribution of the feedback components depends on how the DC charge restoration of C_F is implemented and is beyond the scope of this paper. We will also assume ideal power supplies. The sources of noise in the JFETs can be represented as a voltage source in series with the gate and a current source between gate and source. The first takes into account the thermal nature of the noise in the JFET's channel and of the imperfections present. The second relates to the granular nature of the gate current. The noise of the resistor R_1 is represented as a current source in parallel with the resistor itself. The operational amplifier's contribution is modeled with its total equivalent series and parallel input noise. When the above contributions are accounted for, the equivalent circuit shown in Fig.5 can be used for the noise analysis. The single contributions to the equivalent input series noise of the sources depicted in Fig.5 are given by Formula (1) to (4). The contributions have been calculated in an open-loop configuration, since, as demonstrated [5], the result does not change for the closed-loop configuration.

(1) $$\frac{\overline{v_{J2}^2}}{g_{m1}^2 \cdot r_{ds1}^2}$$

(2) $$\frac{\overline{i_{R1}^2}}{g_{m1}^2}$$

(3) $$\frac{2 \cdot \overline{v_{OA}^2}}{g_{m1}^2 \cdot R_1^2}$$

(4) $$\frac{\overline{i_{OA}^2}}{g_{m1}^2}$$

The expressions for the noise spectral densities for the JFETs and for the resistor R_1 are:

(5) $\overline{v_{J1}^2} = \frac{4kT \cdot \Gamma}{g_{m1}}$

(6) $\overline{v_{J2}^2} = \frac{4kT \cdot \Gamma}{g_{m2}}$

(7) $\overline{i_{R1}^2} = \frac{4kT}{R_1}$

Typical values for the parameters in Formula (1) through (4) and Eq. (5) through (7) are given in Tab.1. Clearly, the input device J_1 contributes the dominant portion of the total noise present at the output of the circuit. There is also contribution coming from the load resistor R_1 that is significant for high values of g_m and low values of R_1. This situation is not uncommon because low values of R_1 are needed to compensate the circuit when the open-loop gain is particularly high. This contribution can be, in theory, up to 5%. In practice, larger contributions can occur if insufficient care is taken in the design of the circuit.

Performance of the Circuit

A preamplifier using the topology of Fig. 3 has been constructed and evaluated, using an InterFET 2N6453 as the input device. The main characteristics of the 2N6453 are shown in Tab.2.

As a second gain stage in the loop we have successfully used two different commercial operational amplifiers, the National Semiconductor LM6171 [6] and the Maxim MAX477 [7].

Fig. 6 shows the response of the circuit using the LM6171 to a short duration positive charge pulse with different capacitive loads connected to the preamplifier input. Some of the circuit construction parameters were: the drain current of J_1 is 10mA (close to its I_{DSS}); the feedback capacitor C_F is 0.5pF and the DC charge restoration is done by connecting a 10^{11} Ω resistor across C_F. It is interesting to point out that the circuit was driving a 50Ω cable shunt-terminated at its far end. This test was performed for three different values of input capacitance C_D (0pF, 196pF and 675pF), each time optimizing the open-loop gain, to obtain the best response. The waveforms were normalized to an arbitrary value. Fall time for the three cases were 11ns, 41ns and 71ns respectively.

The normalization of the output waveforms to an arbitrary value hides the fact that the amplitude of the voltage step decreases as C_D increases, because the input capacitance not only affects the dynamic response of a feedback system, it also changes the DC value of the closed-loop gain. However, for

completeness, this has been evaluated by setting the optimal response for C_D=0pF, measuring the value of the step and comparing it with that measured for C_D=196pF and C_D=675pF. The measurements were done by passing the preamplifier output through a two pole pseudo-Gaussian pulse shaping amplifier with a 1.6μs peaking time and measuring the amplitude of the waveform obtained with a pulse height analyzer. This process also tests the open-loop gain because the effect of the input capacitance is mitigated by the DC value of the open-loop gain. A parameter that takes into account the effects of the input capacitance on the performance of the circuit is the closed-loop gain demand, roughly defined as $GD \approx C_D / C_F$. This parameter is an index of what fraction of the open loop gain is used to drive the capacitive load presented by the input capacitance. The higher GD, the lower the open loop gain available for stability and to drive additional external loads.

The measurement has shown a variation in the peak amplitude of ~1.1% from C_D=0pF to C_D=196pF and ~2.3% from C_D=0pF C_D=675pF. This situations correspond to an open loop gain demand of ~400 and ~1300 respectively. The latter is the worst case because it represents the lowest possible open-loop gain available. The measurement indicates that, despite the high open loop gain demand, the open-loop gain available is still ~60,000.

It should also be noted that the previous measurement does not represent an ideal real-life situation, because a small device such as a 2N6453 would be poorly matched to such a large input load [4]. However, we believe that in this case the implementation of such a test was acceptable in order to demonstrate the performance of the circuit.

Fig. 7 presents the noise levels attained. For these measurement the InterFET 2N6453 was operated at I_D=10mA. Measurements were made at three different values of C_D assuming ε= 2.96eV [8]. The consideration of the large capacitive mismatch between the input capacitance of J_1 and the detector capacitance, C_D=196pF, still applies.

The values in keV FWHM of the points of the graph of Fig.7 are shown in Tab.3.

Conclusions

We have presented a new design of a fast, low noise charge preamplifier implemented on a two gain-stage loop. Although this approach has been studied in the past, it had never lent itself to a simple solution. Only by taking advantage of the results of the latest technological improvement has it been possible to design a very compact, inexpensive and simple circuit. Despite its appearance and simplicity, this circuit performs as well as other commonly used configurations and, is therefore suitable for use in most of the applications where high bandwidth and low noise are fundamental requirements.

Acknowledgements

The authors of this paper wish to acknowledge Fred Goulding, Donald Landis, Paul Luke, Pier Francesco Manfredi, Jacques Millaud and Dick Pehl for their valuable comments and suggestions during the preparation of this work.

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Disclaimer

Reference to company or product names does not imply approval or recommendation of the product by the University of California or the U.S. Department of Energy to the exclusion of others that may be suitable.

Figures

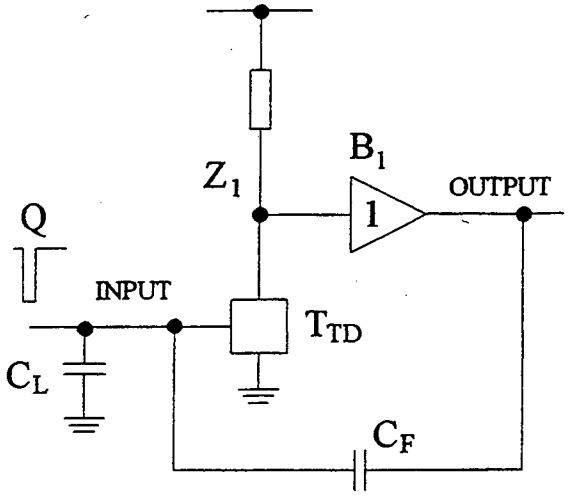

Figure1

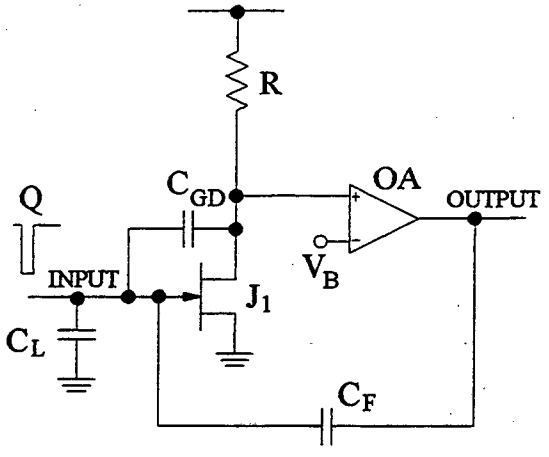

Figure 2

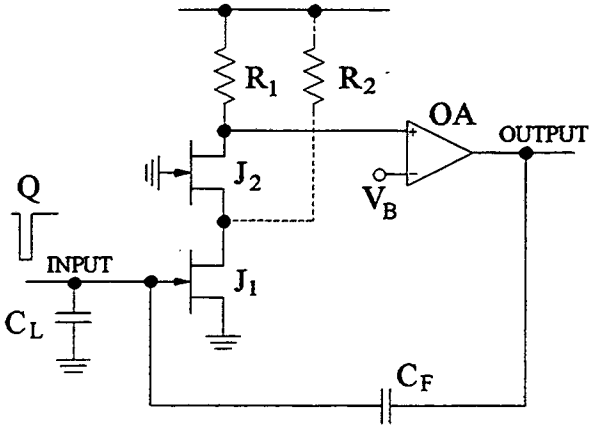

Figure 3

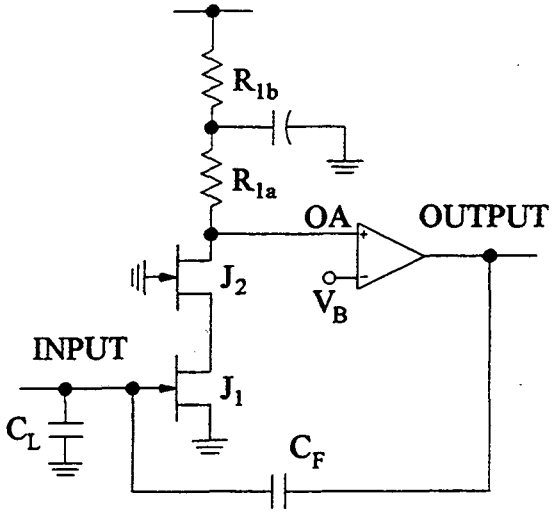

Figure 4

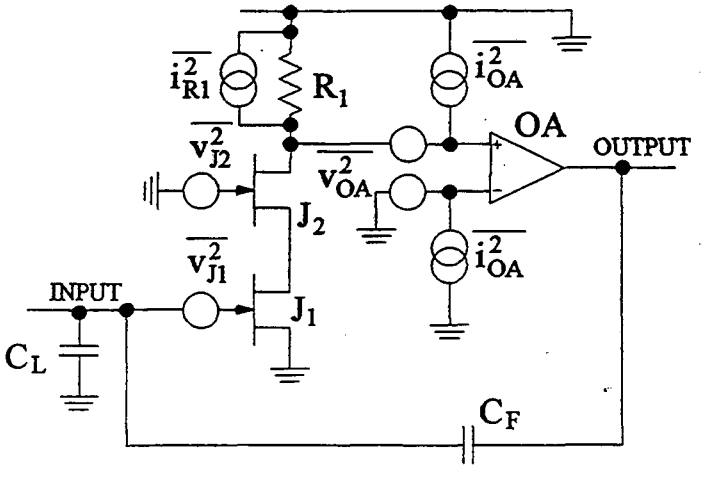

Figure 5

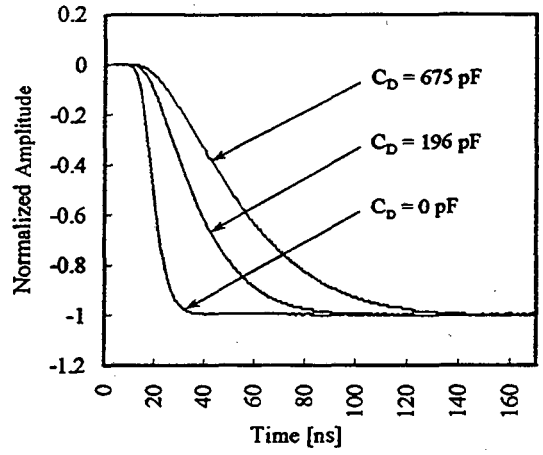

Figure 6

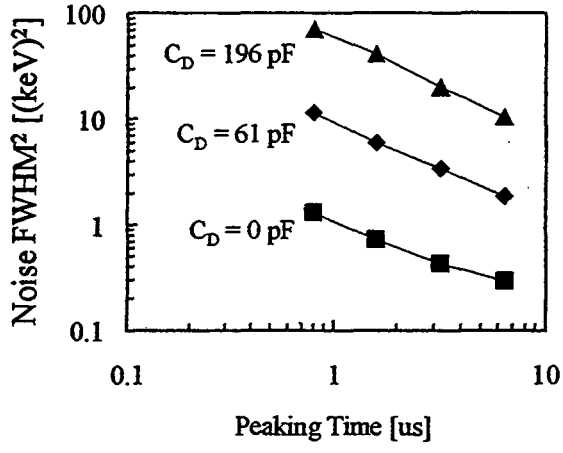

Figure 7

Figure Captions

Figure 1: Block diagram of a low noise charge sensitive preamplifier.

Figure 2: First-order implementation of a two-gain stage charge sensitive preamplifier.

Figure 3: Second-order implementation of a two-gain stage charge sensitive preamplifier.

Figure 4: Dominant pole adjustment.

Figure 5: Main noise sources in a two-gain stage charge sensitive preamplifier.

Figure 6: Output waveforms as a response to an input charge pulse for different input capacitive loads.

Figure 7: Resolution vs. peaking time for three different capacitive input loads.

Tables

Symbol	Meaning	Typ. Range/Value
g_{m1}	Transconductance of J1	5~50 $\frac{mA}{V}$
g_{m2}	Transconductance of J2	15~30 $\frac{mA}{V}$
R_l	Load Resistor	300~3000 Ω
$\overline{v_{OA}^2}$	Equivalent Series Noise Spectral Density at the input of the OpAmp	$2.5 \cdot 10^{-17}$~$1.4 \cdot 10^{-16}$ $\frac{V^2}{Hz}$
$\overline{i_{OA}^2}$	Equivalent Parallel Noise Spectral Density at the input of the OpAmp	$1 \cdot 10^{-24}$ $\frac{A^2}{Hz}$
Γ		0.7
T	Absolute Temperature	300 K
k	Boltzmann's Constant	$1.38 \cdot 10^{-23}$
r_{ds1}	Drain resistance of J1	10000 Ω

Table 1: Typical values of the parameters in Formula (1) to (4) and in Eq. (5) through (7).

Parameter	Value (Typ.)
Drain Current @Vgs = 0, I_{DSS}	16 mA
Gate Reverse Current, I_{gss}	-0.5 nA
Transconductance g_m@10 mA	30 mA/V
Common Source Input Capacitance, C_{iss}	15 pF

Table 2: Main DC and AC characteristics of a 2N6453.

Peaking Time [μs]	0.8	1.6	3.2	6.4
C_D = 0pF	1.1	0.9	0.7	0.5
C_D = 61pF	3.4	2.53	1.9	1.4
C_D = 196pF	8.5	6.4	4.5	3.3

Table 3: Values of resolution corresponding to the points shown in the graph of Fig.7.

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Prepared for the U.S. Department of Energy under Contract No. DE-AC03-76SF00098