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FSD HARDWARE MONITORING

Loren Shalz

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Berkeley, California

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Increased usage of the FSD by DAPR makes it more imperative that we have reliable, economical and efficient means of monitoring hardware performance. Unlike in HAZE, there is no "human guidance" against which current measuring performance is compared.

The output from the digital and track center detection logic and the maintenance of calibration (relating normal and orthogonal mode measurements) are most fittingly monitored by the control computer.

The following is a brief description of the programs which monitor these features.

DIGITAL OUTPUT CHECKING

The digital output of the FSD consists of stage positions, track center values and a full grating count. The stage positions and the most significant digits of the track centers are from a direct readout from gratings. The five least significant digits of the track centers are from interpolation counters.

A frame of film is scanned several times in both normal and orthogonal modes. A variety of tests are made to see if the data transmitted is in the proper format and if each word is within tolerable limits. After each scan, an online report informs the computer operator of the kinds and number of errors. An offline listing gives the details of the data associated with errors, an histogram of the scan line separations, the average scan line separation and histograms of the output from each of three interpolation counters to determine if they are biased.

TEST PATTERN

For the purposes of calibration and track center detector monitoring a special test pattern (Figure 1) is used. The test pattern is an array of fiducials plus a set of 7 parallel lines and 7 converging lines for each mode

of measuring. Our current test frame is on 46 mm. film with the fiducial arms and converging lines about 30μ wide. The parallel lines range from about 15μ to 105μ in width. This enables us to study the effect of track width on track center determination. The lines are about 500μ apart.

TRACK CENTER DETECTOR CHECKING

The Berkeley FSD determines track center by integrating to find center of area. This method was chosen because it is relatively insensitive to fluctuations in the shape of the input signal. Since the integration plus recovery time of an integrator is about 10μsec, we have three integrators to enable the digitizing of close tracks.

Having checked the fidelity of the digital output we check the integrators by studying repeated digitizings, with the stage stopped, of the same point on each of the parallel lines on the test frame. Only one integrator is activated at a time.

Recent hardware changes which facilitate this procedure provide the ability under program control:

1) to obtain digitizings without stage motion

2) to select any one integrator while disabling the other two

3) to set the digitizing threshold

Communication to the FSD is via the mode-speed-density word.

The digitizings associated with each line are determined from a frequency distribution of all digitizings in the vicinity of the 7 lines. For each test, the integrator used, digitizing threshold and total number of scan lines is printed online. For each line, the least and greatest track center values, the average track center value and RMS deviation, the total number of digitings and the fraction of times the line digitized follow.

CALIBRATION

The calibration program determines the coefficients in the transformations which relate normal and orthogonal modes by means of a common orthogonal coordinate system in microns. The transformations are assumed linear and consist of a shear, translation and magnification.

A set of fiducials on the test frame is located and transformed using the coefficients currently in the HAZE and DAPR programs. Then, by a least squares method corrections to the current coefficients are computed and new ones derived.

An offline listing gives the fiducial locations, current coefficients, corrections, the new coefficients and residuals. An appraisal of the acceptability of the current coefficients is printed online.

RESULTS

Experience with the diagnostic programs indicates that the hardware is reliable. Significant errors in the digital output seldom occur. The average track center values from the integrators agree to within about 1.5μ for the 30μ through 90μ lines. Two of the integrators yield comparable results on the 15μ and 105μ lines while the remaining integrator disagrees by larger amounts depending on the digitizing threshold and mode of measurement. We are able to relate normal and orthogonal measurements to within about 2.5μ with systematic differences of up to 5μ on some of the fiducials which we cannot remove at this time. Further investigation of this problem will be done.

PLANS FOR THE FUTURE

The three phases of hardware monitoring will be incorporated into a single real-time program operating under TRIST, our multiprogrammed executive program. This will allow background computations to be done should long periods of FSD monitoring be desired for maintenance. More flexibility in the kinds of output will be provided and the program will suggest likely sources of hardware malfunction and make qualitative judgments as to the acceptability of the hardware.

We will soon have available on the FSD a very slow or crawl stage speed. This will be used in conjunction with the converging lines on the test pattern to investigate digitizings from close and crossing tracks.

A feature planned at least for FSD Unit II is the ability to transmit data to and retrieve the same data from the FSD memories. This will provide a direct and effective means of memory checking using logical checksums.

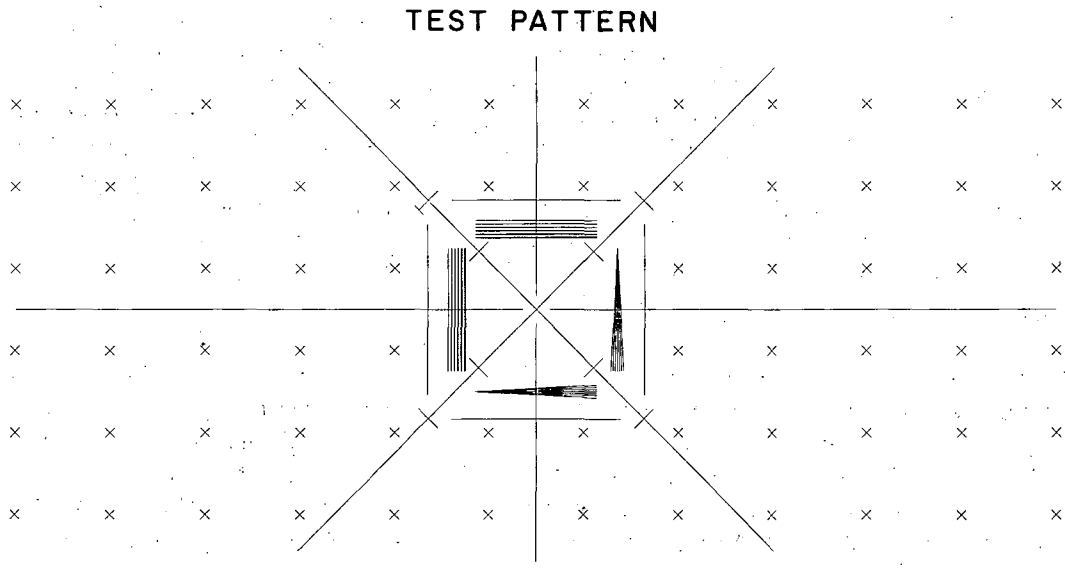

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Fig. 1.