UNIVERSITY OF CALIFORNIA, SAN DIEGO

Compact Modeling of Experimental N- and P-Channel FinFETs

A dissertation submitted in partial satisfaction of the
requirements for the degree Doctor of Philosophy
in
Electrical Engineering (Applied Physics)

by

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The dissertation of Jooyoung Song is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

Chair

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DEDICATION

To my beloved wife Jimin and our kid yet to be born.

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FIELDS OF STUDY

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ABSTRACT OF THE DISSERTATION

Compact Modeling of Experimental N- and P-Channel FinFETs

by

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Doctor of Philosophy in Electrical Engineering (Applied Physics)

University of California, San Diego, 2010

Professor Yuan Taur, Chair

As the conventional bulk CMOS shrinks towards the deep sub-100 nm regime, the advantages of scaling are seriously limited by a series of adverse effects such as random dopant fluctuation, short-channel effects, and mobility degradation primarily due to the high substrate doping level required in ultra small devices. As a solution to extend the scaling limit further, FinFETs have become an important subject of intensive VLSI research. In this dissertation, the analytic potential model for symmetric double-gate MOSFETs is verified and calibrated with experimental n- and p-channel FinFETs over a wide range of gate lengths.

Quantum mechanical effects are incorporated in the model to reproduce the measured $C_g - V_{gs}$ data of n- and p-channel FinFETs. Finite inversion layer thickness due to quantum mechanical carrier confinement at high gate overdrives becomes non-negligible for very thin oxides. The increase of effective oxide thickness degrades the gate capacitance and the drain current.

The long-channel mobility is modeled by including both a phonon scatter-

ing term and a Coulomb scattering term with opposite field dependence. They are extracted from the mobility degradations in the low and high field regions respectively.

The dependence of normalized drain current on gate length at low drain bias reveals that there is a slight mobility dependence on gate length due to different strain effects in n- and p-channel FinFETs respectively. In order to obtain the intrinsic mobility, *Shift-and-Ratio* method is applied to separate out the source-drain series resistance effects. A useful coefficient is defined and extracted to quantitatively indicate the change of mobility from its long-channel value. The coefficient indicates that the electron mobility is degraded as the gate length decreases, whereas the hole mobility is enhanced due to relaxation of the tensile strain induced by the metal gate.

The short-channel model for symmetric double-gate MOSFETs based on the analytic solution to 2-D Poisson's equation is validated in terms of the measured drain-induced barrier lowering, the threshold voltage roll-off, and the subthreshold current slope of sub-100 nm FinFETs. The difference between the extracted effective channel length and the drawn gate length is nearly the same for n- and p-channel FinFETs.

Other high-field effects including the channel length modulation and velocity saturation are also incorporated into the model to reproduce the drain current data at high drain bias.

Chapter I

Introduction

I.A CMOS scaling and Double-Gate MOSFETs

The aggressive scaling of CMOS has been the primary fuel for the semiconductor industry for past several decades. The scaling of CMOS allows obtaining higher switching speed and more densely integrated circuits in smaller devices without noticeable increase of overall power consumption. The scaling trend predicted by the famous Moore's law [1] has been continued through years of technological innovations [2], [3], and is likely to continue in the near future (Fig. Figure I.1:). The technological progress includes the halo doping [4], advanced lithography [5]-[7], strain engineering [8]-[10], and etc.

Currently, CMOS has been scaled into the deep sub-100 nm regime [11], [12], and is thought to be the dominant technology in the near future. By the year of 2011, the physical gate length is expected to be at least at or below 10 nm corresponding to the 22-nm technology node [13] as presented in Fig. Figure I.2:. However, the advantages of further CMOS scaling seems to be fundamentally limited by several non-ideal effects which are not negligible in nano-scale devices [14]-[16]. They are primarily identified to be 1) the severe short-channel effects

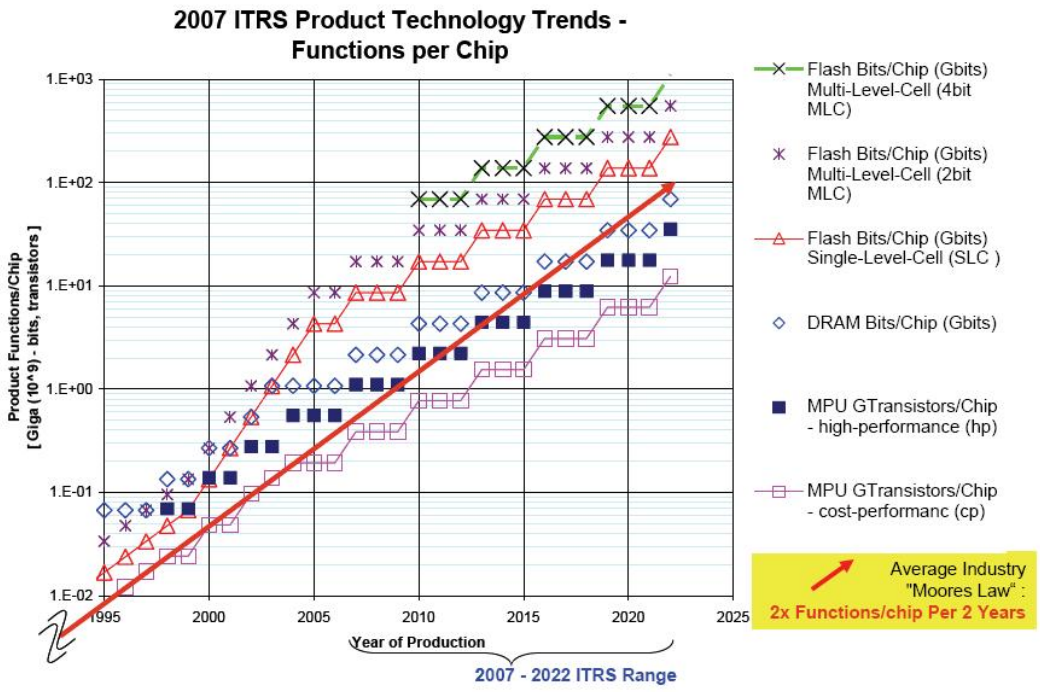

Figure I.1: 2007 ITRS product technology trends: product functions/chip and industry average "Moore's Law" trends (Adopted from [2]).

including threshold voltage roll-off, drain-induced barrier lowering (DIBL), and subthreshold slope degradation, 2) quantum mechanical effects leading to significant gate-tunneling leakage current, threshold voltage shift and gate capacitance degradation, 3) random dopant fluctuation resulting threshold voltage variation, and 4) non-negligible parasitic components.These effects lead to unacceptably high leakage current and degraded switching speed, therefore become limiting factors of further CMOS scaling at present [17].

As a solution to overcome these adverse effects, various types of multiple-gate (MG) structures have been proposed and investigated [18], including double-gate, quadruple-gate, surrounding-gate [19], tri-gate [20], Π-gate [21], Ω-gate [22] MOSFETs and FinFETs [23]. Numerical simulation and analytical analysis have shown that these MG structures give the less short-channel effects or drain leakage current than the conventional planar devices with the same gate-length, hence

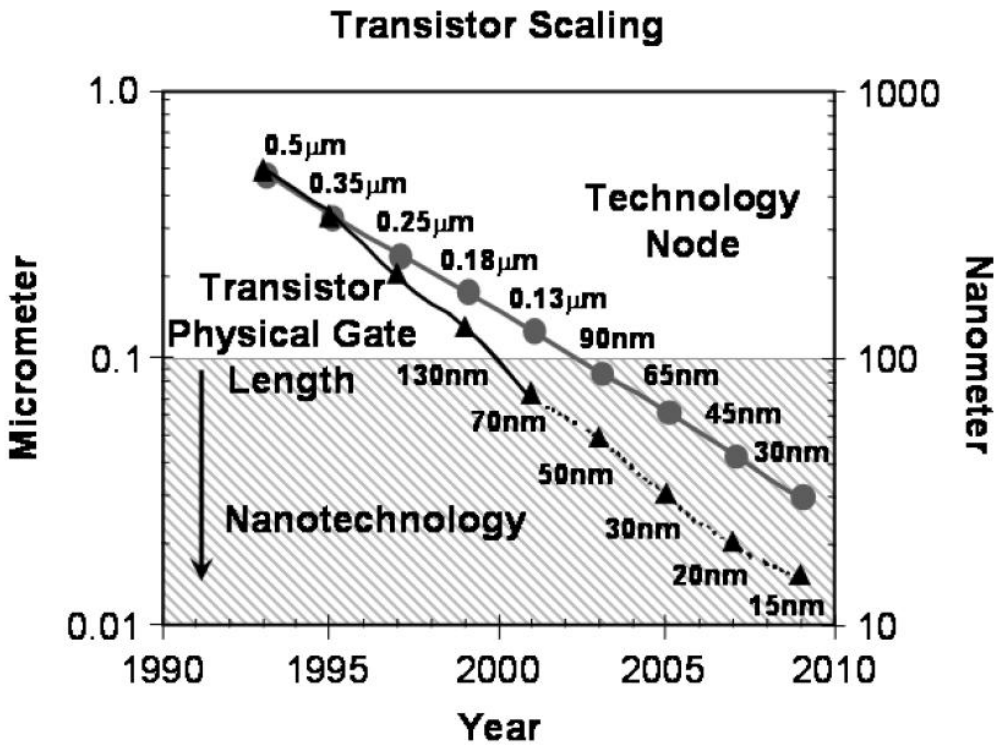

Figure I.2: Scaling of transistor size (physical gate length) with technology node to sustain "Moore's Law" (Adopted from [13]).

the better scalability [24]. Among these novel structures, double-gate (DG) MOSFETs have been intensively studied due to the immediate compatibility with the conventional planar technology.

Fig. Figure I.3: illustrates a typical DG MOSFET structure. In general, DG MOSFETs can be fabricated in two different types depending on the work functions of their gates: symmetric DG MOSFETs have an identical work function for both gates ($\phi_1 = \phi_2$), whereas asymmetric DG MOSFETs have two different work functions for the gates ($\phi_1 \neq \phi_2$). Both types of DG MOSFETs have two different operation modes, i.e., 3-terminal-driven mode and 4-terminal-driven mode. The gate voltages of 3-terminal-driven mode are tied together ($V_{g1} = V_{g2}$), while those of the 4-terminal-driven mode change independently ($V_{g1} \neq V_{g2}$). The 3-terminal-driven mode gives ideal subthreshold current slope; devices with variable threshold

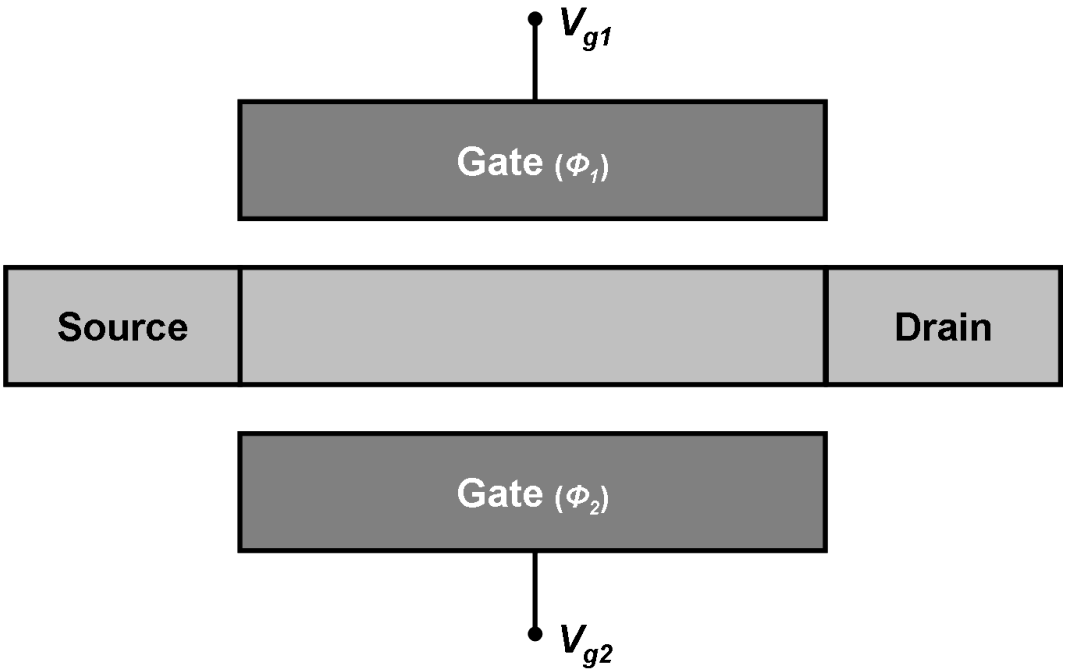

Figure I.3: A cross-section along the channel direction of a general DG MOSFET.

voltage to control the leakage current and driving current can be characterized by the 4-terminal-driven mode. To take full advantage of the DG structure, the body of DG MOSFETs is typically undoped or lightly doped.

I.B Advantages of Double-Gate MOSFETs

The novel structure of DG MOSFETs, namely, two tightly coupling gates and an undoped, thin silicon film, allows DG MOSFETs to have superior performance over the conventional bulk MOSFETs. The primary advantages of DG MOSFETs are the suppression of the short-channel effects, elimination of random dopant fluctuation, and enhancement of the carrier transport. The physical explanations of these benefits are discussed in this subsection.

To scale further down the CMOS, three major technologies exist: 1) the conventional planar bulk MOSFETs (Fig. Figure I.4:), 2) fully-depleted (FD)

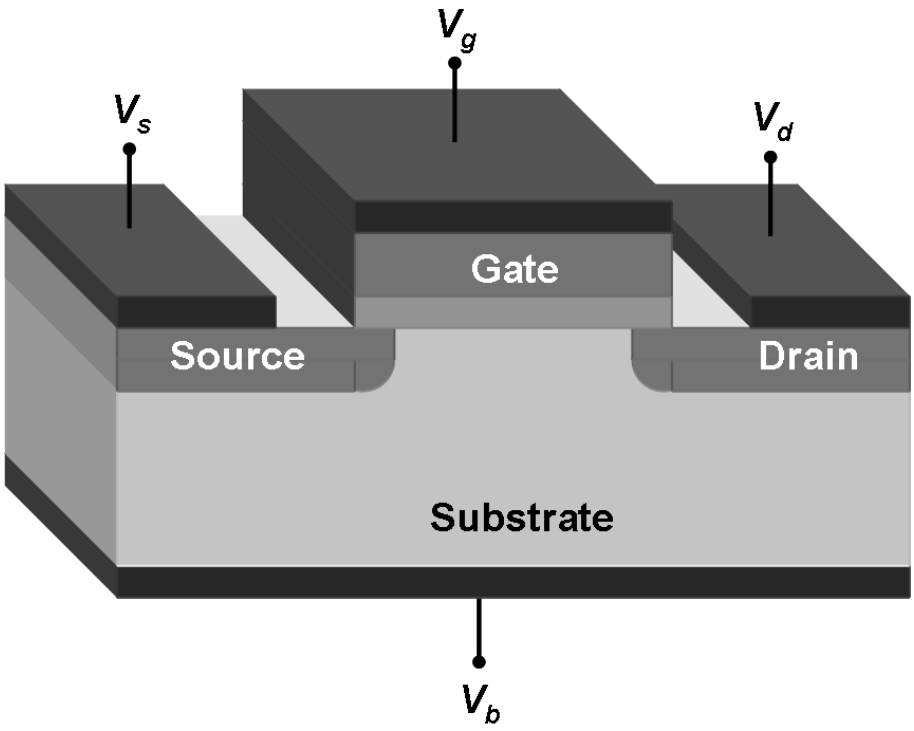

Figure I.4: 3-D schematic diagram of a conventional bulk MOSFET.

silicon-on-insulator (SOI) MOSFETs (Fig. Figure I.5:), and 3) DG MOSFETs (Fig. Figure I.6:). Because the main obstacle for further CMOS scaling is the excessive short-channel effects in very small devices, scaling theories of these approaches are developed to predict and control the short-channel effects in terms of characteristic length or scale length of MOSFETs, which is a measure of scalability. The scaling theory of the conventional CMOS was developed by solving 2-D Poisson's equation in the subthreshold region where the mobile charge density is negligible. The expression for the minimum channel length with tolerable short-channel effects is given by

$$L_{min} = 2\left(W_d + \frac{\epsilon_{si}}{\epsilon_{ox} t_{ox}}\right) \tag{I.1}$$

where ϵ_{si} and ϵ_{ox} are the dielectric constants of the silicon and the silicon dioxide; W_d is the depletion width; t_{ox} is the oxide thickness.

In addition, a small body coefficient is essential to prevent the degradation

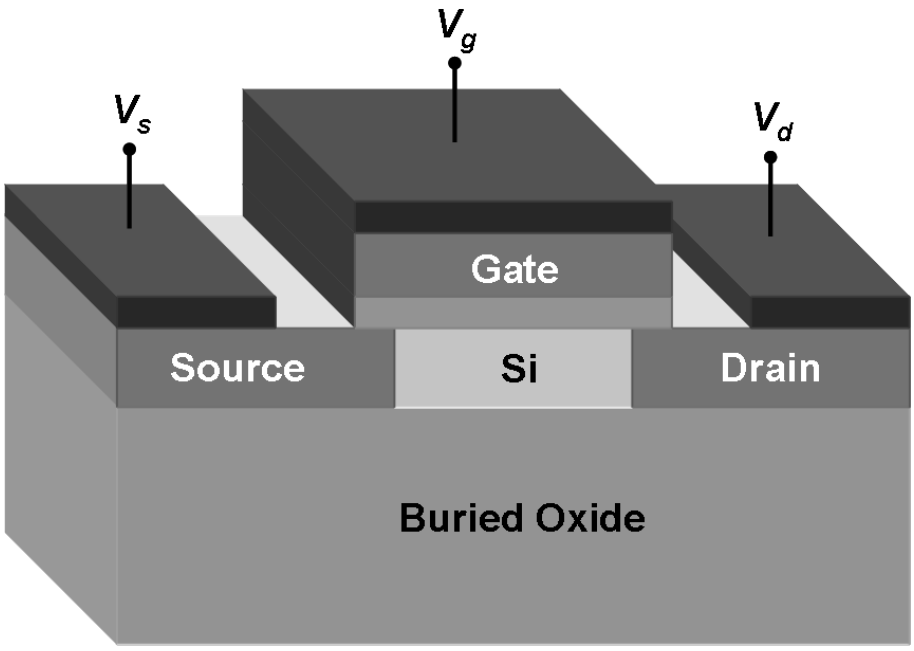

Figure I.5: 3-D schematic diagram of a fully-depleted silicon-on-insulator MOSFET.

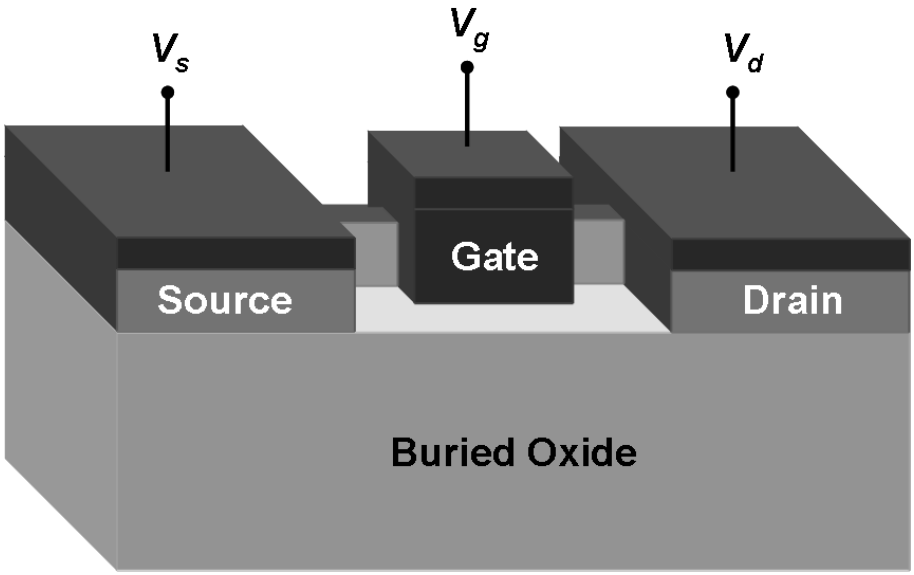

Figure I.6: 3-D schematic diagram of a double-gate FinFET.

of the subthreshold current slope. The body coefficient of the conventional bulk

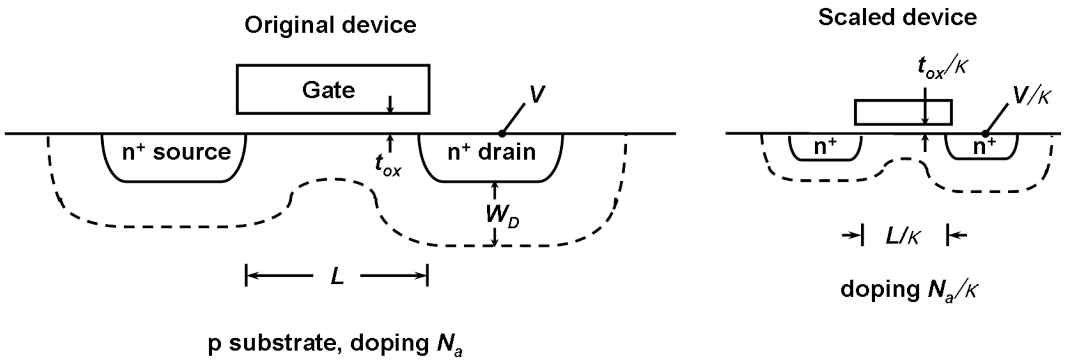

Figure I.7: Principles of MOSFET constant-electric-field scaling (Adopted from [25]).

MOSFETs are expressed as

$$m = 1 + \frac{\sqrt{\epsilon_{si} q N_a / 4\psi_B}}{C_{ox}} = 1 + \frac{C_{dm}}{C_{ox}} = 1 + \frac{3t_{ox}}{W_{dm}} \tag{I.2}$$

where N_a is the substrate doping level, ψ_B the surface potential, C_{ox} the gate capacitance defined by ϵ_{ox}/t_{ox}, and W_{dm} the maximum depletion width. Large body coefficient results in slow subthreshold current slope hence poor on/off current ratio.

Therefore the depletion width and oxide thickness must be scaled down proportionally. As a guide for CMOS scaling, Dennard proposed a constant-field scaling theory as presented in Fig. Figure I.7: [25]. Shrinking the depletion width requires higher substrate doping level, κN_a, which gives rise to a series of undesirable effects. Random dopant fluctuation effects are aggravated to result in large threshold voltage deviation. The introduced impurities degrade carrier mobility. Finally, the increased junction capacitances of source and drain lead to slow switching speed.

In order to eliminate the numerous problems caused by scaling the depletion width, FD SOI MOSFETs were introduced. FD SOI MOSFETs have a thick buried oxide (BOX) layer under the silicon body. The depletion width is decided by the silicon film thickness only, thus no highly doped substrate is necessary. In

addition, the source and the drain capacitances are much smaller than those of the conventional bulk MOSFETs, because the BOX with low dielectric constant separates the source and drain from the substrate. However, a large drain field penetration occurs through the BOX, thus the gate controllability over the channel is greatly degraded. Therefore the short-channel effects of FD SOI MOSFETs are more severe than those of the conventional bulk CMOS. The minimum channel length of FD SOI MOSFETs are given by

$$L_{min} = 4.5\left(t_{si} + \frac{\epsilon_{si}}{\epsilon_{ox} t_{ox}}\right) \tag{I.3}$$

By comparing Eq. (I.1) and Eq. (I.3), one can easily find that the short-channel effects of FD SOI MOSFETs are worse than those of conventional bulk MOSFETs when the silicon thickness and the depletion width are the same.

In case of DG MOSFETs, the tightly coupling gate structure greatly suppresses the field penetration into the BOX hence the better scalability. Furthermore, the ideal subthreshold slope is realized in DG MOSFETs, because the potential in whole silicon body varies at the same time until inversion layer is formed and screens the gate bias. The ideal current slope allows the device to turn off quickly, so that less leakage current or standing power consumption is obtained with the same driving current. On the other hand, it can also be used to allow the device to have lower threshold voltage and thereby achieve the larger drive current or faster switching speed with the same standing power. Because DG MOSFETs, like FD SOI MOSFETs, have small source and the drain capacitances, fast switching speed is expected.

The undoped or lightly doped body of DG MOSFETs is free from the random dopant fluctuation effects, thereby yields better controlled threshold voltage deviation. It also reduces the field crowding or an increase of the local electric field to decrease the occurrences of impact ionization, band-to-band tunneling, and trap-assisted-tunneling. This immunity of DG MOSFETs to high field effects yields less leakage currents hence better on/off-current ratio.

The degradation mechanisms of mobility are greatly suppressed in DG MOSFETs. It is well-known that the mobility is a strong function of the effective field both in low and high field regimes due to the phonon and Coulomb scattering, respectively [26]. Owing to the tightly coupling gates and the negligible depletion charges, the effective field of DG MOSFETs is far smaller than that of the conventional bulk MOSFETs. The effective field of the conventional bulk MOSFETs are given by Gauss's law,

$$E_{eff} = \frac{1}{\epsilon_{si}} \left(|Q_i| + |\eta Q_d| \right). \tag{I.4}$$

where Q_i and Q_d are the inversion and the depletion charges, respectively; η is an empirical parameter to give a universal curve of mobility. In DG MOSFETs, the depletion charge term is negligible, therefore less phonon scattering is experienced by the carriers in the high field regime. In low field regime, the undoped body of DG MOSFETs ideally does not have impurity scattering centers.

I.C Structures of Double-Gate MOSFETs

DG MOSFETs can be fabricated one of three orientations in Fig. Figure I.8: [27]. Type I has the same orientation as the conventional planar MOSFETs except the substrate is substituted by the bottom gate [28]. The thickness of the silicon film can be controlled with high accuracy by thin film deposition. However, the self-alignment of the bottom gate is difficult with planar process. The additional design margin to avoid gate underlaps introduces large parasitic capacitances and resistors, thus degrades device performance [29]. In addition, an additional gate extension to metal contact is necessary to to access the bottom gate [30]. The source and the drain of type II are fabricated vertically with two gates on the sidewall [31]. Again, it is not straightforward to fabricate the source and the gate vertically with conventional planar process. Type III with lateral channel direction in a vertical thin silicon film is the most promising among the proposed double-

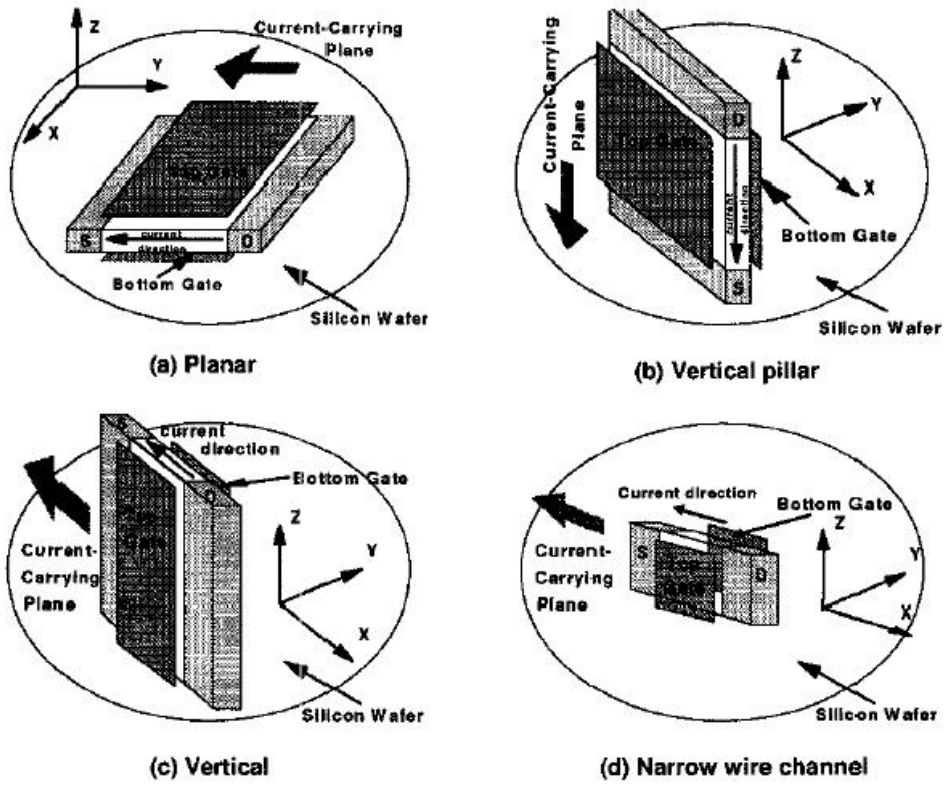

Figure I.8: Possible orientations of a DG MOSFETs on a silicon wafer. (a) Planar, (b) Vertical pillar, (c) Vertical DELTA device, (d) Narrow wire channel. (d) is a special case of (a) or (c) where the channel width dimension of (c) is reduced to a value comparable to the channel thickness (Adopted from [29]).

gate structures [32]. It is easy to self-align the gates with the conventional planar technology; two vertical gates are highly accessible; the height of the silicon film can be fabricated with high uniformity. Depending on the topology of the devices, two major variations have been proposed and studied. If the height of the silicon film is much greater than the width ($H \gg t_{si}$) as in the double-gate FinFET structure in Fig. Figure I.9: (b) , the channel is primarily governed by the sidewalls. In this case, the DG FinFET can be approximated to an ideal DG MOSFET (Fig. Figure I.9: (a)). Tri-gate (TG) MOSFETs, on the other hand, have top gate wide enough to control inversion charges (Fig. Figure I.9: (c)). Because the top gate

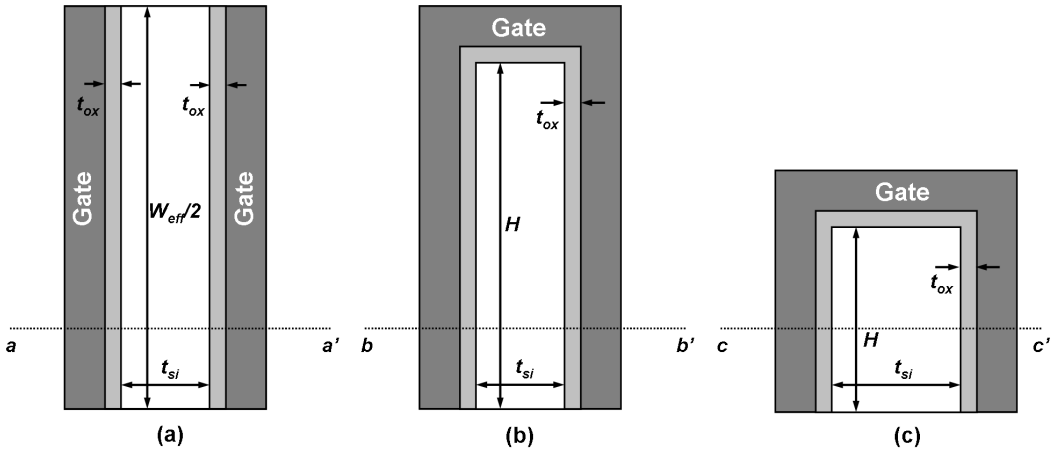

Figure I.9: 2-D cross-sections of (a) an ideal DG MOSFET, (b) a DG FinFET, and (c) a TG MOSFET. 1-D cross-sections of the structures, $a - a'$, $b - b'$, and $c - c'$, are identical.

also plays a role in inducing inversion charge, the short-channel effects are usually better-controlled in TG structures.

Unlike planar devices, DG FinFETs and TG MOSFETs can have surface orientations other than (100)-surface due to their 3-D structure (see Fig. Figure I.10:). The inversion layer of planar devices is formed on the surface of which orientation, usually (110) surface, is determined in wafer level. On the contrary, the inversion layer of FinFETs and TG MOSFETs is formed on the sidewalls. A range of surface between (100)- and (110)-surfaces are available depending on the channel orientation. Because the mobilities of electron and hole are strongly dependent on the surface and the channel orientation, double-gate MOSFETs have additional design freedom for carrier mobility ratio. $\langle 110 \rangle$ channel orientation with (110) surface is commonly employed in modern FinFETs and TG MOSFETs to take advantage of high hole mobility. The enhanced hole mobility is beneficial for device switching, because the hole mobility is much lower in the conventional CMOS thus limits the overall device performance.

Most of the recent progress of the planar technology is readily applicable

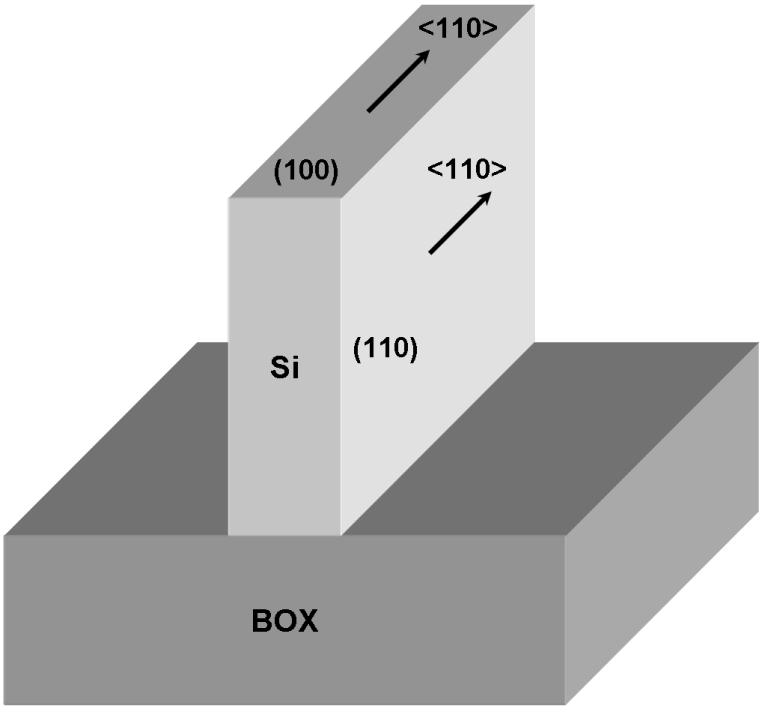

Figure I.10: 3-D schematics of a DG FinFET with (100)-top-surface and (110)-sidewall-surface. Only the buried oxide and silicon body are presented for simplicity.

into the double-gate fabrication. Strain engineering has been migrated to enhance carrier mobilities or driving currents; high-κ materials as gate dielectric are also in the area of active research, resulting greatly suppressed gate leakage currents and high drain current driving ability [33], [34]; halo doping to suppress the short-channel effects is successfully employed as well [4]. In addition, metal gates with appropriate work-functions have been intensively studied to obtain desirable threshold voltage.

I.D Research Status of Compact Modeling of Double-Gate MOSFETs

The usages of the novel devices are seriously limited without physics-based, seamless, accurate and efficient compact model for circuit simulators, even if devices for mass production can be fabricated. A series of attempts have been made to implement compact models giving insight to understand the physics and operation of DG MOSFETs. A core model for symmetric and asymmetric DG MOSFETs was developed by Taur based on the solution of 1-D Poisson and current continuity equations without invoking the charge-sheet approximation [35], [36].

Because the rigorous derivation requires an intermediate parameter to express the body potential, inversion charge, and drain current, a number of attempts have been made to approximate the expressions [37], [38]. Each approximation describes the electric characteristics of DG MOSFETs as functions of charges. The new equations to obtain the charges are, however, still implicit, thus there is no mathematical advantage to remove the intermediate parameter. Furthermore, each approximation introduces non-negligible error either in the transition region or on-current regions.

The short-channel effects were added to the core model by solving 2-D Poisson's equation. The equation can be solved either by evanescent mode which is largely adopted by the bulk MOSFETs [39], [40], or assuming parabolic potential shape [41], [42]. The solution by the parabolic potential assumption is not accurate at the silicon-silicon dioxide interface. Employing the current continuity equation and focusing on the minimum potential barrier along the channel, explicit expressions for threshold voltage roll-off and subthreshold current slope were also developed [40].

Quantum mechanical effects of DG MOSFETs were developed by counting the electron density of states in the double-gate MOSFETs [43]. By solving 1-

D Poisson and the Schrödinger's equation rigorously, explicit expressions for the threshold voltage shift and the finite inversion layer thickness were developed [44].

An analytic potential-based terminal charge and capacitance model then was implemented for AC and transient simulations [45]. Employing different forms of drain current expression results in similar expressions for the terminal charges and capacitances [46].

The effects of body doping was first studied numerically [47]. The threshold voltage shift and the subthreshold current slope degradation are discussed intensively. An analytical solution to the 1-D Poisson's equation with the doping term is followed [48]. Because it is impossible to solve 3 coupling implicit equations analytically, a series of appropriate assumptions were involved to solve the equation in a non-coupling way.

The non-ideal device geometries of DG FinFETs or TG MOSFETs have been also incorporated in the model by adding top transistor effects by applying equivalent geometry [49], or by approximating into other MG MOSFET structures [50].

Explicit solution of the core model was then developed by employing a W-Lambert function without numerical iteration [51]. An explicit solution by high-order corrections of appropriate initial guess was followed [52].

The analytic potential model, in turn, has been validated by numerical simulations and several published data [53], [54]. However, a comprehensive compact modeling of both n- and p-channel devices covering a wide range of device geometry is still necessary to fully demonstrate the technology predictability of the physics-based analytic potential model for DG MOSFETs.

I.E Outline of the Dissertation

The concept of DG MOSFETs including the advantage, operation and structure of DG MOSFETs is briefly introduced in this chapter. The research status of compact modeling of DG MOSFETs is summarized along with the objective of this dissertation. The rest of the dissertation is organized as follows.

The analytic potential model for SDG MOSFETs is described in Chapter Chapter II. First, analytic potential and drain current model is developed in terms of an intermediate parameter β based on the solution of 1-D Poisson's equation. The capacitance model is also given with an accurate gate capacitance expression. Quantum mechanical correction are added to the core model by solving coupling 1-D Poisson and Schrödinger equations. Short-channel effects based on the solution of 2-D Poisson's equation are then incorporated with the model in terms of the DIBL, the threshold voltage roll-off, and the subthreshold current slope. Finally, High-field effects including the channel length modulation and the velocity saturation for DG MOSFETs are also introduced in detail.

Chapter Chapter III describes the experimental FinFET hardware and the measurements. Physical dimension of the FinFETs is given in detail in comparison with an ideal DG MOSFET structure. The fabrication process for the FinFETs are described to provide a physical insight to the compact modeling.

Chapter Chapter IV covers systematic calibration of n-channel FinFET hardware, whereas Chapter Chapter V is for p-channel FinFET hardware.

First, geometric parameters are extracted from the calibration of long-channel $C_g - V_{gs}$ data with the core model incorporated with quantum mechanical effects.

Long-channel mobilities are modeled by a modified universal mobility with a phonon and a Coulomb scattering term. The mobility model is then calibrated to long-channel $I_{ds} - V_{gs}$ data at low drain bias.

Gate length dependence of mobilities are investigated after the separation of source-drain resistance effects from medium-length $I_{ds} - V_{gs}$ data. A useful coefficient to indicate increase or decrease of the intrinsic mobilities from its long-channel values is defined and extracted. The physical reason behind the change of mobility is discussed for both n-channel and p-channel FinFETs. With the gate-length-dependent strain effects, the medium-channel $I_{ds} - V_{gs}$ data is modeled.

High-field effects including the channel length modulation and the velocity saturation are added to reproduce the medium-channel $I_{ds} - V_{gs}$ with high drain bias and the $I_{ds} - V_{ds}$ data for all bias regimes.

Finally, short-channel effects are validated in terms of DIBL, threshold voltage roll-off, and subthreshold current slope degradation of sub-100 nm $I_{ds} - V_{gs}$ and $I_{ds} - V_{ds}$ data with the inclusion of high field effects. The similarity and difference between n- and p-channel FinFETs are clearly discussed in terms of mobilities, strain effects, and high-field behaviors.

Chapter VI concludes the paper and discusses the future research direction of compact modeling of DG MOSFETs further than the scope of this dissertation.

Chapter II

Compact Model for Double-Gate MOSFETs

For bulk CMOS, since Pao-Sah's double integral of drain current based on graduate-channel approximation (GCA) was proposed [55], virtually all existing compact models have been developed starting from it. The double integral has both drift and diffusion terms, thus is valid in all operation regions. However, a closed-formed drain current solution cannot be obtained due to the presence of both depletion and mobile charges in the integral.

Among the attempts to simplify Pao-Sah's expression, charge-sheet approximation by J. R. Brews is most important [56]. The charge-sheet approximation assumes that the depletion charges do not change after inversion layer is formed. Simply speaking, inversion charges distribution takes form of a delta function peaking at the silicon surface. By assuming an infinitely thin layer of inversion charges, closed-formed drain current expression suitable for very-large-scale circuit simulations can be developed. Moreover, the charge-sheet approximation allows the inversion charge density to be described as a function of surface potential only. Practically all commercial compact models for the bulk CMOS including BSIM3, BSIM4, and PSP models are based on the charge-sheet approximation.

On the contrary, compact modeling of DG MOSFETs does not require the charge-sheet approximation. Because the undoped or lightly doped body of DG MOSFETs, the depletion charge is negligible in all region. Therefore, only the mobile charge term appears in Pao-Sah's double integral for DG MOSFETs, yielding a closed-formed drain current expression [36]. Furthermore, the charge-sheet approximation is irrelevant for DG MOSFETs, because not only the surface potential, but also the potential at all points of the channel must be known to describe volume inversion effects [35].

In this chapter, a compact model for DG MOSFETs, without invoking the charge-sheet approximation, is introduced. First, analytic potential potential, charge, and drain current for long-channel DG MOSFETs is derived from 1-D Poisson's equation. Quantum mechanical effects is added to the model by solving 1-D Poisson and Schödinger equations for very thin body and oxide. Short-channel effects are incorporated with the model from the analytic solution of 2-D Poisson's equation in subthreshold region. Finally, the channel length modulation and the velocity saturation effects are added to the core model.

II.A Analytic Potential Model for Double-Gate MOSFETs

For an undoped or lightly doped silicon film as shown in Fig. Figure II.1:, the potential at any points in the device is governed by Poisson's equation with the mobile charge term only [35],

$$\frac{d^2\psi}{dx^2} = \frac{q}{\epsilon_{si}} n_i e^{q(\psi - V)/kT}. \tag{II.1}$$

where V is the quasi-Fermi potential which varies laterally from the source to the drain, and is independent of x. It should be clear that Eq. (II.1) is not valid in accumulation region, where the hole density is non-negligible. In fact, to induce

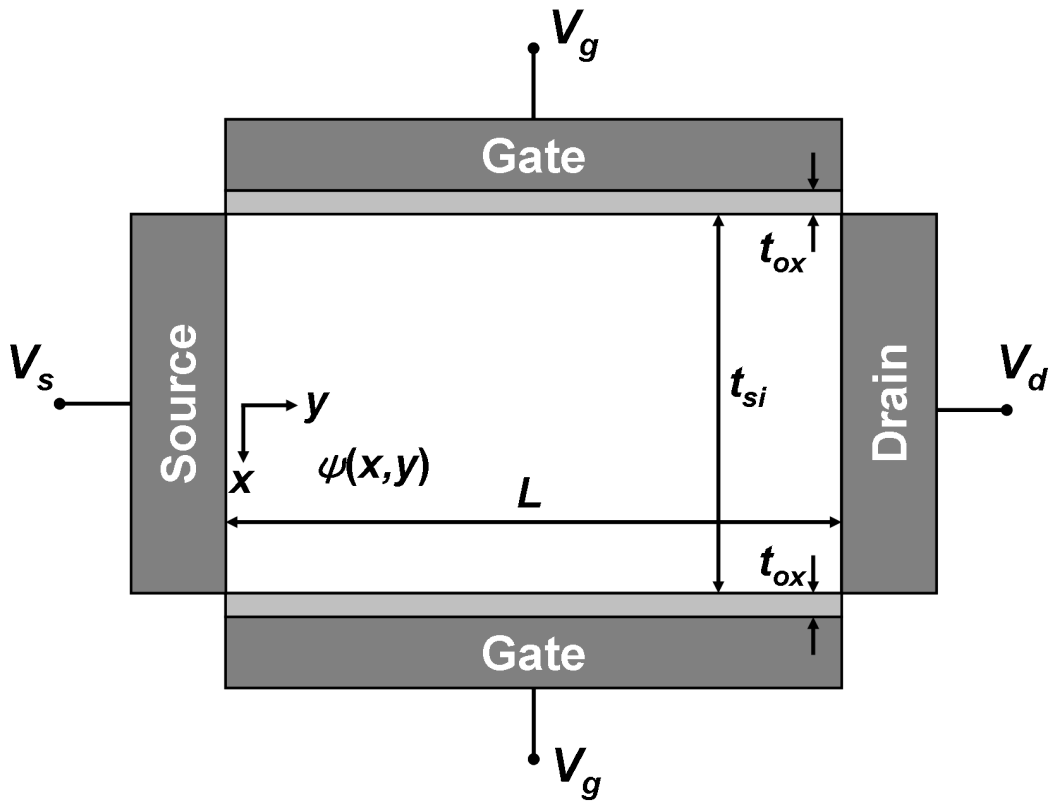

Figure II.1: 2-D schematic diagram of a double-gate MOSFET along the channel direction.

accumulation charge in DG MOSFETs is not easy, because the potential of the body floats. Furthermore, there is no reservoir for holes due to the lack of body contact; generation of electron-hole pair is the only obvious source for holes.

By integrating Eq. (II.1) twice, the potential is given by

$$\psi(x) = V + \frac{2kT}{q}\ln\left(\frac{2\beta L_{Di}}{t_{si}}\right) - \frac{2kT}{q}\ln\left[\cos\left(\frac{2\beta x}{t_{si}}\right)\right] \tag{II.2}$$

where $L_{Di} \equiv \sqrt{2\epsilon kT/q^2 n_i}$ is the intrinsic Debye length, and β is an intermediary parameter obtained by the boundary condition,

$$\frac{q(V_g - \Delta\phi - V)}{2kT} - \ln\left(\frac{2L_{Di}}{t_{si}}\right) = \ln(\beta) - \ln[\cos(\beta)] + 2r\beta\tan(\beta). \tag{II.3}$$

Here a structural parameter for DG MOSFETs is defined as $r \equiv \epsilon_{si}t_{ox}/\epsilon_{ox}t_{si}$. It should be noted that the intermediary parameter β is only dependent on the

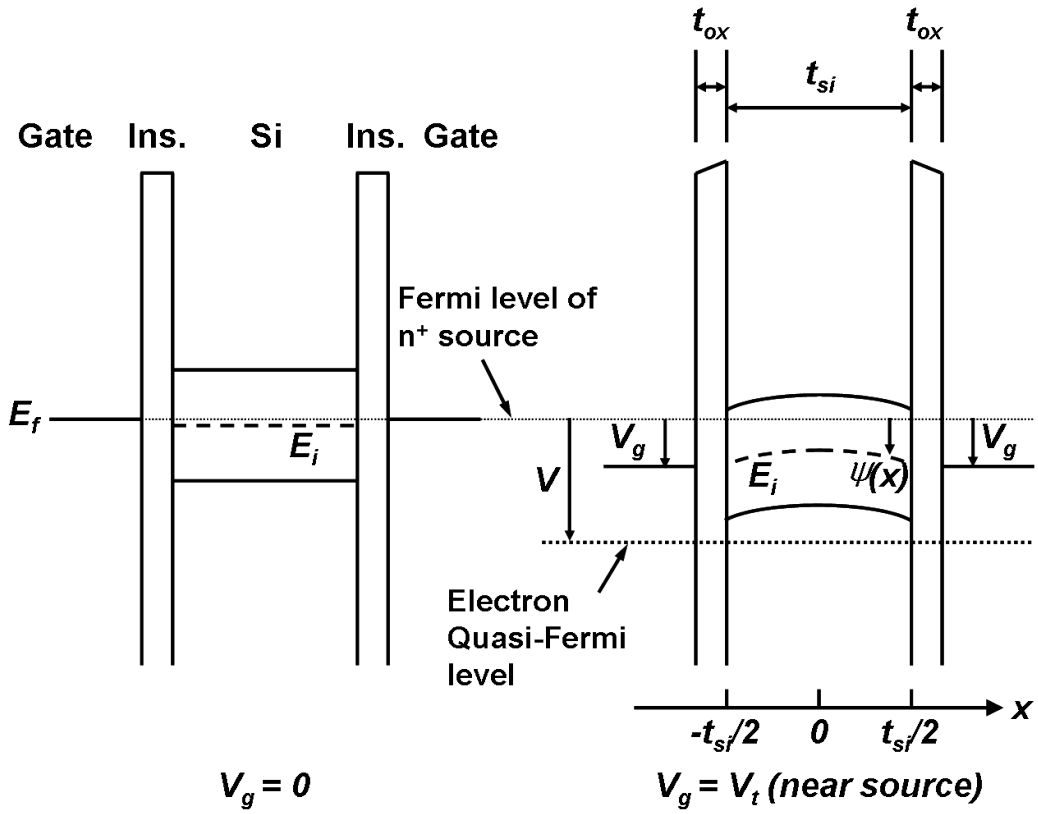

Figure II.2: 1-D schematic diagram of the potential of a DG MOSFET in subthreshold and on-current region.

structural parameter and the external voltages.

Because the potential of the silicon body is flat in the subthreshold region as presented in Fig. Figure II.2:, the mobile charges are induced throughout the whole silicon film. Therefore, volume inversion, which is responsible for an ideal subthreshold current slope, is observed. After the band-bending at the threshold voltage, mobile charges are induced only at the silicon interface, thereby no more volume inversion is achieved.

For not too heavily doped devices, the first-order effect of the depletion charge can be incorporated in the model by simply shifting the gate voltage V_{gs} by $qN_aW/2C_{ox}$. For very heavily doped devices, additional doping term must be included in the 1-D Poisson's equation. The equation cannot be integrated twice to

yield an analytic body potential. Also the boundary condition becomes extremely complicated and imposes heavy calculation load. In usual, heavily doped DG MOSFETs lose many of beneficial properties that undoped DG MOSFETs, and therefore the use of heavily doped devices are limited [57].

The inversion charge density is derived by Gauss's law,

$$Q_i(\beta) = 8\epsilon_{si}\frac{W}{t_{si}}\frac{kT}{q}\beta\tan(\beta) \tag{II.4}$$

By integrating the current continuity equation, the drain current is given [36] by,

$$I_{ds} = \mu_{eff}\frac{W}{L}\frac{8\epsilon_{si}}{t_si}\left(\frac{kT}{q}\right)^2[p(\beta_d) - p(\beta_s)] \tag{II.5}$$

where $p(\beta)$ is defined for convenience as

$$p(\beta) \equiv -2\beta\tan(\beta) + \beta^2 - 2r\beta^2\tan^2(\beta). \tag{II.6}$$

It should be noted that Eq. (II.5) is valid for all operation regions seamlessly. Once the bias condition and the geometry is given, the drain current can be calculated by the single equation.

To calibrate $C_g - V_{gs}$ data, the gate charge and the gate capacitance model is necessary. The gate charge can be obtained easily by integrating the inversion charge density from the source to the drain [45].

$$Q_g = \int_0^L Q_i(y)dy \; = \frac{\mu_{eff}}{I_{ds}}\int_{V_s}^{V_d} Q_i^2(V)dV = \frac{\mu_{eff}}{I_{ds}}\int_{\beta_s}^{\beta_d} Q_i^2(\beta)\frac{d\beta}{dV}dV \tag{II.7}$$

By substituting the previously developed expressions of $Q_i(\beta)$ and $d\beta/dV$ into Eq. (II.7), the gate charge, Q_g is given by

$$Q_g = -\frac{\mu_{eff}W^2}{I_{ds}}\frac{2kT}{q}\left(\frac{8kT\epsilon_{si}}{qt_{si}}\right)^2 \int_{\beta_s}^{\beta_d}\tan^2(\beta)\left\{\frac{1}{\beta} + \tan(\beta) + 2r\left[\beta\sec^2(\beta) + \tan(\beta)\right]\right\}. \tag{II.8}$$

Because Eq. (II.8), the rigorous derivation of Q_g, cannot be fully formulated into a closed-form expression, additional approximations are made to obtain a continuous, analytical gate charge expression. To simplify the procedure, a normalized

inversion charge density is introduced, namely,

$$q_i \equiv \beta \tan(\beta) = \frac{Q_i}{8\epsilon_{si} kT/qt_{si}}. \tag{II.9}$$

The boundary condition for the intermediary parameter β, Eq. (II.3), can be reformulated as

$$\frac{q(V_g - \Delta\phi - V)}{2kT} - \ln\left(\frac{2L_{Di}}{t_{si}}\right) \approx \ln(q_i) + 2r(q_i). \tag{II.10}$$

Eq. (II.10) does not have the second term of Eq. (II.3), β^2, which cannot be expressed as a function of the inversion charge density, thereby yields an explicitly integrable gate charge expression. Yet the solution of the modified boundary condition has the same asymptotic behavior as that of Eq. (II.3). With the modified boundary condition, the drain current expression is approximated to

$$I_{ds} \approx \mu_{eff} \frac{W}{L} \frac{4\epsilon_{si}}{t_{si}} \left(\frac{2kT}{q}\right)^2 \left| \left(\frac{q_i}{2} + r q_m^2\right) \right|_{q_{id}}^{q_{is}}. \tag{II.11}$$

II.11 can also be derived by invoking the charge-sheet approximation, namely,

$$I_{ds} \approx \mu_{eff} W \left(Q_i \frac{d\psi_s}{dy} - \frac{kT}{q} \frac{dQ_i}{dy}\right). \tag{II.12}$$

The surface potential ψ_s is approximated to the quasi-Fermi level V in Eq. (II.12).

The approximated expression of Q_g can be obtained by substituting the inversion charge expression as a function of β, dV, and I_{ds}, from Eq. (II.10) and Eq. (II.11) into Eq. (II.8).

$$Q_g = 8WL \frac{kT}{q} \frac{\epsilon_{si}}{t_{si}} \frac{(1/4)(q_{is} + q_{id}) + (2r/3)(q_{is}^2 + q_{is}q_{id} + q_{id}^2)}{1/2 + r(q_{is} + q_{id})} \tag{II.13}$$

where $q_{is} \equiv \beta_s \tan(\beta_s)$ and $q_{id} \equiv \beta_d \tan(\beta_d)$ are the normalized inversion charge densities at the source and the drain, respectively.

It should be noted that Eq. (II.13) diverges when V_{ds} approaches zero. To avoid the numerical singularity, the expression for Q_g must be changed to its asymptotic value for small V_{ds}.

$$Q_g = 8WL \frac{kT}{q} \frac{\epsilon_{si}}{t_{si}} \beta_s \tan(\beta_s) \tag{II.14}$$

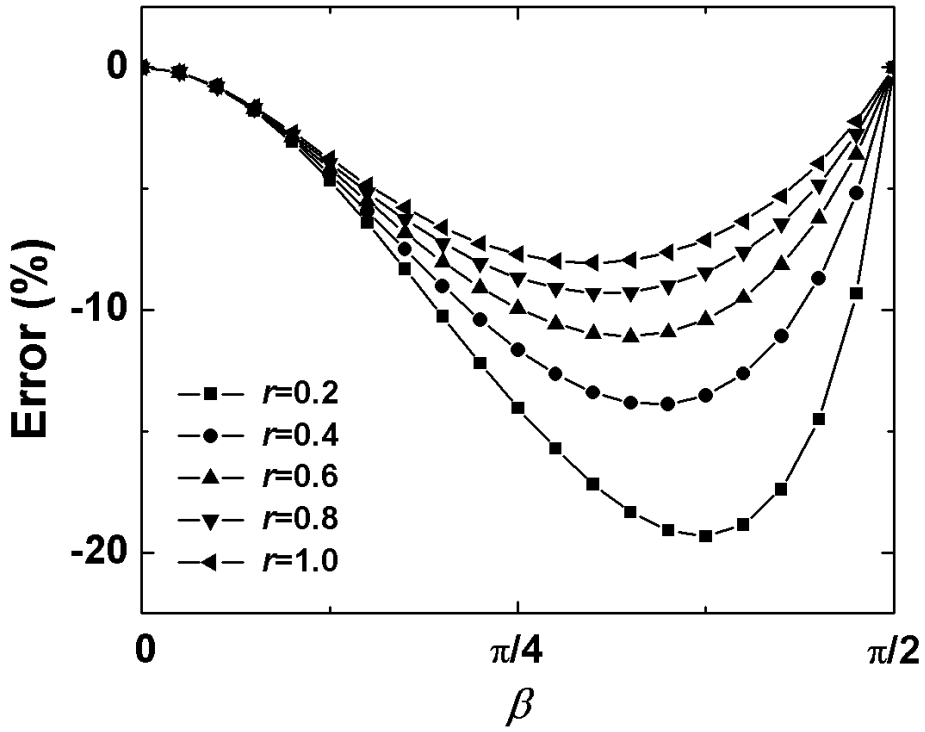

Figure II.3: Error between $p(\beta)$ and $p^{CSA}(\beta)$ versus β. β is an intermediate parameter obtained by Eq. (II.3).

Although the gate capacitance derived by Eq. (II.13) is very tedious and complicated, the asymptotic gate charge expression of Eq. (II.14) yields the total gate capacitance with $V_{ds} = 0$ in a straightforward way.

$$C_g = 4WL\frac{\epsilon_{si}}{t_{si}}\frac{\tan(\beta_s) + \beta_s \sec^2(\beta_s)}{1/\beta_s + \tan(\beta_s) + 2r\tan(\beta_s) + \beta_s \sec^2(\beta_s)} \tag{II.15}$$

It is worth noting that the gate capacitance is a function of only β_s, which in turn is decided by the structural parameter r and the gate bias V_{gs} only.

The unique feature of volume inversion cannot be captured properly by surface potential based models with the charge-sheet approximation. In usual, surface potential based models takes advantages of the charge-sheet approximation

model which is commonly employed in the bulk MOSFETS, namely,

$$I_{ds}^{CSA} = -\mu_{eff} W \left(Q_i \frac{d\psi_s}{dy} - \frac{kT}{q} \frac{dQ_i}{dy} \right), \tag{II.16}$$

where Q_i is the mobile sheet charge density [38], [48]. This led to the final expression,

$$I_{ds}^{CSA} = \left| -\mu_{eff} \frac{1}{C_{ox}} \frac{W}{L} \left[Q_i^2 + C_{ox} \left(\frac{2kT}{q} Q_i \right) \right] \right|_{Q_s}^{Q_d}. \tag{II.17}$$

It should be noted that the drift and diffusion current density,

$$J_y = -qn\mu_{eff} \left(\frac{d\psi}{dy} - \frac{kT}{qn} \frac{dn}{dy} \right) = -qn\mu_{eff} \frac{dV}{dy}, \tag{II.18}$$

where n is the electron volume density, is often integrated to yield

$$I_{ds} = \mu_{eff} W Q \frac{dV}{dy} \tag{II.19}$$

under the gradual channel approximation since the quasi-Fermi potential V and thus dV/dy are independent of x in the depth direction. Eq. (II.16), however, cannot be rigorously obtained by integrating Eq. (II.18) because the potential ψ is a function of both x and y.

Although the asymptotic behavior of the approximated drain current expression, Eq. (II.17) is the same as that obtained from the rigorous Eq. (II.5) in the analytic potential model, there are significant errors in the intermediate region. Using the analytic potential model, the drain current with the charge-sheet approximation, Eq. (II.17), can be shown to be

$$I_{ds}^{CSA} = \left| \mu_{eff} \frac{W}{L} \frac{8\epsilon_{si}}{t_{si}} \left(\frac{kT}{q} \right)^2 \left[p^{CSA}(\beta) \right] \right|_{\beta_s}^{\beta_d} \tag{II.20}$$

where the intermediate function p^{CSA} is

$$p^{CSA} = -\beta \tan(\beta) - 2r\beta^2 \tan^2(\beta). \tag{II.21}$$

The difference to the rigorous drain current equation, Eq. (II.5), is clear. The error between two functions is shown in Fig. Figure II.3:. In the subthreshold

region, $\beta_s \sim 0$ and $\beta_d \sim 0$; in the intermediate region, $\beta_s \sim 0$ and $\beta_d \sim \pi/2$; in the strong inversion region, $\beta_s \sim \pi/2$ and $\beta_d \sim \pi/2$. The maximum drain current error occurs in the intermediate region, where the values of β_s and β_d are not close to each other. As the geometry parameter r decreases, the maximum error in the intermediate region increases.

II.B Quantum Mechanical Effects of Double-Gate MOSFETs

As the thickness of silicon film and oxide of DG MOSFETs decreases to sub-10 nm, quantum mechanical effects become significant and must be taken into account in compact modeling. Quantum mechanical effects in nano-scale MOSFETs are twofold: first, the threshold voltage shifts to a higher value due to the higher electron ground energy; second, the electron concentration peaks away from the surface in contrast to the classical solution in which the carrier density peaks at the surface [58]. Numerical simulations from Poisson and Schrödinger equations show the shift of threshold voltage and the degradation of the slope of $I_{ds} - V_{gs}$ curve, i.e., gate capacitance C_g as a result of the quantum mechanical effects.

Although below derivation is based on the solution of 1-D Poisson and Schrödinger equations for electrons, final expressions are equally applicable to holes, because quantum mechanical effects of holes can also be approximated particles-in-a-potential-well problem. In many commercial compact models, the expressions developed for electrons are also applied to describe quantum mechanical effects of holes by introducing appropriate parameters to take non-idealities into account. Quantum mechanical effects of holes in this dissertation is also described by compact model for electrons.

Unlike the conventional bulk CMOS with 4 terminals, the potential of DG

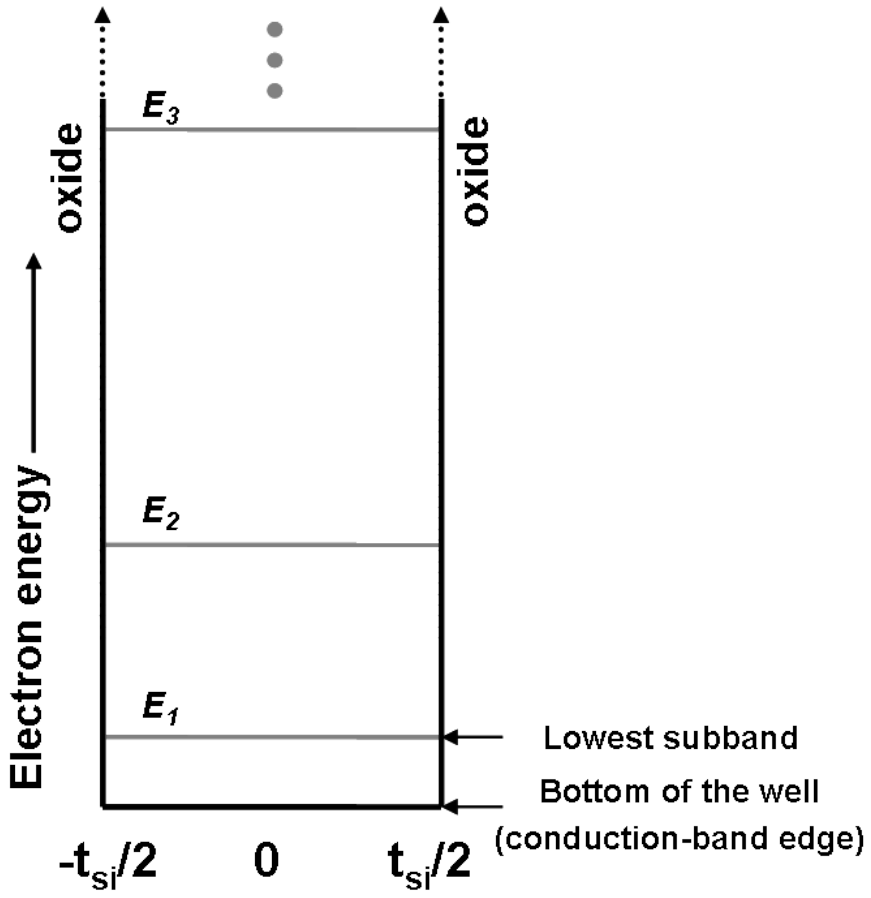

Figure II.4: Quantized energy levels of a DG MOSFET due to quantum mechanical confinement.

MOSFETs in the subthreshold region is essentially flat throughout the silicon film regardless of the oxide thickness due to volume inversion [44]. Since the energy barrier at the oxide interface is very high, the silicon film can be approximated to an infinite potential well (Fig. Figure II.4:). In general, the n^{th} quantized electron energy level in a 1-D infinite potential well is given by

$$E_n = \frac{\hbar^2}{2m^*}\left(\frac{\pi}{nt_{si}}\right)^2 \tag{II.22}$$

Neglecting higher energy level and considering the lowest energy level only, the threshold voltage shift by the electron confinement is given by

$$\Delta V_{th}^{QM} = \frac{E_1}{q} = \frac{\hbar^2\pi^2}{2qm^*t_{si}} \tag{II.23}$$

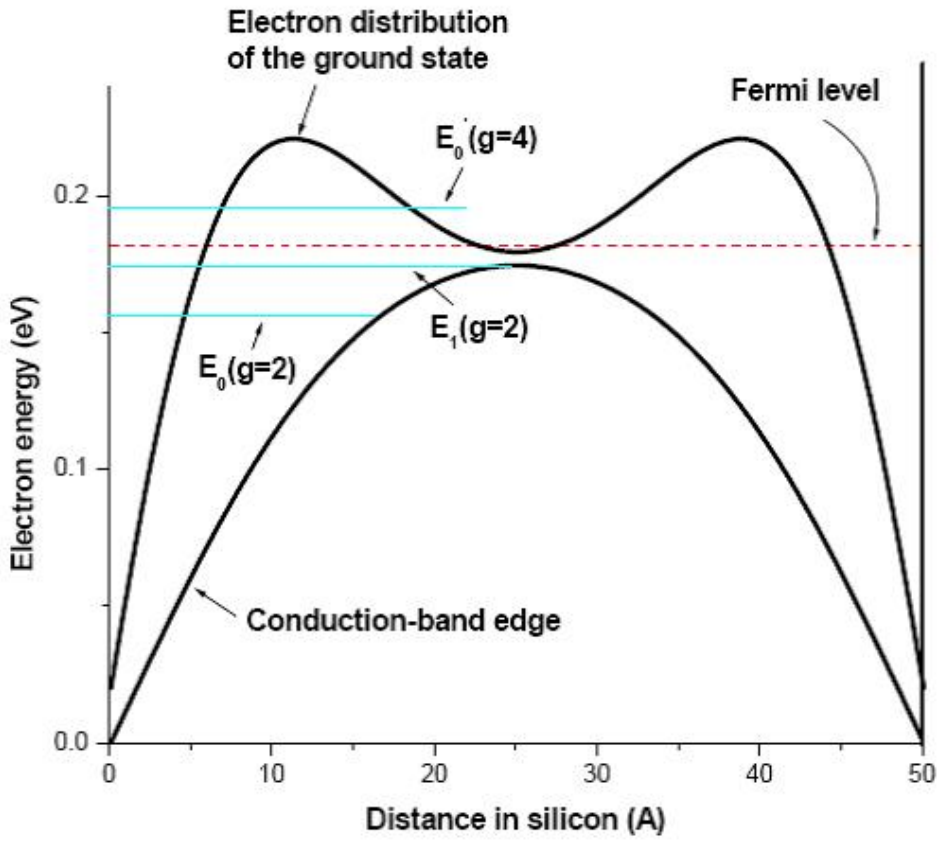

Figure II.5: Electron distribution from coupling Poisson and Schödinger equations in a squre potential well.

where m^* is the effective mass along the confinement direction.

Fig. Figure II.5: shows the shift of the carrier concentration due to quantum mechanical carrier confinement. The inversion layer thickness increases thus the gate capacitance is degraded. The increased inversion layer thickness can be assessed by numerical simulation. An empirical model for the inversion layer thickness is extracted from numerical simulations yielding a similar form to that of the bulk MOSFETs.

$$\delta t_{inv} = \left(\frac{7\epsilon_{si}\hbar^2}{m^* q Q_i} \right)^{1/3} \tag{II.24}$$

This can be lumped into an effective increase of oxide thickness.

It should be noted that the structural parameter of DG MOSFETs, r, is

a function of oxide thickness, hence the boundary condition for β, Eq. (II.3). In order to establish a thorough quantum mechanical correction, the boundary condition Eq. (II.3) must be reformulated with the effective oxide thickness,

$$\frac{q(V_g - \Delta\phi - V)}{2kT} - \ln\left(\frac{2L_{Di}}{t_{si}}\right) = \ln\left(\beta^{QM}\right) - \ln\left[\cos\left(\beta^{QM}\right)\right] + 2r^{QM}\beta^{QM}\tan\left(\beta^{QM}\right) \tag{II.25}$$

where

$$r^{QM} \equiv \frac{\epsilon_{si}(t_{ox} + \delta t_{inv})}{\epsilon_{ox} t_{si}}. \tag{II.26}$$

By substituting Eq. (II.24) into Eq. (II.14), the expression for gate capacitance with quantum mechanical correction is derived by

$$C_g^{QM} = 4WL\frac{\epsilon_{si}}{t_{si}}\frac{\tan(\beta_s^{QM}) + \beta_s^{QM}\sec^2(\beta_s^{QM})}{1/\beta_s^{QM} + \tan(\beta_s^{QM}) + 2r^{QM}\tan(\beta_s^{QM}) + \beta_s^{QM}\sec^2(\beta_s^{QM})} \tag{II.27}$$

The quantum mechanical correction of the finite inversion layer thickness in the gate capacitance expression is captured by the oxide thickness dependence of both r^{QM} and β^{QM}.

By applying the current continuity, the drain current expression with quantum mechanical effects is also obtained.

$$I_{ds}^{QM} = \mu_{eff}\frac{W}{L}\frac{8\epsilon_{si}}{t_{si}}\left(\frac{kT}{q}\right)^2\left[p^{QM}(\beta_d^{QM}) - p^{QM}(\beta_s^{QM})\right] \tag{II.28}$$

where the intermediary function p^{QM} is defined as

$$p^{QM}(\beta) \equiv -2\beta\tan(\beta) + \beta^2 - 2r^{QM}\beta^2\tan^2(\beta^2) - \frac{2}{5}\frac{\epsilon_{si}\delta t_{inv}}{\epsilon_{ox} t_{si}}\beta^2\tan^2(\beta^2). \tag{II.29}$$

Due to the increase of the effective oxide thickness by the non-zero inversion layer thickness, The drain current by Eq. (II.28) is degraded by Eq. (II.5), depending on oxide thickness t_{ox} and quantum mechanical effects decided by the electron effective mass m^* along the confinement direction. It should be noted that each confinement direction is associated with its specific effective mass m^*.

II.C Short-Channel Effects of Double-Gate MOSFETs

As the device dimension decreases, the lateral field penetration from the drain becomes non-negligible, thereby the gradual channel approximation is not valid anymore. The source-drain potential has a strong effect on the band bending over a significant portion of the device. The reduced gate controllability over the channel region [59] and the large field penetration lower the potential barrier in the channel region hence increase the current. In other words, the threshold voltage of the device is decreased.

In CMOS VLSI technology, channel length varies statistically from chip to chip, wafer to wafer, and lot to lot due to process tolerances. The short-channel effect is therefore an important consideration in device design; one must ensure that the threshold voltage does not become too low for the minimum-channel-length device on the chip.

The essence of MOSFET 2-D geometry effect is well-captured by the scale length theory which has been proven a powerful guideline to the minimum channel length design of bulk and DG MOSFETs [60], [61]. To fully quantify the short-channel threshold voltage roll-off, DIBL, and subthreshold slope for compact modeling purposes, the pre-exponential factor of the 2-D potential term needs to be determined in addition to the exponential scale length.

In the subthreshold region in an undoped symmetric DG MOSFET in Fig. Figure II.1:, both the mobile charge and the fixed charge are negligible. Poisson's equation with a non-negligible lateral electric field term then can be written [40] as

$$\frac{d\psi^2(x,y)}{dx^2} + \frac{d\psi^2(x,y)}{dy^2} = 0. \tag{II.30}$$

with the boundary condition

$$\psi\left(-t_{si}/2 - t_i, y\right) = V_g - \Delta\phi \qquad (0 < y < L) \tag{II.31}$$

$$\psi\left(t_{si}/2 - t_i + t_i, y\right) = V_g - \Delta\phi \qquad (0 < y < L) \tag{II.32}$$

$$\psi\left(x, 0\right) = \frac{E_g}{2q} \qquad (-\frac{t_{si}}{2} < x < \frac{t_{si}}{2}) \tag{II.33}$$

$$\psi\left(x, L\right) = V_{ds} + \frac{E_g}{2q} \qquad (-\frac{t_{si}}{2} < x < \frac{t_{si}}{2}). \tag{II.34}$$

2-D simulation results shows that in the oxide gap region between the source/drain and gates, the potential is approximately a linear function of x when $t_{ox}/t_{si} < 1$, e.g., 0.3. The potential in the oxide gap region can then be expressed by linear interpolation

$$\psi\left(x, 0\right) = \frac{E_g}{2q}\frac{(x + t_{si}/2 + t_{ox})}{t_{ox}} - (V_{gs} - \Delta\phi)\frac{(x + t_{si}/2 + t_{ox})}{t_{ox}} \qquad \left(-t_{ox} - \frac{t_{ox}}{2} < x < -\frac{t_{ox}}{2}\right). \tag{II.35}$$

In addition, the Poisson's equation Eq. (II.30) requires $\psi(x, y)$ and $\epsilon(\partial\psi/\partial x)$ be continuous in the x-direction, and $\psi(x, y)$ and $\epsilon(\partial\psi/\partial y)$ be continuous in the y-direction.

A similar approach to the 2-D analysis of the bulk MOSFETs can be carried out with the superposition method. By neglecting high order terms, the 2-D potential expression for SDG MOSFETs in the subthreshold region is given by

$$\psi(x, y) = V_{gs} - \Delta\phi + \frac{b_1 \sinh[\pi(L - y)/\lambda_1] + c_1 \sinh(\pi y/\lambda 1)}{\sinh(\pi L/\lambda_1)} \cos(\pi x/\lambda_1) \tag{II.36}$$

where b_1 and c_1 are the first-order coefficients of the 2-D potential given by

$$b_1 = \frac{2\lambda_1^2 \tan(\pi t_{ox}/\lambda_1)\sin(\pi t_{si}/2\lambda_1)}{\pi^2 t_{ox}\left[\frac{t_{si}}{2} + \frac{\sin(\pi t_{si}/\lambda_1)}{\sin(2\pi t_i/\lambda_1)} t_{ox}\right]}\left(\frac{E_g}{2q} + \Delta\phi - V_{gs}\right), \tag{II.37}$$

$$c_1 = \frac{2\lambda_1^2 \tan(\pi t_{ox}/\lambda_1)\sin(\pi t_{si}/2\lambda_1)}{\pi^2 t_{ox}\left[\frac{t_{si}}{2} + \frac{\sin(\pi t_{si}/\lambda_1)}{\sin(2\pi t_i/\lambda_1)} t_{ox}\right]}\left(\frac{E_g}{2q} + V_{ds} + \Delta\phi - V_{gs}\right). \tag{II.38}$$

λ_1 is the longest scale length that satisfies the eigenvalue equation

$$\tan(\pi t_{ox}/\lambda_1)\tan(\pi t_{si}/2\lambda_1) = \frac{\epsilon_{ox}}{\epsilon_{si}} \tag{II.39}$$

The V_{ds} dependence of c_1 in Eq. (II.36) is responsible for DIBL.

Once the potential is solved, the drain current as a function of the gate voltage expression in the subthreshold region can be derived from current continuity.

$$\begin{aligned} I_{ds} &= \frac{\mu_{eff} W \int_0^{V_{ds}} \exp\left[-q\phi_n(y)/kT\right] d\phi_n(y)}{\int_0^L \frac{dy}{\int_{-t_{si}/2}^{t_{si}/2} n_i \exp\left[q\psi(x,y)/kT\right] dx}} \\ &= \frac{\mu_{eff} W (kT/q)[1 - \exp\left(-qV_{ds}/kT\right)]}{\int_0^L \frac{dy}{\int_{-t_{si}/2}^{t_{si}/2} n_i \exp\left[q\psi(x,y)/kT\right] dx}}. \end{aligned} \tag{II.40}$$

II.40 includes all threshold voltage roll-off, DIBL, and subthreshold current slope degradation.

The threshold voltage roll-off can be extracted by following definition.

$$I_{ds}L(\text{short channel}) = I_{ds}L(\text{long channel}) \times \exp\left[\frac{-q\Delta V_{th}}{kT}\right] \tag{II.41}$$

By considering the minimum potential in the channel length direction,i.e., the most leaky path, explicit expression for the threshold voltage roll-off is obtained by

$$\begin{aligned} \Delta V_{th} = &-2\sqrt{b_1 c_1} \exp\left(\frac{-\pi L}{2\lambda_1}\right) \\ &+ \frac{kT}{q} \ln\left\langle \frac{\sqrt{\pi}}{2D_1 L} \left\{ erf[D_1(L - y_c)] + erf(D_1 y_c) \right\} \right\rangle \end{aligned} \tag{II.42}$$

where the coefficient D_1 is to be

$$D_1 = \left(\frac{\pi^2 q \sqrt{b_1 c_1} \exp\left(-\pi L/2\lambda_1\right)}{\lambda_1^2 kT} \right)^{1/2}. \tag{II.43}$$

Here x_c and y_c are the x and y position at the minimum potential, and function erf is the error function defined as

$$erf(x) = \frac{2}{\sqrt{\pi}} \int_0^x e^{-u^2} du. \tag{II.44}$$

Subthreshold current slope is expressed as

$$\begin{aligned} S \approx &\left\{ 1 - 2B \left[1 + \frac{1}{8} \left(\frac{V_{ds}}{E_g/2q + V_{ds}/2 - V_{g0}} \right) \right] \cos\left(\frac{\pi x_c}{\lambda_1}\right) \exp\left(\frac{-\pi L}{2\lambda_1}\right) \right\}^{-1} \\ &\times 60\text{mV/dec}. \end{aligned} \tag{II.45}$$

In order to control aggressive short-channel effects, the effective channel length, L, must be greater than the longest scale length, λ_1, i.e., $L > 2\lambda_1$. It has been shown that the above explicit expressions of the threshold voltage roll-off and subthreshold current slope agree well with the numerical simulations and experimental data.

II.D High-field effects

In the presence of an high electric field, carriers gain energy from the filed as they drift along, thereby accompany a number of physical phenomena which changes CMOS characteristics significantly can occur. They are primarily identified to be the velocity saturation and the channel length modulation when the electric field is not excessively high.

II.D.1 Velocity Saturation

The velocity of a carrier v is linearly proportional to the electric field E_y by with the coefficient μ_{eff}. However, when the lateral field becomes sufficiently high, the carrier interacts with phonon to lose its energy thereby the carrier velocity tends to saturate. The relation between the velocity saturation and the effective field is empirically known to be

$$v = \frac{\mu_{eff} E_y}{[1 + (E_y/E_c)^{\alpha}]^{1/\alpha}} \tag{II.46}$$

where E_c is the empirically decided critical electric field where the carrier velocity saturates; μ_{eff} is the effective mobility at the low lateral field; α is a fitting parameter indicating how fast the velocity saturates.

When the empirical parameter $\alpha = 1$, a closed-form drain current expression is obtained. However, odd α breaks source and drain symmetry thus gives undesirable discontinuity of high order derivatives of the drain currents [62]. For

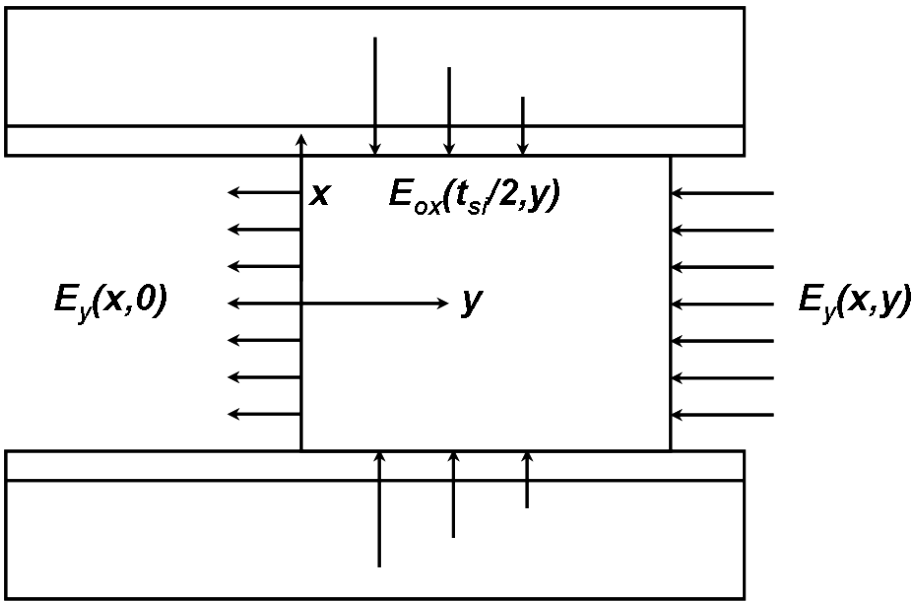

Figure II.6: Schematic diagram of the velocity saturation region for illustrating the pseudo-2-D model.

compact modeling purpose, even α is necessary. Because even α does not yield a closed-form drain current expression, an approximate solution is developed to model the velocity saturation effects in DG MOSFETs.

$$I_{ds}(\text{velocity saturation}) = \frac{I_{ds}(\text{no velocity saturation})}{[1+(V_{ds}/E_cL)^{\alpha}]^{1/\alpha}} \tag{II.47}$$

II.D.2 Channel length modulation

When sufficiently high drain bias is applied, the lateral field becomes comparable to the vertical field, so that the gradual-channel approximation employed in the long-channel core model becomes invalid and carriers are no longer confined to the surface channel. As the drain voltage increases beyond the saturation voltage V_{dsat}, the saturation point where the surface channel collapses begins to move slightly towards the source. In other words, the channel length effectively shrinks to be $L-\Delta L$. This causes non-zero conductance g_{ds} in the saturation region.

A pseudo-2-D model based on the application of Gauss's law for the bulk

CMOS [63] can also be applied to analyze the channel length modulation of DG MOSFETs. By assuming a rectangular saturation region and apply the Gauss's law to the saturation region, an expression of ΔL is derived in the similar form as the bulk CMOS.

$$\Delta L = \sqrt{\frac{\epsilon_{si} t_{si} t_{ox}}{\epsilon_{ox}}} \ln \left[\frac{V_{ds} - V_{dsat} + \sqrt{(V_{ds} - V_{dsat})^2 + (E_{sat} l)^2}}{E_{sat} l} \right] \tag{II.48}$$

where the characteristic length l is given by

$$l = \sqrt{\frac{\epsilon_{si} t_{si} t_{ox}}{\epsilon_{ox}}} \tag{II.49}$$

and the E_{sat} is the electric field at the saturation point. The drain current with channel length modulation can then be expressed as

$$I_{ds}(\text{channel length modulation}) = \frac{L}{L - \Delta L} I_{ds}(\text{no channel length modulation}) \tag{II.50}$$

II.E Summary

The full-blown analytic potential model for DG MOSFETs has been introduced. Quantum mechanical effects was added to the core model based on the 1-D Poisson's equation to consider the inversion layer thickness and threshold voltage shift. The core model is seamless through all operation regions and describes the volume inversion effects properly. The short-channel effects has been described in terms of the threshold voltage roll-off, the DIBL, and the subthreshold current slope degradation. High-field effects also has been included in the core model in regard of the velocity saturation and the channel length modulation.

The text of Chapter Chapter II, in part, is a reprint of the material as it appears in "A Review on Compact Modeling of Multiple-Gate MOSFETS" by Jooyoung Song, Bo Yu, Yu Yuan, and Yuan Taur, IEEE Transaction on Circuits and Systems I:Regular Papers, Aug 2009. The dissertation author was the primary investigator and author of this paper.

Chapter III

Experimental FinFET Hardware

To fully validate a compact model, model verification by experimental hardware is essential in addition to numerical simulations. The fabrication of DG MOSFETs, however, is still in its early stage. So far, only limited number of devices are available in public. Although a few researches on hardware calibration has been done based on published DG FinFET and TG MOSFET data, the limited range of device geometries has prevented comprehensive validation of DG MOSFETs. Moreover, active employment of novel technologies introduces beneficial but requires additional modeling concern. To incorporate those non-ideal effects adequately, the nature of the effects needs to be identified carefully.

Experimental FinFETs were fabricated over a wide range of gate lengths for both n- and p-channel FinFETs by Advanced Technology Development Facility associated with Texas Instruments, Inc. Gate capacitances and drain currents at various gate and drain biases are available with high resolution. Employing identical technology and process to all experimental hardware allows systematic compact modeling from long-channel to medium- and short-channel devices in order.

In this chapter, the specification, the fabrication process, and the mea-

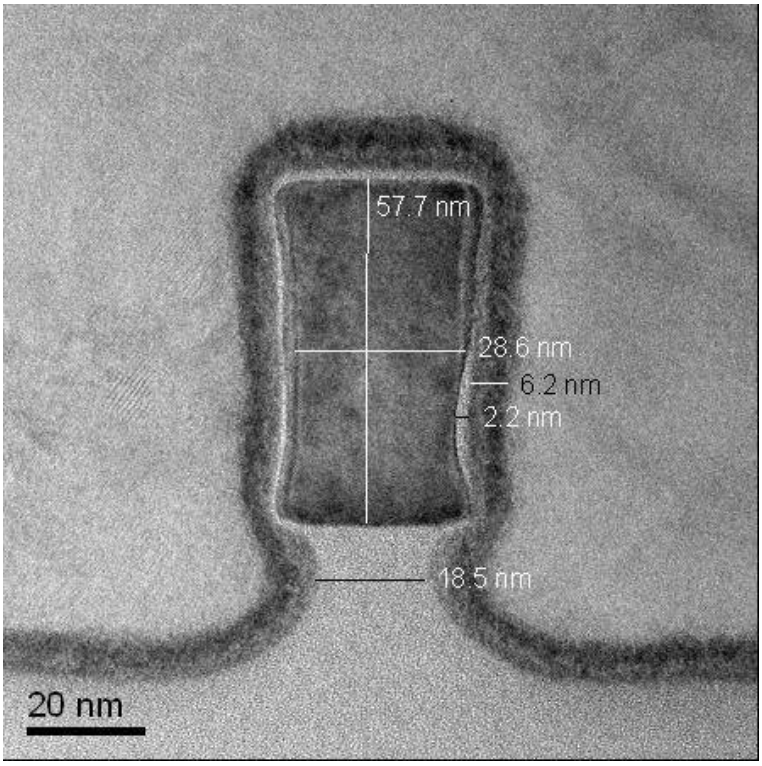

Figure III.1: An SEM picture of the cross-section of a FinFET perpendicular to the channel direction.

surements of experimental hardware used in calibration are described in detail to provide a firm basis to understand physical phenomena to be discussed in later chapters. The author would like to acknowledge Advanced Technology and Development Facility and Texas Instruments, Inc. for providing valuable experimental FinFET data.

III.A Hardware Specification

N- and p-channel FinFETs were fabricated with $\langle 110 \rangle$ channel orientation on an (100)-surface oriented SOI substrate with a 145-nm thick BOX layer. As a result, the top surface of the FinFETs is (100)-surface oriented, whereas the sidewalls have (110)-surface orientation. The schematics of a DG FinFETs with

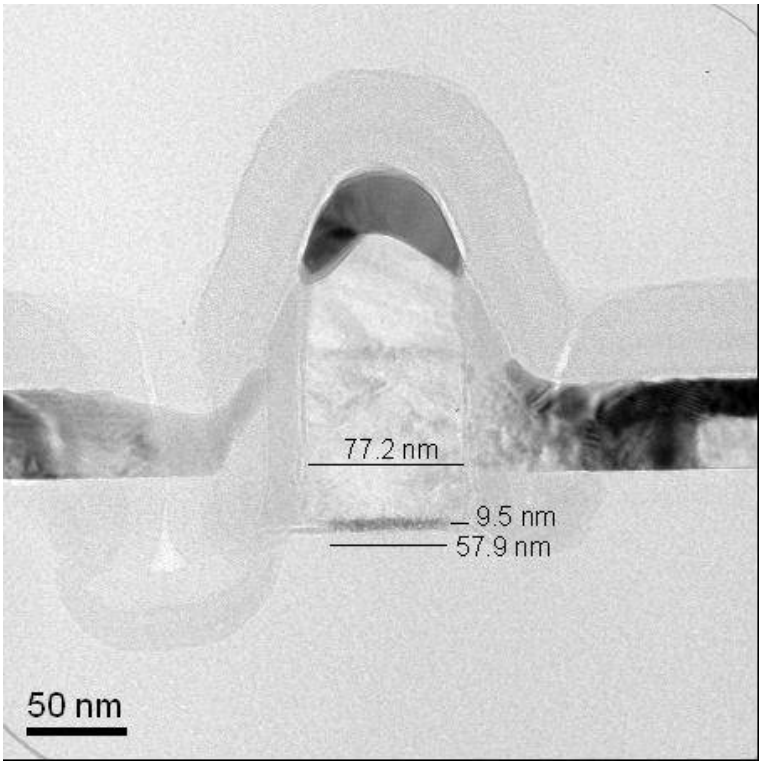

Figure III.2: An SEM picture of the cross-section of a FinFET along the channel direction.

given surface orientation is presented in Fig. Figure I.10:. It should be noted that the band structure is dependent of surface- and channel-orientation dependent, and so is the effective mass of carriers. Due to the different effective mass, the carrier mobility and the quantum mechanical effects also have dependence of surface- and channel-orientation and must be considered in compact modeling of experimental hardware.

The fin height of the experimental hardware is 60 nm; the fin width is drawn by 55 nm with the physical width of 30 nm. The SEM picture of the cross-section of a fin presented in Fig. Figure III.1: shows a close agreement between the nominal specification and the physical device geometry. An Optical Proximity Correction (OPC) process was employed to fabricate fins with identical dimension over all gate lengths.

The gate length are drawn from 10 μm to 90 nm. 10-μm FinFETs are long-channel devices with an ideal capacitance and current characteristics; 5 μm, 1 μm, and 0.25 μm are medium-channel devices; 110 nm, 100 nm, 95 nm, 90 nm, and 85 nm are short-channel devices. The lateral cross-section of a FinFET is shown in Fig. Figure III.2:.

2-nm thick silicon dioxide was used as gate dielectric. For the gate electrode, a 10-nm thick TiSiN metal gate with mid-gap work-function is deposited, followed by a 10-nm thick amorphous Si deposition and a 5-nm nitride spacer formation. Fig. Figure III.1: shows a very uniform deposition of the gate oxide and electrode.

The number of fins is 20 to increase the drain currents and alleviate the process variation of the devices. In addition, the increase currents provides higher immunity to the noise introduced in measurements. The shape of the body of the fins are almost perfect rectangle; therefore the experimental FinFETs are well-approximated to the ideal DG FinFET structure presented in Fig. Figure I.9:(b). Non-zero gate tail at the bottom of the fins is introduced during an etching process. The aggressive etching of the bottom of the fin provides an excellent isolation from the BOX, hence less lateral field penetration through the BOX. The metal gate stack at the bottom of the fins acts as an additional short bottom gate; the experimental FinFETs act similar to Π-gate MOSFETs.

III.B Fabrication Process

The fabrication starts from an SOI material from SOITEC as shown in Fig. Figure III.3:. 88-nm thick initial silicon is thinned to 60 nm by oxidation on an 145-nm thick BOX. Fin hard mask of 4.5-nm thick oxide and 20-nm thick nitride is deposited on the silicon film.

After 30-nm wide fin patterning Fig. Figure III.4:, fin hard mask is stripped with hot phosphorus and hydrogen fluoride (HF). 3-nm thick dry sidewall oxidation

Figure III.3: A starting SOI material after initial oxidation.

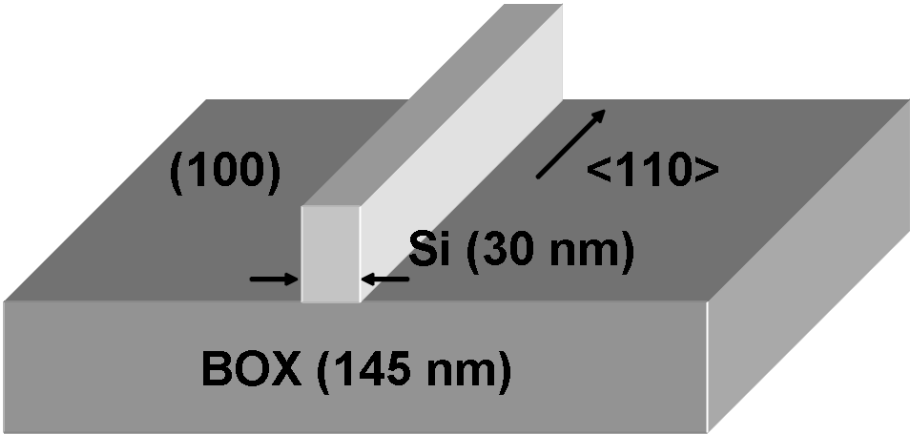

Figure III.4: An initially patterned fin structure.

is then performed, followed by high-temperature annealing. The sidewall oxide is stripped by vapor HF, and H_2 annealing is performed.

2-nm thick gate oxide is deposited by in-situ-stream-gas (ISSG) oxidation, followed by the gate stack deposition of 10-nm thick TiSiN and 10-nm thick amorphous-silicon, and 50-nm thick SiN. 55-nm nitride hardmask for gate patterning is deposited after resist etch-back planarization to form smooth surface. The patterned gate structure is presented in Fig. Figure III.5:.

5-nm spacer nitride with lightly-doped-drain (LDD) implantation is de-

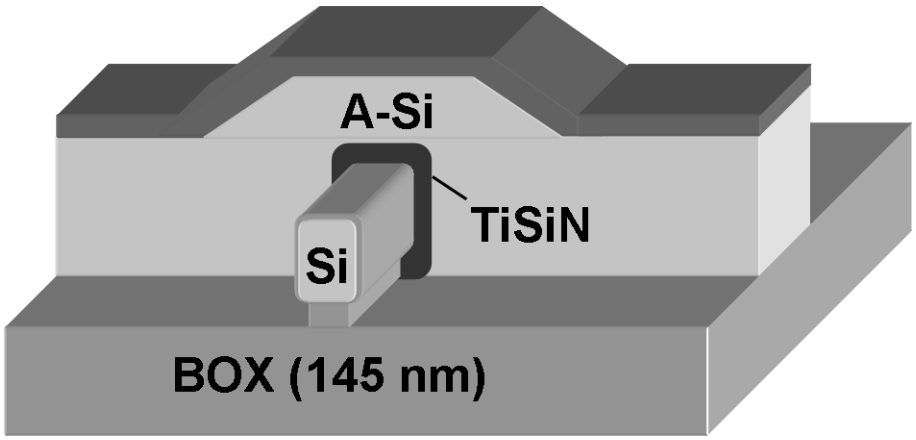

Figure III.5: A fin structure with gate stack deposition and patterning.

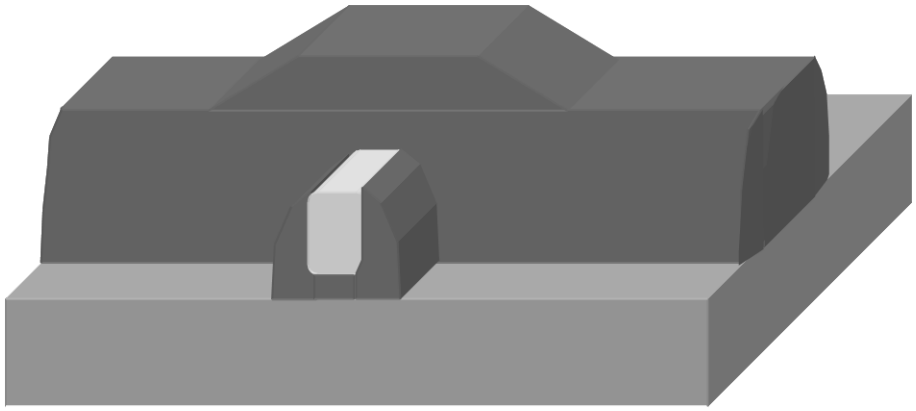

Figure III.6: A fin structure after spacer nitride deposition and N-type lightly-doped drain (NLDD) implant.

posited after 55-nm gate pattering. Finally, 50-nm thick second spacer and deep source/drain implantation finish the fabrication of the experimental hardware.

III.C Measurements

Gate capacitance and drain currents of the FinFET hardware were measured with various gate and drain biases in the room temperature. The supply voltage V_{DD} is 1.0 V.

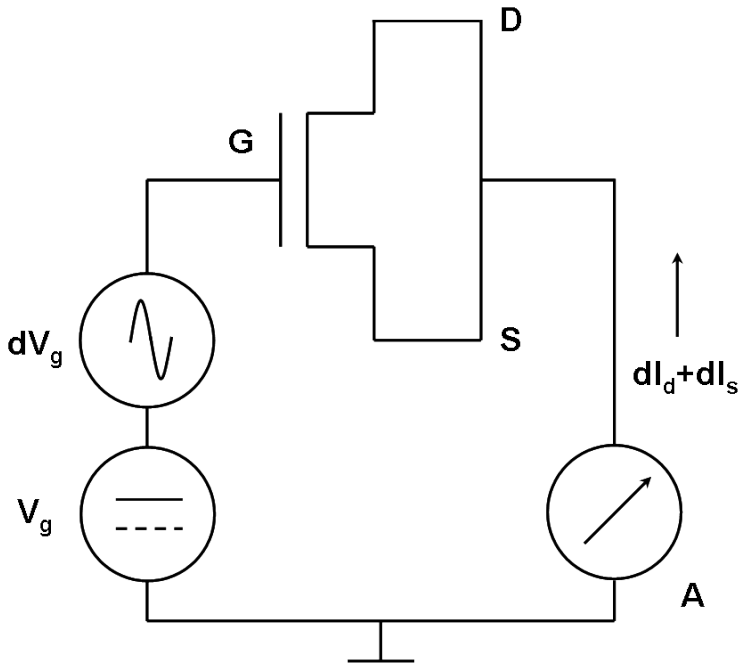

Figure III.7: Scheme of the low frequency split CV measurement for 3-teminal devices including DG FinFETs (Adopted from [64]).

$C_g - V_g$ data of 10-μm n- and p-channel FinFETs are measured with gate bias from 0 V to 1.5 V by widely adopted split $C - V$ method [64]. The basic scheme of the split $C - V$ method of a FinFET is shown in Fig. Figure III.7:. Because of the absence of body contact, body current I_b, present in conventional 4-terminal devices, is not measured in the capacitance measurement of FinFETs or other SOI devices with floating body. The resolution of the gate capacitance is 6 digits with high accuracy.

The drain currents data of the n- and p-channel FinFETs were measured over all the gate lengths from 10 μm to 85 nm. $I_{ds} - V_{gs}$ data with both low and high drain biases are available. The low drain bias is 50 mV, and the high drain bias is 1.0 V, i.e., V_{DD}. $I_{ds} - V_{ds}$ data were measured with the gate biases of 0 V, 0.2 V, 0.4 V, 0.6 V, 0.8 V, and 1.0 V. The resolution of the drain currents is 5 digits.

Because both the gate capacitance and the drain current versus the gate voltage are available for 10-μm, n- and p-channel FinFETs,long-channel electron and hole mobilities can be extracted. With the low drain bias of 50 mV, the following drain current expression for linear region is applicable, namely,

$$\mu_{eff} = \frac{I_{ds}}{\frac{W}{L}\int Q_i(V_{gs})dV_{gs}} \tag{III.1}$$

where

$$Q_i = \int C_g(V_{gs})dV_{gs} \tag{III.2}$$

The method is widely adopted by industry for long-channel devices with negligible parasitic components. The resulted mobilities are comparable with reported long-channel electron and hole mobilities under tensile strain.

The mobilities of medium- or short-channel devices, however, are not readily extractable from raw capacitance and drain current data due to non-negligible parasitic effects, and are believed to be the same as the long-channel in general for the compact modeling purpose.

III.D Experimental FinFETs as Double-Gate MOSFETs

As briefly discussed in Chapter Chapter I, DG FinFET is a common form of realized DG MOSFET structure due to its intrinsic compatibility with the conventional bulk MOSFET process. A FinFET structure is not identical, but similar to a DG MOSFET structure except the presence of its top-gate as shown in Fig. Figure I.9:.

To approximate a FinFET to a DG MOSFET with physical sanity, the height of the FinFET is sufficiently long to lead a relatively small top-gate effects. The experimental devices have the height of 60 nm and the width of 30 nm. The width of the FinFETs are narrow enough to allow close coupling of two gates. In

addition, the ratio of the top gate and the sidewalls is small to minimize effects by two different surface orientations. For the devices in concern, the sidewall structure is dominant, and therefore the inversion layer can be considered to be formed on (110)-oriented surface with the introduction of an appropriate fitting parameter. Furthermore, the corner effects by the rounding of the top-gate structure has been reported to be almost negligible by numerical simulations and experiments. In conclusion, the analytic DG MOSFET model described in Chapter Chapter II can be applied to the experimental FinFETs, since the conditions for the approximation of FinFETs to DG MOSFETs are satisfied. The validity of the model is now shown by the calibration of n-channel and p-channel FinFETs over a wide range of gate lengths in the later chapters.

III.E Summary

The experimental FinFET hardware has been described in this chapter. The physical dimension of the fins were given by a TEM picture as well as the drawn gate lengths. The fabrication process has been summarized briefly. The metal gate material introduces tensile strain to the channel region. The given fin structure can be safely approximated to a double-gate structure with physical sanity.

The text of Chapter Chapter III, in part, is a reprint of the material as it appears in "Gate-Length-Dependent Strain Effects in N- and P-Channel FinFETs" by Jooyoung Song, Bo Yu, Yu Yuan, and Yuan Taur, IEEE Transaction on Electron Devices, Mar 2009. The dissertation author was the primary investigator and author of this paper.

The text of Chapter Chapter III, in part, is a reprint of the material as it appears in "Compact Modeling of Experimental N- and P-Channel FinFETs" submitted to IEEE Transaction on Electron Devices. The dissertation author was

the primary investigator and author of this paper.

Chapter IV

N-Channel FinFET Hardware Calibration of Double-Gate MOSFET Compact Model

For the conventional bulk MOSFETs, a great number of experimental hardware calibrations have been reported by a variety of compact models [65], [66]. Several important compact models for bulk MOSFETs widely adopted in the semiconductor industries include BSIM3, BSIM4, and PSP. Due to their innate physics-based properties, they have been shown to predict device characteristics closely when geometric and electrical parameters are given.

The device physics of MG MOSFETs, however, is different from that of the bulk MOSFETs, and therefore, the compact models for the bulk MOSFETs are not able to regenerate the capacitances and currents of MG MOSFETs [35]. Furthermore, the available experimental MG MOSFET data are significantly smaller than the bulk MOSFETs. Only limited number of researches on compact modeling of experimental MG MOSFETs have been published so far. Therefore, a systematic validation of compact model by experimental MG MOSFET hardware is necessary.

To begin the compact modeling, n-channel devices are more appropriate than p-channel devices in general. It has been known that n-channel devices are more immune to the short-channel devices, thus act closer to the ideal devices. This is primarily due to the slow Arsenic diffusion hence the steep doping profile in channel region. High electron mobility results in high drain current in n-channel devices. Moreover, highly complicated hole band structure makes it difficult to analyze quantum mechanical effects of inversion layer.

Detailed procedure of a systematic compact modeling of n-channel FinFETs with previously described DG MOSFETs are covered in this chapter. First, $C_g - V_{gs}$ data of a long-channel n-channel FinFET is calibrated with the 1-D analytic potential model for DG MOSFETs incorporated with quantum mechanical effects. With extracted geometric parameters, $I_{ds} - V_{gs}$ data is modeled by a physical mobility model. Medium-channel FinFETs are modeled with the geometric parameters and the mobility model after separating out source-drain series resistance effects. The short-channel effects are validated in terms of the threshold voltage roll-off, the DIBL, and the subthreshold current slope degradation by the 2-D analytic potential model for DG MOSFETs. The addition of high-field effects completes the compact modeling of n-channel FinFETs.

IV.A Compact modeling of a $C_g - V_{gs}$ data

Compact modeling of CMOS device starts from $C_g - V_{gs}$ data, whenever capacitance data are available. Gate capacitance per unit area, C_g, is a function of device geometry and gate bias only with the measurement configuration of Figure III.7:, i.e., $V_{ds} = 0$ [45], [44]. Because the gate capacitance does not depend on mobility thus drain current, a series of non-ideal effects accompanied by drain current are absent in the $C_g - V_{gs}$ data without any additional procedure.

The expression for gate capacitance of DG MOSFETs with quantum cor-

rection is derived as II.27. The gate capacitance depends only a few parameters: the geometric parameters including the gate length L, effective width W_{eff}, oxide thickness t_{ox}, silicon thickness t_{si}, and a structural parameter r^{QM}; work-function difference between the gate material and the silicon $\Delta\phi$; and the gate and drain biases V_{gs} and V_{ds}.

IV.A.1 Geometric parameters for $C_g - V_{gs}$ calibration

Because there are multiple number of unknown parameters, one needs to make an appropriate assumption to reduce the mathematical calculation load of the calibration.

First, a very long device is free from the effect caused by the difference between the effective channel length and the physical drawn length. It has been widely shown that the actual gate length is smaller than the drawn gate length due to dopant diffusion. In addition, complex modern semiconductor fabrication process including material deposition, etching, masking, and optical proximity correction (OPC) may result a different effective channel length from the drawn gate length. However, usually the difference is comparable to a few nm, so that the introduced deviation of the device characteristics is essentially unrecognizable in 10-μm devices. The immunity to the channel length shrinking of long channel devices validate assuming the gate length is given by 10 μm.

Furthermore, practically all the parasitic effects are negligible in long channel devices. For example, the overlap capacitance of modern CMOS is known to be about 0.3 fF/μm resulting about 1 fF for the devices in consideration. The measured total gate capacitance in the strong inversion region is about 400 fF. The ratio of two components is 400, thereby the overlap capacitances are negligible. Therefore, one can safely ignore all the parasitic components, and employ the long-channel core model to the hardware in consideration.

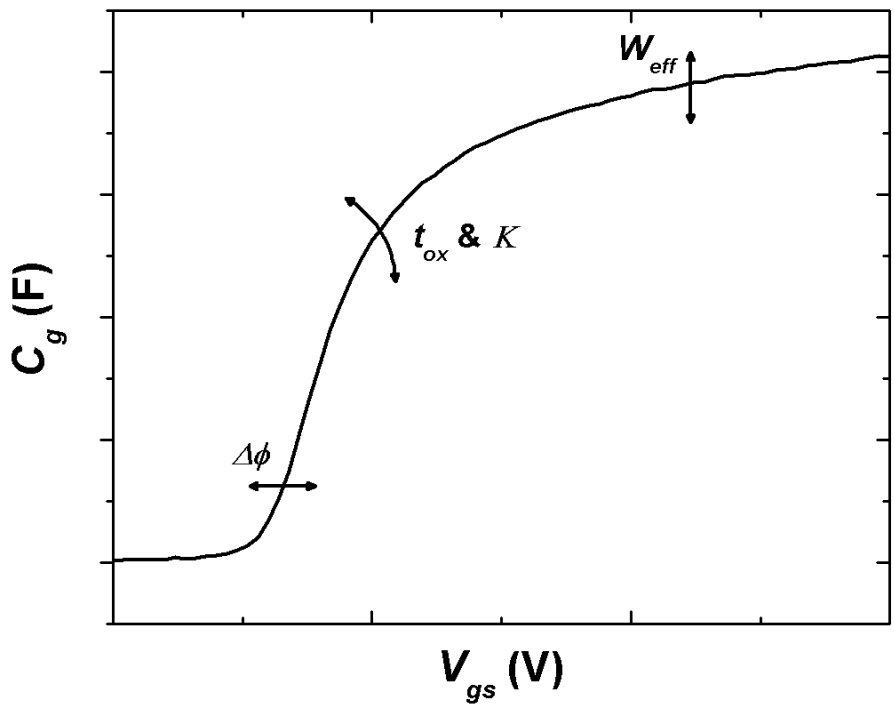

Figure IV.1: Illustration of the effects of geometric parameters of FinFETs to $C_g - V_{gs}$ data. W_{eff} is the effective width, t_{ox} the oxide thickness, $\Delta\phi$ the work-function difference gate material and the silicon, and K the coefficient for quantum mechanical effects.

In TG MOSFET structure, it has been extensively shown by numerical simulations that the corner effects do not change the device characteristics noticeably. Also, the width and height of the fins are well-controlled as presented in Fig. Figure III.1:. The dimension of the fins, therefore, can be assumed to be the same as the measured physical values.

The determination of the above parameters leaves device width, oxide thickness, and the work function of gate material. Although the approximate values of these parameters are known by SEM picture or measurements, the exact values

for compact modeling are different from the nominal values. For example, the device width is difficult to determine due to the presence of the non-zero gate tail structure at the bottom of the fins (see Fig. Figure III.1:). Although the total width of 20 fins is about 3 μm, each fin does not have an ideal DG FinFET structure covering only 3 sides completely. Considering the non-zero gate tail structure, defining effective device width is necessary by a systematic and physically-sound method. The extracted effective width must be comparable to the nominal device width, i.e., 3 μm for 20 fins.

The oxide thickness t_{ox} is also extracted from the measurement data. The oxide thickness of modern CMOS devices has shrunken aggressively below a few nanometer. Although the physical value of the oxide thickness is given by an SEM figure (Figure III.1:), it is extremely difficult to control the thickness of ultra thin oxides. Effective oxide thickness is defined to represent the oxide thickness in regards to the electric properties of the FinFET hardware.

The work-function of the metal gate is also subject to a finite variation. The nominal value of the deposited TiSiN gate material is located at the mid-gap level of the silicon. However, it was reported that the work-function of TiSiN is a function of the thickness of the gate [67]. Since the nominal thickness of the metal gate is only 5 nm, it is also difficult to control the thickness of the gate, hence the work-function of the gate material. The error of the work-function is measured to be about 50 mV from the mid-gap. The The work-function, therefore, must be extracted for each individual FinFET.

Although all the geometric parameters and the work-function of gate material are covered, a coefficient for quantum mechanical effects, K, remains to be determined during the calibration. Remembering that the quantum mechanical correction on the finite inversion layer thickness assumes an infinite square quantum well, a coefficient to lump the effects of the finite barrier height is necessary. Furthermore, in DG FinFET structure, the electrons in the inversion layer

experience two different surface orientation, namely, (110)-oriented surface and (100)-oriented surface. Because electrons have different effective masses on each surface, the deviation from perfect (110)-oriented surface must be included in K.

The effects of the geometric parameters for the compact modeling of $C_g - V_{gs}$ data are presented in Fig. IV.A.1. The effective width linearly scales the C_g curve for all gate bias regime, and the work function difference between the gate material and the silicon body $\Delta\phi$ horizontally moves the curve. Without quantum mechanical effects, the oxide thickness t_{ox} also linearly scales the gate capacitance; with the inclusion of the finite inversion layer thickness, effective oxide thickness given by II.24 depends on the gate bias. The gate bias dependence of the inversion layer thickness controls the slope of C_g in the vicinity of the threshold voltage condition.

In summary, for the 10-μm n-channel FinFET, many parameters can be used in their nominal values: the gate length L, the height and the width of fins. The remaining parameters extracted from the $C_g - V_{gs}$ calibration are the effective device width W_{eff}, the oxide thickness t_{ox}, the work-function of the gate material $\Delta\phi$, and the quantum mechanical coefficient K.

IV.A.2 Calibration of $C_g - V_{gs}$ data

$C_g - V_{gs}$ calibration is performed to minimize the error between the model data and the experimental data. Two possible choices exist to define the error. First, the ratio of the model and the experimental data yields a well-fitted $C_g - V_{gs}$ curve.

$$R_{C_g}(V_{gs}) \equiv \frac{C_g^{model}(V_{gs})}{C_g^{exp}(V_{gs})} \tag{IV.1}$$

The closer to the unity the ratio is, the smaller the error. The method is a generalized form of *Shift-and-Ratio* method by Taur [68].

Second, simply the absolute value of the difference of the model and exper-

imental data can be another parameter to minimize.

$$D_{C_g}(V_{gs}) \equiv \left| C_g^{model}(V_{gs}) - C_g^{exp}(V_{gs}) \right| \tag{IV.2}$$

In both cases, to choose the set of parameters which minimizes the standard deviation of errors yields the best fitting curve.

$$\sigma(R_{C_g}) \equiv \left[\int_{V_s}^{V_d} \left(R_{C_g} - R_{mean} \right)^2 dV_{gs} \right]^{1/2} \tag{IV.3}$$

$$\sigma(D_{C_g}) \equiv \left[\int_{V_s}^{V_d} \left(D_{C_g} - D_{mean} \right)^2 dV_{gs} \right]^{1/2} \tag{IV.4}$$

where R_{mean} and D_{mean} are the averages of the ratio and the difference, respectively.

With the help of numerical computing languages such as *Matlab* or *Mathematica*, the parameter sets yielding minimum standard deviations can be obtained automatically. Being different from simple two parameter analysis in the original *Shift-and-Ratio* method, all four parameters to be extracted are substituted to calculate the local minimum of the errors.

Due to the nature of two methods, comparing the ratio agrees better in the weak inversion region, whereas minimizing the absolute difference matches in the strong inversion region. In the subthreshold region, the capacitance is very small, thereby both methods yield extremely small errors.

Fig. Figure IV.2: and Fig. Figure IV.3: illustrate the calibration results by minimizing the standard deviation of the ratio and the difference, respectively. As expected, comparing the standard deviation of the ratio of two curves gives an excellent agreement especially in the vicinity of the threshold voltage condition, whereas minimizing the difference yields closely matched strong inversion region. The extracted model and nominal parameters of the 10-μm n-channel FinFET are given in Table Table IV.1:.

The choice of $C_g - V_{gs}$ calibration for further compact modeling depends on the region of interest. When the compact modeling is performed for analog circuit

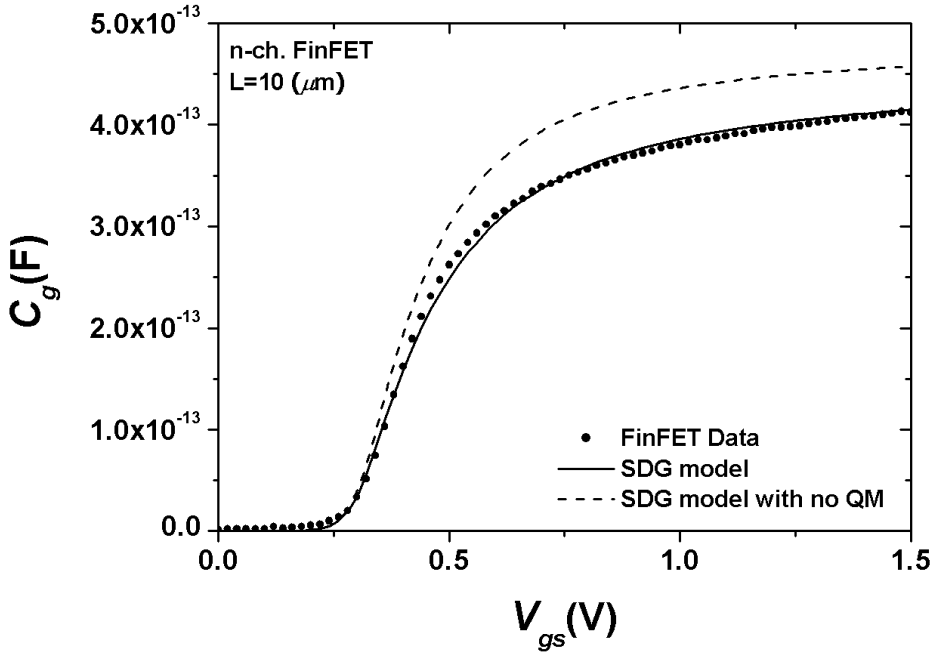

Figure IV.2: Model and measured $C_g - V_{gs}$ data of a 10-μm n-channel FinFET by minimizing the standard deviation of the ratio of two values. Symbol is for the measured data, dashed line for the model without quantum mechanical correction, solid line for the model with quantum mechanical correction.

simulations, the transition region or weak inversion region is significant. Accuracy in the strong inversion region is desirable for digital circuit simulations. A hybrid method is also a valid option for calibration, when mathematical complexity is not important. In this dissertation, further compact modeling is based on the minimization of the difference, being suitable for digital circuit simulations.

As can be seen in Fig. Figure IV.4:, quantum mechanical capacitance due to the finite inversion layer thickness plays a role in addition to oxide capacitance and inversion capacitance. In the subthreshold region, the inversion capacitance is not observed; in the strong inversion region, the inversion capacitance becomes very large so that the oxide and quantum mechanical capacitances play a dominant

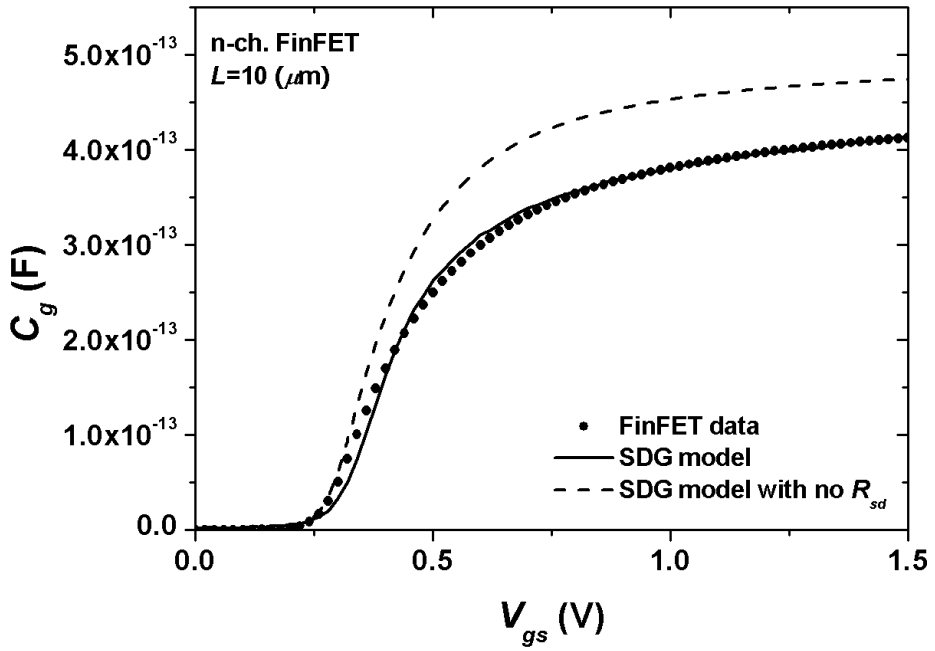

Figure IV.3: Model and measured $C_g - V_{gs}$ data of a 10-μm n-channel FinFET by minimizing the standard deviation of the difference. Symbol is for the measured data, dashed line for the model without quantum mechanical correction, solid line for the model with quantum mechanical correction.

role. In the strong inversion region, the inversion capacitance can be excluded in the analysis of the $C_g - V_{gs}$ data. With small gate bias, there is no inversion layer and thus, no capacitance due to quantum mechanical effects is observed. As the gate bias increases and the inversion layer forms, the quantum mechanical capacitance becomes significant to degrade the oxide capacitance hence the slope of the transition region.

The measured data has the steeper slope in the transition region due to corner effect from the non-ideal geometry. The corner effects and the surface-orientation dependence of the electron effective mass are lumped to the quantum

Table IV.1: Nominal and extracted parameters by model with and without quantum mechanical correction of 10-μm n-channel FinFETs.

Parameter	Unit	Nominal Values	Model by Ratio	Model by Difference
W_{eff}	nm	150	154.4	167.6
L	μm	10	10	10
t_{ox}	nm	2.0	2.2	2.2
t_{si}	nm	30.0	30.0	30.0
$\Delta\phi$	mV	0	-79	-65

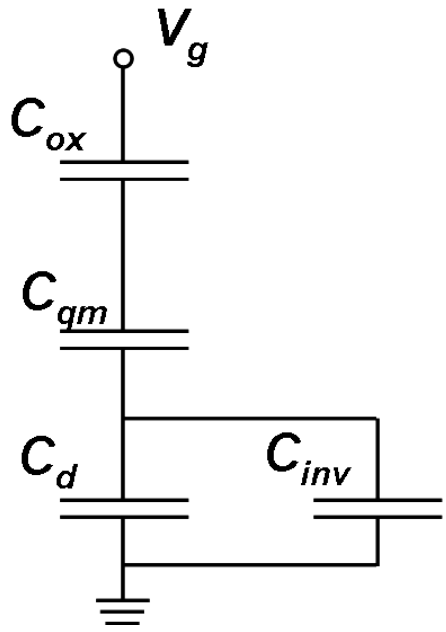

Figure IV.4: A simple capacitance model for a long-channel FinFET with quantum mechanical effects. C_{ox} is gate oxide capacitance, C_{qm} quantum mechanical capacitance due to finite inversion layer, C_d depletion capacitance, and C_{inv} inversion capacitance.

mechanical coefficient. The extracted effective width is slightly larger than the nominal value presumably due to the non-zero gate tail structure at the bottom of the fins. Considering the gate-tails, the effective width well agrees with the measured physical dimension of the fins. Also, the thickness of the gate oxide is 2.2

nm and is very close to the measured value. It should be noted the effective width and the oxide thickness are electrically decided, suitable for compact modeling. The work-function difference between the metal gate and the silicon mid-gap is determined as -0.06 V to be in the range of the expected error bar. The long-channel threshold voltage extracted from the model is about 0.4 V. Fig. Figure IV.3: shows a close agreement between the threshold voltage of the model and the measurement.

The model without quantum mechanical correction, dashed curve in Fig. Figure IV.3:, obviously overestimates the gate capacitance due to the absence of the capacitance degradation by the finite inversion layer thickness. Classical model for gate capacitance to calibrate the experimental $C_g - V_{gs}$ data requires the oxide thickness of 5 nm or higher. The number is much greater than the nominal value, being unphysical. On the contrary, the model with quantum mechanical correction closely matches with the experimental data with physically sound parameters. The quantum mechanical correction is necessary to model the gate capacitance data of the long-channel n-channel FinFET.

It is worthy to note that the $C_g - V_{gs}$ curve of the experimental long-channel FinFET does not have local maximum in the strong inversion region. Usually, gate capacitance of CMOS degrades with high gate overdrives due to the polysilicon depletion effects [69]. When the gate material consists of polysilicon, the gate capacitance degrades at high gate overdrives due to the depletion region at the polysilicon gate. The induced charges form additional parasitic capacitance component above the gate oxide capacitance in Fig. Figure IV.4:. The experimental devices have metal gate, hence no depletion region is formed. The gate capacitance, therefore, monotonously increases as the gate bias increases, because the inversion layer decreases and thus serial quantum mechanical capacitance increases.

IV.B Compact modeling of a long-channel n-channel FinFET

Since all the geometric parameters are extracted from the calibration of $C_g - V_{gs}$ data, the drain currents of the device can be modeled. $I_{ds} - V_{gs}$ data of a long-channel FinFET with low drain bias is an ideal choice for the next step, because most parasitic effects including high-field effects and source-drain sires resistance effects as well as the short-channel effects are negligible. The drain current data of the 10-μm n-channel FinFET used in $C_g - V_{gs}$ calibration is available.

To connect the gate capacitance and the drain current, mobility model is necessary. With a versatile mobility model, drain current of the long-channel n-channel FinFET is calibrated with the analytic potential model for DG MOSFETs including quantum mechanical effects.

IV.B.1 Long-channel mobility of n-channel FinFET

The raw electron mobility data from the measurement data is presented in Fig. Figure IV.5: extracted by Eq. (III.1). The effective field are calculated by Gauss's law,

$$\begin{aligned} E_{eff} &= \frac{Q_d + Q_i}{2\epsilon_{si}} \\ &= \frac{Q_i}{2\epsilon_{si}} \end{aligned} \tag{IV.5}$$

where Q_d is the depletion charge, which is negligible with the undoped silicon body. The mobility shows degradations in both the low and high field regime due to Coulomb and phonon scattering, respectively. The peak mobility is about 550 cm·V/s^2, and the mobility in the strong inversion region is 300 cm·V/s^2. The values are comparable to the reported electron mobility data on (110)-oriented surface with tensile strain [67].

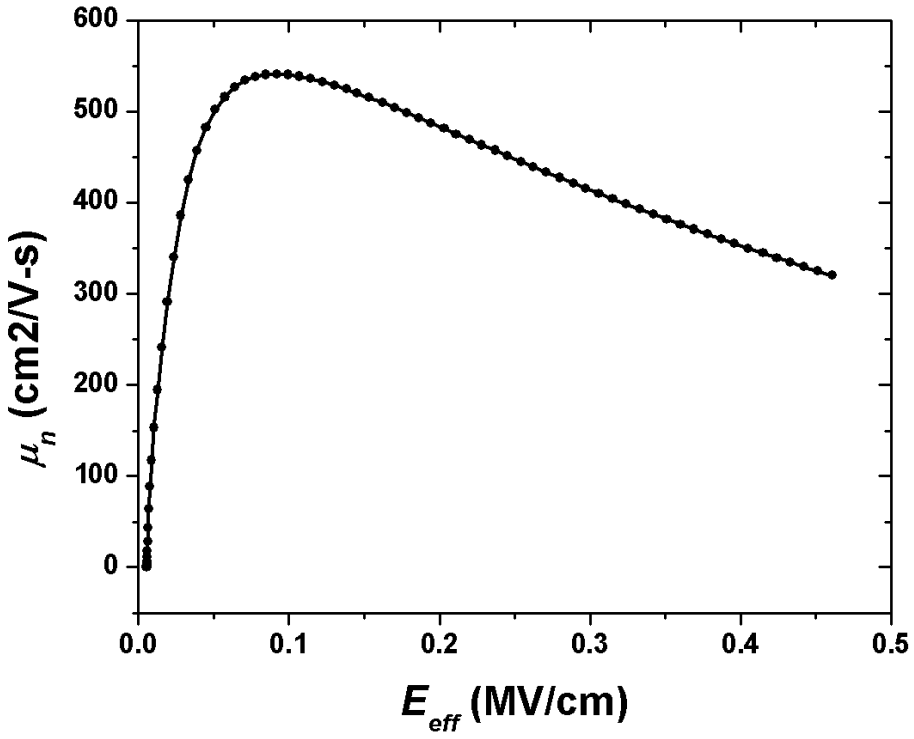

Figure IV.5: Electron mobility versus effective field of a 10-μm n-channel FinFET from measurement.

The conventional universal mobility model, widely adopted in most of commercial compact models, is empirically expressed as

$$\mu_{eff} = \frac{\mu_0}{\left(1 + \frac{E_{eff}}{E_c}\right)^{\nu}} \tag{IV.6}$$

where E_{eff} is the effective vertical electric field, E_c is the critical electric field, μ_0 and ν are empirical parameters. Eq. (IV.6) well describes the mobility degradation in the high field regime due to the phonon scattering mechanism.

However, the degradation in the low field regime due to the Coulomb scattering is not captured by Eq. (IV.6). Although the body of the experimental DG FinFET is undoped, certain Coulomb scattering centers are present due to vacan-

cies, interstitial atoms, or dangling bonds at the surface. The absence of the low field degradation is absorbed by shifting threshold voltage and adjusting the high field mobility. The obtained mobility model with a phonon scattering term only, therefore, does not give a physically correct picture.

An additional term to take Coulomb scattering into account is necessary. A modified universal mobility model with both a phonon scattering and a Coulomb scattering term is proposed by Mathiesen's rule.

$$\begin{aligned}\frac{1}{\mu_{eff}} &= \frac{1}{\mu_{eff}^{Coulomb}} + \frac{1}{\mu_{eff}^{phonon}} \\ &= \frac{1}{\mu_0^{Coulomb}\left(1+\frac{E_{eff}}{E_c^{Coulomb}}\right)^{\nu^{Coulomb}}} + \frac{1}{\frac{\mu_0^{phonon}}{\left(1+\frac{E_{eff}}{E_c^{phonon}}\right)^{\nu^{phonon}}}}\end{aligned} \tag{IV.7}$$

where the superscripts phonon and Coulomb designate the phonon scattering and the Coulomb scattering, respectively. The proposed mobility model is versatile enough to describe both the low and high field degradations.

In Eg. (IV.7), 6 empirical parameters determine the effective mobility, μ_{eff}. Similar to the calibration of the gate capacitance, two different methods are available to extract the effective mobility: comparing the ratio or the difference of the model and the experimental data. However, different from the $C_g - V_{gs}$ calibration, there are two distinctive regions in the drain current as a function of the gate voltage, namely, the subthreshold region and the strong inversion region. If the difference between the model and the experimental data only is in consideration, a relatively large error in the subthreshold region is unavoidable. On the contrary, minimizing the standard deviation of the ratio will produce relatively large error in the strong inversion region. In order to achieve a well-matched curve in both regions, one needs to apply each method separately to appropriate regions. *Shift-and-Ratio* method is applied to the subthreshold region, and the difference is minimized in the strong inversion region.

The electron mobility extracted from Eq. (II.28) is presented in Fig. Figure

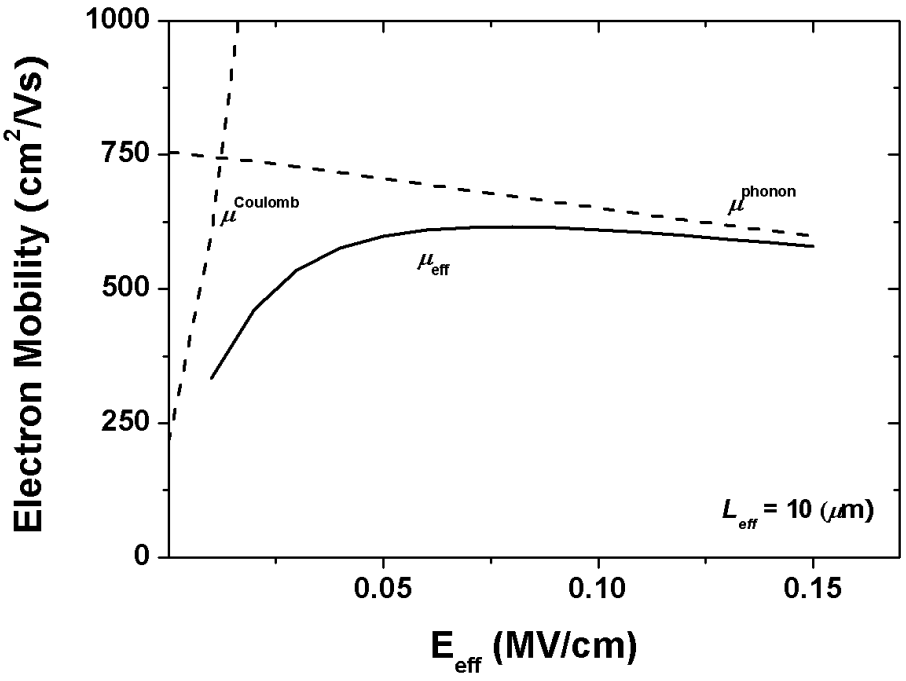

Figure IV.6: Electron mobility versus effective field of a 10-μm n-channel FinFET from Eq. (II.28). The solid line is for the extracted mobility, μ_{eff}, and the dashed lines are for the Coulomb and phonon scattering term.

IV.6:. The curve well describes the degradation in the low and high field regime in the measured raw mobility in Fig. Figure IV.5:. The long-channel mobility parameters of the n-channel FinFET are given in Table Table IV.2:. Widely employed universal mobility model is simple but cannot take into account Coulomb scattering. Unphysical threshold voltage adjustment is required for the universal mobility model, leading to inconsistent threshold voltages of the gate capacitance and the drain currents. The mobility model of Eq. (IV.7) has both a Coulomb and a phonon scattering terms. They correspond to the dashed lines in Fig. Figure IV.6:. The dashed line which degrades in the low field regime presents Coulomb scattering effects by impurities or surface states. Coulomb scattering is dominant

Table IV.2: Mobility parameters of n-channel FinFETs.

Parameter	Unit	Values
μ_{eff}^{phonon}	$cm^2/V{\cdot}s$	755
E_{eff}^{phonon}	kV/cm	460
ν_{phonon}	-	1.2
$\mu_{eff}^{Coulomb}$	$cm^2/V{\cdot}s$	213
$E_{eff}^{Coulomb}$	kV/cm	65
$\nu_{Coulomb}$	-	1.4

in the low electric field regime; after the inversion layer is formed, the impurities and the Coulombic traps are screened by the heavily induced electrons. The other dashed line accounts for phonon scattering effects in the high field regime; as the electron energy increases phonon scattering mechanism becomes significant, because the number of electrons with sufficiently high energy for phonon interaction increases exponentially.

The slight difference from the raw electron mobility and the extracted mobility is due to the error of the $C_g - V_{gs}$ calibration. Because the mobility describes the relation between gate capacitance and drain currents by Eq. (III.1), the error introduced by the gate capacitance integrates in the mobility. Therefore, the mobility suffers relatively larger error even with very small errors from $C_g - V_{gs}$. However, in the final circuit simulation, mobility is not a final output characteristics; actually mobility can absorb various non-ideality effects from $C_g - V_{gs}$ data.

IV.B.2 Drain current of long-channel n-channel FinFET

The drain current versus the gate voltage at low drain bias ($V_{ds} = 50$mV) with the modified universal mobility is presented in Fig. Figure IV.7:. The model and experimental values give an excellent agreement with errors within 3% for all gate bias regimes. All geometric parameters are identical to the those of $C_g - V_{gs}$

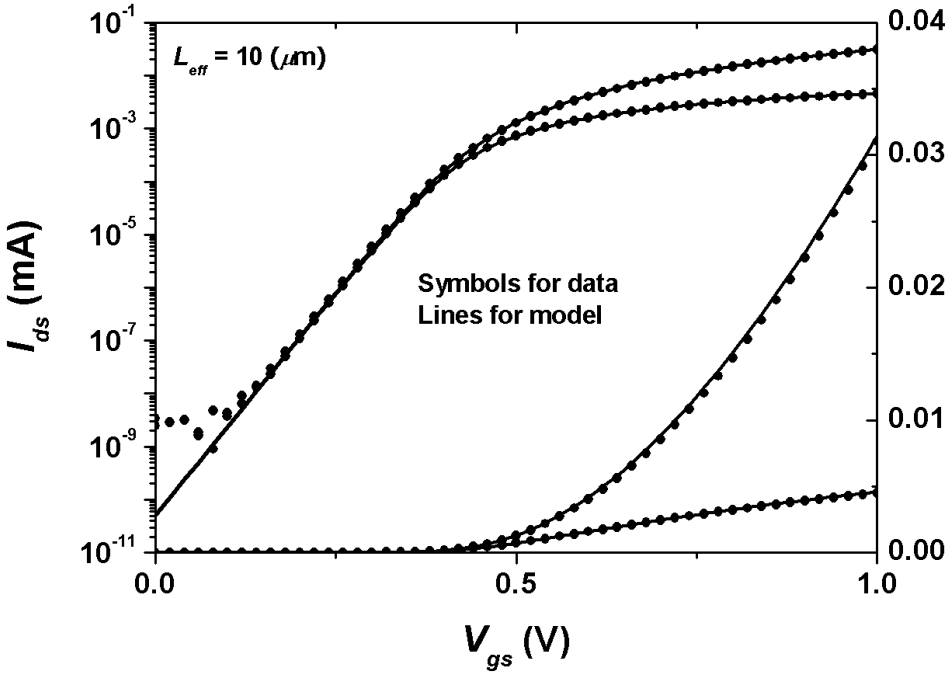

Figure IV.7: Drain current versus gate voltage of a 10-μm n-channel FinFET with modified universal mobility model with the low (V_{ds} = 50mV) and high drain voltages (V_{ds} = 1V).

calibration. The core model incorporated with quantum mechanical effects and the applied mobility model successfully describe the drain current of the long-channel FinFETs. The ideal 60 mV/dec. of subthreshold current slope is generated by the experimental data and well-captured by the analytic potential model. The degradation of the transconductance g_m is observed at high gate overdrives. This is due to the mobility degradation due to phonon scattering.

Although $I_{ds} - V_{gs}$ data of 10-μm at high drain bias is also presented in Fig. Figure IV.7:, compact modeling of high-field effects is to be discussed in later sections. While high-field effects play a role with high drain bias, long-channel devices are not greatly affected by high-field effects thus not suitable for parameter

extraction. High-field effects are extracted medium- and short-channel devices, and reversely applied to the long-channel device to minimize possible errors from various non-ideal effects introduced during measurements.

In summary, the long-channel mobility and drain current at low drain bias are modeled. The modified universal mobility model is suitable for modeling the electron mobility degraded in the low and the high field regimes. The extracted mobility and drain current agree with the measurement with high accuracy.

IV.C Compact modeling of medium-channel n-channel FinFETs

The long channel device with the gate length of 10 μm can be approximated to ideal device under low drain biases. Not only the short-channel effects, but also source-drain series resistance effects are negligible. As discussed in Chapter Chapter I, the short-channel effects are not significant until the gate length is close to the scale length. Considering the device structure in Chapter Chapter III, the scale length of the experimental FinFETs are calculated to be about 45 nm. The short-channel effects, therefore, can be safely ignored in the devices longer than 0.25 μm. However, the source-drain series resistance effects are observable before reaching the scale length, as the gate length shrinks. A medium-channel device is defined as the device with no short-channel effects, but with non-negligible series resistance effects. The FinFETs with the gate length from 5 μm to 0.25 μm can be categorized as medium-channel devices. In this section, compact modeling of the medium-channel devices are discussed.

To model the characteristics, e.g., mobility, of the intrinsic devices, the separation of the source-drain series resistance effects is necessary. Well-known *Shift-and-Ratio* method is employed. After removing the source-drain series resistance effects, the same procedure as the long-channel device is applicable to the

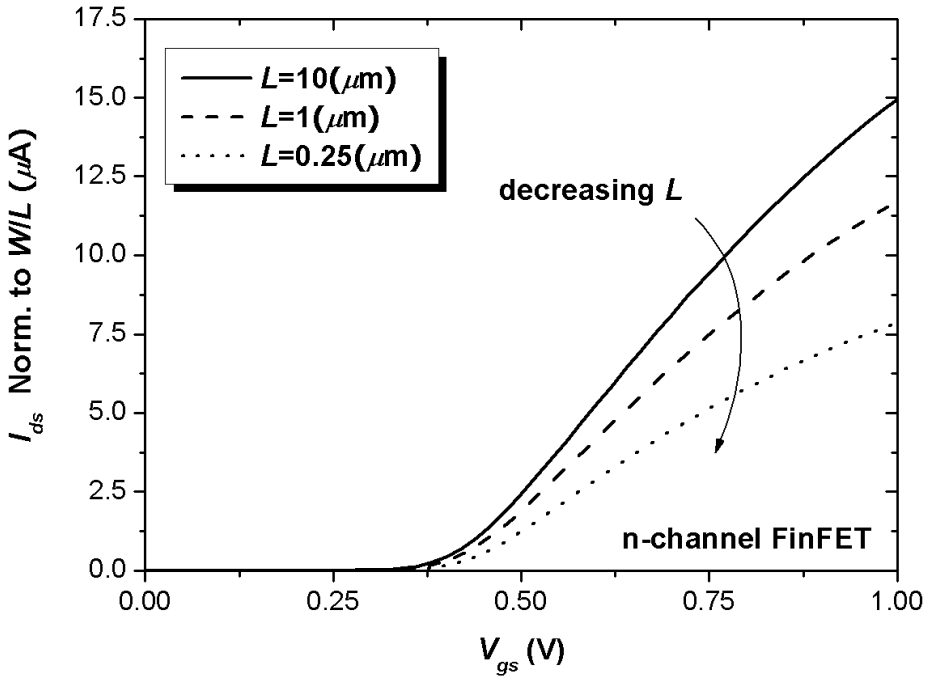

Figure IV.8: Normalized drain currents versus gate voltage of 10-μm, 1-μm, and 0.25-μm n-channel FinFETs. The drain currents are normalized by W/L.

extracted intrinsic devices. In fact, the long-channel FinFET has been approximated to be intrinsic without separating out the source-drain series resistances. The extracted mobility trend from the $I_{ds} - V_{gs}$ at the low drain bias is discussed with physical explanation.

IV.C.1 Normalized drain current trend of n-channel FinFETs

Comparing normalized current trend of a series of devices is a good way to observe non-ideal effects in the low field regime. The normalized current trend of n-channel FinFETs in Fig. Figure IV.8: degrades as the gate length L decreases. The

trend suggests the existence of non-negligible source and drain series resistances. Since the channel resistance decreases linearly proportional to the gate length, the effect of the parasitic resistance increases.

It is an attractive and immediate idea to lump the drain current degradation towards the shorter devices into the parasitic resistance effects. This approach has fully proved its validity in the compact modeling of such devices. However, it is possible that the parasitic resistance are not the only source of the degradation. Also, in general, the additional effects may even change the drain current trend radically. Therefore, one needs to understand the nature of source-drain series resistances, and separate out their effects in a physically-sound way.

IV.C.2 Source-drain series resistance

Fig. Figure IV.9: illustrates an equivalent circuit with source-drain series resistance [70]. A source resistance R_s and a drain resistance R_d are assumed to connect an intrinsic MOSFET to the external terminals where voltages V_{ds} and V_{gs} are applied. The internal voltages are V'_{ds} and V'_{gs} for the intrinsic MOSFET. As depicted in the figure, the series resistances degrade the gate and drain voltages hence the drain currents. The source series resistance R_s is more troublesome, because it degrades the gate drive as well.

In general, the source and drain series resistance effects are expressed by the following relations:

$$V'_{ds} = V_{ds} - (R_s + R_d)I_{ds} \tag{IV.8}$$

and

$$V'_{gs} = V_{gs} - R_s I_{ds} \tag{IV.9}$$

With associating the drain current expression for DG MOSFETs, Eq. (II.28), V'_{ds}, V'_{gs}, and I'_{ds} can be calculated. Three coupling equations are implicit in nature. Although several explicit expressions for the drain current with the source-drain

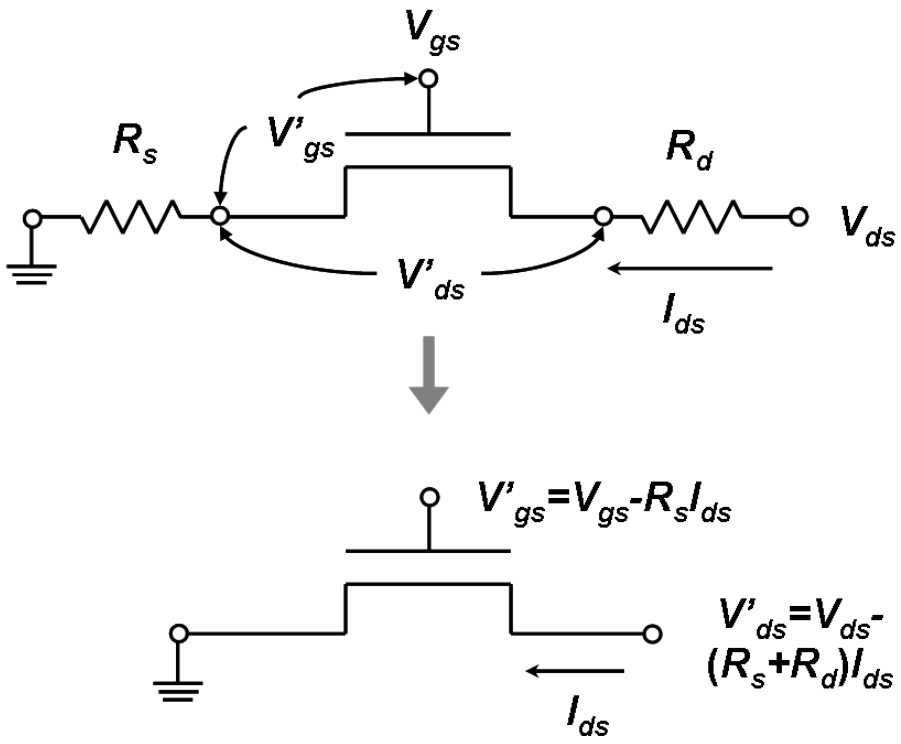

Figure IV.9: Equivalent circuit of a DG MOSFET with source and drain series resistance. The intrinsic part of the top circuit is equivalent to the bottom circuit with redefined terminal voltages (Adopted from [70]).

resistance effects were developed by first- or second-order approximations, no complete analytic solution exists for the equations.

With redefined voltage symbols, the channel resistance and the total resistance are given by

$$R_{ch} \equiv \frac{V'_{ds}}{I_{ds}} = \frac{L}{\mu_{eff} C_{ox} W (V'_{gs} - V_t)}. \tag{IV.10}$$

and

$$R_{tot} \equiv \frac{V_{ds}}{I_{ds}} = R_{sd} + R_{ch} = R_{sd} + \frac{L}{\mu_{eff} C_{ox} W (V'_{gs} - V_t)}. \tag{IV.11}$$

where R_{sd} is the total source-drain parasitic resistance, and $R_s = R_d = R_{sd}/2$.

The source and drain series resistances R_s and R_d are, in general, weak functions of the gate over drive. The source and drain resistances consist of overall 4 components as illustrated in Fig. Figure IV.10: [71]. R_{ac} is the accumulation-

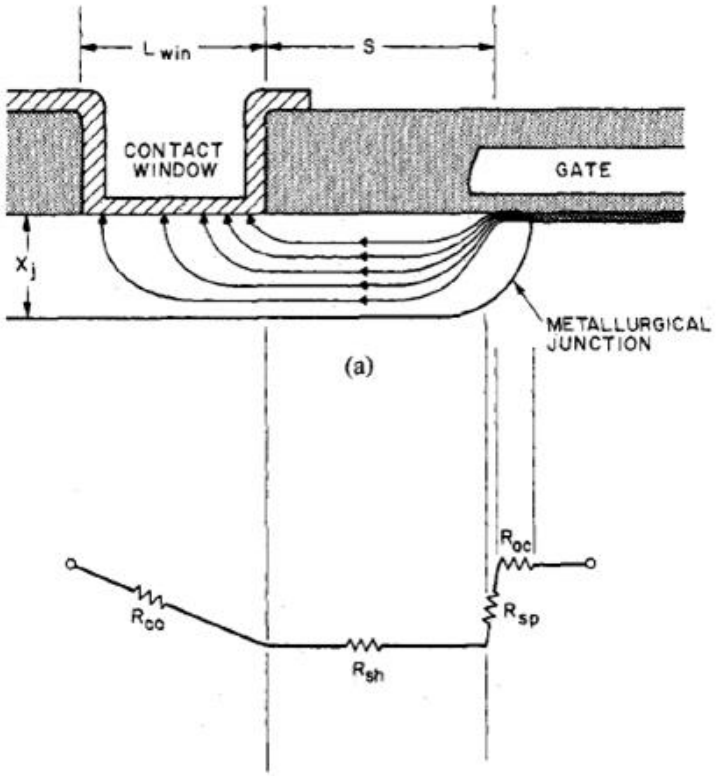

Figure IV.10: A schematic cross-section showing the pattern of current flow from a MOSFET channel through the source or drain region to the aluminum contact the aluminum contact. The diagram below identifies various contributions to the series resistance. The device width in the z-direction is assumed to be W (Adopted from [71]).

layer resistance, R_{sp} the spreading resistance, R_{sh} the sheet resistance, and R_{co} the contact resistance. It is worth nothing that R_{ac} has dependence on the gate drive. The accumulation-layer resistance term introduces a weak dependence of gate bias to the source or drain series resistances. Since the channel resistance is a strong function of the gate drive, all three terms of Eq. (IV.11) are gate bias dependent.

It is clear from Eq. (IV.11) that the channel resistance decreases linearly proportional to the gate length, whereas the parasitic resistances scale down. On the contrary, the short-channel effects are exponentially dependent on the gate length. Therefore, the series resistance effects are observable in medium length

devices which do not suffer from the short-channel effects. To model the intrinsic characteristics of the FinFETs, separation of the series resistance effects is necessary.

IV.C.3 Shift-and-Ratio method for separation of series resistance effects

The *Shift-and-Ratio* method, briefly introduced in the previous section, is also a powerful tool to separate out the series resistance effects. The original *Shift-and-Ratio* method was first developed to determine the effective channel length of a short-channel device when the drain currents data of two or more devices are available with an identical mobility throughout the same process. The idea of *Shift-and-Ratio* method is to minimize the standard deviation of the ratio of two different data sets, when the data have a relation of constant multiplication.

If the gate drive dependence of the parasitic resistances can be approximated to be negligible, one can immediately remove R_{sd} term in Eq. (IV.11) by differentiating it with respect to the gate voltage. Eq. (IV.11) can be rewritten for two devices with different gate lengths as

$$R^0_{tot} = R^0_{sd} + \frac{L^0/W}{\mu^0(V_{gs})C_{ox}(V_{gs} - V_t)} \tag{IV.12}$$

and

$$R^i_{tot} = R^i_{sd} + \frac{L^i/W}{\mu^i(V_{gs})C_{ox}(V_{gs} - V_t)} \tag{IV.13}$$

where the superscript 0 denotes a 10-μm (L^0) device with mobility μ^0 and series resistance R^0_{sd}, and i denotes the i^{th} device with gate length L^i, mobility μ^i and series resistance R^i_{sd}.

By taking the derivatives of IV.12 and IV.13, the series resistance terms are removed. The assumption of negligible gate voltage dependence of the series resistance is justified in later discussion. The derivatives of the total resistance is

expressed as

$$S^0 \equiv \frac{dR^0_{tot}}{dV_{gs}} = \frac{L^0}{WC_{ox}}\frac{df^0}{dV_{gs}} \tag{IV.14}$$

and

$$S^i \equiv \frac{dR^i_{tot}}{dV_{gs}} = \frac{L^i}{WC_{ox}}\frac{df^i}{dV_{gs}} \tag{IV.15}$$

where f^0 and f^i are defined by

$$f^0 \equiv \frac{1}{\mu^0(V_{gs} - V_t)} \tag{IV.16}$$

and

$$f^i \equiv \frac{1}{\mu^i(V_{gs} - V_t)}. \tag{IV.17}$$

A coefficient to represent the normalized ratio of the derivatives of the total resistance then can be introduced for the sake of convenience

$$\kappa^i \equiv \frac{L^i}{L^0}\frac{S^0}{S^i}. \tag{IV.18}$$

For two devices fabricated by an identical process, κ^i is the unity. However, for the experimental hardware, the coefficient may deviate from the unity. In Eq. (IV.14) and Eq. (IV.15), L^0 and L^i are known parameters in sufficiently long devices, because the difference between the effective channel length and the actual gate length is negligible; W, C_{ox} are common to both devices; gate overdrive $V_{gs} - V_t$ are also identical when the short-channel effects are not excessive. Therefore, any deviation from the unity can be attributed to the only uncommon parameters μ_0 and μ_i.

By substituting the result back to the Eq. (IV.12) or Eq. (IV.13), the value of the series resistances can be obtained as

$$R_{sd} = \frac{\kappa^i R^i_{tot}(V_{gs}) - R^0_{tot}(V_{gs})}{\kappa^i - 1} \tag{IV.19}$$

The degradation of the drain currents by the extracted series resistance can be calculated by solving 3 coupling equations mentioned above, namely, Eq. (IV.8), Eq. (IV.9), and Eq. (II.28).

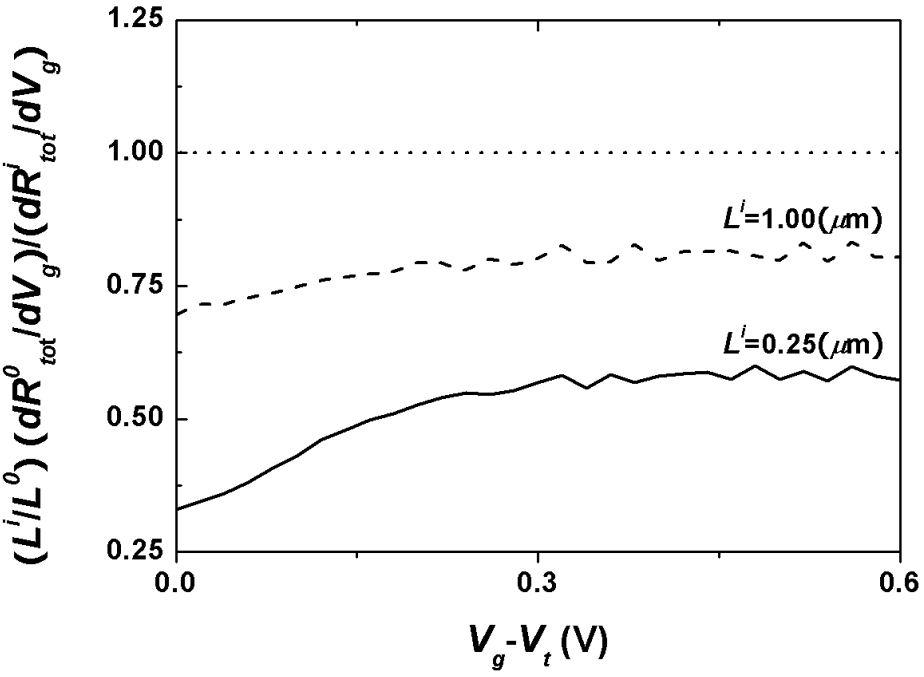

Figure IV.11: The normalized ratios of the derivatives of the total resistances κ^i versus the gate overdrive of selected n-channel FinFETs. The dashed line indicates the ratio of the unity. L^0 is 10 μm for both devices.

IV.C.4 Mobility and drain currents of medium-channel n-channel FinFETs

The normalized ratios of the derivatives of the total resistances κ^i of 1-μm and 0.25-μm n-channel FinFETs are presented in the Fig. Figure IV.11: . In both cases, κ^i reach plateaus at high gate over drives. As discussed in a previous section, the constant values at high gate overdrive region indicate the mobility change of shorter devices from the 10-μm device. While the dashed, unity line indicates no change of mobility, κ^i smaller than the unity means the degradation of the electron mobility. Because the gate length of 0.25-μm is much longer than the difference of the effective channel length and the drawn gate length ΔL_{eff}, deviation of κ^i

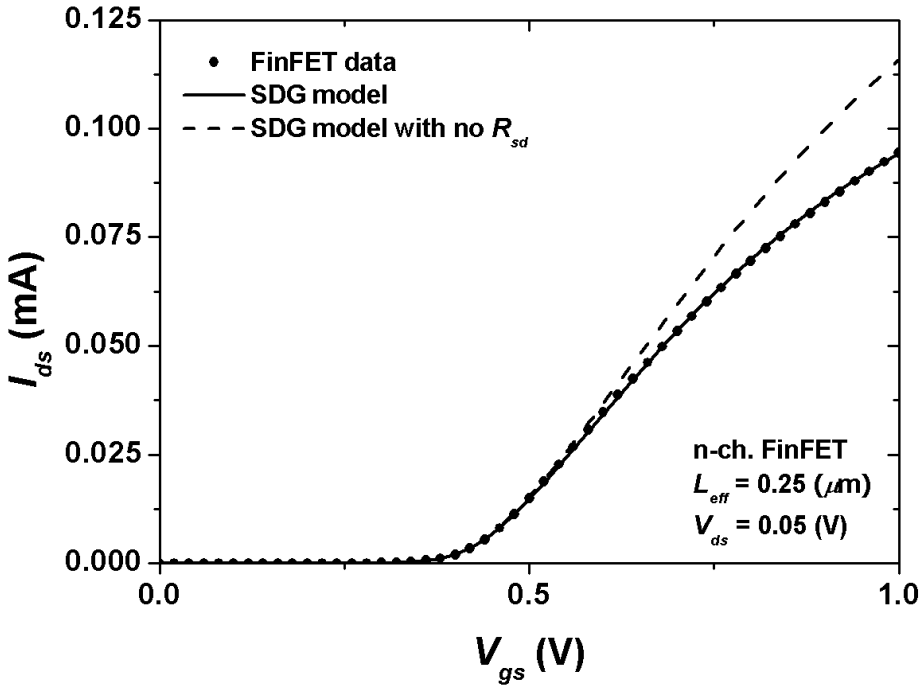

Figure IV.12: Drain currents versus gate voltage for the experimental data and SDG model of 0.25-μm n-channel FinFET at low drain bias ($V_{ds} = 0.05$V). Symbol is for the experimental data, solid line for model with source-drain series resistance, and dashed line for model without source-drain series resistance.

from the unity is solely attributed to the change of the mobility.

By substituting the extracted κ^i into IV.19, the source-drain series resistance of the n-channel FinFETs is calculated to be 170 $\Omega \cdot \mu$m. The values are comparable to modern semiconductor fabrication process. With 3 coupling equations and the extracted R_{sd}, it is possible to model the drain currents. The drain currents are presented in Fig. Figure IV.12:. It is clear from the figure that the series resistance effects are already significant in the gate length of 0.25 μm. The drain current data of intrinsic device, i.e., without source-drain series resistance, are necessary to model the intrinsic mobility of the devices. Once the intrinsic drain

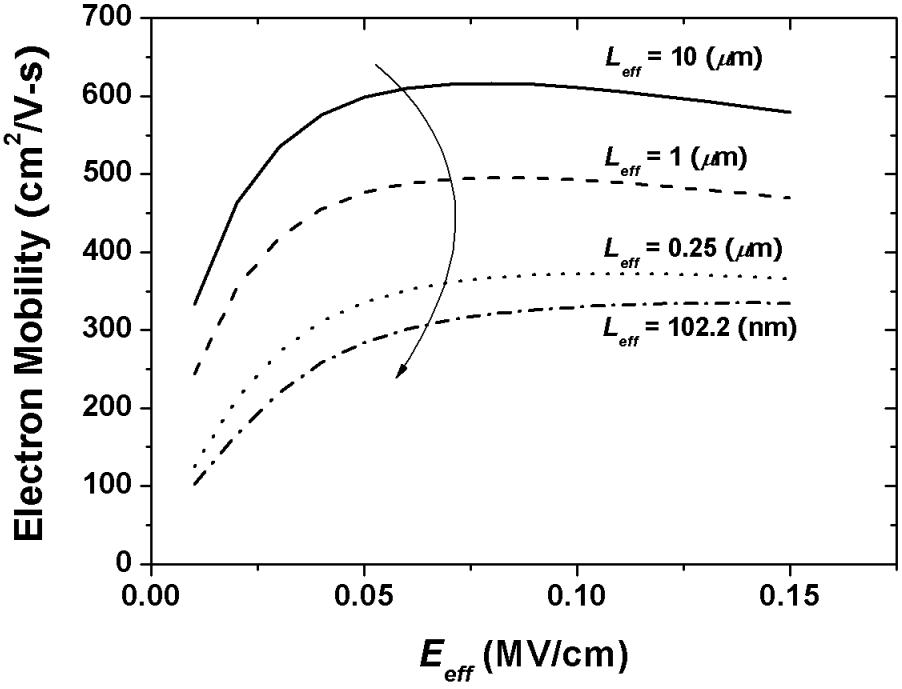

Figure IV.13: Mobilities of 10-μm, 1-μm, and 0.25-μm n-channel FinFETs.

currents at the low drain bias (V_{ds} = 0.05V) are obtained, the same approach in the long-channel FinFET can be applied. The extracted intrinsic mobilities of 10-μm, 1-μm, and 0.25-μm n-channel FinFETs are shown in Fig. Figure IV.13:.

As expected from Fig. Figure IV.11:, the mobility degrades toward shorter devices. The mobility trend can be explained by the reduced tensile strain. As mentioned in Chapter Chapter III, the TiSiN gate introduces tensile strain to the channel region. Many literatures report the tensile strain enhances electron mobility in $\langle 110 \rangle$-channel orientation on (100)-surface as in Fig. Figure IV.14: [72]. The reported electron mobility in Fig. Figure IV.14: for (110)/$\langle 110 \rangle$ surface/channel orientation is comparable to the raw electron mobility and the extracted mobility.

To measure and analyze process-induced strain is extremely difficult. A number of mobility model with strain effects have been proposed and validated

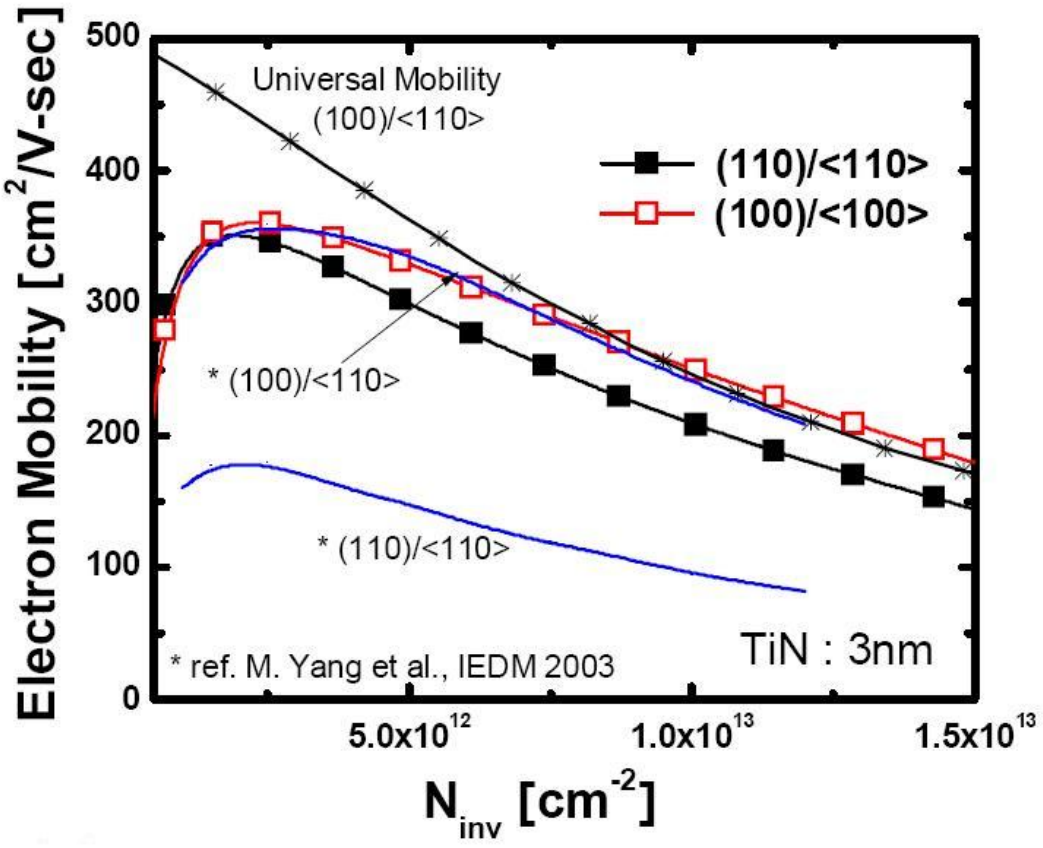

Figure IV.14: Electron mobility versus inversion charge for (110)/⟨110⟩ and (100)/⟨100⟩ surface/channel orientation (Adopted from [67]).

by numerical simulations and experimental data. They are based on the electron band structure warping and the following change of effective mass and electron re-population of each valley of the silicon [73]. It has been known that the electron mobility is enhanced with tensile strain in the silicon. The physical reasons behind the mobility enhancement, however, depends on the surface and channel orientations.

The mobility enhancement in ⟨110⟩-oriented channel on (110)-oriented surface by tensile strain results from the warped band structure and following electron re-population to the lower energy band with lighter electron mass. Fig. Figure IV.15: shows the warped band structure and the effective masses of each valleys.

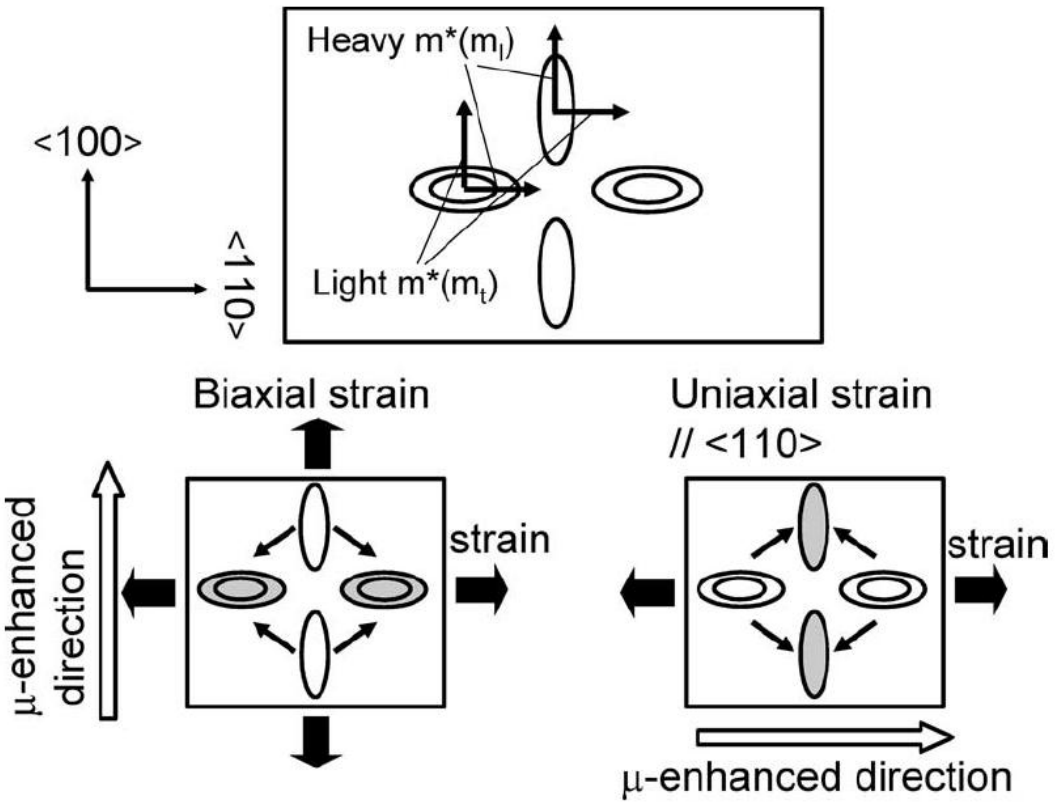

Figure IV.15: Equivalent valleys of the silicon for inversion-layer electrons on (110) surface with and without strain (Adopted from [73]).

A numerical simulation with strain-dependent effective mass is shown in Fig. Figure IV.16:. The figure confirms that tensile strain enhances the electron mobility along the channel direction $\mu_{||}$ in (110)/$\langle 110 \rangle$ surface/channel orientation. Other numerical simulations give similar trend.

However, the tensile strain induced by the gate metal is believed to be relaxed in shorter gate lengths, thereby the drain current enhancement is not observed due to the mobility degradation. The degradation of electron mobility in shorter gate lengths has been reported by several researches. The drain currents versus gate voltage at the low drain bias of selected medium-channel n-channel FinFETs are obtained with the extracted mobility. The calibrated $I_{ds} - V_{gs}$ data are shown in Fig. Figure IV.17:. Because the medium-channel FinFETs are still

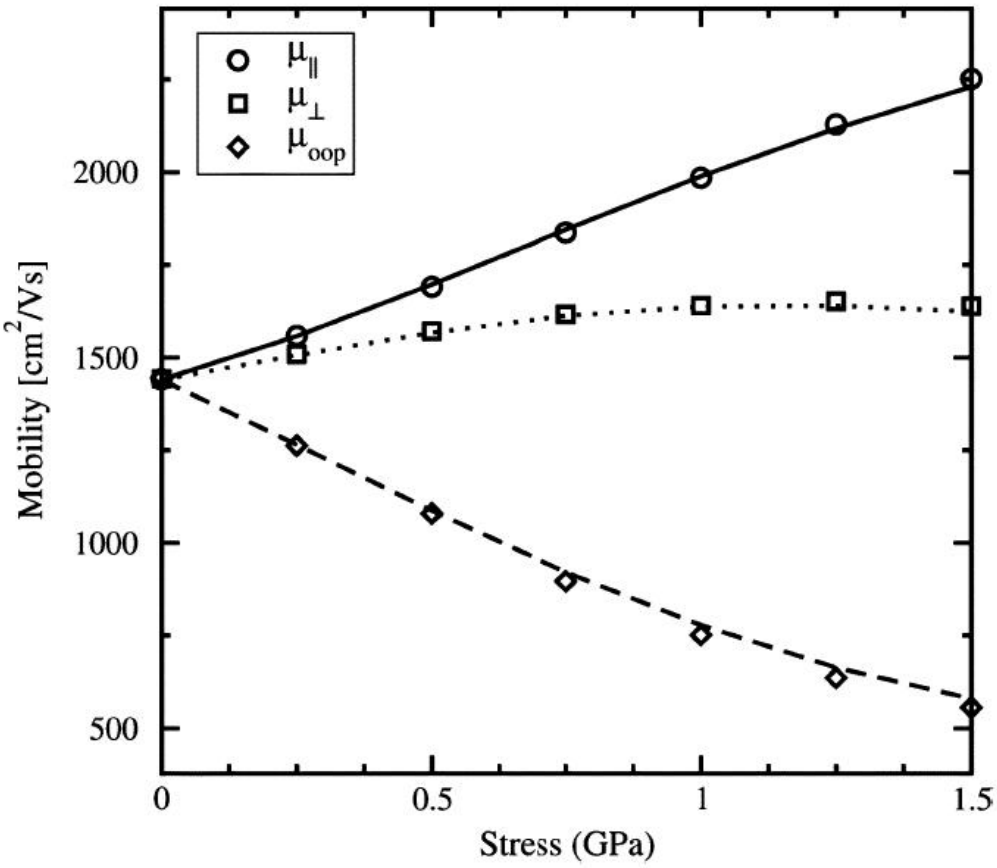

Figure IV.16: Equivalent valleys of the silicon for inversion-layer electrons on (110) surface with and without strain (Adopted from [72]).

free from the short-channel effects, the ideal 60 mV/dec. of subthreshold current slope is achieved for both devices. With high gate overdrives, degradation of transconductance g_m is observed. The drain current does not increase linearly proportional to $1/L$ because the parasitic resistance effects in addition to the mobility degradation due to the relaxed tensile strain. In other words, the normalized drain current degrades towards shorter gate lengths.

Although the drain currents with high drain bias are given in Figure IV.17:, it requires to model high field effects. The compact modeling of high field effects for the medium-channel n-channel FinFETs are given in the later subsection.

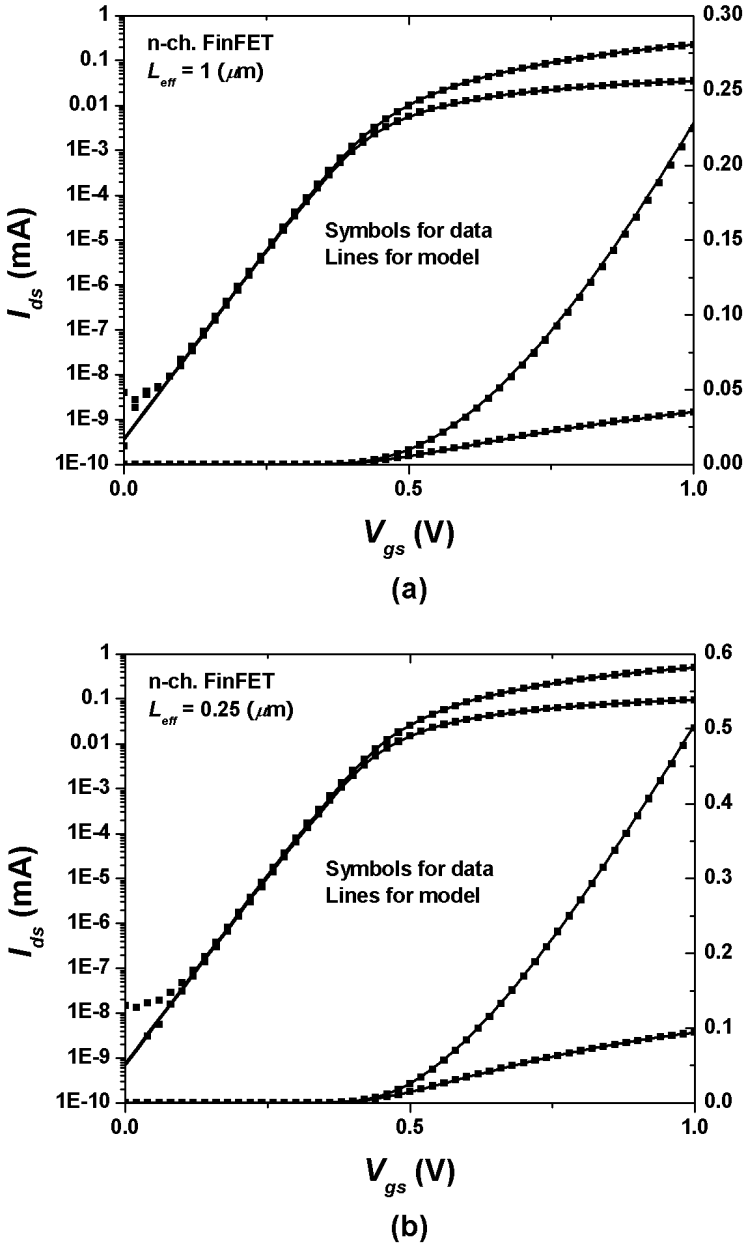

Figure IV.17: Drain currents versus gate voltage of (a) 1-μm and (b) 0.25-μm n-channel FinFETs at low ($V_{ds} = 0.5$mV) and high drain voltages ($V_{ds} = 1.0$V).

IV.C.5 High-field effects of medium-channel n-channel FinFETs

In order to model $I_{ds}-V_{ds}$ data at high drain bias ($V_{dd} = 1.0$V), the inclusion of high field effects is necessary. The 0.25-μm device, the shortest device among

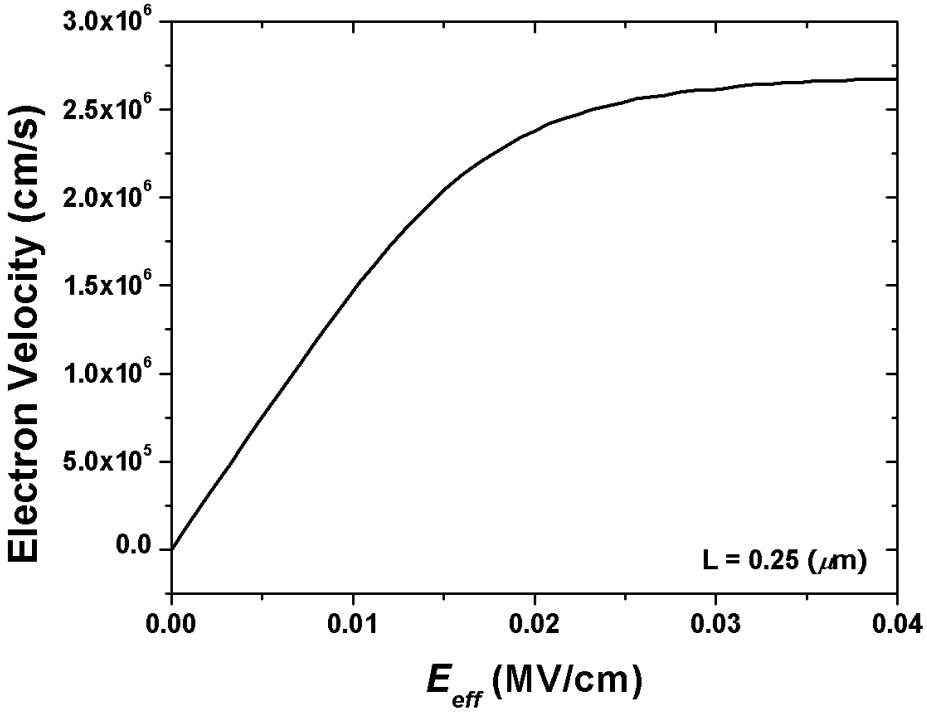

Figure IV.18: Electron velocity versus effective lateral field in long- and medium-channel n-channel FinFETs. Saturation velocity of electron is 2.67×10^6 cm/s.

the medium-channel FinFETs, is desirable to model the high-field effects. If the constant voltage scaling scheme is applied, shorter devices have higher electric-field, hence the stronger high-field effects. Therefore, the shorter device gives the smaller modeling error.

First, the channel length modulation is modeled by the slope of $I_{ds} - V_{ds}$ data, i.e., g_{ds}, in the saturation region based on Eq. (II.50). With the extracted channel length modulation, saturation velocity is modeled to give accurate on-current. The extracted carrier velocity is given in Fig. Figure IV.18:. The extracted saturation velocity is smaller than those of modern bulk CMOS devices, presumably due to the different surface and the channel orientation. The veloc-

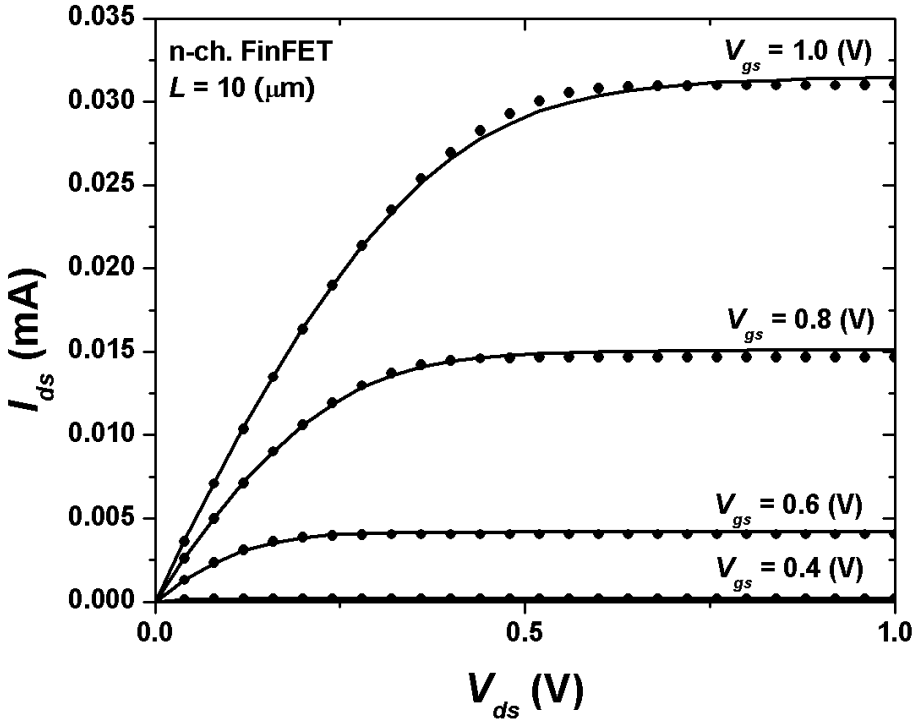

Figure IV.19: Drain current versus drain voltage of 10-μm n-channel FinFET. Symbols are for the experimental data, and the lines are for the model.

ity saturation effects in the experimental devices affects the device characteristics significantly.

The extracted model parameter from 0.25-μm device is also applied to the other medium-channel and long-channel, n-channel FinFETs. The $I_{ds} - V_{ds}$ plots of the experimental and model data of long- and medium-channel FinFETs are presented in Fig. Figure IV.19: and Fig. Figure IV.20: respectively. The channel length modulation and the on-current limited by the velocity saturation effects are well-modeled. The experimental FinFETs does not suffer from excessive channel length modulation, due to the superior gate-controllability over the channel region.

In summary, the medium-channel devices are defined as the devices with

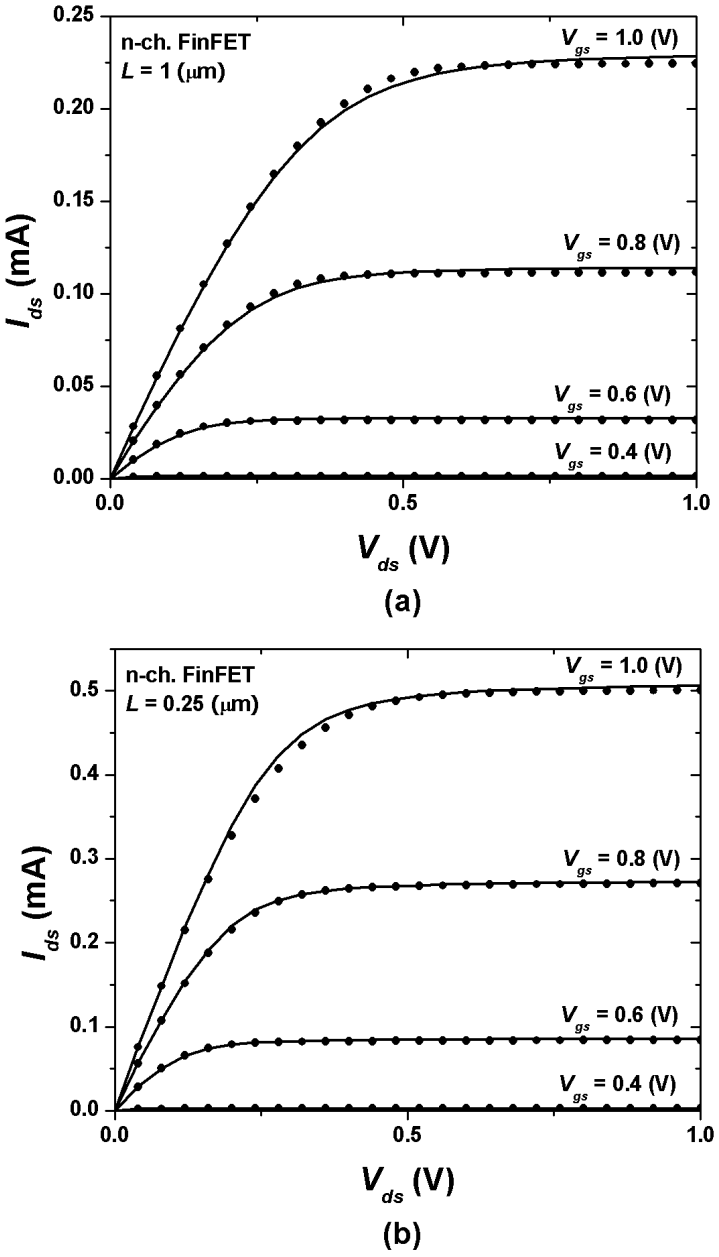

Figure IV.20: Drain current versus drain voltage of (a) 1-μm n-channel FinFET and (b) 0.25-μm n-channel FinFET. Symbols are for the experimental data, and the lines are for the model.

the source-drain series resistance effects, but without the short-channel effects. The drain currents versus gate voltage and drain voltage of medium channel, n-

channel FinFETs are adequately modeled by employing the same unified mobility model in the compact modeling of the long-channel FinFET. The intrinsic electron mobility after the separation of the parasitic resistance effects degrades towards shorter devices. The trend is explained by the reduced tensile strain in the shorter devices. An adequate inclusion of high-field effects well describes the drain current behavior at high drain voltage.

IV.D Compact modeling of short-channel n-channel FinFETs

When the gate length of a MOSFET shrinks close to 2 or 3 times larger than its scale length, short-channel effects must be taken into account. The short-channel effects are due to the excessive lateral field penetration from the drain, including drain-induced barrier lowering (DIBL), threshold voltage roll-off, and subthreshold current slope degradation. The compact model for the short-channel effects of DG MOSFETs by solving 2-D analytical potential is described in Chapter Chapter II in detail.

In this subsection, devices with the sub-100 nm gate lengths are modeled with the inclusion of short-channel effects based on 2-D analytic potential solution. The gate lengths are very short, therefore the difference between the electrically-defined effective channel length and the drawn gate length starts playing a significant role. The effective channel length of the short-channel devices are systematically extracted, and validated by the correct description of all three aspects of the short-channel effects.

The parasitic resistance effects become more important with small intrinsic channel resistance. The gate-length-dependent strain effects in the short-channel effects are discussed in comparison with those of the long- and medium-channel FinFETs. The high field effects in short-channel effects are also significant. The

extracted $I_{ds} - V_{gs}$ and $I_{ds} - V_{ds}$ plots from the core model incorporated with the above listed effects are presented, providing a graphical interpretation of the short-channel effects.

IV.D.1 Effective channel length of short-channel n-channel FinFETs

Although there are various definitions of channel length, effective channel length has been most widely adopted in compact modeling. Effective channel length L_{eff} is a measure of how much gate-controlled current a MOSFET delivers and is therefore most suitable for compact model. In most cases, effective channel length is shorter than drawn gate length by ΔL_{eff}. ΔL_{eff} is a process-dependent constant. Many physical phenomenon is responsible the difference: dopant diffusion, resolution of lithography, mask material, optical proximity correction, etc.

In long-channel MOSFETs, one can safely approximate the effective channel length as the drawn gate length, because ΔL_{eff} is negligible with very long gate lengths. As the gate length decreases, however, the difference between the effective channel length L_{eff} and the drawn gate length becomes significant. In the first order, L_{eff} increases the drain current by

$$I'_{ds} = \frac{L}{L - \Delta L_{eff}} I_{ds}. \tag{IV.20}$$

Furthermore, the short-channel effects are strongly dependent of the effective channel length. Therefore, specifying the effective channel length is crucial in the compact modeling of the short-channel devices.

In principle, any of the three aspects of the short-channel effects can be analyzed to extract L_{eff}, because all of them are strong functions of the effective channel length. However, to investigate the threshold voltage roll-off, drain currents of several well-controlled short-channel devices with the gate lengths close to the roll-off point are necessary. Although experimental data of several short-

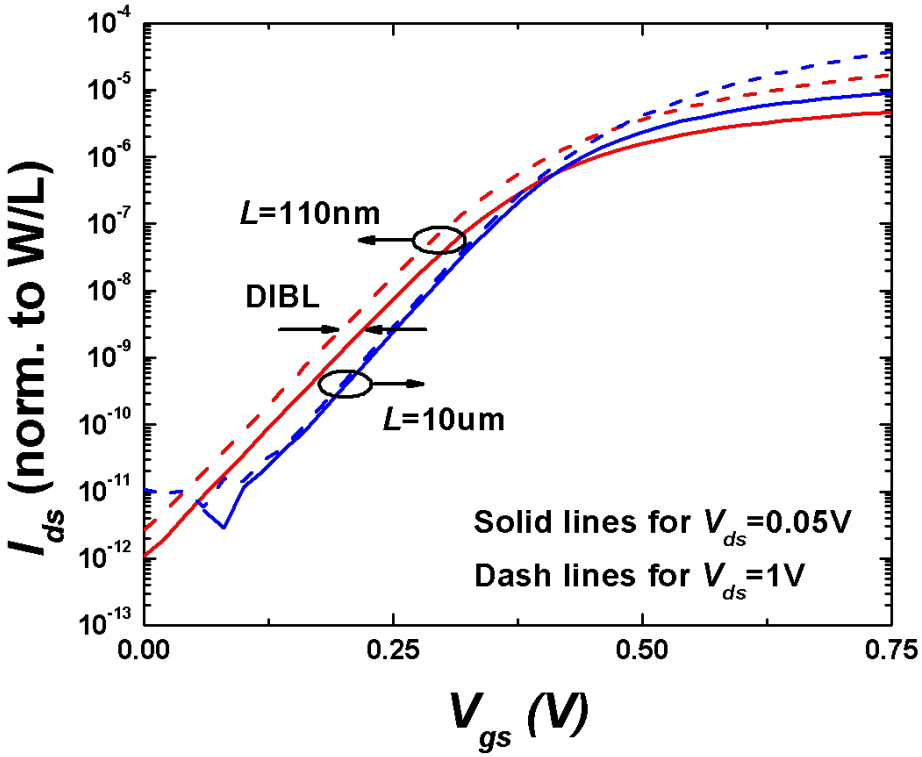

Figure IV.21: Normalized drain currents versus gate voltage at low ($V_{ds} = 0.05$mV) and high ($V_{ds} = 1.0$V) bias of 10-μm and 110-nm n-channel FinFETs. Blue lines are for the 10-μm FinFET and red lines for the 110-nm FinFET. Solid lines are for the low drain bias, and dashed lines for the high drain bias. 10 μm and 110 nm are drawn gate lengths.

channel FinFETs are available, the effective channel lengths of multiple devices have to be decided simultaneously. This introduces very large calculation load. On the contrary, DIBL can be a good parameter to extract the effective channel length, because the effective channel lengths are obtained one by one without coupling each other. Also, the measured DIBL is free from process variation, because the $I_{ds} - V_{gs}$ data of an identical device is observed.

Fig. Figure IV.21: illustrates the DIBL and the threshold voltage roll-off

Table IV.3: Nominal and effective channel length of short-channel n-channel FinFETs.

Parameter	Unit	Value		
Drawn Gate Length L	nm	110	100	95
Effective Channel Length L_{eff}	nm	102.2	89.2	85.8
ΔL_{eff}	nm	7.8	10.8	9.2

of 110-nm n-channel FinFET. The 10-μm device is also presented without any noticeable DIBL effects. The DIBL of 110-nm FinFET is clearly measurable in the subthreshold region. The threshold voltage roll-off is also observed assuming an identical gate material work-function for both devices. The work-function error bar of the gate material is negligible under an identical fabrication process. As can be observed in the figure, the subthreshold slope degradation is not very noticeable to extract the effective channel length.

In the explicit expression for DIBL of DG MOSFETs introduced in Chapter Chapter II, L_{eff} is the only unknown. The effective channel length is easily obtained by substituting extracted parameters into Eq. (II.42). The extracted L_{eff} of short-channel n-channel FinFETs are presented in Table Table IV.3:. The difference between the effective channel lengths and the drawn gate lengths are close to 9 nm for all three devices. This suggests that dopants diffuse into the channel by the same distance under an identical process. The extracted ΔL_{eff} can be used to predict the characteristics of further scaled devices with the same fabrication technology.

With the extracted parameters, the $I_{ds} - V_{gs}$ data of the short-channel n-channel FinFETs are calibrated in Figure IV.22:. The source-drain series resistances are identical to those of the long- and medium-channel devices. The mobility of the short-channel devices saturates in the short-channel devices, presumably because the relaxed tensile strain reaches its minimum value. The mobility of the short-channel devices is presented in the Fig. Figure IV.13:. It is worth noting that

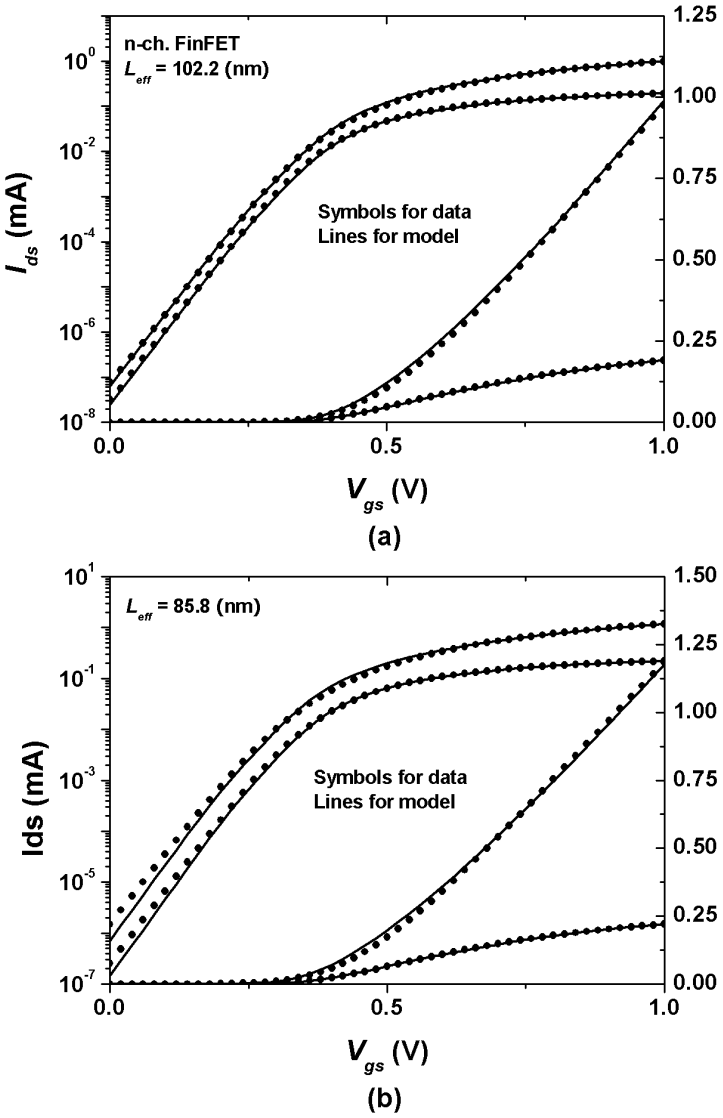

Figure IV.22: Drain currents versus gate voltage at low ($V_{ds} = 0.05$mV) and high ($V_{ds} = 1.0$V) bias of (a) 110-nm and (b) 95-nm n-channel FinFETs. Symbols are for the experimental data and the lines for the model.

the value of the extracted mobility is close to the mobility on unstrained silicon in Fig. Figure IV.14:. In other words, in the sub 100-nm region, the tensile strain induced by the TiSiN metal gate is almost fully relaxed.

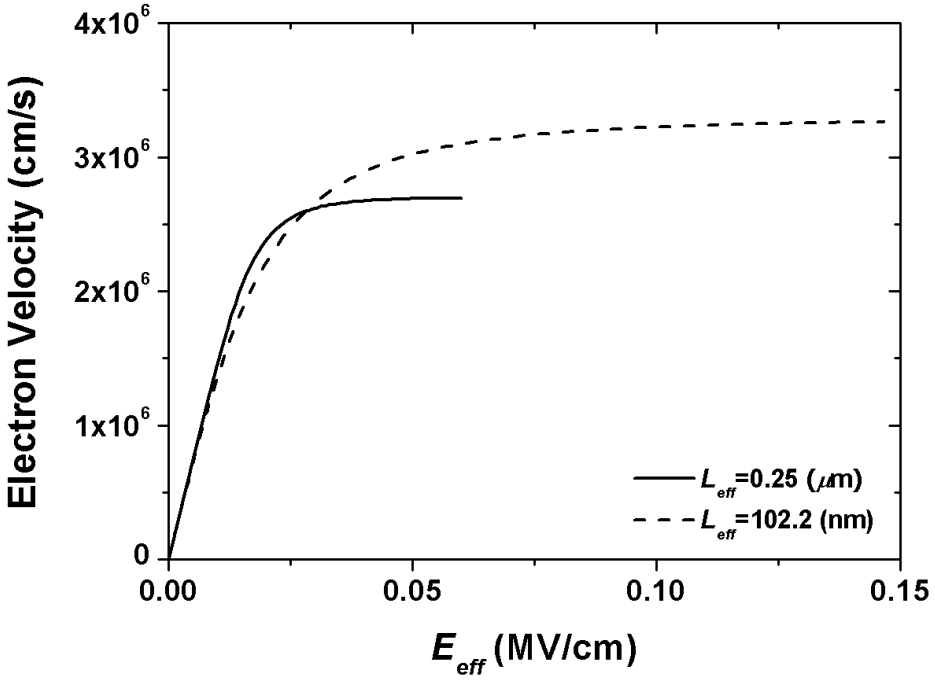

Figure IV.23: Electron velocities versus effective lateral field in 0.25-μm and 0.11-μm n-channel FinFETs.

IV.D.2 High-field effects of short-channel n-channel FinFETs

Under the constant voltage scaling, short-channel devices have larger high-field effects than long-channel devices. Therefore, an adequate compact modeling of high-field effects is of greater importance. Because of the relatively severe high-field effects, it is much easier to calibrate the model to the experimental data. The same approach as the medium-channel devices can be also applied to the short-channel devices.

The carrier velocity behaviors of the medium-channel and the short-channel devices are, however, different from each other. Fig. Figure IV.24: shows that

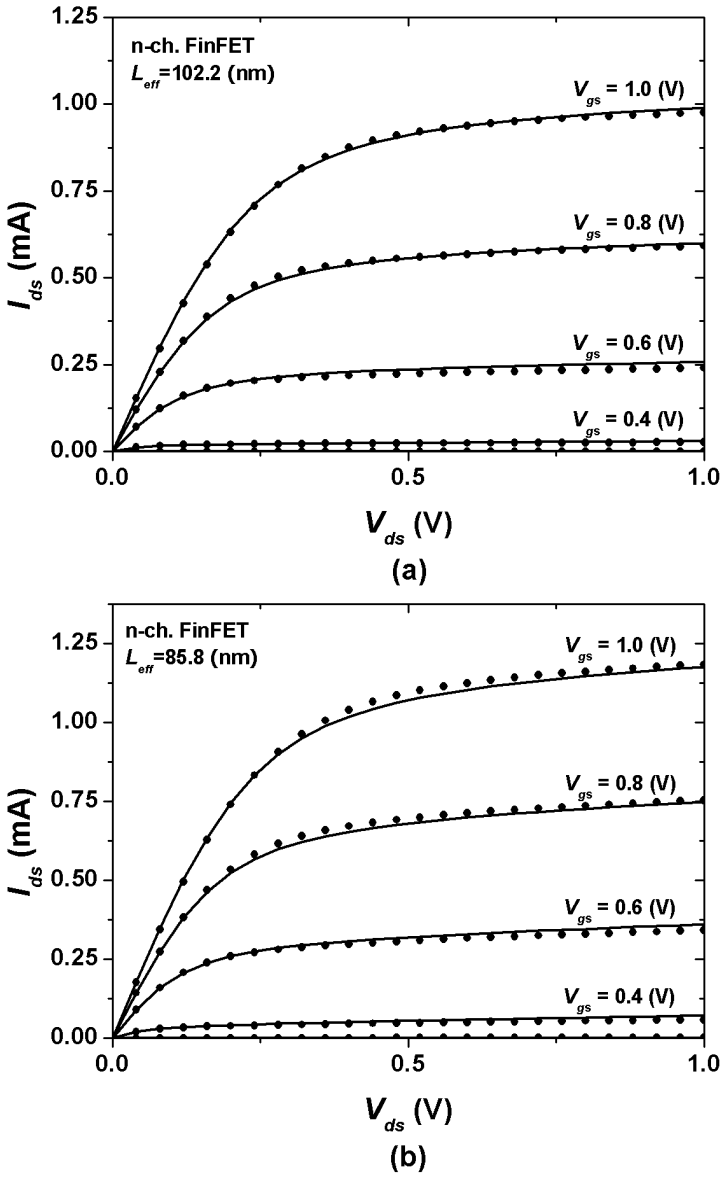

Figure IV.24: Drain currents versus drain voltage with $V_{gs} = 0.0$V, $V_{gs} = 0.2$V, $V_{gs} = 0.4$V, $V_{gs} = 0.6$V, $V_{gs} = 0.8$V, and $V_{gs} = 1.0$V of n-channel FinFETs with the drawn gate lengths of (a) 110 nm and (b) 95 nm. The effective channel lengths are 102.2 nm and 85.8 nm, respectively.

the saturation velocity of 0.25-μm and 0.11-μm n-channel FinFETs. The saturation velocity of the short-channel devices is slightly higher than the long- and the

medium-channel devices. The different saturation velocity suggests the velocity overshoot in short-channel devices. In sub-100 nm bulk MOSFET devices, the velocity saturation has been reported in many literatures. The effective channel length of the experimental short-channel FinFETs is smaller than 100 nm, which is close to the mean free path of electrons in the silicon. Furthermore, the silicon body is not doped, thereby the electrons experience extremely small number of scattering centers. The velocity overshoot effects can be lumped into an effective increase of the saturation velocity. The velocity overshoot is beneficial escpecially for n-channel devices, because in general, the performance of the n-channel devices with short gate lenghs are known to be more limited by saturation velocity.

The experimental and model $I_{ds} - V_{ds}$ data of n-channel FinFETs with the drawn gate lengths of 110 nm and 95 nm are presented in Fig. Figure IV.24: with the extracted saturation velocity and the channel length modulation. The drain current plots are in an excellent agreement with the experimental data in all bias regimes. Channel length modulation effects are not excessive in the experimental data due to the excellent control of gate over the channel region. It is worth noting that the geometric parameters from the long-channel FinFETs are common to all the medium- and short-channel FinFETs. Although the short-channel effects are extremely sensitive to the geometric parameters, the same geometric parameters describe the electric characteristics of very short FinFETs with an extremely good agreements. The physical soundness of the analytic model for DG MOSFETs and the validity of the systematic modeling procedure have been validated by the well-agreeing drain current plots for all operation regimes over a wide range of gate lengths.

IV.E Summary

The experimental n-channel FinFETs has been calibrated with the analytic potential model for DG MOSFETs. The geometric parameters can be extracted from the $C_{gs} - V_{gs}$ data modeled with quantum mechanical effects. Minimizing the standard deviation of the errors, an excellent agreement between the experimental and the model data can be achieved. The extracted geometric parameters are close to the nominal values. With the modified universal mobility model with both a phonon and a Coulomb scattering term is applied to calibrate the $I_{ds} - V_{gs}$ data with low drain bias.

The source-drain series resistance effects are separated out by the *Shift-and-Ratio* method to model the intrinsic mobility of the medium-channel FinFETs. The extracted intrinsic mobility decreases as the gate length shrinks, degrading the normalized drain currents in the shorter devices more aggressively. The high-field effects were modeled in terms of the saturation velocity and the channel length modulation to regenerate $I_{ds} - V_{gs}$ and $I_{ds} - V_{ds}$ data for all bias regimes.

The short-channel n-channel FinFETs are calibrated by 2-D analytic potential model. The short-channel effects have been adequately modeled in terms of the DIBL, the threshold voltage roll-off, and the subthreshold current slope. The extracted effective channel lengths gives 9 nm of ΔL suggesting that the dopants in an identical process diffuse into the channel by the same distance. It is found that the electron mobility of the short-channel FinFETs does not degraded further once it reaches a minimum. The electron mobility of the short-channel devices are comparable to that of the unstrained silicon. The saturation velocity of the short-channel devices is slightly higher than the long-channel and medium-channel devices due to the velocity overshoot.

In the compact modeling of the n-channel FinFETs, the same geometric parameters have been used covering all the devices with a wide range of gate

lengths. The extracted geometric are close to the nominal values; the electric parameters are comparable to those of modern CMOS technologies. The analytic potential model has been fully validated by calibrating the experimental n-channel FinFETs over a wide range of gate lengths and bias regimes, incorporated with quantum mechanical effects, the short-channel effects, the high-field effects, the parasitic resistance effects, and the gate-length-dependent strain effects.

The text of Chapter Chapter IV, in part, is a reprint of the material as it appears in "Gate-Length-Dependent Strain Effects in N- and P-Channel FinFETs" by Jooyoung Song, Bo Yu, Yu Yuan, and Yuan Taur, IEEE Transactions on Electron Devices, Mar 2009. The dissertation author was the primary investigator and author of this paper.

The text of Chapter Chapter IV, in part, is a reprint of the material as it appears in "Compact Modeling of Experimental N- and P-Channel FinFETs" by Jooyoung Song, Yu Yuan, Bo Yu and Yuan Taur, Submitted to IEEE Transactions on Electron Devices. The dissertation author was the primary investigator and author of this paper.

Chapter V

P-Channel FinFET Hardware Calibration of Double-Gate MOSFET Compact Model

The unique complimentary property of the modern CMOS technology is due to the availability of p-channel MOSFETs pairing n-channel MOSFETs. Unlike other unipolar devices, the compact modeling of CMOS is incomplete without a valid model for p-channel devices. As the dimension of the CMOS continues to shrink, formerly poor performance of pMOSFETs has been enhanced greatly due to advanced stress engineering and intensive studies of various channel orientation, and thus the importance of the model accuracy of p-channel MOSFETs is ever increasing.

Although the compact model for DG MOSFETs in Chapter Chapter II assumes n-channel devices, it is equally valid in p-channel devices with an appropriate conversion of polarity. For example, Poisson's equation Eq. (II.1), the very starting point of the DG MOSFET model, can be rewritten for holes as

$$\frac{d^2\psi}{dx^2} = \frac{-q}{\epsilon_{si}} p_i e^{-q(\psi - V)/kT}. \tag{V.1}$$

The simple conversion of q into $-q$ gives a valid Poisson's equation for p-channel DG MOSFETs, which is almost identical to that of n-channel DG MOSFETs. The identical derivations as introduced in Chapter Chapter II can be also conducted for p-channel devices starting from Eq. (V.1). This results a core model for p-channel DG MOSFETs identical to that of n-channel FinFETs except that the opposite polarity of the external voltages, i.e., $V_{gs} < 0$ and $V_{ds} < 0$ in normal operation condition; also the sign of threshold voltage changes to negative.

While the core model and the short-channel model of MOSFETs are clear to convert from n-channel MOSFETs to to p-channel MOSFETs, quantum mechanical effects of holes are not straightforward to be adopted from the electron model. Not only the electric field pattern inside the silicon body, but also the carrier energy band structure is important in quantum mechanical effects. The band structure of the holes in the silicon is highly complicated; the rigorous modeling of quantum mechanical effects of p-channel MOSFETs often leads to mathematical complexity with no physical insight. On the other hand, adopting quantum model of n-channel devices with adjustable coefficient provides a satisfactory accuracy. In general, quantum mechanical effects is smaller in p-channel devices than in n-channel devices, because the hole mass is heavier than the electron mass in most surface and channel orientation.

In this chapter, the compact modeling of p-channel FinFETs are covered. Like the n-channel FinFETs, a long-channel gate capacitance data and drain currents data over a wide range of gate lengths are available for p-channel FinFETs. Because the same compact model is also applicable with minimum change, mostly the differences between the characteristics of n-channel FinFETs and p-channel FinFETs due to different band structures are discussed.

Table V.1: Nominal and extracted parameters by model with and without quantum mechanical correction of 10-μm p-channel FinFETs.

Parameter	Unit	Nominal Values	Model by Ratio	Model by Difference
W_{eff}	nm	150	147.3	156.6
L	μm	10	10	10
t_{ox}	nm	2.0	2.2	2.2
t_{si}	nm	30.0	30.0	30.0
$\Delta\phi$	mV	0	-23	-16

V.A Compact modeling of a $C_g - V_{gs}$ data

The compact modeling of p-channel FinFETs also starts from the calibration of $C_g - V_{gs}$ data. The same gate length of 10 μm is used to calibrate the gate capacitance data. The same approach as the n-channel FinFETs is applicable. Minimizing either of the standard deviation of the ratio or the difference is applicable to calibrate the model with the data. The same sets of geometric parameters as the n-channel FinFET, namely, the effective width, the effective oxide thickness, the quantum mechanical coefficient, and the work-function difference between the gate material and the silicon body are adjusted at the same time.

V.A.1 Calibration of $C_g - V_{gs}$ data

The model and the experimental data are presented in Fig. Figure V.1: and Fig. Figure V.2: comparing the ratio and the difference respectively. The best-fitting regions of two curves show a similar trend to those of the n-channel FinFETs. Minimizing the standard deviation of the ratio gives a very accurate transition region, whereas the minimization of the difference gives an accurate strong-inversion region. In the further compact modeling, the difference model, suitable for digital applications, is used.

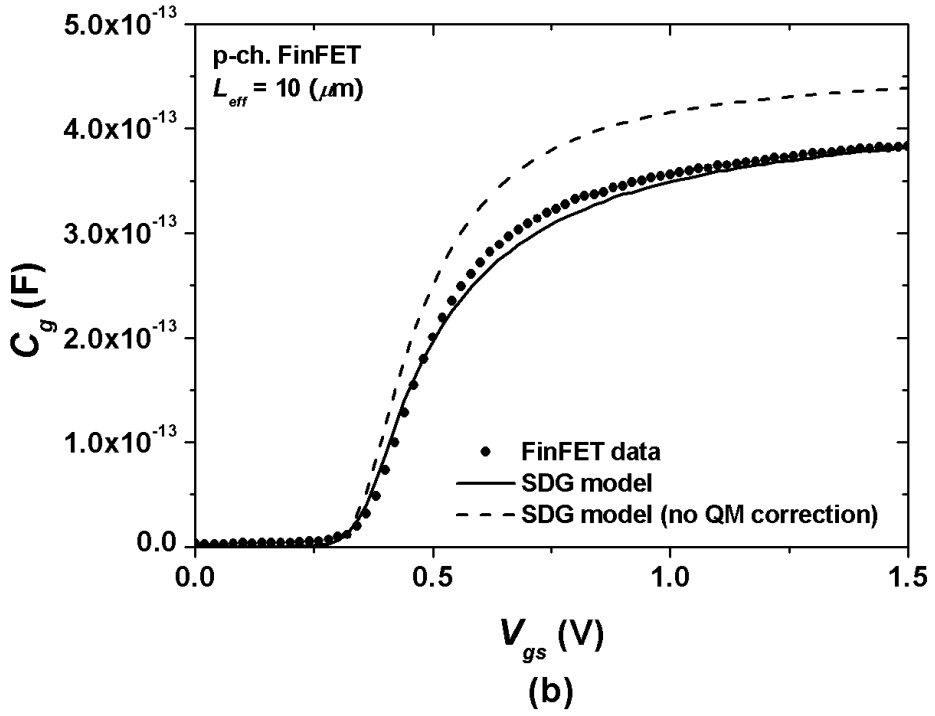

Figure V.1: Model and measured $C_g - V_{gs}$ data of a 10-μm p-channel FinFET by minimizing the standard deviation of the ratio. Symbol is for the measured data, dashed line for the model without quantum mechanical correction, solid line for the model with quantum mechanical correction.

The gate capacitance of the 10-μm p-channel FinFET in Fig. Figure V.2: is smaller than that of the n-channel FinFET. Due to the heavier hole mass than the electron, quantum mechanical effects in the p-channel FinFETs is smaller than the n-channel FinFETs. In other words, the p-channel FinFETs have the higher gate capacitance than the n-channel FinFETs with the same gate area. However, the effective width of this particular p-channel FinFET is smaller than the n-channel FinFET presumably due to shorter inversion layer in the vicinity of the gate tail structure in Fig. Figure III.1:. The die-to-die variation in the fabrication process must be taken into account as well. Table Table V.1: presents the nominal and

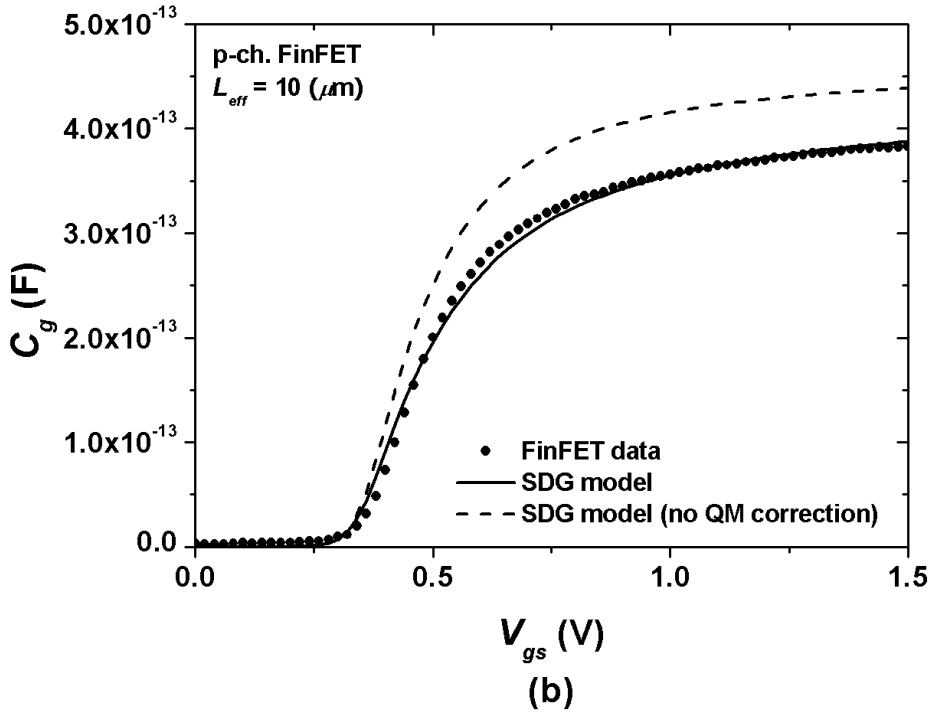

Figure V.2: Model and measured $C_g - V_{gs}$ data of a 10-μm p-channel FinFET by minimizing the standard deviation of the difference. Symbol is for the measured data, dashed line for the model without quantum mechanical correction, solid line for the model with quantum mechanical correction.

the extracted model geometric parameters of the long-channel, p-channel FinFET. The extracted model parameters are close to the expected nominal values, thereby the physical soundness of the model is shown in the case of the p-channel FinFET as well.

In both cases, it is clear that quantum mechanical effects are required to reproduce the experimental data. Without quantum mechanical effects, the gate capacitance is seriously overestimated. Quantum mechanical effects degrade the gate capacitance and hence the drain currents of the p-channel FinFET.

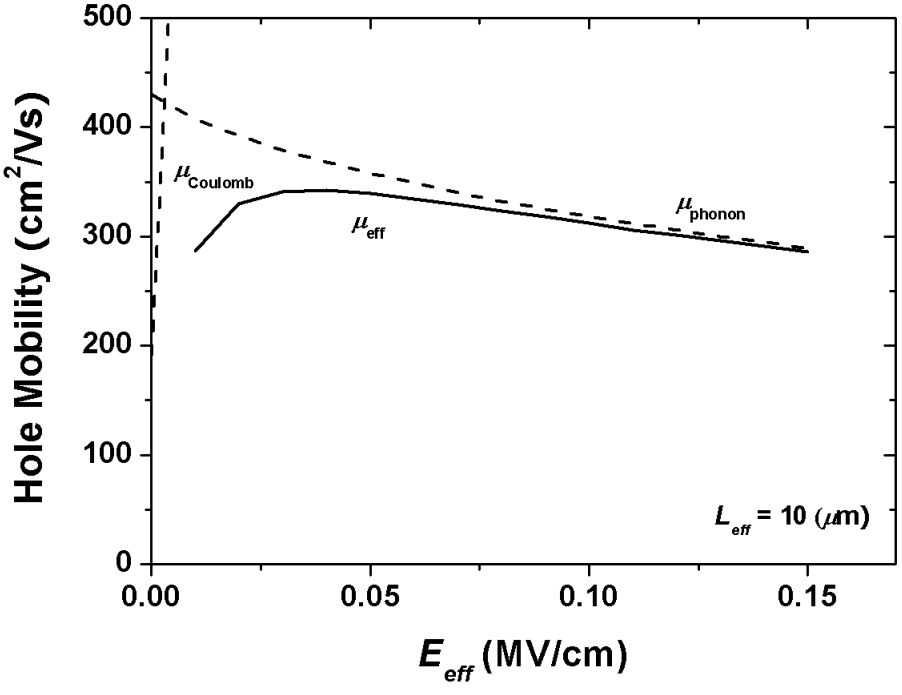

Figure V.3: Hole mobility versus effective field of a 10-μ p-channel FinFET from Eq. (II.28). The solid line is for the extracted mobility, μ_{eff}, and the dashed lines are for the Coulomb and phonon scattering term.

V.B Compact modeling of a long-channel p-channel FinFET

Once the geometric parameters are extracted, the drain currents with low drain bias of a long-channel p-channel FinFET can be calibrated with the same modified mobility model for the n-channel FinFETs. The long-channel p-channel FinFET is also free from the short-channel effects and the series resistance effects.

Table V.2: Mobility parameters of p-channel FinFETs.

Parameter	Unit	Values
μ_{eff}^{phonon}	$cm^2/V{\cdot}s$	430
E_{eff}^{phonon}	kV/cm	370
ν_{phonon}	-	0.8
$\mu_{eff}^{Coulomb}$	$cm^2/V{\cdot}s$	191
$E_{eff}^{Coulomb}$	kV/cm	34
$\nu_{Coulomb}$	-	1.3

V.B.1 Long-channel mobility of p-channel FinFET

The universal mobility model of Eq. (IV.7), employed in the n-channel FinFETs, also successfully describes the mobility of the p-channel FinFETs as a function of effective field. The effective field is given by

$$\begin{aligned} E_{eff} &= \frac{Q_d + Q_i}{3\epsilon_{si}} \\ &= \frac{Q_i}{3\epsilon_{si}}. \end{aligned} \tag{V.2}$$

The pre-factor 3, adopted by Takaki *et al.* [26], is purely empirical to allow the universal mobility behavior of the hole mobility versus the effective field. The extracted mobility is presented in the Fig. V.B.1 with the degradation in the low and the high field regimes due to the Coulomb and the phonon scattering, respectively. The extracted parameters for the long-channel mobility of the p-channel FinFET are given in Table Table V.2:.

The mobility is comparable to the reported hole mobility of ⟨110⟩-oriented channel on (110)-oriented surface in Fig. Figure V.4:.

The (110)/⟨110⟩ surface/channel orientation is beneficial for hole mobility, although electron mobility is smaller than the (100)/⟨100⟩ surface/channel orientation [67]. In the conventional planar devices, employing (110)-oriented surface requires (110)-oriented substrate which has to be prepared separately. In case of

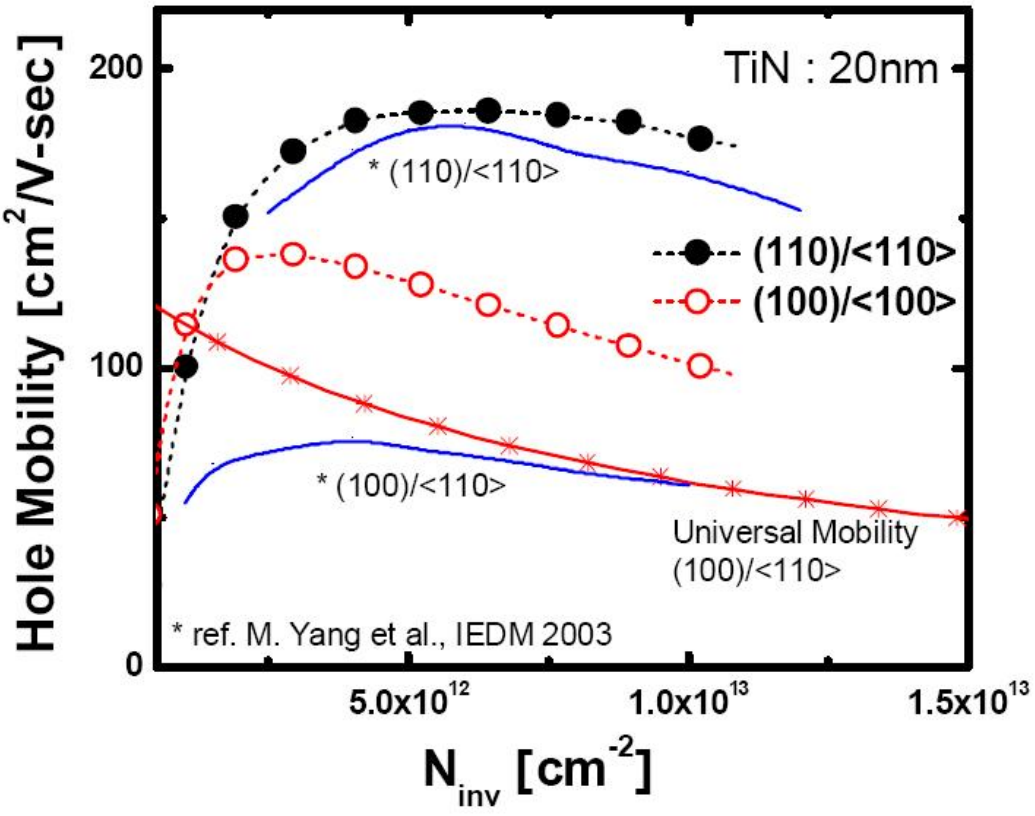

Figure V.4: Hole mobility versus inversion charge for (110)/⟨110⟩ and (100)/⟨100⟩ surface/channel orientation (Adopted from [67]).

DG FinFETs, various surface orientation including (110)-oriented surface can be easily obtained by sidewalls depending on the channel direction without additional fabrication process to achieve enhanced hole mobility.

V.B.2 Drain current of long-channel p-channel FinFET

The extracted mobility well describes the $I_{ds} - V_{gs}$ data with the low drain bias ($V_{ds} = 0.05$V) of Fig. Figure V.5:. Unlike the long-channel n-channel FinFET, the experimental data of the long-channel p-channel FinFET show a large gate-induced drain leakage (GIDL) in the deep subthreshold region presumably due to the deep boron diffusion into the channel region hence more dense packed electric

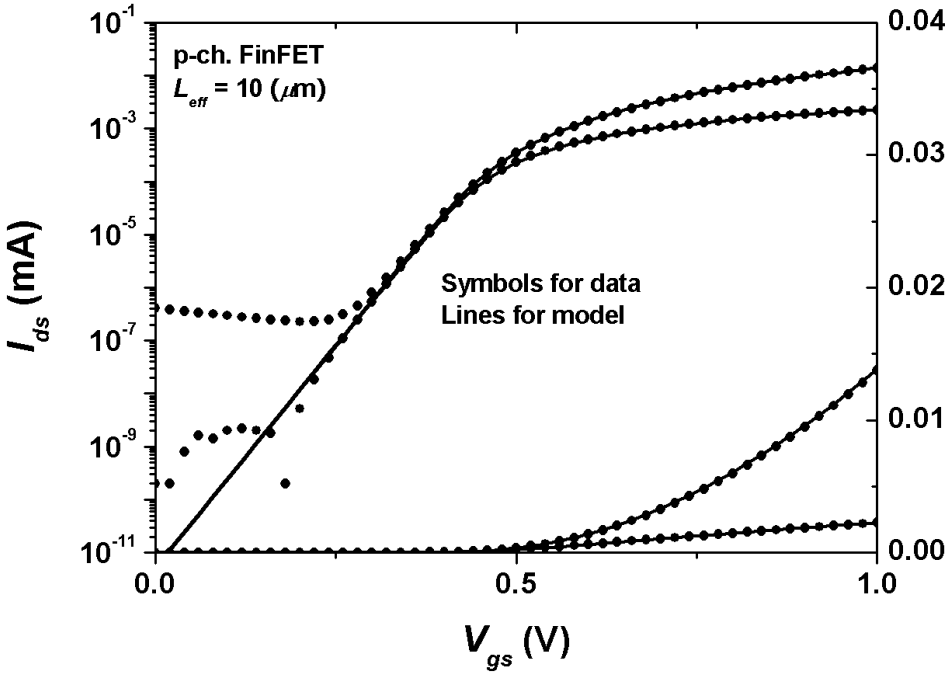

Figure V.5: Drain current versus gate voltage of a 10-μm p-channel FinFET with modified universal mobility model with the low (V_{ds} = 50mV) and high drain voltages (V_{ds} = 1V).

field in the vicinity of the source and the drain. However, an ideal 60 mV/dec. of the subthreshold current slope, expected by the model, is generated from the experimental device. With high gate overdrives, degradation of the transconductance g_m is observed due to the mobility degradation.

In summary, the long-channel, p-channel FinFET is calibrated by the analytic potential model for DG MOSFETs. The experimental $C_g - V_{gs}$ data was calibrated by minimizing the difference of the model and the experimental data. The extracted geometric parameters closely agree with the expected nominal values. The modified universal mobility describes the drain current versus the gate voltage well. An ideal 60 mV/dec. of subthreshold current slope is reproduced by

the analytic model.

V.C Compact modeling of medium-channel p-channel FinFETs

With the extracted geometric parameters from the $C_g - V_{gs}$ calibration, the medium-channel devices can be calibrated. Similar to the n-channel FinFETs, the medium-channel p-channel FinFETs have no short-channel effects, but non-negligible source-drain series resistance effects. The *Shift-and-Ratio* method is employed to remove the series resistance effects to model the intrinsic mobility. However, due to the different energy band structure of the hole and the electron, the intrinsic mobility trend of the hole does not follow that of the electron. In this subsection, the compact modeling of medium-channel p-channel FinFETs in terms of the intrinsic mobility is discussed.

V.C.1 Normalized drain current trend of p-channel FinFETs

Like the compact modeling of the n-channel FinFETs, investigating the trend of the normalized drain currents of the p-channel FinFETs gives physical insight of the device characteristics with respect to the gate length. The normalized drain currents of p-channel FinFETs with selected gate lengths are presented in Fig. Figure V.6:.

While the drain current of each device looks similar to that of the n-channel FinFETs, its trend as a function of the gate length is completely different. As the gate length decreases, the normalized drain current increases. Because the parasitic resistances always degrade the drain current, the increase of the normalized drain currents cannot be explained by the series resistance effects alone. A negative

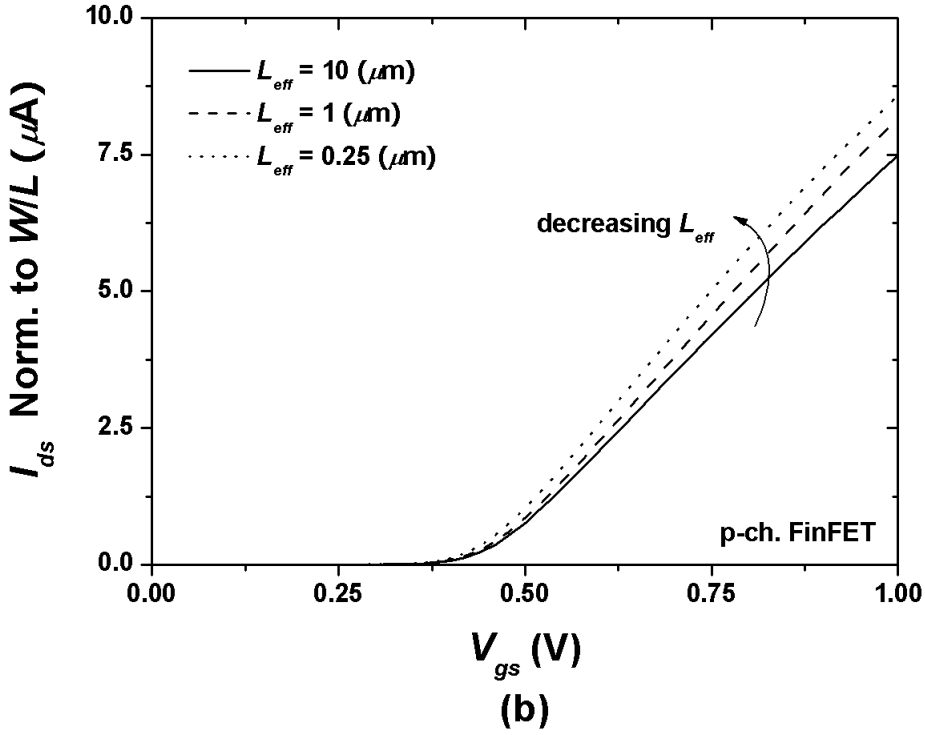

Figure V.6: Normalized drain currents versus gate voltage of 10-μm, 1-μm, and 0.25-μm p-channel FinFETs. The drain currents are normalized by W/L.

series resistance is required to describe the phenomenon. However, the assumption of a negative resistance is not physical.

In order to investigate the source of the increase of the normalized currents, separation of the source-drain series resistances is necessary. The same technique of *Shift-and-Ratio* is also applicable to the p-channel FinFETs. After removing the parasitic resistance effects, the remaining change of normalized drain current can be attributed to the intrinsic mobility.

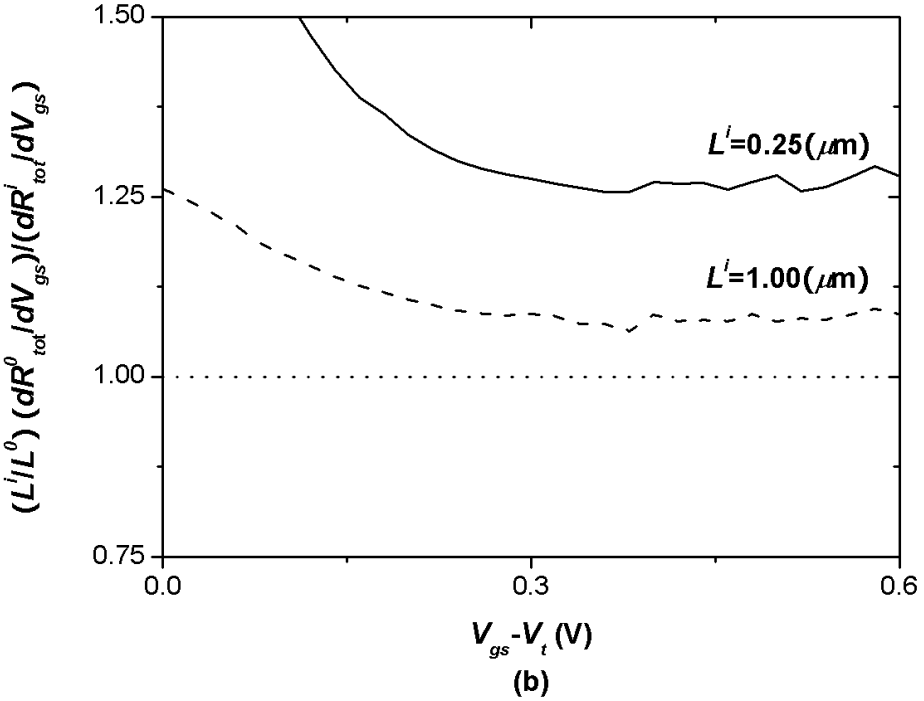

Figure V.7: The normalized ratios of the derivatives of the total resistances κ^i versus the gate overdrive of selected p-channel FinFETs. The dashed line indicates the ratio of the unity. L^0 is 10 μm for both devices.

V.C.2 Shift-and-Ratio method for separation of series resistance effects

The previously defined coefficient κ^i of p-channel FinFETs can be obtained by the ratio of the normalized derivatives of the total resistance of two devices with different gate lengths in Fig. Figure V.7:. As expected from the normalized current behaviors, κ^i of the medium-channel, p-channel FinFETs are greater than the unity. In other words, the hole mobility is enhanced as the gate length decreases.

By putting κ^i back into the total resistance equation, the series resistance of 156 $\Omega\cdot\mu$m is obtained. Interestingly the series resistance is smaller in the p-channel

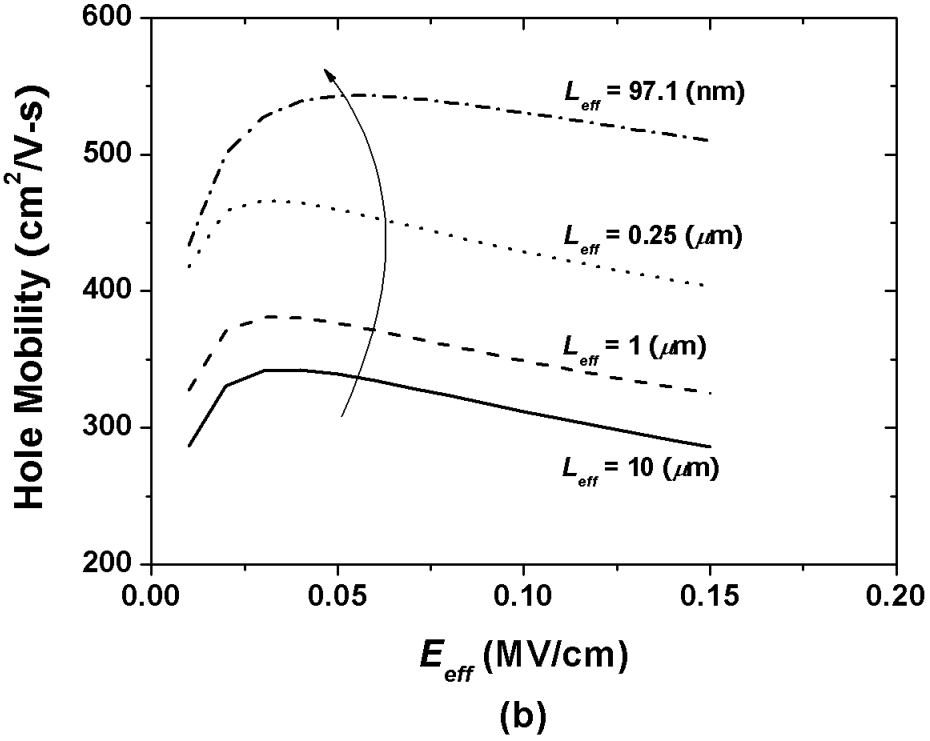

Figure V.8: The normalized ratios of the derivatives of the total resistances κ^i versus the gate overdrive of selected p-channel FinFETs. The dashed line indicates the ratio of the unity. L^0 is 10 μm for both devices.

FinFETs than in the n-channel FinFETs, presumably due to the wider diffusion of the boron in the source and the drain. Also, the mechanism responsible for the enhancement of the hole mobility may play a role in the reduction of the series resistance.

V.C.3 Mobility and drain currents of medium-channel n-channel FinFETs

The extracted mobility of medium-channel p-channel FinFETs in Fig. Figure V.8: explains the normalized current trend of Fig. Figure V.6:. The hole mobility increases as the gate length decreases; the enhancement is even larger than the degradation by the parasitic resistance effects. The abnormal normalized current trend can be explained by this large enhancement of the hole mobility.

With the extracted geometric parameters and the hole mobility, drain currents of the medium-channel p-channel FinFETs are calibrated. Several selected drain currents of the medium-channel FinFETs at the low drain bias are presented in Fig. Figure V.9:. The extracted model data agree with the experimental data excellently. Because the medium-channel devices do not have the short-channel effects, ideal 60 mV/dec. of the subthreshold current slopes are generated in the all p-channel FinFETs in observation.

By comparing the Figure IV.17: and Figure V.9: for n- and p-channel FinFETs respectively, the drain currents of n- and p-channel FinFETs become comparable towards the shorter gate lengths. Because the devices of interest are shorter devices, the comparable drain currents in the shorter devices simplifies design consideration greatly. Remembering that the primary limiting factor of the CMOS technology is the low current driving ability of p-channel devices, the experimental FinFETs are expected to show better performance in the shorter devices. Although the drain currents with the high drain bias ($V_{ds} = 1.0$V) are presented, the modeling of the high-field effects will be discussed in later sub-section.

V.C.4 Piezoresistance effects on p-channel FinFETs

Same as the n-channel FinFETs, the relaxed tensile strain explains the hole mobility enhancement. However, the physical reason for the hole mobility

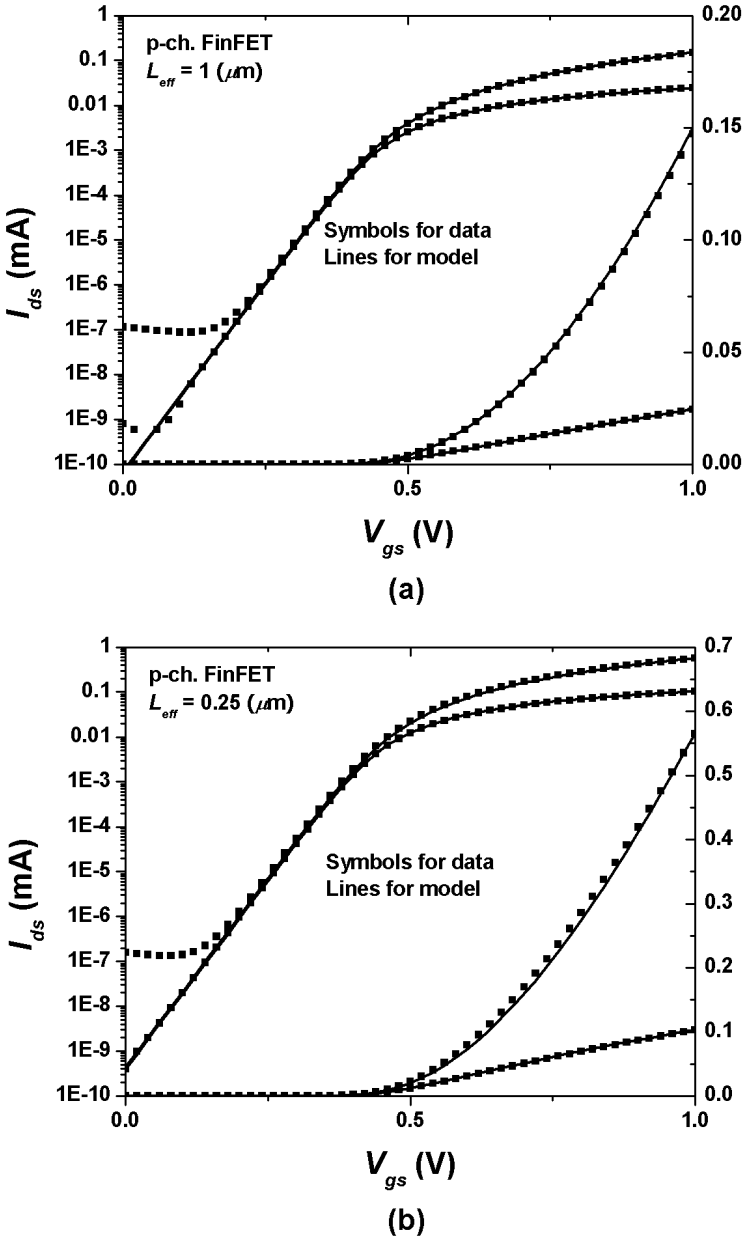

Figure V.9: The normalized ratios of the derivatives of the total resistances κ^i versus the gate overdrive of selected p-channel FinFETs. The dashed line indicates the ratio of the unity. L^0 is 10 μm for both devices.

enhancement is different from the electron mobility degradation. In case of the electron, the migration of the electron to the energy band with the low electron

mass is the cause of the enhancement under a strong tensile strain. The hole mobility degradation under a tensile strain is explained by so-called piezoresistive effects [74].

When a semiconductor is under strain, the energy band structure of the semiconductor experiences warps, changing the mobility of the carriers depending on the orientation and the strength of the applied strain. Although the final band structure is extremely complicated, the whole effect can be lumped into the change of resistance. This is known as piezoresistive effects. Because of its conceptual simplicity and relatively easy measurements and simulation procedures, it has been widely adopted in the semiconductor industry. It has been known that increase or decrease of the resistance is almost linearly proportional to the strain, especially when the strain is not very intense, i.e.,

$$\Delta R = \pi\sigma \tag{V.3}$$

where ΔR is the change of the resistance, π the piezoresistive coefficient, and σ the applied strain. The positive sign of σ corresponds to the tensile strain, whereas the negative sign corresponds to the compressive strain. Due to its clear definition and relatively easy measurement, piezoresistance has played a major role in the strain analysis in the semiconductor industries.

The piezoresistive coefficient π is easily measured by a simple apparatus in Fig. Figure V.10: for various strain and current orientation. Table. Table V.3: gives the measured piezoresistive parameters for Si p-channel MOSFETs with (001)- and (110)-surface orientations. The longitudinal piezoresistive coefficient, π_L, corresponds to the tensile strain induced by the metal gate has same orientation as the channel direction. π_L for silicon p-MOSFET for $\langle 110\rangle$-channel orientation on (110)-surface is a positive value, 27.3 [75]. By the definition of the piezoresistance Eq. (V.3), the positive piezoresistive coefficient gives increased resistance under tensile strain. Therefore, in the piezoresistive regime, the tensile strain on (110)/$\langle 110\rangle$ p-channel MOSFET increases the resistance, hence decreases the mo-

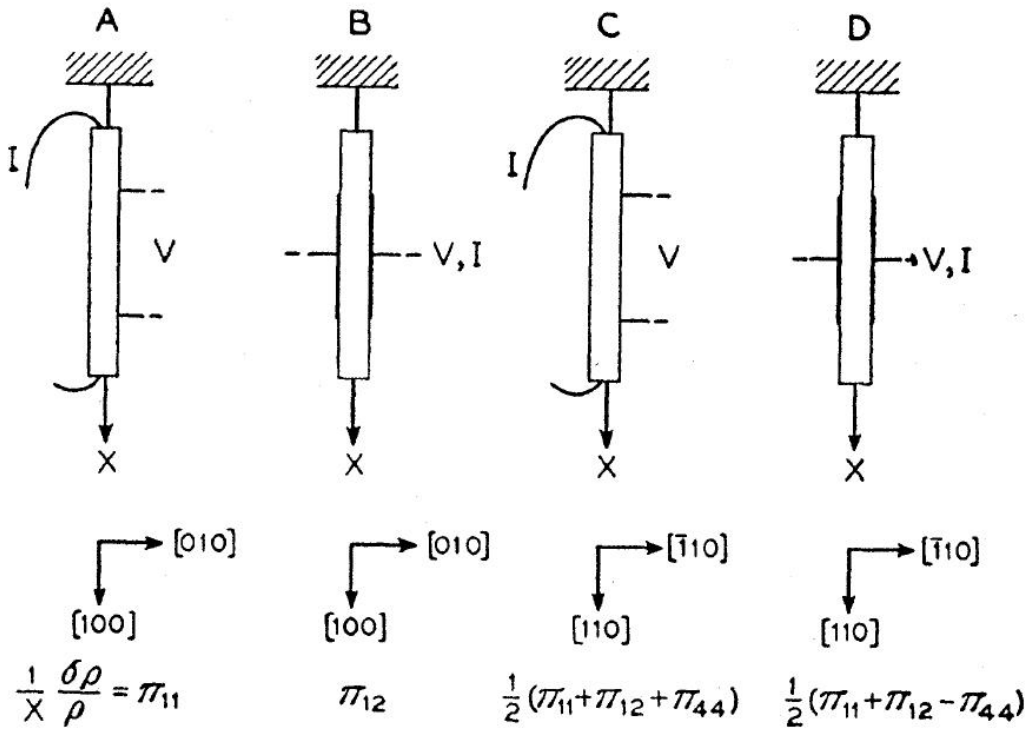

Figure V.10: Schematic diagram showing the stress sytem, the crystallographic orientation and the electrode structures for piezoresistance measurement. Arrangement A and C are designated as longitudinal; B and D are transverse (Adopted from [74]).

bility. However, it has been known that the hole mobility actually increases once the tensile strain increases beyond the piezoresistive regime. The mobility behavior in the excessive tensile strain cannot be explained by the piezoresistance, and a thorough analysis on the hole energy band structure is necessary.

V.C.5 High-field effects of medium-channel, p-channel FinFETs

By adding the high-field effects, $I_{ds} - V_{ds}$ data of medium-channel p-channel FinFETs are modeled for all bias regimes. After the channel length modulation

Table V.3: Calculated and measured piezoresistance coefficients for Si p-MOSFETs with (001) or (110) surface orientation (Adopted from [75]).

Substrate	(001)	(110)	
Channel	⟨110⟩	⟨110⟩	⟨111⟩
	Measured/Calculated		
π_L	71.7[a]/72.2	27.3(8.8)[b]/34	86[c]/79.1
π_T	-38.8[a]/-45.8	-5.1(3)[b]/-6.6	-50[c]/-43
$\pi_{Biaxial}$	40[a]/35.7	25.8(2.2)[b]/28.7	15.1[c]/10.2

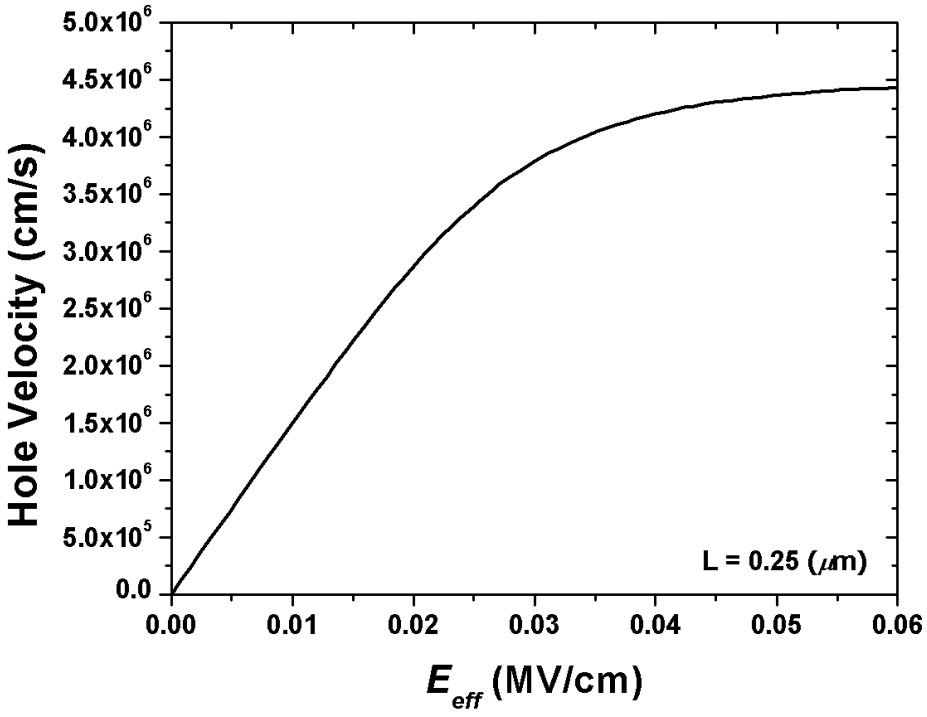

Figure V.11: Hole velocity versus effective lateral field of long- and medium-channel p-channel FinFETs. Saturation velocity of hole is 4.43×10^6 cm/s.

effects are modeled with the g_{ds} in the saturation region, hole saturation velocity is extracted to yield an accurate on-current. The extracted hole velocity is given

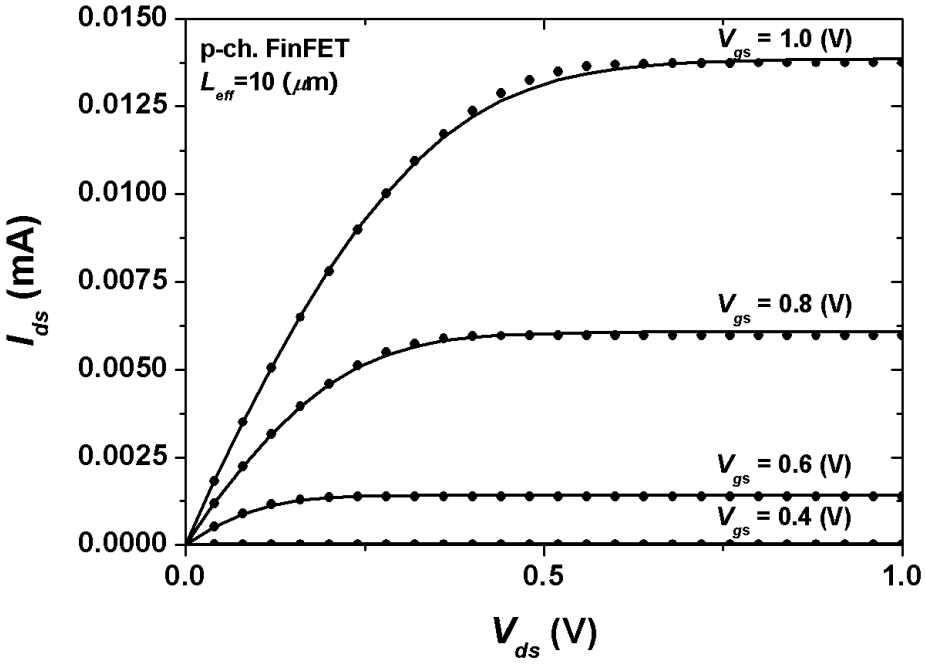

Figure V.12: Drain current versus drain voltage of 10-μm p-channel FinFET. Symbols are for the experimental data, and the lines are for the model.

in Fig. Figure V.11:. The saturation velocity is slightly higher than that of the n-channel FinFETs. P-channel FinFETs are less limited by the velocity saturation effects than the n-channel FinFETs.

The $I_{ds} - V_{gs}$ plots with the modeled saturation velocity of the long- and the medium-channel p-channel FinFETs are presented in Fig. Figure V.12: and Fig. Figure V.12:, respectively. The channel length modulation is modeled by the slope in the saturation region. Although the channel length modulation is slightly more observable in the p-channel FinFETs, the high-field effects of the medium-channel p-channel FinFETs are well-controlled with small channel length modulation.

In summary, the medium-channel p-channel FinFETs are modeled by the analytic potential model with the modified universal mobility model. The *Shift-*

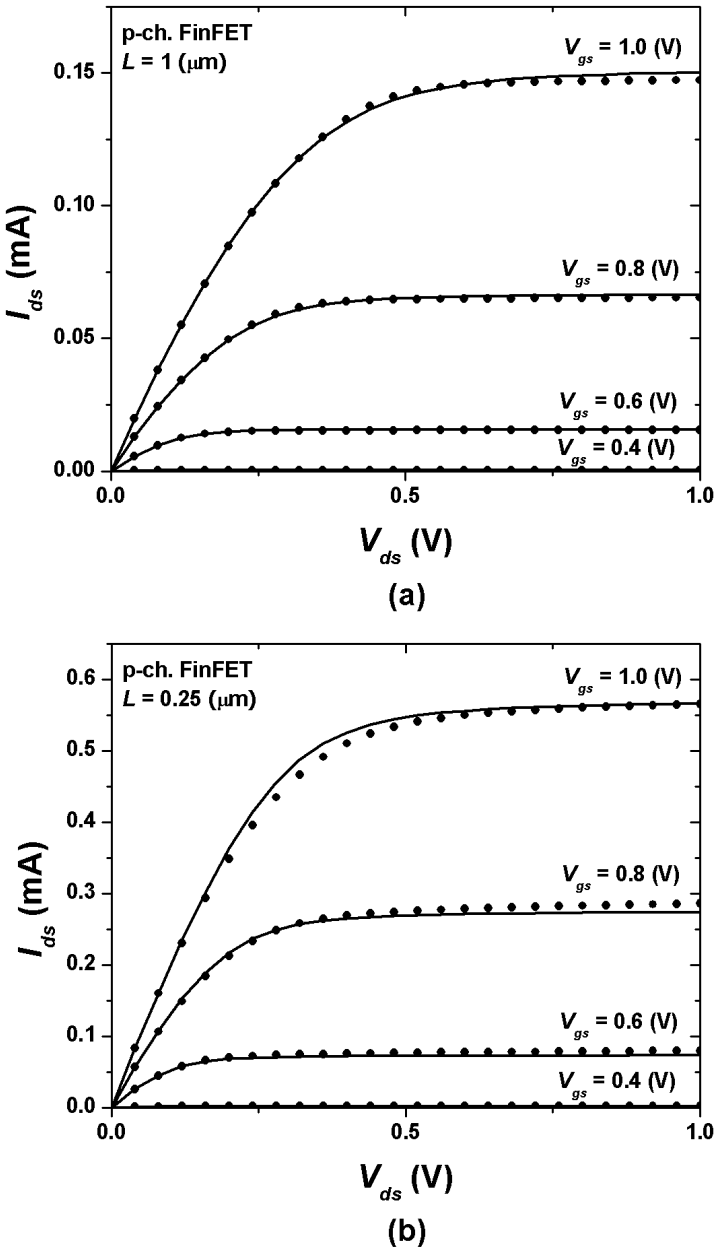

Figure V.13: Drain current versus drain voltage of (a) 1-μm p-channel FinFET and (b) 0.25-μm p-channel FinFET. Symbols are for the experimental data, and the lines are for the model.

and-Ratio method successfully separates out the source-drain series resistances. The enhancement of the intrinsic hole mobility is well-explained by the piezore-

sistance effects. The addition of high-field effects reproduces the drain currents of the medium-channel p-channel FinFETs in all bias regime with high accuracy.

V.D Compact modeling of short-channel p-channel FinFETs

The same 2-D short-channel model for n-channel MOSFETs is also applicable to the p-channel MOSFETs with a minimum change of the polarity, because the short-channel analysis does not rely on the effective masses of the carriers or more accurately, the band structure. The same explicit expressions for the threshold voltage roll-off, the DIBL, and the subthreshold current slope in Chapter Chapter II are fully valid in the p-channel FinFETs.

However, p-channel MOSFETs have relatively severe short-channel effects, therefore the compact modeling of an accurate compact modeling is demanding. Because boron diffuses deeper and faster into the silicon than arsenic, the effective channel length of the p-channel devices are shorter than that of n-channel devices. The doping profile of p0channel devices is also not abrupt, so that the 2-D analytic model assuming an abrupt rectangular channel region needs to be calibrated more carefully.

Similar to the n-channel devices, the high-field effects manifest themselves in terms of the channel length modulation and the velocity saturation. On the other hand, it has been known that the performance of p-channel devices are less limited by the carrier velocity saturation. Although the high-field effects are still important in the short-channel p-channel FinFETs, the high-field effects in the short-channel FinFETs is not as prominent as those of the n-channel FinFETs.

In this section, the compact modeling of short-channel, p-channel FinFETs are covered. The short-channel model for DG MOSFETs are validated by the

Table V.4: Nominal and effective channel length of short-channel n-channel FinFETs.

Parameter	Unit	Value		
Drawn Gate Length L	nm	110	100	95
Effective Channel Length L_{eff}	nm	96.1	87.1	80.1
ΔL_{eff}	nm	12.9	13.9	14.9

p-channel FinFETs in terms of the threshold voltage roll-off, the DIBL, and the subthreshold current slope. Also high-field effects are incorporated with the 2-D analytic potential short-channel model adequately.

V.D.1 Effective channel length of short-channel p-channel FinFETs

The effective channel lengths of the p-channel FinFETs are usually shorter than those of the n-channel FinFETs, hence larger short-channel effects. Nevertheless, a similar relation can be found between the effective channel length and the short-channel effects. The DIBL is most suitable to extract the effective channel lengths, because a single device is involved in the calibration. The extracted effective channel lengths of the p-channel FinFETs are given in Table Table V.4:. The differences between the drawn lengths and the effective channel lengths ΔL_{eff} are about 13 nm, being slightly longer than that of the n-channel devices. This is due to the faster and deeper boron diffusion.

The hole mobility is higher in the short-channel devices than in the medium-channel devices (Fig. Figure V.8:). However, the hole mobility does increase further in the short-channel devices. This saturation of the hole mobility enhancement confirms that the tensile strain reaches its minimum with the gate lengths of sub-100 nm. The hole mobility of the short-channel FinFETs are comparable to the mobility measured on unstrained (110)/$\langle 110 \rangle$ silicon. Therefore, one can

safely conclude that the gate-induced tensile strain is fully relaxed in the sub-100 nm regime.

Losing the tensile strain is beneficial for the p-channel devices, but degrades the performance of the n-channel devices. An interesting opposite trend has been reported by Thompson *et al.* The hole mobility is degraded towards the shorter gate lengths, whereas the electron mobility is enhanced with contact-etch-liner-induced tensile strain [76]. The trend by the contact-etch-liner-induced strain is exactly opposite to the metal gate-induced tensile strain, suggesting that the tensile strain becomes stronger towards the shorter gate lengths. If the technological difficulties can be resolved, dual-source-induced tensile, i.e., metal gate-induced and contact-etch-induced tensile strain for p- and n-channel FinFETs respectively, gives a possibility to achieve a maximized FinFET performance.

With the extracted effective channel lengths and the hole mobility model, it is possible to calibrate the $I_{ds} - V_{gs}$ data at the low drain bias with the modified universal mobility model. The calibrated model and the experimental data are presented in Figure V.14: for p-channel FinFETs with the drawn gate lengths of 110 nm and 95 nm. The model values of the DIBL well agrees with the experimental data without introducing any unphysical parameters. The subthreshold current slopes of the experimental data are slightly larger than the model prediction, due to the excessive short-channel effects and the non-ideal channel geometry. A mathematical fitting parameters, introduced in many compact modeling, can give a more closely matching curve. However,the introduced error by the 2-D analytic potential model is acceptable for digital applications. Furthermore, introducing non-physical parameters significantly degrade the predictability of the model for future technology generations.

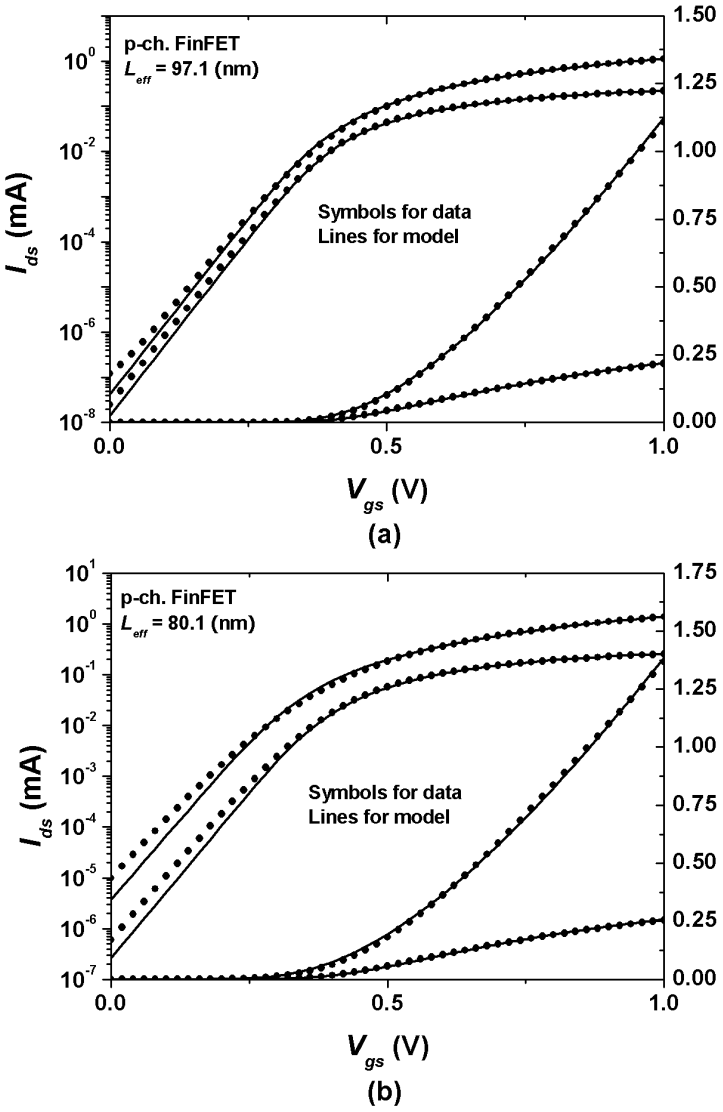

Figure V.14: Drain currents versus gate voltage at low (V_{ds} = 0.05mV) and high (V_{ds} = 1.0V) bias of (a) 110-nm and (b) 95-nm p-channel FinFETs. Symbols are for the experimental data and the lines for the model.

V.D.2 High-field effects of short-channel p-channel FinFETs

The addition of the high-field effects completes compact modeling of the p-channel FinFETs. After modeling the channel length modulation effects, the

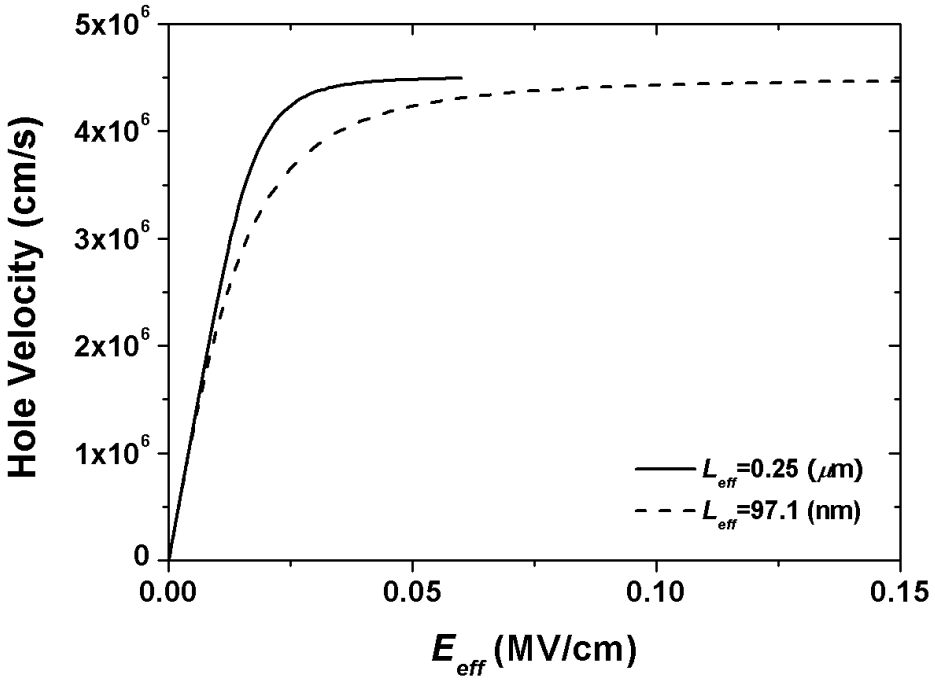

Figure V.15: Hole velocities versus effective lateral field of 0.25-μm and 0.11-μm p-channel FinFETs.

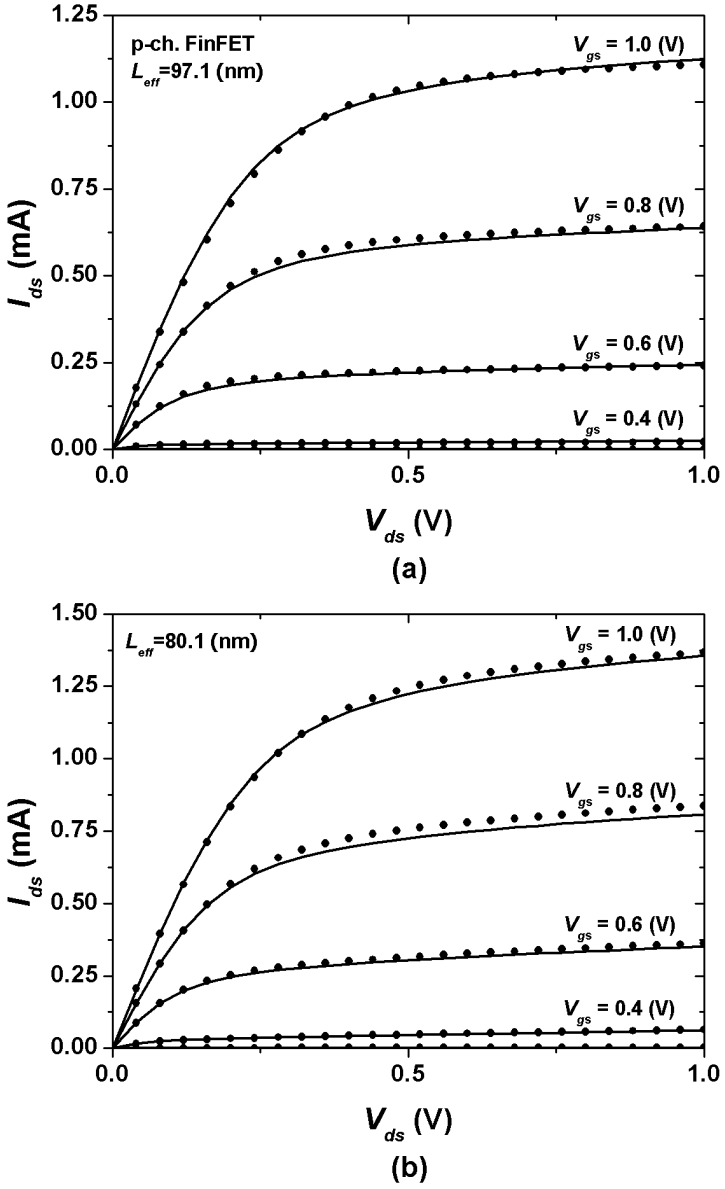

Figure V.16: Drain currents versus drain voltage with V_{gs} = 0.0V, V_{gs} = 0.2V, V_{gs} = 0.4V, V_{gs} = 0.6V, V_{gs} = 0.8V, and V_{gs} = 1.0V of p-channel FinFETs with the drawn gate lengths of (a) 110 nm and (b) 95 nm. The effective channel lengths are 96.1 nm and 80.1 nm, respectively.

saturation velocity is extracted from the $I_{ds} - V_{ds}$ data of short-channel p-channel FinFETs. The extracted hole velocity as a function of effective lateral field is presented in Fig. Figure V.15:

The channel length modulation and the velocity saturation is adequately modeled in $I_{ds} - V_{ds}$ curves in Figure V.16:. Unlike the n-channel devices, the saturation velocity of the holes in p-channel FinFETs presented in Figure V.15: is identical for the long-channel and short-channel devices. Remembering the discrepancy of the electron saturation velocities of the long- and short-channel n-channel FinFETs is due to the velocity overshoot, the velocity overshoot is not significant in the experimental p-channel devices. The holes with the given channel length still experience non-negligible scattering events in the channel region.

V.E Summary

The short-channel, p-channel FinFETs with various gate lengths have been calibrated with the 2-D analytic potential model for short-channel DG MOSFETs. A single parameter for the short-channel effects, effective channel length L_{eff}, was extracted for each devices. The short-channel model well agrees with the experimental data in terms of the threshold voltage roll-off, the DIBL, and the subthreshold current slope degradation. The high-field effects of the short-channel FinFETs are adequately modeled to describe the channel length modulation and the velocity saturation effects.

The text of Chapter Chapter V, in part, is a reprint of the material as it appears in "Gate-Length-Dependent Strain Effects in N- and P-Channel FinFETs" by Jooyoung Song, Bo Yu, Yu Yuan, and Yuan Taur, IEEE Transactions on Electron Devices, Mar 2009. The dissertation author was the primary investigator and author of this paper.

The text of Chapter Chapter V, in part, is a reprint of the material as it

appears in "Compact Modeling of Experimental N- and P-Channel FinFETs" by Jooyoung Song, Yu Yuan, Bo Yu and Yuan Taur, Submitted to IEEE Transactions on Electron Devices. The dissertation author was the primary investigator and author of this paper.

Chapter VI

Conclusion

This dissertation presents comprehensive compact modeling of experimental n- and p-channel FinFETs with the analytic potential model for double-gate MOSFETs.

First, the analytic potential model for DG MOSFETs is derived from the solutions to 1-D Poisson's and current continuity equations to yield the silicon body potential, the inversion charge, the drain current, and the gate capacitance expressions in terms of an intermediate parameter β. The expressions are valid for all operation regions seamlessly.

Quantum mechanical effects were empirically modeled to take the finite inversion layer thickness into account. A quantum mechanical correction term was added to the oxide thickness.

The short-channel model is derived from the 2-D Poisson's equation with its associated boundary-value problem to give the potential at any point in the silicon body. By focusing on the minimum potential barrier along the channel direction, explicit expressions of DIBL, threshold voltage roll-off, and subthreshold current slope are obtained as a function of channel length for the purpose of compact modeling.

The high-field effects including the velocity saturation and the channel length modulation are modeled similar to those of the bulk MOSFETs.

Verification and calibration of the compact model start with the gate capacitance or $C_g - V_{gs}$ data of the $\langle 110 \rangle / (110)$ channel/surface-oriendted, long-channel n- and p-channel FinFET. Incorporation of quantum mechanical effects in the model is essential so as not to overestimate the gate capacitances.

The mobility model with both a phonon and a Coulomb scattering term is employed to describe the carrier mobility and the $I_{ds} - V_{gs}$ data at low drain bias of long-channel n- and p-FinFETs. The commonly adopted universal mobility model with only a phonon scattering term cannot adequately describe the drain current data at low gate overdrives.

The normalized drain current trends of medium-channel n- and p-channel FinFETs are opposite to each other. While the normalized current of n-channel FinFETs decreases towards shorter gate lengths, that of the p-channel FinFETs increases. The observed data cannot be explained by the source-drain series resistance alone as it always degrades normalized drain currents at short gate lengths.

In order to extract the intrinsic mobilities, *Shift-and-Ratio* method was applied to separate out the parasitic resistance effects. A useful coefficient κ^i was defined to indicate the increase or decrease of the intrinsic mobility with gate length. The intrinsic mobilities are degraded for n-channel FinFETs and enhanced for p-channel FinFETs towards shorter gate lengths. The mobility trends are consistent with a relaxed tensile strain towards the shorter devices. With tensile strain, the subband with lighter electron effective mass becomes more populated than the subband with heavier effective mass. The reduced effective mass results in the increased mobility. Holes in the piezoresistive regime behave oppositely, with their mobility lowered at increased tensile strain.

The short-channel model is validated by the calibration of the short-channel $I_{ds} - V_{gs}$ data in terms of the threshold voltage roll-off, the DIBL, and the sub-

threshold current slope degradation. The extracted effective channel lengths give almost uniform values of ΔL_{eff}, the difference between the drawn gate length and the effective channel length. The uniform ΔL_{eff} suggests that dopants diffuse into the channel by the same distance. As expected, boron diffuses farther than arsenic.

Finally, adding the high-field effects completes the compact modeling of the experimental hardware. The $I_{ds} - V_{gs}$ data at high drain bias and the $I_{ds} - V_{ds}$ data of all bias regimes are in full agreement with the compact model following the addition of velocity saturation and channel length modulation effects.

With the comprehensive compact modeling of experimental FinFET hardware, the analytic potential model for DG MOSFETs has been fully validated.

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