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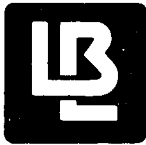

Lawrence Berkeley Laboratory

UNIVERSITY OF CALIFORNIA

Materials & Chemical Sciences Division

Submitted to Journal of Electronic Materials

Materials Study of Silicon-on-Insulator Material by TEM

E.P. Kvam, J. Washburn,
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MATERIALS STUDY OF SILICON-ON-INSULATOR MATERIAL BY TEM

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Materials Study of Silicon-on-Insulator Material by TEM

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Silicon-on-insulator (SOI) technology addresses the need for many different device applications, such as radiation tolerant devices, high voltage, and three-dimensional circuitry applications. Isolated silicon epitaxy (ISE) is a commercialised process which results in excellent SOI material quality with proven results, having overcome most of the obstacles of other processes, although only having reduced, not eliminated, threading dislocations. The remaining isolated dislocations have been examined in detail by transmission electron microscopy (TEM). These have been diagnosed as normal lattice dislocations, with no faults or twins in the material. The nature, source, and behavior of the remaining dislocations is discussed.

Materials Study of Silicon-on-Insulator Material by TEM

E.P. Kvam, J. Washburn, L.P. Allen, and P.M. Zavracky

Abstract

Silicon-on-insulator (SOI) technology addresses the need for many different device applications, such as radiation tolerant devices, high voltage, and three-dimensional circuitry applications. Isolated silicon epitaxy (ISE) is a commercialised process which results in excellent SOI material quality with proven results, having overcome most of the obstacles of other processes, although only having reduced, not eliminated, threading dislocations. The remaining isolated dislocations have been examined in detail by transmission electron microscopy (TEM). These have been diagnosed as normal lattice dislocations, with no faults or twins in the material. The nature, source, and behavior of the remaining dislocations is discussed.

Introduction

There is considerable interest in silicon-on-insulator (SOI) wafer materials because of the inherent structural advantages for radiation hardened, high voltage, high packing density, and three-dimensional circuitry, as well as for high-temperature device applications[1-5]. The topic here, isolated silicon epitaxy (ISE), has been shown to be a leading process technology for the production of SOI wafers[6,7], and is an attractive technology from a manufacturing point of view because of its potential for large scale, low cost production. The process is fundamentally simple, and the equipment costs are low.

This technology (ISE SOI) has evolved from the techniques used in zone melt recrystallization (ZMR) and lateral epitaxy by seeded solidification (LESS), processes which were developed at MIT Lincoln Laboratory[4,5]. In contrast to its predecessors, however, development of ISE SOI processing has managed to overcome material defect

problems such as protrusions, severe wafer warp, high surface roughness, and waviness, so that values for these characteristics are now comparable to bulk Si[8].

The process by which a bulk Si wafer is converted to an ISE SOI structure encompasses three essential steps. First, most of the wafer surface is thermally oxidized. A thin polycrystalline Si film, followed by a SiO_2 cap, are then deposited upon the entire wafer. This process is carried out in large wafer batches in commercial tube furnaces. Finally, the polycrystalline layer is melted and directionally regrown, using the unoxidized portion of the wafer as a seed, leaving an isolated single crystal layer, which may be exposed by the easy removal of the oxide cap.

The cross sectional structure of the ISE wafer during regrowth is illustrated in Figure 1. The dimensions of the oxide and upper Si layer thicknesses are, of course, variable, from 0.2 to 2.5 μm. The dimensions are essentially constant across the wafer, excepting the very rim. The roughness of the isolated-Si/SiO_2 interface is ~5nm over a distance of about 1μm.

Experimental Observations

The structure of the upper Si layer has been carefully examined. In this paper, we report the results from transmission electron microscopy (TEM), which was used to study the nature of individual defects and interfaces. X-ray topographic images[9] and Nomarski images of etched samples[6] have shown lines of defects ("trails") spaced about 100μm apart, with very closely spaced defects within these trails. These defect trails ran parallel to each other along the [010] regrowth direction.

Closer examination of these trails in TEM revealed them to consist of dislocations threading from the SiO_2 interface to the vacuum interface. These were closely spaced, about 0.5 to 1μm, along the trails. Diffraction contrast was used to identify the dislocations' Burgers vectors (**b**). Averaged over many dislocations, the assortment of Burgers vectors was approximately evenly divided amongst the six possible $^1/_2$<110>

lattice vector dislocations. The dislocations were nearly randomly arrayed, or in small combinations of same-type groupings, but occasionally up to 12 dislocations of the same **b** (and, incidentally, same line directions) were observed. These two morphologies are shown in Figure 2(a and b).

The fact that the dislocations were of approximately equal numbers and types agrees with previous high-resolution x-ray work, in which the mosaic spread was found to be quite small[9]. This indicated that the defect trails contained a net Burgers vector content (i.e. sum of all **b**s in the trail) of near zero: thus, they contributed no long range misorientation effects.

Although all of the observed dislocations were of the full lattice translation vector type, a few were observed to be somewhat dissociated, though these were a minority, and the dissociation was never more than 10nm. Also, many dislocations were observed to react, with three different dislocations all entering a single node. There did not seem to be a tendency for the splitting to yield or remove an extra dislocation; that is, moving from the oxide toward the vacuum interface, a pair of dislocations was about equally as likely to combine as a single dislocation was to "split" into two. Some of these nodes can be seen in Fig. 2(a). These points, and the noncrystallographic threading orientations, indicate that the dislocations were grown in, and that there is very little stress in the epilayer.

No precipitation was observed on any dislocation, even when viewed by weak-beam techniques. The one dislocation which could be observed in cross-sectional TEM showed no variation in image along its length, even at the point of origin on the SiO_2 interface. Similarly, the SiO_2 interface showed no peculiarities near the dislocation. Although not eliminating the possibility of solute segregation to dislocations, the lack of precipitation established an upper bound, and also indicated that precipitate-induced dislocation formation was unlikely.

Discussion

The dislocation trails are thus not an inherent property of the material, but clearly seem to be a growth artifact. If precipitation or low-angle boundaries had been observed, these could have been deemed an external cause, but neither could be identified. The trails are probably associated with a periodically varied solidification front[10,11], such as shown in Figure 3. Cellular growth of this type is generally associated with low-level but detectable solute segregation, and the period wavelength is typically related to the solidification rate[12]. In semiconductor materials, however, the strong tendency to facet on the {111} planes may supply the impetus for breakdown of the planar solidification front.

At the trailing part of the growth front, the undercooling can provide substantial energy to grow defects into the material. Since this is also the point where two nearly independent crystals meet, it is also the most likely place for defects to occur. Fluctuations in temperature, density, growth velocity, or interface stress from the constraining SiO_2 layers could contribute small, transient misalignments of one cell with respect to its neighbor, leading to the introduction of a dislocation at their interface.

A persistent perturbation could consistently induce a single type of dislocation; however, the long-range displacement field of each dislocation would affect the nature of a perturbation in a opposite manner. Thus, a pinned perturbation (e.g. at the oxide/melt interface) would induce a series of like dislocations, which would cause offsetting strain fields, until dislocation array could overcome the perturbation. In fact, the effect of the dislocation introductions would be self-limiting, in that consistent introduction of one type of dislocation would cause high-energy long-range displacement fields, and so would be unfavorable. This may be why no true low-angle grain boundaries are observed in these materials.

Methods for reducing the defect trail density can thus, it appears, concentrate on solidification parameters, such as reducing the growth velocity or incresing the thermal

gradient at the regrowth interface (e.g. by raising the melt temperature). Each of these should have the effect of spreading the defect trail spacing.

Conclusions

An effective production-scale SOI growth technique has been described. Those defects which still remain are trails of dislocations aligned along the growth direction. These have been examined by TEM, and shown to have nearly zero net Burgers vector content. A mechanism by which the defect trails are introduced during regrowth is suggested.

Acknowledgement

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Figures

Figure 1.

As heating strip moves to the right, polycrystalline Si layer (sandwiched between oxide layers) is melted and regrown as single crystal Si, initally seeded by substrate wafer at edge.

Figure 2.

Plan view of isolated Si layer; grown-in dislocations periodically arrayed along growth direction, usually randomly assorted (left), but occaisionally in short series of same type (right).

Figure 3.

Regrowth front is probably facetted, allowing dislocation formation along lines where cells meet.

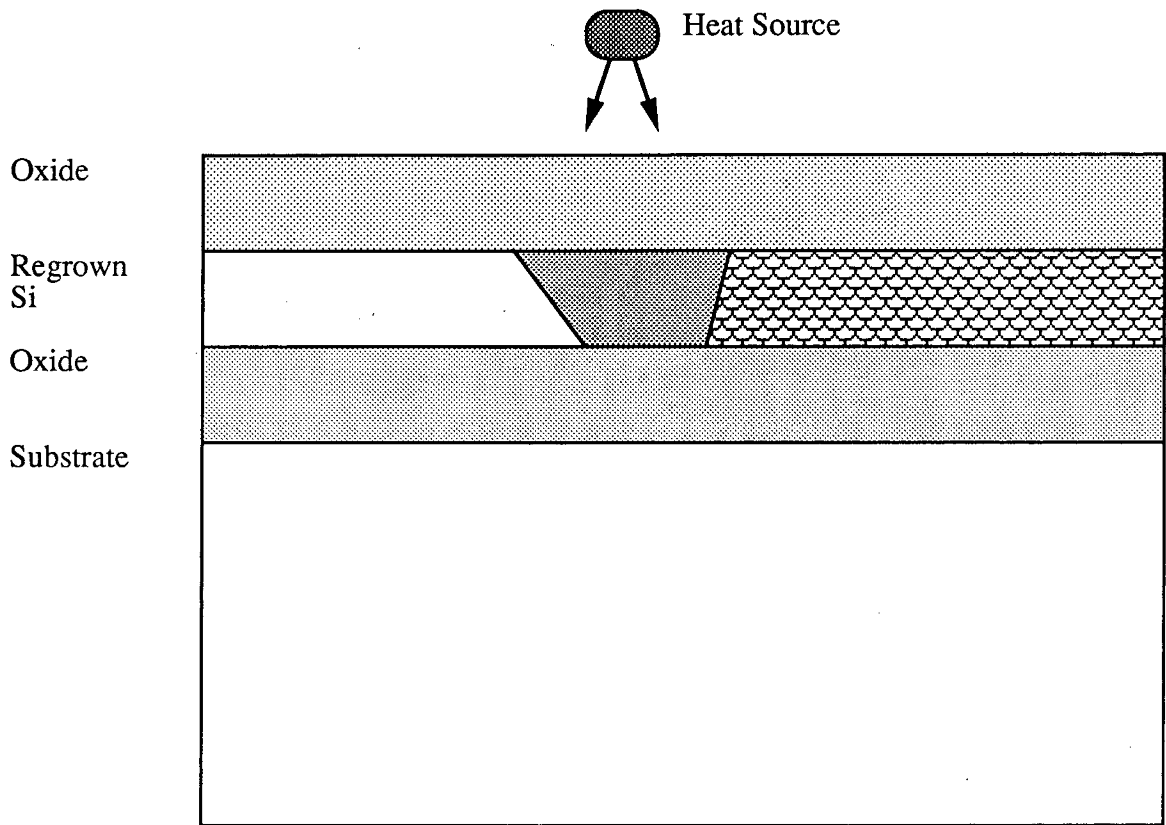
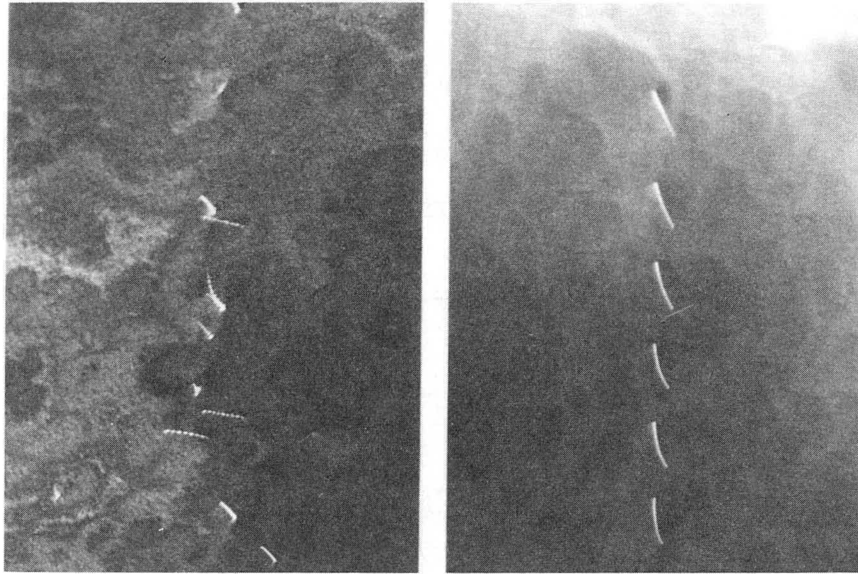


Figure 1



1.0μm

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Figure 2

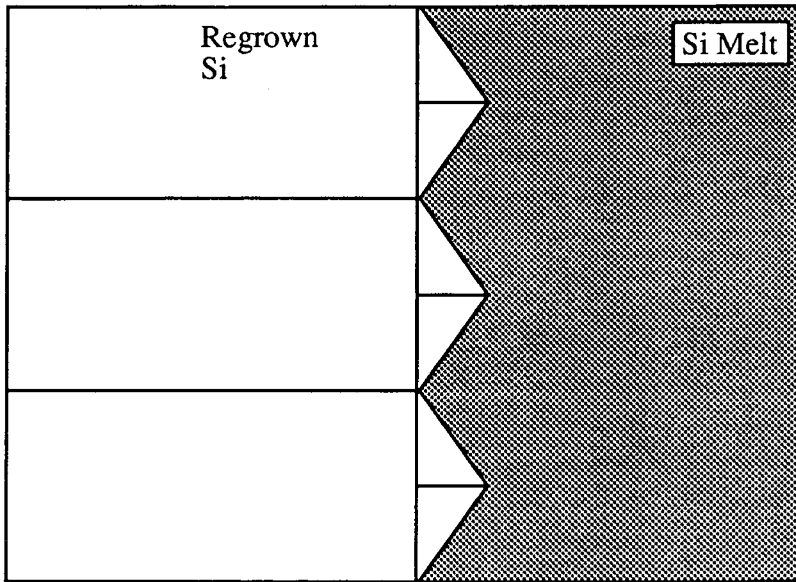

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Figure 3

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