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Authors
Ahadi, Kaveh
Shoron, Omor F
Marshall, Patrick B
et al.

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Electric field effect near the metal-insulator transition of a two-dimensional electron system in $SrTiO_3$

Kaveh Ahadi, Omor F. Shoron, Patrick B. Marshall, Evgeny Mikheev, and Susanne Stemmer[a)]
Materials Department, University of California, Santa Barbara, California 93106-5050, USA

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$SmTiO_3/SrTiO_3$ interfaces exhibit a two-dimensional electron system with carrier densities in the order of $3 \times 10^{14}\,cm^{-2}$ due to the polar discontinuity at the interface. Here, electric field effect is used to investigate an electron system at this interface whose carrier density has been depleted substantially by the gate metal and by reducing the thickness of the $SmTiO_3$. At zero applied gate voltage, the sheet resistance exceeds the quantum resistance, h/e^2, by more than an order of magnitude, and the $SrTiO_3$ channel is in the hopping transport regime. The electric field modulates the carrier density in the channel, which approaches the transition to a metal at positive gate bias. The channel resistances are found to scale by a single parameter that depends on the gate voltage, similar to two-dimensional electron systems in high-quality semiconductors. *Published by AIP Publishing.*
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Metal-insulator transitions in two-dimensional electron systems are a subject of long-standing interest in condensed matter physics.[1–4] Modulation of charge carrier densities by electric field effect is one of the main experimental methods used to study the transition. Two-dimensional electron systems at complex oxide interfaces are expected to provide both new insights and potentially new phenomena, as they exhibit, for example, various instabilities associated with magnetic or orbital order and strong coupling to the lattice. One extensively investigated two-dimensional electron system in complex oxides is that formed in $SrTiO_3$ when it is interfaced with an insulator that has a polar surface, such as $LaAlO_3$ or $RTiO_3$ (R is a rare earth ion).[5] Electric field tuning of the two dimensional electron system at the $LaAlO_3/SrTiO_3$ interface has been demonstrated and a transition between an insulating and a superconducting state was discovered.[6–9] The two-dimensional electron system at $RTiO_3/SrTiO_3$ interfaces is more challenging to substantially modulate by electric field effect, due to the much higher carrier densities, which correspond to the theoretically expected density of $\sim 3 \times 10^{14}\,cm^{-2}$ for the polar interface.[10] "Inverted" field effect devices that utilize the large dielectric constant of $SrTiO_3$ have resulted in record carrier density modulation in the order of $10^{14}\,cm^{-2}$,[11–13] which is, however, not sufficient to completely deplete the channel.

Here, we investigate a top-gated field effect device, in which $SmTiO_3$ acts as the gate dielectric and the polar $SmTiO_3/SrTiO_3$ interface provides the mobile charge in the $SrTiO_3$ channel. Figure 1 shows the heterostructure and device geometry. For very thin $SmTiO_3$ ($\sim$3 unit cells), the capacitance density is high and, more importantly, the carrier density in the channel is depleted significantly to $\sim 1 \times 10^{14}\,cm^{-2}$. A likely explanation for the reduced density is trapping by states on the polar $SmTiO_3$ surface, which is in close proximity. The carrier density in the channel systematically increases with increasing $SmTiO_3$ thickness until it reaches the full density of $3 \times 10^{14}\,cm^{-2}$ (see supplementary material). We note that the behavior is different from $LaAlO_3/SrTiO_3$ interfaces, where a critical thickness is observed.[14] However, carrier densities at these interfaces are also lower (even for thick $LaAlO_3$), so a direct comparison is difficult. The lower carrier densities allow for devices with rectifying gates. Upon further depletion of carriers by the Schottky barrier formed by a Pt gate, the carrier density in the channel falls below a critical value and transitions to an insulator. Here we investigate the transistor characteristics of these insulating channels as the applied gate voltage modulates the channel conductance.

Epitaxial heterostructures containing three (pseudocubic) unit cells (u.c.s) of $SmTiO_3$ ($\sim$1.2 nm) on a 20-nm-thick $SrTiO_3$ layer were grown by molecular beam epitaxy on a (001) $(La_{0.3}Sr_{0.7})(Al_{0.65}Ta_{0.35})O_3$ (LSAT) single crystal, as described in detail elsewhere.[15,16] Device fabrication involved conventional photolithography (lift-off) with electron beam deposition of Ti/Au (40/400 nm) and Pt (100 nm) for the Ohmic contacts and the gate metal, respectively. The Pt gate metal showed a rectifying behavior and low leakage

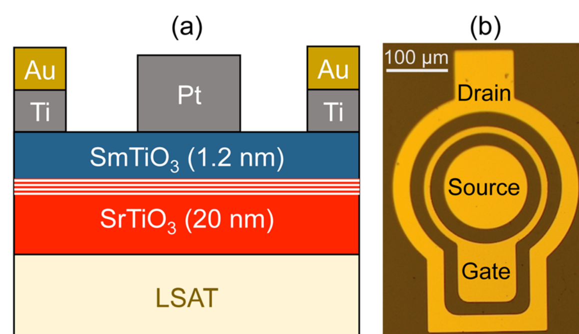

FIG. 1. (a) Schematic cross-section of the field effect device. The shaded area indicates the presence of the two-dimensional electron system at the interface. It is known that a fraction of the carriers spread over the entire $SrTiO_3$ thickness. (b) Optical micrograph of the device, showing the circular device geometry.

a)Author to whom correspondence should be addressed. Electronic mail: stemmer@mrl.ucsb.edu

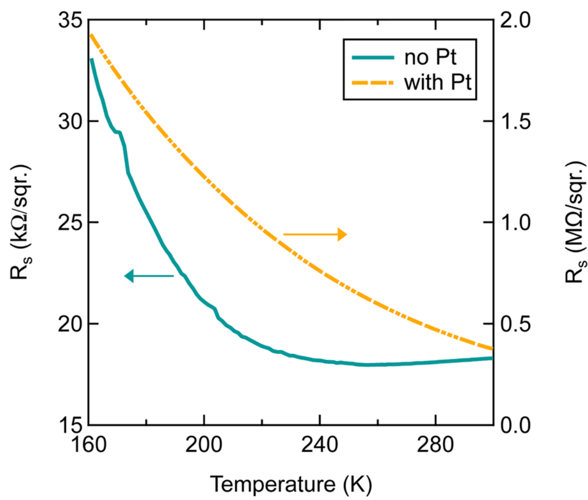

FIG. 2. Four-terminal sheet resistance as a function of temperature for $SmTiO_3/SrTiO_3$ heterostructure with 3-u.c.-thick $SmTiO_3$ with and without the Pt gate metal, respectively.

(see supplementary material). Three terminal measurements were carried out on the fabricated transistors at room temperature using an Agilent B1500A parameter analyzer, which was also used for capacitance-voltage (CV) measurements (signal amplitude 30 mV). Temperature dependent electrical measurements were carried out using a Quantum Design Physical Property Measurement System (PPMS). Four-terminal electrical measurements (Hall and sheet resistance) were carried out on square Van der Pauw structures.

Figure 2 shows the four-terminal sheet resistance (R_s) as a function of temperature for a 3-u.c.-thick $SmTiO_3/SrTiO_3$ heterostructure measured using square van der Pauw structures. After an initial measurement, Pt was deposited using a shadow mask and the measurement was repeated. Without Pt, metallic behavior is observed near room temperature and a metal-insulator transition occurs at ~260 K. Hall measurements reveal a sheet carrier concentration of $9.5 \times 10^{13}\,cm^{-2}$, which is significantly reduced from the $3 \times 10^{14}\,cm^{-2}$ carrier density observed with thick $SmTiO_3$,[10,17] and a carrier mobility of $3.6\,cm^2\,V^{-1}\,s^{-1}$ at room temperature. We note that the room temperature R_s value (~18 kΩ/□) is close to the two-dimensional Mott-Ioffe-Regel limit of h/e^2 or 25 kΩ/□, where the channel should become strongly localized (e is the elementary charge and h is Planck's constant).[18] Additional depletion of carriers should therefore result in insulating behavior even at room temperature. With a 100-nm-thick Pt layer, R_s increases by more than an order of magnitude to about 380 kΩ/□ and insulating behavior is observed at all temperatures. From the Schottky barrier, which is about 0.82 eV (see supplementary material), the maximum sheet carrier density that could ideally be depleted by the gate metal is estimated to be about $9.5 \times 10^{13}\,cm^{-2}$.

Figure 3 shows the drain current vs. drain-source voltage (I_{DS}-V_{DS}) characteristics of the transistors as a function of gate voltage (V_G) at different temperatures. At high temperatures, well-behaved transistor characteristics are observed, including cut-off, linear, and saturation regions. I_{DS} increases with temperature (it almost doubles every 100 K in saturation at $V_G = 1$ V), indicating that the channel is not metallic. At $V_G > 1$ V, gate leakage dominates the device characteristics. At lower temperatures, in particular, at negative V_G, the channel becomes too resistive, causing the observed upturn in the I_{DS}-V_{DS} characteristics which is an artifact caused by gate leakage. At negative bias, tunneling through the very thin gate barrier layer (~1.2 nm of $SmTiO_3$) causes leakage. At low temperature, the area under Pt gate becomes very

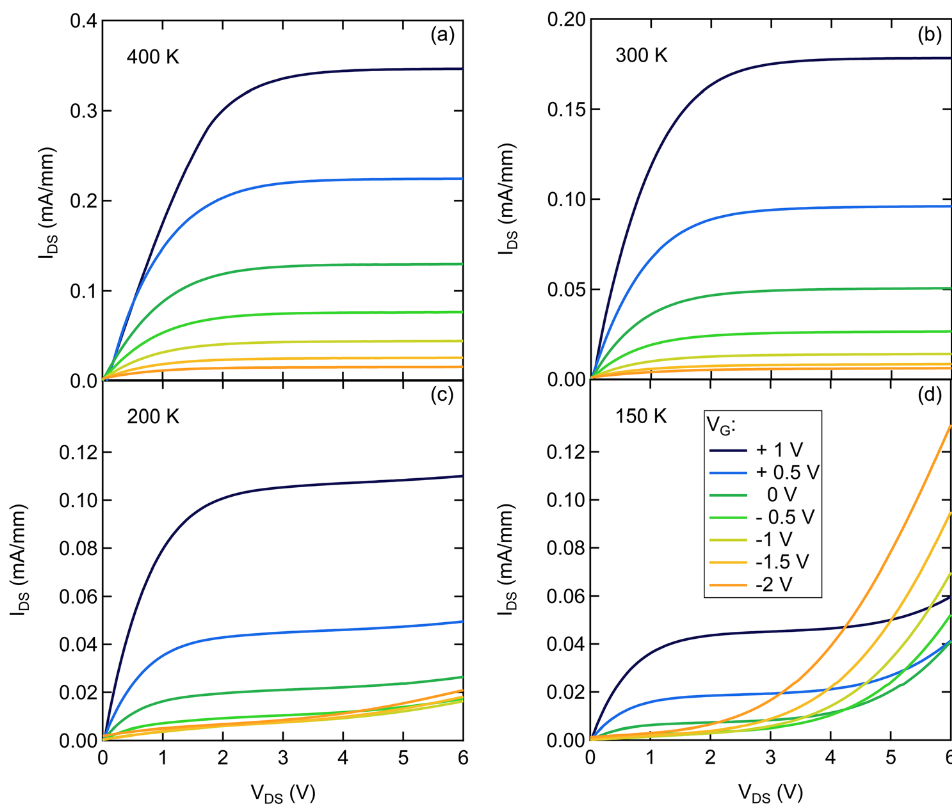

FIG. 3. Transistor I_{DS}-V_{DS} characteristics as a function of V_G at (a) 400 K, (b) 300 K, (c) 200 K, and (d) 150 K. V_G was changed from −2 V to +1 V (top curve in each panel) in 0.5 V increments. The current data is normalized to gate inner circumference.

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resistive. As the resistance under the gate increases, the voltage drop across the access region decreases and most of the voltage drops across the gate. This effectively increases the reverse electric field at the gate and results in higher leakage. In the following, we only discuss the data not influenced by gate leakage artifacts.

To estimate the charge modulated by V_G, Fig. 4 shows the frequency-dependent CV characteristics at 300 K. The capacitance density reaches a maximum of $3.5\,\mu\mathrm{F\,cm^{-2}}$ (1 kHz) and then drops mainly due to gate leakage at positive V_G. The capacitance density (and thus the modulated charge density), while high, is almost entirely limited by the quantum capacitance of the two-dimensional electron system and any unintentional layers at the *ex-situ* deposited interface between the $SmTiO_3$ and the Pt gate[19] and not by the gate capacitance. The capacitance roll-off with increasing frequency is a consequence of the high channel resistance. Integration yields a carrier modulation of $\sim 3.6\times10^{13}\,\mathrm{cm^{-2}}$ for a V_G sweep from -1.5 V to $+0.5$ V. While it is consistent with the capacitance density, it is much less (by a factor of almost three) if the I_{DS} modulation within the same V_G range would be ascribed to a modulation of *only* the carrier density. This suggests that V_G substantially modulates not only the carrier density but also their mobility. The transconductance of the device as a function of V_G at $V_{DS} = +6$ V is presented in the Supplementary Material. Leakage dominates the transport characteristics at $V_G > 1$ V. Accordingly, transconductance drops, and I_{DS} is almost independent of the gate voltage.

Figure 5(a) shows the sheet resistance estimated from the low V_{DS} (linear) region as a function of temperature as V_G is changed between -1.5 V and 0.5 V. The sheet resistance was estimated by modeling the I_{DS}-V_{DS} characteristics at $V_{DS} < 0.5$ V using the known I_{DS}-V_{DS} relationship (see e.g., Ref. 12) and the geometry of the device. While the results are order of magnitude estimates only (the sheet resistance estimated in this way is a factor of five higher than that determined by the four point probe measurement) the data should at least reflect the general trends. From Fig. 5(a), we see that an insulating behavior is observed at all V_G. At

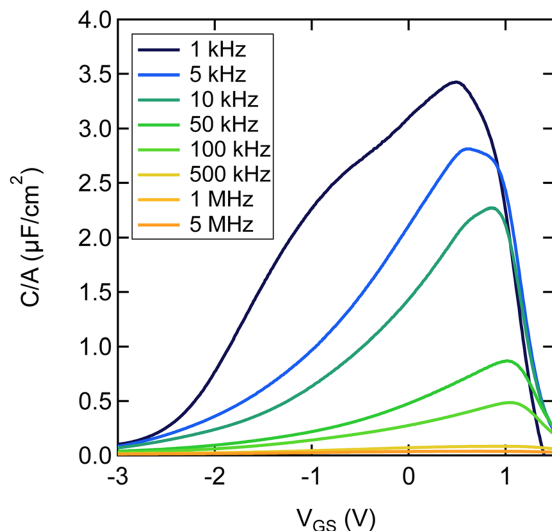

FIG. 4. Frequency-dependent CV characteristics at 300 K.

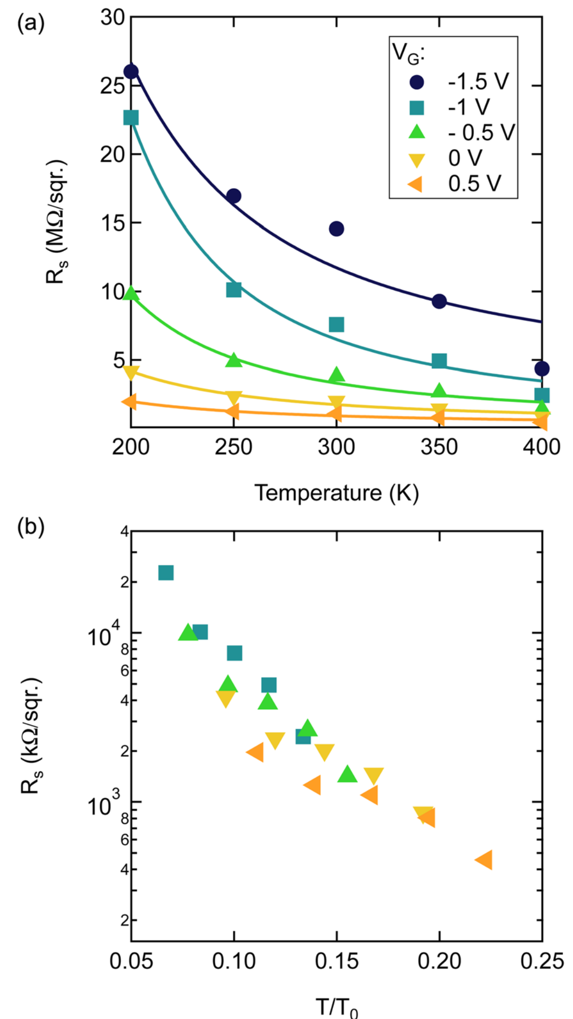

FIG. 5. (a) Sheet resistance as a function of temperature at different V_G extracted from the low V_{DS} characteristics shown in Fig. 3. The solid lines are a fit to a variable range hopping law. (b) Data in (a) as a function of a scaled temperature T/T_0, where T_0 is the energy scale in the variable range hopping law, which systematically shifts with V_G. Data at $V_G = -1.5$ V is not shown in (b) because of the scatter in the data [see (a)], which produced an unreliable fit. It could, however, also be brought into overlap with the other curves by adjusting T_0.

$V_G = 0.5$ V, the channel is almost metallic and the sheet resistance is almost independent of temperature. Thus, the positive V_G brings the channel close to a metal-insulator transition. To drive the system across the transition, higher positive gate voltages would have to be applied, but gate leakage becomes too high.

To summarize, the results show that the electric field effect tunes the two-dimensional electron system in $SrTiO_3$ that is deep in the insulating phase ($R_s > 380\,\mathrm{k\Omega/\Box}$) *near* the transition to a metal (R_s becomes almost temperature-independent), which occurs near the quantum limit, $R_s \sim h/e^2$ [see Fig. 2]. The behavior can be compared with that of the field effect devices with $LaAlO_3/SrTiO_3$ interfaces and with two-dimensional electron systems in semiconductors. Electric fields have been shown to modulate the channel conductance at metallic $LaAlO_3/SrTiO_3$ interfaces at very low temperatures,[8] mainly because the electric field modulates the spatial distribution of carriers, which affects the mobility at low temperatures when it is dominated by interface roughness scattering.[8] For the insulating $SmTiO_3/SrTiO_3$ interfaces

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studied here, the resistance modulation is due to the proximity to the metal-insulator transition. The trends in the sheet resistance characteristics (Fig. 5) are remarkably similar to those found for high-quality, two-dimensional electron gases in Si on the insulating side of the quantum phase transition,[20,21] although the temperatures here are orders of magnitude higher. In particular, the sheet resistances in Fig. 5(a) can be made to overlap by scaling the temperature (T) axis by a characteristic temperature T_0, as shown in Fig. 5(b). T_0 was obtained from fits to a variable range hopping law, $R_S \sim \exp[(T/T_0)^{-\alpha}]$, see solid lines in Fig. 5(a). The exponent α depends on the nature of the hopping, dimensionality, and the Coulomb gap.[22,23] We used $\alpha = 1/4$ (three-dimensional Mott variable range hopping) but using a different α did not affect the qualitative results, only the absolute values for T_0. The systematic scaling of T_0 with V_G likely reflects the divergence hopping length, as expected near the metal-insulator transition.[23,24] This further confirms the interpretation that the gate voltage tunes the channel in proximity to the metal-insulator transition.

The differences in the characteristics of *metallic* two-dimensional electron systems in $SrTiO_3$ with thick $SmTiO_3$ capping layers, which have the full carrier density of $3 \times 10^{14}\,cm^{-2}$, should be noted. These electron systems have room temperature sheet resistances and mobilities of $\sim$2000 Ω/sqr. and $\sim 9\,cm^2\,V^{-1}\,s^{-1}$, respectively.[10] The high R_s observed here even without Pt (Fig. 2) is due to a reduction in carrier density *and* mobility, each by about a factor of three. A possible explanation for the lower mobility is the depletion of higher mobility electrons in $d_{xz,yz}$-derived subbands, which are higher in energy and further away from the interface than electrons in the strongly confined d_{xy}-derived subbands, which are expected to scatter strongly from the interface and surface.[25] Additional reduction in mobility is also expected from scattering from defects on the nearby $SmTiO_3$ surface or the LSAT substrate, as the lower density system is also more poorly confined[26] and from the uncompensated polar charge at the $SmTiO_3/SrTiO_3$ interface.

See supplementary material for leakage current data, carrier density as a function of $SmTiO_3$ thickness, and transconductance data.

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