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Silicon carbide technologies for interfacing with the nervous system

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Silicon carbide technologies for interfacing with the nervous system

by

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Abstract

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In the past couple of decades we have seen remarkable advances in the integration of biological systems with artificial ones. Our knowledge of both of these worlds has grown exponentially, and in particular our knowledge of the human body. In recent years we have been able to understand and treat diseases we never thought we would, and we have even been able to interface with the body to restore lost functions. Direct interaction with the human brain to read and write information to it has been achieved thanks to the development of neural probes. The work presented in this thesis focused on improving the performance of such probes in regards to their operational lifetime. This work begins with a description and demonstration of how silicon carbide technologies are suitable and compatible with neural probes, and is a better material choice for device insulation. Then, a fabrication method for silicon carbide based electrode arrays is presented, in which conductive silicon carbide is integrated with insulating silicon carbide to form an electrode architecture in which the only exposed material is the superior silicon carbide. Following this, *in-vivo* demonstration of these silicon carbide based electrode arrays is done by recording from the nervous system of an animal model.

This dissertation is dedicated to my wife, with whom I have shared this whole journey.

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Acknowledgments

To my wife, many thanks for being my companion during these years of grad school. This experience was definitely made easier by being able to share the challenges with her and by counting on her unconditional support. I am grateful for all the smiles and happiness she has brought into my life. I look forward to enjoying many more years of curiosity for the world out there with her.

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Chapter 1

Introduction to neural probes

1.1 Advances in brain-machine interfaces

In recent years we have seen remarkable advances in the integration of artificial devices with the human body. A prime example of such advances is the development of tools that directly interact with the nervous system enabling applications that range from the treatment of diseases to restoration of function[11, 22, 34]. In a beautiful example of what the collision of engineering and neuroscience can accomplish, one of the first devices to show the impressive ability of the human brain to integrate signals produced by external devices and restore auditory function was the cochlear implant; speech sounds encoded in electrical stimulation in the cochlea were received and interpreted by the brain allowing deaf patients to hear again[11, 45]. Equally impressive are the results of using deep brain stimulation to treat diseases affecting the nervous system like Parkinsons[29], or more recently to treat neuropsychological disorders like depression and schizophrenia[32]. In the last few years patients with tetraplegia have been able to use the thoughts to move robotic arms and feed themselves[22], or interact with computers to type on a screen[28, 6]. And the most recent demonstration if this integration is that of a patient with spinal cord injury who, after several years with complete lack of movement, was able to move his own arm, grasp and feed himself by means of electrode arrays implanted in his brain and electrical stimulation of the muscles in his arm and hand[5].

The applications described above, and many others, have been enabled through the use of electrode arrays that record and stimulate neural activity[39]. These electrodes in particular are implanted directly within brain tissue to allow maximal recording and stimulating resolution. While these devices come in many forms and shapes, they all have the common goal of accurately recording, or stimulating, the electrical signals generated by the brain while minimizing the negative impact that the foreign object may have in the tissue around it. To accomplish this goal microfabrication techniques have been used to make devices whose size more closely compares to that of neurons, though still significantly larger in some cases. Some examples of such devices are microelectrode or "Utah" arrays[33], microwire

electrodes[33], planar arrays or "Michigan" probe[23], microelectrocorticography (μECoG) arrays[26] and, most recently, carbon fibers[38]. Within each of these examples there is a myriad of materials that have been tested to ultimately create a system with adequate functionality and operational lifetime. The latter has been a particularly challenging problem that this thesis work has attempted to solve.

1.2 Failure modes of neural probes

Several types of neural probes have been used in the past few decades, mostly in animal research. Many authors have comprehensively studied the performance of these devices and determined many of their failure modes[42, 2, 25]. Failure of neural probes occurs when electrodes stop recording or stimulating meaningful signals, which may happen when the electrode themselves degrade or when the electrodes induce neuronal death or neuronal migration[13, 24]. There are three main categories under which most failures fit: Surgical procedures, biological response and material failure.

Failure due to surgical procedures

The first of these categories, surgical procedures, includes all failures of the devices during implantation as well as failure due to external factors that arise as a result of surgery. For some neural electrodes in particular, breakage of the recording elements may occur during implantation as well as breakage of the interconnects between electrodes and external connector[2]. However, a more significant problem in this category is the creation of routes for infection due to these same interconnects; these are usually passed through a hole in the skull bone in a manner that the external connectors can be accessed from outside the skin. In animal research this is a very significant problem because animals are not particularly worried about cleanliness around these exposed areas. Additionally, if these systems were to be translated to humans in their current state, people would be significantly impeded to perform certain activities that could increase the chance of infection, similarly to having to care for an open wound.

Other failure modes that apply both here and in the next category are surgery complications due to excessive bleeding and the speed at which electrodes are embedded in the brain[4]. Bleeding can be caused by electrodes stiff enough to pierce through vein walls or can come from other tissues like the dura matter.

Failure due to biological response

Failures due to biological response have been perhaps the major driver for most of the development of neural probes in recent years. The need for materials and device form factors that seamlessly integrate with the body has motivated the creation of thin film flexible devices that more closely match the natural behavior of the brain[39, 27].

The first element to consider in biological response is the effect of the body's immune system on a foreign object (e.g. electrodes). Depending on the material the electrodes are coated with and depending on the size of the electrodes, glial encapsulation may occur[13, 24]. This glial encapsulation significantly reduces the signal to noise ratio (SNR) of the recorded signals because neurons of interest are pushed away from the recording sites[41, 24]. Materials with poor biocompatibility and neural electrodes with large cross sectional area are more susceptible to encapsulation[37]. When neural encapsulation does not occur, however, material choices may still cause neuronal death or migration. In particular, it has been observed that silicon, silicon dioxide and silicon nitride based neural probes continuously release silicon in the microenviroment around the electrodes, resulting in a reduced number of neurons remaining in close proximity to the recording sites[16].

The last component of this category is perhaps the most closely related to probe design. For many years neural probes were fixed or tethered to the skull and the effects of brain micromotion were neglected[3]. In large species like non-human primates (NHP) and humans, the brain may move by tens of microns with the heart pulsation and breathing[19], not to mention external impact to the skull. This continuous motion of the brain tissue relative to the fixed implant results in a continued activation of the immune system and destruction of the tissue around the electrodes, once again diminishing the signal quality. Increased incidence of glial encapsulation has also been observed in implants that lack the flexibility to move with the brain.

Failure due to material degradation

Beyond the failure modes described above, material integrity is perhaps the ultimate factor determining the operational lifetime of a device. Once acute responses to the foreign object have ceased, the neural electrodes are left in an environment traditionally very harsh for electronic devices; salts are just one example of one of the elements present in bodily fluids that efficiently corrode electronic devices quickly (consider dropping a cell phone in sea water). Material degradation is observed in neural electrodes in two ways, insulation failure and delamination of heterogeneous materials[40, 18, 25].

Insulation failure happens when the dielectric that encapsulates conducting elements becomes faulty due to the presence of pinholes, cracking or thinning. All materials commonly used for insulation of neural probes have been observed to behave in this manner both *in-vivo* and *in-vitro*[12]. Parylene, for example, in films of 10μm or thicker presents longitudinal cracks when explanted from NHP, and presents high leakage currents in accelerated longevity tests[18, 46]. Similarly, silicon dioxide and silicon nitride quickly dissolve in bodily fluids as observed in planar array implants in rodents[25]. Finally, polyimide films present two main problems, they ought to be significantly thick (>4μm) in order to be pinhole free and they lack a conformal deposition method, which is important for proper coverage of the elements to be insulated[12]. The use of polymers as only insulation has an additional problem: molecular diffusion through the polymer matrix. Parylene and polyimide, for example, allow water and other molecules to reach the inner layers of the electrode structure,

creating eruptions at the interface between the conductor and the insulator These eruptions may cause electrical shorts between the electrodes or complete exposure of the conducting element to the exterior.

The second problem in material degradation is the long term stability of the interface between the conducting element and insulation at the recording (or stimulating) sites; this interface is exposed to the biological fluid by design. When this interface is composed of heterogeneous materials, not only must each of these materials be immune to degradation but the adhesion mechanism between those two (or more) materials must be at least equally robust. For example, when parylene is used as insulation two adhesion mechanisms may be observed: chemical bonds through an adhesion promoter consisting of a silane chain and an oxygen bond and mechanical interlock due to surface roughness. In both of these cases, direct exposure of the interface to aqueous environments results in breaking of the oxygen bond and the silane chain, or diffusion of molecules through the gaps between the two materials due to the lack of chemical bonds, leading to delamination[18]. In the case of polyimide, the adhesion mechanisms are mechanical interlock and carbide formation with transition metals; mechanical interlock of polyimide films is very weak: a common method used to release polyimide films from silicon carrier wafers is to immerse the sample in water, which diffuses through the interface between the polymer and the carrier (or through the polymer matrix itself), allowing easy peel off of the films. The formation of carbides with transition metals is in principle a very strong bond, but these carbides have been observed to rapidly hydrolyze in aqueous solutions[1]. These failure modes have been extensively observed in *in-vivo* implants; the interface of tungsten-polyimide in microwire arrays rapidly degrades due to dissolution of tungsten[42], and parylene delaminates at the recording sites in silicon based microelectrode arrays[18, 2, 7].

1.3 Progress towards long lasting materials for neural probes

Of the failure modes described above, surgical procedures and biological response have been largely solved by improved surgical practices and by smarter design of the neural probes themselves. In particular, the introduction of miniaturized, highly flexible electrodes with flexible interconnects has resulted in improvement of the body's acceptance of neural implants[37], and recent developments and on going efforts towards fully wireless technologies will move towards infection free systems. In the following paragraphs I will describe some of the progress towards solving the material degradation issues and how silicon carbide fits very well in this spectrum.

A first example, is the alumina/Parylene-C bilayer being developed for microelectrode arrays, which to this date remain the most used neural implant in NHP and is one of the few systems with FDA approval for use in human patients. This bilayer consists of a 50nm alumina layer deposited by atomic layer deposition (ALD) directly on the silicon surface of

the electrodes, followed by chemical vapor deposition (CVD) of a 6μm thick layer of Parylene-C[46]. Alumina has been shown to be an excellent moisture barrier, solving one of the main polymer failure modes, molecular diffusion[10]. This material stack significantly improves insulator lifetime when compared to Parylene-C-only insulation test structures[46]. This has been shown through accelerated aging tests by soaking test devices in phosphate buffered saline (PBS) at elevated temperatures and using electrochemical impedance spectroscopy (EIS) to test for proper insulation. The authors of these studies found that the thickness of each of the two components of the bilayer determine the longevity of the films; more interesting is that the degradation of the outer parylene layer still occurs, so the ultimate lifetime is dependent on how long will it take for the bodily fluids to create cracks in the parylene and reach the alumina, which will then degrade[35]. A more significant problem with this system is the exposed interface of silicon - alumina - Parylene-C at the recording (or stimulating) sites. Delamination of the encapsulating layer occurs due to degradation of the adhesion promoter used between alumina and Parylene-C and due to degradation of ALD alumina in environments at 100% humidity[35, 7]. Finally, miniaturization of electrodes insulated by this bilayer is limited to encapsulated films totaling at least 12μm thick, which is more than the ideal thickness for electrodes that may bypass the body's immune system.

A second example of a multilayer approach for long lasting insulation is the use of polyimide with sputtered or PECVD amorphous silicon carbide (a-SiC) as an adhesion layer between the metal and the polymer[36]. The goal of this approach is to combine the formation of metal silicides between the metal and the a-SiC and the formation of carbon bonds between the a-SiC and the backbone of the polymer. The integrity of the exposed interface at the recording (or stimulating) site depends on the stability of the silicide that forms; in addition, the stability of the exposed a-SiC and its carbon bond with the polymer must be sufficient to prevent delamination of the polymer, as long as the metal silicide does not break. The weakness of this system lies in the fact that it still relies on polyimide as insulation; thin films (<2μm) of polyimide have pinholes in the as-coated state[12], and more defects form with aging. When these defects appear in the polymer, the underlying a-SiC film is exposed. Although good dielectric a-SiC films may be deposited, sputtered films used as adhesion layers are too thin (less than 100nm) to provide good insulation due to low sheet resistivity and high pinhole density (More details of sputtered a-SiC will be discussed in Chapter 2).

The third, and last, example in this section is the use of transferred thermal oxide films to encapsulate thin film neural probes[12]. This is a promising solution for a particular subcategory of implants. This method employs thermal oxide films to encapsulate thin film devices from the bottom and the top; devices are fabricated directly on a thermally grown film of silicon dioxide, and are capped on the top by transferring and glueing a thermal oxide film grown on a separate wafer. This method effectively prevents molecular diffusion through the thermal oxide films, hence protecting the actual device from the aging effects of the bodily fluids. The authors of this study demonstrated the stability of the thermal oxide films through accelerated aging tests, and estimated a time to failure at body temperature of about seventy years. There are three main limitations of this method: 1) transfer of thin films in microfabrication is usually avoided due to the complexity and low reliability of this

process. 2) transfer of thin films does not allow the presence of significant topography on the neural device. 3) Electrode miniaturization is hampered due to the lack of encapsulation of the side walls.

1.4 The scope of this dissertation

In the past decade we have expanded our understanding of how the body, and specifically brain tissue, responds to the presence of neural implants. With this knowledge, a new generation of more brain-like devices has been developed. Examples include devices so small as to cause minimal tissue damage when implanted and bypass the immune system, or highly flexible devices that move with the brain. However, solving the failures due to material degradation remains an open challenge in neural engineering.

This dissertation work focuses on finding a practical solution to the failure of neural implants due to material degradation, with regards to both failure of the insulation and faulty interfaces at the recording or stimulating sites. Such a solution requires both materials with improved stability and a reliable and accessible fabrication process. The materials of choice must not degrade and must have properly sealed interfaces, must be flexible and very thin, must provide adequate insulation or conduction as necessary, must be biocompatible, must be compatible with current microfabrication processes and scalable, and must accept the conditions of accelerated aging tests. The final devices must be mechanically sound so they can be handled by a person or a machine, and must be customizable and able to be miniaturized.

The purpose of this thesis is to describe the development of a silicon carbide electrode array. In the following pages I will explore the properties of silicon carbide as demonstrated in the literature and make a case for why this is a suitable material for neural implants. Then I will show how we have the ability to deposit films with these properties in our facilities while explaining what the failure modes for other silicon carbide films are. I will then continue to introduce the fabrication method that I developed and show the devices made. And finally, I will demonstrate that these silicon carbide based devices are suitable for neuroscience experiments involving the central and the peripheral nervous system.

Chapter 2

Silicon carbide is suitable for neural probes

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2.1 Chapter overview

This chapter presents a discussion and validation of the potential of silicon carbide as a material for neural probes. It begins with a general description of the material properties and deposition methods in section 2.2. Then section 2.3 presents our findings of the effects that different deposition parameters have in the quality of the films. Finally, section 2.4 presents a demonstration of the long term stability of our insulating films.

2.2 Validation of silicon carbide as material suitable for neural probes

To recapitulate from the previous discussion, the ideal material for the development of neural probes has the following characteristics: chemically inert, biocompatible, good molecular barrier, flexible, high resistivity if used as insulation, high conductivity if used as conductor, and compatible with standard silicon microfabrication techniques. In the next paragraphs I will discuss examples from the literature showing that silicon carbide (SiC) combines all of these characteristics.

The chemical inertness of SiC is a property that arises from the surface chemistry of the films[31]. In polycrystalline SiC every silicon atom is bound to a carbon atom, all the way from the surface down to the bulk of the material. This bond is particularly strong and does not break even at elevated temperatures. In addition to its stability, this bond is also very short, which prevents molecules from diffusing through the top surface of the films reaching structures in the bulk of the material. This chemical inertness is evidenced in the fact that there are not known wet etch chemistries that can etch SiC at room temperature. Similarly, SiC is used as protective coating in some rocket elements susceptible of reaching temperatures about 1000^oC in order to prevent corrosion[21]. SiC is also used for various sensing applications including operation in highly corrosive environments[31], such as bodily fluids would be.

SiC is also a biocompatible material as a result of its chemical inertness[15, 16]. Due to the stability of the bonds in this material, silicon atoms remain in the SiC film. Counter examples of this phenomenon are silicon dioxide and silicon nitride; these two materials have significant dissolution rates in aqueous environments that result in the continuous bleed of silicon in the microenvironment around the film that would activate an immune response[25, 12]. Biocompatibility of SiC has been tested *in-vitro* and *in-vivo*; cell cultures show better growth, coverage and adhesion on surfaces coated with SiC when compared to other silicon based materials, and show similar behavior when compared to other bicompatible materials like gold[9, 14]. *In-vivo*, stiff silicon pieces implanted in the brain are better accepted by this tissue when they are coated with SiC; pieces without the encapsulation tend to cause glial scarring while pieces with SiC allow neural processes to grow on them[15, 16].

Like many other materials in the thin film regime, SiC is very flexible. Polycrystalline SiC films of 2μm have radii of curvature as low as 150μm and amorphous SiC (a-SiC) films

of similar thickness have been shown to be flexible as well[17, 47]. In our experience, the flexibility of thin SiC films is high enough that devices can curl on themselves without creating cracks in the ceramic.

In terms of electrical conductivity, SiC is a semiconductor. This means that the material can be doped with impurities to achieve sheet resistivity as low as 2mΩ.cm[30] or can be deposited in the amorphous state and achieve sheet resistivity as high as $10^{13}\Omega$.cm[8]. There are several examples that replace the use of polysilicon for doped SiC in the fabrication of transistors, or that use doped SiC as conducting element for the realization of microheaters for gas sensing[43, 20]. Similarly, SiC films have been used as main insulation in some electrode arrays for *in-vitro* experimentation with neuronal circuits.

Finally, the compatibility of SiC with standard silicon microfabrication processed is the last piece of the puzzle that truly makes this material a candidate for neural probes and many other devices[31]. Deposition of SiC can be done by low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD) or physical vapor deposition (PVD), the three of which are standard tools in many fabrication facilities. Similarly, patterning of SiC can be done by reactive ion etching (RIE) with chemistries similar to those used for etching silicon; fluorinated gases or chloride chemistry etch SiC. The lack of a wet chemistry for etching of SiC is perhaps the one difference between SiC and silicon processing, but at the same time that is what makes SiC so attractive.

2.3 Development of insulating and chemically inert SiC films

Most of the outstanding properties of SiC have been demonstrated for the polycrystalline versions of the material. In fact, many of these properties arise as a result of the bond structure that generates the crystallinity; in 3C-SiC every silicon atom has four bonds with carbon atoms and every carbon atom has four bonds with silicon atoms, meaning that every single bond in this crystal is of superb stability. This phenomenon, in combination with the fact that residually doped polycrystalline SiC is not resistive enough to serve as insulator, poses a significant challenge in developing good insulating SiC films; insulating SiC need be amorphous films, which alters the stoichiometry and chemical bond composition.

Polycrystalline SiC and sputtered a-SiC are poor insulators

In our experience, polycrystalline SiC is not a suitable insulator because of practical limitations related to the equipment available and considerations regarding scalability of the process. Deposition of crystalline SiC structures requires high process temperature, in the vicinity of 800^{o}C. At this temperature, impurities easily incorporate and diffuse in the films which results in the deposition of residually doped SiC, rather than undoped SiC. There are some reports showing that it is possible to deposit the latter, but such demonstrations require very clean furnaces that can only accommodate small samples and exotic precursors,

and such furnaces are exclusively dedicated to deposition of undoped films. This limits the scalability to wafer level fabrication process. An additional, and more fundamental limitation, is the potential for doping by diffusion of these SiC insulating films during their high temperature deposition on other doped or conducting elements. An example of this scenario is that in our final devices there would be a need to deposit an insulating layer on metal interconnects. We also observe dopant diffusion from the carrier wafer into the 'undoped' SiC. The alternative to polycrystalline SiC is amorphous SiC (a-SiC). The two most common methods used to deposit such films are sputtering, or PVD, and PECVD.

Sputtering of SiC can be done in two ways: co-sputtering using a silicon target and a carbon target, or sputtering with a single target of SiC. The latter option is highly preferred and the following description of sputtered films applies when a single target is used. The chemical composition of sputtered films usually replicates that of the target because the plasma necessary for the deposition is generated with inert gases like argon. In this manner, there is no, or almost no, incorporation of impurities in sputtered SiC films. Additionally, the energy used in the sputtering process removes SiC molecules off the target as opposed to single silicon or carbon atoms, resulting in films with almost perfect stoichiometry. This chemical composition translates in superb chemical resistance; sputtered a-SiC does not etch in any commonly used etchant for silicon based materials like HF, KOH or XeF_2, or other strong chemicals like those used in hot piranha or aqua regia. Figure 2.4 shows some sputtered SiC films that have been subject to etching in XeF_2 but films thickness did not change. The failure mode of sputtered SiC films deposited at room temperature for the purpose of insulating material for neural probes is low sheet resistivity and high pinhole density. Sheet resistivity of these films is typically in the range of $10^6\Omega$.cm, which is too low for a good insulator. Resistivity tends to increase by one or two orders of magnitude after annealing in inert atmosphere, but is never high enough. Presence of pinholes is a more delicate problem for insulators meant to be used in aqueous environments; sputtered SiC films of up to 700nm deposited on doped silicon carriers have high density of pinholes as evidenced by the low DC resistance measured between the silicon carrier and a small drop of saline placed on the thin film.

PECVD a-SiC films are good insulators

The last option for achieving highly resistive a-SiC films is PECVD. Similar to the PVD films described above, PECVD of SiC can be done using a single gas precursor providing the SiC molecule, or can be done by using separate precursors for the silicon and the carbon atoms. Unlike PVD, however, the preferred method here is to use separate precursors. There are three big challenges to overcome in the deposition of SiC by PECVD: hydrogen incorporation, stoichiometry and pinhole density. The following paragraphs describe a systematic characterization of the deposition parameters used in the Oxford Plasmalab System 100 in the Marvell Nanofabrication Laboratory at UC Berkeley. The goal of this study was to find the optimal recipe that can deposit a-SiC films that are good insulators in dry and wet conditions without sacrificing chemical inertness. The PECVD system here uses two

precursor for SiC deposition, methane and silane, and has choices of nitrogen, argon and hydrogen as carrier gases. It has three power generators, one low frequency (50-460kHz) and two high frequency (13.56MHz and 81MHz), and a heated chuck. In this manner, the space of parameters explored includes precursor flow rates and ratios, carrier gas choice and flow rate, generator choice and power, process pressure and table temperature. Recipes with deposition rate below 5nm/min were discarded because they were impractical to characterize and would add significant delays to a high throughput fabrication process. The following subsections describe the main findings of this exploration.

Chamber cleanliness and conditioning

PECVD systems are often used for deposition of multiple materials that use many kinds of gases. Additionally, many chemistries are used to clean the chamber and prevent deposited materials from building up on the chamber surfaces. For proper recipe repeatability it is crucial to guarantee that start conditions of the chamber are always the same. Consequently, the deposition chamber is always cleaned for at least 30min with a combination of CF_4 and N_2O using the 13.56MHz and low frequency generators, prior to the deposition of the first sample of each session. After cleaning, the chamber is allowed to reach pressures below 5e-6 Torr and then coated with 500nm of SiC. Deposition of SiC on actual samples is performed after the chamber had been conditioned and it had been evacuated to pressures below 1e-6 Torr. Once wafers are brought inside the chamber and it has been flushed out with argon, the chamber is evacuated to pressures below 5e-6 Torr just prior process gases start to flow. With this cleaning protocol recipe repeatability is confirmed by depositing a standard recipe at the beginning of each session.

Use of 81MHz generator results in higher deposition rates and lower leakage current

Precursor dissociation is significantly more efficient when the 81MHz high frequency generator is used. This is evidenced by the three to five times faster deposition rates when compared to deposition rates with the 13.56MHz generator. Refractive index of films is still dominated by the precursor ratio, which means the 81MHz generator provided similar films to the 13.56MHz generator but deposited at a faster rate. Leakage current at room temperature are significantly lower for films deposited using the 81MHz generator compared to the 13.1MHz generator. Selectivity of Si to SiC in XeF_2 does not depend on the generator used.

Deposition rate saturated at 250W using 81MHz generator

Three levels of power for the 81MHz generator were tested 100W, 250W and 350W, recipes 7, 3 and 45 of table 2.1, respectively. For a fixed precursor flow rate the deposition rate is higher for 250W than 100W, but it is the same for power of 250W and 350W. Refractive index is the same for these three recipes. Leakage currents for films deposited at 100W and 250W are the lowest, and effectively zero when films are 1000nm thick. For a 1000nm film

deposited at 350W, leakage current is about 1nA/cm^2 at room temperature and increases with temperature to above 100nA/cm^2 as temperature rose to 90^{o}C. We think this is evidence of pinholes in the film, as opposed to chemical etching, suggesting that deposition power too high has a detrimental effect in insulating properties of the film. The film deposited at 100W has the most silicon-carbon bond content while the film deposited at 250W has the fewest. All three films have comparable carbon-hydrogen and silicon-hydrogen bond content (fig. 2.5a).

Use of low frequency generator results in higher pinhole density

Using the low frequency generator consistently results in films with higher pinhole density as evidenced by high leakage currents at room temperature of all films deposited in this manner. These films have reduced silicon-carbon bonds content compared to films in which low frequency is not used. In the contrary, films in which low frequency is used have lower carbon-hydrogen and silicon-hydrogen bond content (fig. 2.5b). Use of low frequency generally has a positive effect in reducing etch rates of SiC films in XeF_2.

High precursor flow rates reduce pinhole density

Several of the recipes tested used very low precursor flow rate in an attempt to reduce the amount of impurities incorporated to the films. However, the low deposition rates that result generate films with high pinhole density; these pinholes propagate as the film gets thicker resulting in films with high leakage current even at thickness of 1000nm. In contrast, high precursor flow rates in combination with the 81MHz generator described above result in very high deposition rates and pinhole density that rapidly decreases as the film goes from 100nm to 400nm to 1000nm.

Hydrogen dilution reduces hydrogen incorporation in the film

Use of hydrogen dilution reduced the amount of carbon-hydrogen bonds in the films compared to argon diluted precursor (fig. 2.5c). In addition, the content of silicon-carbon bonds is slightly higher when the hydrogen dilution is used. Etch rates in XeF_2 of SiC deposited with hydrogen dilution are very low for most films tested.

High chuck temperature significantly improves film quality

The absorption spectra of the films deposited at 350^{o}C and 200^{o}C suggest they have similar bond compositions, but the film deposited at lower temperature has more carbon-hydrogen and silicon-hydrogen bonds and fewer silicon-carbon bonds (fig. 2.5d). Still, the film deposited at lower temperature behaves like a perfect insulator at the beginning of the aging test even at high temperature. The low Si-C bond content and higher hydrogen content of this film, however, may explain the poor long term performance in the accelerated aging test; leakage current of the film deposited at 200^{o}C increases to very high levels after 18h of

ageing, while the film deposited at 350^{o}C lasts more than 600h.
While the film deposited at low temperature performes poorly in the aging test, the deposition rate of >70nm/m would allow for deposition of films tens of microns thick in which removal of impurities might not result in a direct open pinhole through the entire film, or in which removal of all impurities might take several decades when implanted in the body.

2.4 Demonstration of long term stability of insulating a-SiC films

Active accelerated aging tests of insulating SiC films demonstrate the long term reliability of this material. Traditionally, these tests consist of immersing the material to be tested in PBS and maintaining the solution at elevated temperatures. In the case of neural probes, these tests are most often passive; there is no use of electrical potential during the aging tests, except for when impedance of the electrodes is measured. This passive test is not realistic because neural electrodes implanted in the body are subject to continuous electrical potential, especially in the case of stimulating electrodes. In our tests, in addition to the heated solution, we apply a constant DC bias across the insulating film. By measuring leakage currents in this manner we are able to continuously monitor the insulating properties of the films and quantitatively determine the exact moment when they fail. In addition to leakage current, the chemical inertness of the films in the aging solution is verified by the lack of change in film thickness. I was able understand the effects of a large matrix of PECVD parameters that influenced the behavior of insulating SiC for neural electrodes by building a system that can test several films in parallel while subjecting them all to the same conditions.

Active accelerated aging test set up for thin films

The method for accelerated aging tests used here was inspired by the work of Fang et al.[12], in which they use leakage currents to quantitatively determine the time to failure of insulating films. The method consists on depositing the films to be tested directly on a conductive substrate and creating a sealed chamber on top of the thin film to contain the aging solution; a DC bias is applied between the aging solution and the conductive substrate, and the system is then heated up to temperatures up to 96^{o}C. When leakage currents across the thin film go above a predetermined threshold, the film is considered to have failed.

The system used for this dissertation work is shown in Figure 2.1. Thin films are deposited on doped silicon wafers and a chamber made out of polydimethylsiloxane (PDMS, Sylgard 184 silicone elastomer, Sigma-Aldrich) is bonded to the thin film by oxygen plasma. The samples are placed on an aluminum plate and fixed using stainless steel screws and plastic washers; mechanical fixing is important for proper electrical contact between the silicon and the metal plate. Each sample has a platinum wire pierced through the PDMS that connects to one of sixteen inputs of a digital multiplexer through a resistor; the electrical circuit then consists of a series connection between the silicon wafer, the thin film, the aging solution, the

platinum wire, the resistor and the DC power supply. In order to measure the leakage current, a multimeter is used to measure the voltage drop across the resistor; one terminal of the multimeter is connected to the common output of the multiplexer and the second terminal is connected to the common node of the resistors, which is also the positive terminal of the power supply. Each one of the sixteen inputs of the multiplexer connects to the node connecting each platinum wire coming from the sample and each of the sixteen resistors. This system is automated using a Raspberry Pi and a custom Python script; the I/O pins of the Raspberry Pi are used to select the input of the digital multimeter, the script then synchronizes this selection and commands the multimeter to take the measurement. These data are stored in text files. The system is control with the custom graphical user interface shown in Figure 2.2.

Molds to create the PDMS chambers are designed in Autocad Illustrator (Autodesk Education licensing, San Rafael, CA, USA) and 3D printed in ABS plastic (uPrint plus, Stratasys, Eden Prairie, MN, USA), shown in Figure 2.3. The molds resemble a cup with a small column inside of it attached to the base. The column has a cross sectional area of $1cm^2$, which is the same amount of area to be exposed to the aging solution in the films. In this manner, the measured current is already normalized to an area of $1cm^2$. 3D printed items have textured surfaces with longitudinal groves that result from the way the filament is lay down during printing; this groves transfer to the PDMS and would act as fluidic channels if not properly sealed. The PDMS cups are thus created in a two step process: uncured PDMS is poured in the plastic mold and allowed to cure overnight at 50^oC on a hot plate. After the mold is removed by breaking it, the PDMS cup is placed on a leveled surface such that the opening of the chamber is facing up, then a small quantity of uncured PDMS is poured on the surface of the PDMS cup to be contacted with the thin films and allowed to level itself by gravity. PDMS cups ware then placed on a hot plate set to 100-120^oC for 1h (Actual temperature around the uncured PDMS is about 80^oC).

Thin a-SiC films are more stable than thin thermal oxide films

Thin a-SiC films 150nm or less in thickness were compared side by side to 100nm thermal oxide films. Both types of films are deposited on p-type silicon wafers. Non-zero leakage currents at room temperature are measured for all of these a-SiC, with significant increments due to temperature effects as shown in Figure 2.6. However, for most films the leakage current remains stable at the same value through the entire duration of the experiments, and returns to low values when the sample is cool down to room temperature. In contrast, thin thermal oxide films act as a perfect insulator at room temperature and at high temperatures at the beginning of the experiment, but for all samples tested, there is complete failure of the insulation in less than 3h.

After the aging test of these thin films is complete (16 to 24h of aging), the PDMS chamber is removed from the sample in order to assess how the aging solution affects the film. For most a-SiC films tested, the films are visually intact; the color of the film exposed to the solution is exactly the same as the color of the film outside of the chamber, indicating

complete lack of etching. Ellipsometry confirmed minimal change in thickness of the aged films. In contrast, thermal oxide films etch in the aging solution at rates of at least 70nm/day. In some cases, the oxide film is completely removed and the silicon carrier is exposed. Optical images of aged films are shown in Figure 2.7.

The failure mode of thin a-SiC in leakage current tests is the high density of pinholes present in the film. To confirm this hypothesis two experiments were performed: 1) Deposit a 100nm a-SiC film on 100nm thermal oxide and perform the accelerated aging test. If there are pinholes in the carbide film, then the expected time to failure of this sample is the same as a 100nm thermal oxide without the carbide film on top. 2) Deposit a 1000nm a-SiC and perform accelerated aging test. If non-zero leakage currents in the 100nm film are due to low resistivity of the a-SiC, then leakage currents of the 1000nm a-SiC should be about 1/10th the leakage current of the thinner film. If the magnitude of the leakage current of the thicker film is similar to that of the thinner film, that suggest there is a direct interaction of the solution with the silicon carrier through pinholes in the films. These experiments were performed using recipe 29 of table 2.1 and the results are shown in Figure 2.8 and support the idea of pinholes in the a-SiC film. It is worth noting that non of these films had visual damage as a result of the aging test.

Thick a-SiC films are stable insulators

The only failure mode found in thin insulating a-SiC films is the presence of pinholes in the as-deposited state. What this means is that the magnitude of the leakage current of these films remains largely stable through out the accelerated aging experiments. The alternative to this scenario is that leakage currents through thin films increase as impurities embedded in the film are removed by the aging solution creating new pinholes. Since this is not observed in our experiments, depositing thicker a-SiC films is an effective way to decrease the pinhole density; the aging process will not create new defects in the film so leakage currents will not increase over time.

a-SiC films 1000nm thick were deposited on n-type silicon wafers with recipes 3 and 7 in table 2.1 and accelerated aging tests performed on them. As shown in Figure 2.9, one of these samples maintains leakage currents below 1nA/cm^2 for more than 600h and the other one for up to 1500h. In addition, the failure of the first sample does not occur as a result of the effect of the aging solution, rather dielectric breakdown occurs due to high transitional voltages when some connections were made with the power supply on. Even when this happens, the leakage current of this sample is about 2nA/cm^2 and is below 100nA/cm^2 when the experiment was terminated. This sample is also cosmetically intact as shown in Figure 2.9 and the change in thickness measured by refractometry is negligible.

In contrast to the long term stability of silicon carbide, all thermal oxide films fail the leakage current test as it was expected. Fang et al.[12] found that 1000nm thermal oxide films have significantly high leakage currents after about 200h of aging at 96^{o}C and in our experiments 850nm SiO_2 films fail at about 160h (Figure 2.9). Figure 2.10 also shows how these films are clearly etched by the aging solution.

High chuck temperature significantly improves film quality

Chuck temperature of 350^{o}C significantly improves the lifetime of the a-SiC over a film deposited at 200^{o}C. A 1000nm film deposited with recipe 3 maintains leakage currents below 1nA/cm^2 for over 600h at high temperatures while a 1000nm film deposited with recipe 47 maintains zero leakage current for only 18h. The latter film, however, initially behaves like a perfect insulator both at room temperature and at >90^{o}C and after 24h of aging the color of the film exposed to the PBS does not have an observable change suggesting that the failure mode is removal of impurities that results in exposure of pinholes. The results of this aging test are shown in Figure 2.11.

Table 2.1: Recipe matrix of PECVD SiC.
HF=13.56MHz and VHF=81MHz.

No	Ar	H2	CH4	SiH2	Pressure	LF	HF	VHF	Temp	Rate	RI
	sccm	sccm	sccm	sccm	mTorr	W	W	W	°C	nm/m	
1	500	0	60	7.5	1400	0	250	0	350	12	2
2	500	0	60	3.8	1400	0	250	0	350	7.6	1.92
3	500	0	60	7.5	1400	0	0	250	350	46	1.85
5	500	0	60	7.5	1400	200	0	0	350	11	2.21
6	500	0	60	7.5	1400	0	250	0	350	5.6	87
7	500	0	60	7.5	1400	0	0	100	350	36	1.82
8	67	0	8	1	1400	0	0	250	350	7.3	1.78
9	500	0	8	1	1400	0	0	250	350	6.5	1.64
10	500	0	8	1	1400	200	0	250	350	6.35	1.63
11	0	180	8	1	1400	0	0	250	350	2.2	1.74
12	0	180	8	1	1400	100	0	250	350	5	2.1
13	180	0	8	1	1400	100	0	250	350	5.5	1.61
14	0	180	8	1	1400	100	0	350	350	5	2.45
15	0	180	8	1	1400	300	0	350	350	6.2	1.7
16	0	180	8	1	1400	0	0	350	350	5.1	1.88
17	0	180	8	1	1400	350	0	350	350	5.9	1.9
18	0	180	8	1	1400	300	0	400	350	5.5	1.7
19	0	180	8	2	1400	300	0	350	350	11.5	2.12
20	0	180	8	1	1400	0	0	400	350	5.5	1.79
21	0	180	8	1	700	0	0	350	350	4.8	1.72
22	0	180	8	1	1400	300	0	350	350	5.7	1.77
24	0	180	8	3	1400	100	0	350	350	12.1	2.16
25	0	180	8	3	1400	0	0	350	350	12.1	2.15
26	0	180	24	3	300	100	0	350	350	5.8	2.5
27	0	180	24	3	300	0	0	350	350	9.75	2
29	0	180	16	2	300	100	0	350	350	5.85	1.93
30	0	180	24	2	300	0	0	350	350	8.1	1.67
31	0	180	16	2.7	300	100	0	350	350	6.7	2
32	0	180	24	2	300	100	0	350	350	5.7	1.83
33	0	180	8	2	300	100	0	350	350	5.5	1.96
34	0	180	16	4	300	100	0	350	350	9.5	2.11
35	0	180	4	2	300	100	0	350	350	4.2	1.94
36	0	180	16	2	300	0	0	350	350	7.4	1.7
38	0	180	12	1.5	300	0	0	350	350	5.4	1.64
39	0	180	16	2	300	0/100	0	350	350	4.5	1.84
40	500	0	60	7.5	1400	100	0	250	350	40	1.89
41	0	180	60	7.5	1400	0	0	250	350	22	2.08

No	Ar	H2	CH4	SiH2	Pressure	LF	HF	VHF	Temp	Rate	RI
42	500	0	16	2	1400	0	0	250	350	16	1.63
43	500	0	60	7.5	500	0	0	100	350	23	1.92
44	500	0	60	7.5	1400	25	0	250	350	43	1.83
45	500	0	60	7.5	1400	0	0	350	350	45	1.84
46	500	0	60	12	1400	0	0	250	350	67	1.87
47	500	0	60	7.5	1400	0	0	250	200	77	1.66
48	500	0	60	7.5	1400	100	0	250	200	69	1.68

2.5 Chapter figures

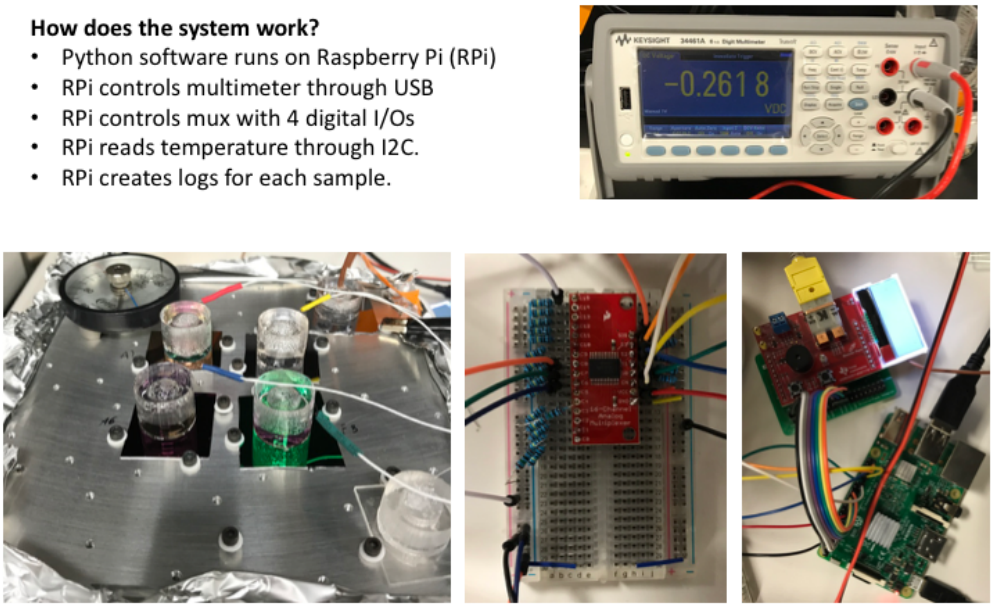

Figure 2.1: Set up for active accelerated aging of thin films. The system uses a power supply to continuously apply a DC bias between PBS and a silicon wafer which are separated only by the thin film to be tested. Leakage current through the film is measured by measuring the voltage across a resistor in series with the film. A Raspberry Pi computer (Bottom right) is used to communicate with the multimeter (Top right) to make and store voltage measurements for each of the films being tested. The Raspberry Pi uses a digital multiplexer (Bottom center) to connect the multimeter probe to several thin films. Aging samples are placed on an aluminum plate on a hot plate (Bottom left).

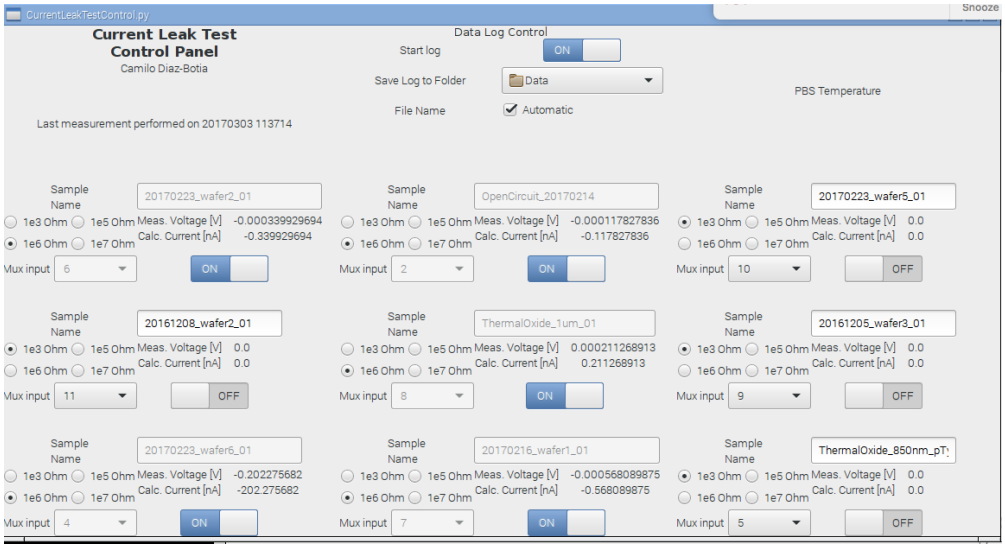

Figure 2.2: A custom graphical user interface writen in Python is used to control the active accelerated aging system. The GUI allows to assign a name and a multiplexer input to each of the samples as well as choosing the multiplexer inputs to be measured. The program can store all the data, which include voltage measurements, temperature and time stamps.

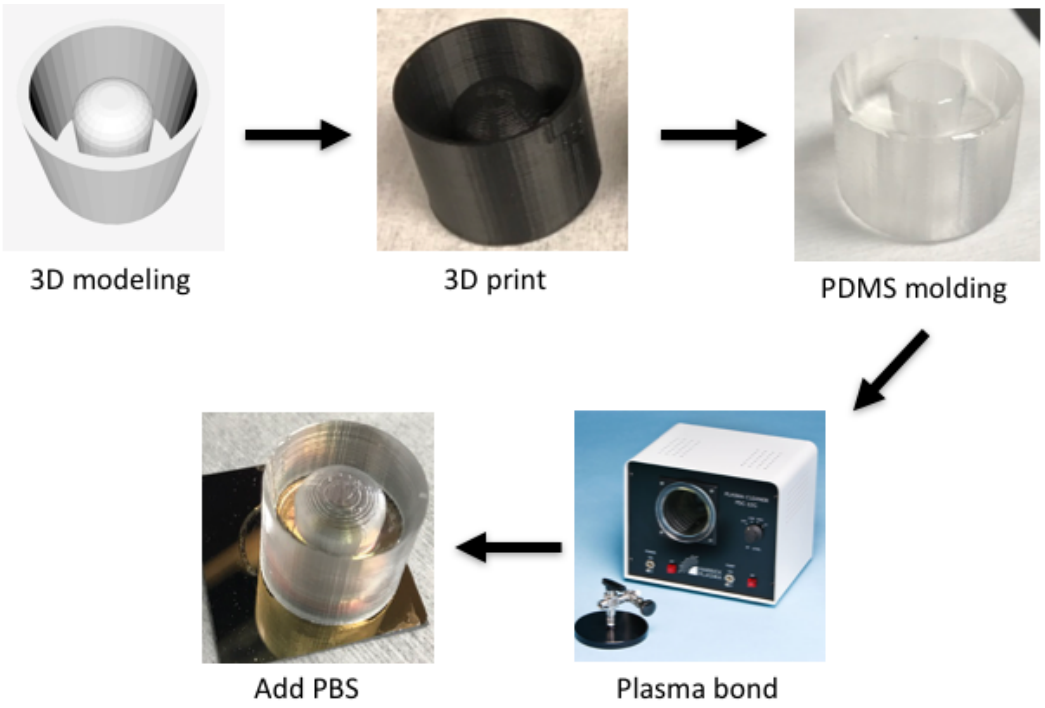

Figure 2.3: PDMS chambers for active accelerated aging tests were custom designed can fabricated. First, a 3D model of the chamber is created in a computer and then 3D printed in ABS plastic. PDMS is prepared in a 1:10 ratio, poured into the plastic mold and fully cured at temperatures below 65^{o}C. Then, the plastic mold is broken and the PDMS chamber released. Finally, the chamber is permanently bonded to the thin film by oxygen plasma activation.

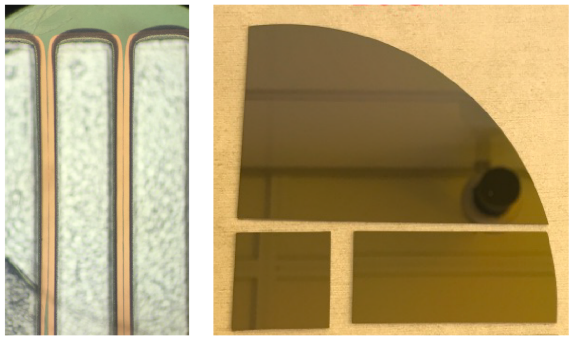

Figure 2.4: Chemical inertness of sputtered silicon carbide is evidenced by the lack of etching in XeF_2. The photo on the left shows that silicon underneath the 50um wide sputtered SiC features is being selectively etched; the SiC left is of uniform color which means it is not being etched. The photo on the left shows that the piece of wafer etched in XeF_2 is indistinguishable from the pieces that were not etched (substrate was a 6" silicon wafer).

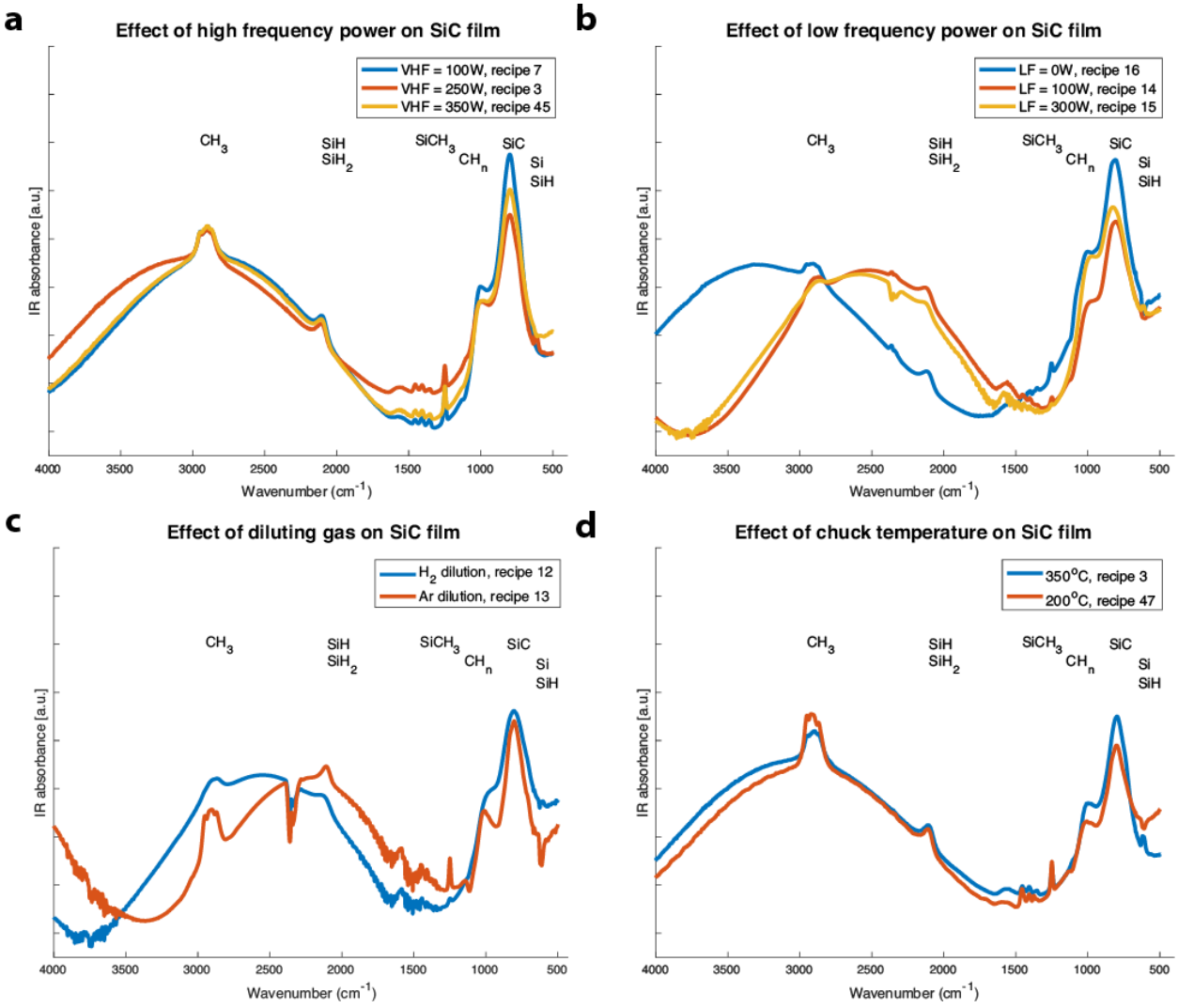

Figure 2.5: FTIR spectra of multiple a-SiC films. a) Effect of high frequency power in bond density. Film deposited at 100W has the highest Si-C peak while the Si-H_{1-2} and C-H_3 have little change. b) Effect of low frequency power in bond density shows that use of low frequency decreases the amount of Si-H_{1-2} and C-H_3 at the expense of reducing the height of the Si-C peak. c) Effect of gas dilution showing that hydrogen dilution reduces Si-H_{1-2} and C-H_3 content without harming the Si-C_{1-2} content. d) Lower deposition temperature results in reduced Si-C bond content and increased C-H_3 content

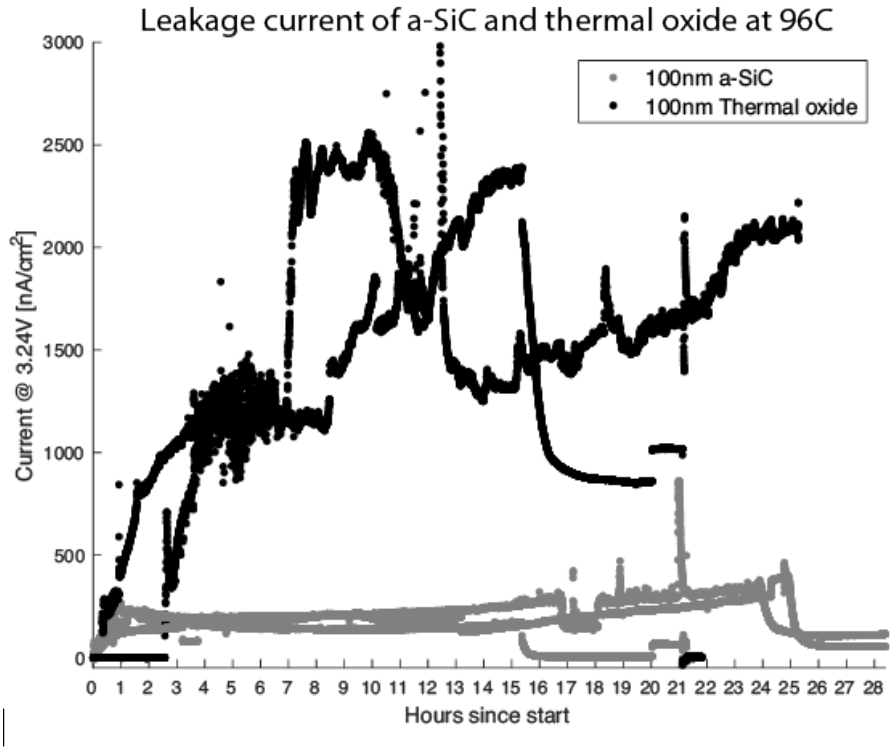

Figure 2.6: Leakage current of a-SiC and SiO_2 films 100nm in thickness on p-type silicon wafers. Leakage current of a-SiC increases at the beginning of the experiment as a result of temperature increase and then is maintained at about the same level for up to 15 hours. Leakage current of these films returns to low levels upon cool down. Leakage current of thermal oxide films starts at zero independent of the temperature but rapidly increases to very high values at about 3 hours or less and does not return to zero upon sample cool down.

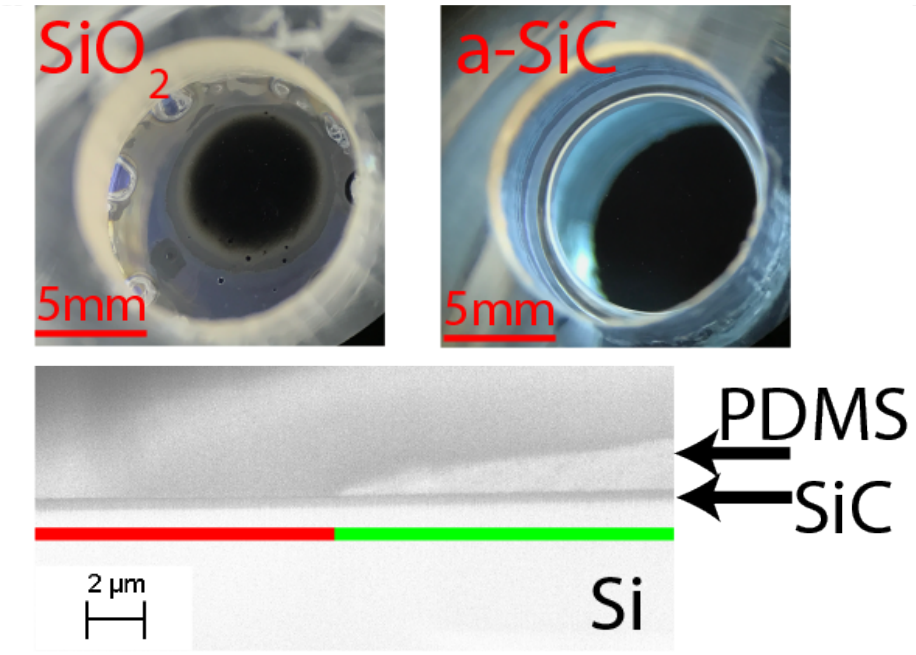

Figure 2.7: Silicon carbide films do not dissolve during accelerated aging tests in PBS. Top left shows a what used to be a 100nm thermal oxide film but after 24h of accelerated aging the film has been dissolved and left the silicon carrier exposed. Top right shows a 100nm a-SiC film aged for 24h that has not changed in color and still looks uniform and pristine. Bottom shows an SEM cross sectional image of a 450nm a-SiC aged for 280h; the thickness of the film exposed to the aging solution (red line) is the same as the thickness of the film protected byt the PDMS chamber (green line).

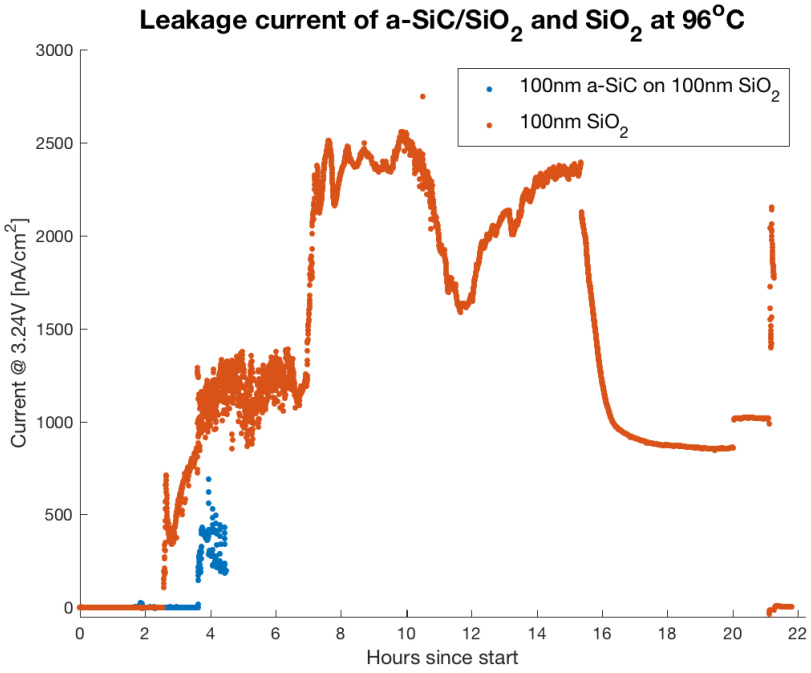

Figure 2.8: Evidence of pinholes in thin a-SiC films. When a-SiC are as thin as 100nm the presence of pinholes explain the leakage current through the film. When a 100nm a-SiC film is deposited on 100nm thermal oxide, the time to failure is about the same as the time to failure of just 100nm thermal oxide. This suggest that the aging solution has access to the thermal oxide under the a-SiC right from the beginning through pinholes.

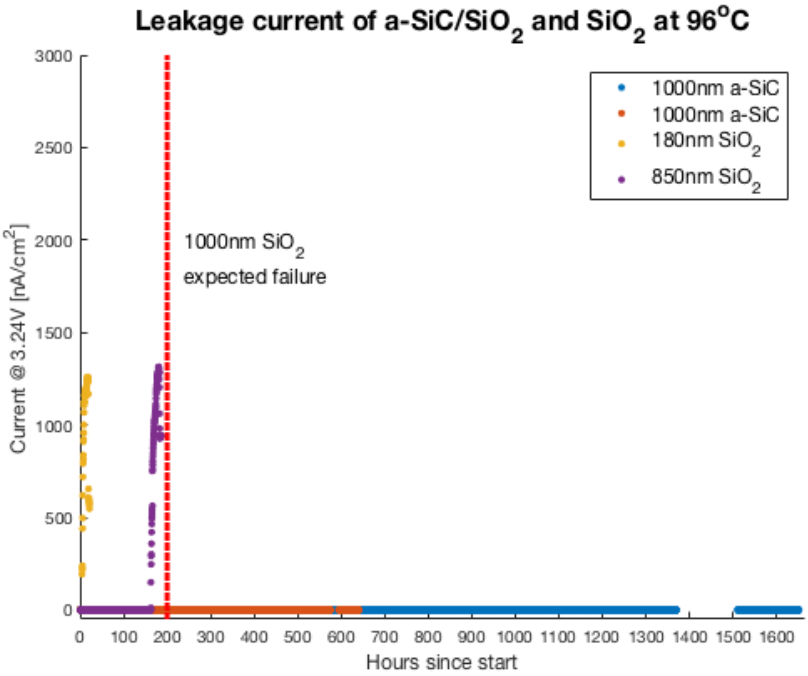

Figure 2.9: Thick a-SiC films are pinhole free and stable. a-SiC films 1000nm in thickness maintained leakage current below 1nA/cm^2 for up to 1500 hours while thermal oxide films of comparable thickness failed in less than 200h.

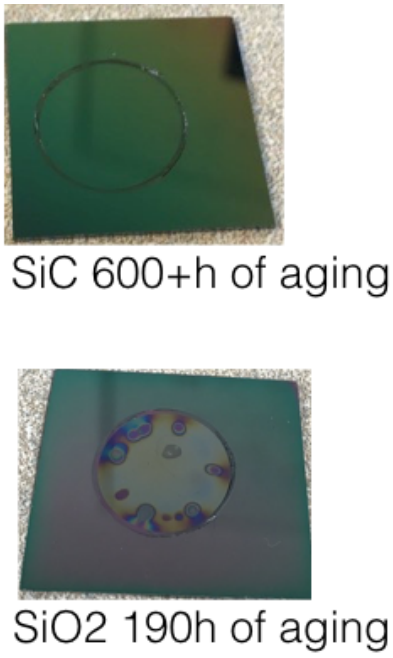

Figure 2.10: Silicon carbide films do not dissolve during accelerated aging tests in PBS. Top photo shows a 1000nm a-SiC film aged for more than 600h that has not changed in thickness; the color of the film exposed to the aging solution (area inside the circle) is the same as the color of the film not exposed (area outside the circle). Bottom photo shows a 850nm thermal oxide film aged for 190h that has been clearly degraded by the aging solution. Area within the circle in each image is $1cm^2$.

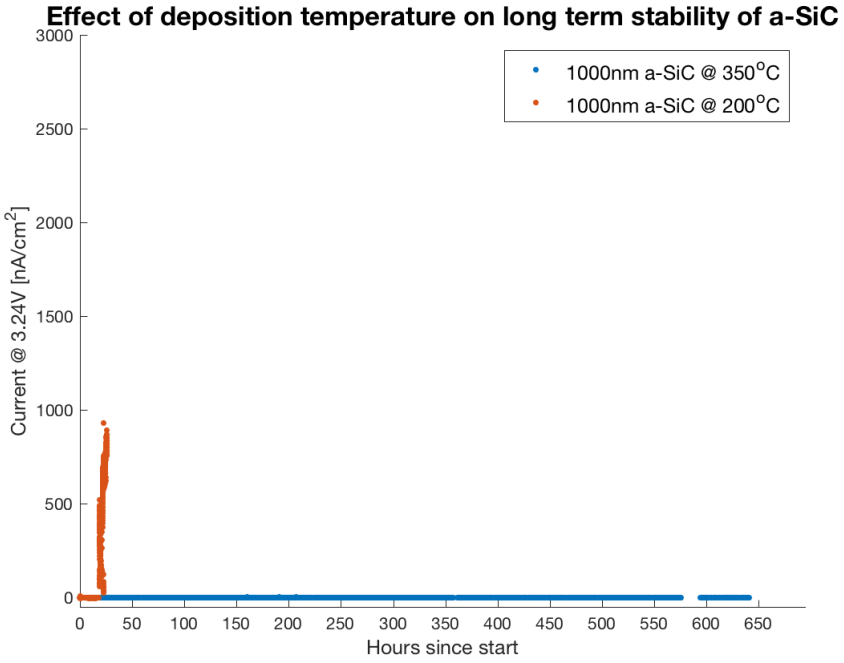

Figure 2.11: Higher deposition temperature has a beneficial effect in the long term stability of a-SiC films. While a film deposited at 350^{o}C can maintain negligible leakage current for more than 600h, a film deposited at 200^o fails the test within 24h of active accelerated aging.

Chapter 3

Device design and fabrication method for silicon carbide based devices

Adapted with permission from:
Diaz-Botia, C., Luna, L., Neely, R., Chamanzar, M., Carraro, C., Carmena, J., Sabes, P., Maboudian, R., and Maharbiz, M.
A silicon carbide electrode technology for the central and the peripheral nervous system.
J. Neural Eng. (2017) DOI:10.1088/1741-2552/aa7698

3.1 Chapter overview

This chapter presents the design and fabrication of silicon carbide based electrode arrays. In section 3.2 the designs of devices included in the lithography masks are briefly discussed. Then, the development of our fabrication method along with discussion on failure modes are discussed in section 3.3. Finally, section 3.4 describes early versions of the silicon carbide based devices and lessons learned from those processes.

3.2 Device design

The main goal of the work described here was the development of electrocorticography (ECoG) arrays for rodents. The active area of the arrays have 64 or 32 recording sites 40μm in diameter at a 200μm pitch. The interconnect between each recording site and the bondpad is a trace of 20μm in a serpentine pattern; the purpose of this feature is to allow the thin traces to slightly stretch or shrink, a concept borrowed from flexible electronics. This feature is particularly useful when the electrodes are placed on a backing layer that is elastic itself. An additional benefit of traces with this pattern is that the stress of the thin films is not aligned in a single direction, which prevents the traces from excessive curling that could lead to cracking when they are forced to conform to a surface. A draw back of this trace design is that the length of the conductor is about three times larger than that of a design with straight traces. In order to minimize track resistance, and therefore thermal noise, the cross sectional area of the metal trace is made larger to compensate for the effect. Here, platinum traces 100nm thick and 8μm wide are used to achieve thermal noise of about 1μVrms, which is smaller than the noise of commonly used pre-amplifiers.

The bondpad area is designed to be integrated with a printed circuit board (PCB) with anisotropic conductive film (ACF, 3M Anisotropic conductive film 7379). In order to guarantee good yield with this assembly method, bondpads have a pitch of 200μm and their dimensions are 150μm in width and 2.85mm in length. The actual bond area depends on the ACF bonding equipment and the film used; bond area of these devices is 0.3mm^2 which is significantly larger than the minimum area required for the film used guaranteeing good bond yield. Doped SiC bondpads were confirmed to bond properly to the PCB.

In addition to the rodent ECoG arrays, a larger ECoG array suitable for larger species like non-human primates was design, as well as a linear array meant for intracortical recordings. The CAD designs for all of these devices are shown in Figure 3.1.

3.3 Detailed description of fabrication method

The fabrication method developed in this dissertation is divided in three major components: Definition of conductive SiC features exposed to the exterior of the electrodes embedded in insulating SiC, definition of metal interconnects completely embedded in SiC, and electrode

array release. The following sections will describe each of these component in detail, along with observed failure modes and alternative processes tested in this work.

Creating conductive SiC features embedded in insulating SiC

Deposition of doped SiC requires the use of high process temperatures of about 800^{o}C. The reason for this is that molecular diffusion through the SiC matrix is very slow, requiring *in-situ* doping during deposition of the film, which uses thermal energy for the dissociation of the gas precursor. The need for high temperature requires that the conductive features of the devices be deposited before the insulating SiC; the high resistivity of a-SiC relies on the amorphous morphology of the film, and high temperature anneal of such an structure would cause crystallization of the matrix reducing the sheet resistivity. Additionally, impurity diffusion would occur during the crystallization process of the a-SiC further reducing the resistivity.

A schematic of the first stage of the fabrication process is shown in Figure 3.2, the first step in the fabrication process of SiC based devices is the deposition of doped SiC (n-SiC). This film can be deposited directly on silicon carriers, or on oxidized silicon carriers. The advantage of depositing directly on silicon is that upon device release, the conductive SiC features will be exposed and the devices ready to use. The disadvantages, however, are reduced control on the overetch step during patterning of the n-siC due to faster etch rates of silicon over SiC and direct exposure of the SiC features during device release in XeF_2. In the case of deposition of n-SiC on oxidized wafers (1000nm of thermal oxide), the advantages are the presence of a buffer layer between SiC and XeF_2 during device release and good etch selectivity of SiC over SiO_2, while the disadvantage is the need for an HF dip after device release; some backing layers might not be compatible with this acid as will be mentioned later. Regardless of these disadvantages, devices have been successfully fabricated with both alternatives of this n-SiC deposition step.

Silicon wafers 6" in diameter are cleaned with the following procedure: Piranha bath at 120^{o}C for 10min, followed by a rinse in 18MΩ water, immersion in 1:10 HF at room temperature for 1min, a rinse in 18MΩ water and spin drying. If a thermal oxide is desired, it can be now grown by dry or wet oxidation following standard procedures. Deposition of n-SiC is done by low pressure chemical vapor deposition (LPCVD) using methylsilane (CH_6Si) as as Si-C source, dichlorosilane (SiH_2Cl_2) as source of silicon, ammonia (NH_3) as source of nitrogen for doping and hydrogen as diluting gas, with flow rates of 30sccm, 15sccm, 2sccm and 48sccm, respectively. Process pressure is set 170mTorr and temperature is 800^{o}C[30]. Deposition rate for this conditions depend on the wafer location in the furnace tube and is typically around 40-50Å/min with better than 2% uniformity. The target thickness of this carbide layer depends on the desired thickness of the insulating carbide; both thicknesses should be the same.

The second step of this stage is to deposit an oxide film that will act as separator between the n-SiC features and the a-SiC films that will be conformally deposited at a later stage. This oxide film can be a low temperature oxide (LTO) or a PECVD oxide film. The advantage

of the former is that several wafers can be deposited at the same time, allowing for high throughput. The thickness of this film is determined by the SiC:SiO_2 selectivity and the uniformity of the plasma etch of SiC; the oxide film has to be thick enough to prevent etching of the n-SiC features during etch of the a-SiC layer (This will be clearly explained in the next paragraphs). Typical thickness of this oxide layer was 500nm. The actual thickness of this film is measured on every wafer as knowing this value is important for calculation of the thickness of the insulating layers.

Features in the n-SiC/LTO stack are patterned using g-line photoresist (PR) and standard photolithography techniques. For a stack of carbide less than 1000nm and oxide less than 500nm, 2μm of photoresist are enough to withstand the etches as long as the photoresist is hard baked in a conventional oven or an UV oven. Etch selectivity of SiO_2:PR depends on the exposed surface area of oxide, but can be as low as 1:1, and etch selectivity of SiC:PR is 1:1, less dependant on exposed surface area. Etching of the oxide and carbide films is done in in Lam Research reactive ion etchers using a CF_4 chemistry for the oxide etch and a Cl_2/CF_4 chemistry for the carbide etch. When the initial thermal oxide is used, this layers acts as an etch stopper due to the high etch selectivity of SiC over SiO_2 so there is a high degree of control over final height of the n-SiC/LTO structures left on the wafer. When the thermal oxide is not used, etching of the carbide layer has to be properly timed and overetch should be avoided due to significantly faster etch rates of Si compared to SiC in the chloride chemistry. Etching more than 100nm of silicon might be detrimental for the final structure of the electrodes because the a-SiC films necessary to match the height of the doped SiC might become too thick. Once the dry etch steps are complete the photoresist is removed heated solvent baths followed by piranha clean.

After the wafer is cleaned, the first insulating SiC layer is deposited. Using a conformal method of deposition like PECVD is very important to properly cover the side walls of the n-SiC on the wafer. The thickness of this a-SiC layer is determined by the height of the n-SiC features on the wafer relative to the back plane of the wafer. A surface profilometer is used to measure the height of the n-SiC/LTO stack relative to the silicon or the thermal oxide back plane. The thickness of the a-SiC to be deposited is equal to the height of the stack minus the thickness of the LTO. In order to guarantee that the a-SiC is actually being deposited on the a-SiC, a 10s CF_4 etch followed by 1min argon sputter etch is performed in the PECVD chamber to remove any native oxide that may have formed on the carbide walls. For additional details on the deposition parameters of this film refer to chapter 2.

The next step is to open electrical access to the n-SiC features through the recently deposited a-SiC. For the design of this lithography mask, it is very important to only expose regions in the a-SiC that are directly on top of n-SiC/LTO features, specially if a thermal oxide film was initially used. The reason for this is that there will be an oxide etch later that could attack the thermal oxide if the acid has access to it. A g-line photoresist mask of 2-4μm is spin coated with standard photolithography techniques and hard baked for at least 2h at 120^{o}C, in order to improve etch selectivity. In this manner, a small portion of the a-SiC directly on top of every n-SiC/LTO feature is etch in a Lam Research reactive ion etcher in a Cl_2/CF_4 similar to the one used for the doped carbide film. Since both n-SiC

and a-SiC are about the same thickness, etch time should be about the same. In this case, however, the oxide separating the two types of carbide acts as etch stop allowing for any overetch necessary to complete expose the portion of every n-SiC/LTO stack on the wafer.

The last step of this stage is to remove the oxide and remaining a-SiC on top of the doped carbide. To this end, wet etch of the oxide is done in diluted HF acid and ultrasonic agitation in water is used. Several microns of oxide need to be etched laterally since only a small portion of the a-SiC was etched, so this step might take several minutes depending on the concentration of the acid bath used. Alternating between wet etch and ultrasonic agitation can be used to break off the free standing portions of a-SiC and create more access to the LTO to be etched. During this wet etch process the integrity of the n-SiC/a-SiC interface is tested if a thermal oxide film was used; if the interface is faulty, the acid will reach the thermal oxide creating visible defects. These situations were sometimes observed due to defects in the photoresist mask or due to slight misalignment of the lithography mask. The topography around the bondpads presented some sharp corners prone to defects in the photoresist mask; this could be addressed by changing their design. The interface between the two types of carbide at the recording sites was properly sealed in most cases. Finally, after all the oxide and a-SiC on top of the doped carbide features have been removed, a contact profilometer is measure the step height between the n-SiC and the a-SiC backplane; step height was about 20nm.

Definition of metal interconnects completely embedded in SiC

Silicon carbide is a semiconductor that can reach resistivity of as low as 2mΩ.cm. This level of conductivity is good enough for use of doped SiC in electronics devices but is not suitable for use of doped SiC for long interconnects. As mentioned in earlier in this chapter, interconnects between recording, or stimulating, sites and bondpads may be several centimeters long with electrodes of small cross sectional area. If only n-SiC was used as the interconnect, the track resistance of a 5cm electrode with cross sectional area of 8x1μm would be higher than 100kΩ and the thermal noise associated to it would be about 5μVrms, which is too high for just the interconnect. For this reason, a metal interconnect completely embedded in SiC is more appropriate.

The metal of choice needs to be compatible with the tool in which the a-SiC is deposited. Metals with low gas pressures such as gold may contaminate the PECVD chamber, so they are not recommended to be used as interconnect. For the purpose of this thesis, 100nm platinum interconnects were used. The metal features are patterned on the wafer by standard lift-off techniques using a photoresist bilayer of 1μm LOR-5A and 1μm i-line. The advantage of this bilayer is that, rather than being photo activated, the LOR-5A etches in i-line developer making the coating process simpler. The metal is deposited by electron beam evaporation and 5nm Ti layer is used as adhesion layer between the SiC and Pt.

Subsequently, the second insulating a-SiC is deposited with the same process parameters as the first one. Similarly, the native oxide that may form on the surface of the first a-SiC layer is etched in the PECVD chamber with CF_4 followed by argon sputter etch. This

second layer of a-SiC completely covers all the metal traces making it possible to use the high performance Lam Research etchers without risk of cross contamination. Additionally, all the electrical contacts of the devices face towards the wafers, which means there will not be any metal exposed during patterning of the a-SiC. Patterning of this a-SiC films is done in the same way as the previous ones, using g-line photoresist mask and reactive ion etching. This time, both insulating a-SiC films are etched down to the silicon or thermal oxide backplane. Once the photoresist mask is removed, a thin film of SiC can be sputtered on the entire wafer in order to add a protective coating layer of stoichiometric carbide. At this point, the electrode fabrication is finished; what remains is adding a backing layer and electrode release.

Electrode release

The SiC electrodes are only about 2μm thick and are too brittle and flexible to be handled on their own. For this reason a backing layer is necessary to keep electrodes in place and to be able to attach them to a printed circuit board. The backing layer can be chosen from a wide variety of materials such as polyimide, PDMS or parylene. Stiff backing can also be used if the application requires it. For the release method used here, the requirements for the backing layer are the ability pattern it and negligible etch rates in silicon etchants. Long term reliability of the backing layer is not a concern since it only serves a function of mechanical support while neural probes are handled and implanted in the brain. Once there, delamination of degradation of the backing layer will not compromise the electrical performance of the SiC electrodes. Biocompatibilty of the backing layer should be considered, however, since it will remain implanted in the body for as long as the electrodes. In this order of ideas, the backing layer of choice here is polyimide. Polyimide can easily be patterned in oxygen plasma, can easily be casted on the electrode topography, is inert to XeF_2, forms a strong bond with the carbon atom of the SiC matrix and is biocompatible.

A 4μm polyimide film (PI-2611, HD microsystems, Wilmington, DE) is spin coated at 3000rpm for 30s and cured at 450^{o}C for 30min in nitrogen at 300mTorr. It is important to reach this high temperature to promote the formation of C-C bonds between the SiC and the polymer backbone, which will prevent premature delamination of the backing layer. In the event that the SiC directly exposed to the polyimide is silicon rich, a short silicon etch can be done on the entire wafer just prior to casting of the polyimide; this will remove excess silicon on the surface of the carbide and either leave an stoichiometric SiC surface or a carbon rich surface. Next, the outline of the devices and access holes are patterned on the polyimide by oxygen plasma using a hard mask of silicon dioxide deposited by PECVD and g-line photoresist. Access holes are necessary in the event that device release will be perform from the top by etching the silicon in the carrier wafer that is in direct contact with the electrodes. Alternatively, device release can be done by doing a back etch of the silicon wafer, although this process is often much more time consuming and less reliable. Release by etching through the top of the wafer can be done by XeF_2 etching and release by back etching can be done in KOH at 80^{o}C followed by XeF_2 etching.

Device release by silicon etch in XeF_2 may be a very time consuming process if the surface area of silicon to be etched is too large. The etch mechanism of silicon by XeF_2 uses up the gas so the whole process is limited by how fast the byproducts can be pumped out and fresh gas brought in. For this reason, the pattern etched in the polyimide only exposes areas of silicon that are near the electrodes and must be removed, while the rest of the silicon in the wafer that is far away from any structures of interest is covered from the gas. The XeF_2 etch process consists of a series of cycles composed of an etch period followed by a pump out period; during the etch, XeF_2 gas is brought into the etch chamber at a specified pressure and kept in the etch chamber for a preset period of time, then the etch chamber is pumped out, and then a new etch cycle can begin. Optimal etch rates can be achieved by figuring out the maximum etch period in which there is still XeF_2 gas available for etching, and the minimum pump time necessary to successfully remove the byproducts. In this order of ideas, an element that could limit the silicon etch is inefficient removal of byproducts trapped under the pockets created under the polyimide upon removal of silicon.

3.4 Notes on device fabrication

Devices fabricated with the method described above are shown in Figure 3.5. The following sections will describe the experience fabricating SiC electrode arrays and mention some practical considerations to take into account to improve process reliability and yield.

Creation of conductive SiC features

The critical element in this part of the process that will enable a high yield is good uniformity in the deposition and patterning of this film, specially if the devices are being fabricated directly on silicon. For n-SiC films of 1μm target thickness, deposition and dry etch uniformity should ideally be within 2% on a 6" wafer. If the thickness or etch rate varies too much between the center and the edge of the wafer, it is very plausible that the step height between the bottom a-SiC insulating layer and the n-SiC features will be small in some locations of the wafer and very large in others; yield might be reduced by the inability of the metal interconnect thickness to overcome the step. While metal deposition methods other than electron beam evaporation (which is very directional) could be used, the ideal scenario is that the step height between the two types of carbide is significantly smaller than the metal film thickness.

Generous overetch of the n-SiC film can be done if the devices are being fabricated on a thermal oxide layer due to the good selectivity of the dry etch chemistry against oxide. However, if the n-SiC deposited directly on silicon the amount of overetch needs be minimized. Silicon etches about 3 times faster than SiC in the chemistry described above; excessive overetch in combination with poor etch uniformity might create a similar issue as above, which is step heights between the a-SiC and n-SiC too dissimilar across the wafer. Additionally, excessive overetch might put the top of the n-SiC features too far from the backplane

requiring very thick a-SiC layers; SiC too thick will limit the flexibility of the device. Figure 3.6 confocal images of recording sites and bondpads of devices being fabricated on silicon.

Deposition of first insulating layer and accessing the n-SiC features

Similarly to the description above, deposition uniformity of this first a-SiC film is critical to accomplish small step heights across the entire wafer. Figure 3.6 shows the result of depositing this film with non-uniformity as bad as 50%; while the step height at some locations on the wafer is less than 10nm, in other locations is as large as 300nm. If e-beam evaporation is to be used, due to the directionality of this method a large step height might not be overcome by the metal.

An other important element during patterning of this film is the alignment of the lithography mask used to expose a small section of the a-SiC directly on top of all the n-SiC features. While there is generous tolerance for misalignment (10μm), the subsequent step of oxide etch is faster if the mask features are perfectly centered. The reason for this is that removing the oxide in between the two types of carbide happens mostly by lateral etching as shown in Figure 3.7. If the access hole through the a-SiC is significantly displaced, there might be a need to etch as much as 20μm of oxide in the lateral direction. The downsides of this issue is extended processing time and extended exposure of the carbide to HF.

When the mask to access the n-SiC is badly misaligned, there is risk of damaging the interface of a-SiC and n-SiC. Figure 3.8 shows an example of a bondpad in which the interface was accidentally exposed during alignment of this mask. During the dry etch of the a-SiC, the n-SiC was also etched and the thermal oxide underneath got exposed. During the oxide wet etch is evident how the acid is prematurely reaching underneath the bondpads and recording sites.

Finally, removal of free standing a-SiC films after oxide etch by ultrasonic agitation may need to be done more than once. Partially removing some of the a-SiC allows easier access to the HF to etch any remaining oxide in between the carbides. Figure 3.9 shows an example of recording sites and bondpads in which the free standing films of a-SiC have been removed along with examples in which some of these films still remain.

Metal interconnect and second insulation

Electron beam evaporation of platinum may introduce process challenges for the lift off process. In particular, infrared radiation from the melt that results from heating the metal is absorbed by the photoresist, which causes the following problems. When the photoresist gets too hot, the bilayer profile of the lift off resist expands and collapses onto the trace features causing the metal to form a continuous film and features lose their well define edges. The second problem caused by infrared absorption is hard baking of the photoresist, which significantly slows down the removal of the photoresist.

To solve overheating of the photoresist due to infrared absorption a two way approach was taken: reduction of the time the film is exposed to the radiation by depositing platinum at high deposition rates of up to 3Å/s, particularly during the first 30nm of metal, in order to quickly build up a film that reflects the radiation off the wafer. The second component of the solution is to use heat sinks on the back of the wafer to maintain the wafer as cold as possible. With these modifications of the protocol well define platinum features can be achieved.

Once the metal features are finalized on the wafer it is time for deposition of the second insulation. Due to the processes done on the wafer it is very likely that a native oxide has built up on the surface of the a-SiC. It is crucial then to remove such oxide prior to deposition of the following a-SiC, otherwise the layer may delaminate upon immersion in HF or may delaminate as the oxide degrades in the body. In the case of SiC, HF dips may not be the most efficient way to remove native oxide because the surface chemistry favors the creation of hydroxyl groups. Also, immersion of the wafer in HF at this stage would cause delamination of the metal interconnect as titanium was used as adhesion layer. Removal of the native oxide can be done by a combination of CF_4 etch followed by argon sputter etch in the same PECVD chamber where a-SiC is deposited, or by argon sputter etch if a cluster system is available and the wafer can be transported to the PECVD chamber without breaking the vacuum seal. Figure 3.10 shows the result of using these methods to remove native oxide.

Device release

Spin coating of the polyimide precursor can be challenging due to the topography on the wafer. It is recommended to pour copious amounts of the polyimide precursor to prevent lack of uniform coverage. After oxygen plasma etching of the access holes and device outline, it is important to verify that the silicon carrier has been reached; even an extremely thin film of unetched polyimide, or unetched SiC from previous steps, will mask the silicon and prevent its removal. This test can be accomplished by using a surface profilometer to measure the step height of the polyimide plus oxide hard mask stack as well as the surface roughness at the bottom of the features; surface roughness after complete polyimide removal should be similar to that of bare silicon or thermal oxide. An additional test could be done by reactive ion etch of silicon or thermal oxide; silicon or thermal oxide etch can be verified by optical inspection or surface profilometry.

The process of silicon etch by XeF_2 can be very non-uniform at the wafer scale. In order to minimize the time that carbide features are exposed to the etching gas, due to some devices releasing significantly faster than others, the mask was design to allow dicing of the wafer in five strips; Having fewer devices in the chamber allows for more uniform release within each strip. Progress of the release process is easily observable under an optical microscope because large regions of the silicon being removed can be observed through the polyimide. Figure 3.11 shows a devices being released.

3.5 Device version history

In the development of the fabrication method presented here several versions of the devices were realized. Naturally, the latest devices were the ones to perform the best and most of the descriptions in this document refer to them, but valuable lessons were learned from early attempts to build all-SiC devices.

First prototypes and release methods

The early developments of this project focused on demonstrating the potential of SiC to be used as conductor, insulator and substrate of neural electrodes. Much of the effort went towards development a process to release the devices; this is not trivial for two reasons, many of the films are deposited directly on the carrier wafers where strong chemical bonds are formed and the use of sacrificial layers is not ideal due to the high process temperatures required for deposition of doped SiC.

The first release method tested consisted on using thermal oxide as a sacrificial layer and long immersions in HF. While SiC molecules are not harmed by this acid, long exposures of polycrystalline SiC to HF result in structural weakening of the films; HF is unable to break the Si-C bond but it is able to break through the interfaces of grains within the polycrystalline film. The device design used during this stage of the project require lateral etch of the oxide under the carbide features for several millimeters, which translates in HF immersions of several hours. In addition to weakening the film, intrinsic stress in the SiC causes the films to have excessive curl upon release. Figure 3.12 shows a photo of this release attempt. Other single crystal SiC films were released by immersion in HF and were successfully mounted on glass slides, however, at this point it was clear the need for a backing layer for mechanical support of the SiC thin films.

In order to avoid long exposure of the SiC devices to HF, back etch of the silicon wafer was the next method to be tested. The main advantage of this method is that it gives more flexibility in the type of backing layer to be used; backing layer does not need to be patterned, so materials like PDMS can be used. The two backing layers tested in this release process were parylene-C and PDMS. In the case of parylene-C, an adhesion promoter is used to enhance adhesion of the parylene-C film to the SiC so that the SiC features do not delaminate during the silicon back etch. In the case of PDMS, oxygen plasma treatment is performed prior to casting of the uncured PDMS to promote adhesion of the elastomer to the carbide by means of oxygen bonds.

Device release of these two samples consisted of silicon back etch in KOH at 80^{o}C. While etching of the entire silicon carrier was successful in relatively short periods of time, the following challenges were encountered. Some of the wafers had to be mounted on carrier wafers with crystal bond, which does not remain stable in the hot etching solution, although the main problem with this release method is that the KOH solution not only removes silicon but also breaks the adhesion promoter between SiC and parylene-C causing the carbide features to fall off. While parylene-C backing is not reliable, large SiC films were released

and are mechanically stable as shown in Figure 3.13. In the case of PDMS, SiC films with very large surface area are successfully release as shown in Figure 3.14 by building a custom Teflon jig that allows clamping of the PDMS backing layer and controlled exposure of the back of the wafer to the KOH. The limitation of using PDMS backing layer is the shrinkage of the elastomer upon release causing the SiC to wrinkle as shown in Figure 3.14; Final design of SiC devices incorporates curved traces inspires from flexible electronics to account for this shrinkage.

In this manner, an early version of SiC devices was fabricated. First, n-SiC recording sites and bondpads embedded in sputtered a-SiC are created in the same way described in section 3.3 and then a metal interconnect of Cr/Au is patterned by lift-off and deposited by e-beam evaporation. For the purpose of proof of concept, the second insulator in this early devices is the PDMS backing layer. Devices are released by doing back etch of the silicon carrier until about 50μm of silicon is left before reaching the carbide features, and the final etch is done in XeF_2. Some of these early devices are shown in Figure 3.15.

Two failure modes ware observed in these devices, the metal interconnect fails to contact the recording sites and bondpads due to prohibitively large step height between the doped and the insulating carbide. The second failure mode is cracking of the bondpads during ACF bond assembly due to the PDMS not providing stable support when pressure is applied to the bondpad area.

Version 1

Version 1 of this SiC devices is the first one to be fully encapsulated with SiC made with the fabrication process presented in Figures 3.2-3.4. These devices use sputtered SiC for both layers of insulation and Cr/Au or Ti/Pt interconnects. Given the failure modes observed during release procedures in KOH, this version of the devices is mounted on polyimide films which have access holes patterned in them for the purpose of release in XeF_2.

This version of the devices iss the first prototype fully assembled to a PCB and implanted *in-vivo* as shown in Figure 3.16. The polyimide film is thin enough that the carbide bondpads are not observed to crack during ACF bonding. Several of these devices have adequate connectivity between the n-SiC recording sites and bondpads and platinum black electroplating is successful.

The failure mode of these devices is faulty insulation. Sputtered SiC turns out to not be a suitable insulator due to low sheet resistivity and the presence of pinholes inherent to the deposition process. This failure mode will be further discussed in the next chapter. As a result of the poor insulation, neural recordings done by this device are too noisy and no neural signatures are identified from the animal recordings.

Version 2

The last version of the devices use PECVD SiC as insulator and Ti/Pt for the interconnect. PECVD films can be deposited with a much lower pinhole density, which effectively becomes

null when the films are thick enough. These devices have been successfully used in *in-vivo* experiments to record from the central and the peripheral nervous system.

Version 3

The main improvement of this version is the incorporation of sputtered SiC as the outer most layer of the a-SiC insulation. Sputter SiC has perfect stoichiometry, which translates in superb chemical inertness. While our PECVD SiC films do not suffer from degradation in PBS, which is the solution used for accelerated aging tests, they do show a very slow etch in XeF_2. Adding the sputtered SiC to the exterior of every layer in the SiC devices results in a device whose most exterior layer is stoichiometric SiC, either polycrystalline or sputtered a-SiC, making the devices resistant to virtually any chemical present either in the body of during the fabrication process.

3.6 Chapter figures

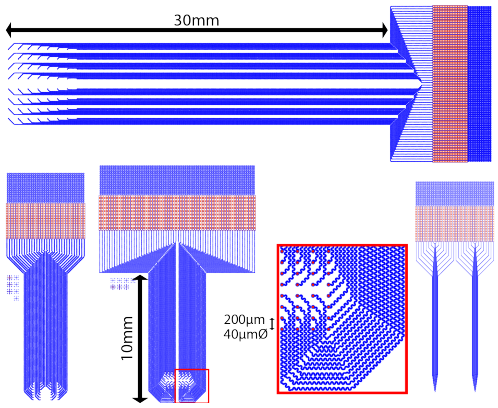

Figure 3.1: CAD designs of devices v1 and v2. Top device corresponds to an ECoG array intended for large animals. Bottom devices correspond to ECoG arrays of 32 and 64 channels for small animals, and one 32 channel device for intracortical recordings. Zoomed in section corresponds to active area of small 64 channel ECoG array.

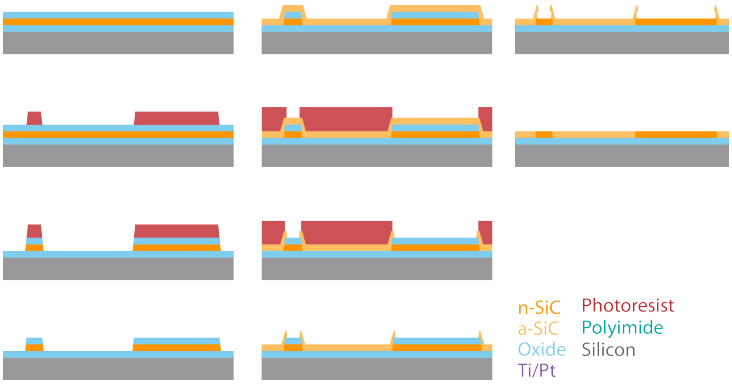

Figure 3.2: Schematic of fabrication process for creating features of doped n-SiC embedded in a film of insulating a-SiC

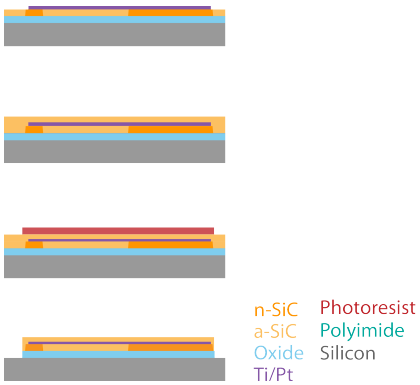

Figure 3.3: Schematic of fabrication process for creating metal interconnects between features of doped n-SiC embedded in insulating a-SiC and final encapsulation in insulating a-SiC

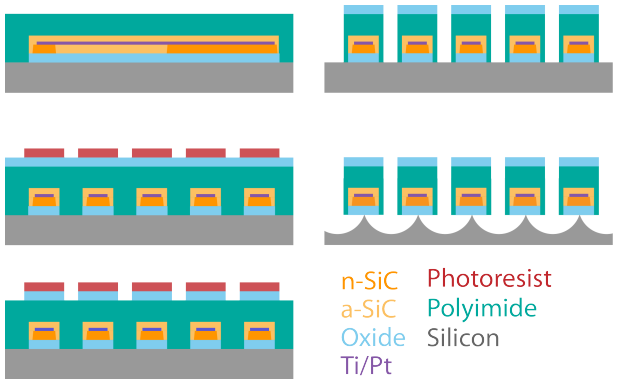

Figure 3.4: Schematic of fabrication process for adding a backing layer to the SiC electrodes and device release.

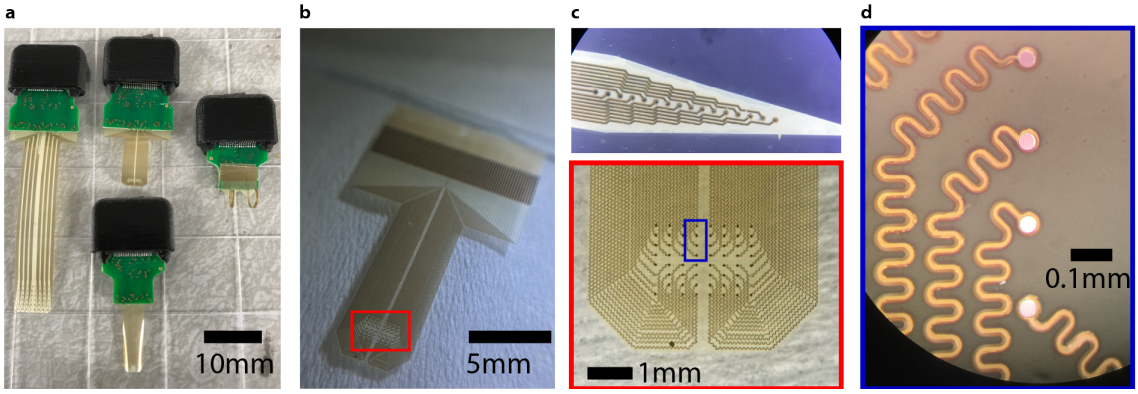

Figure 3.5: a) Assembled SiC electrode arrays. b) SiC electrode array as released from the wafer before assembly. c) Active area of SiC electrode arrays for intracortical (top) and surface (bottom) recordings. d) Zoomed-in optical image of recording sites.

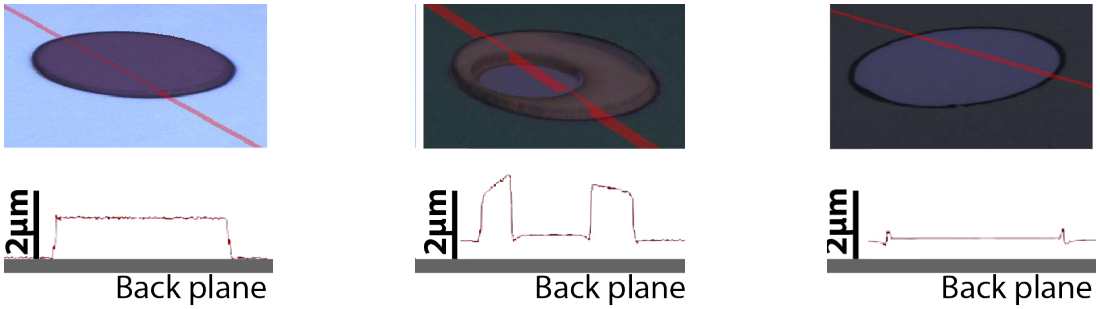

Figure 3.6: Confocal image and surface profile of SiO_2 on n-SiC pillar recording site on a thermal oxide backplane (left), opening through a-SiC on top of recording site exposing n-SiC (middle), and n-SiC rec site embedded in a-SiC backplane after freestanding a-SiC pieces were removed in ultrasound bath (right).

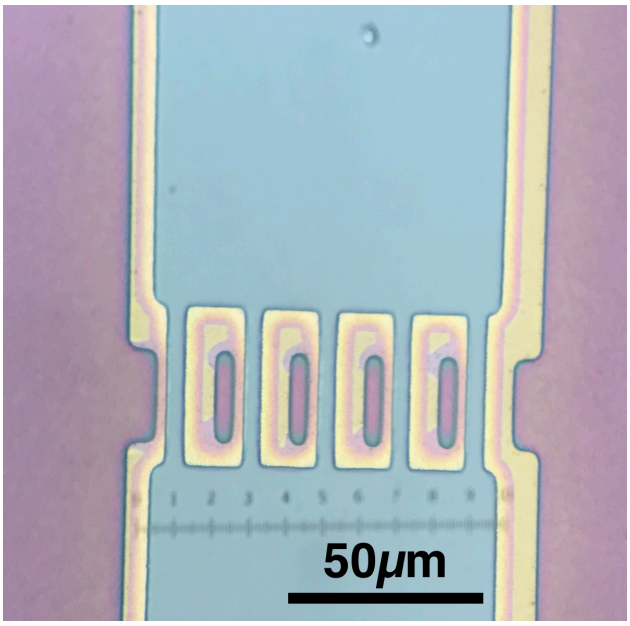

Figure 3.7: The oxide in between two types of SiC is being isotropically etched. The front of the oxide film under the a-SiC can be observed recessing towards the edge of the bondpad (and the features in the middle).

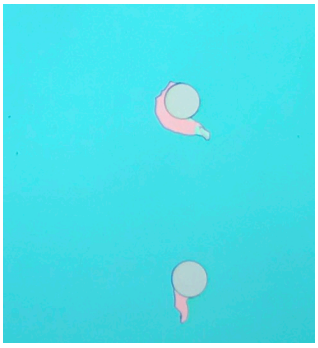

Figure 3.8: Optical images of n-SiC/a-SiC not properly sealed that were damaged during HF immersion. In this particular case residual polymer from CF_4 etch prevented adequate adhesion. In other cases native oxide or lithographic defects may compromise the interface. Recording sites in image are 40μm in diameter

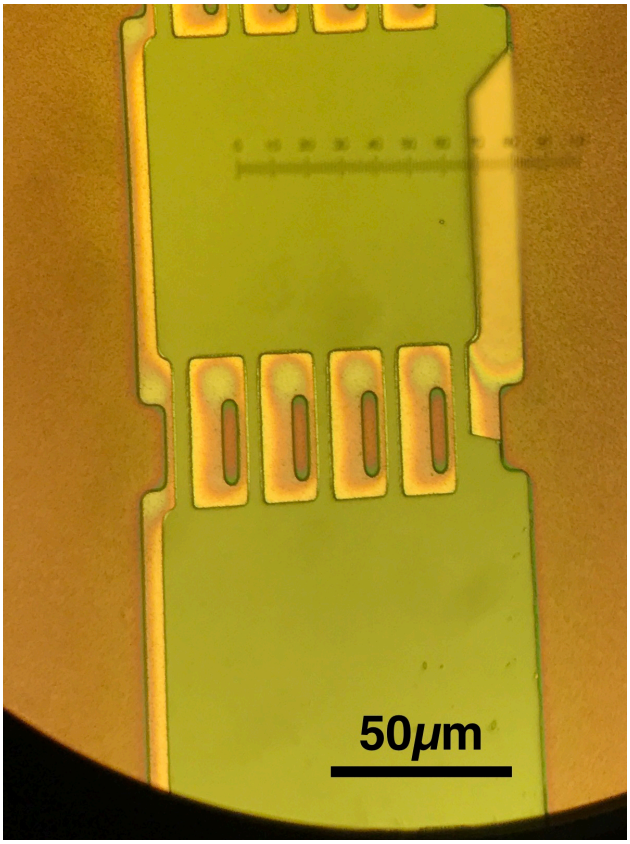

Figure 3.9: Optical image showing how the free standing a-SiC can be removed by ultrasonic agitation. The lower right of the bondpad is an example of an edge where the a-SiC wall has been completely removed while the rest of the bondpad requires more ultrasonic agitation.

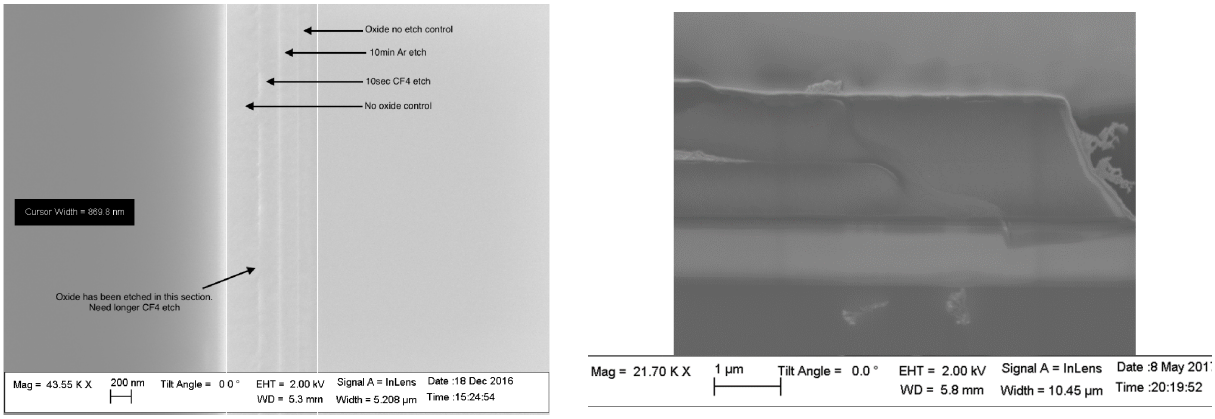

Figure 3.10: SEM images showing removal of native oxide in between a-SiC layers. Image on the left shows the effect of multiple treatments in between film deposition. Image on the right shows a continuous a-SiC/a-SiC interface as a result of using argon sputter etching to remove native oxide of bottom a-SiC layer.

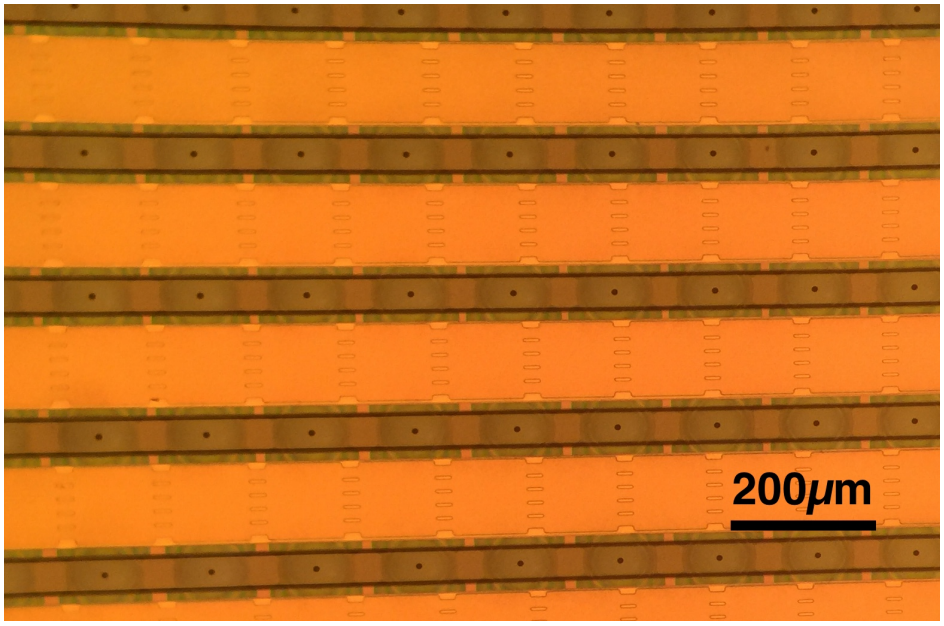

Figure 3.11: Optical image of array bondpads partially release in XeF_2. Each access hole in the polyimide backing layer has a circular halo around it where the silicon has been removed. Bondpad is completely released when all such circles completely overlap.

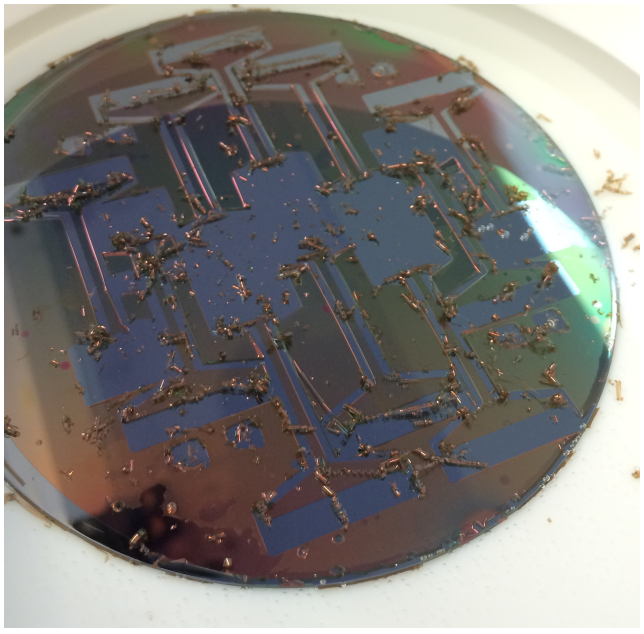

Figure 3.12: Detrimental effect of long exposure to HF of polycrystalline SiC. After several hours of immersion, the polycrystalline SiC film crumbles and cracks as the oxide underneath is being etched. Substrate in the image is a 4" silicon wafer.

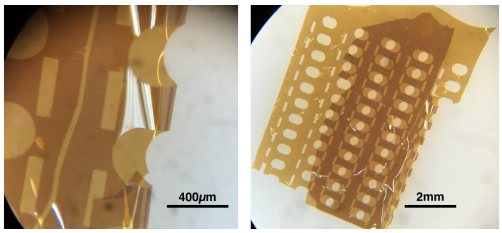

Figure 3.13: Examples of free standing polycrystalline SiC films. These films were mounted on parylene-C backing layer but delaminated during release in KOH. Nevertheless, SiC were strong enough to stand on their own.

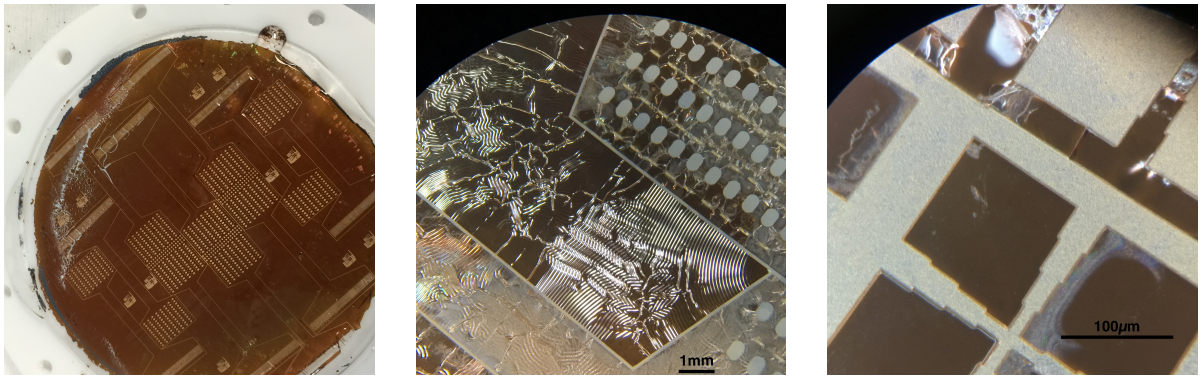

Figure 3.14: Optical images of SiC films mounted on PDMS. An entire SiC film, that ahd been deposited and patterned on a 4" silicon wafer, is now mounted on PDMS and released from the carrier wafer (left). Large surface area regions of SiC on PDMS wrinkle due to shrinkage of the PDMS (middle). SiC films with surface area in the order of 200μmu by 200μm do not wrinkle (right).

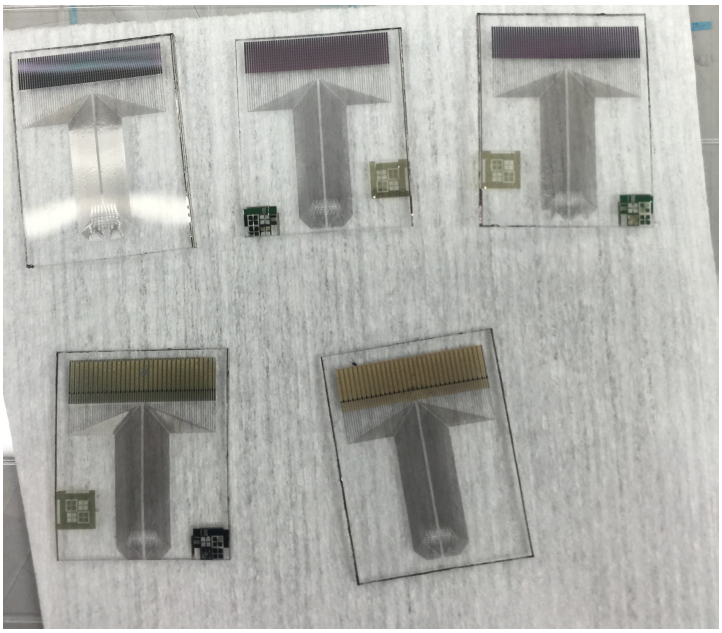

Figure 3.15: Optical images of SiC ECoGs v0.1. These devices were mounted on PDMS and released in a combination of KOH and XeF_2 silicon carrier back etch.

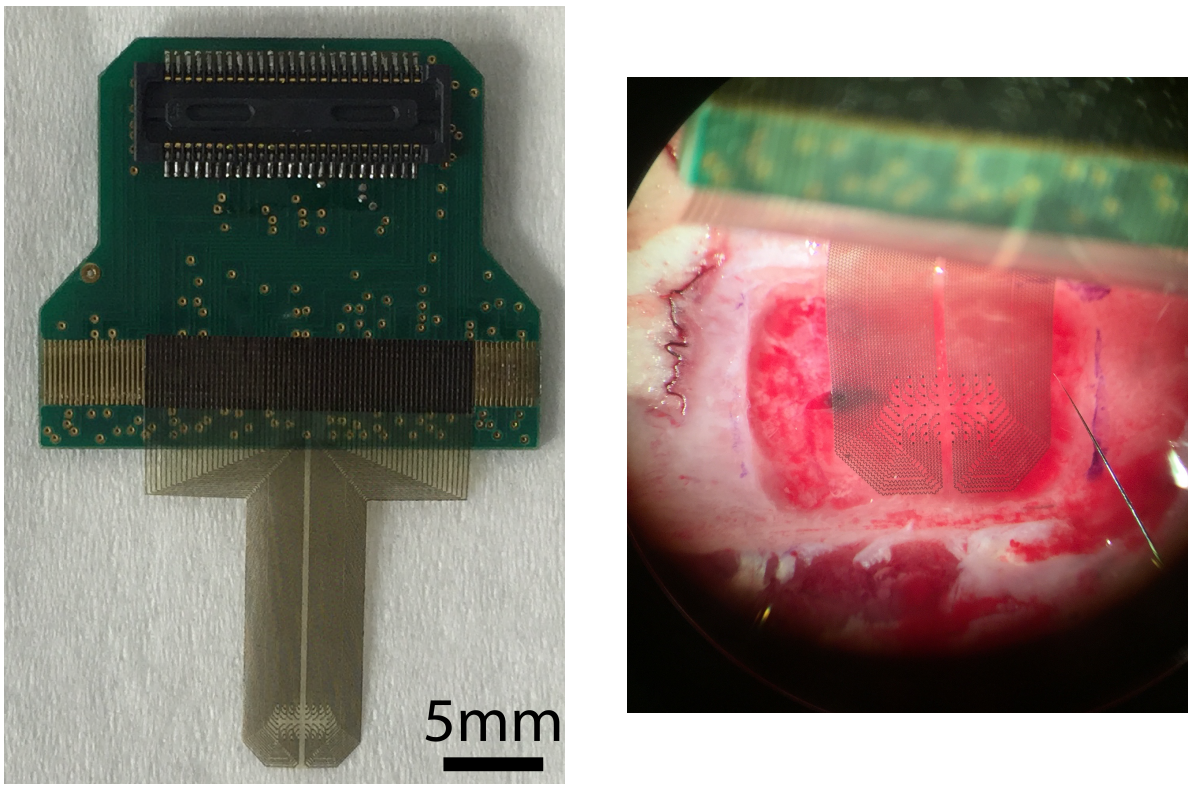

Figure 3.16: A photo of a SiC ECoG v1.0 assembled to a PCB by ACF bond (left) and acute implantation of similar device in rat barrel cortex.

Chapter 4

In-vitro characterization and neural recordings

Adapted with permission from:
Diaz-Botia, C., Luna, L., Neely, R., Chamanzar, M., Carraro, C., Carmena, J., Sabes, P., Maboudian, R., and Maharbiz, M.
A silicon carbide electrode technology for the central and the peripheral nervous system.
J. Neural Eng. (2017) DOI:10.1088/1741-2552/aa7698

4.1 Chapter overview

This chapter presents the *in-vitro* and *in-vivo* characterization of silicon carbide based devices. In the first part, the probe assembly is briefly described followed by their electrical characterization, sections 4.2 and 4.3. And in the second part, *in-vivo* recordings from the central and the peripheral nervous system of a rat are presented, sections 4.4 and 4.5.

4.2 Device assembly

Electrode arrays are connected to printed circuit boards (PCB) using anisotropic conductive film (ACF, 3M anisotropic conductive film 7379) as developed by Ledochowitsch et al.[26]. This method consist of an adhesive film that has conductive particles embedded in it; when two conductive surfaces are brought together with the ACF in between and heat and pressure is applied, the adhesive bonds the two surfaces and the conductive particles create a low resistance electrical connection between the surfaces only in the direction normal to them.

Thin film electrode arrays are assembled as follows: ACF film is prebonded to the ACF bondpad area of the PCBs using an Ohashi HMB-10 table-top bonder (5s, 90Kg/cm^2, 90^{o}C at bond site, blade set to 135^{o}C), then the bondpads of the ECoGs are aligned to the footprint on the PCB under a microscope and tacked to the tape with a soldering iron. Finally, permanent bonding is done using the Ohashi Bonder (30s, 160Kg/cm^2, 160^{o}C at bond site, blade set to 235^{o}C). Typical yield of this assembly method is about 80%.

4.3 *In-vitro* characterization of SiC devices

In-vitro characterization of SiC devices is first done in a probe station in order to determine the yield of the wafer level fabrication and isolate failure modes of assembly steps downstream the process. The goals of this characterization are to determine the insulating properties of a-SiC traces, verify ability to electroplate the recording sites and compare these results to electrode arrays fabricated with traditional methods using polyimide. The SiC devices described in this section correspond to devices in which the insulating a-SiC was deposited using the 13.56MHz generator. While we observe that the electrical characteristics of these devices are suitable for electrophysiology, further development of the insulating films has been done (refer to chapter 2 for details) and some of the failure modes described in this section were fixed by the improved a-SiC films.

Methods for *in-vitro* characterization

The techniques used for electrical characterization of devices are described here.

DC leakage current: The purpose of this leakage current test is to determine if the a-SiC films is pinhole free and to determine if it remains pinhole free when DC bias is applied. The test consists on applying a DC bias of up to 100mV between one of the bondpads of the

array (anode) and a drop of saline placed on the cable of the device, as shown in Figure 4.1. The bias is applied with a Keithley 2400 power source which measures the current flowing in the circuit.

Electrolyte-interface impedance spectroscopy: A common method in the characterization of neural probes is electrolyte-interface impedance spectroscopy (EIS). This method can be used to determine the suitability of electrodes to record high quality neural signals as well as the quality of electrode insulation. Spectroscopy is done using a NanoZ Impedance Analyzer (Tucker Davis Technology, Alachua, Fl). The measurement is done by applying a sinusoidal voltage signal between two terminals, one terminal usually in direct contact with a bondpad and the second terminal usually immersed in saline placed on a recording site or insulating trace, and measures the current flowing in the circuit; the impedance of the electrode is determined by the difference in amplitude and phase between the two signals. For this NanoZ device in particular it is very important to ground the device; power line noise can travel through the computer and contaminate the measurement signal.

Platinum black electroplating: Electroplating of a variety of materials is typically used in neural electrodes as a method to lower the impedance of recording or stimulating sites. The goal of this process is to enlarge the surface area of the active sites creating larger regions for the ionic interaction. Here, platinum black (YSI 3140 platinizing solution, Fondriest Environmental, Fairborn, OH) is electroplated on the n-SiC recording site by applying a DC current between a bondpad and the electroplating solution in which the recording sites are immersed. This process is also performed by the NanoZ device.

a-SiC provides good trace insulation

Electrodes are adequately insulated by a-SiC as can be observed in the impedance spectra of representative devices shown in Figure 4.2. The impedance magnitude resembles the impedance for an open circuit across the spectrum and impedance phase is almost purely capacitive as well. The impedance spectra of the insulation of control polyimide devices was also measured and Figure 4.2 shows that it matches the spectra of SiC devices. This comparison serves as reference of SiC device suitability for neural recordings as polyimide devices have extensively been used in *in-vivo* applications. Additional evidence of good insulation will be mentioned later when active site electroplating is discussed.

This films of SiC are very flexible and do not crack during normal handling of the devices. While no formal experiments were conducted to determine how far can these thin films be bent without cracking of the a-SiC films, the release and assembly processes require manual handling of the thin film. Films are usually laid flat on glass slides and when the devices are peeled off the slides with tweezers, they bend. Faulty insulating is not usually observed after manual handling, which suggests the a-SiC has not cracked.

Leakage currents through the a-SiC insulation are usually maintained below 10pA for DC bias of up to 100mV. However, when the bias is increased to values of up to 5V pinholes are created in the film leading to significant leakage current; breakdown of the dielectric may occur in locations of the film where the solution is in close proximity to the inner conductor

creating high electric fields in the order of 10^6V/cm. A much more careful study of this failure mode was done on the improved PECVD SiC films described in chapter 2.

Early versions of the SiC devices that used sputtered SiC lack adequate insulation. Figure 4.3 shows the impedance spectra of a few traces that should have been insulated; the impedance magnitude is fairly low and the impedance phase has a significant resistive component. The reasons sputtered SiC films fail to provide good insulation are the presence of pinholes in the film and the low sheet resistivity in the range of $10^6\Omega$.cm, too low for a good insulator.

SiC electrodes are suitable for electrophysiology

A large number of electrode arrays were electroplated with platinum black as shown in Figure 4.4. Recording sites that are properly connected to the bondpad or the PCB are easily recognized by the electroplated material on them, while sites whose electrical connection is faulty remain with clean n-SiC surfaces. It is important to observe the lack of non-specific electroplating through the a-SiC insulation; presence of pinholes or cracks in the insulation would allow the electroplating solution to reach the inner conductor and electroplate it. Recording sites are usually electroplated at -2μA for up to 10s, beyond this no further reduction in impedance is observed.

The impedance of the electrodes measured by EIS is usually below 100kΩ at 1KHz, which is typical for recording sites of the dimensions used here and is suitable for electrophysiological recordings. Figure 4.2 shows the impedance spectra of a representative SiC measured in a probe station; the purpose of this experiment is to isolate the effects of the assembly process by ACF bond in the electrical characteristics of the device. The impedance of these devices is similar to devices of similar geometry fabricated with polyimide, as shown in Figure 4.2.

The majority of SiC devices are assembled to PCB's in order to allow higher throughput of the electroplating and characterization process. While the ACF bond reduces the overall yield, devices that do work show similar impedance spectra as those characterize in the probe station and as those of polyimide controls. Figure 4.5 shows impedance spectra of a representative SiC device.

Recording sites that are not properly connected to the bondpads are also easily recognizable in the EIS measurements since they behave like an open circuit. The impedance spectra of disconnected recording sites has impedance magnitude as high as the NanoZ device can measure and impedance phase almost purely capacitive. Notice that this is the same scenario observed for properly insulated traces, so it is important to verify trace connectivity before assessing proper insulation.

4.4 Recording from an animal model

All animal experiments were performed in accordance with the University of California-Berkeley Animal Care and Use Committee regulations. Neural recordings from the central

nervous system (CNS) and the peripheral nervous system (PNS) were done in adult male Long-Evans rats.

Primary visual cortex

An adult male Long-Evans rat is anesthetized with urethane and placed in a stereotaxic instrument. ECoGs are acutely implanted in the right primary visual cortex (V1), and visual stimuli is presented contralaterally to the left visual field on an LCD monitor. Stimuli consists of drifting sinusoidal gratings at 100% contrast ratio. The direction of motion of each stimulus is randomly chosen between 45 and 360 degrees in 45-degree intervals. Stimuli are presented in a series of trials consisting of a 2s zero contrast display, followed by 2s of a drifting grating at the randomly chosen orientation, followed again by a 2s zero contrast display. Trials are repeated at 15 second intervals. Control trials consist of a zero contrast display during the stimulation period of the trial, resulting in the presentation of a zero contrast display during the entire 6s period.

Signals from the surface of the rat primary visual cortex are sampled at 25kHz using a TDT RZ2 digital signal processor and PZ2 pre-amplifier (Tucker Davis Technology, Alachua, Fl). Data are analyzed using custom routines written in Python. Spectral estimation of field potential activity is done using the multi-taper method[44]. A total of 5 tapers are used with a time-bandwidth product of 3. To calculate spectrograms displaying spectral power over a given trial interval, spectral estimates are computed every 50ms with a window size of 750ms. Each individual frequency band of the resulting spectrogram is normalized to its own mean power over the entire time interval.

A 64 channel SiC ECoG is used to measure the neural responses of the rat V1 to the visual stimuli. Fig. 4.6a shows the location of the active area of the array in V1. Increases in the gamma-band activity are observed in all of the stimulation trials, and some electrodes record apparent orientation-tuned responses. Fig. 4.6b shows the neural response recorded in one channel during a period of stimulation of bars in the 270^o orientation; the green line indicates the onset of stimulation and red line the offset. A significant increase signal power in the gamma and high gamma bands is observed with a delay of about 100ms. An example of orientation tuning is shown in fig. 4.6c where the strongest activity is observed in response to the 270^o and 225^o stimuli orientations and the least strong response for 45^o and 180^o. In the macro scale, neural responses are distributed along the cortex as shown in Fig. 4.6d. As expected, the control stimuli fails to elicit neural activity in response to the onset of the stimulation; this is shown in Fig. 4.6e. Activity seen in some of the channels during the control trial is outside the stimulation window.

Sciatic nerve stimulation

SiC electrode arrays were used to record from the peripheral nervous system. The active site of a SiC electrode array is wrapped around the right sciatic nerve of an anesthetized adult Long Evans rat in an acute experiment as shown in Fig. 4.7a. Electrical stimulation is deliv-

ered through stainless steel needles to the biceps femoris muscle ipsilateral to the electrode array. The stimulation consists of square pulses of 10μs at 0.5Hz that vary in amplitude between 0.5 and 1.2mA. Electrical stimulation of the contralateral muscle is performed as a control.

Data are collected on 32 channels using TDT RZ2 digital signal processor and PZ2 pre-amplifier at a sampling rate of 25kHz. Data analysis is done using custom Matlab scripts; data are high pass filtered to remove the DC offset and stimulus triggered averages are calculated for each of the stimulus amplitudes used.

Figure 4.7 shows the peripheral nerve response to electrical stimulation of the biceps femoris muscle ipsilateral to a SiC array. Fig. 4.7b shows the recorded response to each of the amplitudes tested and Fig. 4.7c shows a summary of the response of the sciatic nerve as the amplitude of the electrical stimulation increases. For low stimulation amplitudes, 0.5mA and 0.6mA, the average peak-to-peak amplitude of the combined action potential is the smallest, and this amplitude rapidly increases for amplitudes of 0.7 to 0.9mA and saturates at around 1mA. Fig. 4.7d shows the nerve response for measured channels during 0.8 mA stimulation. When electrical stimulation is applied to the muscle contralateral to the array, no action potential is observed regardless of the amplitude of the stimulation.

4.5 Chapter figures

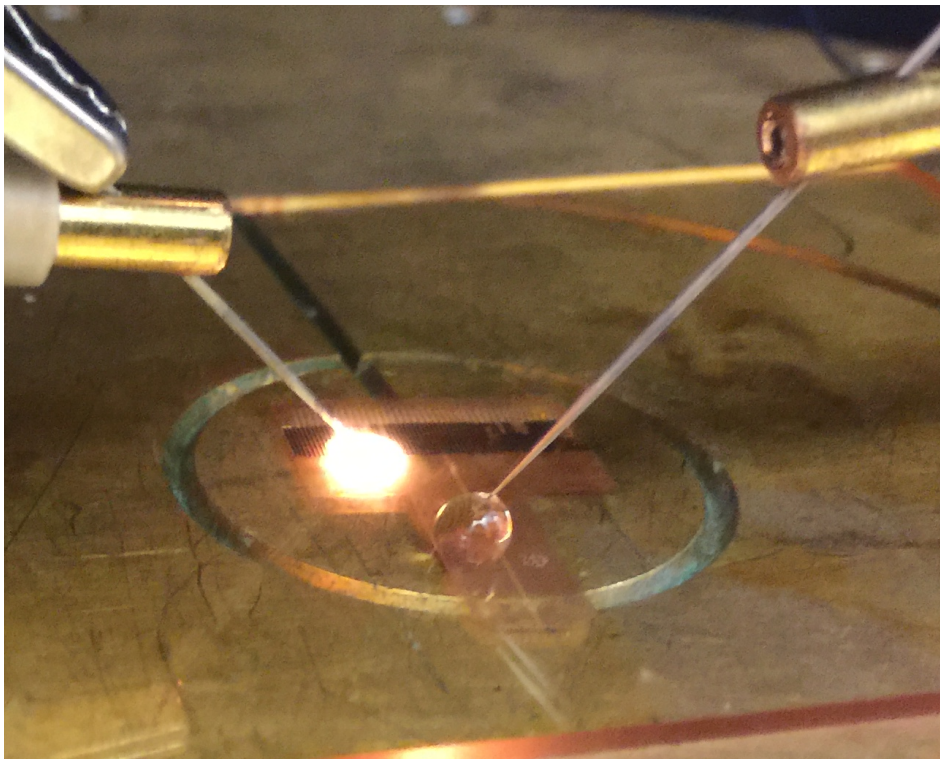

Figure 4.1: Set up for testing DC leakage current of devices. A drop of PBS is placed on the cable (fully insulated traces) and a DC bias is applied between the saline drop and the bondpads while current is being measured.

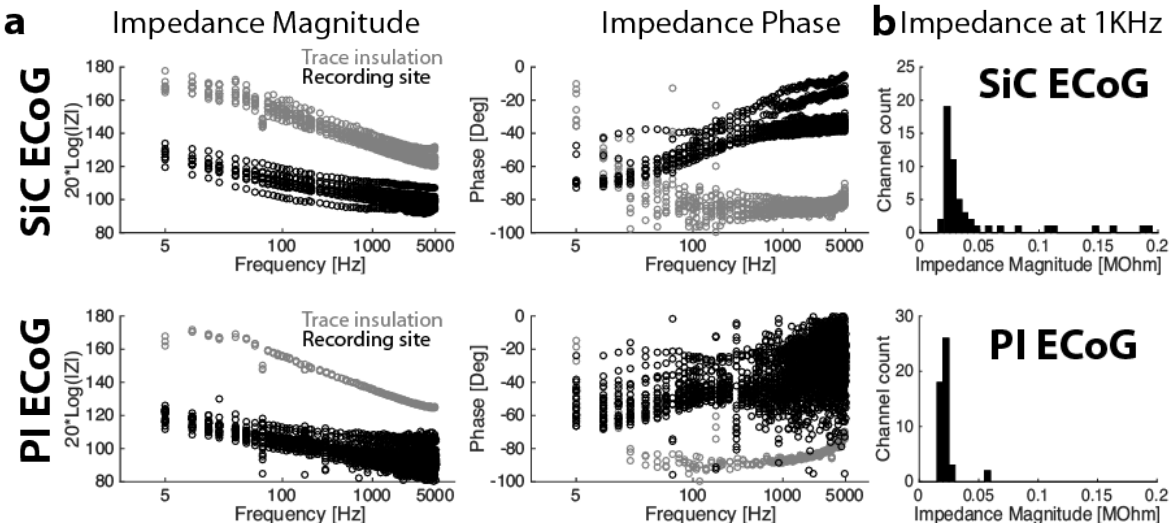

Figure 4.2: EIS characterization of SiC ECoG v2.0: a) Impedance magnitude and phase of trace insulation (gray traces) and recording sites (black traces) for SiC device (top) and polyimide device (bottom). b) Distribution of impedance magnitude at 1KHz for SiC device (top) and Polyimide device (bottom).

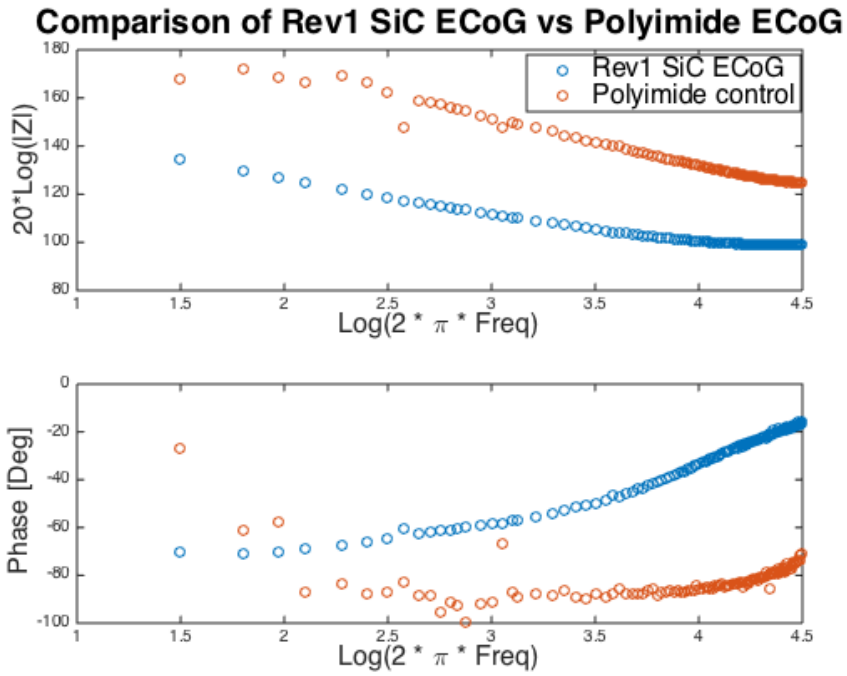

Figure 4.3: *In-vitro* characterization of SiC devices v1.0 showing defective insulation. Impedance magnitude of sputtered a-SiC insulation is much lower than the polyimide control. Impedance phase of sputtered a-SiC insulation shows partially resistive behavior.

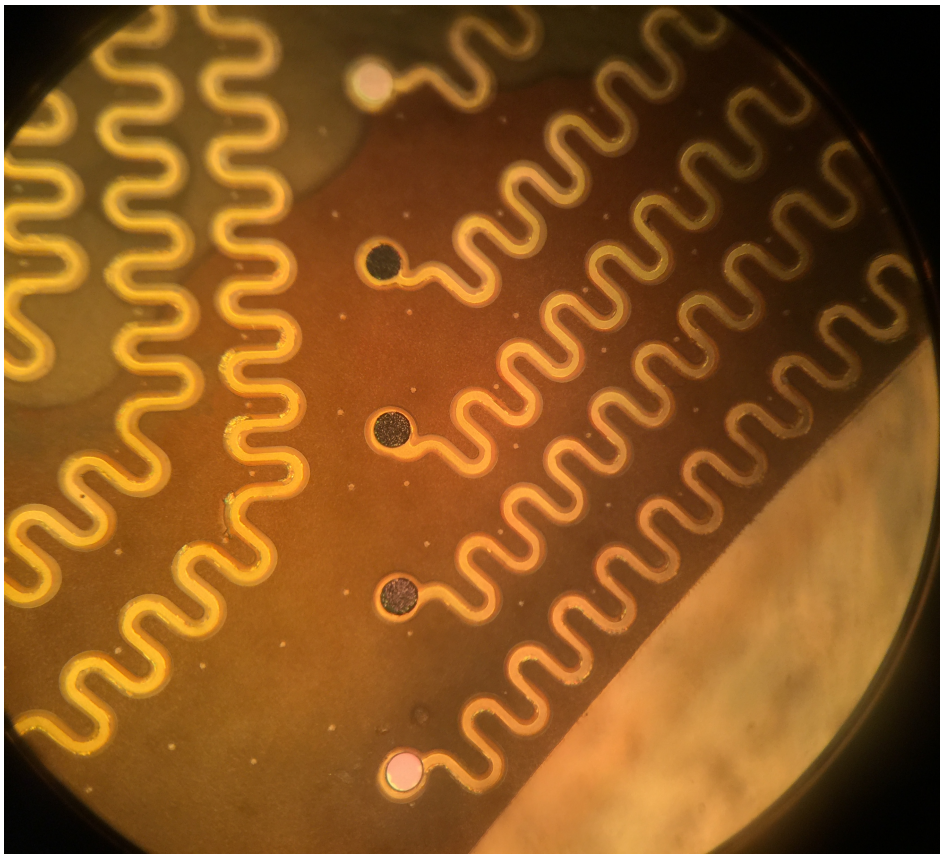

Figure 4.4: Example of electroplated rec sites. Recording sites are 40μm in diameter. Some sites did not electroplate likely due to lack of connection with the bondpad.

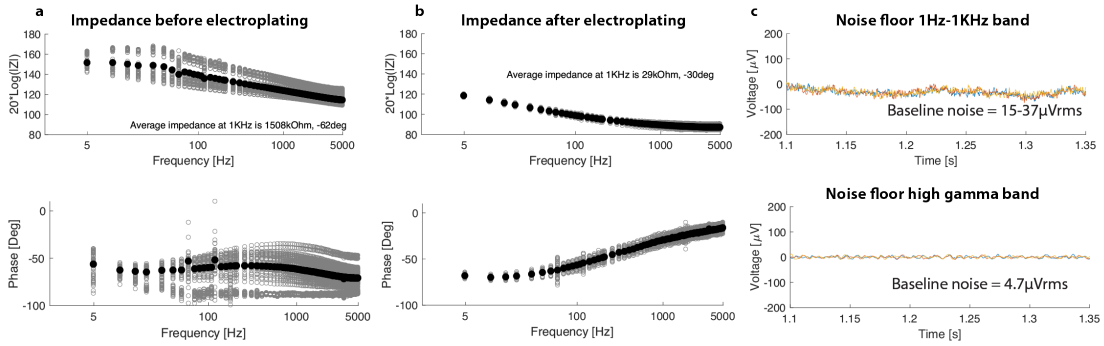

Figure 4.5: a) Impedance magnitude and phase of recording sites before electroplating. Gray traces represent each electrode measured and black traces are averages. b) Impedance magnitude and phase of recording sites after electroplating. Gray traces represent each electrode measured and black traces are averages. c) Baseline noise measured in saline in the 1Hz-1KHz band and high gamma band (60-200Hz), top and bottom respectively, for three representative channels.

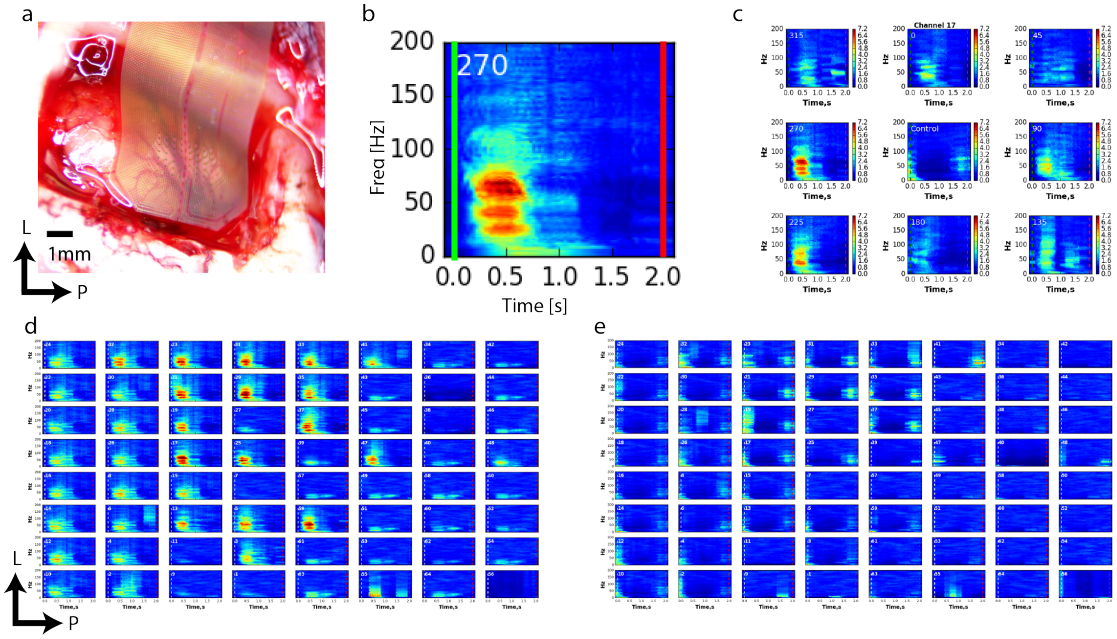

Figure 4.6: a) Photo of SiC ECoG implanted on primary visual cortex of a rat. b) Spectrogram of neural response to visual stimulus. Green line is stimulus onset and red line is offset. c) Spectrograms of representative channel with orientation tuning. Center plot is control trial and plots around it corresponds to all orientations tested. d) Whole ECoG array spectrograms during visual stimulation with bars at 270^o. e) Whole ECoG array spectrograms during control trial.

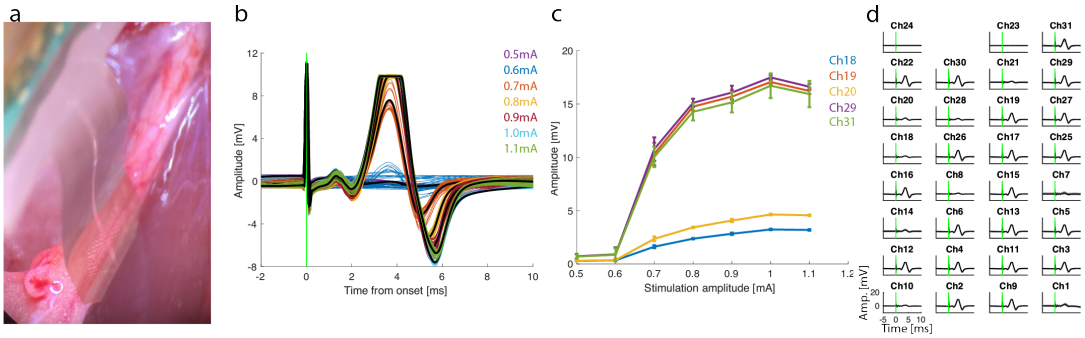

Figure 4.7: (a) Photo of SiC electrode array implanted on sciatic nerve. b) Signal recorded on one representative channel showing sciatic nerve response to electrical stimulation. Individual responses have been aligned to the artifact caused by the electrical stimulation. Each color represents an stimulus amplitude and black traces are averages. 0.5mA was below threshold and failed to elicit an action potential strong enough to be observed. When stimulation was increased to 0.6mA, a compound action potential of small amplitude was observed 10% of the time. Stimulation at 0.7mA or higher reliably elicit an action potential every time the muscle was stimulated. c) Five representative channels showing sciatic nerve saturation as stimulation amplitude increased. The plot shows the average peak to peak amplitude of the recorded action potential as a function of stimulation amplitude. d) Example of the signals recorded by the whole electrode array for one representative stimulation amplitude. Each plot corresponds to one electrode. Some channels that recorded significantly smaller signals or not signal at all likely correspond to those whose impedance was too high.

Chapter 5

Future development

5.1 Use of a-SiC encapsulation for medical devices

One of the most potentially impactful contributions described in this dissertation is the demonstration that silicon carbide (SiC) deposited by plasma enhanced chemical vapor deposition (PECVD) can be a good insulator in aqueous environments (i.e. films can have high sheet resistivity and low pinhole density) while maintaining its superb chemical stability. We showed that a film of a-SiC as thin as 1μm is enough to maintain good long term insulation. This is an important result not only for the development of neural probes but also for the development all implantable devices; the need for devices with small footprint that may be better accepted by the body significantly limits the allowable thickness of encapsulating layers. To the best of our knowledge, our a-SiC films are the most chemically stable and thinnest insulating films suitable for aqueous environments that can be deposited at temperatures below 400^{o}C[12].

Dielectric a-SiC can be used in many applications. An example of this is the use of carbide as a protective coating for chips with wireless communication. This is particularly attractive because the lack of external connections of these chips allows for full encapsulation of the device, eliminating any weak interface. a-SiC could be used for example to coat radio frequency ID tags with their antennas for operation in aqueous, highly corrosive environments. a-SiC is also an excellent molecular barrier, so it could be used to encapsulate devices sensitive to moisture or to encapsulate devices that contain non-biocompatible or toxic components, preventing diffusion of such elements into the environment surrounding the device.

The main challenge in turning a-SiC into the go-to material for device encapsulation is a material compatibility issue. For example, a-SiC could be used as outer encapsulation of commercial integrated circuits so these can operate in aqueous environments like the body. Commercially fabricated chips almost always require electrical connections to spare components for proper functionality (e.g. antennas, capacitors, batteries), so chips have exposed pads to which such connections can be made. The most commonly used material

covering these pads is gold; gold is a highly diffusive metal that in most facilities is not allowed to enter PECVD chambers because it would permanently contaminate them, hindering the ability to deposit materials with specific electrical properties under such contamination. In this manner, custom fabrication protocols have to be developed to either encapsulate contaminants like gold or remove them completely from the devices to be coated with a-SiC.

The presence of complicated topography might pose additional challenges. PECVD processes are highly conformal and are specially good at coating sidewalls. However, due to the plasma mediated reactions, coverage of shadowed features may not be as good. In this case, device features should be carefully designed to avoid such a problem, or coating in multiple stages in which the devices are turn around could be done.

Finally, deposition of SiC films on flexible substrates should be limited to carbide films only a few microns thin to avoid cracking. Films of 2μm or less can have radii of curvature as small as 150μm, which is sufficient for many applications; thinner films than this may be coupled with other highly flexible materials like polyimide or parylene and still be compliant and not crack. Conversely, thick films of SiC can serve as mechanical support for other layers; SiC fibers 8μm thick are stiff enough that they can be inserted in brain tissue without the need for additional support.

5.2 Case study: integrating SiC devices with invasive neural probes

In the Maharbiz lab, we have been developing various systems for brain-machine interfaces. One of these systems involves the development of polyimide based electrodes for intracortical recordings. This section will describe our progress and contributions towards this system and will end with a description of how to integrate SiC technologies to it.

Fabrication of minimally invasive neural electrodes

In collaboration with the Sabes lab at the University of California, San Francisco we have developed and fabricated minimally invasive neural electrode arrays. The fabrication protocol is briefly explained below. The electrodes are composed of a thin platinum trace with polyimide insulation on top and bottom; these polyimide layers are spin coated on 6" silicon wafers and cured at temperatures up to 450^oC in a low pressure nitrogen environment, and 100nm platinum traces are pattern and deposited by standard lift-off techniques and electron beam evaporation. An optical image of the electrode heads is shown in Figure 5.1.

The insertion method of these highly flexible neural probes consists of a robotic system with an ultra-fine needle that threads through a loop located at the end of each polyimide electrode and individually inserts them into the brain. For this purpose, the flexible electrodes need be neatly arranged so that they can be automatically identified, threaded and inserted. We use a sheet of parylene to keep the electrodes in a 1D array as shown in Figure 5.2, with the electrode heads slightly extending beyond the parylene edge. The parylene

sheet is conformally deposited by chemical vapor deposition, patterned with an aluminum hard mask and etch in oxygen plasma.

Thin films electrodes are connected to standard printed circuit boards (PCBs) by wire bonding. In order to be able to create these connections, the thin film bondpads need to be electroplated so there is sufficient mechanical support to absorb the ultrasonic power necessary for bonding. We electroplate bright nickel pads up to 20um in height using Krohn bright nickel electroplating solution with a DC bias of 1.6-1.8V. Electroplating current is uniformly delivered to all bondpads on the wafer by using a copper bus 400nm in thickness which is deposited by electron beam evaporation, patterned with standard photoresist and wet etched. The electroplated bondpads with aluminum wirebonds are shown in Figure 5.3.

Thin film electrodes are assembled on PCBs. To this end, a low viscosity epoxy is used to create a very thin film between the PCB and the thin film polyimide. This way, the ultrasound power during wirebonding is properly transferred to the bondpad instead of being dissipated by the epoxy. Once assembled to the PCB, the electrical connections can be made as shown in Figure 5.4 by aluminum wedge wirebond. The PCB allows connection of the polyimide electrodes to other systems via a 64 pin Zero-Insertion-Force (ZIF) clip. We use a NanoZ impedance measuring and electroplating device to measure impedance and electroplate platinum black on the active sites of the polyimide electrodes. Typical impedance measurement after electroplating are shown in Figure 5.5; these electrodes have average impedance of about 30kΩ and are suitable for intracortical recordings. These electrode arrays have been successfully used to record neuronal signals *in-vivo* as shown in Figure 5.6.

Thin film electrodes integration with neuro modulator

We integrate our thin film electrodes to a neuro modulator integrated chip (NMIC) developed by the Berkeley Wireless Research Center for neural recordings and stimulation. We accomplish integration of these two systems via the flexible printed circuit (FPC) shown in Figure 5.7; the thin film and integrated chip are mounted and wirebonded to the board along with several passive components necessary for digital noise reduction and the stimulating features of the chip. Analog data from the 64 recording electrodes is digitized and serialized by the chip and transferred to an aggregator module via one of the seven I/Os of the board. Since the purpose of this FPC is to be implanted subcraneally or subcutaneously, the board has a flexible tail 5 or 10cm long that connects the NMIC with an external aggregator module. This integrated system is shown in Figure 5.8.

An aggregator module can be used to simultaneously communicate with several NMIC's to achieve high channel count systems. As part of this effort, we use a field programmable gate array (FPGA) as aggregator module to interface with up to 16 chips. Consequently, an adapter board between the FPC and the FPGA is necessary. We designed a series of adapter boards to, initially, connect one FPC system to the FPGA and then expanded the adapter to allow connection of all 16 boards. The final version of this adapter board includes voltage lever translators to interface the 3V logic of the FPGA with the 1.5V logic of the NMIC and

includes voltage regulation to power the chips with batteries in order to minimize noise in the neural recordings. An added benefit of this configuration, is that the total length of the connection between the FPGA and the NMIC can be twice as a long as a direct connection between the two components; the level translator acts as a relay that prevents data packet corruption. Figure 5.9 shows the version history of these adapter boards.

This whole system has been tested on a bench-top setup to record sinusoidal signals. In one example, we apply differential signals to the landing pads of the thin film electrodes on the FPC and record them with the NMIC as shown in Figure 5.11. Then, a similar experiment is performed in which the differential signal is applied to the polyimide electrodes immersed in phosphate buffered solution as shown in Figure 5.12

Incorporation of silicon carbide

The main challenge to overcome of the polyimide probes described in the sections above is their limited lifetime once implanted within neural tissue. These probes have been specifically designed to be minimally invasive with the purpose of causing as little damage to the brain tissue as possible and the purpose of bypassing the body's immune system due to their small footprint. Specifically, failure of the electrode insulation may occur through pinholes inherently present in very thin polyimide films ($<2\mu$m), degradation of these thin films in a time scale of months (rather than decades) and degradation of the polyimide-polyimide interface in the lateral dimension (metal to polyimide edge in this probes may be as little as $<2\mu$m).

Adding a-SiC to the insulating layer of these probes may significantly improve the chronic performance of the system. It was demonstrated in earlier chapters that our a-SiC insulating films are remarkably stable in accelerated aging tests. However, these films lack the mechanical properties necessary for probe insertion; SiC is a brittle ceramic that would crack when the needle threads through the head loop and pulls on the electrode. Suitable electrodes will require the mechanical properties of the polymer and the long term stability of the carbide. In this manner, once the probes have been implanted in the brain and the polyimide insulation begins to fail, a-SiC will still provide good, stable insulation to the metal traces.

Some significant changes need be considered when adding a-SiC insulation to the polyimide probes. First, material compatibility with the PECVD chamber and process temperature do not allow traditional photoresist lift off patterning of these carbide films. Second, release of polyimide devices from the carrier wafer relies on water diffusion through the polymer; regions of a-SiC with large surface area must be minimized to allow proper release. The current and proposed cross sections of the polyimide probes are shown in Figure 5.13. The fabrication process to achieve this structure would be as follows:

- Cast and cure 1-2μm polyimide film on a silicon wafer.
- (Optional) Deposit <50nm of PVD SiC at room temperature.
- Deposit 500-1000nm of PECVD SiC at 350^{o}C.

- Lift off patterning of e-beam evaporated Ti/Pt.
- Deposit 500-1000nm of PECVD SiC at 350°C.
- (Optional) Deposit <50nm of PVD SiC at room temperature.
- DRIE patterning of SiC that stops on the bottom polyimide.
- Cast and cure 1-2μm polyimide film on silicon wafer.

The remaining steps of the SiC process follow the non-SiC process. The addition of SiC on top of the metal structures has the added benefit of protecting the exposed bond pads and active sites from residue left after oxygen plasma etch of the polymer; clean metal surfaces are critical for subsequent electroplating steps. Use of these thin SiC films combined with polyimide results in a flexible, minimally invasive neural probe with superb, stable insulation.

5.3 Chapter figures

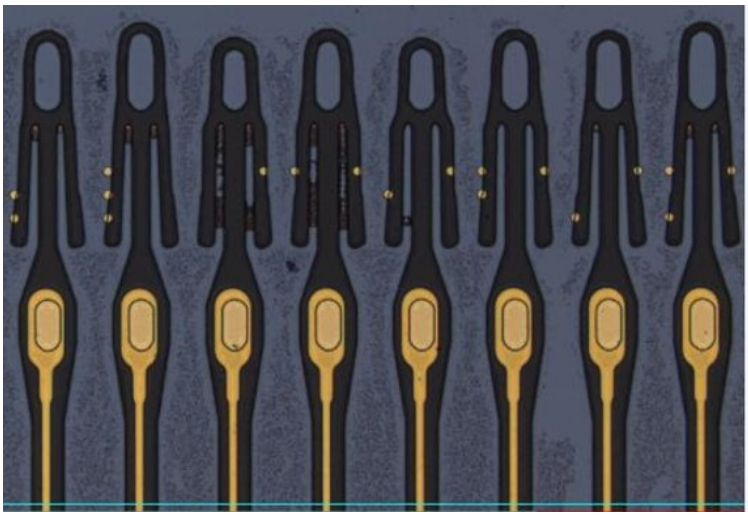

Figure 5.1: Optical image of polyimide electrode heads. In this particular example, metallization is Cr/Au. Electrode shank is 20μm.

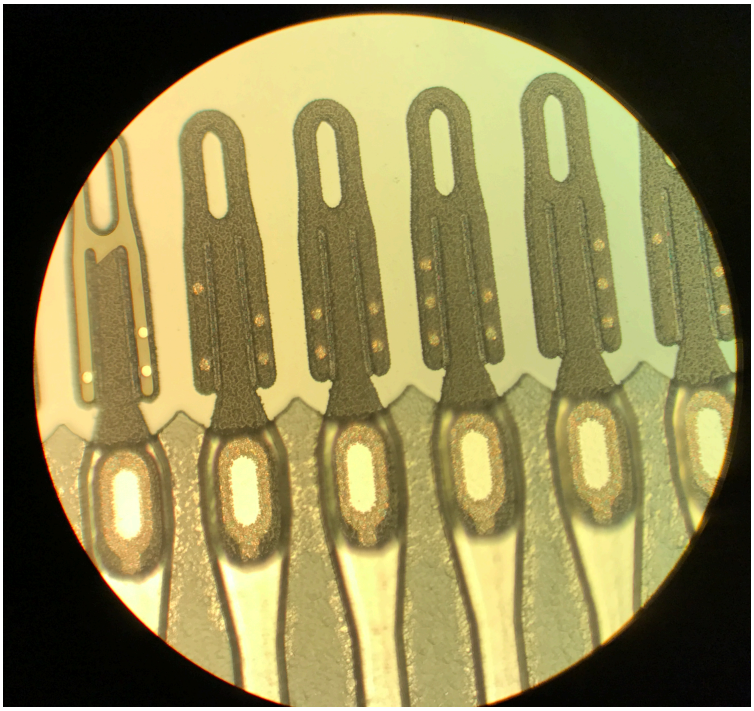

Figure 5.2: Optical image of PI electrodes kept in place by parylene sheet. Electrode shank is 20μm.

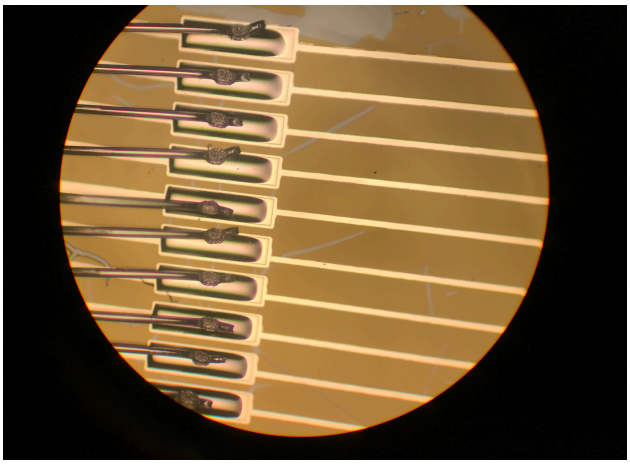

Figure 5.3: Optical image of PI electroplated bondpads. The nickel bump has an uniform and shiny surface that permits proper wirebonding. Bondpads are 100μm by 350μm.

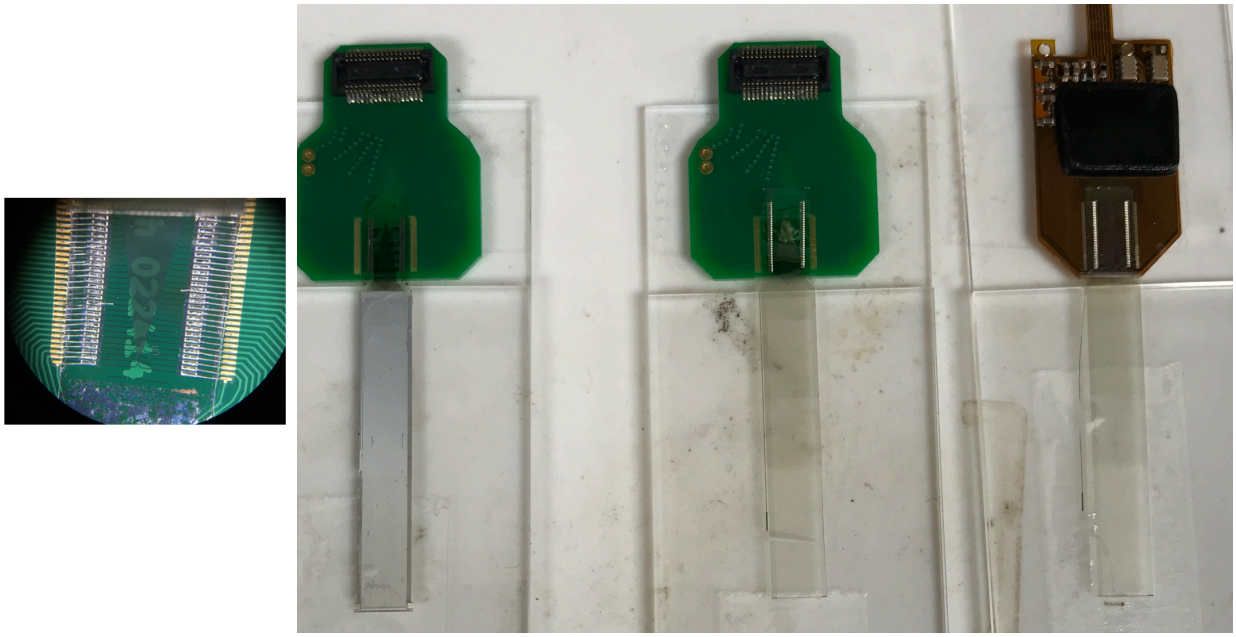

Figure 5.4: Optical image of assembled polyimide electrode arrays. On the right, a photo a 64 electrodes properly wirebonded to the PCB and on the left a photo of to arrays assembled to PCBs and one assembled to FCP.

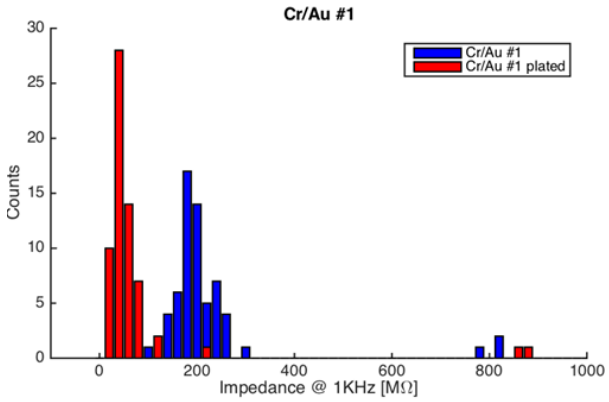

Figure 5.5: Characteristic impedance of polyimide electrode arrays. For some arrays, mean impedance is about 30kΩ at 1kHz, appropriate for electrophysiology.

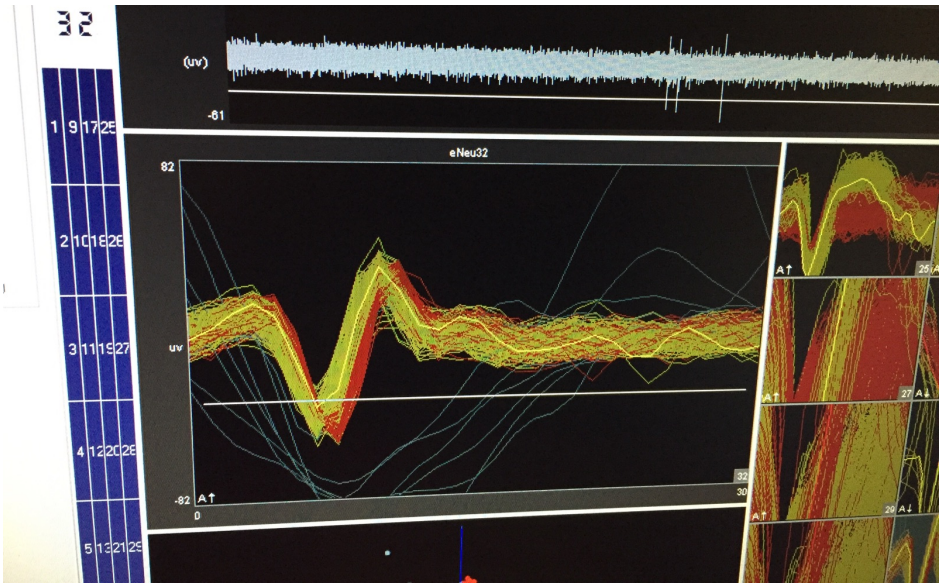

Figure 5.6: Example of neural recordings done with polyimide electrodes implanted in rat primary sensory cortex.

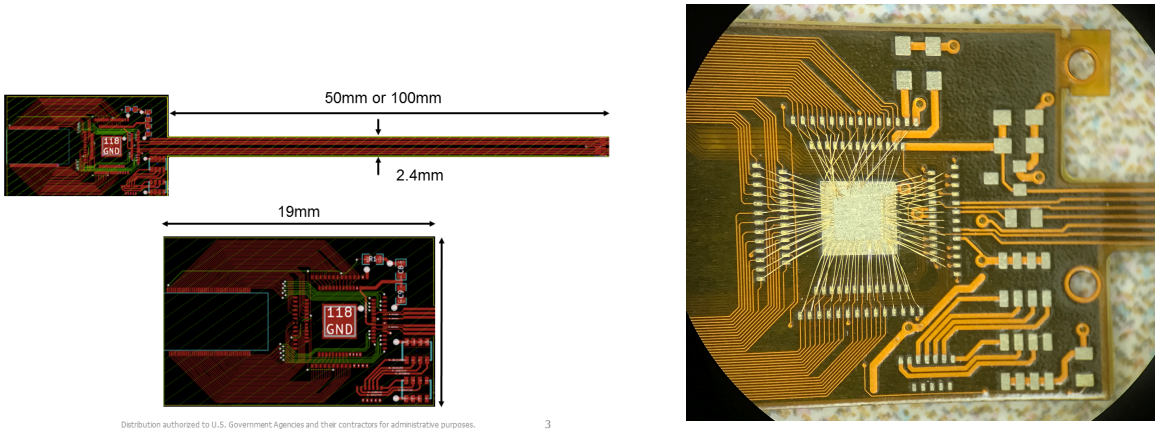

Figure 5.7: Flexible circuit board for integration of NMIC and polyimide electrodes. Figure on the left shows the CAD designs and dimensions and figure on the right shows a photo of the actual board with test wirebonds.

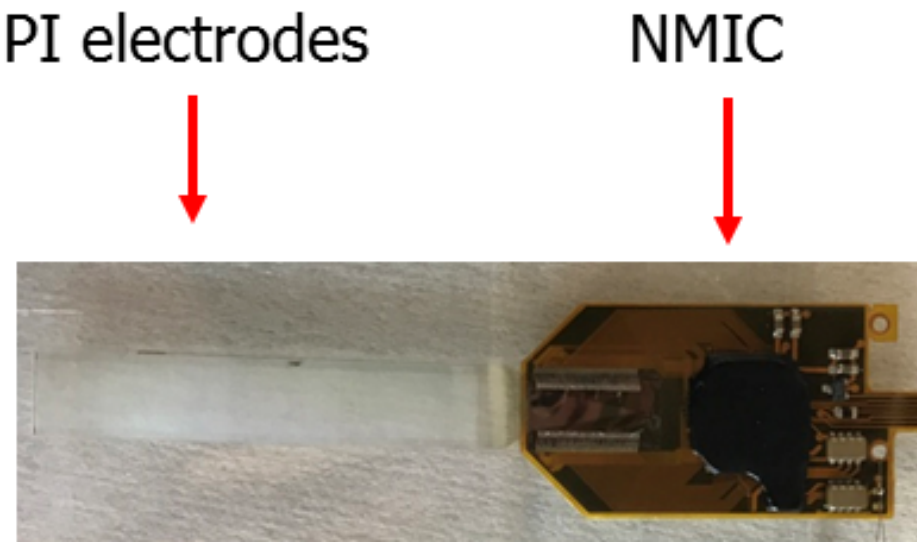

Figure 5.8: Photo of integrated NMIC and PI electrodes in FPC. NMIC has been wirbonded to FPC followed by surface mounting of passive components. Polyimide electrodes have been epoxied to the board and wirebonded.

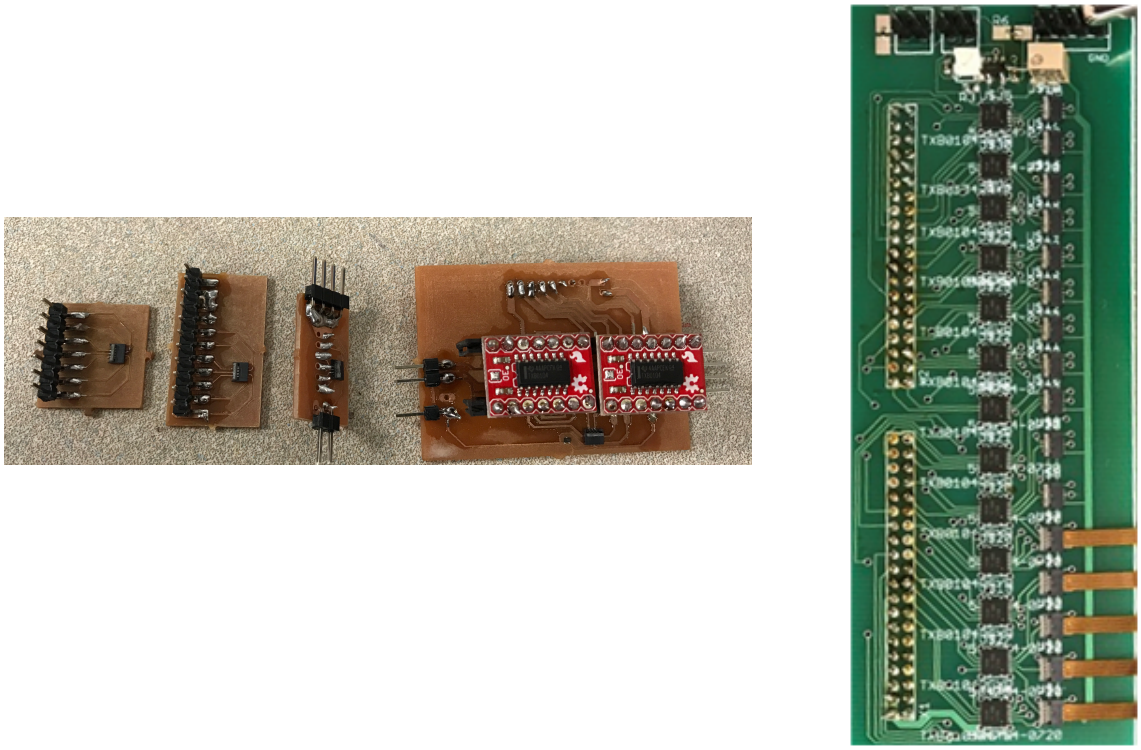

Figure 5.9: Evolution of Adapter boards for FPC-FPGA connection. First versions were just breakout boards of the 7-pin molex connector. Later versions incorporated level shifters and voltage regulators for noise reduction. Last version on the right can connect up to 16 NMICs.

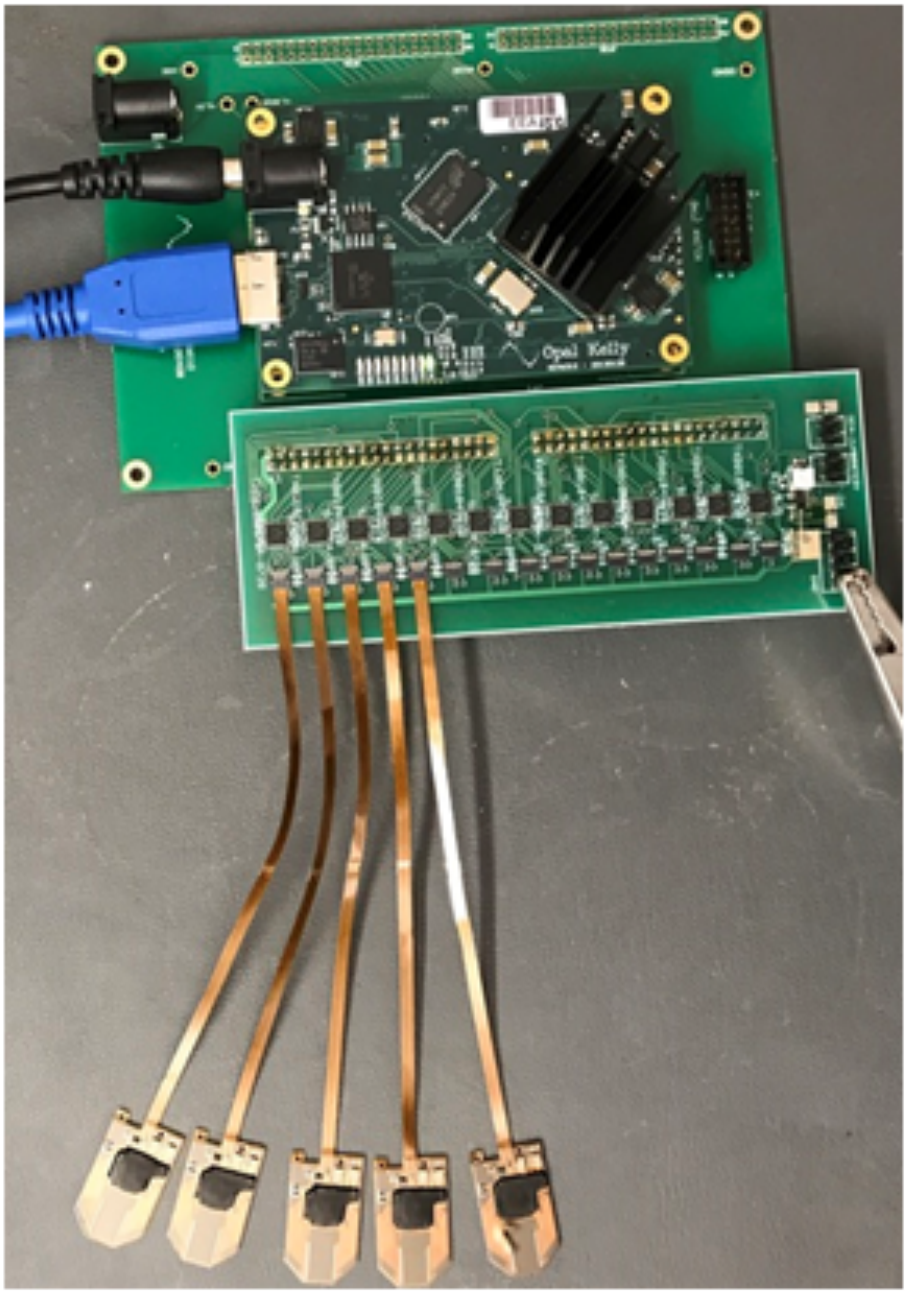

Figure 5.10: Complete system showing 5 NMICs connected to the FPGA via the adapter board.

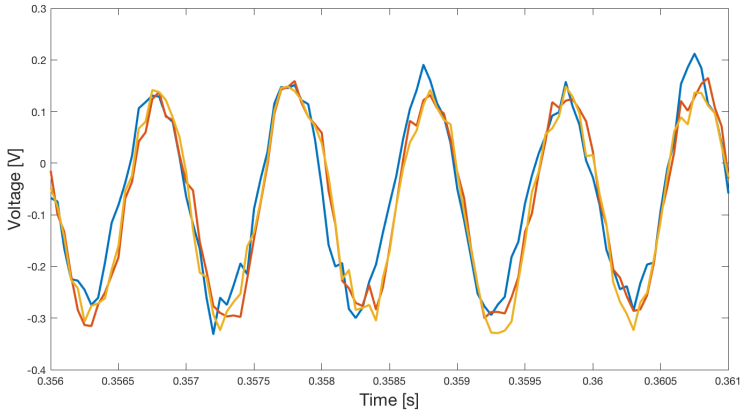

Figure 5.11: Example of a 1kHz differential signal being applied directly to the bondpads on the FPC. The NMIC can reliably record such a signal.

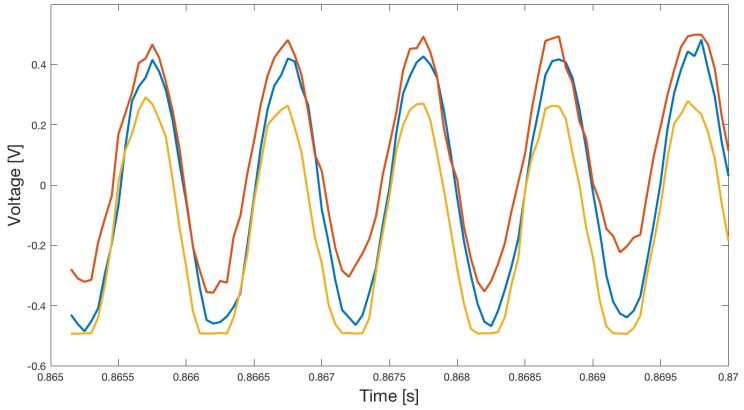

Figure 5.12: Example of NMIC recording through polyimide electrode. A 1kHz differential signal was applied to a saline solution in which the polyimide electrodes had been immersed.

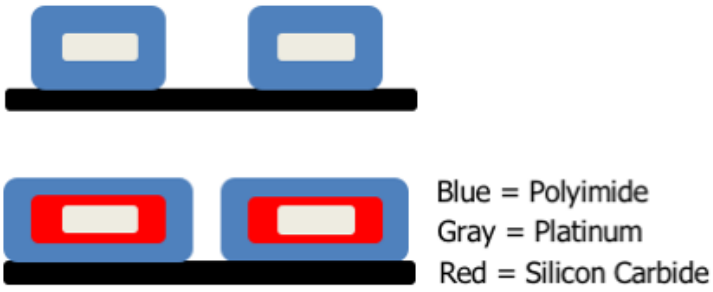

Figure 5.13: Cross section of polyimide probes. Top shows current design and bottom shows proposed design that incorporates a-SiC

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