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UNIVERSITY OF CALIFORNIA,
IRVINE

Semiconductor Chip Electrical Interconnection and Bonding by Nano-Locking

DISSERTATION

submitted in partial satisfaction of the requirements
for the degree of

DOCTOR OF PHILOSOPHY

in Engineering

by

Jielin Guo

Dissertation Committee:
Professor Frank G. Shi, Chair
Professor James Earthman
Professor Lizhi Sun

2021

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DEDICATION

To

my distinguished professor Frank G. Shi, my dearest husband, my beloved parents, and my friends with their unconditional love and support to offer me strength and courage and made it possible for me to complete this work.
Thank you all.

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CURRICULUM VITAE

Jielin Guo

2009-2013 Bachelor of Science

Electrical Engineering

Harbin University of Science and Technology

2013-2016 Master of Science

Electrical Engineering

Xi'an Jiaotong University

2016-2021 Doctor of Philosophy in Engineering

Materials and Manufacturing Technology

University of California, Irvine

2019.1-2020.6 Packaging Engineer Internship at *Skyworks Solutions Inc*. Part-time

2020.6-2020.9 Packaging R &D Engineer Internship at *Intel Corporation.* Full-time

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ABSTRACT OF THE DISSERTATION

Semiconductor Chip Electrical Interconnection and Bonding by Nano-Locking

By

Jielin Guo

Doctor of Philosophy in Engineering

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University of California, Irvine, 2021

Professor Frank G. Shi, Chair

Nowadays, the relentless needs for increasing functionality and speed of ubiquitous electronic and optoelectronic devices with reduced cost, size and weight call for novel on-chip and off-chip interconnect technologies. Thus, in addition to the continuing overall push for an ever shrinking pitch size of off-chip interconnections, there are compelling reasons to seek an alternative chip bonding approach enabling simultaneous mechanical, thermal and electrical interconnections with a much reduced vertical dimension than what can be achieved by the current mainstream bump and bumpless methods.

This dissertation explored a new die-attach method used for die-substrate electrical interconnection without requiring a prior time-consuming and expensive surface nanoscopic planarization and without requiring any intermediate conductive material. A chip bonding method with a concept of "nano-locking" (NL) is proposed: The new method takes advantage of the intrinsic nanoscopic surface roughness on the interconnecting surfaces: the two surfaces are locked together for electrical interconnection and bonding with a conventional die bonder, and the connection is stabilized by a dielectric adhesive filled into nanoscale valleys on the interconnecting surfaces.

This “nano-locking” (NL) method for chip interconnection and bonding is demonstrated by its successful application for the attachment of high-power GaN based semiconductor dies to its device substrate.

In Chapter3, the electrical, thermal and optical performances of devices enabled by the present NL bonding are evaluated. The resulting bond-line thickness of devices enable by NL bonding approach achieved is shown to be as low as 30 nm, several hundred times thinner than those achieved using mainstream bonding methods, resulting in a lower overall device thermal resistance, and a reduced electrical resistance, and thus an improved overall device performance.

In Chapter4, the wet high temperature operating life test and thermal cycling test are performed to evaluate the reliability of the packaged devices enabled by the NL bonding method and compared with the conventional Ag-epoxy and AuSn bonding approach. The experimental results help demonstrate the fact that the NL bonding approach helps reduce the risk of interfacial delamination during bonding operation and the chances of commonly observed failure caused by interfacial delamination and the mechanical breakdown can be significantly reduced without adding the conductive metallic fillers.

Chapter5 and Chapter6 focused on the study on the influence of bond-line thickness (BLT) and surface morphology on the device performance and reliability. The performances and reliability of the devices enabled by the NL bonding method follows a power law relationship with the different BLT and different density of surface height distribution and leads to different value of electrical and thermal resistance.

The present work opens a new direction for the scalable, reliable and simple nanoscale off-chip electrical interconnection and bonding for nano- and micro-electrical devices. In addition, the

present method applies to the bonding of any surfaces with intrinsic or engineered surface nanoscopic structures as well.

Chapter1

Introduction and Background

Nowadays, the relentless needs for increasing functionality and speed of ubiquitous electronic and optoelectronic devices with reduced cost, size and weight call for novel on-chip and off-chip interconnect technologies. Although significant innovations in design and process technologies are ongoing, to continue the drive to the next nodes, Moore's Law economics are coming to an end and some key performance metrics at advanced nodes are plateauing. It is much difficult to enhance the performance of a chip-to-package electrical bonding by size scaling, which often suffers from electrical and reliability issues [1]. System-on-chips including chiplets, enabled by 2.5D and 3D integration of dies from separate or the same wafers onto a single chip, represents a new paradigm for advantages beyond Moore's law [2]. This new paradigm is essential to the further development of innovative electrical interconnection technologies for die-to-die, die-to-wafer, die-to-interposer, die-to-substrate or board, die-to-redistribution layer, and wafer-to-wafer, interpose-to-substrate interconnections [3]. The semiconductor packaging technology progression from dual in line (DIP) to surface mount technology (SMT) and then developed to area array packages such as ball grid array (BGA) to achieve higher I/O density as shown in Fig. 1.1. For off-chip electrical interconnections, bump and bumpless methods are two mainstream ones. In bump-based interconnection with thermocompression or thermosonic bonding, which has a relatively low throughput due to the long process time, two interconnecting metallic surfaces are bonded together using electrically conductive bumps made of conductive adhesives such as solders, Cu bumps, or other conductive materials. The most advanced mainstream bump is made of copper pillars with the smallest interconnect pitch achieved being 40 μm, i.e., a 25 μm Cu bump with 15 μm spacing. It becomes a serious challenge to

further shrink the Cu bump pitch: although a 20 µm pitch is possible from a lithography standpoint, the difficulty lies in other process steps including the strict surface nanoscale flatness requirement [4].

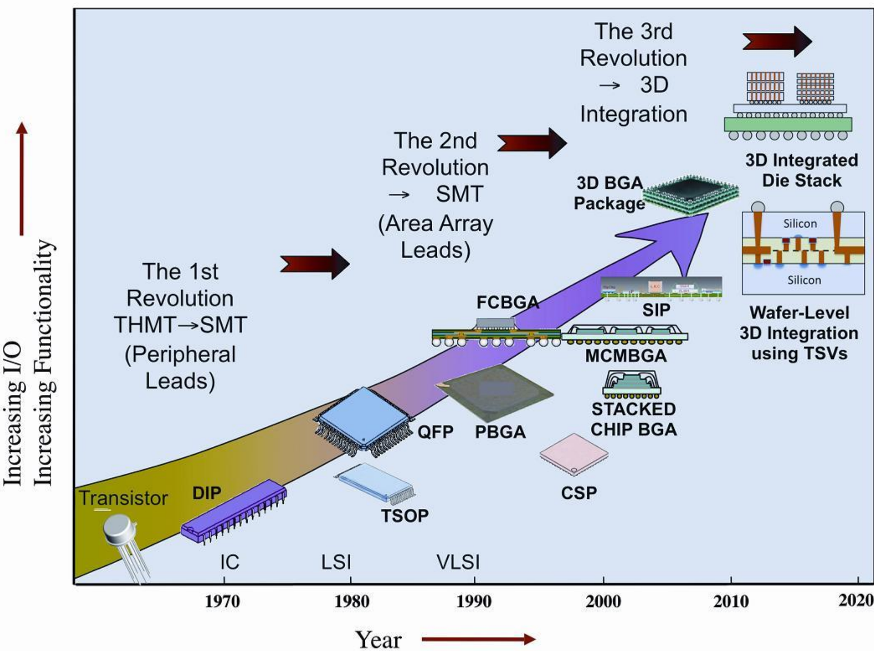


Figure 1.1 Electronic packaging trend. Source: Electronics Cooling [5]

The bumpless method eliminates the need for intermediate conductive bump and the warpage or delamination issue associated with the bumps and die stacking with a pitch down to 2 µm or lower becomes possible. Achieving a good bumpless Cu-to-Cu bonding requires precise control over the nanoscale topography of the interconnecting surfaces which thus must be well planarized by using chemical mechanical polishing to reduce the respective surface roughness below 0.1 nm, and in some cases, the surfaces must also be plasma activated in an ultra-high vacuum of 10^{-4}~10^{-7} Pa, before eventually undergoing a low temperature annealing around 300°C [6].

Although the interconnection pitch has a paramount significance for enhancing the integrated density of silicon dies, it is noted that the overall purpose of various integration schemes is to reduce the device power consumption and to increase the device speed at a lower cost. Thus, in addition to

interconnection pitch, the vertical thickness of the interconnection is also critical since it contributes to the overall thermal and electrical resistance of the resulting devices. For example, with a 3D die stack, the potential hot spot within the middle of the stack could be a challenging thermal management and cost issue, which contribute to its much slower commercial adoption than interposer-based 2.5D integration that has less thermal related issues, even though the 3D IC design and architecture have been explored for several decades [7].

The significance of the vertical interconnecting dimension or bond-line thickness (BLT) is even more evident in the case of die-to-substrate bonding in power devices based on wide band gap (WBG) SiC and GaN, which are being explored as another route to extend Moore's law and to replace silicon for many needed emerging devices and applications under high power, high temperature, high frequency, high radiation and other harsh working conditions [8-9]. However, the apparent potential of WBG semiconductors cannot be fully realized until a more advanced die bonding with much lower thermal and electrical resistance can be established, although many bump-based bonding methods including nano-silver sintering have been explored for decades [10].

Thus, in addition to the continuing overall push for an ever shrinking pitch size of off-chip interconnections, there are compelling reasons to seek an alternative chip bonding approach that enabling simultaneous mechanical, thermal and electrical interconnections with a much reduced vertical dimension than what can be achieved by the current mainstream bump and bumpless methods.

1.1 Overview of Microelectronic Packaging

An integration of many circuits or components on a single chip is defined as an integrated circuit (IC). Packaging is the bridge that interconnects the ICs and other components into a system-level

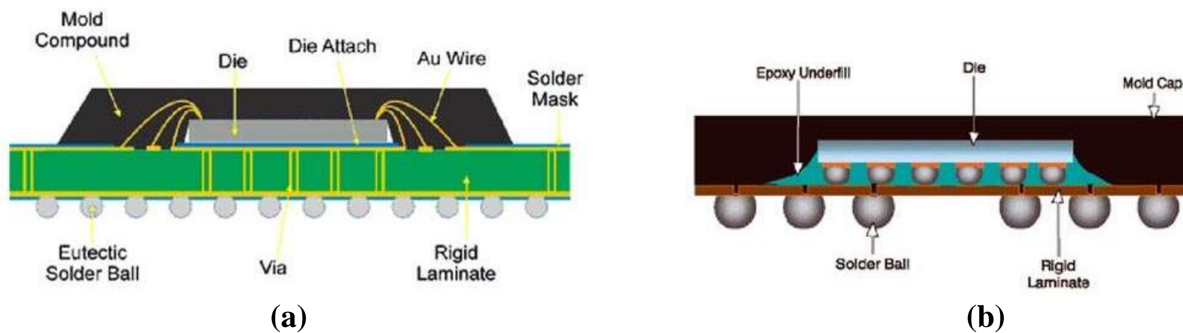
board to form electronic products [11]. IC packaging has three important parameters: the amount of I/O which determines the pitch of the IC package as well as the wiring needs at the system level, the size of the IC which affects the reliability of the IC to package connection and the power which affects the heat dissipation and properties of IC and system level packaging.

The electronic packaging has following four main functions: (1) signal distribution; (2) power distribution, involving electromagnetic, structural, and material aspects; (3) heat dissipation (thermal management); (4) protection (mechanical, chemical, electromagnetic) of components and interconnections. These enables the IC package to protect, power, and cool the microelectronic device and to provide an electrical and mechanical connection between the chip and the outside world.

The package interconnects may be classified to die-to-die interconnects, die-to-package interconnects, also known as first level interconnect (FLI), package-to-board interconnect, also known as the second level interconnect (SLI). In this study, the focus is on the first-level packaging that the die is bonded to the substrate. The bonding can take place with a conductive or non-conductive adhesive layer. Electrical interconnection is made possible through a variety of materials and techniques such as wire bonds, Cu pillars, solder bumps, eutectic solder adhesives or conductive epoxy-based adhesives. Two types of first-level interconnection dominate the industry: 1) wire bonding and (2) flip-chip attachment. The wire bonding consists of ball bonds and wedge bonds. The flip-chip attachment technology is used to improve the high integrated density and shorten the signal travel distance, the die is flipped over and facing directly down to the substrate and without using of bond wire. In order to enhance the reliability of flip-chip technology, epoxy based underfill are applied to redistribute the thermo-mechanical stress caused by coefficient of thermal expansion (CTE) mismatch between the die and substrate [12]. After die bonding process, the encapsulant will be applied as the molding cap to protect the die from environmental effects. Three types of molding

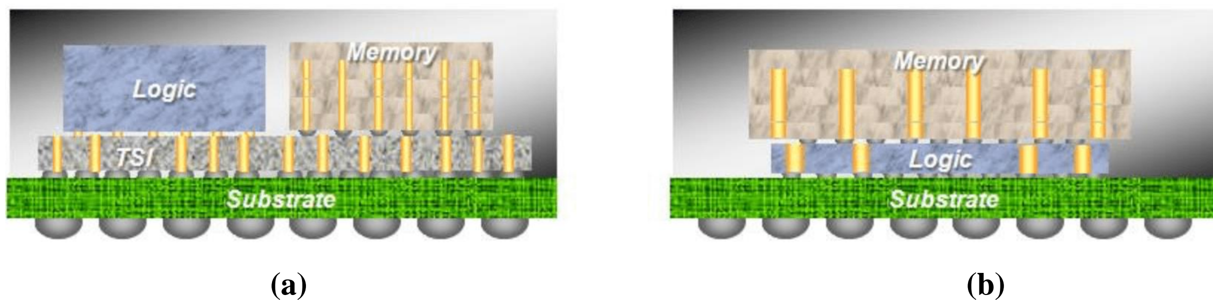
are involved: compression molding, transfer molding and injection molding. Typical first level interconnect wire bonding and flip-chip packaging technologies are shown in Fig.1.2.

The recent semiconductor industry is embracing multi-chip package (MCP), integrates a number of ICs in a single packaging structure. It is done either by multi-chip modules (MCMs) in the planar fashion or by 3D stacked-chip packaging referred to as system-in-package (SiP) which incorporates ICs stacked vertically. The advanced 2.5D and 3D integration that can stack different functional components vertically in a single package is very promising technology to overcome the physical, technological, and economic limitations that encountered in planar ICs, extending Moore's law and enabling "More than Moore" applications. Typical 2.5D and 3D IC package are shown in Fig.1.3.



(a) **(b)**

Figure 1.2 Typical first level interconnect (a) wire bonding (b) flip-chip package. Source: Amkor



(a) **(b)**

Figure 1.3 Schematic illustration of typical (a) 2.5D and (b) 3D IC package. Source: ASE/SPIL

The 3D integration is classified in three main categories:1) stacking of packages (or substrates); 2) stacking of embedded dies (without TSVs); 3) 3D TSV technology in high volume manufacturing

[13,14]. Generally, 3D integration schemes rely on traditional interconnect methods such as wire bonding and flip chip to achieve vertical stacks [15]. The key technologies in 3D integration are wafer thinning and dicing, chip/wafer stacking, bonding, through-silicon via (TSV) and its associated underfill materials. Through-silicon via (TSV) is a vertical electrical interconnection (via) that passes completely through a silicon wafer or die that the reduced vertical interconnect length and substantially high integrated density. In addition, the TSVs enable reduced latency, lower capacitance and inductance and permit higher speed communications which form higher numbers of interconnections and lower power level communication links between circuits [16].

To continue Moore's Law, the heterogeneous integration is proposed to build large systems out of smaller functions [17]. Heterogeneous integration refers to the integration of separately manufactured components into a higher-level assembly (System in Package, SiP) which provides enhanced functionality, smaller size, lower latency, lighter weight and lower cost [18]. In heterogenous integration, components such as dies with different feature size can be integrated into a single package as shown in Fig.1.4. 3D heterogeneous integration includes the following three main categories: 1) 3D System-on-Chip (3D-SoC); 2) 3D Wafer-level Packaging (3D-WLP); 3) 3D System-in-Package (3D-SiP) [19].

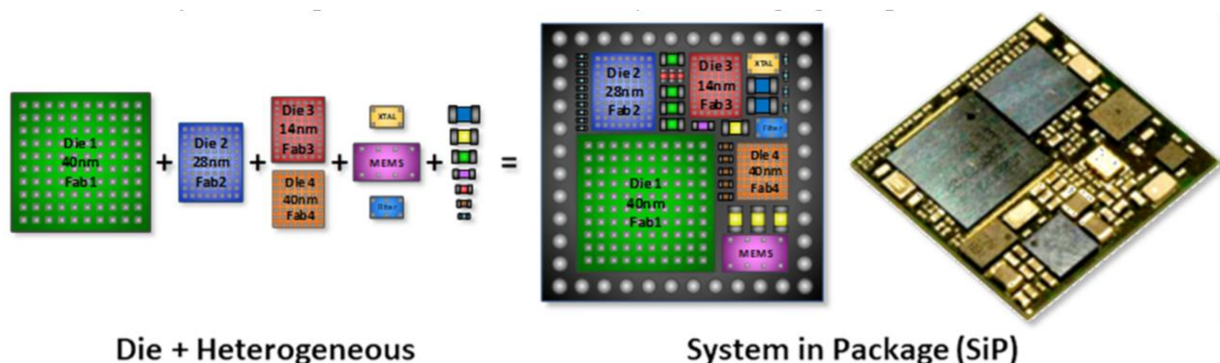


Figure 1.4 Heterogeneous integration and system in package (SiP). Source: ASE

The primary driver for advanced packaging technologies is the need for increased interconnect densities to support heterogenous integration and deliver increasing bandwidth. Key challenges will continue to be in fine pitch sort, thermal management, power delivery and reliability for high volume manufacturing.

1.2 Die-Attach Materials in Semiconductor Package

Die-attach is the process of attaching the die to the support structure (die cavity or die pad) of the semiconductor package and provide the electrical interconnection between the die and substrate. The two key functions of die attach materials are to ensure the heat dissipation and mechanical fixation of the die on substrate. The attach materials used in the package play an important role in degerming the overall performance, reliability and lifetime of the semiconductor devices.

The two commonly used die-attach materials include electrically conductive adhesives (ECAs) and eutectic alloy solders. The ECAs are consisted of a polymeric binder matrices and conductive metallic fillers. The conductive fillers provide the electrical conduction and the polymetric matrices provide the physical and mechanical properties. There are two types of ECAs: 1) isotropically conductive adhesives (ICAs) which are conductive equally in all directions and 2) anisotropically conductive adhesives (ACAs) which are only conductive in one direction, typically along the z-axis [20]. Figure 1.5 is the schematic drawing of ICA and ACA. For ICAs, they have been proposed as an alternative to tin/lead solders in surface mount technology, flip chip, and other applications [21]. For ACAs, the directional conductivity is achieved by using a relatively low volume loading of conductive filler (5-20 volume percent) which enables prevents conductivity in the x-y plane of adhesives.

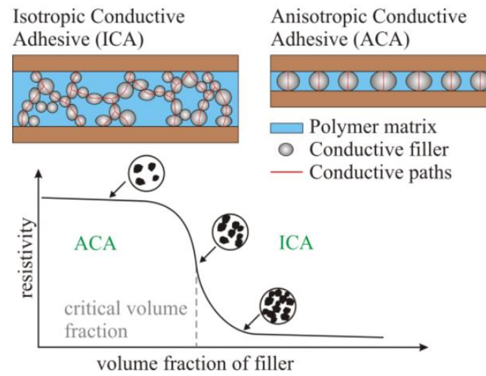


Figure 1.5 Electrically conductive adhesive types and effect of filler volume fraction [22].

For the lead-free interconnect materials, in soldering process, the molten solder reacts to a base metal to ignite the bonding. The bonding action is initiated by intermetallic compound (IMC) formation, which is a chemical reaction [23]. Take Sn-based Pb-free solder on copper as an example. During the soldering process, the solder melts and reacts with copper to form Cu_6Sn_5 intermetallic compound and link the solder and cupper together, also known as wetting action, on the interface as shown in Fig.1.6. The IMC formation occurs on all known soldering systems and the soldering process can't be successful without it. The key requirement for soldering is to remove or convert the oxides. The table 1.1 summarize some commonly used die-attach material.

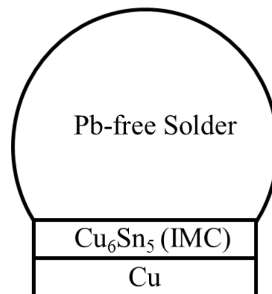


Figure 1.6 Illustration of IMC during the soldering process.

Table1.1 Commonly used die-attach materials in electronic packaging

Die-attach material	Remark
Electrically conductive adhesive (ECA) [Ag-epoxy]	Pros: high conductivity; reduced costs through reduction in number of processing steps; low curing temperatures; low thermal stresses; better fatigue resistance Cons: higher electrical and thermal resistance compared with solders; not compatible for high temperature electronics
Eutectic solder paste [Au80Sn20]	Pros: high thermal conductivity and excellent mechanical properties; Cons: high fabrication temperature
Lead free solder [SnAgCu]	Pros: high melting temperature Cons: formation of intermetallic compound and high fabrication temperature
Sintered nano-silver	Pros: high thermal and electrical conductivity Cons: expensive and excessive voiding
Non-conductive adhesive (NCA) [epoxy]	Pros: Avoid short circuits; ease of processing; cost-effectiveness Cons: No direct electrical interconnection

1.3 Flip-chip Interconnection Technology

Flip-chip technology was first invented by IBM in 1961 and it is an interconnect method where the semiconductor IC is manufactured such that the electrical terminals can be connected in a face down or flipped manner to the package substrate [24]. The schematic drawing of a flip-chip package is shown in Fig. 1.7. Flip-chip assembly becomes a mainstream packaging interconnect technology within the recent decades in response to the need for a relatively large number of highly reliable input/output connections in semiconductor devices. Several types of flip-chip interconnects being used today: solder bumps, Cu pillar bumps, solder pastes, electrically conductive adhesives, sintering nano-silver, Cu-Cu bonding etc.

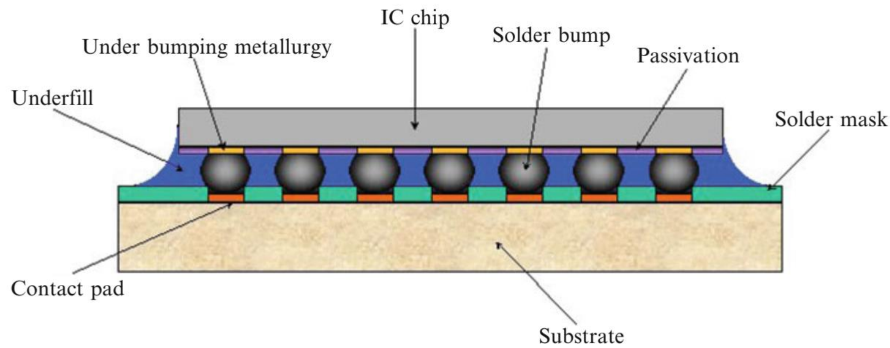


Figure 1.7 Schematic configuration of typical flip chip package with underfill [25].

Pb-free solders such as SnCu, SnAg, and SnAgCu are used in flip-chip technology. The solder bumping includes a series of steps: 1) the incoming wafers with open via to process; 2) the under bump metallization (UBM) is applied by plating; 3) a photoresist is deposited and patterned on the wafer over the device pads for bumping; 4) the solder metallurgy is then plated to deposit the appropriate solder composition on the chip pads; 5) the photoresist is stripped from the wafer and the UBM metallization is then removed; 6) the solder bumps are then reflowed to form characteristic truncated sphere shapes [26].

Cu pillar is introduced as an alternative to the conventional solder bumps for first level flip-chip interconnections [27]. The Cu pillar bump is an emerging technology for high performance packaging since it offers fine pitch capabilities. Cu pillar is fabricated over a variety of spacing on a Cu-seed layer. A solder cap can be optionally plated on top of Cu pillar and subsequently reflowed form a solder bump or cap. Figure 1.8 illustrates the schematic drawing of solder bump and Cu pillar bump with solder cap.

The anisotropic conductive adhesives are employed for electrical interconnection in flip-chip technology. By controlling the particle volume fraction in the adhesive below the percolation, the insulation in x-y plane is ensured. The conductive particles used are typically solid metal or metal

plated polymer spheres. During the bonding process, it is essential and important to remain precise alignment, electrical contact, parallelism and uniform pressure. There are several requirements for the selection of the adhesive materials. The coefficient of thermal expansion of the particles should be matched to the adhesive. Besides, the glass transition temperature, adhesion strength, modulus of the adhesive and its resistance to moisture are all important to maintain processing capability and reliability.

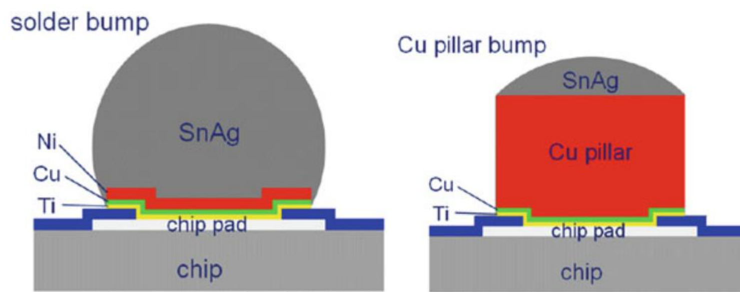


Figure 1.8 Schematic drawing of a conventional solder bump and a copper pillar with solder cap [28].

Metal to metal solid state diffusion bonding of Cu-Cu and Au-Au has been widely used in IC stacking. The advantages of using metal to metal bonding are the formation of a non-melting micro-joint during the sequential stacking processes which enables good heat transfer and reliable mechanical support. Cu-Cu bonding is achieved by thermo compression under bonding pressure with high temperature. The cleanliness of surface before bonding is very important which are influenced by the surface oxide, contamination, hardness and surface roughness in achieving successful bonding. The annealing step using N_2 or N_2-H_2 gas is essential to get higher bonding strength by allowing Cu interdiffusion and grain growth. Figure 1.9 shows the example of Cu-Cu bonding technology.

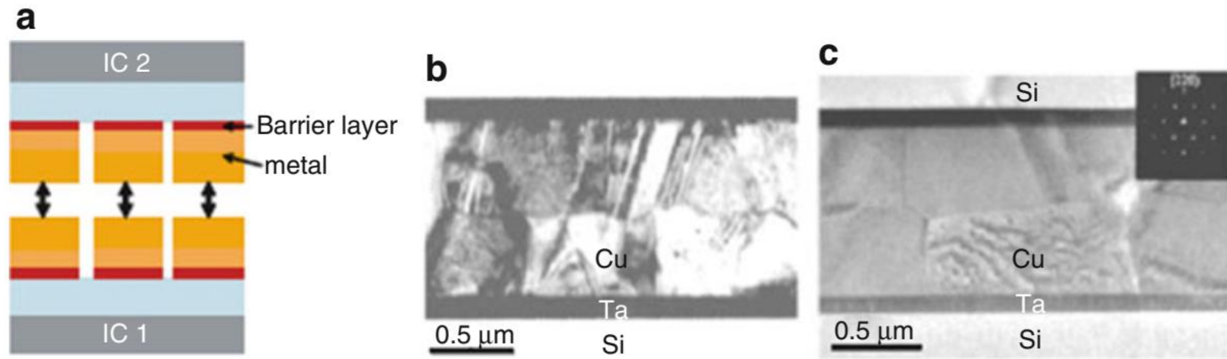


Figure 1.9 (a) IC stacking using Cu-Cu bonding, (b) cross-sectional TEM image of Cu-Cu bond (c) after annealing (no visible interface) [29].

As the physical feature size continues to shrink according to Moore's law, the flip-chip technology has steadily advanced to accommodate the interconnection requirements by decreasing bump size and pitch as well as increasing the number of interconnecting bumps. Conventional underfill is applied to reduce the CTE mismatch between the die and substrate. Epoxy resin mixed with inorganic fillers are often used as typical underfill material by flowing into the gap between the die and substrate.

1.4 Light Emitting Diode (LED)

Light-emitting diode (LED) is a semiconductor light source that emits a narrow spectrum of light when the electric current flows through it. The recombination of electrons and electron holes in a semiconductor produces light. The working principle of LED is shown in Fig.1.10. As shown in the Fig.1.10, the n-type region has a high electron concentration and p-type region has a high hole concentration, electrons diffuse from n-type side to p-type side. Similarly, the holes flow by diffusion from p-type side to n-type side. Resulting in an electron field at the junction and forming the depletion region which allows electrical current pass through the junction in only one direction. It is widely

applied for outdoor lighting, automotive headlamps, traffic signals, camera flashes etc. For mini- and micro-LEDs are used for the advanced display technology. According to the peak wavelength of emitted photos, modern LEDs can be classified as visible LEDs, ultraviolet LEDs, and infrared LEDs [30]. The dominant wavelength of visible LEDs ranges from 400 to 760 nm.

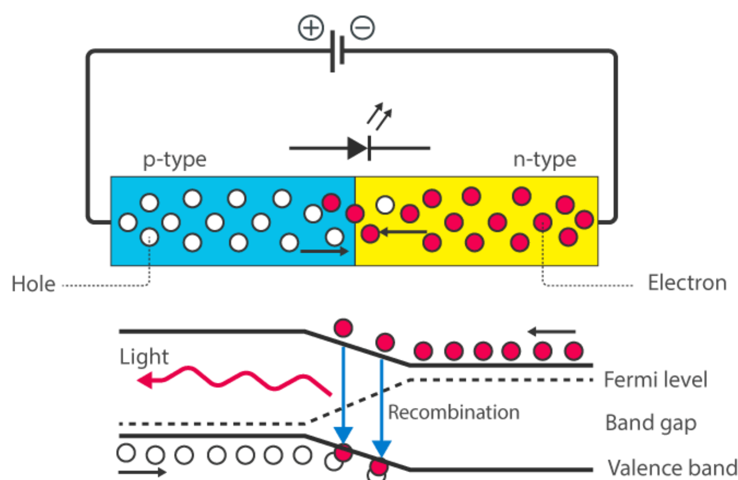


Figure 1.10 Working principle of LED. Source: BYJU'S

Based on the different structures of GaN based junction configuration, LEDs can be classified as lateral LEDs, flip chip LEDs and vertical LEDs. Figure 1.11 shows these three-types of chip structure. The conventional lateral type of LED consists of sapphire substrate, GaN buffer layer, n-GaN layer, p-GaN layer, electrodes and active layer. Inside the active layer multi-quantum well (MQW) lead to electron-hole combination and light emission. GaN-based LED is the most popular LED which is grown on the sapphire (Al_2O_3). The light efficiency of lateral structure is not high, function needs high forward voltage, and heat dissipation in the chip is poor due to the low thermal conductivity of sapphire substrate.

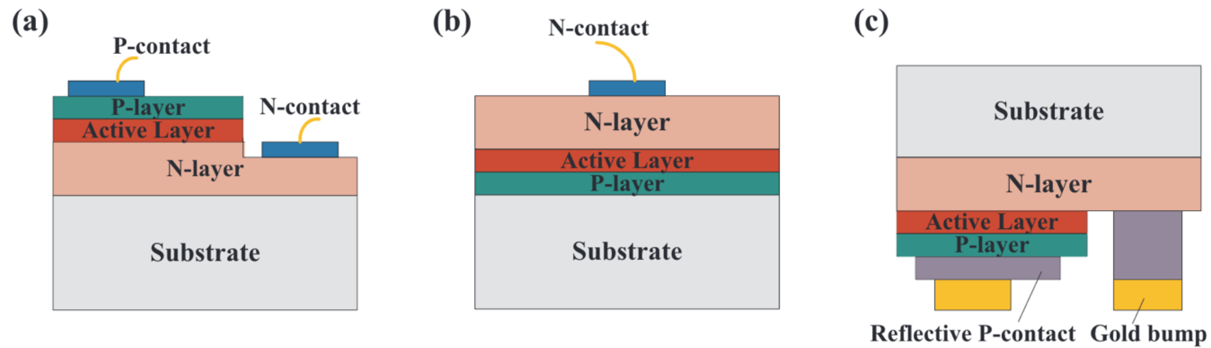


Figure 1.11 Three common types of high-power LED structure: (a) lateral LED, (b) vertical LED, (c) flip-chip LED [31].

The LEDs with vertical structure have been introduced recently to address the aforementioned shortcomings. In the vertical design, the electrodes are placed on both the top and bottom of LED chips. Vertical LEDs could grow on thermal/electrically conductive substrate such as Si, SiC and metal alloys. Compared to the conventional lateral LEDs, the vertical LEDs possess uniform current spreading, smaller thermal resistance and series electrical resistance.

The third type of LED structure is the flip-chip, in this configuration LED dies are flipped over and facing down bonded onto the substrate by metal bump or a uniform bonding layer. In the flip-chip design, the sapphire layer with low thermal conductivity is not within the heat dissipation path and the generated heat can flow downward through the thinner epitaxial material, solder/bonding later and substrate; accordingly, thermal performance of this structure is considerably improved, and thus high-power operation can be achieved with this configuration. A drawback in the manufacturing and packaging process of these structures is the precision alignment needed for bonding metals pads onto the substrate.

The LED light extraction efficiency is greatly influenced by the packaging materials used. Ideally, all the electron-hole pairs should be combined, and the input power should be converted 100% into

optical power. However, the only 70%~85% of electrical power is converted into heat generation. The increase in junction temperature of LED chips will also result in reduction of output power, forward voltage and mean time of failure, additionally shifting of the output wavelength can occur [32].

The electrical interconnection between LED die and package substrate mainly includes wire bonding and flip chip bonding. In wire bonding, most LED's failures are induced by the break-down of ultra-thin gold wire. Furthermore, with the progress of LED industry towards high power, high density and low cost, flip chip bonding has attracted more attentions and the interconnection between LED die and package substrate improve the heat dissipation.

1.5 Thermal Management in Semiconductor Packaging: Role of Die-attach Material

The electrical energy supplied to electronic devices will ultimately transform into heat dissipation and accompanied by a temperature rise at the heat source followed by the transport of heat to regions of lower temperature within and outside of the electronic package. For the inside of the package, the heat flux flows through the process of thermal conduction in the solid material that making up the package. When the heat reaches the external surfaces of the package, it usually transfers to a cooling fluid via a thermal convection process. The temperature within the semiconductor package is supposed to continue rising until the rate of heat removal from the package is equal to the rate of heat generation. However, the resulting temperatures would be too high in most cases and become the major failure for the electronic devices as shown in Fig.1.12.

The high packaging density leads to increasing heat flux levels at both the chip and module package. There are three fundamental mechanisms of heat transport from the generation source to the external environment: thermal conduction, convection and radiation. The task of maintaining

relatively low device and package temperature while keep supporting the increased heat fluxes has become one of the most challenges facing today. The die-attach material is the bottleneck for effective heat dissipation among the packaged device.

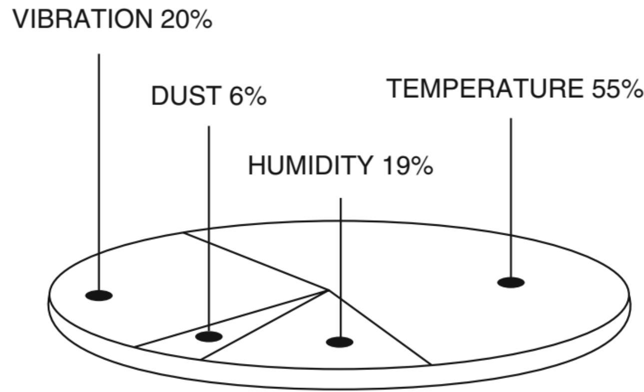


Figure 1.12 Major causes of electronic failures in U.S.A.F. Avionics Integrity Program Study [33].

Locally high heat fluxes can result large local temperature increases which is often called as hot spots. The thermal design objectives for the packaged devices includes the followings. The temperature of all components needs to be maintained within specific functional limits. Besides, a cooling system needs to be designed to meet the overall system reliability. Thermal interface materials (TIMs) are used to bond the heat spreader with the back side of the chip package. The goal of TIM is to mechanically couple the back side of the chip to the heat spreader while also provide heat conduction. Another important attribute of TIM is its coefficient of thermal expansion, because it acts as the interlayer between a chip and a substrate with significantly different CTEs, the CTE of TIM should be matched with two other bonding surfaces. Studies have shown that 60% of the thermal resistance of a system is in TIMs [34]. TIM thermal resistance $R_{TIM} = \frac{BLT}{k_{TIM}} + R_{c1} + R_{C2}$, where BLT

is the bond line thickness, k_{TIM} is the thermal conductivity of the TIM material, R_{c1} and R_{C2} are the thermal contact resistance between the TIM and the bonding surface.

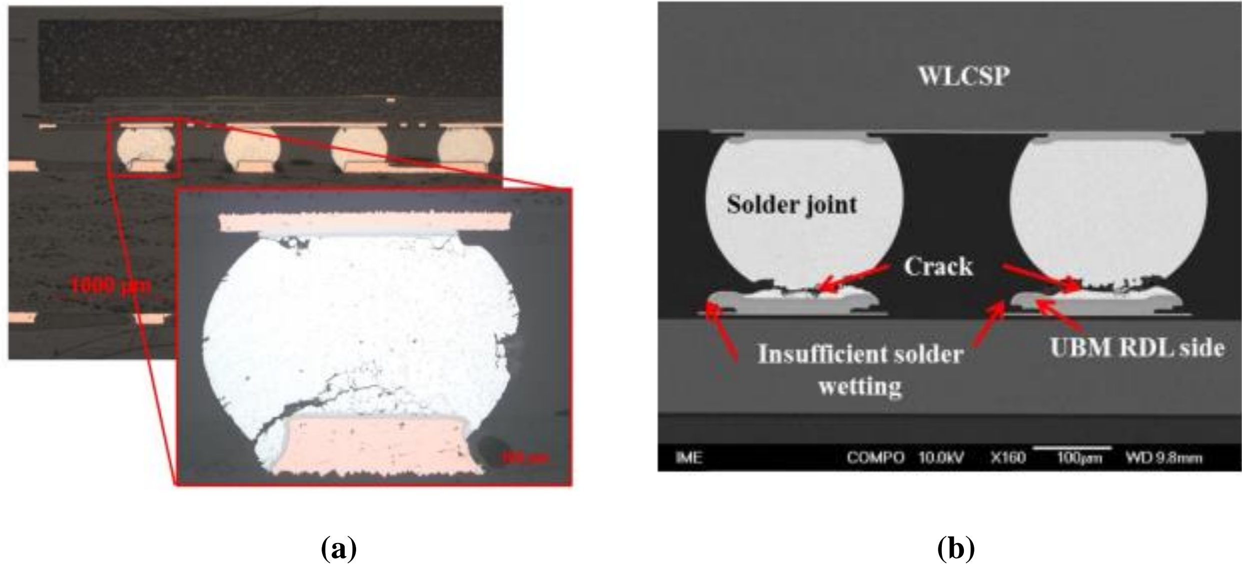
1.6 Reliability for Chip Interconnection and Bonding

The reliability of chip interconnection and bonding is highly dependent on the properties of the constituent components and the interfaces formed between the chip and package substrate. Chip-package interconnection can cause chip cracking, solder bump cracking, package substrate trace cracking, and delamination of underfill encapsulation for the flip chip assembly.

For eutectic AuSn bonding, the primary reliability issues arise from defects introduced during processing (voids, irregular phase formation, weak interfaces due to insufficient barrier metals, etc.) that act as crack initiation sites [35]. The failure modes of the interconnection include delamination, solder ball fatigue/ball crack due to the poor adhesion at interfaces between die and package substrate. Or crack formation and propagation within the under-bump metallization, intermetallic compound, or solder interconnect as descript in [36-38]. In addition, there also exists Cu pad peeling off problem and crack happened to Cu trace at the corner of the package of top wafer level chip scale packaging (WLCSP) and cracks happened to solder joints on back redistribution layer (RDL) side. Figure 1.13 shows the failure mode in solder balls.

For electrically conductive adhesives, the delamination caused by poor adhesion which occurs with both ICAs and ACAs can weaken the mechanical strength of the interconnection. Under high humidity bias environment, moisture can penetrate through the package and the water will degrade the polymers by reacting with them by producing hydroxyl and carbonyl end groups [39]. The silver flakes in ECA are prone to oxidation and can cause problems for adhesive interconnections. In addition, it has been observed that when the ECA interconnection is thermally cycled over its lass transition temperature, the silver flakes may start to segregate. This leads to open circuit as the

particles move away from the other pad. Besides, other impact factors such as air bubbles within an ACA interconnection may retain moisture diffusing and cause short circuits.



(a) (b)

Figure 1.13 (a) Cross section of control BGA after 4400 thermal cycles at High Mean thermal profile [40]. (b) Failure mechanism of the package edge solder joints of top WLCSP with details of cracking on RDL side [41].

The reliability of the second level interconnection and bonding can be evaluated by a number of different methods, including wet high temperature operating life test (WHTOL), thermal cycling (TC), thermal shock (TS), highly accelerated temperature and humidity stress test (HAST), high temperature storage test (HTSL) etc. The environmental tests and conditions are summarized and shown in Table 1.2.

Table 1.2 Environmental Tests & Conditions

Environmental Stress Test	Abbr.	Specification	Stress Conditions	Requirements
Preconditioning	PRECON	JESD22-A113	/	Pass level
Temperature Cycling Test	TC	JESD22-A104	-65℃~+150℃	500 cls 3× 0/25
Temperature Humidity Bias	THB	JESD22-A101	85℃, 85% RH, Biased	1000hr 3× 0/25
Highly Accelerated Stress Test	HAST	JESD22-A110	130℃, 85% RH, Biased	96hr 3× 0/25
Highly Temperature Storage Test	HTSL	JESD22-A103	150℃	1000hr 3× 0/25
High Temperature Operating Life	HTOL	JESD22-A108	150℃ (junction), Biased	1000hr 3× 0/77
Pressure Cooker Test	PPOT	JESD22-A102	121℃, 100% RH, Unbiased	96hr 3× 0/25

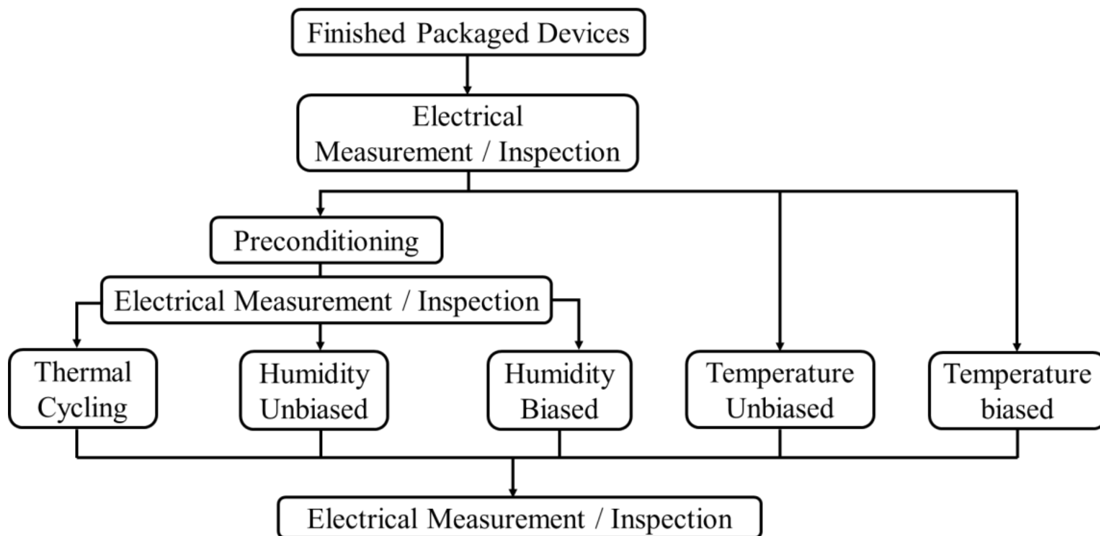


Figure 1.14 Environmental reliability stress test flow.

To study the root cause of the failure mechanism, Fig. 1.14 shows the environmental reliability stress test flow of integrated circuits. These tests are capable of stimulating and precipitating semiconductor device and packaging failures [42]. The objective is to precipitating failures in an accelerated manner compared to use conditions.

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Chapter 2

New Methodology: "Nano-locking" (NL) Chip Bonding

2.1 "Nano-locking" (NL) Chip Bonding Method

In this Chapter, an innovative off-chip interconnection method is proposed free of any electrically conductive metallic fillers by using only pure dielectric adhesive to achieve the die-substrate bonding between semiconductor die and device package substrate. This NL bonding method has been successfully applied to the die-substrate bonding process of high-power LED. A detailed study of the present "nano-locking" structure is illustrated, the electrical and thermal conduction mechanism between bonding surfaces and the fabrication of packaged devices enabled by the NL bonding approach is presented and demonstrated. Besides, the impact factors for the electrical and thermal resistance of the NL bonding layer is also fully discussed and the microstructure of the scalable bond-line thickness is also observed.

2.1.1 "Nano-Locking" Structure for Electrical Interconnection

The "nano-locking" chip bonding approach refers to the bonding between two surfaces using dielectric adhesive (silicone) without adding any conductive fillers to achieve the electrical and thermal conduction between the electronic component and package substrate. Fig. 2.1 illustrates the interconnection and bonding between two surfaces with exact matching structures without any intermediate material. In general, however, the intrinsic surface structures are not as exactly matching as in Fig. 2.1, but they are random as shown in Fig. 2.2. For any microscopically flat surface, intrinsic surface nanoscale structures are unavoidable. The electrical interconnection of such two metallic

surfaces can be established when the nanoscopic structures from the interconnecting surfaces are brought to be in contact, and such an interconnection can be mechanically stabilized and by filling the nanoscopic valleys with a structural adhesive, as illustrated in Fig. 2.2. This process is sufficiently simple in concept, it has never been demonstrated for semiconductor die electrical connection and bonding, and it can be performed with a simple bonder.

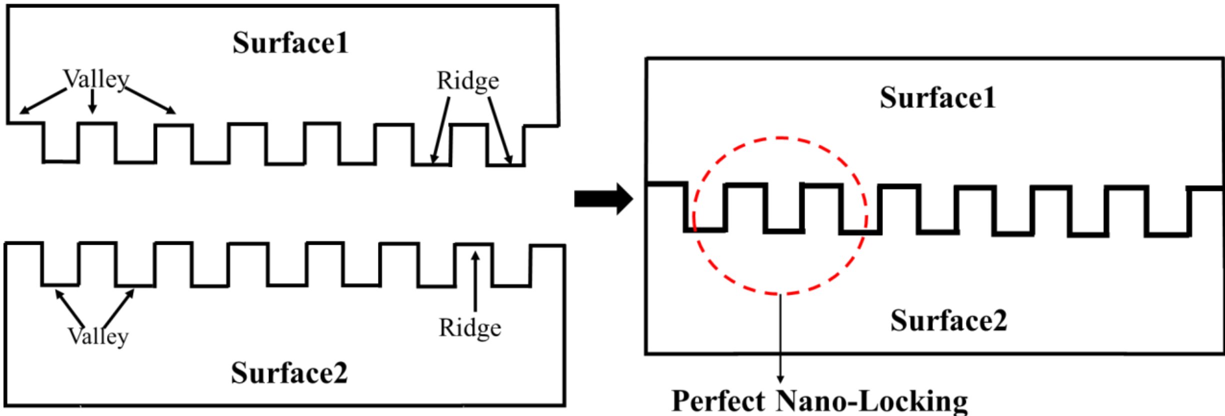


Figure 2.1 Schematic illustration of the Nano-Locking (NL) method for chip interconnection and bonding: a perfect locking for two surfaces with exact matching structures.

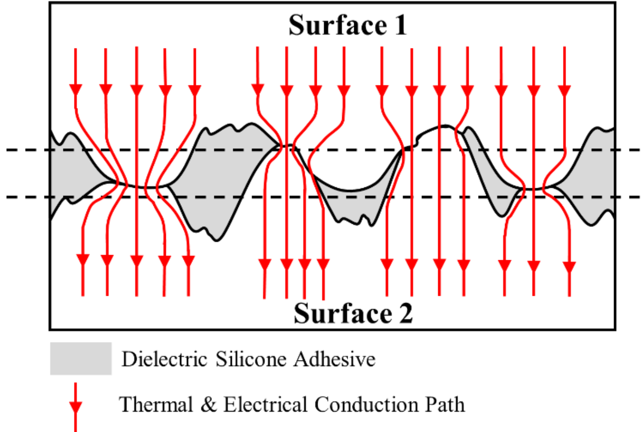


Figure 2.2 Schematic illustration of the Nano-Locking (NL) method for chip interconnection and bonding: a locking for general interconnecting surfaces with random intrinsic structures: electrical and thermal interconnections are established (the indicated pathways) when the

surfaces are in contact, and the interconnection is stabilized and the two surfaces are bonded by the adhesive filled in the surface valleys (the gray area).

The bond-line thickness (BLT) is defined as the vertical distance between the baseline of the surface roughness on the two bonding surfaces as shown in Fig. 2.3 [1]. The BLT of the present NL bonding approach is scalable and its potential range is within the maximum and minimum limits, controlled by the highest ridges and deepest valleys on the interconnecting surfaces, as illustrated by Fig. 2.4(a) and (b): The maximum value results from the contacts between the highest ridges on die and substrate while the minimum value results from the contacts between the highest ridge and deepest valley of die and substrate. The specific BLT value (within the maximum and minimum range) obtained during a die bonding process is dependent on the bonding pressure.

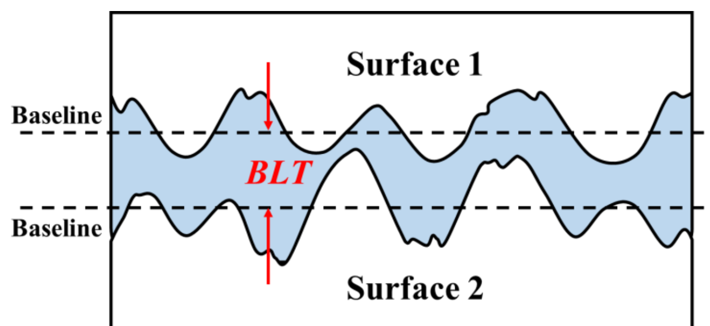
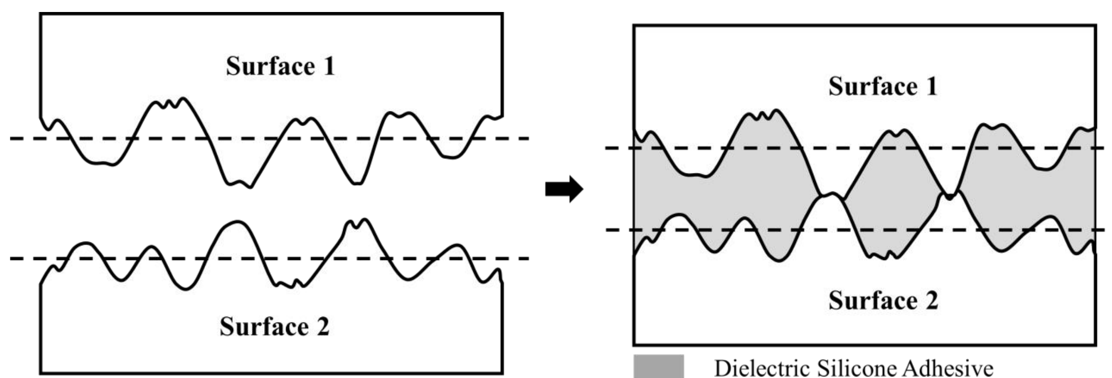
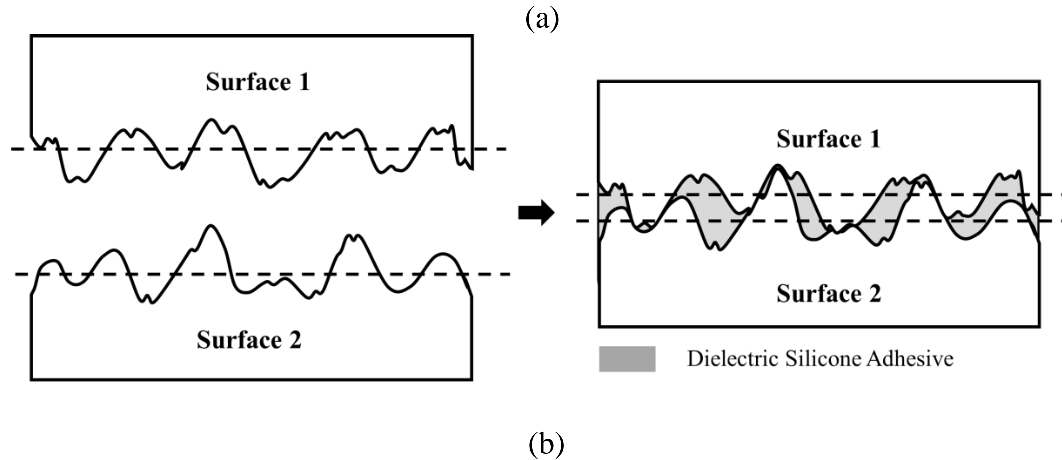


Figure 2.3 Schematic illustration of the bond-line thickness (BLT): vertical distance between the baseline of the surface roughness on the two bonding surfaces.



(a)



(b)

Figure 2.4 Schematic illustration of the BLT limits: (a) the maximum BLT; (b) the minimum BLT. The maximum BLT is achieved when the two highest ridges on two surfaces are contact with each other, and the minimum BLT is reached when the highest ridge on surface 2 is contact with the deepest valley on surface 1.

2.1.2 Surface Topographical Characterization of Metallic Pads on Chip and Substrate

The atomic force microscopy (AFM) was employed to investigate the surface topographies of the metallic pads on the semiconductor die and package substrate before bonding together. The AFM microscopes are based on a unique non-optical surface interrogation technique. This is built on the fundamentals of scanning probe microscopy, which utilizes a physical probe to measure the surface features of samples with atomic resolution for lateral and height measurements. AFM microscopes operate on the principle of surface sensing using an extremely sharp tip on a micromachined silicon probe. This tip is used to image a sample by raster scanning back and forth over the sample surface, and the method varies dramatically between distinct operating modes [2]. The tip is on the end of a cantilever, which deflects when the tip encounters features on the sample surface. This deflection is sensed with an optical lever (red line): a laser beam reflecting off the end of the cantilever onto a segmented photodiode magnifies small cantilever deflections into large changes in the relative intensity of the laser light on the two segments of the photodiode as shown in Fig.2.5. In this way,

the AFM makes a topographic map of the sample surface. There are different modes in AFM imaging: contact mode, tapping or non-contact mode. The contact mode where the tip scans the sample in close contact with the surface. The force on the tip is repulsive with a mean value of 10^{-9} N. This force is set by pushing the cantilever against the sample surface with a piezoelectric positioning element. Tapping mode is a key advance in AFM and it overcomes problems associated with friction, adhesion, electrostatic forces, and other difficulties that an plague conventional AFM scanning methods by alternately placing the tip in contact with the surface to provide high resolution and then lifting the tip off the surface to avoid dragging the tip across the surface.

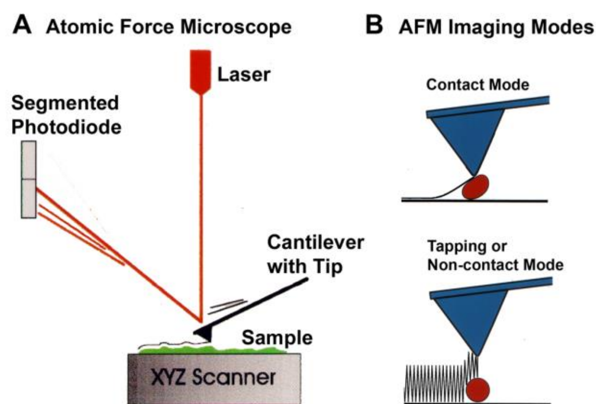


Figure 2.5 Schematic illustration of the working principle of atomic force microscopy (AFM) [3].

The surface roughness of metallic pads on die and substrate is determined by the atomic force microscopy (Anton Paar Tosca 400 AFM), using an Arrow NCR cantilever with a reflective aluminum coating which has a typical tip radius of < 10 nm, resonance frequency of 285 kHz and spring constant of 42 N/m. Images were acquired using a scan rate of 1 line/s. All images were collected in tapping mode with auto-slope correction. The scanning parameters such as the scan rate, Z frequency and Z gain were adjusted to optimize image quality. All AFM images were flattened

using a first-order polynomial in the X and Y directions to compensate for the bowing of the piezo tube.

The typical AFM images were obtained for 5 μm×5 μm scan area for the die and 50 μm×50 μm scan area for the substrate, and the co-ordinate (x, y and z) were defined and shown in Fig.2.6. The AFM surface topography and histogram of surface heights distribution are shown in Fig. 2.7 and Fig. 2.8. There are valleys and ridges on the surface of metallic pads: The surface height of the die metallic pad ranges from -78±2 nm to +64±2 nm and the surface height of the substrate metallic pad ranges from -113±2 nm to +100±2 nm.

From the surface height distribution shown in Fig. 2.7 and Fig. 2.8, the maximum BLT equals the sum of the highest ridges (on both die and substrate metallic pads) illustrated in Fig. 2.4 (a), with the max BLT =(100±2) + (64±2)=164±4 nm. Similarly, the minimum BLT equals the value of highest ridge (on substrate metallic pad) minus the value of deepest valley (on die metallic pad), as shown in Fig. 2.4 (b), with min BLT =(100±2) - (78±2) =22±4 nm. Therefore, the possible range of the BLT for the present NL bonding approach is 22±4~164±4 nm.

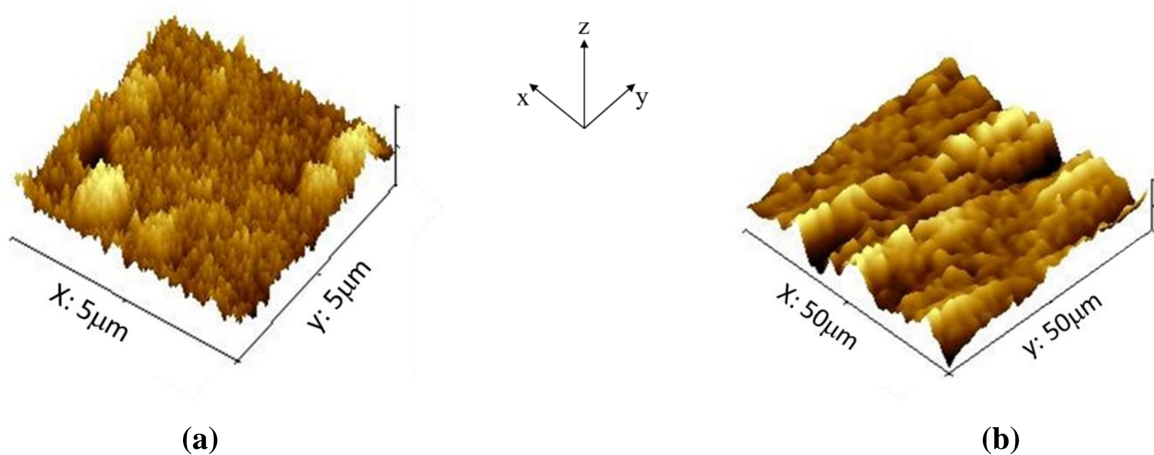


Figure 2.6 Definition of the test sample and test area of metallic pads on (a) semiconductor die and (b) substrate for AFM analysis.

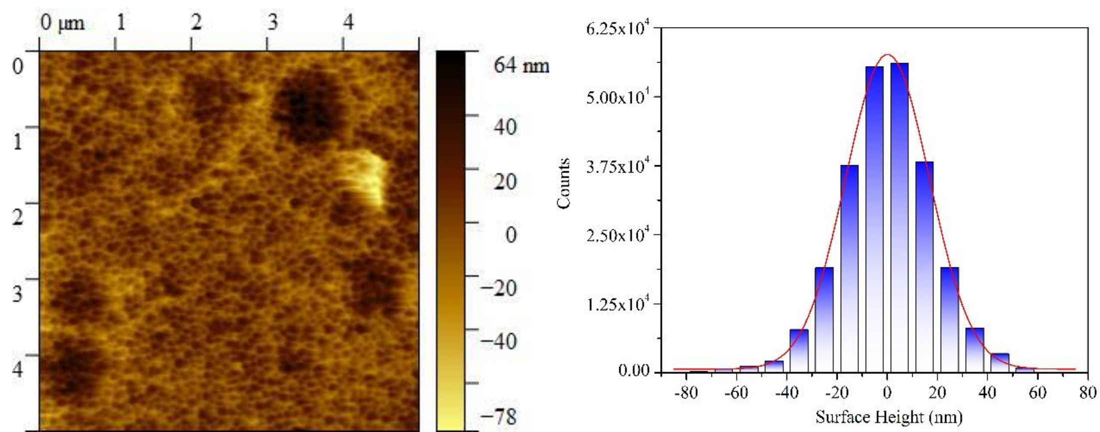


Figure 2.7 Atomic force microscopy for the topography and height distribution histogram of the surface roughness on the semiconductor die metallic pad.

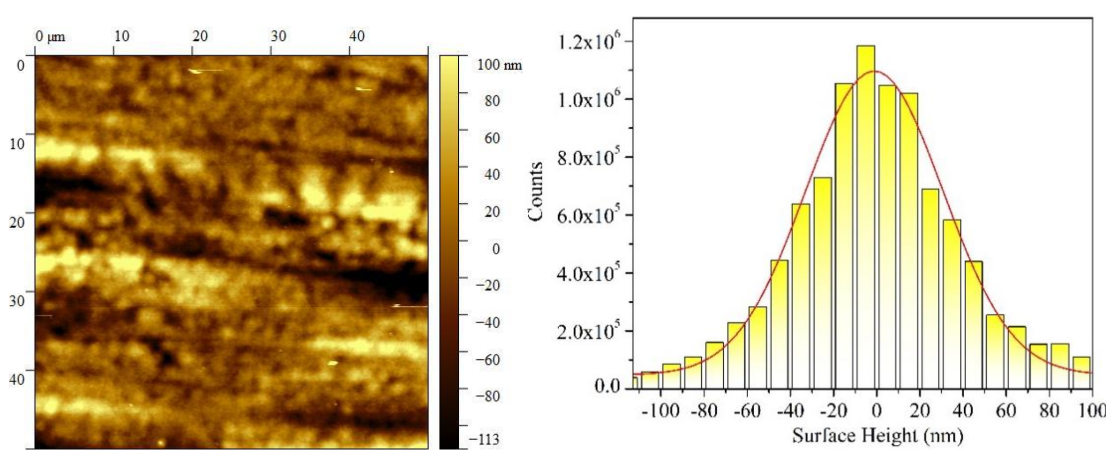


Figure 2.8 Atomic force microscopy for the topography and height distribution histogram of the surface roughness on the package substrate metallic pad.

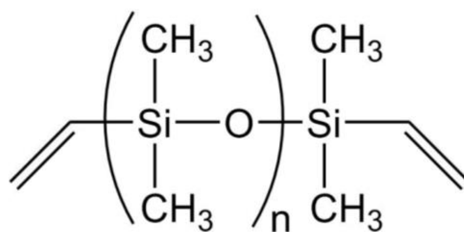
2.2 Fabrication of Packaged Devices Enabled by NL Bonding Method

2.2.1 Fabrication of the Dielectric Adhesive for Off-chip Bonding and Interconnection

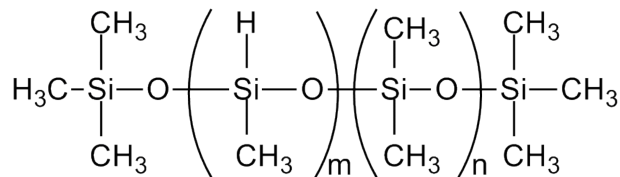
Polymetric materials such as epoxy resins, epoxy-phenolic resins, epoxy-silicone compositions, silicone resins, acrylics resins and polyimides are most used for adhesive in the electronics packaging industry [4]. Among them, silicone (Polyorganopolysiloxanes) resin with a repeating unit of

alternating silicon-oxygen (Si-O) siloxane backbone, has some unique chemistry. Silicone resins have a general formula of RnSiXmOy, where R is a nonreactive substituent, usually Me or Ph, and X is a functional group H, OH, Cl, or O. These groups are further condensed in many applications, to give highly cross-linked, insoluble polysiloxane networks [5]. Silicone adhesive is very useful in a variety of applications by virtue of its unique combination of properties, including high thermal stability, good moisture resistance, excellent flexibility, high ionic purity, and good adhesion to various substrates. Silicone adhesive is the most common organic matrix for optical die attach adhesives.

In this study, the dielectric adhesive used for die-substrate bonding is a kind of silicone-based mixture. The followings are the fabrication process: 1) DMS-V31 (vinly terminated polymidmethylsiloxane) and HMS-301 (25-35% methylhydrosiloxane-dimethylsiloxane copolymer, trimethylsiloxane terminated) from Gelest Inc. are mixed with a ratio of 7:3, and 1% of catalyst is added to help curing. 2) After fully stirring, the mixture is put into the vacuum oven for 0.5 h to degas until there is no bubbles coming out. Then the nano-dielectric adhesive is ready to use for the die bonding process.



(a) DMS-V31



(b) HMS-301

Fig.2.9 Chemical formula of silicone-based adhesive (a) DMS-V31 (vinly terminated polymidmethylsiloxane); (b) HMS-301 (25-35% methylhydrosiloxane-dimethylsiloxane copolymer, trimethylsiloxane terminated).

2.2.2 Fabrication of Packaged Devices with Different BLTs

The robustness of the NL method is demonstrated by bonding high-power GaN based dies to the device substrate, i.e., the bonding between the metallic pad on the semiconductor die and the pad on the package substrate, without using any intermediate conductive material, and without requiring a pre-bonding surface planarization. The as-received commercially available semiconductor dies and packages are employed in the present work. The dies used are flip-chip type light emitting diodes (LEDs) with the size of $1 \times 1\ \mathrm{mm}^2$ and a forward voltage of 3.0 V (San'an Optoelectronics Corp.). The specified maximum operating DC current is 700 mA with an emission peak at 455 nm. The composition of die pads consists of Ti/Ni/Au. The package substrate has a size of $5 \times 6\ \mathrm{mm}^2$ and consists of an optically reflective cup and the heatsink slug (Jufei Optoelectronics Corp.). The composition of substrate pad is Cu plated with Ag.

In this research, the packaged device is comprised of a flip-chip LED, a lead-frame with a reflector cup, a die attaching material and encapsulation. The fabrication process of the device packaging is shown in Fig.2.10 as follows: The semiconductor die bonder employed is a conventional Mech-EI manual die bonder. The dielectric adhesive is applied as the die-attach adhesive and fill the nanoscale valleys between the two interconnected bonding surfaces. Then it is subsequently cured in an oven at a temperature of 150°C for one and half hour. The encapsulation of the die-package is made by another commercially available silicone (OE-6630 resin, Dow Corning), and the encapsulation is completed by another thermal curing at 150°C for two hours. The packaged device is then soldered to an Al-based printed-circuit-board (PCB) before performing any property measurement.

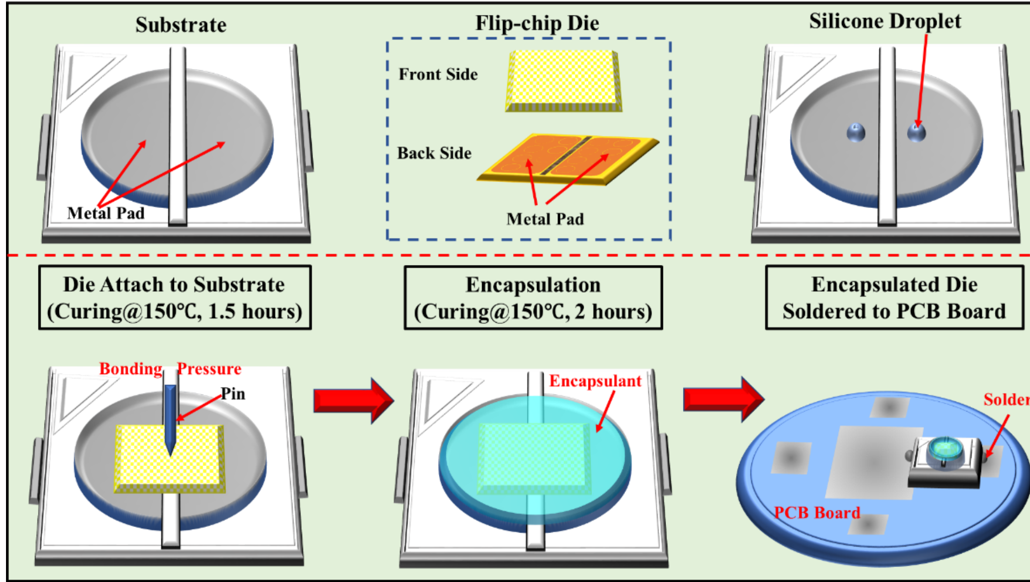


Fig.2.10 Fabrication of packaging process for flip-chip type high power LED.

As discussed above, the range of BLT is controlled by the bonding pressure and the amount of the silicone used during the die bonding process. Indeed, three sets of devices made using the present NL approach have the respective BLT value of 28±5 nm, 47±5 nm and 85±5 nm as shown in Table2.1, which are evidently within the BLT range.

For the purpose of comparison, the devices made by using conventional die-substrate bonding methods are prepared as shown in Table 2.2, i.e., one is bonded by using a commercial silver-epoxy adhesive with a silver flake amount of 85% by weight, and its volume resistivity is 8×10^{-5} Ωm; and another is bonded by using AuSn (80% gold and 20% tin) eutectic solder with a volume resistivity of 1.64×10^{-7} Ωm. The associated BLT is based on the industrial standard for reliability, i.e., 25 ± 2 μm for the silver-epoxy bonding and 20 ± 2 μm for the AuSn eutectic bonding, respectively [6].

Table 2.1 Packaged devices with different BLTs

Bond-line Thickness	NL-I	NL-II	NL-III
(nm)	28±5	47±5	85±5

Table 2.2 Electrical and thermal properties of different die-substrate bonding methods

Bonding Material	Electrical Resistivity (Ωm)	Thermal Conductivity (W/mK)
Silicone	1×10^{14}	0.2
Ag-epoxy	8×10^{-5}	60
AuSn	1.64×10^{-7}	57

2.3 Microstructure of NL Bonding Method

2.3.1 SEM/FIB Technique

The bond-line thickness of the packaged devices enabled by the NL bonding method is observed by the scanning electron microscopy/focused ion beam (SEM/FIB). SEM operates with high-resolution by scanning an electron beam over the sample and measuring the electrical interactions with the surface [7]. The electrons interact with atoms in the sample, producing various signals that contain information about the sample's surface topography and composition. The working mechanism of SEM is shown and illustrated in Fig. 2.11. The electrons are produced by a thermal emission source (tungsten filament): once the electrons are created, they are accelerated away from the filament by an applied voltage (up to 30,000 V) to pull them down towards the sample. The electrons then pass through a magnetic lens (condenser lens) which focus them to a spot (determines final spot size and the resolution of the SEM), and then through a scanning coil which bends the beam to the spot on the sample. By varying the current through the scanning coils with time, the position of the beam can be moved. Once the electron beam is focused down to a spot which then strikes the surface, the images can be created from a number of different signals such as high energy backscattered electrons, low energy secondary electrons, and characteristic X-rays. Signals can be collected using different detectors to form the final image. SEM uses electron beam to image and the

electron beam wavelength is far away from the visible wavelength of light used in conventional optical microscope. The contrast and brightness in the image critically are depended on the interaction between the electrons and the sample under study. Higher atomic number regions in the sample generally look brighter than lower atomic number regions because of scattering effect.

Focused Ion Beam (FIB) is a technique used particularly in the semiconductor industry, material science and increasingly in the biological field for material removal, deposition and site-specific analysis. A FIB setup is a scientific instrument that resembles a scanning electron microscope (SEM). FIB is widely used in microelectronics and very helpful in creating clean cross-sections to verify parameters, by avoiding smear effects that are typically induced when using conventional mechanical polishing.

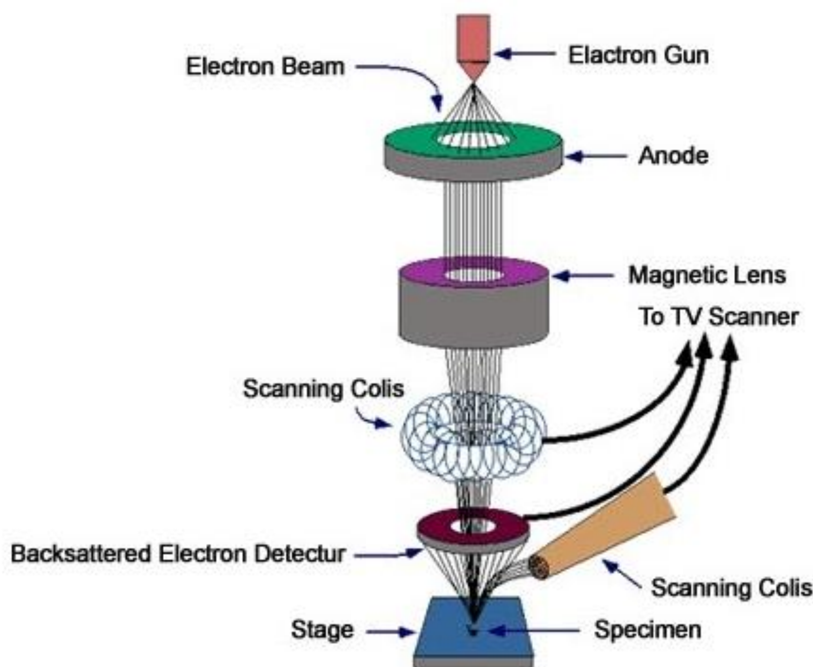


Fig. 2.11 Schematic illustration of measurement principle of SEM, source: Frontier LAB Inc.

FIB uses a finely focused beam of gallium ions that can be operated at low beam currents for imaging or high beam currents for site specific sputtering or milling. Besides, due to some unique

material systems that process high hardness, FIB can be used as an alternate to mechanical polishing techniques. The gallium (Ga+) primary ion beam hits the sample surface and sputters a small volume of material, which leaves the surface as either secondary ions or neutral atoms. The primary beam can produce secondary electrons as well. With the primary beam rasters back and forth on the sample surface, the image is created by the signal gathered from the sputtered ions or secondary electrons. Furthermore, with high ion beam currents, a great amount of material can be removed by sputtering, allowing accurate milling of the specimen down to a submicron scale. In addition to primary ion beam sputtering, the sample can be flooded with an incoming gases species. These gases can interact with the primary gallium beam to provide selective gas assisted chemical etching, or selective deposition of conductive or insulating material, enabled by the primary ion beam decomposing the deposition gas [8].

Fig. 2.12 Tescan GAIA3 SEM-FIB instrument.

2.3.2 SEM/FIB Observation of Packaged with Different Bond-line Thickness

In this study, all the SEM-FIB studies are carried out using a Tescan GAIA3 SEM-FIB instrument. Focus Ion Beam resolution of 2.5 nm with gallium at 1pA, can be attained using this instrument. In the context of this dissertation, FIB is used as milling and cutting trenches to create a clean cross-section for the BLT observation and its dimension measurement.

The specimen prepared for SEM generally requires mounting so that it is supported in a stable medium for grinding and polishing. In our study, a cold mounting system was chosen by using the epoxy system. This is because epoxies have the lowest shrinkage of all cold mounting resins. Shrinkage is the term given when the resin shrinks away from the sample surface during curing. This is undesirable as the gap forms harbors contaminates, grit from grinding and polishing stages to cause cross contamination of polishing surfaces. Further, unsupported edges are more prone to damage during preparation and rounding during polishing stages. It is difficult to obtain a well-polished, starch free surface when gaps in the mounting material are present. Besides, the epoxy resin also has the best characteristics with respect to higher hardness and low viscosity, less heat generation during curing. The curing time of epoxy system is relatively long to ensure that the material is fully cured before proceeding, but the adhesion to most materials is excellent.

The cold mounting of cross-section sample is prepared as followings: 1) Clean a mounting cup with alcohol and coat a thinner layer of Vaseline inside. 2) Mix the epoxy resin (Buehler EpoxiCure 2 Resin) and hardener (Buehler SampleKwick Liquid Fast Cure Acrylic) with a ratio of 5:1 to provide the mounting compound. 3) Place the encapsulated flip-chip type LED into the mounting cup and next pour in the epoxy compound. 4) Fully cured the sample at room temperature within the next 12 hours. 5) Take the cured sample out of the mounting cup for the grinding and polishing process. 6) Sample grinding and polishing was carried out under the mechanical grinder (Model 900, South Bay

Tech.) with both coarse grinding and fine grinding. The course grinding was carried out by using sandpaper of #320, 400, 600 grit size at a speed of 120 r/min and then followed by fine grinding with sandpaper of #800, 1200, 2000 grit size at a speed of 150 r/min to a proper size for SEM/FIB observation. 7) Due to the non-conductive nature of epoxy resin, the surface of the sample acts as an electron trap and resulted in electrons accumulation and influence the image information. Thus, a sputter coating is needed to act as a channel that allows the charging electrons to be removed from the material. Therefore, the well-polished was put into high-vacuum chamber for sputter deposition (EMS 150T Sputter Coater, Quorum Technologies Inc.) to apply a very thin functional coating on the sample surface for electrical conductivity. The sputter coating material used in this study is platinum.

The sample is placed on the stage and then tilted to 55 degrees. A voltage of 30kV and current of 9.5 nA ion beam was used to cut a trench within the sample. Several different places along the cross-section of each sample have been measured and the mean value of the measurements is taken to estimate the final BLT (marked with yellow dashed lines), as shown in Fig.2.13. Additionally, most of the heights of ridges and valleys on metal pads of die and substrate are between 0~20 nm according to AFM measurements (see Fig.2.7 & Fig.2.8). Therefore, the boundary of the BLT looks quite flat in SEM images which is consistent with the AFM topography features.

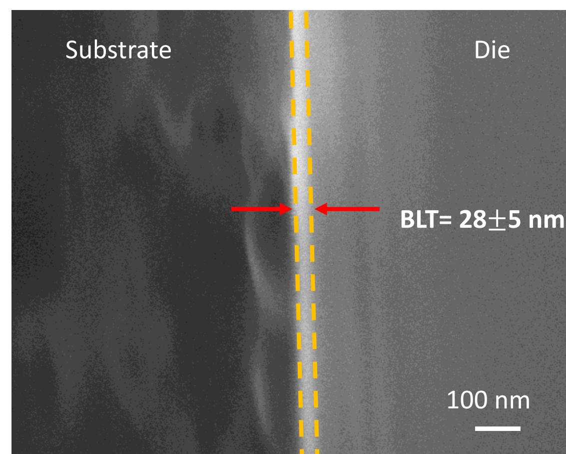


Figure 2.13 SEM imaging of bond-line thickness (BLT) for packaged devices enabled by NL.

2.4 Electrical and Thermal Conduction Mechanism of NL Bonding Method

For the “nano-locking” structure of present bonding method, the electrical and thermal conduction are established between the ridges and valleys of the intrinsic nanoscopic structures on surface roughness when the interconnecting surfaces are brought to be in contact under the controlled bonding pressure. The electrical and thermal conduction paths for the electric current and heat flux are as shown in Fig.2.14.

A contact interface is defined as the boundary between two solid bodies brought into contact under load [9]. And the contact interfaces between dielectric silicone adhesive and interconnecting surfaces (metallic pads on semiconductor die and metallic pads on package substrate) are perfect without introducing defects during curing process as shown in Fig. 2.13. Normally smooth surfaces usually comprise numerous asperities of various sizes on top of each other. At each contact point, there exists a contact resistance between the intrinsic nanoscale structures of two interconnecting surfaces, the equivalent electrical/thermal resistance circuit is shown in Fig. 2.14. The overall electrical resistance (R_e) equals as below:

$$\frac{1}{R_e} = \frac{1}{R_{c1}} + \frac{1}{R_{c2}} + \cdots + \frac{1}{R_{ci}} \quad \text{(Eq. 2.1)}$$

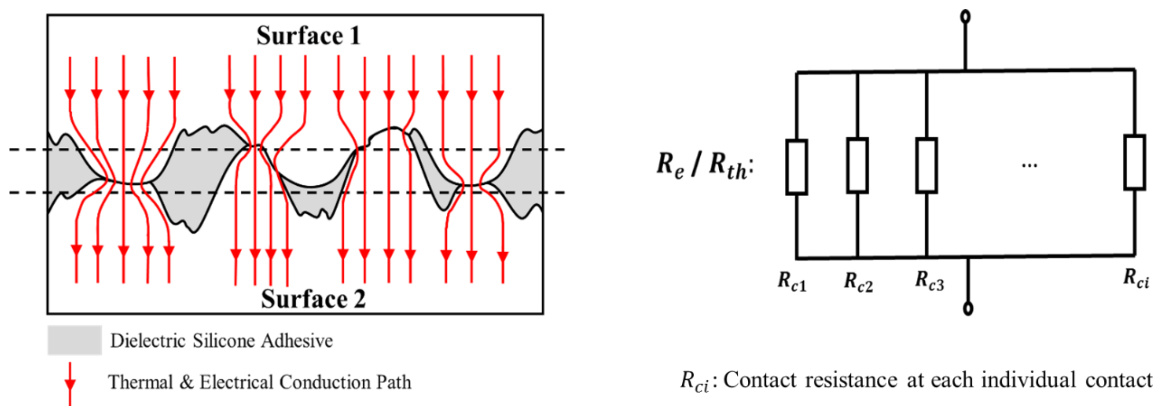


Figure 2.14 Schematic illustration of electrical and thermal conduction mechanism of NL bonding method and its equivalent circuits between the two interconnecting surfaces.

As discussed above, the essence of electrical and thermal conduction of NL bonding approach is established by forming the “nano-locking” structure between contacts of ridges and valleys on the intrinsic roughness. The electrical and thermal resistances are determined by contact area/size per contact and total number of contacts which is controlled by the bonding pressure. The silicone adhesive filling into the nanoscale valleys only helps stabilize the mechanical interconnection between two surfaces. And even if there are defects inside the silicone adhesive, it will not affect the electrical/thermal conduction, and neither will the electrical/thermal resistance.

2.5 Adhesion Strength of NL Bonding with Ultra-thin BLT

The adhesive strength is the interfacial strength between adhesive and substrate, it is the most important criteria when designing the adhesive bonded assembly. The adhesive bonding strength is usually measured by the simple single lap shear test as shown in Fig. 2.15. The shear strength (τ) is reported as the failure stress in the adhesive, which is defined and calculated by dividing the failing load by the bond area, $\tau = F/s$. Since the stress distribution in the adhesive is not uniform over the bonding area, the calculated shear stress is lower than the actual strength of the adhesive. The whole package is fixed on a tester, and a horizontal force which parallels to the package substrate is applied to push the die until the die is removed off the substrate.

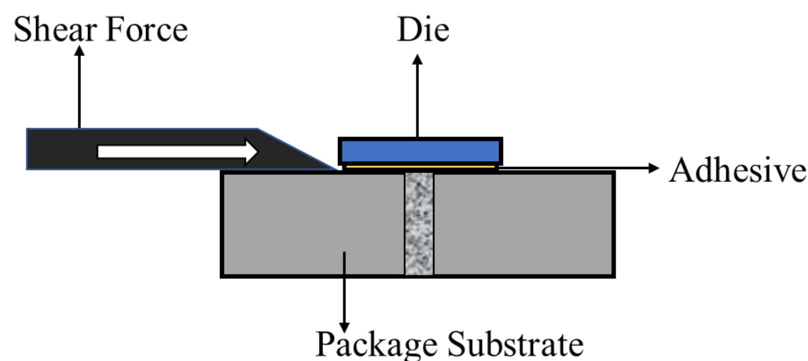


Figure 2.15 Schematic drawing of experimental set-up for die shear strength measurement.

The adhesion strength of the packaged die with different BLTs are measured and the experimental results are shown in Fig. 2.16. In Fig.2.16, the adhesion strength has a relationship with the bond-line thickness, and it decreases with the increasing bond-line thickness: the thicker BLT is shown to have a weaker adhesion strength when the BLT is under 100 nm.

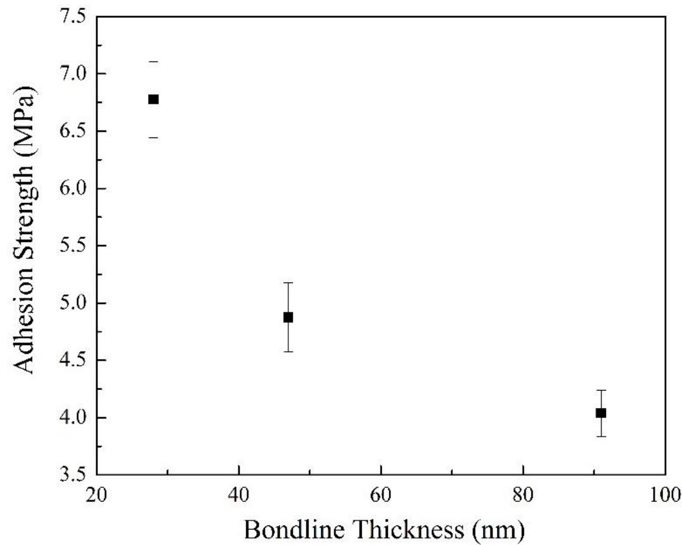


Figure 2.16 Adhesion strength of the NL bonding method as a function of bond-line thickness.

2.6 Summary

For the current advanced 2.5D/3D packaging technology, the mainstream off-chip electrical interconnection is achieved via the bump and bumpless methods. However, the main challenge is to further shrink the pitch size due to the physical limitations. Since the overall purpose for the advanced integration scheme is to reduce the device power consumption and increase the signal travel speed with a lower cost. Therefore, besides the pitch size, the vertical dimension or thickness of the interconnection is also very crucial and plays an important role in both thermal management and electrical signal travel.

In this Chapter, a novel die bonding method is proposed without using any metallic fillers achieve the electrical interconnection for die-substrate bonding. This method can be successfully applied to the die-substrate bonding for flip-chip type high power GaN-based LED.

A chip bonding method with a concept of "nano-locking" structure is illustrated for die attach between the die and package substrate. The electrical and thermal conduction mechanism has been discussed which is built through the contacts between the ridge and valleys on the surface roughness of the two bonding surfaces. The electrical/thermal resistance is influenced by the total number of contacts and contact area at each contact. This NL bonding method takes the advantage of the intrinsic nanoscopic structure and is mechanically stabilized by filling the nanoscale valleys with pure dielectric adhesive.

Without using the metallic fillers, the unique contributions of this method are as followings: 1) the bond-line thickness is scalable and can be controlled by the bonding pressure during the die bonding process. 2) the resulting bond-line thickness is in nanoscale ranges which is several hundred times of thinner in vertical dimension compared with the commercial ECA or eutectic solder pastes. 3) the cost can be greatly reduced, and the manufacturing process of the NL bonding can be simplified, no more surface modification will be needed.

Reference

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Chapter 3

Devices Enabled by NL Bonding Method

3.1 Introduction

The novel die-substrate bonding method is proposed, and all the details have been demonstrated in Chapter2. In this chapter, the NL bonding method is successfully applied to the die-attach process of a flip-chip type GaN based high power LED die. To make further study on the properties of the present NL bonding method, the electrical performance, thermal performance and optical performance of the packaged devices enabled by the NL bonding method are all evaluated and been analyzed with the conventional Ag-epoxy and AuSn solder pastes as bonding materials.

The electrical performance of the devices enabled by the NL bonding method with different bond-line thickness are prepared and evaluated by measuring the I-V curve and thus the electrical resistance of the overall bonding layer can be extracted and make comparison with conventional Ag-epoxy pastes and AuSn pastes. The thermal performance of the devices enabled by the NL bonding method with different bond-line thickness are prepared and are evaluated by measuring the junction temperature using the diode forward voltage method. Besides, the thermal resistance for the overall bonding layer is calculated based on the measured junction temperature. The optical performance of the devices enabled by the NL bonding method with different bond-line thickness are prepared and evaluated by measuring the lumen output using the integrated sphere system and make comparison with conventional Ag-epoxy pastes and AuSn pastes.

3.2 Electrical Performance of Packaged Devices

To study the electrical performance of the packaged devices enabled by the NL bonding method, the electrical resistance of the overall bonding layer is studied and analyzed. The electrical resistance is extracted by measuring the I-V characteristic curve of the packaged devices. The impact factors of electrical resistance will be discussed in the later chapters. To make further comparison, the electrical resistance of other two commercial bonding methods are also measured and studied.

3.2.1 I-V Characterization of Packaged Devices

To evaluate the electrical performance of the devices enabled by NL bonding method, the relationship between the current goes through the packaged devices and its corresponding terminal voltage is measured and recorded. Figure 3.1 (a) shows the experimental setup for the I-V curve measurement of packaged flip-chip LEDs. The I-V curve is powered and measured by KEITHLEY 2450 source meter (Tektronix Company) using 4-wire mode. The device under test (DUT) is connected to the KEITHLEY source meter through copper wires. A serious of voltages are applied to the packaged device, meanwhile, the corresponding current that goes through the device is also recorded. For the flip-chip type high power GaN based LED, since its specified maximum operating DC current is 700 mA as suggested by the vendor, thus the measurement stops when the electric current reaches 700 mA. And 15 samples are prepared and measured for each set of packaged devices with different die-substrate bonding methods.

The equivalent electrical circuit is shown in Fig. 3.1 (b). The effective interconnection electrical resistance $R_e = dV/dI = (V_m - V_F)/I_F$, where V_m is the measured terminal voltage applied on the packaged device, V_F is the forward voltage and I_F is the forward current.

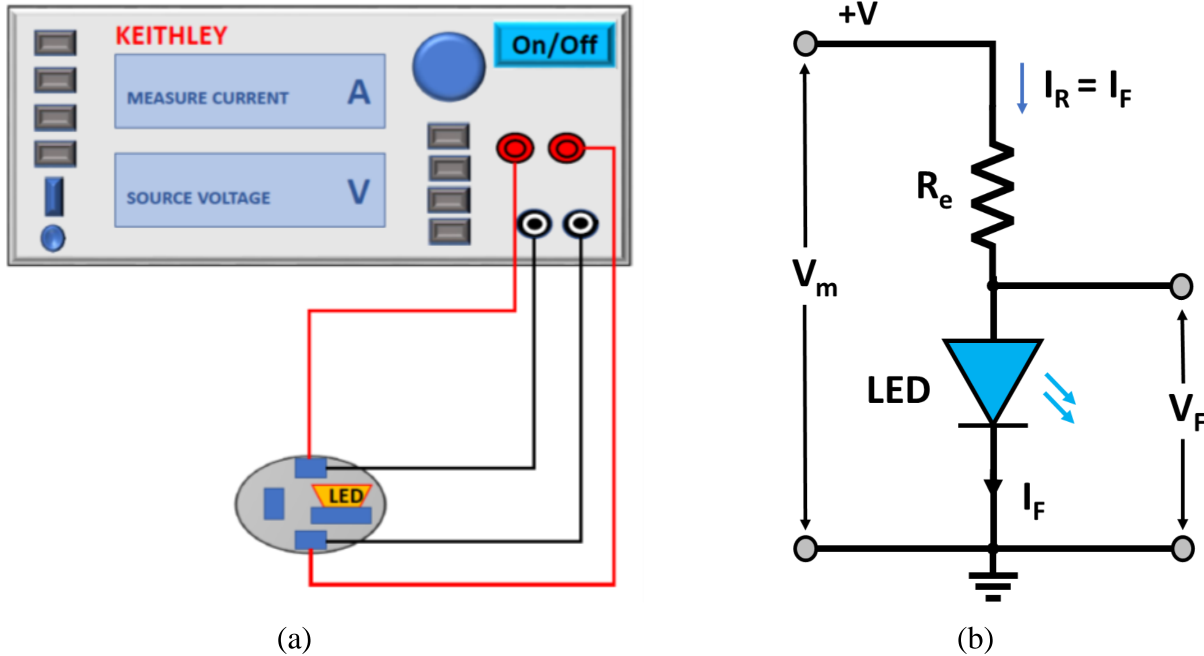


Figure 3.1 (a) Experimental setup for I-V characterization of packaged devices. (b) Equivalent electrical circuit for I-V measurement.

3.2.2 Electrical Resistance for NL Bonding Method

Figure 3.2 presents the electrical performance for devices made with the NL method, and its comparison to two conventional die-substrate bonding methods. The measured voltage for the devices made by the NL approach are all less than that for the devices using other two conventional methods, under the same forward current of 700 mA. Thus, a reduced interconnection electrical resistance is evident for the devices made by the present NL approach, which is supported by the result presented in Fig.3.3. The extracted R_e presents of different die-substrate bonding methods: the R_e for the devices made by the NL approach with a BLT of 85±5 nm is about 12% lower than the conventional AuSn bonding method and is about 35% lower than the conventional Ag-epoxy bonding.

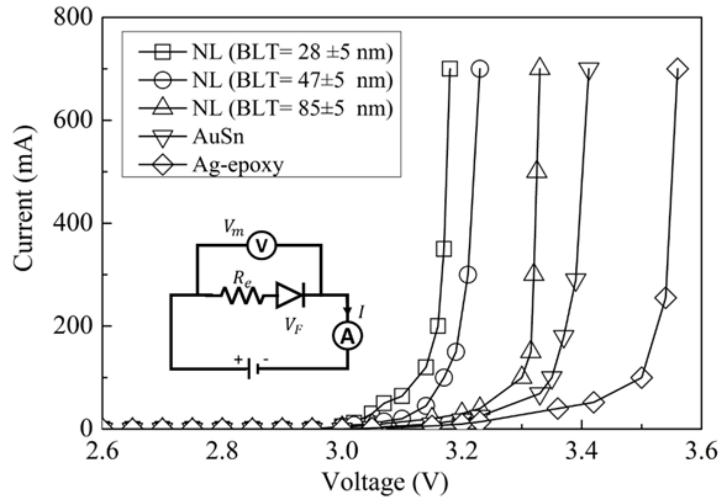


Figure 3.2 Measurement of current (I) and voltage (V) relationship for the devices made of the present NL and conventional die-substrate interconnection and bonding methods. The open square symbol (□) represents the NL bonding with BLT=28±5 nm, the open circle symbol (○) represents the NL bonding with BLT=47±5 nm, the open triangle symbol (△) represents the NL bonding with BLT=85±5 nm, the open triangle symbol (▽) represents the AuSn bonding; the open rhombus symbol (◇) represents the Ag-epoxy bonding. The solid curve represents the best I-V fitting.

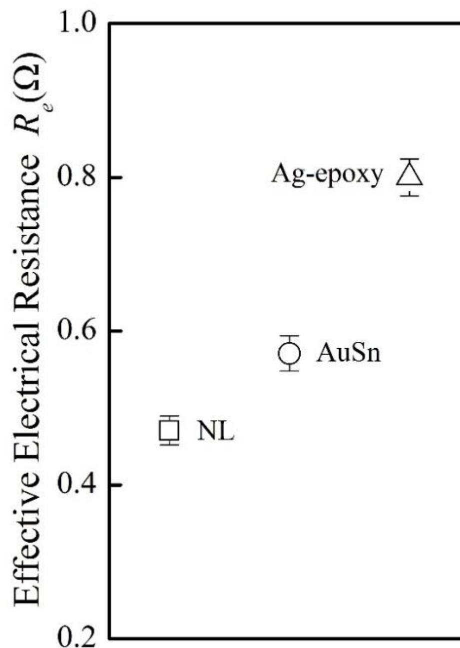


Figure 3.3 The R_e of different die-substrate bonding and connection methods: the open square symbol (□) represents NL bonding with BLT=85±5nm, the open circle symbol (○) represents

AuSn bonding with an industrial standard BLT value of 20± 2 μm, the open triangle symbol (△) represents Ag-epoxy bonding with an industrial standard BLT value of 25± 2 μm.

The reason of the reduced electrical resistance is not only attributed to its ultra-thin BLT, but also because of the different electrical conduction mechanism when compared with Ag-epoxy and AuSn bonding approaches.

For the Ag-epoxy based electrically conductive adhesive (ECA) bonding approach, its electrical conduction mechanism is mainly attributed to three contacts as shown in Fig. 3.4: upper interfacial contact resistance (R_{int1}) between die metallic pad and silver flakes in ECA, bottom interfacial contact resistance (R_{int2}) between substrate metallic pad and silver flakes in ECA, contact resistance (R_c) among ECA silver flakes in forming the conductive path between two metallic pads. Its effective electrical resistance (R_e) is determined by the conductivity of the silver flakes and the BLT. Larger BLT means a smaller number of contacts and conducting areas at the upper/bottom interfacial contacts, as well as among the conductive metallic fillers [1]. The upper/bottom interfacial contact resistances and the contact resistances among silver flakes are all proportional to the BLT and inversely proportional to the conducting area which increases with the increasing BLT [2]. The overall electrical resistance (R_e) equals as below:

$$R_e = R_{int1} + R_c + R_{int2} \text{ (Eq. 3.1)}$$

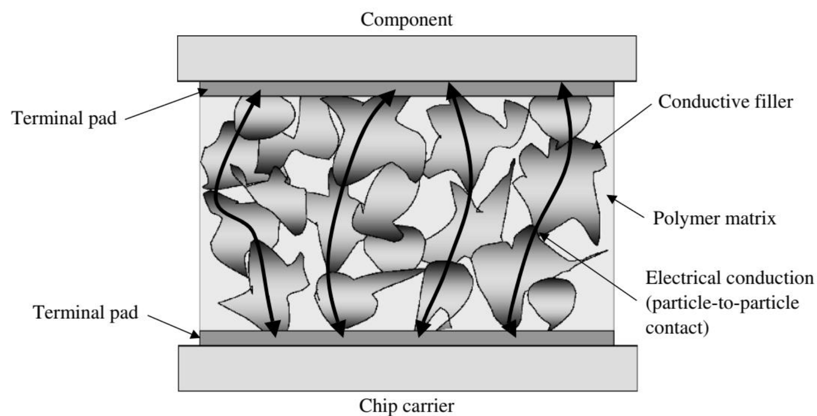


Figure 3.4 Schematic illustration of how electrical conduction paths are established by uninterrupted particle-to-particle contact between the component and the chip carrier terminal pads in an ICA joint [3].

For the eutectic AuSn bonding approach, its electrical conduction mechanism is also attributed to three factors: upper interfacial contact between die metallic pad and AuSn paste, bottom interfacial contact between substrate metallic pad and AuSn paste, conduction path formation after reflowing over eutectic points. Its effective electrical resistance is also determined by BLT, but the reason is different from the Ag-adhesive case: the small BLT only reduces the bulk resistance ($R_{bulk} = BLT/kA$, $k =$conductivity, $A =$ contacting area), but don't alter the upper/bottom interfacial contact resistances.

In addition to the nanometer scale BLT achieved for the first time with the present NL method, another significant advantage is the present interconnection is not critically affected by any possible interfacial defects resulting from voids and delamination formed during die bonding process associated with the two conventional methods. Such a defect resulting in a poor interfacial contact. And this type of interfacial poor contact increases the interfacial electrical and thermal resistance and degrades fatally the corresponding electrical and thermal performance and reliability [4].

3.3 Thermal Performance of Packaged Devices

Thermal management is very critical especially for high-power electronics and more than 60% of the electrical power input is converted into heat and build up at the junctions of LEDs due to nonradiative recombination of electron-hole pairs and low light extraction [5]. In high power LED, a part of the power converts into light flux and if the power conversion efficiency is low then the

loading of excess heat conduction is high. Heat flow path in high power electronics becomes more and more important with increasing input power.

The packaging materials including the die attach materials can decide heat flow rate from junction to board. The thermal conductivity of die attach materials thus can be reflected in the thermal resistance of heat flow path and the junction temperature for different die attach material shows an abrupt behavior with changes in their thermal conductivity [6]. Numerous studies have shown that junction temperature determines the lumen performance and the device lifetime [7-8]. The resulting challenge is the heat conduction after the die is packaged. An elevated junction temperature is related to the degradation of lumen performance and has an effect on the reliability of the packaged devices.

Based on our lab's previous study, the die-attach materials act as a bottle neck to control the heat flow path and thus affect the heat flow rate. For high power more than 1W LEDs, the die-attach materials become more and more important with increasing input power, shown in Fig.3.5. Besides, the power consumption of die attach material is relatively small compared to total input power. As a result, the development of new die attach material for high power electronics is a more important factor compared to its electrical conductivity.

Thermal performance of the packaged devices enabled by NL bonding method is evaluated by measuring its junction temperature and thermal resistance. The impact factors of thermal resistance will be discussed in the later chapters. To make further comparison, the junction temperature and thermal resistance of other two commercial bonding methods are also measured and studied.

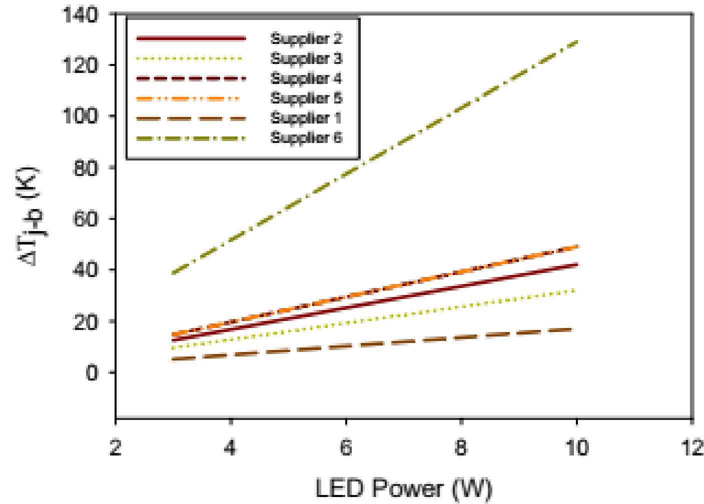


Figure 3.5 The estimated temperature differences from junction to board of more than 1 W LED. As increasing input power, the die-attach materials become more important [6].

3.3.1 Junction Temperature and Thermal Resistance Measurement

The junction temperature is measured by using the diode forward voltage method [9]. In the test technique, the device under test (DUT) is placed on the heat sink in a temperature oven and connected to the drive and measurement equipment (Everfine power generator) as shown in Fig.3.6. With most material, there is a linear correlation between the junction temperature (T_j) and the forward voltage drop (V_f):

$$T_j = m \cdot V_f + T_0 \qquad \text{(Eq. 3.2)}$$

m: slope in °C/Volt; T_0: intercept in °C

The diode forward voltage method consists of two series of measurements, a calibration measurement and real junction temperature measurement. The initial point is measured at 25°C, with the DUT then allowed to reach the thermal equilibrium. The dwell time is 10 min. After the junction has come to thermal equilibrium, a short duration current is sourced into the DUT and the voltage drop is measured. Then the temperature is elevated to a higher value of 50°C and 75°C respectively

to repeat the same measuring steps. And the slope and intercept can be calculated accordingly and get the equation. The calibration curve serves as the reference for the deduction of the junction temperature from DC measurement and establishes the relation between the forward voltage and junction temperature. Next the temperature of the oven was cooled down to room temperature, then the current pulse is again delivered to measure the forward voltage drop of DUT. After putting the value of the measured forward voltage drop back to the equation, the value of junction temperature can be got.

The thermal resistance R_{th} was extracted by following the equation:

$$R_{th} = (T_j - T)/\Delta W \qquad \text{(Eq. 3.3)}$$

T_j: junction temperature, T: ambient temperature, $\Delta W = IV$, V: forward voltage drop at thermal equilibrium, I: forward current that goes through the device.

Fifteen samples are prepared and measured for each set of packaged devices with different die-substrate bonding methods.

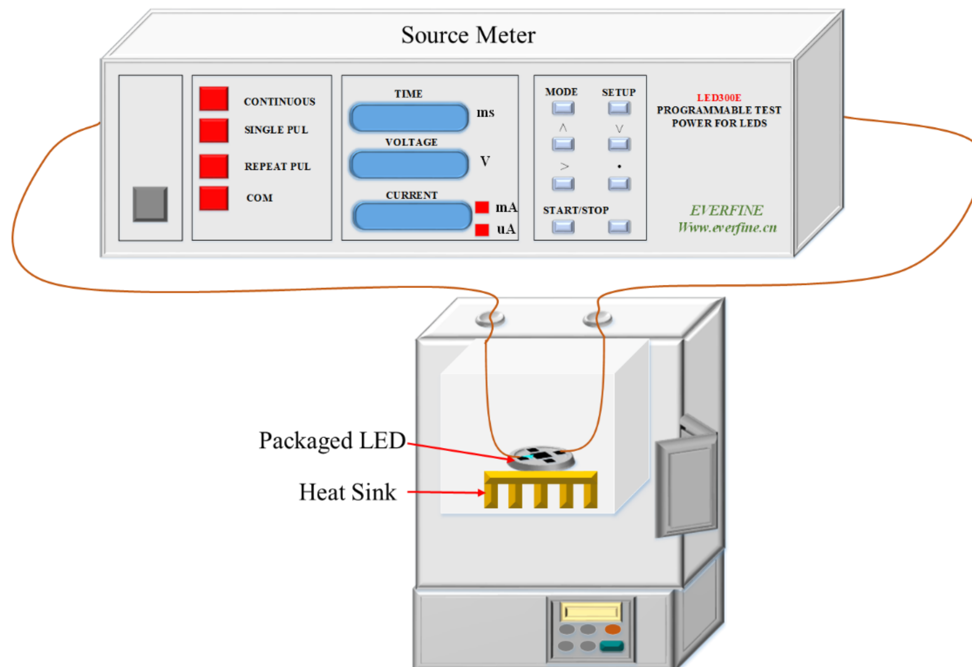


Figure 3.6 Experimental setup for junction temperature measurement of packaged devices.

3.3.2 Results and Discussion

The schematic diagram of the high-power GaN based flip-chip LED package is shown in Fig. 3.7. Fig. 3.8 presents the measured die junction temperature (T_j) for the devices made with the present NL bonding approach with different BLTs. The y-axis represents the measured junction temperature and the x-axis represents the operation time. The results from junction temperature measurement show that there is a rapid increase in between 60 and 360 seconds after the power is on for all samples and then systems reached steady state after 600 seconds when junction temperature remained constant. The junction temperature (T_j) of the packaged devices at steady state made by NL bonding with different BLTs range from 85℃ to 93℃. It is obviously to figure out that the junction temperature (T_j) decreases with the BLT. The die junction temperature (T_j) of the packaged devices enabled by NL with BLT= 28±5 nm is about 8℃ lower than the case of packaged devices with BLT= 85±5 nm. This will be discussed in our later chapters. And Fig. 3.9 presents the thermal performance for the devices made with the present NL approach (BLT=28±5 nm) and two conventional die-substrate bonding methods. It is evident from the device made by the NL method with a BLT=28±5 nm, a much lower T_j is resulted, which is about 10℃ lower than the AuSn bonding, and about 30℃ lower than Ag-epoxy bonding.

Based on the Eq. 3.3, once we measured the junction temperature T_j, and the heat generated from input (ΔW), the thermal resistance R_{th} can be calculated and shown in Fig.3.10. The thermal resistance of the packaged devices enabled by NL with BLT= 28±5 nm is about 6.3% lower than the case of packaged devices with BLT= 85±5 nm. This significant difference in T_j is also reflected in the huge difference in the corresponding thermal resistance of the die-substrate bonding layer made

with different die bonding methods as shown by Fig3.11: the thermal resistance (R_{th}) for the NL bonding with a BLT=28±5 nm, is about 7% lower than the AuSn bonding, and about 26% lower than the Ag-epoxy bonding.

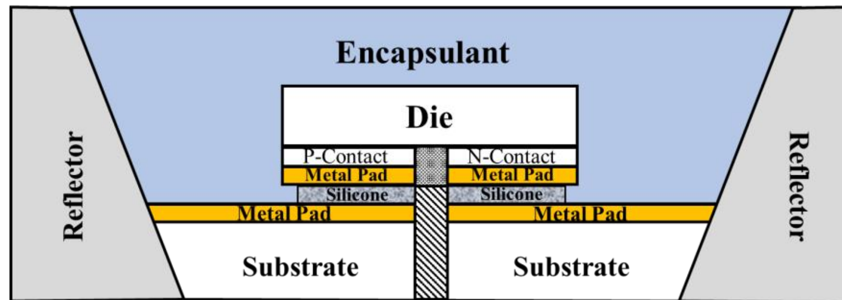


Figure 3.7 Flip-chip LED package structure.

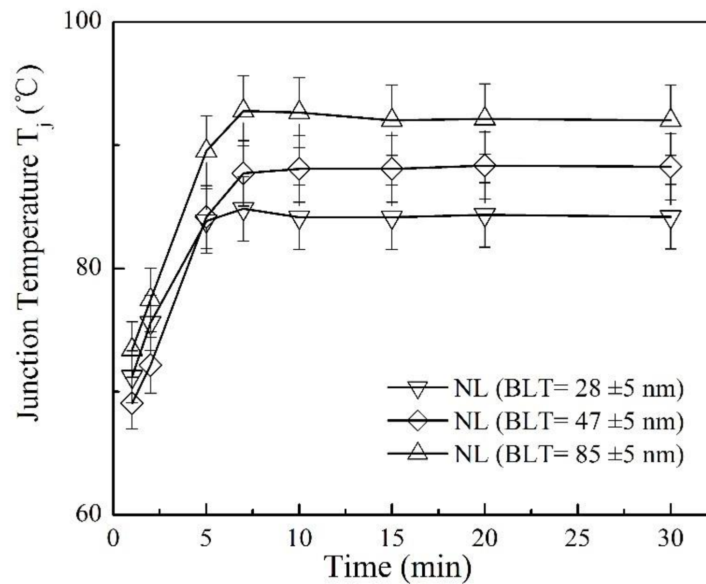


Figure 3.8 The die junction temperature (T_j) of the devices made by NL bonding approach with different BLTs.

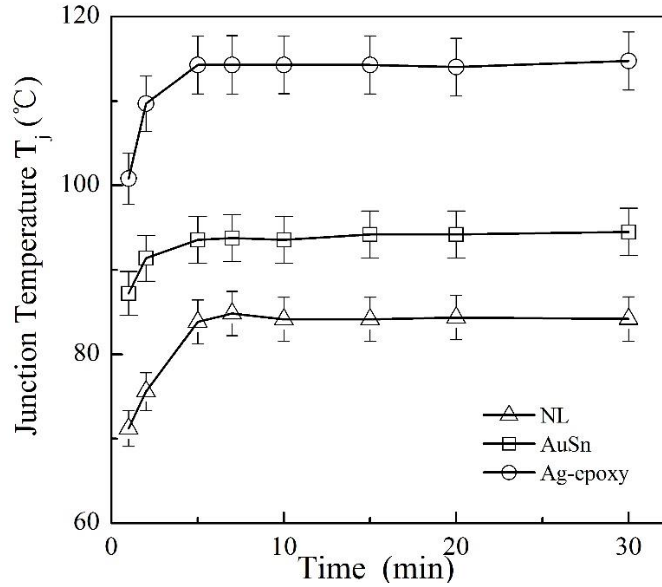


Figure 3.9 The die junction temperature (T_j) of the devices made by three different die-substrate bonding methods: the open triangle symbol (△) represents the experimental measurement of T_j for the device made with the NL approach with a BLT of 28±5 nm. The open square symbol (□) represents T_j data for the device made by the AuSn bonding with an industrial standard BLT value of 20± 2 μm, the open circle symbol (○) represents T_j data for the device made with Ag-epoxy bonding with an industrial standard BLT value of 25± 2 μm. The solid lines represent the best fitting.

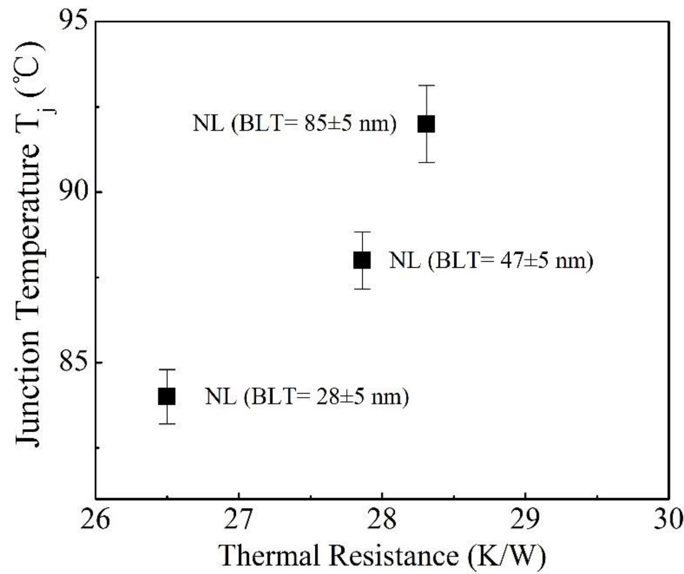


Figure 3.10 The thermal resistance of (R_{th}) of the devices made by NL bonding approach with different BLTs.

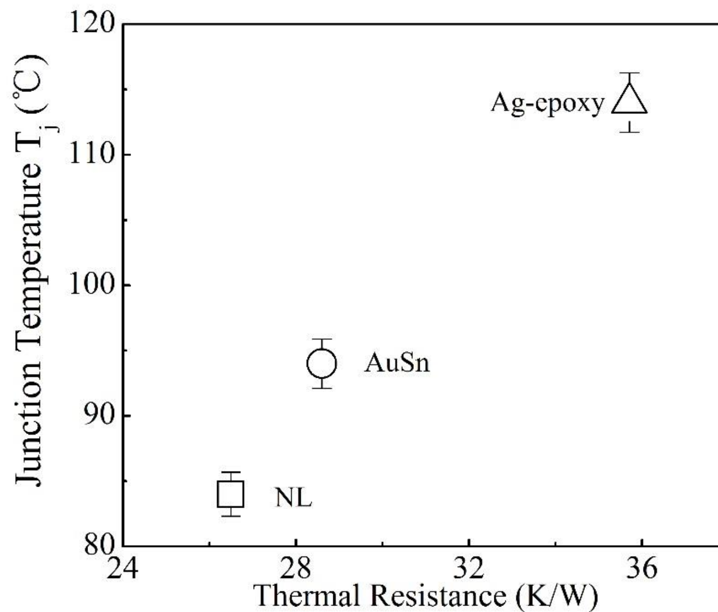


Figure 3.11 The relationship between T_j and R_{th} : the open square symbol (□) represents NL bonding with BLT=28±5 nm, the open circle symbol (○) represents AuSn bonding with an industrial standard BLT value of 20± 2 μm, the open triangle symbol (△) represents Ag-epoxy bonding with an industrial standard BLT value of 25± 2 μm.

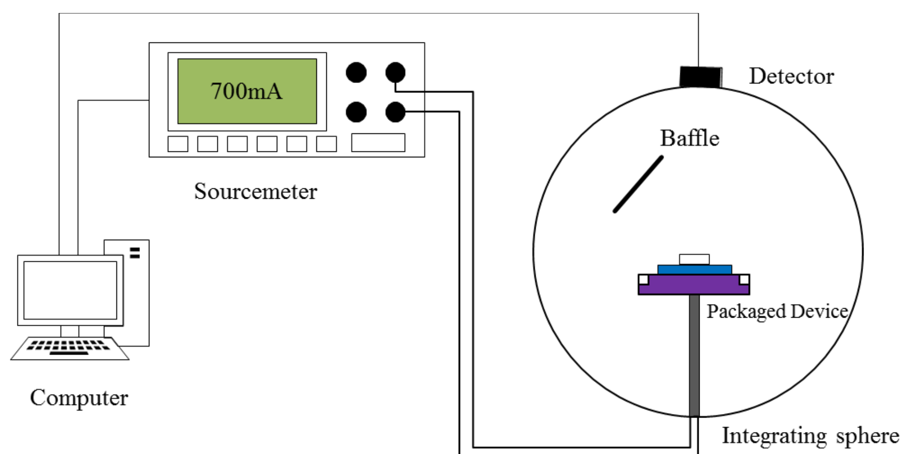
3.4 Optical Performance of Packaged Devices

The high-power LED as a solid-state lighting source is a promising candidate for the next generation illumination applications [10]. LED offers light output performance superior to that of other technologies with predictable, superior, and stable long-term performance. Thermal management has developed major issues affecting the performance of LED industries. The optical performance of the LED package based on fixed DC input current is tested by using the integrating sphere system.

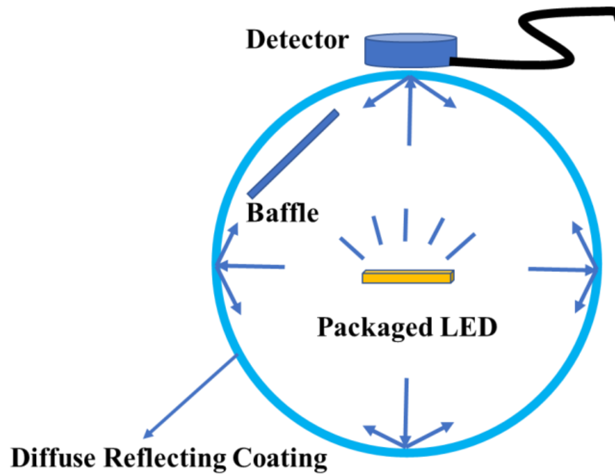
3.4.1 Lumen Output Measurement by Integrated Sphere System

The lumen output performance measurement of the packaged devices is carried out by using the integral sphere measure system (LabSphere) with the suggested maximum input constant current of

700 mA. The integrated sphere system is consisted of a power generator, an integrating sphere and a computer as shown in Fig. 3.12(a). The current source with corresponding forward voltage is supplied by Everfine power generator. An integrating sphere collects electromagnetic radiation from a source completely external to the optical device, usually for flux measurement or optical attenuation. The integrating sphere photometry is shown in Fig. 3.12 (b). The integration sphere for lumen output measurement is a hollow intact sphere shell with white diffuse reflecting coating. Radiation introduced into an integrating sphere strikes the reflective walls and undergoes multiple diffuse reflections. Light incident on a diffuse surface creates a virtual light source by reflection. The light emanating from the surface is best described by its radiance, the flux density per unit solid angle. Radiance is an important engineering quantity since it is used to predict the amount of flux that can be collected by an optical system that might view the illuminated surface. After numerous reflections, the radiation is dispersed highly uniformly at the sphere walls. Baffles help preventing that the direct incident light enters the field-of-view of the photodetector. The resulting integrated radiation level is directly proportional to the initial radiation level and may be measured easily using a detector.



(a)



(b)

Figure 3.12 (a) Spectral light measurement system for LED lumen output. (b) Integrating sphere photometry.

Deriving the radiance of an internally illuminated integrating sphere begins with an expression of the radiance, L, of a diffuse surface for an input flux, Φ_i.

$$L = \frac{\Phi_i \rho}{\pi A} \quad \text{(Eq. 3.4)}$$

where ρ is the reflectance, A the illuminated area and π the total projected solid angle from the surface.

For an integrating sphere, the radiance equation must consider both multiple surface reflections and losses through the port openings needed to admit the input flux, Φ_i, as well as view the resulting radiance. Consider A_s is the surface area of the entire sphere with input port area A_i and exit port A_e. The input flux is perfectly diffused by the initial reflection. The amount of flux incident on the entire sphere surface is:

$$= \Phi_i \rho \left(\frac{A_s - A_i - A_e}{A_s}\right) \quad \text{(Eq. 3.5)}$$

where the quantity in parenthesis denotes the fraction of flux received by the sphere surface that is not consumed by the port openings. It is more convenient to write this term as (1-f) where f is the

port fraction and $f = (A_i + A_e)/ A_s$. When more than two ports exist, f is calculated from the sum of all port areas.

By similar reasoning, the amount of flux incident on the sphere surface after the second reflection is:

$$= \Phi_i \rho^2 (1-f)^2 \qquad \text{(Eq. 3.6)}$$

The third reflection produces an amount of flux equal to:

$$= \Phi_i \rho^3 (1-f)^3 \qquad \text{(Eq. 3.7)}$$

It follows that after n reflections, the total flux incident over the entire integrating sphere surface is:

$$\Phi_i \rho (1-f)\{1 + \rho(1-f) + \cdots + \rho^{n-1}(1-f)^{n-1}\} \quad \text{(Eq. 3.8)}$$

Expanding to an infinite power series, and given that $r(1\text{-} f) < 1$, where r is the sphere surface reflectance and this reduces to a simpler form:

$$= \frac{\Phi_i \rho (1-f)}{1-\rho(1-f)} \qquad \text{(Eq. 3.9)}$$

Equation 3.9 indicates that the total flux incident on the sphere surface is higher than the input flux due to multiple reflections inside the cavity. It follows that the sphere surface radiance is given by:

$$L_s = \frac{\Phi_i}{\pi A_s (1-f)} * \frac{\rho(1-f)}{1-\rho(1-f)}$$

$$= \frac{\Phi_i}{\pi A_s} * \frac{\rho}{1-\rho(1-f)} \qquad \text{(Eq. 3.10)}$$

This equation is used to predict integrating sphere radiance for a given input flux as a function of sphere diameter, reflectance, and port fraction.

The design of an integrating sphere for any application involves a few basic parameters. This includes selecting the optimum sphere diameter based on the number and size of port openings and peripheral devices. Selecting the proper sphere coating considers spectral range as well as

performance requirements. The incident radiant flux is modified by the efficiency of the optics used. The centrally located baffle is recommended. Direct illumination through a side port would create areas of increased radiance. The field of view into the integrating sphere should be confined to the baffle.

The integral sphere measure system is calibrated before test and 15 samples are prepared and measured for each set of packaged devices with NL bonding method with various BLTs and different die-substrate bonding methods.

3.4.2 Results and Discussion

The sample we prepared for the optical performance evaluation are as followings: packaged flip-chip LED enabled by NL bonding method with different BLTs: 28$\pm$5, 47$\pm$5, 85$\pm$5 nm. Another group of samples prepared are using the same type of LED enabled by Ag-adhesive bonding (BLT= 25$\pm$2 μm and AuSn bonding (BLT=20$\pm$2 μm) approach.

In Figure 3.13, it is obviously to found that the lumen output of the packaged devices decreased with the increasing BLT and the normalized lumen output of the packaged devices with BLT= 28$\pm$5 nm is about 7% higher than the case of that with BLT= 85$\pm$5 nm. This will be fully discussed in our later chapters. Figure 3.14 presents the optical performance in terms of normalized lumen output at the suggested maximum input current of 700 mA for the devices made with the NL method, and the comparison to two conventional die-substrate bonding methods. It is evident that the devices made with the NL method (BLT=28±5 nm) results in a much higher lumen output (I_m): about 9.8% higher compared with the AuSn bonding, and about 17% higher compared with the Ag-epoxy bonding.

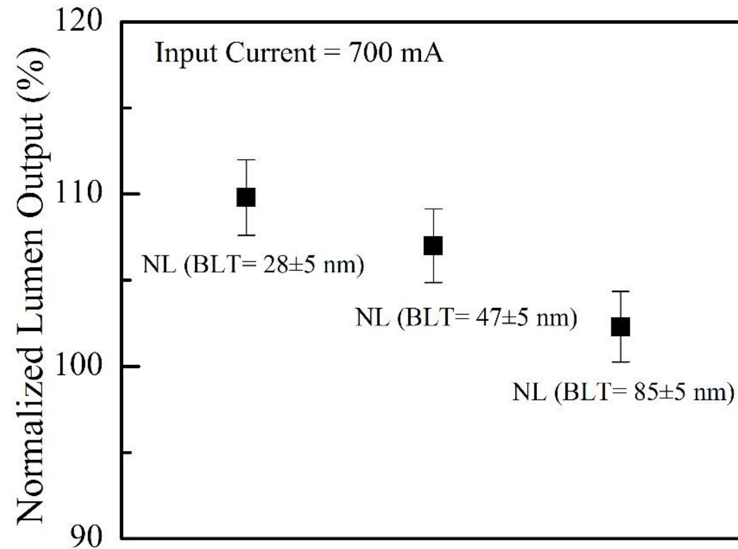


Figure 3.13 Normalized lumen output of the devices made by NL bonding approach with different BLTs.

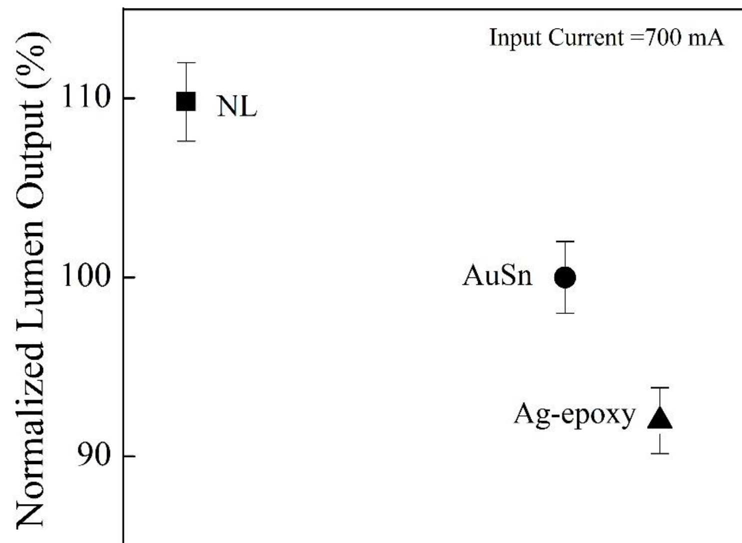


Figure 3.14 Normalized lumen output of the devices made by three different die-substrate bonding methods at an input current of 700 mA: the solid square symbol (■) represents the NL bonding approach with BLT=28±5 nm, the solid circle symbol (●) represents AuSn bonding with an industrial standard BLT value of 20±2 μm, the solid triangle symbol (▲) represents Ag-epoxy bonding with an industrial standard BLT value of 25±2 μm.

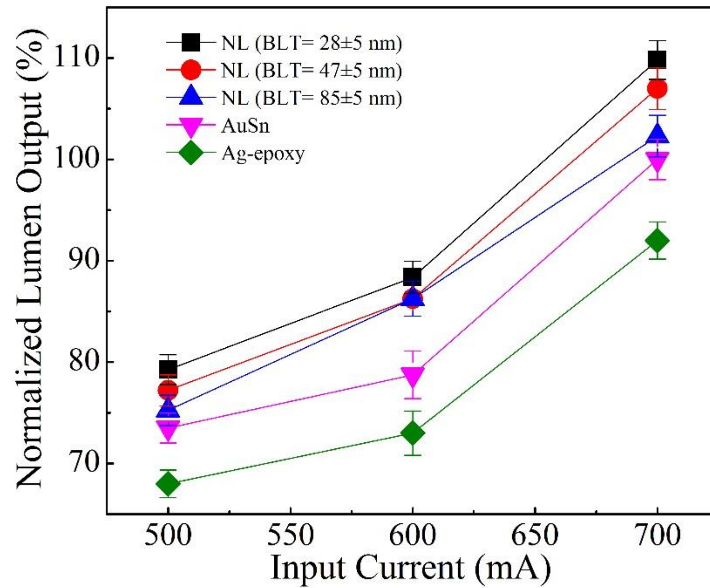


Figure 3.15 Changing trend of normalized lumen output of the packaged devices under different input current: the solid square symbol (■) represents the NL bonding approach with BLT=28±5 nm, the solid circle symbol (●) represents the NL bonding approach with BLT=47±5 nm, the solid upside triangle symbol (▲) represents the NL bonding approach with BLT=85±5 nm, the solid downside triangle symbol (▼) represents AuSn bonding with an industrial standard BLT value of 20±2 μm, the solid rhombus symbol (◆) represents Ag-epoxy bonding with an industrial standard BLT value of 25±2 μm.

Figure 3.15 describes the relationship between the lumen output of the packaged devices and the different input current. The x-axis represents the different input DC current and the y-axis represents the corresponding normalized lumen output under different input currents. It is evidently to figure out that the lumen output of the packaged devices is proportional to the input DC source current and it increases with the increasing input current. This is because the luminous flux of LEDs is largely governed by the current flowing through the device [11]. More input current means more input power will applied to the packaged LEDs, and the input power was found to be directly proportional to the square of light intensity for high power blue LEDs [12].

3.5 Summary

In this chapter, the electrical, thermal and optical performance of the packaged devices enabled by the NL bonding approach with different BLTs are evaluated and made comparison with the other two different commercial die-substrate bonding methods. Without adding any traditional metallic fillers to achieve the electrical and thermal conduction, the BLT can be largely compressed and controlled during the bonding process under different bonding pressure. Due to its electrical (and thermal) conduction mechanism mentioned in Chapter 2, the overall contact resistance between the two metallic bonding surfaces are affected by the different resulting BLTs.

Based on the experimental results shown above, it is evidently to figure out that when the vertical dimension of the off-chip interconnection is reduced to ultra-fine thickness (nanoscopic range), the electrical resistance and thermal resistance can be greatly reduced compared with the traditional electrically conductive adhesive and eutectic solder pastes.

The extracted electrical resistance for the devices made by the NL bonding approach with a BLT of 85±5 nm is about 12% lower than the conventional AuSn bonding method and is about 35% lower than the conventional Ag-epoxy bonding.

The junction temperature of the device made by the NL method with a BLT=28±5 nm is about 10℃ lower than the AuSn bonding, and about 30℃ lower than Ag-epoxy bonding. Based on the measured junction temperature and the heat generated from input power, the thermal resistance the thermal resistance of the NL bonding with a BLT=28±5 nm is about 7% lower than the AuSn bonding, and about 26% lower than the Ag-epoxy bonding.

The devices made with the NL method (BLT=28±5 nm) have a much higher lumen output which is about 9.8% higher compared with the AuSn bonding, and about 17% higher compared with the Ag-epoxy bonding.

The improved packaged device performance will also contribute to its reliability and reduce the happened of failure and improve the yield for the further application to high volume manufacturing. This is a huge breakthrough especially to the physical limitation of the shrink of Cu bump or the scale down of fine interconnect pitch.

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Chapter 4

Reliability Tests for Devices Enabled by NL Bonding Method

4.1 Introduction

Nowadays, the development process of highly integrated electronic systems, including ball grid arrays, flip-chip chip scale packages, as well as fanout packages has to take mission profiles into account which cover harsh environmental conditions [1]. An increasing demand to use such packages is seem at advanced Si-technology nodes for more complex applications in the field of data processing, internet of things sensor technology and automation. For electronic devices, systems and materials begin to wear out during use, and various mechanisms can contribute to the failure. The failures are defined within specific bounds under specific tolerance limits. Early failures may come from poor design, improper manufacturing, or inadequate use. It is also known that failures result from the aging process, material fatigue, excessive wear out, environmental corrosion, and undesirable environment can contribute to this process [2].

In this chapter, we will focus on the environmental reliability stress test for the packaged devices enabled by the present NL bonding approach. The samples are prepared as followings: devices enabled by NL bonding methods with different BLTs and other two different die-substrate bonding materials Ag-epoxy and AuSn. Wet high temperature operating life test and thermal cycling test are performed in order to evaluate the reliability of the new proposed NL bonding method and make comparison with commercially Ag-epoxy and AuSn bonding approaches.

4.2 Wet High Temperature Operation Life (WHTOL) Reliability Test

The wet high temperature operation life (WHTOL) reliability test is performed to evaluate the reliability of non-hermetic packaged IC devices in humid environments. Temperature, humidity, and bias conditions are applied to accelerate the penetration of moisture through the external protective material (encapsulate or seal) to along the interface between the external protective material and the metallic conductors which pass through it [3]. The high temperature and moisture is used to induce mechanical and electrical failure in the electronic device. This test requires a temperature-humidity test chamber capable of maintaining a specified temperature and relative humidity continuously, while providing electrical connections to the devices under test in a specific biasing configuration. In this study, the typical test condition we choose is known as 85/85, meaning the temperature is 85℃ and 85% of relative humidity, and the duration temperature is 1250 h.

4.2.1 Experimental Procedure

Figure 4.1 shows the experimental setup of the 85/85 reliability test measuring system which is consist of source meter and reliability chamber (GLMP50, Chemkorea Corp.). All the devices under stress are connected in series by copper wire and placed on a heat sink located inside the chamber. A maximum suggested input DC current of 700 mA is applied continuously on the devices provided by the source meter. All the samples are evaluated by measuring the lumen maintenance as a function of aging time every 250 hours after stressed in a high temperature of 85°C and a relative high humidity of 85% chamber. During the ramp-up process, the time to reach stable temperature and relative humidity conditions is less than 1 hour. And during the ramp-down process, the temperature of the test chamber is always ensured to exceed the wet-bulb temperature. The test clock starts when the temperature and relative humidity reach the setpoints and stops at the beginning of ramp-down. The

lumen output measurement of the stressed devices is performed less than 48 h after the end of ramp-down. For intermediate readouts, devices are returned to stress within 96 h of the end of ramp-down. The failure criteria is defined as lumen degradation or any open circuits (delamination, voids, crack) at the bonding interface. The wet high temperature operation life (WHTOL) reliability test goes beyond the requirement of the industrial standard JEDEC No.22-A101C by extending the test duration by 25% from 1000 hours to 1250 hours.

Care must be exercised in order to minimize release of contamination and degradation due to corrosion and other mechanism. Ionic contamination from the test apparatus (card cage, test boards, sockets, wiring, storage containers etc.) shall be controlled to avoid test artifacts. The humidity is produced by the deionized water in the water tank with a minimum resistivity of 1 megohm-cm at room temperature. 15 samples were prepared and measured for each set of packaged devices with different die-substrate bonding methods.

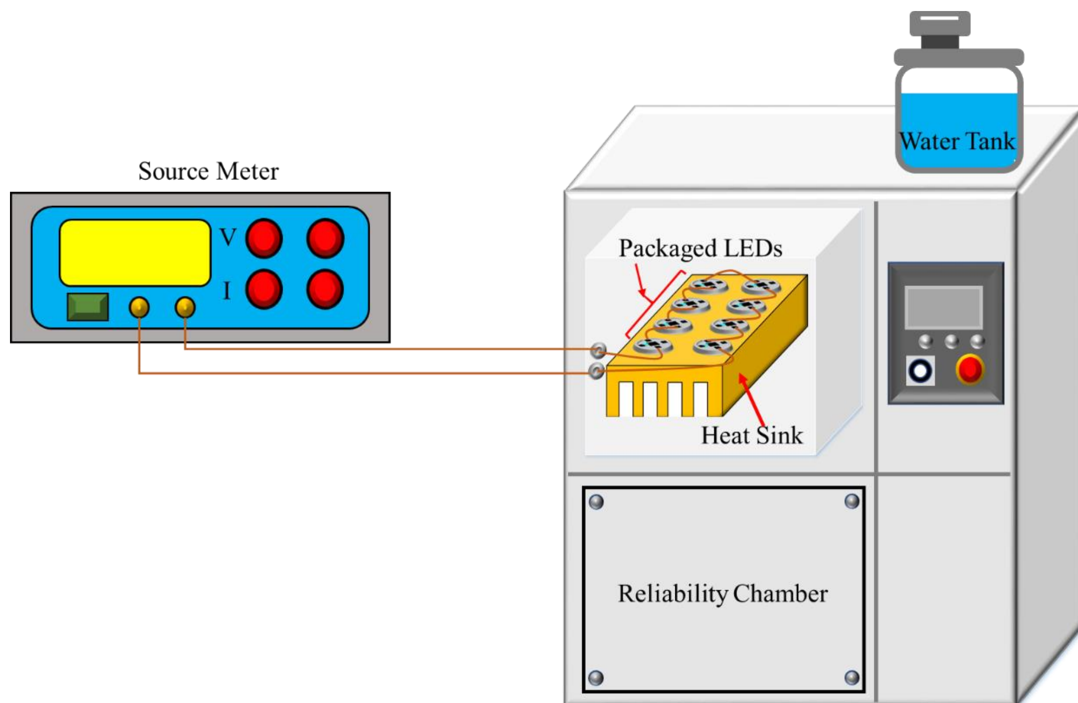

Figure 4.1 Experimental setup for the wet high temperature operation life (WHTOL) reliability test.

4.2.2 Results and Discussion

Figure 4.2 presents a comparison of the aging time-dependent lumen maintenance of the devices made by the NL approach with different BLTs under the industrial standard condition of high chamber temperature of 85℃ and high relative humidity of 85% for a total duration of 1250 hours. The y-axis represents relative change in the lumen maintenance normalized to the initial lumen output. The x-axis represents the aging time.

Based on the experimental result in Fig.4.2, the lumen output of the packaged devices degrades as aging time goes by: the lumen output drops quickly from the beginning to the aging time of 750 h, then the lumen degradation slows down and prone to stable after aging time of 1000 h. The lumen maintenance of the packaged devices enabled by NL bonding approach is decreased with the increasing BLT after aging. The relationship between the lumen degradation and BLT will be discussed in our later chapter.

Figure 4.3 presents a comparison of the aging time-dependent lumen maintenance of the devices made by the NL approach and two other conventional methods. It is evidently that at the aging time of 1250 h, the NL method in the case of BLT=28±5 nm results in a much higher lumen output, i.e., about 4% higher than device made by the AuSn bonding method, and about13% higher than the device made by the Ag-epoxy bonding method. This is because the NL bonding approach helps reduce the risk of interfacial delamination during bonding operation and chances of commonly observed failure caused by interfacial delamination and the mechanical breakdown can be significantly reduced without adding the conductive metallic fillers. Furthermore, the electrical contacts of the NL bonding approach are not fatally impacted by the potential interface delamination, voids, cracking etc. as in the cases of Ag-epoxy and AuSn bonding. The increase of the overall electrical resistance and thermal resistance also contributes to the lumen degradation. The lumen

output of the packaged devices enabled by NL bonding and AuSn bonding approaches degrade as aging time goes by: the lumen output drops quickly from the beginning to the aging time of 750 h, then the lumen degradation slows down and prone to stable after aging time of 1000 h. However, the lumen degradation of the Ag-epoxy drops dramatically from the beginning to the 250 h, and then becomes stable after aging time of 750 h.

When more moisture is absorbed during the aging process, the die-attach material and substrate swell to cause hygroscopic swelling stresses applied on the interface, these stresses are tensile state and results in delamination for ECAs and AuSn solder pastes. This, in turn, results in the degradation of the compressive force maintaining the contact between adhesive and semiconductor die. The hygroscopic swelling usually creates a large stress field, especially in the center of the package, thus the failure stars in the middle of the package and propagates outwards to the edge. In addition, metal electromigration and corrosion due to the chemical or electrolytic reactions in the presence of accelerated temperature, moisture, contaminants and bias also contribute to the lumen degradation.

Good thermal path from LED die to substrate is essential to ensure that heat can be effectively removed from LED semiconductor itself. As we have discussed above, the junction temperature of the packaged LED enabled by NL bonding method is largely reduced compared with other two commercial bonding methods which helps prevent junction temperature rise too high to affect the LED lifetime adversely. This also can be supported by the decreased thermal resistance of the overall NL bonding layer.

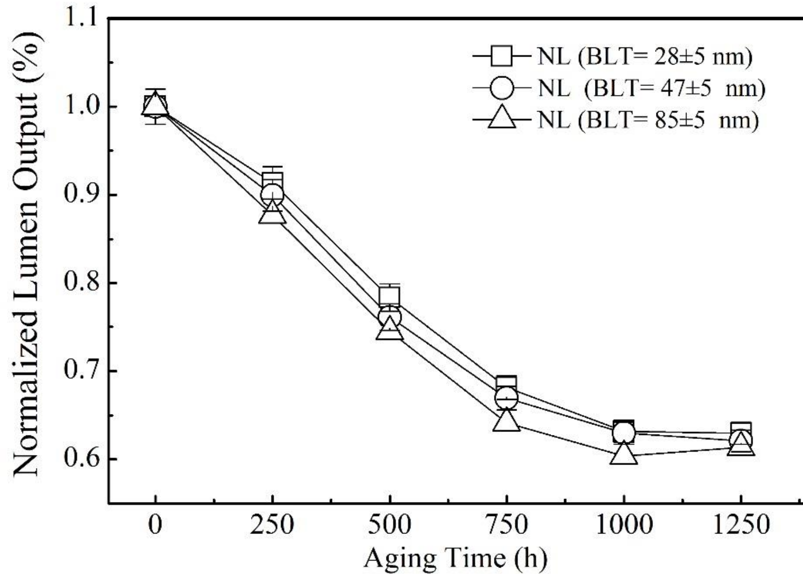

Figure 4.2 Long-term lumen maintenance of the devices enabled by NL bonding with different BLTs as a function of aging time under the stressing condition of an operating current of 700mA, a relative humidity RH=85%, and a high environmental temperature of 85℃: the open square symbol (□) represents the experimental data of NL bonding with BLT=28±5 nm, the open circle symbol (○) represents the experimental data of NL bonding with BLT=47±5 nm, the open triangle symbol (△) represents the experimental data of NL bonding with BLT=85±5 nm. This Wet High Temperature Operating Life (WHTOL) test goes beyond the requirement of the standard JEDEC No.22-A101C while extending the test duration by 25% from 1000 to 1250 hr.

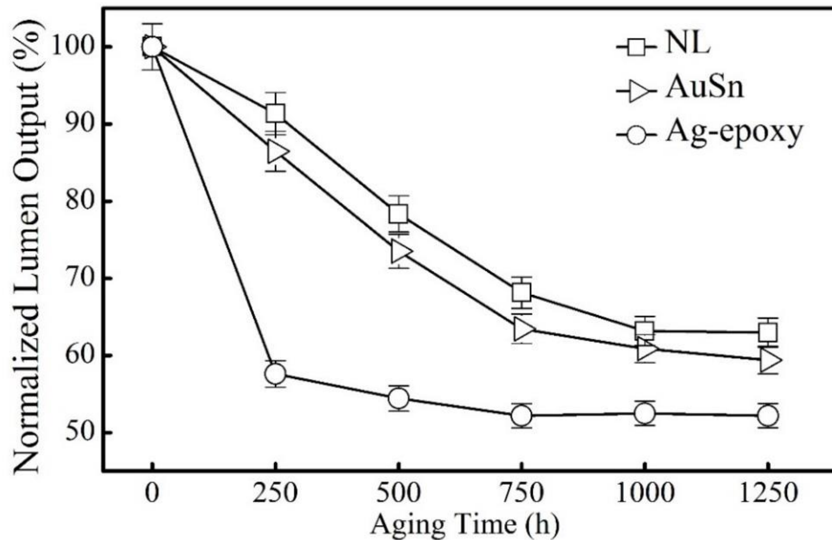

Figure 4.3 Long-term lumen maintenance of the devices with three different die-substrate bonding methods as a function of aging time under the stressing condition of an operating current of 700mA, a relative humidity RH=85%, and a high environmental temperature of 85℃: the open square symbol (□) represents the experimental data of NL bonding with

BLT=28±5 nm, the open triangle symbol (▷) represents the experimental data of AuSn bonding, the open circle symbol (○) represents the experimental data of Ag-epoxy bonding. This Wet High Temperature Operating Life (WHTOL) test goes beyond the requirement of the standard JEDEC No.22-A101C while extending the test duration by 25% from 1000 to 1250 hr.

4.3 Thermal Cycling Test

Stress management is critical for adhesive application and a serious concern is the long-term reliability of the joint under thermal stress caused by mismatch of coefficient thermal expansion (CTE) between the die, the package substrate being bonded and the adhesive. CTE is a material property that describes how the size of an object changes with a change in temperature [4]. Most solid materials expand upon heating and contract when being cooled. The change in length with temperature for a solid material is expressed as follows:

$$\frac{\Delta l}{l_0} = \alpha_l \Delta T \quad \text{(EQ. 4. 1)}$$

Where l_0 is initial length and Δl is length change, ΔT is temperature change, α_l is linear coefficient of the thermal expansion. Therefore, for a given temperature, the amount of expansion (or contraction) of a material is proportional to its CTE and to its initial length. At each joint, as the bonded materials expand and contract at a different rate, they push and pull on each other with different forces. Repeated movement due to temperature changes produce cyclic stress as shown in Fig.4.4. The generation of thermal stresses resulting from change of temperature gradients between the outside and interior These differential forces lead to stress build up and this stress is relieved through cracking, warping, fracturing, and other failures [5].

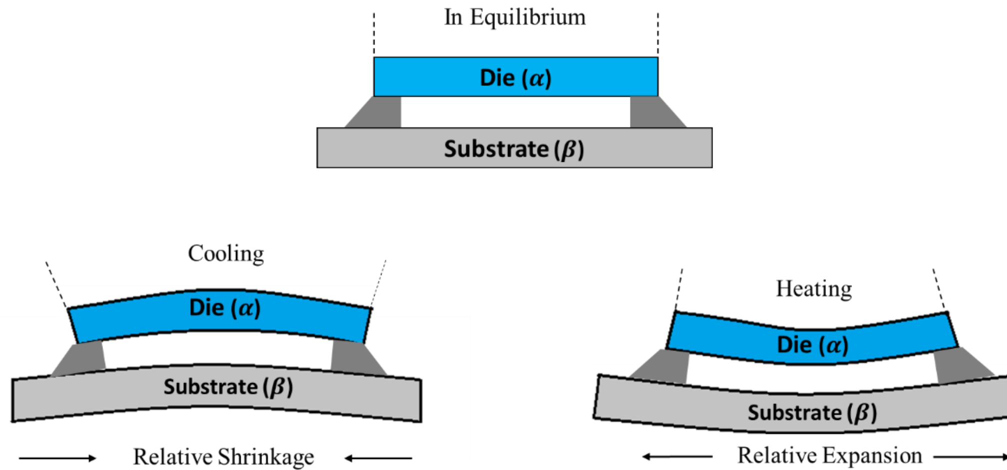

Figure 4.4 CTE mismatch producing cyclic stress.

The scope of thermal cycling test is to determine the ability of components and die-substate interconnection bonding by NL bonding approach to withstand mechanical stresses induced by alternating high- and low-temperature extremes [6]. Permanent changes in electrical and/or physical characteristics can results from mechanical stresses.

In this study, we focused on the reliability study using thermal cycling (TC) method. We fabricated samples of high power GaN based LED die bonded to package substrate using NL bonding method and two other commercial methods Ag-epoxy and AuSn bonding. 15 samples were prepared and measured for each set of packaged devices with different die-substrate bonding methods.

4.3.1 Experimental Procedure

The temperature cycling reliability test is conducted according to the industrial standard JEDEC (No.22-A104-B). All the samples are placed on the heat sink inside an experimental chamber which the temperature can be well controlled. The cycling is between -40℃ and 125℃ with a rate of 3℃ /min, and the dwell time is 5 min at -40℃ and 125℃, respectively. The number of samples used in

the test for each type of the packaged LEDs with different electrical interconnections is 15 and the total exposure period is 200 cycles. The criteria for the thermal cycling test are to see whether the packaged LEDs can be lit up after the thermal cycling test. The thermal cycling profile is shown in Fig. 4.4.

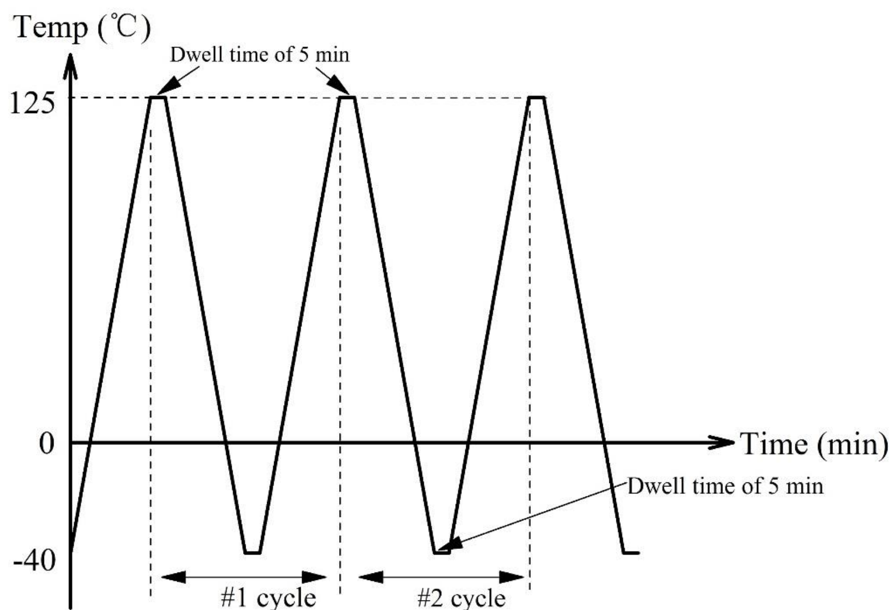

Figure4.5 Thermal Cycling (TC) profile between -40°C and 125°C.

4.3.2 Results and Discussion

The thermal cycling results of the packaged LEDs with different die-substrate bonding materials are shown in Table 4.1 below. For each group of samples, the packaged LEDs using NL bonding with a BLT= 85±5 nm show a 100% pass rate and all the samples pass the thermal cycling test. However, for packaged LEDs with AuSn bonding, 2 out of 15 samples are failed. And for packaged LEDs with Ag-epoxy boding, 2 out of 15 samples are failed. Both the pass rate of Ag-epoxy and AuSn bonding are about 86.7% after the thermal cycling test.

Table 4.1 Thermal cycling results of packaged LEDs with different die-substate bonding materials

NL Bonding	Criteria	AuSn Bonding	Criteria	Ag-epoxy Bonding	Criteria
#1	Pass	#1	Pass	#1	Pass
#2	Pass	#2	Fail	#2	Pass
#3	Pass	#3	Pass	#3	Pass
#4	Pass	#4	Pass	#4	Pass
#5	Pass	#5	Pass	#5	Fail
#6	Pass	#6	Pass	#6	Pass
#7	Pass	#7	Pass	#7	Pass
#8	Pass	#8	Pass	#8	Pass
#9	Pass	#9	Pass	#9	Pass
#10	Pass	#10	Pass	#10	Pass
#11	Pass	#11	Pass	#11	Pass
#12	Pass	#12	Pass	#12	Pass
#13	Pass	#13	Pass	#13	Fail
#14	Pass	#14	Fail	#14	Pass
#15	Pass	#15	Pass	#15	Pass

The thermal cycling experimental result demonstrates the truth that the adhesion strength of NL bonding with BLT<100±5 nm is better than the case of AuSn bonding and Ag-epoxy bonding methods. This is attribute to the perfect interfacial between pure adhesive and bonding surfaces without too much defects compared to AuSn and Ag-epoxy bonding methods as discussed above.

4.4 Summary

In this Chapter, the reliability of packaged devices enabled by the NL bonding method are evaluated and compared with the conventional Ag-epoxy and AuSn bonding methods. According to the experimental result of wet high temperature operating life test, the lumen maintenance of

packaged devices enabled by NL bonding method decreases with the increasing bond-line thickness. It is evidently that at the aging time of 1250 h, the NL method in the case of BLT=28±5 nm results in a much higher lumen output, i.e., about 4% higher than device made by the AuSn bonding method, and about13% higher than the device made by the Ag-epoxy bonding method. This is because the NL bonding approach helps reduce the risk of interfacial delamination during bonding operation and the chances of commonly observed failure caused by the mechanical breakdown can be significantly reduced without adding the conductive metallic fillers.

Furthermore, the electrical contacts of the NL bonding approach are not fatally impacted by the potential interface delamination, voids, cracking etc. as in the cases of Ag-epoxy and AuSn bonding. The increase of the overall electrical resistance and thermal resistance also contributes to the lumen degradation. The adhesion strength of NL bonding with BLT<100±5 nm is better than the case of AuSn bonding and Ag-epoxy bonding methods. This is attribute to the perfect interfacial between pure adhesive and bonding surfaces without too much defects compared to AuSn and Ag-epoxy bonding methods as discussed above.

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Chapter 5

Effect of Bond-line Thickness (BLT) on Device Performance by NL Bonding Method

5.1 Introduction

For the present NL bonding method, without adding any metallic fillers to provide the thermal and electrical conduction between the two bonding surfaces, the bond-line thickness (BLT) is scalable and can be controlled by the bonding pressure during the manufacturing process. The range of the BLT can be as thin as several tens of nanometers and about 200 times thinner than the traditional electrically conductive adhesives. This is one of the most important breakthroughs compared to the other bonding methods.

According to the result shown in Chapter 3, the BLT plays an important role in determining the electrical, thermal performance as well as the long-term reliability of the packaged devices enabled by the present NL bonding approach. In this Chapter, we will discuss the relationship between BLT vs. the electrical resistance, BLT vs. the thermal resistance, BLT vs. the junction temperature and BLT vs. lumen maintenance. The changing trend of the device performance and its reliability as the function of BLT will be studied.

5.2 Device Performance and Reliability Dependence on Bond-line Thickness

5.2.1 Electrical Performance Dependence on BLT

The experimental data of electrical resistance (R_e) for the devices made by the present NL approach with different BLTs has been shown in Chapter 3. As shown in Fig. 5.1, for the devices

made by the present NL approach, R_e decreases significantly with decreasing BLT, and such a BLT dependence of R_e follows a relationship of $R_e = 0.039(BLT)^{0.56}$.

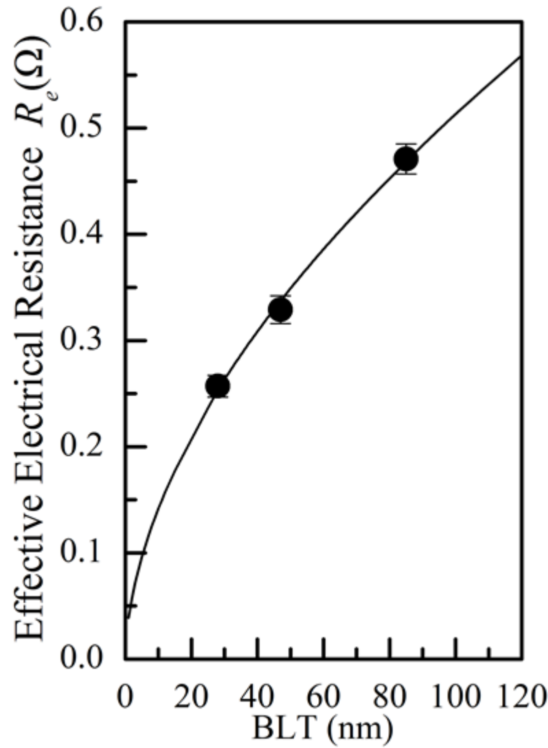

Figure 5.1 The solid circle symbol (●) correspond to the extracted values for R_e in the NL approach, which indicates R_e decreases with decreasing BLT which can be described by $R_e = 0.039(BLT)^{0.56}$ (the solid curve).

This is expected in view of the prior result on the relationship between the contact resistance and applied bonding pressure [1], and in the present case the BLT is inversely dependent on the applied pressure. In the present NL method, however, the only function of the adhesive used is for mechanically bonding and it does not impact on the electrical and thermal resistance of the formed interconnection, so long a reasonable bonding is achieved, even with some defects. The electrical performance in the present method is more strongly related to the individual contact area of nano-contacts on the interconnecting surfaces, and the total number of those contacts [2], which is thus

strongly dependent on the BLT: a reduced BLT results in a larger individual contact area, as well as an increased number of contacts [3]. This is illustrated in Fig. 5.2 below.

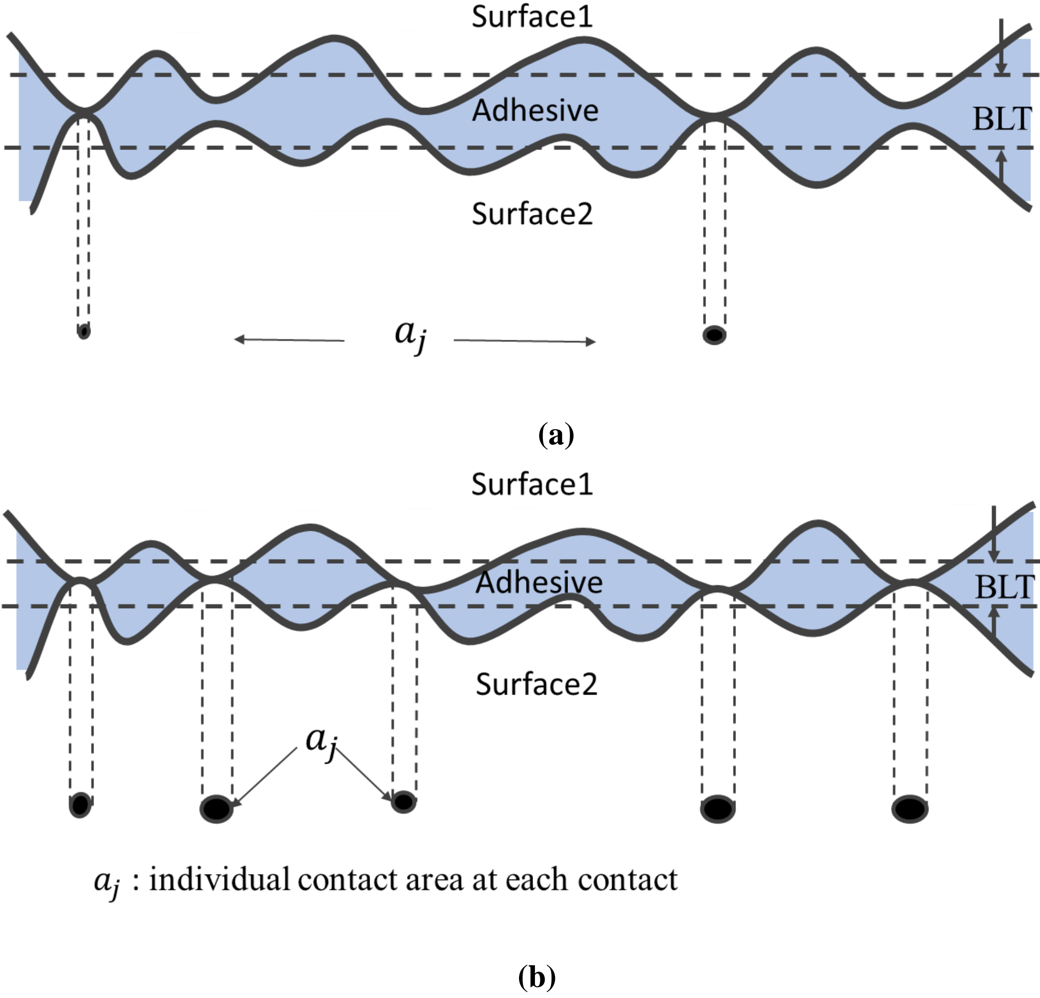

Figure 5.2 Illustration of contact resistance on the dependence of BLT: thinner BLT leads to larger number of total contacts and larger individual contact area at each contact.

5.2.2 Thermal Performance Dependence on BLT

The thermal performance of the packaged devices enabled by NL bonding with different BLTs is evaluated by measuring the its junction temperature (T_j) and thermal resistance (R_{th}). The experimental data of junction temperature (T_j) for the devices made by the present NL approach with

different BLTs has been shown in Chapter 3. Figure 5.1 shows the junction temperature (T_j) as a function of bond-line thickness. The junction temperature (T_j) has an increasing trend with the thicker BLT, and the BLT dependence of T_j follows $T_j = 64.06(BLT)^{0.082}$ as shown in Fig 5.3.

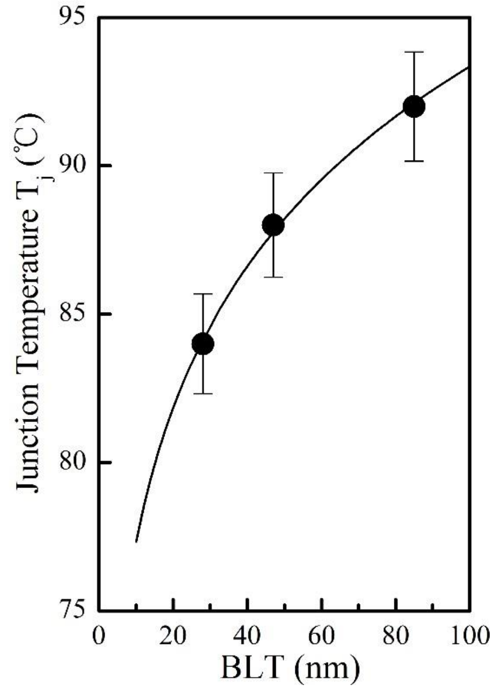

Figure 5.3 For the devices made by the NL bonding, T_j is found to decrease with the decreasing BLT, which can be described by $T_j = 64.06(BLT)^{0.082}$ (the solid curve), and the solid circle symbol (●) represents the experimental data for T_j.

The experimental data of thermal resistance (R_{th}) for the devices made by the present NL approach with different BLTs has also been shown in Chapter 3. Figure 5.3 shows the thermal resistance (R_{th}) as a function of bond-line thickness. As discussed above in Chapter 3, the thermal resistance R_{th} was extracted by following the equation: $R_{th} = (T_j - T)/\Delta W$, where T_j: junction temperature, T: ambient temperature, $\Delta W = IV$, V: forward voltage drop at thermal equilibrium, I: forward current that goes through the device. Besides, the thermal resistance of the present method is more strongly dependent on the individual contact area of nano-contacts on the interconnecting

surfaces, and the total number of those contacts. Thinner BLT leads to larger individual contact area and increase the number of total contacts. Therefore, R_{th} decreases with decreasing BLT, and the BLT dependence of R_{th} follows $R_{th} = 21.75(BLT)^{0.059}$ as shown in Fig. 5.4, which is fully understandable in view of the prior result on the dependence of thermal resistance on the thickness of bonding layer. Since the value of BLT depends on the bonding pressure, and thus the T_j and R_{th} are essentially a dependence on the bonding pressure.

As discussed above, the relatively significant large thermal resistance values associated with Ag-epoxy and AuSn bonding, might to do with unavoidable imperfect die-substrate interfacial bonding resulting from voids and other defects during bonding process.

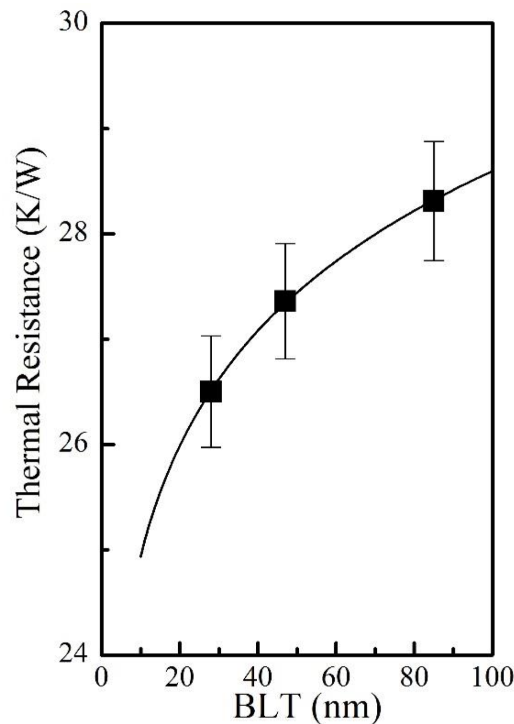

Figure 5.4 For the devices made by the NL bonding, R_{th} is found to decrease with the decreasing BLT, as described by $R_{th} = 21.75(BLT)^{0.059}$ (the solid curve). The solid square symbol (■) represents the extracted thermal resistance R_{th}.

5.2.3 Lumen Performance Dependence on BLT

The lumen performance of the packaged devices enabled by NL bonding with different BLTs is evaluated by measuring lumen output (I_m) as shown in Chapter3. The lumen degradation drops as the increasing of BLT. Figure 5.5 shows the normalized lumen output as a function of bond-line thickness. For present NL method, lumen output (I_m) decreases with increasing BLT and the BLT dependence of lumen output (I_m) follows $I_m = 1.36(BLT)^{-0.064}$ as shown in Fig. 5.5. This is fully consistent with the prior results on the dependence of T_j and R_{th} on the applied pressure since BLT is inversely proportional to the applied pressure. Therefore, the normalized lumen output dependence on BLT in Fig. 5.5 is essentially dependent on the bonding pressure.

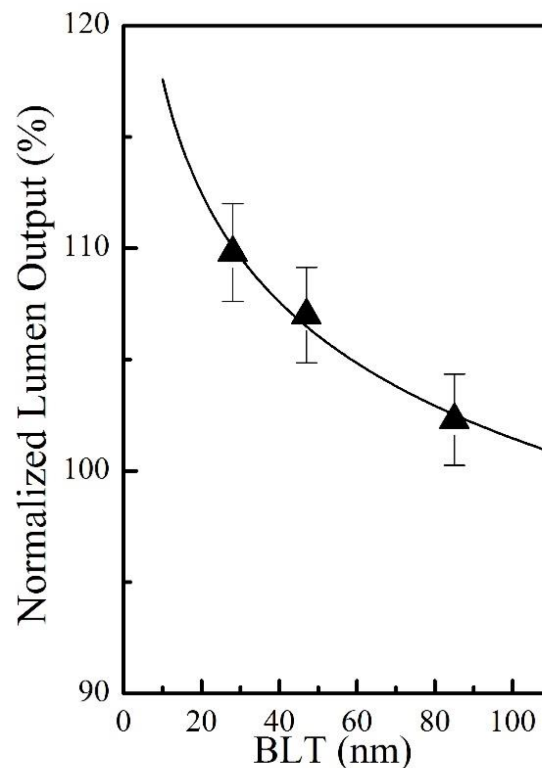

Figure 5.5 For the devices made by the NL bonding, the normalized lumen output (I_m) is found to be increased with the decreasing BLT, which can be described by $I_m = 1.36(BLT)^{-0.064}$ (the solid curve), and the solid triangle symbol (▲) represents the experimental data for normalized lumen output (I_m).

5.2.4 Reliability Dependence on BLT

The we high temperature operating lifetime reliability is performed under the stressing condition of an operating current of 700mA, a relative humidity RH=85%, and a high environmental temperature of 85°C. The aging time beyond the requirement of the standard JEDEC No.22-A101C while extending the test duration by 25% from 1000 to 1250 hour as shown in Chapter 4. Figure 5.6 describes the lumen drop (I_d) at different aging time of packaged devices with different BLTs. The dependence of lumen-drop (I_d) on BLT (d) at an aging time of 500 h follows a power-law relationship $I_d = 0.13d^{0.15}$ as shown in Fig. 9 (b). The same happens to the dependence of lumen-drop (I_d) on BLT (d) at an aging time of 1000 h follows a power-law relationship $I_d = 0.29d^{0.07}$ as shown in Fig. 9 (c). This is fully consistent with the prior result on the dependence of lumen output on the applied pressure since BLT is inversely proportional to the applied pressure.

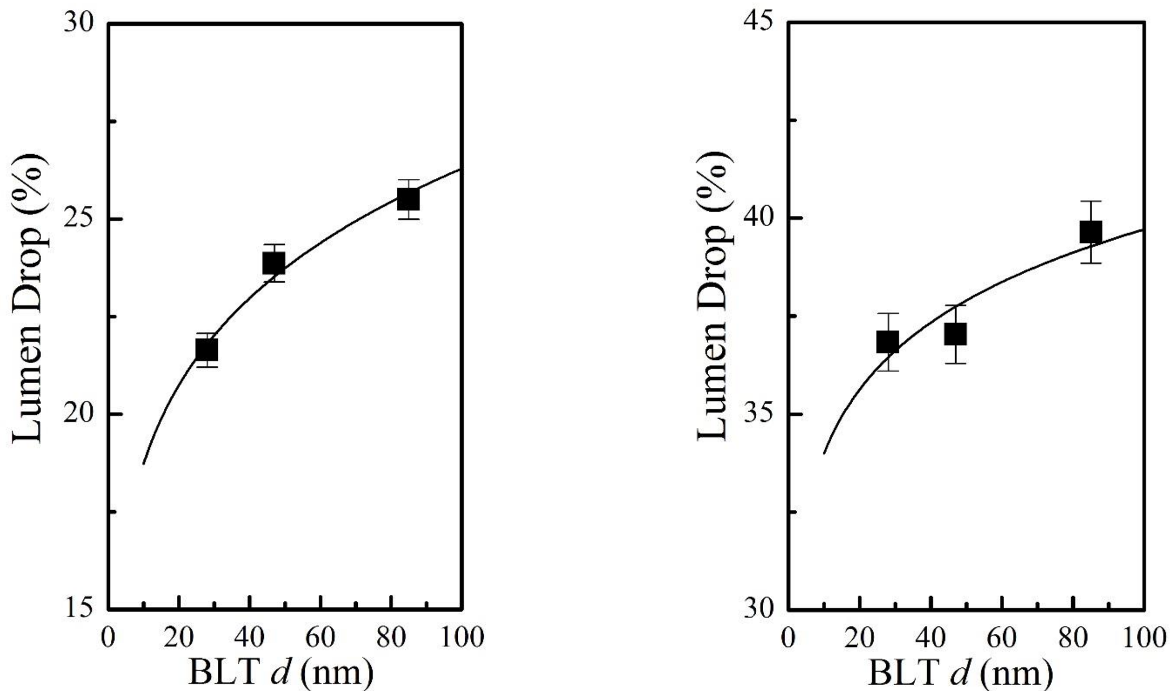

Figure 5.6 The lumen drop (I_d) at aging time of 500h vs BLT(d): it follows a power-law relationship $I_d = 0.13d^{0.15}$ as presented by the solid line; (c) The lumen drop (I_d) at aging time

of 1000h vs BLT(d): it follows a power-law relationship $I_d = 0.29d^{0.07}$ as presented by the solid line.

5.3 Summary

In this Chapter, we discussed the influence of bond-line thickness (BLT) on the device performance enabled by the NL bonding approach. It is evidently to figure out that the electrical resistance, thermal resistance, junction temperature and lumen degradation all have a power-law relationship with the BLT. And the BLT is inversely proportional to the bonding pressure.

These reflect the fact that the performance of packaged device made with the NL bonding approach can be predicted by controlling the bonding pressure during the manufacturing process: with larger bonding pressure, thinner BLT achieved, and a larger total number of contacts is formed, in addition, the individual contact area at each contact is increased, all these result in a reduced contact resistance between the two interconnect bonding surfaces and lead to a smaller electrical and thermal resistance.

Therefore, the BLT plays an important role in determine the performance and reliability of the devices made by NL bonding approach. The electrical resistance, thermal resistance and junction temperature increase with the increasing BLTs. The lumen output decreases with the increasing BLTs and the lumen degradation increases with the increasing BLTs.

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Chapter 6

Device Performance and Reliability Dependence on Surface Morphology

6.1 Introduction

For the present NL bonding method, when two surfaces are brought into contact, they touch at the tips of the higher asperities and the total area of intimate contact is determined by the deformation of the material in these regions under the applied load. The deformation mechanisms encountered at the asperity level control the surface conformity, which intern influences the transmission of heat and electric current across the contact interface [1].

An important property of solid material is surface morphology, the morphology governs the effective surface area and various treatment procedures have been employed to modify the surface properties of modern materials prior to their applications or any further processing [2]. For the bumpless based bonding approach, take the Cu-Cu bonding as an example, it requires precise control over the topography of the interconnection metallic surfaces which thus must be well planarized to reduce the respective surface roughness below 0.1nm using chemical mechanical polishing (CMP), and in some cases, the surfaces must also be plasma activated in an ultra-high vacuum (UHV) of 10^{-4}~10^{-7} Pa. The CMP process usually takes extra time and increase the manufacturing cost. Our present NL bonding method takes the advantage of intrinsic nanoscopic surface roughness and doesn’t need the extra CMP or other surface modification processes.

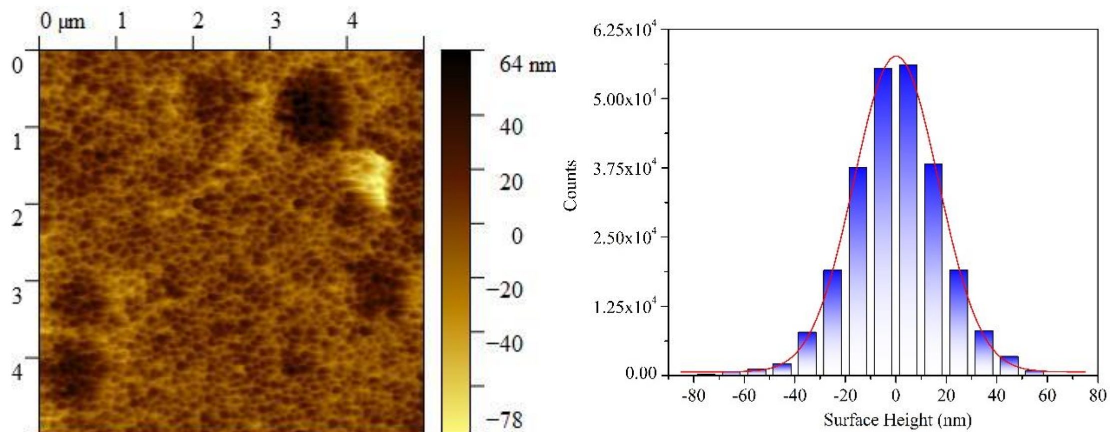
The study of surface morphology on our present NL bonding method is of highly importance because it will exhibit a profound effect on the overall response of electronic components subject to various mechanical, thermal, electrical effects as well as the reliability performance. To study the

effect of the surface morphology on the present NL bonding approach, two different types of substrates are employed, which we name as type-I (SUB-I) and type-II (SUB-II). The packaged devices enabled by the NL bonding approach using different types of substrates are all well controlled with similar BLT=100±5 nm. The voltage-current (I-V) behavior of the fabricated device is determined by using the Keithley 2450 source meter. The junction temperature and thermal resistance for the overall die-substrate interconnection and bonding layer is measured under natural convection condition. The current source with corresponding forward voltage was supplied by Everfine power generator, and the lumen output was measured in a LabSphere integral sphere with the suggested maximum input constant current of 700 mA. The wet high temperature operation life (WHTOL) reliability test goes beyond the requirement of the industrial standard JEDEC No.22-A101C by extending the test duration by 25% from 1000 hours to 1250 hours. All the samples were placed on the heat sink and evaluated by measuring the lumen maintenance as a function of aging time at a temperature of 85°C and a relative humidity of 85% with the maximum suggested input DC current of 700 mA, which is aged in a high temperature and humidity chamber (GLMP50, Chemkorea Corp.)

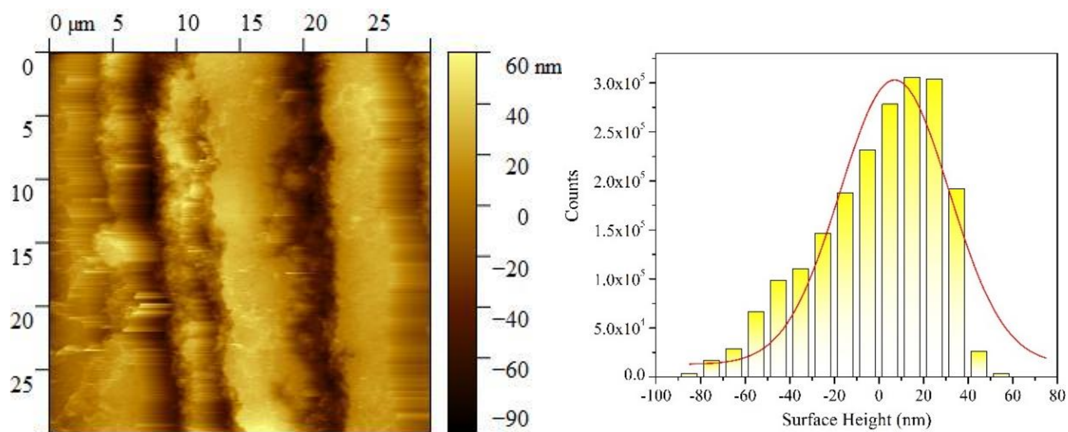
6.2 AFM Analysis for Surface Roughness Heights Distribution on Metallic Pads

The surface morphology of the two different types of the metallic pads on the substrate are observed by using AFM (Keysight 7500 system). Fig. 6.1 presents surface morphology for the die and substrate metallic pads. As shown in Fig. 6.1(a), the AFM image of the die pad shows surface topography and the histogram of roughness height distribution. The surface roughness ranges from -78±2 nm to +64±2 nm. Figure 6.1(b) and (c) presents the AFM image as well as the surface roughness distribution of the different two types of substrate pad. It is noted that the surface roughness of

substrate-I ranges from -90±2 nm to +60±2 nm, and the surface roughness of substrate-II ranges from -113(±2) nm to +100(±2) nm.



(a)



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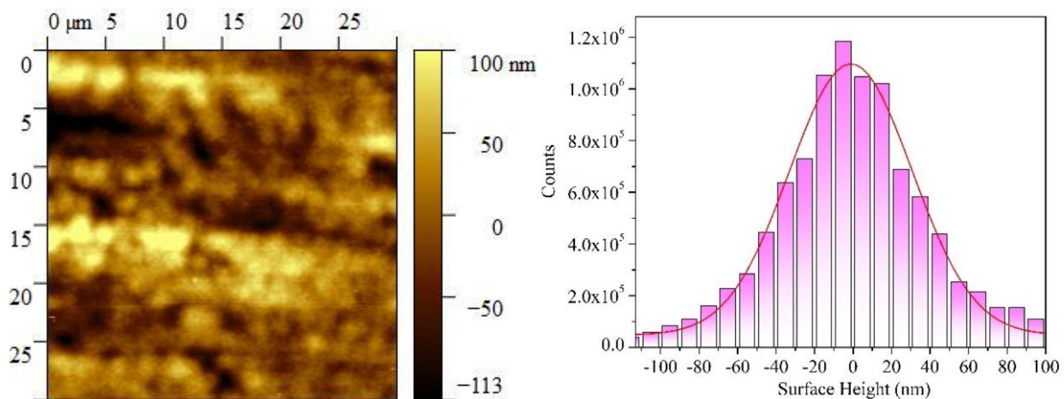


(c)

Figure 6.1 Atomic force microscopy (AFM) for the surface topography and surface roughness distribution (a) the semiconductor die metallic pads; (b) the package substrate-I metallic pad; (c) the package substrate-II metallic pad.

Two sets of devices made using the present NL bonding method have same BLT value of 100±5 nm. Cross-sectional SEM images are taken at various locations along the die-substrate bonding layer for each sample and the mean is taken to estimate the BLT value, marked with yellow dashed lines in Fig 6.2. Most of the heights of ridges and valleys on metal pads of die and substrate are between 0~20 nm according to AFM measurements (see Fig.6.1). Therefore, the boundary of the BLT looks quite flat in SEM images.

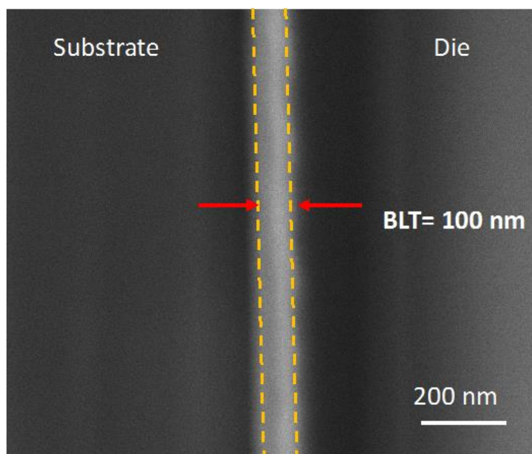


Figure 6.2 SEM/FIB observation of BLT of nano-locking chip bonding approach.

The contact electrical (and thermal) conductivity based on the formation of “nano-locking” structure at each contact spot can be summarized as a function of surface heights distribution:

$$\gamma = \alpha \cdot [w_1 r_1 + w_2 r_2 + \cdots + w_i r_i]$$

Where w_i is the probability of the contacts for the certain surface heights range, r_i is the ratio of the certain surface heights range, and n is the number of the bins considered for the surface heights

distribution that establish the effective "nano-locking" structure under certain BLT, α is the conductivity of unit effect area.

The w_i is a binary value considered by threshold method, for simplification [3]. When the certain height distribution of the surface roughness contributes to the formation of the "nano-locking" structure under specific BLT, w_i=1, otherwise, if the certain height distribution doesn't contribute to the formation of the "nano-locking" structure, $w_i = 0$. In the real-world scenario, the w_i should be a continuous value between 0 and 1. Then, the value of w_i can be further studied by using machine learning which is out of the scope of this study [4].

To achieve the electrical interconnection with specific BLT= 100±5 nm, the surface roughness heights range of the package substrate is selected according to the surface roughness heights distribution on the semiconductor die to establish the effective "nano-locking" structure. Table 6.1 describes the certain frequency percent distribution of surface roughness heights for the die and the two different types of package substrates. The total frequency percent of qualified surface roughness heights distribution for substrate type I (SUB-I) is about 11%. And the total frequency percent of qualified surface roughness heights distribution for substrate type II (SUB-II) is about 21%.

Since the BLTs of the two packages are controlled the same, the surface morphology of the metallic pads on semiconductor die is the same, therefore the overall bonding layer using the substrate type II (SUB-II) has a larger total contact number and contact area compared with the case using the substrate type I (SUB-I). Figure 6.3 shows the distribution of the real effective contact area on the two different package substrates within the scanning area which forms the "Nano-locking" structure under the same BLT.

Table 6.1 Frequency Percent Distribution of Surface Roughness Heights

Semiconductor Die		Substrate	SUB-I	SUB-II
Heights (nm)	Frequency Percent	Heights (nm)	Frequency Percent	Frequency Percent
0-10	0.2242	90-100	0	0.0113
10-20	0.1529	80-90	0	0.0160
20-30	0.0761	70-80	0	0.0160
30-40	0.0324	60-70	0	0.0222
40-50	0.0138	50-60	0.0016	0.0264
50-60	0.0035	40-50	0.0131	0.0456
60-70	0.0004	30-40	0.096	0.0604
-10-0	0.2248	100-110	0	0.0071
		Total	0.11	0.21

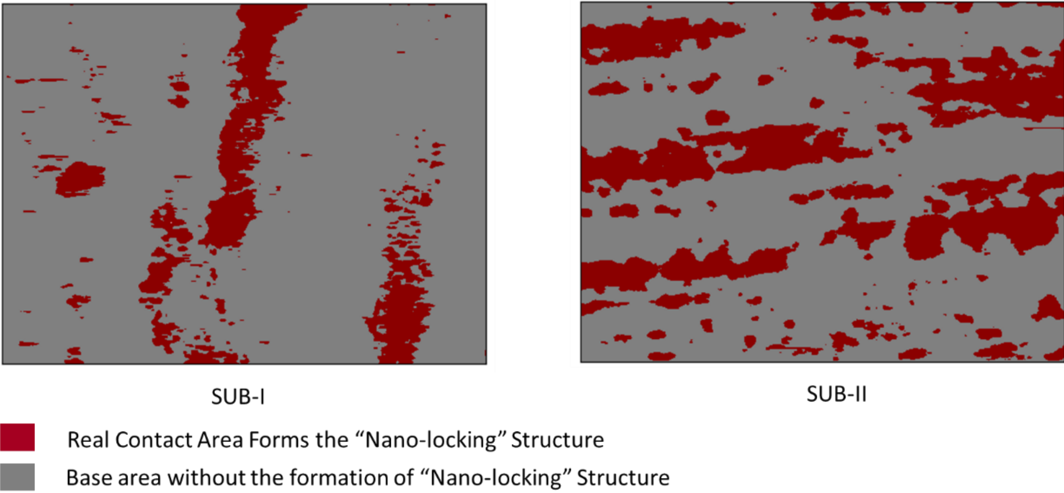


Figure 6.3 Real contact area distribution on the metallic pads of the two different types of package substrates under the same BLT.

6.3 Device Performance and Reliability Dependence on Surface Roughness Heights Distribution

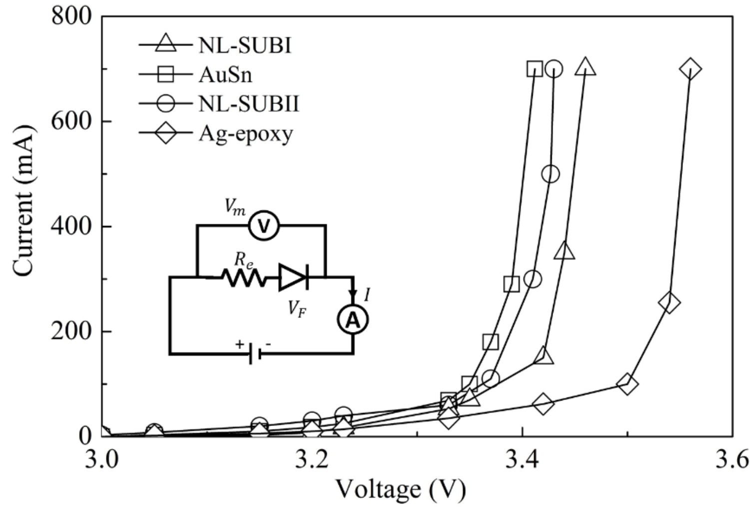
6.3.1 Electrical Performance Dependence on Surface Roughness Heights Distribution

Fig.6.4(a) presents the electrical performance for devices made by the NL bonding method with different package substrates, and its comparison to two conventional die-substrate bonding methods. According to Fig. 6.4 (a), the measured voltage for the devices made by the NL approach are all smaller than that for the devices using Ag-epoxy bonding method and larger than that for the devices using AuSn bonding method under the same forward current of 700 mA. The effective interconnection electrical resistance $R_e = dV/dI = (V_m - V_F)/I_F$, where V_m is the measured device voltage, V_F is the forward voltage and I_F is the forward current.

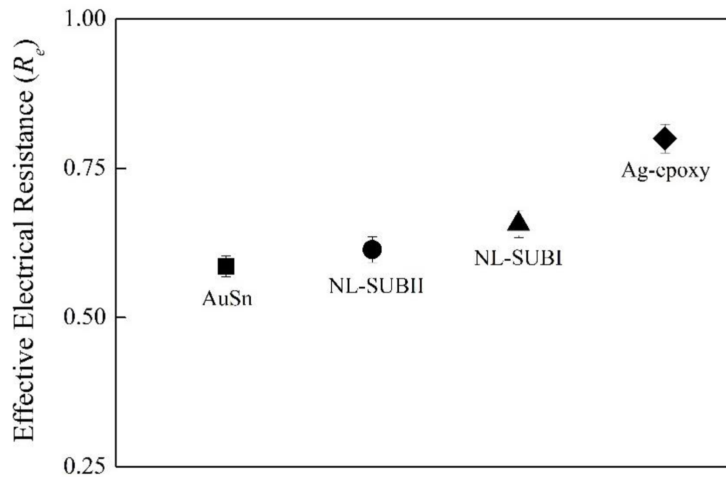
Figure 6.4(b) presents the extracted R_e value of devices made by the NL bonding method with different substrates and its comparison to two conventional die-substrate bonding methods: the R_e of devices made by NL bonding with package substrate type I (SUB-I) is about 7% higher than the R_e of NL bonding with package substrate type II (SUB-II). This is easily understandable because the package substrate type II has a larger frequency percent of the qualified height distribution that can establish a larger total number of contacts and larger overall contact area under the same BLT as shown in Table 6.1. Therefore, the R_e of NL bonding with package substrate type II (SUB-II) is decreased.

In addition, the R_e value of NL bonding method with package substrate type II (SUB-II) is about 4.8% larger than case of AuSn bonding and is about 23% smaller than the case of Ag-epoxy bonding. This is because the defects such as voids, delamination or cracks introduced at the interfaces during

curing process for Ag-epoxy will largely increase the interfacial resistance and degrades the corresponding electrical performance [5].



(a)



(b)

Figure 6.4 (a) Measurement of current (I) and voltage (V) relationship for the devices made of the present NL with different substrates and conventional die-substrate interconnection and bonding methods. The open square symbol (□) represents the AuSn bonding; the open circle symbol (○) represents the NL bonding with substrate type-II; the open triangle symbol (△) represents the NL bonding with substrate type-I; the open rhombus symbol (◇) represents the Ag-epoxy bonding. The solid curve represents the best I-V fitting. (b) The R_e of packaged devices made by NL bonding with different substrates and different die-substrate interconnection and bonding methods: the solid square symbol (■) represents AuSn bonding with an industrial standard BLT value of 20± 2 μm; the solid circle symbol (●) represents the NL bonding with substrate type-II; the solid triangle symbol (▲) represents the NL bonding

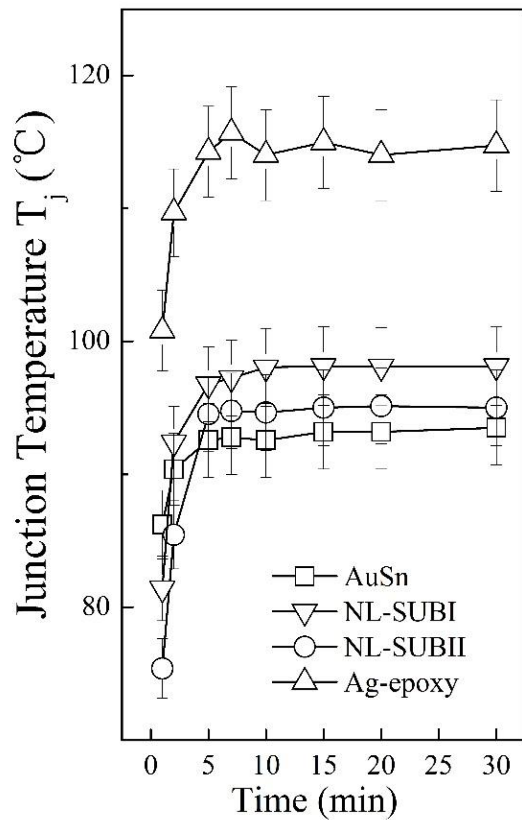
with substrate type-I; the solid rhombus symbol (◆) represents the Ag-epoxy bonding with an industrial standard BLT value of 25± 2 μm.

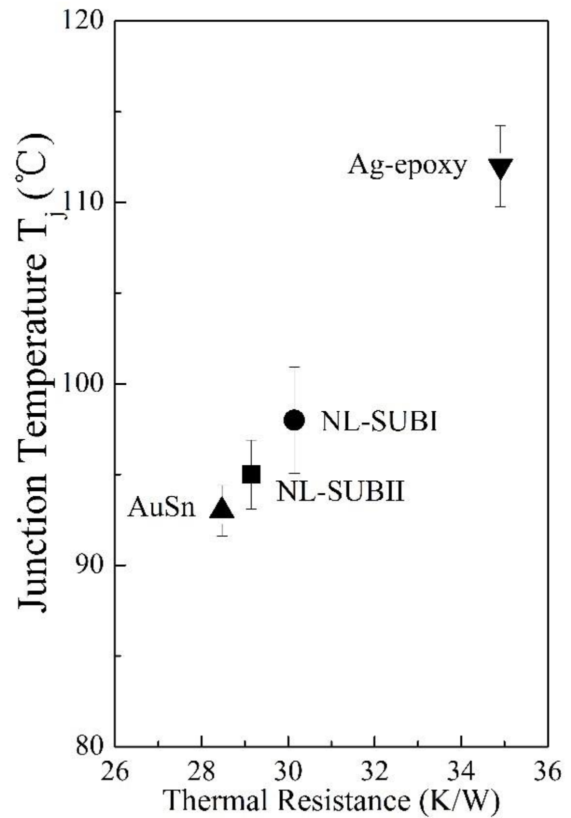
6.3.2 Thermal Performance Dependence on Surface Roughness Heights Distribution

Fig. 6.5 presents the thermal performance for the devices made by the NL approach with different substrates and two conventional die-substrate bonding methods. Fig. 6.5 (a) presents the measurement of the die junction temperature (T_j). It is evident from the device made by the NL bonding method with substrate type I (SUB-I) is about 3℃ higher than the devices made by substrate type II (SUB-II). In addition, the junction temperature (T_j) of devices using NL bonding method with substrate type II (SUB-II) is about 2℃ higher than the AuSn bonding, and about 19℃ lower than Ag-epoxy bonding.

In Fig. 6.5 (b), the thermal resistance (R_{th}) of the packaged devices is proportional to its junction temperature (T_j). The R_{th} of the packaged devices using NL with substrate type II (SUB-II) is about 3% smaller than the case of using substrate type I (SUB-I), and is about 2% larger than the AuSn bonding, and about 16.5% smaller than the Ag-epoxy bonding.

As discussed above, the package substrate type II has a larger frequency percent of the qualified height distribution that can establish more total number of contacts and larger contact area under the same BLT as shown in Table 6.1. Therefore, the R_{th} of devices made by package substrate type II will be decreased. However, for the cases of Ag-epoxy bonding, the existence of defects at interfaces during the curing process can greatly affect the interfacial resistance, heat dissipation and lead to a largely increase for the overall R_{th} which degrades the thermal performance.





(a) **(b)**

Figure 6.5 (a) The die junction temperature (T_j) of the devices made by NL bonding method with different substrates and two conventional die-substrate bonding methods: the open circle symbol (○) represents T_j data for the device made by NL bonding with substrate type-II, the open downside triangle symbol (▽) represents T_j data for the device made by NL bonding with substrate type-I, the open square symbol (□) represents T_j data for the device made by the AuSn bonding with an industrial standard BLT value of 20± 2 μm, the open upside triangle symbol (△) represents Ag-epoxy bonding with an industrial standard BLT value of 25± 2 μm. (b) The relationship between T_j and R_{th}: the solid circle symbol (●) represents NL bonding with substrate type-I, the solid square symbol (■) represents NL bonding with substrate type-II, the solid upside triangle (▲) represents AuSn bonding with an industrial standard BLT value of 20± 2 μm, the solid downside triangle (▼) represents Ag-epoxy bonding with an industrial standard BLT value of 25± 2 μm.

6.3.3 Optical Performance Dependence on Surface Roughness Heights Distribution

Figure 6.6 presents the optical performance in terms of normalized lumen output at the suggested maximum input current of 700 mA for the devices made by the NL bonding method with different

substrates and the comparison to two conventional die-substrate bonding methods. It is evident that the lumen output for the devices made by NL bonding with package substrate type II (SUB-II) is enhanced about 2% higher compared with the devices using package substrate type I (SUB-I). This is fully consistent with the prior results on the dependence of T_j and R_{th} on the total contact number and contact area under the same BLT. In addition, the lumen output for the devices made by the NL bonding approach with package substrate type I (SUB-I) is about 6% higher than the Ag-epoxy bonding, and about 4% lower than AuSn bonding.

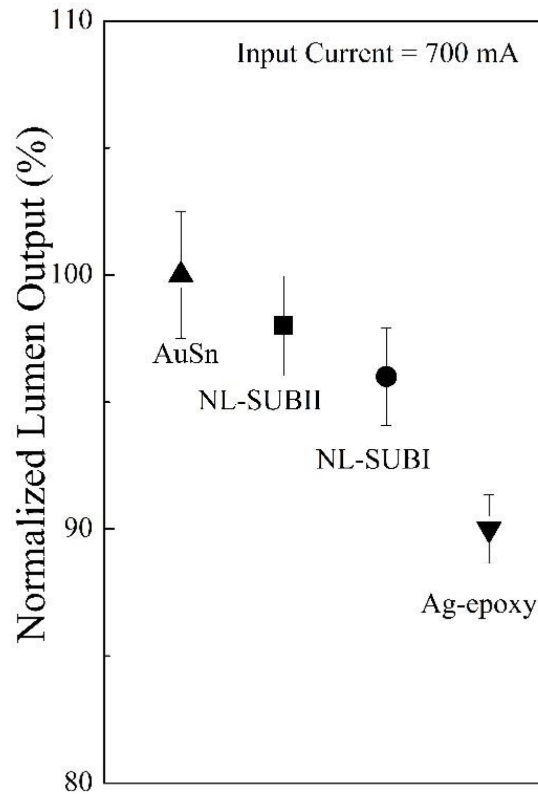


Figure 6.6 Normalized lumen output of the devices made by NL bonding method with different substrates and two conventional die-substrate bonding methods at an input current of 700 mA: the solid circle symbol (●) represents NL bonding with substrate type-I, the solid square symbol (■) represents NL bonding with substrate type-II, the solid upside triangle (▲) represents AuSn bonding with an industrial standard BLT value of 20± 2 μm, the solid downside triangle (▼) represents Ag-epoxy bonding with an industrial standard BLT value of 25± 2 μm.

6.3.4 Reliability Dependence on Surface Roughness Heights Distribution

Figure 6.7 presents a comparison of the aging time-dependent lumen maintenance of the devices made with the NL approach with different substrates and the other two conventional methods under the industrial standard condition of high chamber temperature of 85℃ and high relative humidity of 85% for a total duration of 1250 hours. The y-axis represents relative change in the lumen maintenance normalized to the initial lumen output. The x-axis represents the aging or stressing time. It is evidently that at the aging time of 1250 h, the devices made by NL bonding method, the lumen maintenance using package substrate type II (SUB-II) is about 3% higher than the devices using package substrate type I (SUB-I). The lumen maintenance of the packaged LEDs made by NL with packaged substrate type I (SUB-I) is about 4% lower than device made by AuSn bonding and about 5.1% higher than device made by the Ag-epoxy bonding. The superior reliability associated with the NL bonding method with package substrate type II (SUB-II) compared with the devices using package substrate type I (SUB-I) is evidently resulted from the observed reduced electrical resistance as well as a reduction in thermal resistance, as discussed above.

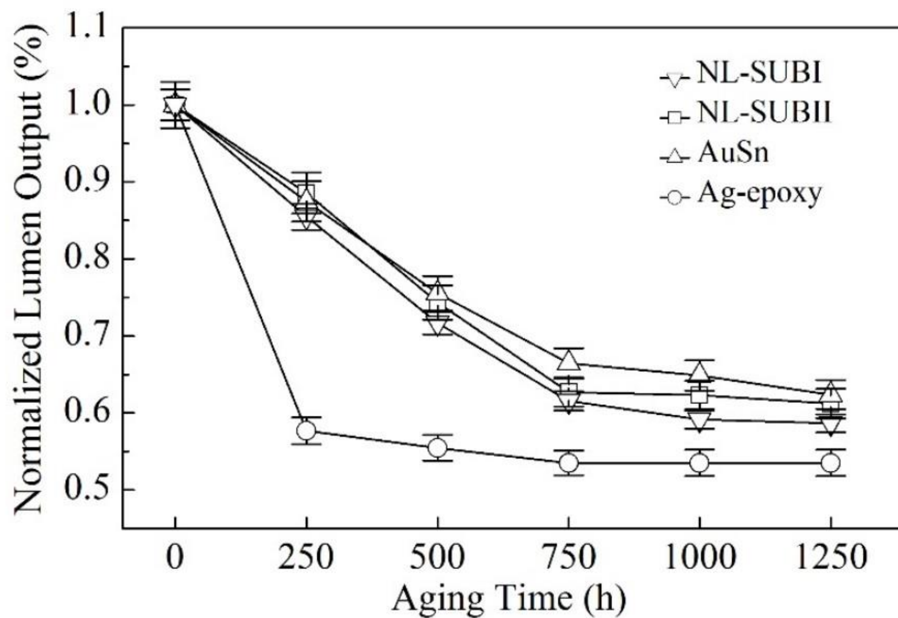


Figure 6.7 Long-term lumen maintenance of the devices made by NL bonding method with different substrates and two conventional die-substrate bonding methods as a function of aging time under the stressing condition of an operating current of 700mA, a relative humidity RH=85%, and a high environmental temperature of 85℃: the open downside triangle symbol (▽) represents the experimental data for the device made by NL bonding with substrate type-I, the open square symbol (□) represents the experimental data for the device made by NL bonding with substrate type-II, the open upside triangle symbol (△) represents Ag-epoxy bonding with an industrial standard BLT value of 25± 2 μm, the open circle symbol (○) represents the experimental data of Ag-epoxy bonding with an industrial standard BLT value of 20± 2 μm. This Wet High Temperature Operating Life (WHTOL) test goes beyond the requirement of the standard JEDEC No.22-A101C while extending the test duration by 25% from 1000 to 1250 hr.

6.4 Summary

The potential of an innovative off-chip bonding method has been explored which can establish a simultaneous electrical, thermal and mechanical connection between two metallic bonding surfaces without requiring a prior time-consuming and expensive surface nanoscopic planarization and without requiring any intermediate conductive material. This "nano-locking" method for chip interconnection and bonding has been demonstrated as an example by its application for the attachment of high-power GaN based semiconductor dies to its device substrate. The surface morphology on metallic pads plays an important role in forming the effective total number of contacts and overall contact area between the ridges and valleys on the two different bonding surfaces: larger frequency percent of qualified surface roughness heights distribution contributes to smaller electrical (and thermal) resistance between the two bonding surfaces, resulting in a lower overall device electrical resistance, and a reduced thermal resistance, and thus an improved overall device performance and reliability. The present work opens a new direction for scalable, reliable and simple nanoscale off-chip electrical interconnection and bonding for nano- and micro-electrical devices as well as other functional devices.

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Chapter 7

Conclusion and Future Perspectives

In this study, to solve the interconnection physical limits challenge of high integration density in advanced chiplet based system-on-chip or system-in-package enabled by 2.5D or 3D packaging technology, a new nano-locking (NL) bonding methodology is proposed by using a pure polymer without adding any metallic fillers to achieve electrical interconnection.

This NL bonding approach has been successfully demonstrated for the die-to-substrate bonding in the packaging of high-power GaN based dies, as an example. The NL structure is formed by taking advantage of the surface topographic features between the metal pads on the die and substrate. Although this process is sufficiently simple in concept, it has never been demonstrated for semiconductor die electrical connection and bonding. The electrical and thermal conduction mechanism for the present NL bonding approach is achieved by the contact area/size and total number of contacts. Without adding any metallic fillers, the bond-line thickness is scalable and can be controlled by different bonding pressure during the manufacturing process. By taking advantage of the intrinsic nanoscopic surface roughness, no extra surface modification such as chemical mechanical planarization is needed. The fabrication of the packaged devices includes die attach, curing, soldered to printed print circuits board and encapsulation before making performance evaluation and different reliability tests.

The cost and manufacturing process can be greatly reduced as well. Additionally, the mechanical interconnection is stabilized by using the pure dielectric polymer without introducing any delamination at the interface between adhesive and metal pads. The electrical and thermal conduction

mechanism is achieved through the contact s between the ridges and valleys on the bonding surfaces and is determined by the total number of contacts and contact area at each contact.

The packaged high-power GaN based dies enabled by NL bonding approach have been shown to exhibit superior optical, electrical and thermal performances, and moreover a remarkable long-term reliability under strict industrial stressing conditions. The electrical and thermal performance all follow a power relationship with the bond-link thickness. This is because the bond-line thickness is inversely proportional to the bonding pressure and thinner bond-line thickness leads to more contacts between bonding two surfaces.

When the bond-line thickness is compressed to ultra-thin thickness, the observed remarkable enhancement of device performance and reliability has been clarified to be related with the perfect interfacial contact as well as die-to-substrate adhesion strengthening between pure adhesive and metal pads. The extracted electrical resistance for the devices made by the NL bonding approach with a BLT of 85±5 nm is about 12% lower than the conventional AuSn bonding method and is about 35% lower than the conventional Ag-epoxy bonding. The junction temperature of the device made by the NL method with a BLT=28±5 nm is about 10℃ lower than the AuSn bonding, and about 30℃ lower than Ag-epoxy bonding. Based on the measured junction temperature and the heat generated from input power, the thermal resistance the thermal resistance of the NL bonding with a BLT=28±5 nm is about 7% lower than the AuSn bonding, and about 26% lower than the Ag-epoxy bonding. The devices made with the NL method (BLT=28±5 nm) have a much higher lumen output which is about 9.8% higher compared with the AuSn bonding, and about 17% higher compared with the Ag-epoxy bonding.

According to the experimental result of wet high temperature operating life test, the lumen maintenance of packaged devices enabled by NL bonding method decreases with the increasing bond-

line thickness. It is evidently that at the aging time of 1250 h, the NL method in the case of BLT=28±5 nm results in a much higher lumen output, i.e., about 4% higher than device made by the AuSn bonding method, and about13% higher than the device made by the Ag-epoxy bonding method. All the packaged devices enabled by NL bonding method pass the thermal cycling test. And for packaged LEDs with Ag-epoxy and AuSn boding, 2 out of 15 samples are failed. Both the pass rate of Ag-epoxy and AuSn bonding are only about 86.7% after the thermal cycling test.

The resulting bond-line thickness has an effect on the performance of packaged devices enabled by the NL bonding methods: electrical resistance, thermal resistance, junction temperature and lumen degradation all have a power-law relationship with the BLT. Both the electrical and thermal resistance decrease with the thinner BLT and the lumen output increases with decreasing bond-line thickness. The lumen degradation at different aging time increases with the thicker bond-line thickness.

The surface morphology on metallic pads also plays an important role in forming the effective total number of contacts and overall contact area between the ridges and valleys in the present NL bonding method. Two different packaged substrates with different surface morphology analyzed by AFM observation on bonding surfaces have different contributions to the device performance of packaged devices enabled by NL bonding method: larger frequency percent of qualified surface roughness heights distribution contributes to smaller electrical (and thermal) resistance between the two bonding surfaces, resulting in a lower overall device electrical resistance, and a reduced thermal resistance, and thus an improved overall device performance and reliability.

Besides silicone adhesive, different pure dielectric adhesive can also be applied as the die-attach material for present NL bonding approach such as epoxy resin or polyimides. Because epoxy resin formulations are also important with many applications in electronic packaging industry [1]. There are several outstanding physical properties of epoxy resin as die-attach adhesive, it has excellent such

as resistance to thermal cycling, mechanical shock and vibration resistant, good adhesion to mismatched coefficients of thermal expansion. More importantly, epoxy is also void free and advanced to heat dissipation and low humidity sensitivity.

In addition, the present NL bonding method can also be applied to other different types of semiconductor devices. For example, this NL bonding method can be applied to vertical LED using wire bonding after die-attach process. The present NL bonding approach is also a promising candidate for advanced mini-LED display technology. As the size of LEDs decreasing, the applications transit from illumination to display using flip-chip assembly. However, for the advanced mini-LED display, the bonding technology is the roadblock since the size of mini-LED is too small and a large amount of metal in the solder paste may cause short circuit easily. Therefore, the adhesion process technology is a big obstacle for commercializing the micro LED process. Without adding metallic fillers, the present pure dielectric adhesive also can be applied to the die attach process of flexible electronics packaging and skin sensors to achieve the electrical interconnection and bonding with high yield and stable reliability.

Further reliability tests such as low/high temperature storage tests can be operated to study the effect of time and temperature under storage condition for thermally activated failure mechanism of solid-state electronic devices [2]. The packaged devices will be aged in a temperature-controlled chamber capable of maintaining the specified temperature over the entire sample population under test.

The present work opens up a new direction for the high integration density of advanced 2.5D/3D ICs without using electrically conductive adhesives and fine pitch micro-bumps, while enhancing thermal and electrical performance as well as the reliability of advanced semiconductor devices. This

method has large potential for the high-volume manufacturing with high yield in the semiconductor industry.

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