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A 238 GHz, 0.5 W, 2.3 mm^2 InP HBT Power Amplifier with Cascade Topology and 4:1 Series Power Combining Technique

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by

Hai Yu

Committee in charge:

Professor Mark Rodwell, Chair

Professor James Buckwalter

Professor Luke Theogarajan

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The thesis of Hai Yu is approved.

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James Buckwalter, Committee Member

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Luke Theogarajan, Committee Member

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Mark Rodwell, Committee Chair

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ABSTRACT

A 238 GHz, 0.5 W, 2.3 mm^2 InP HBT Power Amplifier with Cascade Topology and 4:1 Series Power Combining Technique

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This work demonstrates the design of a MMIC solid state class-A power amplifier in 250nm InP HBT technology achieving 0.5W saturated output power at 238 GHz at compressed gain of 14dB and power added efficiency of 10%. The 3dB bandwidth is 230 GHz to 242GHz. The power amplifier uses 4:1 travelling wave combiner to combine the output power of 8 power cells. Each power cell is a 3-stage cascaded amplifier with 2 common-base gain stage and 1 common emitter power stage.

Index Terms – Millimeter wave integrated circuit, solid state power amplifier, MMICs, common base power amplifier, travelling wave combiner, distributed power amplifier.

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II. INTRODUCTION

To enable future high resolution imaging systems and radars, interest and demand for sub-THz solid state power amplifier has been ever increasing [1]. A frequency spectrum around 220GHz is specifically useful, as a low loss atmosphere window resides at this frequency. Nevertheless, power output is still precious given high attenuation at this frequency.

The highest output power around 220GHz up to now was reported from a solid-state power amplifier was a 250nm HBT MMIC power amplifier with 180mW saturated output power at 214GHz. [2]

The approach taken by previous work is cascode amplifiers combined by Wilkinson power combiner. The cascode topology ensures higher gain, but causes inefficient area usage. Moreover, the common base(CB) amplifiers were biased at emitter by a biasing resistor. Huge amount of DC power is burnt on the resistor and thus the design as very low efficiency. The Wilkinson power combiner which contains quarter-wavelength has low area efficiency and higher loss, too.

In this work, double-sided 4:1 balun is used to combine output power from 8 power cells. Each power cell has 3 stages of power amplifiers in cascade, with the first 2 stages to be gain stages using common base topology and the last stage as power output stage using common emitter topology. Cascade topology is used so that the large DC blocking capacitor is replaced by a small one which can be absorbed into matching network between stages. All stages are biased at class-A quiescent point. Comparing to previous work [2], the common base stages were biased using current mirror at base node and thus a great amount of DC biasing power is saved.

II. 250NM INDIUM PHOSPHIDE HBT PROCESS

The power amplifier reported in this work is designed in 250nm InP HBT technology[3]. One single HBT has a peak f_{max} = 700GHz and f_T = 400GHz.

For maximum output current and thus maximum output power, all transistors in this design have emitter area of 6um×0.25um, which is the maximum value allowed in this technology.

The maximum collector current density is J_C = 12mA/um^2 and thus around 18mA for transistor with maximum emitter area. The collector-emitter breakdown voltage is ~4.5V.

III. POWER CELL DESIGN

A. Trade-off between Output Power and Gain

While the purpose of power amplifier is to deliver as highest power as possible to the load, high gain is also preferred to achieve higher power added efficiency and to relax power source requirement. However, there is often a 'gain and power trade-off'. To achieve high output power, amplifier should be loaded with an optimal load resistance, $R_{L,opt}$. This matching condition is called loadline matching. On the other hand, to achieve high gain, amplifier is loaded with impedance $Z_{L,conj}$, which is conjugate to the output impedance of the amplifier, resulting a power gain close to maximum available gain(MAG). This matching condition is called gain matching or conjugate matching. Determined by transistor's maximum voltage and current rating and its internal parasitic components, different topologies have different $Z_{L,conj}$ and $R_{L,opt}$. When these two values are close to each other, the amplifier can have both high gain and high output power at the same time. However, when they are very different from each other, the amplifier must lean towards one and to

sacrifice the other one. Due to the above reason, in this technology, common base is better to be used as gain stage and common emitter is better at playing the role of output stage. To achieve both high gain and high power output, this power amplifier is designed to have 3 stages in each cell, and uses common emitter as its final output stage to output maximum amount of power and uses common base as gain stages.

B. Output Stage

Given the scarcity of power at frequency as high as 220GHz, efficiency is sacrificed for high output power whenever possible. Also, most intended applications of the design, such as imaging systems, have direct access to power grid, which makes efficiency not the most critical limitation of the design. Therefore, this design chose class-A bias point for all stages to maximize output power.

To achieve the best output power possible for this technology, the load line shown in Figure 1 stage is used at the power stage.

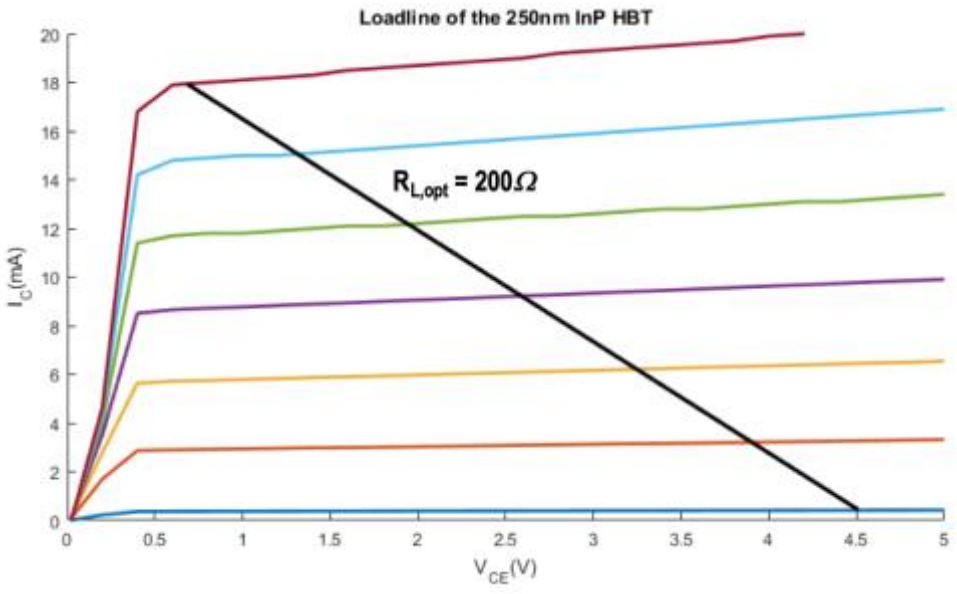

Figure 1. Load line at maximum output power condition

The load line extends to V_{max} at right, which is the collector and emitter breakdown voltage BV_{CE} = 4.5V; to V_{min} at left, which is the knee voltage of $V_{CE} = V_K$ = 0.8V, where the transistor drops to linear region; to I_{max} at top, which is the maximum collector current allowed for the transistor to operate safely; to I_{min} at bottom, which is zero when the transistor is cutoff.

Therefore, the output power for each cell is

$$P_{out} = (V_{max} - V_{min}) \times \frac{I_{max} - I_{min}}{8}$$

$$= (4.5V - 0.8V) * \frac{18mA - 0mA}{8} = 8.325mW \quad (1)$$

The optimal load resistance for maximal output power is

$$R_{L,opt} = \frac{V_{max} - V_{min}}{I_{max} - I_{min}}$$

$$= \frac{4.5V - 0.8V}{18mA - 0mA} \approx 200\Omega \quad (2)$$

Hence, for class-A power amplifier, the quiescent biasing point is at $I_{C,Q}$ = 9mA and $V_{CE,Q}$ = 2.7V. At this quiescent biasing point, f_{max} is 590GHz and f_T = 350GHz.

The double-sided balun which is explained in Section IV present 25Ω at each of its ports. Therefore, 8 transistor fingers are used so that the optimal load resistance is

$$R_{L,shunt} = \frac{R_{L,single}}{8} = 25\Omega \quad (3)$$

at the node where the output of the 8 of the transistors are combined in shunt. Thus, the total maximum output power by a power cell is then

$$P_{sat,3} = P_{out} \times 8 = 66.6mW = 18.2dBm \quad (4)$$

, which is the saturated output power of the CE stage.

At frequency as high as 220GHz, the collector-base capacitance(Ccb) of the transistor plays a significant role in reducing the MAG of a common emitter amplifier. Biased at the

quiescent point, the MAG of a single transistor in common emitter topology is only 5dB. And when loaded with $R_{L,opt}$, the power gain is 4dB. To get a reasonable gain of around 15dB, more than 5 of these CE stages are needed when the loss of the matching network between each stage is considered. This number of stages introduces considerable amount of loss in matching networks and means large chip area occupancy.

C. Gain Stages

To get more gain, CB topology is used for gain stages preceding the last output stage. Low MAG is caused by large feedback capacitance Ccb for common emitter topology. While for CB topology, the feedback capacitance is the collector-emitter capacitance(Cce), which is much smaller than Ccb for this technology. Indeed, the MAG for CB topology is 12dB. With the transistor footprint be included into the simulation, which adds additional 2dB loss, the MAG of a CB cell is 10dB.

However, in this technology, the conjugate match impedance $Z_{L,conj}$ for maximum gain of CB topology is quite different from the optimal load resistance $R_{L,opt}$ for maximum output power. When loaded with $Z_{L,conj}$, the common base amplifier's output clips at very low output voltage swing, resulting in very limited output power. On the other hand, when loaded with $R_{L,opt}$, the power gain of the common base amplifier is below 3dB. However, in this technology, the optimal load resistance $R_{L,opt}$ and the conjugate match impedance $Z_{L,conj}$ happen to be similar values for CE amplifier. When presented with best $R_{L,opt}$, the CE amplifier is capable of outputting 8.3mW power with 4dB power gain, nearly its MAG which is 5dB. Namely, when outputting the same amount of power of 8.3mW, which is the maximum value for safe operation for this technology, CE has 1.5dB higher power gain than its CB counterpart. Therefore, although having lower MAG, CE is more suitable for the last

power output stage. CB is still good for gain stage that precedes the power stage, since only moderate output power is required.

To determine the load impedance of the CB stages, there is a continuous 'spectrum' to choose from. When loaded with an impedance that is closer to $Z_{L,conj}$ than to $R_{L,opt}$, the CB amplifier can provides relatively high gain but moderate output power. On the other hand, when loaded with an impedance that is closer to $R_{L,opt}$ than to $Z_{L,conj}$, the CB amplifier has lower gain but relatively high output power. Thus, the two gain stages are designed differently, with different emphasis on power gain and power output. As the signal being amplified, the latter stages need to have higher power output capacity. Hence, the second gain stage that is closer to the power stage should have higher power output capacity, sacrificing its power gain, by choosing the load impedance to be closer to $R_{L,opt}$. While for the first gain stage, its power output capacity requirement is further relaxed by the power gain of the second gain stage, so it can lean towards to gain matching more and thus have higher power gain.

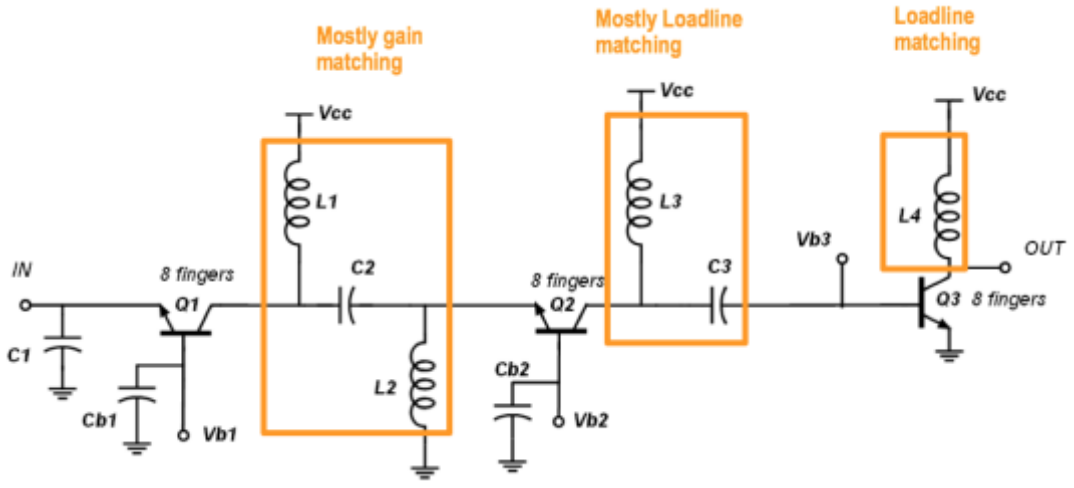

Figure 2. Matching Design of the Power Cell

Figure 2 is the schematic of the power cell. Q3 is the 8-finger common emitter transistor for power output stage. The inductor at its collector serves as matching network at its output. It cancels out the output capacitance of the transistors so real impedance, which is the load line resistance can be presented to the amplifier's output. Vb3 is base bias voltage provided by current mirror. Q2 is the 8-finger common base transistor for the second gain stage. The inductor L3 serves as DC current path for Q2 and the capacitor C3 is the DC blocking capacitor between stage 2 and stage 3. To lower the number of passive components to improve loss and area occupancy, L3 and C3 are also designed to serve the function of matching network between stage 2 and stage 3. This matching network transforms the input impedance of the 3rd stage to an impedance Z_{L2}, as shown in Figure 3.

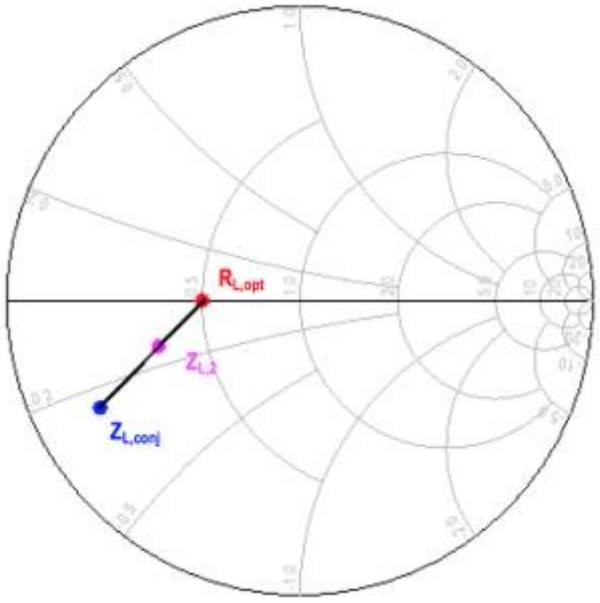

Figure 3. Matching Design of the Power Cell

$Z_{L,2}$ is a value close to $R_{L,opt}$, as calculated in (3), but compromised to the conjugate matching impedance of the CB amplifier, $Z_{L2,conj}$ = 6.8-12.3j Ω, which is the impedance of the center of the power gain circles on Smith Chart. $Z_{L,2}$ is picked on the line connecting

$R_{L,opt}$ and $Z_{L2,conj}$ on the Smith Chart. When $Z_{L,2}$ is closer to $R_{L,opt}$, the amplifier has higher power output capacity but lower power gain, and vice versa when it is close to $Z_{L2,conj}$.

A reasonable value of $Z_{L,2}$ should enable the second stage to deliver enough amount of power to drive the 3rd CE stage while maintaining good power gain. Given the power gain and output power trade-off, the $Z_{L,2}$ is chosen to allow the 2nd CB stage to have a maximum output power just large enough to drive the 3rd stage to its saturation. Since the CE stage has a power gain of 4dB, 14dBm input power is required to drive it to its saturation power of 18dBm. With the 2dB loss of the matching network considered, the output capacity of the 2nd CB stage should be 16dBm. Thus, $Z_{L,2} = 16.7\text{-}7j\Omega$ is chosen, which is shown on Figure 3. This load impedance allows the 2nd CB amplifier to have $P_{sat,2} = 16.3$dBm of saturated output power and a power gain of 7dB. Then, an L-C matching network, which consists L3 and C3, is designed to transform the input impedance of the 3rd stage to $Z_{L,2}$.

In terms of design complexity, CB amplifier is less preferable than CE. CE's emitter can be simply grounded, while for CE, all three terminals must be carefully designed and routed. Especially, its base should be well bypassed by big capacitors of C_{b1} and C_{b2}, as shown in Figure 2. This bypass is key for CB amplifier's stability, as inductive impedance at base terminal is equivalent negative impedance at the emitter, causing potential oscillation.

The 1st gain stage is designed based on the same idea. To drive the second stage to its saturated output power $P_{sat,2}$, the 1st stage should ensure that the power at the input of the second gain stage is at least

$$P_{in,2} = P_{out,2} - G_{p,2} = 16dBm - 7dB = 9dBm. \quad (5)$$

Considering the loss of the matching network between the 1st stage and 2nd stage, the maximum output power of the 1st stage should at least be 11dBm. Thus, the load impedance

of the 1st stage $Z_{L,1}$ should be chosen to allow a load line of 11dBm output power. However, the conjugate matching impedance $Z_{L1,conj}$ = 6.8-12.3jΩ that allows maximum power gain automatically satisfies this requirement. Thus, L1, the inductor providing DC collector current path for Q1, C2, the DC block capacitor, and L3, the DC emitter current path for Q2, are tuned to transform the input impedance of Q2 to $Z_{L1,conj}$. When input with 2dBm input signal, Q3 delivers 11dBm at its output, with a power gain of 9dB. It is less than its MAG due to gain compression at its saturated power, which is caused by some soft clipping of its output swing. The overall power budget is shown in Figure 4 below.

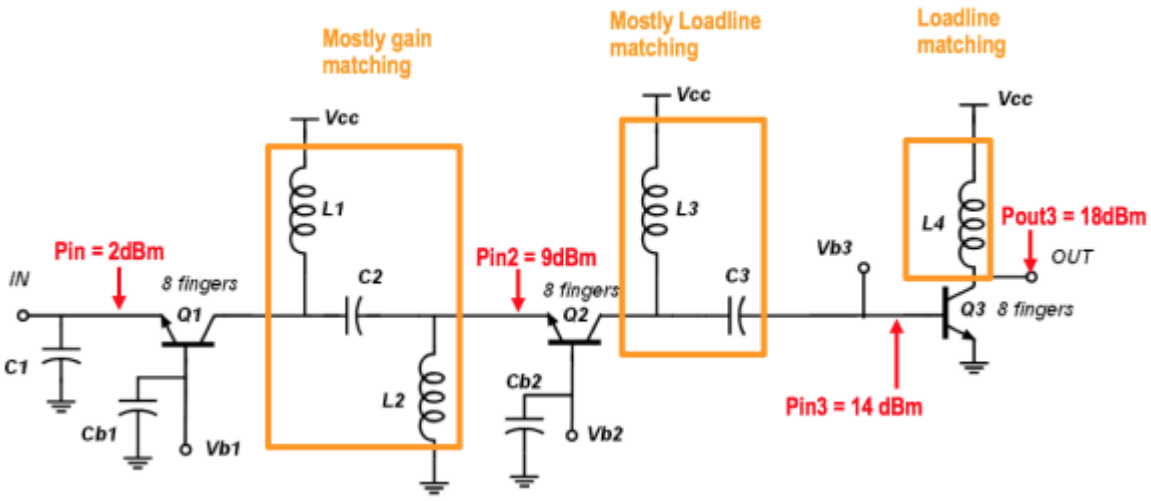

Figure 4. Power Budget Arrangement

IV. SERIES POWER COMBINING WITH 4:1 BALUNS

In [2], Wilkinson power combiners were used to combine output powers from each cell. Due to the quarter-wavelength lines required in it, this type of power combining not only takes a great amount of area, but also causes considerable loss on the signal path. Therefore, this work uses a 3-conductor balun structure, reported in [5], to combine power at the

output. The 4:1 balun structure combines the power cells in series manner. It can transform 50Ω load impedance to 12.5Ω. When designed in double sided, each port presents 25Ω to each power amplifier cell, since the two cells are connected in shunt. As the output balun is double-sided, combining power output from 8 power cell, two input balun is required to split evenly the input power into 8 shares.

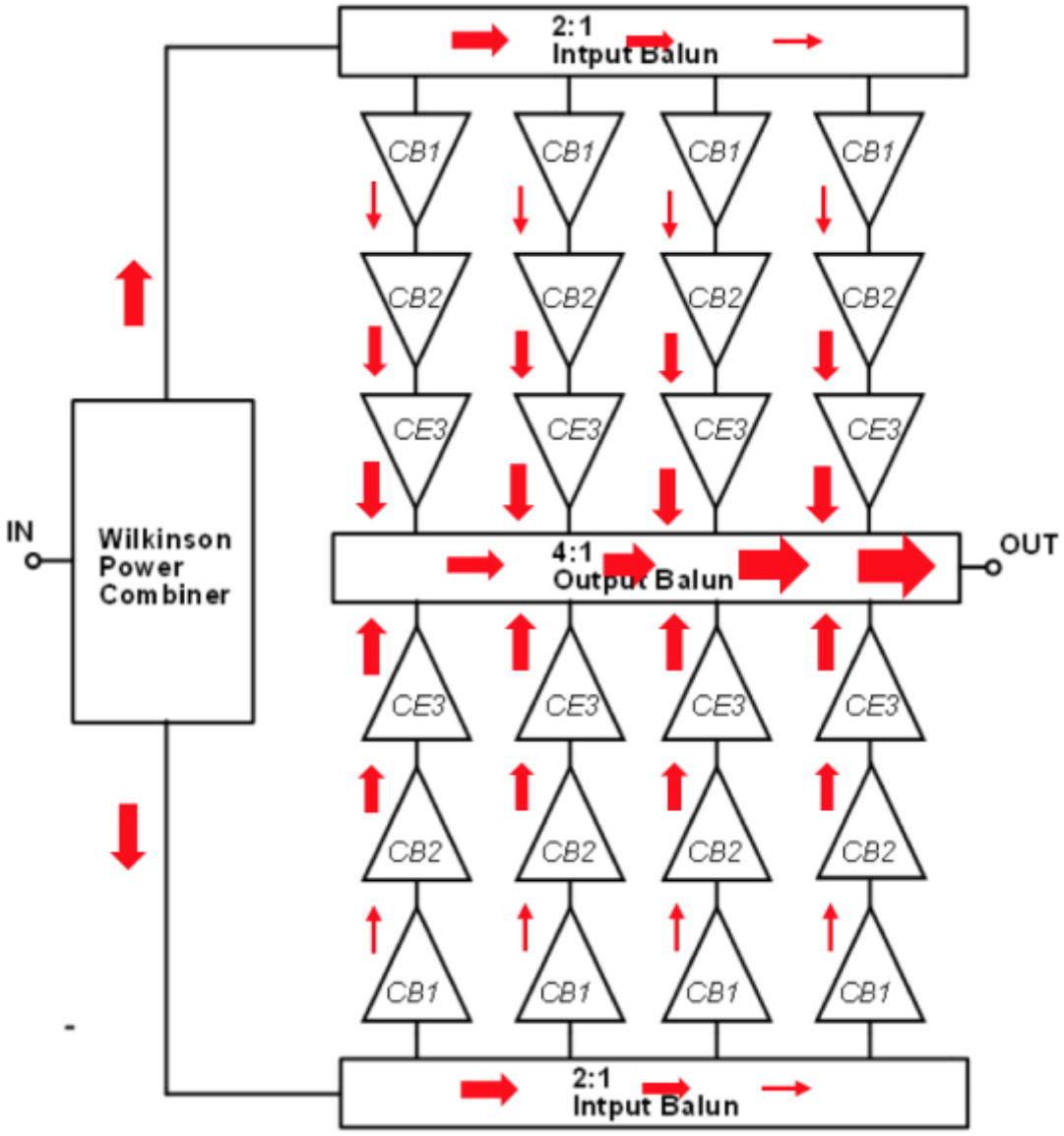

Figure 5. Power Flow Graph in the Power Combining System

Figure 5 shows the power flow to illustrate how power is split and combined.

V. LAYOUT AND SIMULATION RESULTS

Figure 6 shows the overall layout of the design.

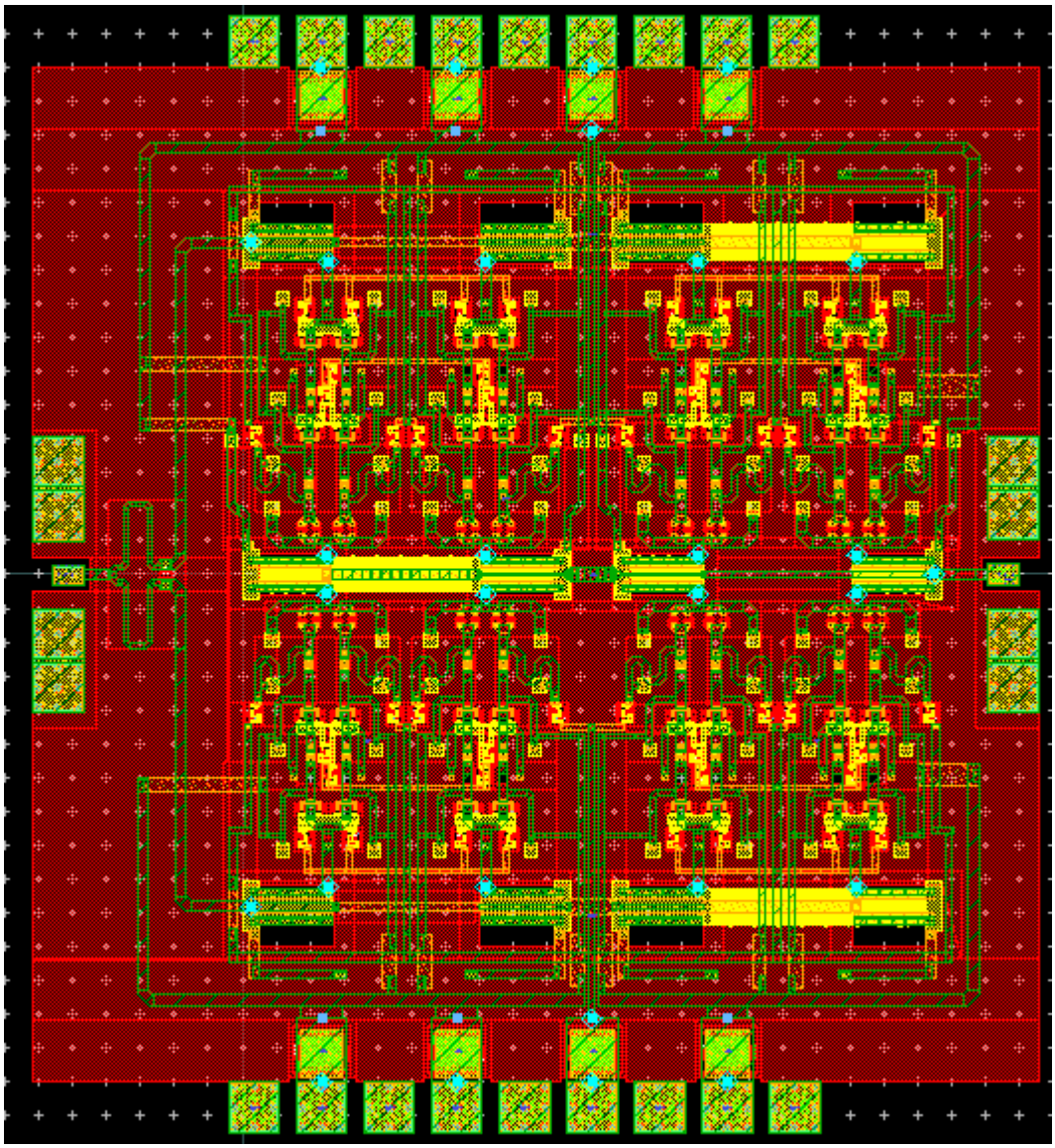

Figure 6. Layout of the Power Amplifier

Figure 7 shows the small signal performance of the power amplifier. At 235GHz, the gain is 20.7dB and the 3-dB bandwidth is 12GHz. The input return loss is below -12dB and the output return loss is below -7dB.

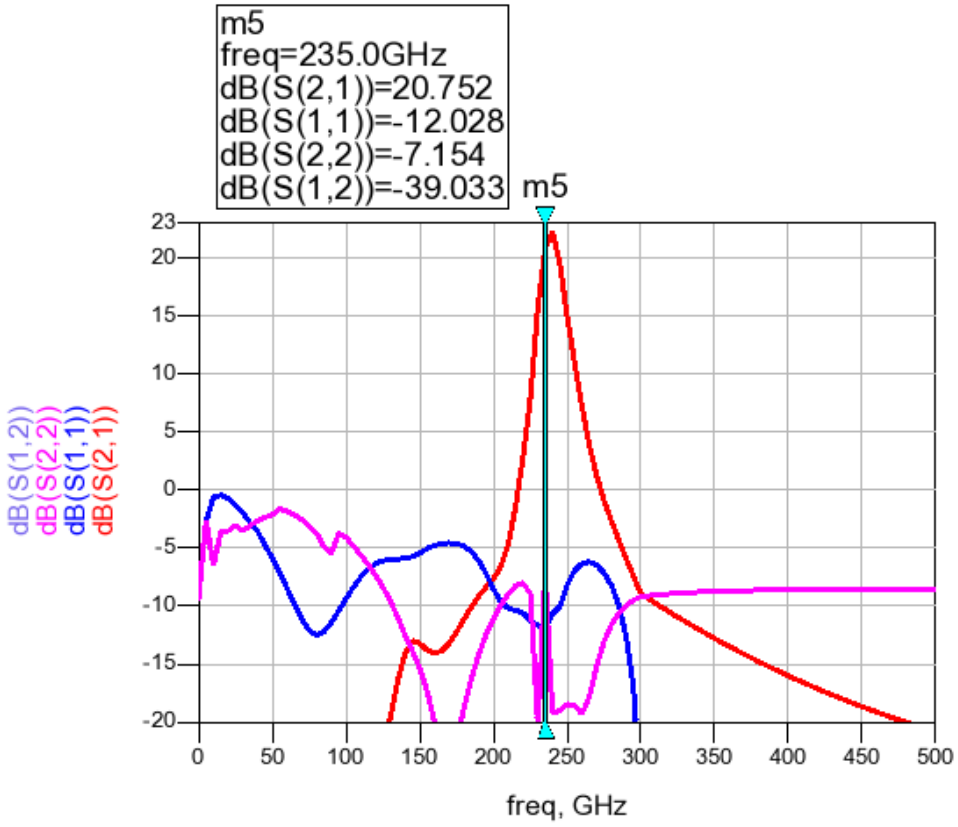

Figure 7. Small Signal Performance of the PA

Figure 8 shows large signal simulation performance of the power amplifier. At saturated output power level of 27dBm, it has a compressed power gain of 14dB and a PAE of 10%. The total DC output power consumed at peak output is 4.8W.

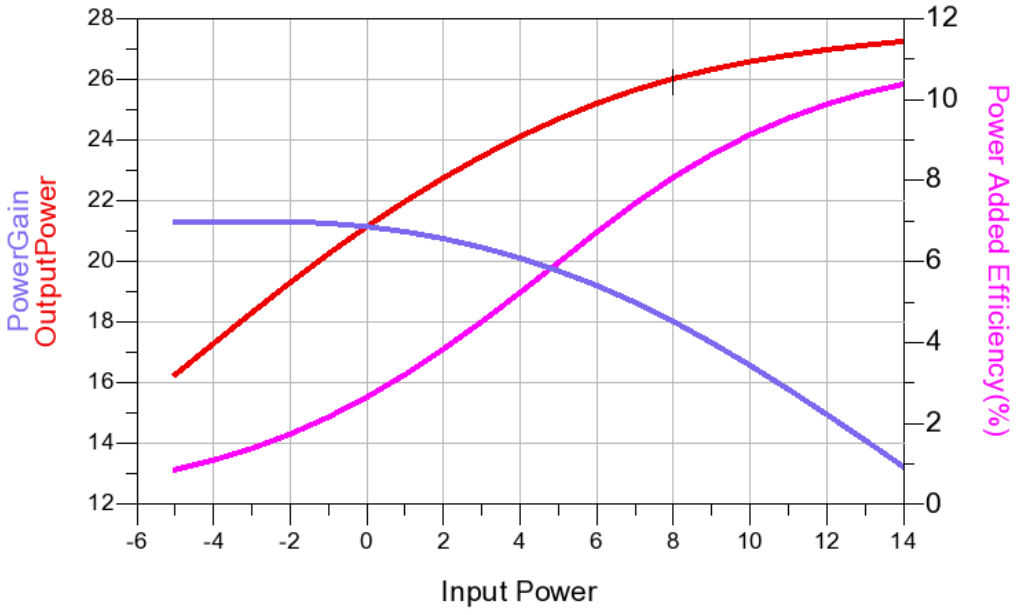

Figure 8. Large Signal Performance of the PA

VI. CONCLUSION

A solid-state power amplifier at 238GHz is designed. It uses cascaded common base stages and common emitter stages to achieve high output power as well as high power gain. 4:1 balun is used to combine the power of 8 power cells. At its saturated output power of 27dBm, it has a compressed power gain of 14dB and power added efficiency of 10%. This design demonstrates the power capacity of InP HBT technology at sub THz frequency.

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