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Physical and Compact Modeling of vertical and lateral tunnel field effect transistors

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Nanoscale Devices and Systems)

by

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2017

The dissertation of Jie Min is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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University of California, San Diego

2017

DEDICATION

To my family, for their continuous support throughout my life

To my past grandfather, Shunxiu Min, for his foresight of the importance of education

To Wenyue, for her care, considerateness and the blessings of meeting her

EPIGRAPH

I used to wander in the sea of electrons

I used to be trapped in the cell of lattice

but now between the bands shall I dance

through the forbidden barrier, quietly tunnel across

—Lyrics of Semiconductor: Tunneling

我曾流浪于电子的海洋

亦曾禁锢于晶格的幽房

而今我将在能带间舞蹈

悄无声息地穿过势垒的高墙

—《半导体中的歌：隧穿》

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doping effect in tunnel FETs with staggered bandgap", *IEEE Electron Dev. Lett.*, vol.36, pp.1094-1096, 2015. The dissertation author was the primary author of the paper. 2. Y. Taur, J. Wu, **J. Min**, "Dimensionality dependence of TFET performance down to 0.1V supply voltage", *IEEE Trans. Electron Dev.*, vol.63, pp.877-880, 2016. 3. J. Wu, **J. Min**, Y. Taur, "An analytic model for heterojunction and homojunction tunnel FETs with 3D density of states", *Device Research Conference*, pp.249-250, 2015. 4. Y. Taur, J. Wu, **J. Min**, "A Short-Channel I-V Model for 2-D MOSFETs", *IEEE Trans. Electron Dev.*, vol.63, no.6, pp.2550-2555, 2016. 5. J. Wu, **J. Min**, Y. Taur, "Short channel effects in tunnel FETs", *IEEE Trans. Electron Dev.*, vol.62, pp.3019-3024, 2015. 6. Y. Taur, J. Wu, **J. Min**, "An analytic model for heterojunction tunnel FETs with exponential barrier", *IEEE Trans. Electron Dev.*, vol. 62, pp. 1399-1404, 2015. The dissertation author was the co-author of the these papers to be included for the congruity of Chapter 2.

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Chapter 5, in full, is a reprint of the publication as it appears in J. Exploratory

Solid-State Computational Devices and Circuits. **J. Min**, P.M.Asbeck, "Compact Modeling of Distributed Effect of 2-dimensional Vertical Tunnel FET and Its impact on DC and RF Performances", *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, vol.3, pp.18-26, 2017. The dissertation author was the primary author of the paper.

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ABSTRACT OF THE DISSERTATION

Physical and Compact Modeling of vertical and lateral tunnel field effect transistors

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With the scaling of MOSFET devices down to the sub-10 nm regime, there has been an active search for novel designs and device physics for lower V_{DD} operation. For MOSFETs, the theoretical limit of 60mV/dec sub-threshold slope has posed a lower limit for V_{th} below which leakage current in OFF-state is undesirably high for digital circuit applications and consequently a limit for supply voltage V_{DD} . What's more, short channel effects such as drain induced barrier lowering (DIBL) has also been a challenge

for every iteration of technology node below 100nm. Tunnel field effect transistor, a design that utilizes band-to-band tunneling (BTBT), becomes a promising candidate because of its capability in achieving sub-60mV/dec, more resistance to short channel effects and less temperature dependent characteristics, especially in OFF-state.

This dissertation focuses on the modeling of tunnel FETs in a variety of aspects, including analytic modeling; temperature dependent factors and physical noise analysis of double gate tunnel FET structures; and compact modeling and physical analysis of vertical tunnel field effect transistors with a distributed circuit model.

In the analytic modeling of double gate TFET work, an analytic tunnel barrier model for TFET is formed by solving a 2D homogeneous Poisson equation. The approximate solution, an exponential function for long channel barrier and a *sinh* function for short channel barrier, is proposed to replace the Kane's tunnel model, which assumes a constant field and homo-junction for tunneling. Tunneling probabilities are thus evaluated analytically for exponential barrier conditions, and current density is integrated numerically. Furthermore, short channel effect, source doping effect, debiasing effect (which details how the carriers accumulated in the channel affect the potential profile in the linear region), and dimensionality dependence (dimension of density of states) are further studied starting from the analytic expressions of tunnel barriers. The model shows much higher computational efficacy than the Sentaurus TCAD simulator and higher accuracy than a simple Kane model.

TFET is also desirable for the weak dependence of BTBT mechanism on temperature. Yet, there are other temperature dependent factors affecting the performance of

TFET such as threshold voltage shift and effective tunnel gap shrinking. In this work, several possible temperature dependent factors that are intrinsic in semiconductors are studied for a double gate TFET, and their effects on V_{th} and tunneling bandgap E_g^{tun} are elaborated. These factors include bandgap shrinkage, temperature dependent Fermi-Dirac distribution in source region (source degeneracy) and temperature dependent effective DOS mass in the channel (which determines quantum confinement). It is found that there are canceling effects between quantum confinement, source degeneracy with bandgap shrinkage in V_{th} calculation as well as tunnelling bandgap calculation. The canceling effects result in a weak dependence on temperature of both threshold voltage (affecting I_{off}) and tunnel bandgap (affecting I_{on}). One can further optimize the temperature dependence and ON-state current by tuning the device thickness. Trap-assisted tunneling (TAT), a temperature dependent extrinsic effect, is further simulated from a more practical standpoint. It is found that the TAT will mostly affect the current leakage floor rather than degrading the sub-threshold slope in a full current range.

Noise model is an essential for many circuit design simulations. To develop a noise model for a TFET involves different noise mechanisms and physics from the case for a MOSFET. In this work, frequency independent noise (white noise) and frequency dependent noise (flicker noise) are considered for a double gate TFET. For white noise calculation, both shot noise at the tunnel junction and thermal noise in the channel are considered for a device with 100nm gate length. Their individual contributions to drain terminal current are calculated using the impedance field method. As for flicker noise calculation, it is found from number and mobility fluctuation models aided by Sentaurus

simulation that the most significant noise contribution originates near the tunnel junction in the saturation region of the $I-V$ curves, and mobility fluctuations become nontrivial in the linear region.

Finally, a novel structure where tunneling happens between two layers in a direction orthogonal to the source-to-drain net current flow direction ("vertical TFET") is studied using a distributed circuit model. Both vertical tunneling and lateral drift-diffusion model are considered in the overall calculation and the competitions between these two mechanisms are shown. A shorter gate length increases the conductivity in the lateral direction, but decreases the conductivity in the vertical direction. Therefore, there exists an optimized gate length for DC ON-current density. However, in terms of RF performance, it is found that shrinking the gate length boosts the cut-off frequency and the speed of transistors because of a major reduction in capacitance with little accompanying decrease of transconductance. Finally, parasitic elements are considered for more realistic RF modeling.

Chapter 1

Introduction

This chapter first presents an overview of design concerns for modern MOSFET technologies, along with their current status and future projections according to the ITRS roadmap. Several important challenges in the future development of MOSFETs are highlighted, including the non-scalability of threshold voltage. Thereafter, several candidates for transistors with sharp sub-threshold current variation with gate voltage (STEEP transistors) to address the power-delay dilemma of conventional MOSFETs at low power operation are introduced, particularly concentrating on tunneling field effect transistors (TFETs). In the following section, the working principles, history and a variety of designs for TFET are browsed through. A review on modeling of TFETs is then presented. The advantages and disadvantages of different types of modeling are listed. The objectives, scope and organization of the thesis are addressed in the last section.

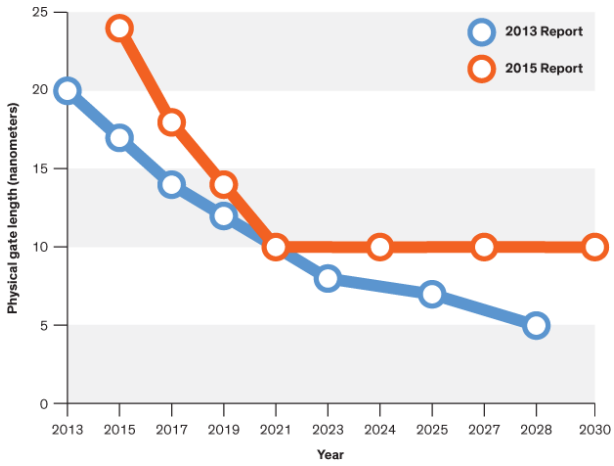

Figure 1.1: Projection of gate length in the near future extracted from 2015 ITRS report (orange circle) and 2013 ITRS report (Blue circle) [1]. 2015 ITRS report predicts the feature size going flat to 10nm on the year of 2021.

1.1 MOSFET Design consideration and limitations

Ever since the invention of MOSFET and CMOS technology, computing power has been expanding at a staggering speed over the past 50 years thanks to CMOS low leakage current and extremely high density of components after scaling. Moore's law (predicted by Gordon Moore in 1965 [2]), initially described a doubling every year in the number of components per integrated circuits. The number was later modified to 18 months as the transistors becomes more and more scaled, and the gate length was projected to hit the floor in 2021 by the prediction of International Technology Roadmap for Semiconductors (ITRS) in 2015 as illustrated in Fig. 1.1 [1]. Such a projection is based on both the increase in OFF-leakage current and in drastic marginal cost in shrinking even 1 nm further. However, the end of shrinking in size does not necessarily mean the doomsday for Moore's law. In fact, with the boost in the power of computation, artificial intelligence (AI) and machine learning become possible at a low cost. Parallel

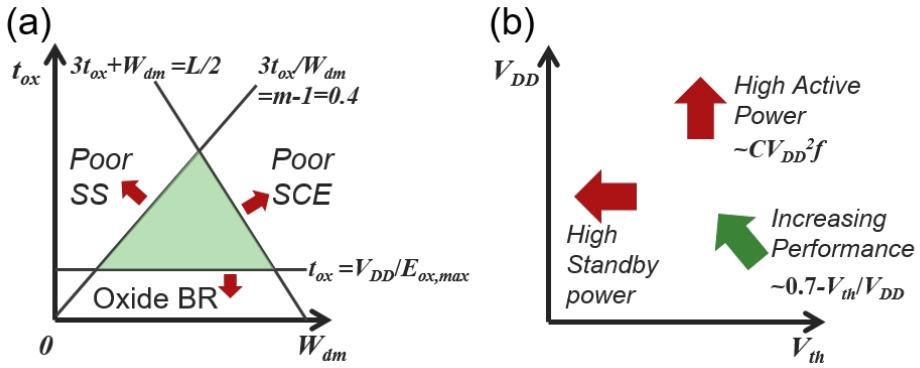

Figure 1.2: Design spaces for (a) $t_{ox} - W_{dm}$ design plane for a single MOSFET: the green region indicates the desired design space for MOSFET with reasonable subthreshold slope, short channel effect and no oxide breakdown in operation, and (b) $V_{dd} - V_t$ design plane for CMOS performance: the trade-off between power and delay are illustrated in terms of V_{dd} and V_{th}.

computation is more preferable compared to serial computation in those applications. Companies such as Nvidia (Volta, GPU) [3] and Google (Tensor Processing Unit, TPU) [4] are diving into new architectures suited for artificial intelligence. However, with more simultaneously active components on the chip for parallel computation, active power (proportional to $CV_{dd}f^2$ per CMOS component) would be a vital concern in those chips. Due to the higher density of power dissipation, self-heating effects will degrade the performance of transistors in mobility, threshold voltage, etc, thus diminish the design margin for circuit designers and device physicists. A lower operation voltage, V_{dd}, can reduce the power consumption, yet at the cost of longer delay time. What's more, lower V_{dd} also indicates more vulnerability to noise, and less integrity in computation.

To have a better picture of MOSFET design concerns, two design-spaces are frequently quoted as illustrated in Fig.1.2 [5]. In Fig.1.2(a), oxide thickness(t_{ox}) and maximum depletion width (W_{dm}), two dimensions of the device, are considered for

MOSFET design. They will affect the sub-threshold swing (SS), short-channel effects (SCE) and oxide breakdown indicated by three straight lines in the space. Poor SS will result in less gate control and higher threshold voltage, while poor SCE will exacerbate the DIBL effect, with higher leakage current. Over the years of developments, metal gate, high-k dielectrics, FinFET structures and even nano-sheet structures fabricated recently by IBM [6] have been adopted to address these issues simultaneously.

In Fig.1.2(b), V_{dd} and V_{th} are used to measure the performance (delay) and power (leakage current). The OFF-state current (at $V_g = 0V$) is lower at higher V_{th}, while the performance degrades for this case because of lower I_{on} and therefore longer delay, and vice versa. Because the leakage current for MOSFET is governed by thermal statistics, there exists a theoretical limit for current on-set ($60mV/dec$ for T=300K). This sets a lower limit for threshold voltage, V_{th}, and thence for applied voltage, $V_{dd} > 4V_{th}$to guarantee a high performance CMOS. STEEP sub-threshold transistors, whose sub-threshold slope could show beyond-60mV/dec characteristics, are potential candidates to push the threshold voltage even lower, guaranteeing a lower leakage current and high ON current at lower V_{dd}.

1.2 MOSFET versus Tunnel FET

There are two steep sub-threshold device candidates: one is called Negative-capacitance FET [7], where a layer of ferroelectric material is deposited on top of a high-k dielectric, utilizing the ferroelectric polarization to achieve steep subthreshold

slope; the other is called tunneling FET [8], where band-to-band tunneling occurs in the device. This thesis focuses on the tunneling field effect transistors.

A comparison of configurations between MOSFET and TFET is first shown in Fig. 1.3, both assuming double gate structures and n-type FET. The first observable distinction for TFET is its asymmetric doping type at source and drain. For n-type TFET, a heavily doped p-type source is needed for optimized source barrier [9], while for n-type MOSFET, heavily doped n-type source is needed for lower electron barriers and small source resistance. A second distinction for TFET is its heterostructure at source/channel junction. Although tunneling could still happen for homojunctions, it will suffer either from low ON-state current when the band gap is as high as 1.1eV as for for silicon; or from high OFF-state current when the band gap is low. Additionally, homojunction TFET cannot turn on abruptly. Heterojunctions, on the other hand, allow engineering of bandgap in different regions for optimized I_{on}/I_{off} trade-off. GaSb/InAs heterojunction as illustrated in Fig. 1.3(b) has a staggered bandgap that could provide high ON current while maintain a low leakage current level.

Comparisons of band diagrams in ON-state and OFF state between a TFET and a MOSFET are illustrated in Fig.1.4. As can be seen in Fig.1.4(a), the leakage in subthreshold region for MOSFET mainly comes from the electrons above the barrier near source, which follows Maxwell-Boltzmann's distribution when the barrier is high enough compared to kT. Therefore, $I_{SS} \propto exp(qV_{gs}/mkT)$, where ideality factor $m = (C_{ox}+C_{dm})/C_{ox}$. On the other hand, tunneling transistors can block the leakage current from thermal excitation by forbidden band gap in OFF-state, as illustrated in Fig.1.4(b),

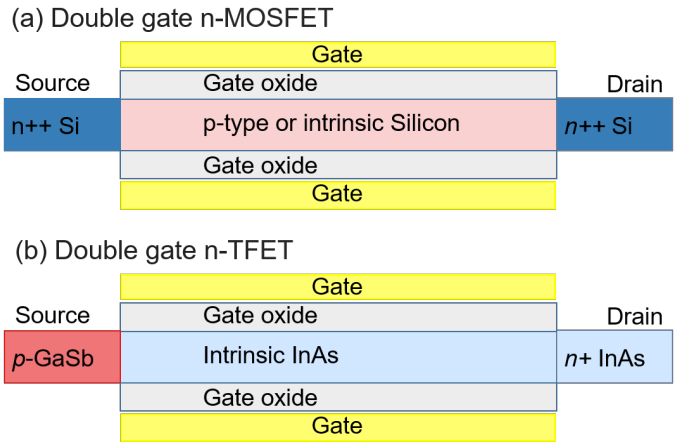

Figure 1.3: Structures, doping profile and materials for (a) double gate n-MOSFET, and (b) double gate n-TFET.

resulting in a much steeper turn-on and thus lower V_{th} without compromising the leakage current.

In ON-state, electrons in the source will be thermally-excited to overcome the barrier and conduct current for MOSFETs, while for TFETs, band-to-band tunneling from source to channel occurs when positive gate bias opens the tunnel window. Because of the limited tunneling probability, the ON-state current at high V_{gs} is not as good as MOSFET current. Nevertheless, designed for low power application, TFET could still outperform MOSFET in current density when V_{dd} is low, as sketched in Fig.1.5.

1.3 Review of Proposed TFET Designs

Tunneling in semiconductors has been studied and practiced since the dawn of the technology. E.O Kane proposed the theory of tunneling in 1961[10], where direct and phonon-assisted tunneling are reviewed with a constant E-field assumption. The model

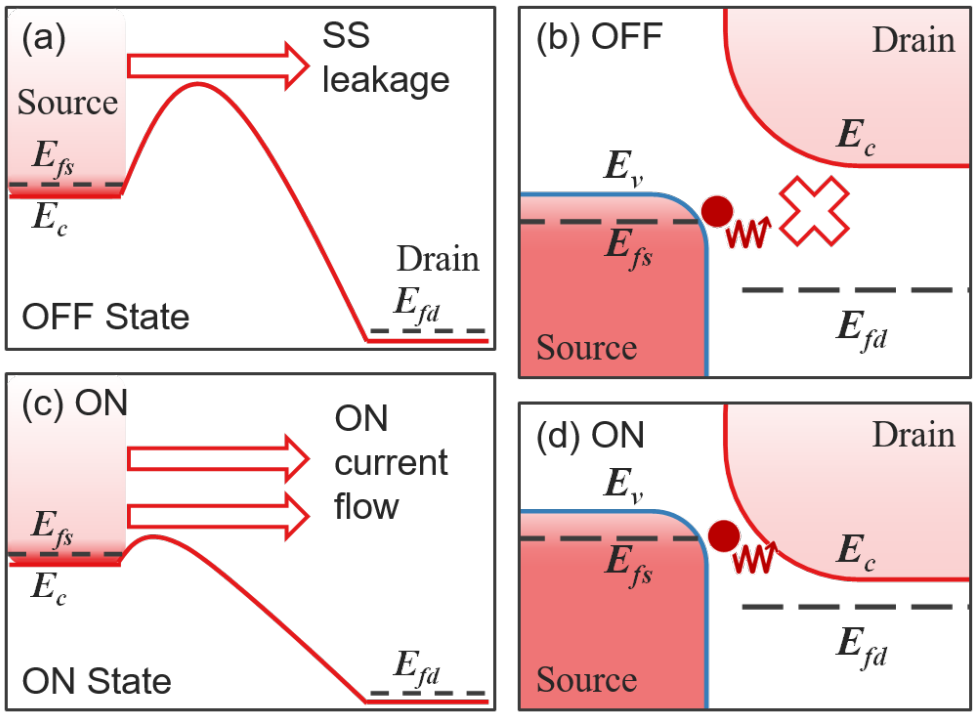

Figure 1.4: Comparisons of band diagrams between TFET and MOSFET: Comparison in OFF state for (a) MOSFET and (b) TFET, indicating a leakage current induced by thermal excitation in MOSFET, while blockage of leakage current from forbidden bandgap in TFET; comparison in ON state for (c) MOSFET and (d) TFET, showing less barrier for MOSFET compared to TFET case.

succeeded in describing a heavily doped p-n diode. Tunneling has seen practical use as Zener diodes and Esaki diodes over the years as well.

A gate controlled tunnel diode, namely a tunnel FET, did not capture the attention of the device community until 2004, when the first TFET made of a carbon nanotube with sub-60mV/dec subthreshold slope was reported by IBM [11]. This may be due to the immature oxide and lattice growth technologies that did not produce high quality interface and thus induce much more leakage current outweighing the advantage of low BTBT leakage. It still turns out to be an important issue for TFET designs today when most designs are dealing with III-V materials. Another possible reason is its

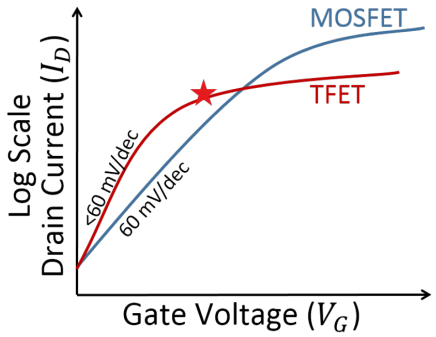

Figure 1.5: Comparisons of $I_{ds} - V_{gs}$ curves for MOSFET (blue line) and TFET (red line). The red star indicates the desired operating bias point for TFET where MOSFET is still in SS. Same off-state current is assumed at $V_{gs} = 0V$ for both devices.

limited ON-state current compared to MOSFET at high V_{DD}, making it less attractive in terms of performance. The incessant scaling of device size and the non-scalability of threshold voltage V_{th} for MOSFET in recent years have urged the engineers to search for alternatives. The quest for TFET commenced under such circumstances. There are several designs proposed by a number of groups, which will be listed and described in more detail in the following paragraphs.

1.3.1 Carbon Nanotube TFET

The first TFET with sub-60mV/dec subthreshold slope was reported in 2004 by IBM [11]. However, the observed slope only occurs at extremely low current density (below 1pA) and the ON-state current is also too low for practical usage.

1.3.2 Si/SiGe based TFET

Silicon technology has become quite mature because of the long-lasting development in CMOS technology. Therefore, fabricating TFET using Silicon and SiGe materials could take full advantage of the mature processing technology and good dielectric/semiconductor interface. It also has better compatibility between TFET and conventional MOSFET devices.

For instance, source-pocket design for Si Tunnel FET is demonstrated for an improvement in SS and an excellent I_{ON}/I_{OFF} ratio[12]. A subthreshold slope of 46mV/dec is observed at $1pA/\mu m$. Strain, which was used to improve the mobility of MOSFET, also proves to be potentially useful for improvement in TFET performance with regard to both I_{on} and I_{off} [13]. Silicon on insulator structure (SOI) has also been demonstrated as the CMOS-compatible technology that allow fabrication of TFET with SS less than 60mV/dec [14].

However, the ON-state current has always been a bottleneck for Si-based TFET. Researchers have proposed Si/SiGe heterostructures to improve the current density and maintain steep subthreshold slope supported by simulation [15]. In [16], the device physics and guiding principles were detailed to design double gate TFET with silicon-germanium source heterojunctions. Experimental results of SiGe nanowire TFET have also been reported [17], where ON current improved by over 10 times and OFF-current decreased by over 3 orders of magnitude. It is also interesting to notice that they conducted pulsed I-V measurement as well to reduce the degradation from charging traps

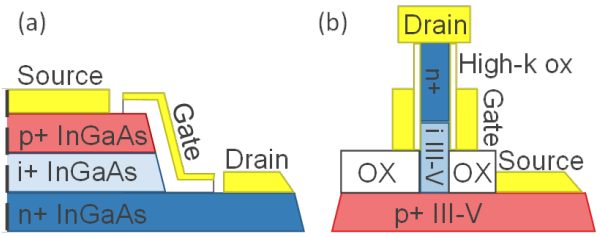

Figure 1.6: III-V TFET structures with (a) Epi-growth channel, and (b) Nanowire structure

and TAT, and observe sub-60mV/dec slope for 10 μs pulse width, while a higher SS is observed for 100 μs width. The on state current density is up to $64\mu A/\mu m$.

1.3.3 III-V based TFET

III-V materials based TFET will provide a much better ON-current and steeper turn-on than Silicon based TFET through bandgap engineering. In general, one could choose different materials for source, channel and drain such that at source junction, the effective band gap is much smaller for a boost in ON-current, while a wider band gap at drain junction to suppress the leakage current. Some of the popular TFET structures have been shown in Fig.1.6.

In Fig.1.6(a), the device is fabricated by first epi-growth of channel, and source, patterning and etching down to the drain region, and depositing Al_2O_3 oxide to cover the side-walls. The side-walls are acting as the tunnel junction. Both [18] and [19] have adopted such structures and achieve a reasonably high ON-current around or greater than $10\mu A/\mu m$. Such structure has the disadvantage of large device diameters limited by lithography. Large diameter limits the gate efficiency and effective tunneling region,

leaving the area in the middle insensitive to gate control as well as one leakage path in OFF-state. Besides, the active regions of tunneling are sidewalls, which possess large number of traps that degrades subthreshold slope greatly.

Another structure is nanowire structure as shown in Fig.1.6(b). There are several advantages of nanowire structure: 1. The nanowire diameter could be scaled down to tens of nanometers, or even down to several nanometers, providing efficient gate control over the channel. 2. The active tunneling region is distributed in the cross-section or even centered in the case of quantum confinement, and the performance is less degraded by the sidewall defects. In [20], InAs nanowires were grown on p-type silicon substrate, forming a Si/InAs heterostructure TFET. A subthreshold swing of 21mV/dec up to 10 $nA/\mu m$, and an ON-current of 1 $\mu A/\mu m$ were achieved. In a most recent study, InAs/InGaAsSb/GaSb nanowire TFET was fabricated and a subthreshold slope of 55 mV/dec was achieved for 1 nA and an ON state current of 0.1 μA per nanowire [21]. Nanowire diameter was down to 20 nm.

1.3.4 Bilayer tunnel FET

Nanowire TFET has the advantage of good gate control, however, the ON-state current density is limited by small diameter, and cannot be scaled by nanowire area. Bilayer tunnel FET, on the other hand, allows a better gate control while the current density is scalable with respect to device area. The features of bilayer TFET are the orthogonality of tunneling direction to gate terminal and two layers acting as source and drain respectively. The structure is sketched in Fig.1.7.

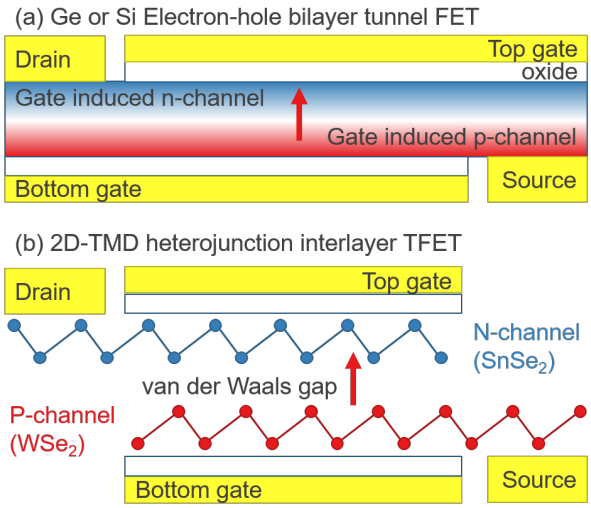

Figure 1.7: Bi-layer TFET structures: (a) Ge or Silicon homojunction electron-hole bilayer TFET and (b) 2D-TMD material based interlayer TFET (Thin-TFET)

Bilayer TFET was first proposed with Si/Ge homojunction designs in [22] and is depicted in Fig.1.7(a). Electron and hole carrier layers that act as source and drain are induced in the same chunk of semiconductor by top and bottom gate. The simulation indicates a nearly ideal SS of 10 mV/dec over 7 orders of magnitude (without considering traps), and I_{ON} of 11 $\mu A/\mu m$ for Ge bilayer TFET, 10 times greater than Ge double gate TFET designs. A number of following simulation studies has been made for this structure such as hetero-gate design [23] and counter doping [24].

With their atomistic level thickness, 2D-TMD materials have also been promising for bilayer TFET structures. Heterojunction can be formed between two layers with a van der Waals gap (assuming around 4$\AA$) between the two layers, as illustrated in Fig.1.7(b). In [25], an average SS of 14 mV/dec is estimated and an ON-current of 300 $\mu A/\mu m$ is projected. The performance, however, is greatly affected by lattice mismatch, rotational asymmetry and mis-alignment, which poses multiple challenges for fabrication. In 2015,

K. Banerjee et. al have demonstrated a bilayer p-type TFET with p-type germanium as the drain and MoS_2 as the source [26]. The ON-state current was probed 10 μA with a tunneling area of 5.1 μm by 15 μm. Sub-60mV/dec slope was observed below 1 nA.

As the first 2D material ever fabricated, graphene has shown some distinct characteristics from conventional semiconductors such as zero bandgap. When a hexagonal boron nitride (h-BN) is sandwiched by two layers of graphene to form a bilayer TFET, negative differential resistance (NDR) is observed because of tunneling resonance [27]. It has been shown the possibility of achieving one-transistor latch or SRAM operation by making use of the NDR effect.

1.3.5 GaN-based TFET

Due to its wide bandgap, GaN is usually considered not an appropriate material for TFET applications. However, in [28], researchers proposed to use a layer of InN as tunneling layer and took full advantage of the intrinsic polarization effect at GaN/InN interface to generate a high electric field. The current density for in-line geometry was over 30 $\mu A/\mu m$, and could be further improved by 2 times with a graded p-InGaN near the tunnel junction. The SS was estimated to be about 15 mV/dec.

1.4 Review of Modeling methodologies

Computer aided simulation has always been a low-cost tool to examine the prototype designs and optimize parameters for device performance in semiconductor

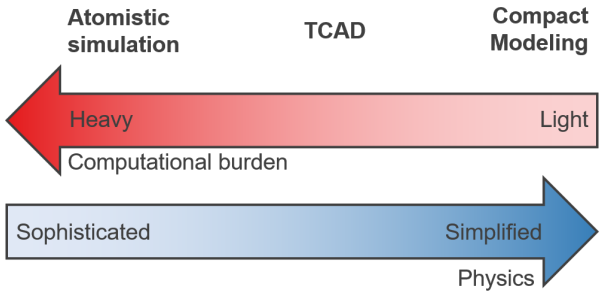

Figure 1.8: Three different types of modeling methodologies: Atomistic simulation, TCAD and compact modeling, and their pros and cons indicated by two arrows: The upper arrow indicating the computational burden and the lower one indicating physics details.

industry. Modeling for tunneling transistors helps device physicists and engineers to understand better the intrinsic performance of a certain design and study the possible sources of degradation. There are three main types of modeling methodologies as illustrated in Fig.1.8, where their advantages and disadvantages are also indicated. A detailed review for each type of simulation will be listed respectively.

1.4.1 Atomistic simulation

Atomistic simulation of TFET usually solves the atomistic full-band tight-binding band calculation. The quantum tunneling is then simulated by using non-equilibrium Green's function method (NEGF). Atomistic simulation is accurate and sophisticated in physics such as phonon scattering and surface roughness scattering. It usually acts as a validation tool for both TCAD simulation and compact modeling [29]. Such simulation usually involves elongated simulation time and requires heavier computational power for the machines. Therefore, it is not suitable to examine the validity of ideas quickly.

There are several toolkits that has been developed by a number of groups, such as OMEN and NEMO3D simulator developed by Klimeck's group etc [30].

1.4.2 TCAD simulations

TCAD simulation is a more efficient way to get physical sensible results compared with atomistic simulation. It also requires less computing power for computers. There are a number of commercialized device physics numerical simulators such as Sentaurus [31] and Silvaco [32] that are widely adopted in designing TFETs and optimizing their performances. Its disadvantages are in the simplification of quantum mechanical calculation and emerge as device size scales to several nanometers. Most of the time, the parameters related to quantum mechanical calculation and nanoscale transport in TCAD are fitted by atomistic simulations. Tunneling characteristics are modeled in TCAD by either local model or non-local model. In local model, electric fields within the tunnel window are extracted first. Then band-to-band generation rate at each point in the tunnel window is calculated by inserting local electric field into Schenk model or Hurkx model. The method works fine in low-field homo-junction conditions, but is inaccurate when tunneling occurs at abrupt junctions with high fields [31]. Under such circumstances, non-local model is more appropriate, which is especially the case for heterostructure tunnel FET simulation. Non-local model will evaluate the barriers profiles and resulted WKB integrals for all tunnel paths within the tunnel window. Then band-to-band tunneling rates are evaluated for each path before they are summed up to render total tunneling current.

Several novel TFET designs have been proposed aided by TCAD simulations, which includes bilayer tunneling FET [22], GaN tunnel FET [28], nanowire TFET etc.

1.4.3 Compact modeling for circuit simulations

Compact modeling usually deals with highest level of simplification and obscuring most physical insights of the device. It is however the most efficient one that is suitable for circuit simulations. Therefore, it is mostly used to reveal potentials in circuit applications and build prototype circuits.

There are a variety of compact models with varying complexities in physics and levels of generalization. Notre Dame semi-empirical model is a semi-empirical model that could be fitted to various types of TFETs, ranging from bilayer TFET[33], III-V TFET [34] to GaN TFET[35]. However, its generalized tunneling expression also leaves most parameters as purely fitting parameters with little or inaccurate physical sense. On the other hand, [36], [29] and [37] proposed models describing double-gate TFET specifically. Potential profiles are first solved and WKB integrals are evaluated analytically with assumptions and approximations.

1.5 Thesis Objectives and Organizations

The objective of this thesis is to develop efficient methodologies and tools for tunnel FETs that are applicable for circuit modeling but still preserve insights of physics. TCAD and compact modeling (using MATLAB, Verilog and ADS (Advanced Design

System fom Keysight) are the crucial tools used throughout the thesis.

The TFET structures studied in this thesis are double-gate heterojunction TFETs (DG-HTFET) and bilayer vertical tunneling TFETs. The first structure is similar to a double-gate MOSFET, and can be readily extended to the nanowire TFET case. Both structures are compatible with modern semiconductor fabrication processes. To build a model that is suitable for benchmarking and efficient comparison with MOSFET technologies, one needs to study not only the DC current characteristics, but also noise performance and temperature dependence to derive reference figures of merit for circuit designers. Bilayer vertical tunnel FETs, on the other hand, show conduction mechanisms significantly different from those of a double gate structure. These bilayer TFETs have the advantage of improving current density per device by increasing device area, without losing the gate control efficiency. However, the lateral conduction can degrade the performance by acting as a distributed FET (and therefore causing extra resistance) for the whole device. A scaling rule with physical insights similar to those of MOSFET scaling would be appropriate as the guidelines for circuit designs implementing such TFETs.

In the thesis, the starting point is the study of current density calculation for double gate TFETs based on analytic potential and WKB expressions. The potential profile analytically derived from Poisson's equation is inserted into the WKB calculation for varying energy levels. The model has a closer relation to the physical structure compared to a simple Kane's model, where constant E-field is assumed, while it is much more efficient than the extensive TCAD simulations. A variety of physic mechanisms are

taken into consideration including short channel effect (SCE), de-biasing effect, source doping etc. after the fundamental simplified tunneling model is built up. The temperature dependence of the double gate TFET is then studied based on the model developed. Band-to-band tunneling itself has little temperature dependence, which is an advantage over the sub-threshold leakage current for MOSFETs. Under such circumstances, temperature dependence of bandgap, Fermi-Dirac distributions and density of states become the dominating factors for the TFET. There are also extrinsic effects that are strongly temperature dependent, such as trap-assisted tunneling (TAT), which is also discussed aided by TCAD simulation. Noise simulation for double-gate TFET will be detailed in the third chapter. Frequency independent noise (white noise) and frequency dependent noise (flicker noise and random telegraph noise) are analyzed separately. For white noise, both shot noise from band-to-band tunneling and thermal noise from drift-diffusion are considered and the impedance field method is used to evaluate the total noise. For frequency dependent noise, flicker noise is mainly studied, but the same method can be applied to random telegraph noise as well. As in the MOSFET noise model, carrier number fluctuations due to trapping/de-trapping and mobility fluctuation during carrier accumulation are both considered based on the data extracted from TCAD simulation. Noise spectral current densities are evaluated and compared with the MOSFET case. Finally, the distributed effect of bilayer vertical tunnel FETs is studied. Current flow entails vertical tunneling and lateral conduction through the drain channel. To study the distributed effect, current and capacitance characteristics are modeled analytically for each current flow component first. The lateral conduction is simplified to a 2D-FET component for drain layer and a

resistor for source layer; the vertical tunneling is simplified to a TFET component. Both are modeled using Verilog-A and simulated in ADS. After the unit cell composed of these elements is built, serially connected unit cells are simulated to evaluate the DC, AC and RF characteristics. Parasitic elements are considered for a more practical estimation on RF performances. Special attention is given to scaling effects in these characteristics as the two different conduction mechanisms compete with each other. Finally, conclusions are drawn and future works related to the thesis study are proposed.

Chapter 2

Analytic DG-TFET modeling

This chapter will introduce a physics based analytic model describing the potential and current characteristics of a double gate tunnel FET (DG-TFET). Fig.2.1 shows a schematic diagram of the double gate TFET. This chapter will introduce the factors that affect the current performance of a double gate tunnel FET through sections starting from the most basic tunnel barriers formed in channel region. Then source doping effect is added to account for a more practical doping set-up. The effect of mobile charges affecting the channel potential in linear region is explained in the third section. It is also known as the de-biasing effect. Finally, current density derivations under different dimensions (1D, 2D and 3D) are elaborated. They are further compared from circuit performance standpoint in this section.

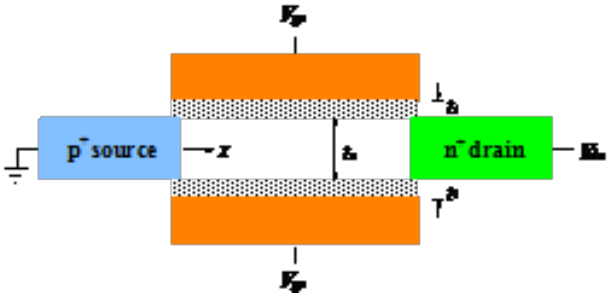

Figure 2.1: A schematic of double-gate TFET.

2.1 Channel Barrier

2-D potential has been solved analytically for a conventional DG as well as NW MOSFETs in the absence of mobile charge [38]–[41]. The solution can be adopted by TFETs with a straightforward change of the source boundary condition from n+ to p+. The assumption of negligible mobile charge is justified when the Fermi level is below the conduction band of channel. The bias condition in which mobile charge has a significant effect on the potential will be addressed later. Focusing on the mathematically simpler DG TFETs, we can express the analytic potential in the semiconductor as a series of eigenfunctions with discrete eigenvalues λ satisfying the equation

$$tan(\frac{\pi t_i}{\lambda})tan(\frac{\pi t_s}{2\lambda}) = \frac{\varepsilon_i}{\varepsilon_s} \tag{2.1}$$

The full 2-D potential is the sum of the long channel term, $V_{gs} - \Delta\phi$, and a series of eigenfunctions with the x dependence,

$$\psi(x) = \frac{b_n sinh(\pi(L-x)/\lambda_n) + c_n sinh(\pi x/\lambda_n)}{sinh(\pi L/\lambda_n)} \tag{2.2}$$

stemming from the source and drain boundary conditions [40]. Here, L is the channel length and $\Delta\phi$ is the gate work function; b_n and c_n are constants expressed in terms of the boundary conditions and the film thickness. Fig.2.2 shows an example of the solutions for two V_{gs} values. The analytic solutions, consisting of four terms of the eigenfunctions (λ_1, λ_3, λ_5, λ_7), are validated by the Sentaurus simulation [42]. Note that a higher V_{gs} causes a thinner barrier as well as a wider tunneling window from the source to the channel.

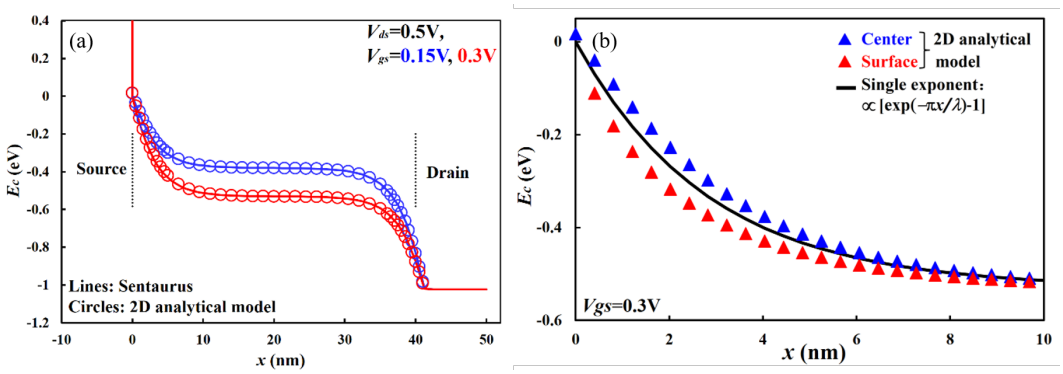

Figure 2.2: (a) Conduction band energy at the center of film for an example of $t_s = 5nm$, $t_i = 2nm$, with $\varepsilon_i = \varepsilon_s$. The conduction band of the source is above the scale due to the band offset of heterojunction. (b) Approximation of the center and surface potential near the source with a single exponential function. The scale length is $\lambda = 9nm$ in this example.

For TFETs biased in saturation, the current is mainly determined by the tunneling barrier near the source. In Fig.2.2(b), we zero in on the potential solution close to the source, where the eigenfunctions are dominated by the term $\propto sinh[\pi(L-x)/\lambda]/sinh[\pi L/\lambda] \approx exp(-\pi x/\lambda)$. Depending on the film thickness, the potential has a slight variation between the surface and the center of the semiconductor. To enable an analytic model for TFET, we approximate both the center and the surface potentials with a single exponential function, $exp(-\pi x/\lambda) - 1$, where $\lambda = t_s + 2t_i$ is the scale length

[43]–[45]. The approximation of uniform potential in the depth direction is more valid for the case of relatively thin t_s and thick t_i. A similar function works for NW TFET as well, with $\lambda = \pi(r_s + t_i)/\alpha$ for the case $\varepsilon_i = \varepsilon_s$, where r_s is the NW radius and $\alpha = 2.405$ is the first zero of the zero-th order Bessel function [41].

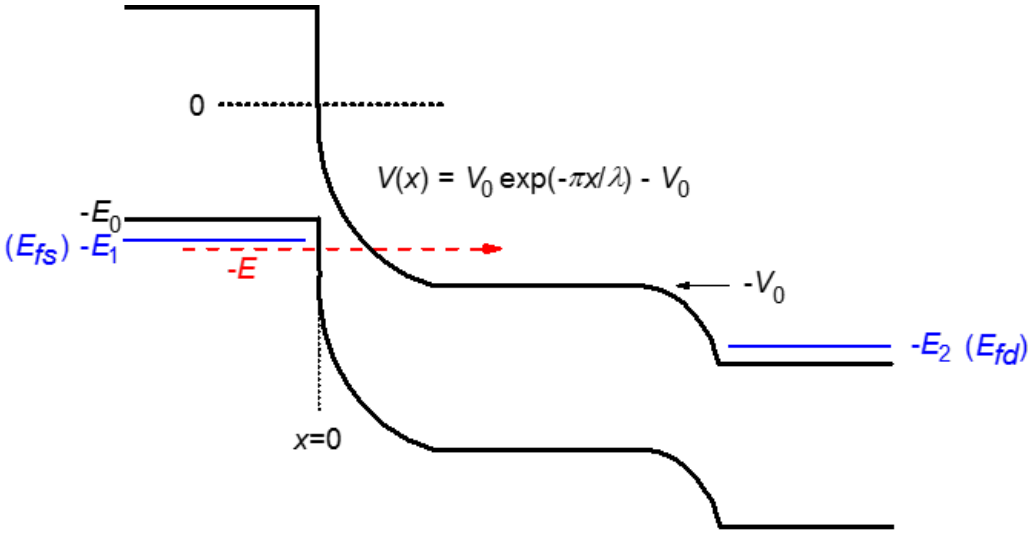

Figure 2.3: Band diagram of a heterojunction TFET biased in saturation.

The band diagram of a staggered heterojunction TFET is shown in Fig.2.3. The zero energy reference is chosen to be the conduction band energy of the channel at the heterojunction boundary. It staggers below the conduction band energy of the source by the band offset. The diagram is for the TFET biased in turn-on and in saturation. Using the single exponent approximation, the potential barrier for electrons tunneling from the valence band of the source to the conduction band of the channel takes the form

$$V(x) = V_0 e^{-\pi x/\lambda} - V_0 \tag{2.3}$$

where V_0 is mainly controlled by the gate voltage. For electrons at energy -E in the valence band, the tunneling probability as given by the WKB integral is

$$\begin{aligned} T(E) &= e^{-\frac{2\sqrt{2m}}{\hbar}\int_0^d \sqrt{V(x)+E}dx} \\ &= e^{-\frac{2\sqrt{2m}}{\hbar}\int_0^d \sqrt{V_0 e^{-\pi x/\lambda}-V_0+E}dx} \end{aligned} \tag{2.4}$$

where $V(d)+E=0$. The integral can be carried out analytically to yield

$$T(E) = e^{-\frac{4\lambda\sqrt{2m}}{\pi\hbar}[\sqrt{E}-\sqrt{V_0-E}\arcsin\sqrt{E/V_0}]} \tag{2.5}$$

For a 1-D ballistic TFET, the current is given by the Landauer equation,

$$\begin{aligned} I_{ds} &= \frac{2q}{h}\int_{E_0}^{V_0}(f_s-f_d)T(E)dE \\ &= \frac{2q}{h}\int_{E_0}^{V_0}[\frac{1}{1+e^{E_1-E/kT}}-\frac{1}{1+e^{E_2-E/kT}}]e^{-\frac{4\lambda\sqrt{2m}}{\pi\hbar}[\sqrt{E}-\sqrt{V_0-E}\arcsin\sqrt{E/V_0}]}dE \end{aligned} \tag{2.6}$$

where E_0, E_1, E_2 are positive quantities defined in figure 2.3. Note that $V_{ds}=(E_2-E_1)/q$. V_{gs} is defined such that $V_{gs}=0V$ corresponds to $V_0=E_0$, i.e., where the tunneling window starts to open up. This definition has the merit that the off condition is maintained at the same V_{gs} for different designs, but it implies a choice of gate work function dependent on the band offset (E_0) and source degeneracy (E_1).

For energies where $f_s-f_d\approx 1$, the current is proportional to the area under T(E) from E_0 to V_0. Fig.2.4 considers an example of $m=0.1m_0$, $\lambda=9nm$ ($t_s=5nm$, $t_i=2nm$, $\varepsilon_i=\varepsilon_s$), and $E_0=0.15eV$ for several values of V_0 ($=qV_{gs}+E_0$). It is clear that as V_0 or

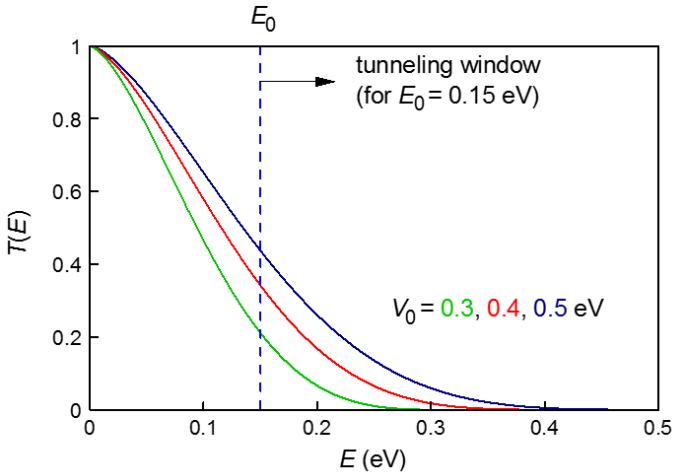

Figure 2.4: Tunneling probability versus carrier energy. The tunneling window is constrained by the density of states to $E_0 < E < V_0$.

V_{gs} increases, most of the current (area) gain comes from thinning of the barrier, rather than from expanding the tunneling window. It is also clear that a smaller E_0 resulting from a larger band offset would significantly raise the tunneling current. Too low an E_0 ($< 0.1eV$) or broken gap ($E_0 < 0$) designs, however, have been reported to result in subthreshold current swing ¿ 60 mV/decade [46].

2.2 Source Doping

In previous section, only channel barrier is considered when evaluating the tunneling probability. In practical applications, source doping and finite density of states will results in band-bending in source region as well. This will introduce another type of barriers in source region.

Fig.2.5 shows the source-channel band diagram of a heterojunction TFET with a staggered bandgap V_1. Both the source and channel bandgaps are assumed to be

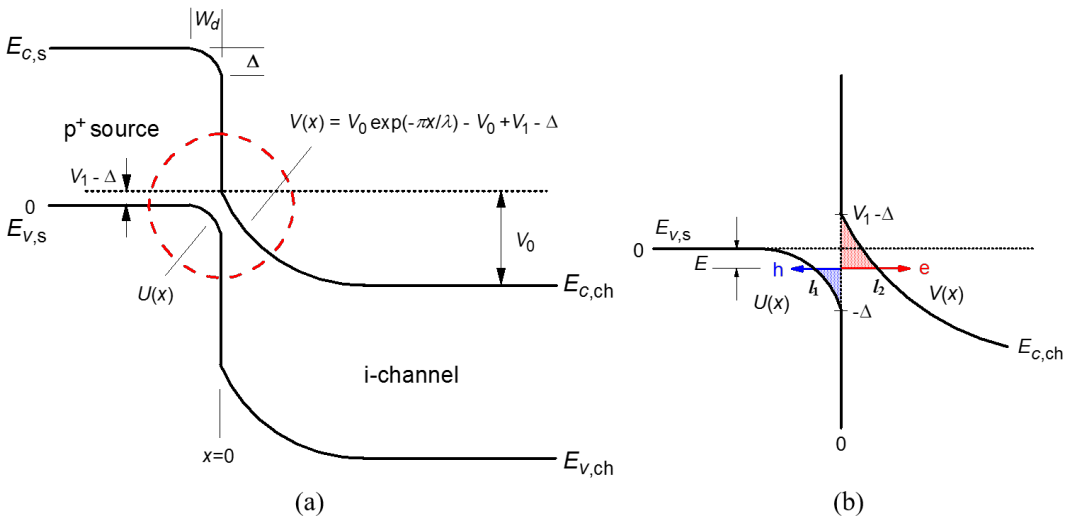

Figure 2.5: (a) Band diagram of turned on TFET. The circled tunneling region is magnified in (b). The shaded areas depict the conduction band and valence band barriers for electron and hole tunneling respectively.

much wider than V_1 that only $E_{v,s}$ and $E_{c,ch}$ are relevant as far as the tunneling current is concerned. The effect of gate voltage goes into $V_0 + \Delta$, the bending of the channel bands and the source bands. The latter extends over a depletion width W_d.

By choosing the valence band edge of source as the zero energy reference, the conduction band of channel is expressed as (note that V is energy in joule):

$$V(x) = V_0 e^{-\pi x/\lambda} - V_0 + V_1 - \Delta \tag{2.7}$$

where x = 0 is at the heterojunction boundary and λ is the scale length solved from 2D Poisson's equation as a function of the physical dimension of the gate insulator and semiconductor and their permittivities. Here we assume that the gate length is over 2λ so the drain effect can be neglected.

By applying the condition that the field is continuous from one side of the

heterojunction to the other (assuming no change of permittivity), we have

$$\frac{1}{q}\left|\frac{dV}{dx}\right|_{x=0} = \frac{\pi V_0}{q\lambda} = \frac{qN_aW_d}{\varepsilon_s} \tag{2.8}$$

where the depletion approximation is employed with source doping N_a. We can then write

$$W_d = \frac{\pi\varepsilon_s V_0}{q^2\lambda N_a} \tag{2.9}$$

and

$$\Delta = q\left(\frac{qN_aW_d}{\varepsilon_s}\right)\frac{W_d}{2} = \frac{\pi^2\varepsilon_s V_0^2}{2q^2\lambda^2 N_a} \tag{2.10}$$

The function describing the bending of the source valence band in Fig.2.5(a) is therefore

$$U(x) = -\frac{q^2N_a}{2\varepsilon_s}(x+W_d)^2 = -\frac{q^2N_a}{2\varepsilon_s}\left[x+\frac{\pi\varepsilon_s V_0}{q^2\lambda N_a}\right]^2 \tag{2.11}$$

Note that the TFET starts to turn on when $V_0+\Delta = V_1$. If we define this condition to be $V_{gs}=0$, then

$$qV_{gs} = V_0+\Delta-V_1 = V_0+\frac{\pi^2\varepsilon_s V_0^2}{2q^2\lambda^2 N_a} - V_1 \tag{2.12}$$

This is valid under saturation, or $V_{ds} > V_{gs}$, where there is negligible mobile charge in the channel and the gate direct modulates the channel potential. For a given V_{gs}, V_0 is solved by the above quadratic equation:

$$V_0 = \frac{q^2\lambda^2 N_a\left[sqrt(1+2\pi^2\varepsilon(V_1+qV_{gs})/(q^2\lambda^2N_a))-1\right]}{\pi^2\varepsilon_s} \tag{2.13}$$

The region of band-to-band tunneling is magnified in Fig.2.5(b). Consider tunneling at an energy -E ($E > 0$) in the valence band of source. For electron energies lying within the staggered bandgap, i.e., $\Delta - V_1 < E < \Delta$, the process consists of hole tunneling (m_h) to the left of the heterojunction and electron tunneling (m_e) to the right of the heterojunction. The total tunneling probability is given by

$$T(E) = e^{-\frac{2sqrt(2)}{\hbar}\left[\sqrt{m_h}\int_{l_1}^{0}\sqrt{-E-U(x)}dx+\sqrt{m_e}\int_{0}^{l_2}\sqrt{V(x)+E}dx\right]} \tag{2.14}$$

where $E + U(l_1) = 0 (l_1 < 0)$, and $E + V(l_2) = 0$. With $V(x)$ of equation 2.3 and $U(x)$ of equation 2.11, both integrals can be carried out analytically:

$$\int_{l_1}^{0}\sqrt{-E-U(x)}dx = \sqrt{\frac{\varepsilon_s}{2q^2N_a}}\left[\sqrt{\Delta(\Delta-E)} - E\ln\left(\sqrt{\frac{\Delta}{E}}+\sqrt{\frac{\Delta-E}{E}}\right)\right] \tag{2.15}$$

and

$$\int_{0}^{l_2}\sqrt{V(x)+E}dx = \frac{2\lambda}{\pi}\left[\sqrt{E+V_1-\Delta} - \sqrt{V_0+\Delta-E-V_1}\arcsin\sqrt{\frac{E+V_1-\Delta}{V_0}}\right] \tag{2.16}$$

For $E > \Delta$, there is only electron tunneling given by equation 2.16. For $E < \Delta - V_1$ (if $\Delta > V_1$), there is only hole tunneling given by equation 2.15. With the bandgap of both the source and the channel much wider than V_1, the two-band effects can be neglected.

With the analytically solved T(E), the current density of a ballistic TFET with 3D density of states is calculated from [47]. (A detailed comparison of 1D, 2D and 3D

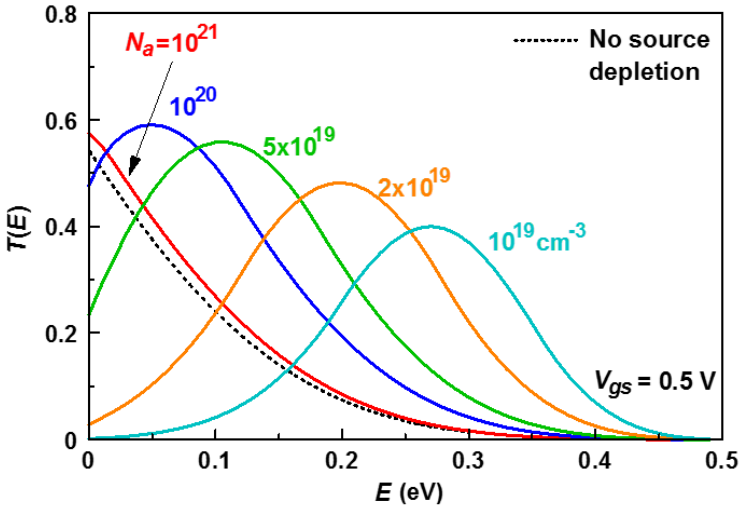

Figure 2.6: Tunneling probability versus energy from the analytic model for a hetero-junction TFET biased at $V_{gs} = 0.5V$. The parameters are $V_1 = 0.15eV$, $m_e = m_h = 0.1m_0$, $\lambda = 9nm$, and $\varepsilon_s = 11.7$

conditions will be demonstrated in section 2.5)

$$j = \frac{qm}{2\pi^2\hbar^3}\int_0^{V_0+\Delta-V_1}(f_s - f_d)\int_0^E T(E,E_\perp)dE_\perp dE \tag{2.17}$$

and f_s, f_d are the source and drain occupation factors with Fermi energies $-d_1$ and $-d_1 - qV_{ds}$, in terms of the source degeneracy d_1 and the drain voltage V_{ds}. The upper limit of integration in equation 2.17 is for the saturation region where the tunneling window is bounded by the channel conduction band.

An example of $T(E)$ (or $T(E,E_\perp = 0)$) is shown in Fig.2.6 for a range of source doping levels. For $N_a = 10^{21}cm^{-3}$ or higher, source depletion is negligible. T(E) is all due to electron tunneling of barrier V_1, the same as that from the no source depletion model described in section 2.1. For N_a between 10^{20} and $10^{20}cm^{-3}$, however, T(E) exhibits a peak at $E > 0$, i.e., at an energy $-E$, below the valence band of source. This is

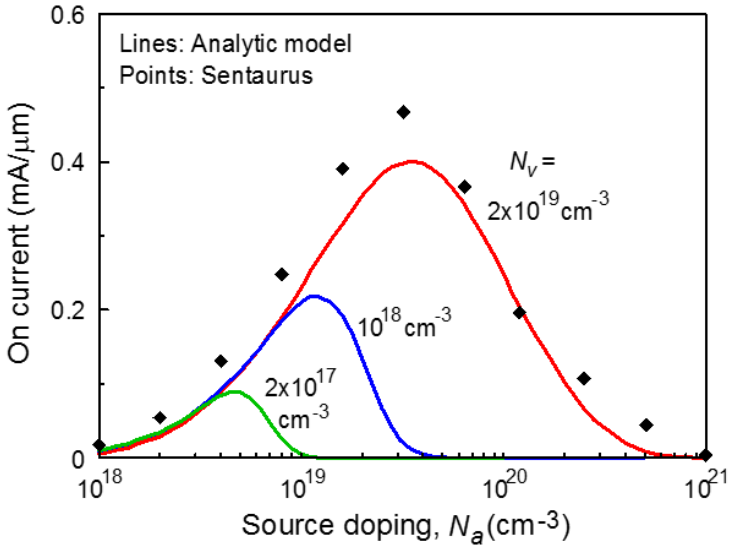

Figure 2.7: On current (at $V_{gs} = V_{ds} = 0.5V$) of heterojunction TFETs versus source doping concentration for three values of N_v (effective density of states). N_v is set to $2 \times 10^19 cm^{-3}$ for the Sentaurus simulation.

because hole tunneling comes into play when the source depletion is significant. As can be seen from Fig.2.5(b), the probability of hole tunneling with respect to the valence band barrier increases with E, in contrary to electron tunneling. The total T(E) therefore first increases then decreases with E. Fig.2.6 also shows that some degree of source depletion can help, as the total area under the T(E) curve for N_a high $10^{19} cm^{-3}$ is significantly larger than that of no depletion.

The effective density of states of the source valence band is fixed at $N_v = 2 \times 10^{19} cm^{-3}$ as N_a is varied. The degeneracy factor d_1 is calculated for each Na using Fermi integrals, namely, from $F_{1/2}(d_1/kT) = (\pi^{1/2}/2)(N_a/N_v)$. By earlier definition, $I_{ds} = 0$ when $V_{gs} = 0$ where $V_0 + \Delta = V_1$. The gate work function is allowed to vary for each N_a to maintain this condition. The current rises up more sharply for lighter source doping with a smaller d_1. The on current at $V_{gs} = 0.5V$, however, is highest at some intermediate

doping between 10^{19} and $10^{20} cm^{-3}$. This is more clearly shown in Fig.2.6 where the on current for $N_v = 2 \times 10^{19} cm^{-3}$ peaks at a source doping of $N_a = 3.5 \times 10^{19} cm^{-3}$. Also shown is the Sentaurus [42] validation of the model result. For materials with lower N_v, the degeneracy factor increases. The peak current decreases and shifts to a lighter N_a.

A different value of V_1 will change the magnitude of peak current as expected, but not the N_a value where the current peaks. If m_h is changed to $10m_e$ with the same m_e ($= 0.1m_0$), the current peak (for $N_v = 2 \times 10^{19} cm^{-3}$) becomes 40% lower and shifts to a higher N_a ($7 \times 10^{19} cm^{-3}$).

2.3 De-biasing

When the TFET is biased in the linear region, E_2 approaches E_1 and $f_d \neq 0$. Moreover, since the Fermi level in the channel is near or above the conduction band edge, there is a de-biasing effect on V_0 due to the channel inversion charge [38], [40]. Instead of $V_0 = E_0 + qV_{gs}$ as in the high V_{ds} case, V_0 is reduced to $E_0 + q(V_{gs} - Q_{inv}/C_{ox})$, where Q_{inv}/C_{ox} is the potential drop across the gate insulator. This is an electrostatic effect unrelated to the transport. For a given $V_{gs} - V_{ds}$, Q_{inv}/C_{ox} can be calculated from a continuous, analytic solution of Poisson's equation with mobile charge for DG MOSFETs [48]:

$$Q_{inv} = \frac{4kT\varepsilon_s}{qt_s}\beta \tan\beta \tag{2.18}$$

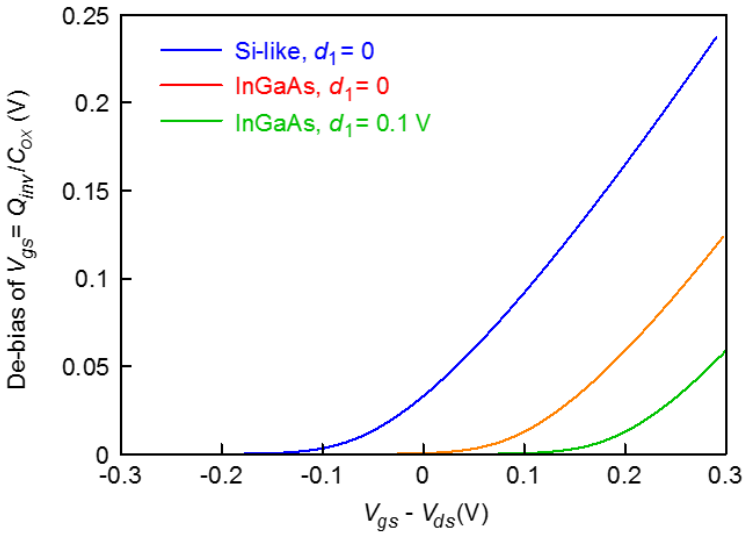

Figure 2.8: Reduction of V_0 in the linear region by Q_{inv} in the channel. $N_c = 3 \times 10^{19} cm^{-3}$ for Si-like, $N_c = 8.7 \times 10^{16} cm^{-3}$ for InGaAs. $\varepsilon_s = \varepsilon_i = 14.6\varepsilon_0$ for all cases.

where the intermediary parameter β is solved from an implicit equation,

$$\frac{q(V_{gs} - V_{ds} - d_1)}{2kT} - \ln\left[\frac{2}{t_s}\sqrt{\frac{2\varepsilon_s kT}{q^2 N_c}}\right] = \ln\beta - \ln\cos\beta + \frac{2\varepsilon_s t_i}{\varepsilon_i t_s}\beta\tan\beta \qquad (2.19)$$

Here, N_c is the effective density of states of the conduction band and d_1 is the source degeneracy. They play a key role on the onset of de-biasing versus V_{ds}, and therefore on the linear region characteristics. Fig.2.8 shows three de-biasing curves, one for silicon-like and two for InGaAs with different source degeneracies. The silicon-like case assumes the N_c of silicon, with everything else the same as the AlGaAsSb/InGaAs heterojunction example considered in section 2.1. Table 2.1 summarizes the device parameters. The high N_c of silicon results in a significant de-bias as soon as V_{ds} is below $V_{gs} + 0.1V$. The de-bias for InGaAs does not start until V_{ds} is below $V_{gs} - 0.05V$ if no source degeneracy, and below $V_{gs} - 0.15V$ if there is a source degeneracy of 0.1 eV.

Table 2.1: Parameters for debiasing and source degeneracy comparison.

	Effective Bandgap, E_0	Electron Effective Mass, m	Effective Density of States, N_c	Source Degeneracy, d_1
Si-like	0.23eV	$0.1m_0$	$3\times10^{19}cm^{-3}$	0
InGaAs	0.23eV	$0.1m_0$	$8.7\times10^{16}cm^{-3}$	0 and 0.1eV

To incorporate the de-bias effect in the generation of continuous $I_{ds}(V_{gs},V_{ds})$ characteristics from equation 2.6, we take an extra step to first calculate Q_{inv} from Equations 2.18 and 2.19 for given V_{gs} and V_{ds}. Then V_0 is set to $E_0+q(V_{gs}-Q_{inv}/C_{ox})$ in the current integral. At a fixed V_{gs}, when V_{ds} becomes high enough, $V_{gs}-V_{ds}$ in Fig.2.8 goes negative and $Q_{inv}\rightarrow 0$. The corresponding I_{ds} makes a smooth transition to the saturation value for that V_{gs}. Fig.2.9(a) shows the model generated $I_{ds}-V_{ds}$ characteristics for InGaAs, $d_1=0.1eV$ with and without de-bias. In the no de-bias case, the only V_{ds} dependent factor in equation 2.6 is f_d. I_{ds} saturates quickly when E_{fd} is approximately 0.15 eV below E_{fs} and the current becomes source injection limited. The effect of de-bias is to reduce the linear region current and push V_{dsat} higher with no impact on I_{dsat}. For the case of InGaAs with $d_1=0$ in Fig.2.9(b), the de-bias effect is more pronounced, resulting in higher V_{dsat}. But the magnitude of I_{dsat} is significantly higher than that of $d_1=0.1eV$. The most severe de-bias happens with the silicon-like TFET in Fig.2.9(c). The high Nc of silicon gives rise to the super-linear $I_{ds}-V_{ds}$ characteristics. These trends are all confirmed qualitatively by Sentaurus simulations, as well as by published hardware data in the literature [49]–[52].

The $I_{ds}-V_{ds}$ characteristics in Fig.2.9 are generated by equation 2.6 of the model with a modification that the low end of the tunneling window is limited by the E_c of the channel or the E_c of the drain, whichever is higher. In other words, the upper bound of

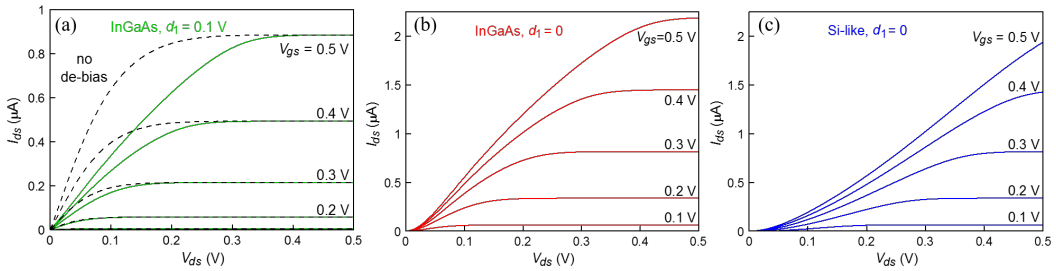

Figure 2.9: Model generated $I_{ds} - V_{ds}$ characteristics for the three de-biasing conditions in Fig.2.8. The dashed curves in (a) are for no de-biasing.

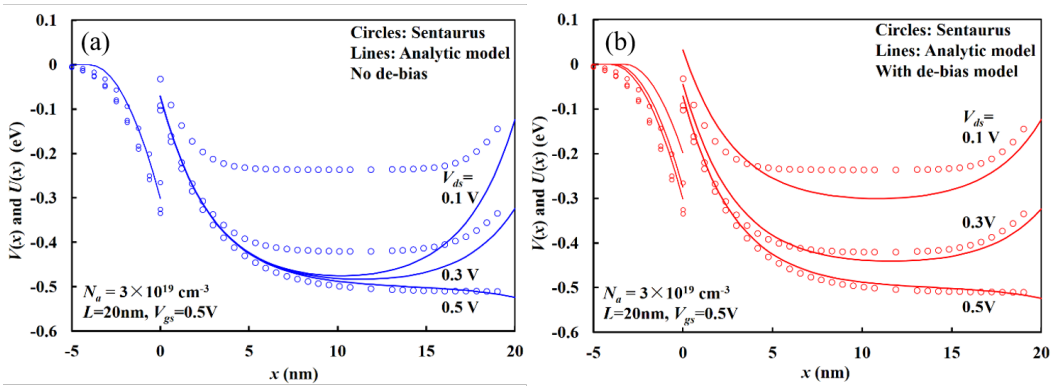

Figure 2.10: Conduction band energy of channel from source to drain and valence band energy of source for a 20 nm TFET. V_{gs} is fixed at 0.5 V. The solid lines are calculated from (a) no de-bias model and (b) de-bias model. $Nc = 8.7 \times 10^{16} cm^{-3}$ (InGaAs) is assumed. $d_2 = 0$. The circles are from Sentaurus simulations taken at the center of film [same in both (a) and (b)].

the integral in equation 2.6 is given by V_0 or $E_0 + qV_{ds} + d_1 + d_2$, whichever is lower. Here d_2 is the drain degeneracy. In practice, this makes only a very slight difference in I_{ds} at V_{ds} below 0.1 V, because in that energy range, the tunneling path is long and both f_s and $f_d \approx 1$. There is very little contribution to the tunneling current.

Band diagrams at varying biases conditions for a 20nm TFET with and without de-bias effect is illustrated in Fig.2.10. Note that there is less source depletion in the $V_{ds} = 0.1V$ case because of the lower field at the junction due to de-bias. The model curves are generally consistent with those of Sentaurus taken at the center of the semiconductor

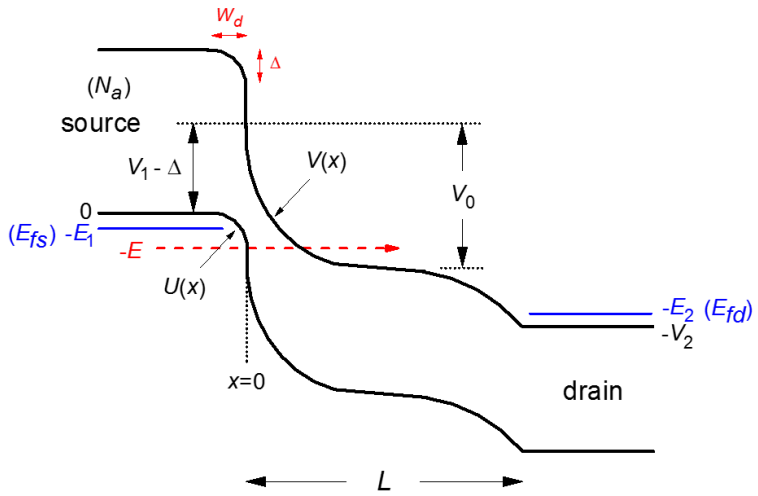

Figure 2.11: Band diagram of a heterojunction TFET with p^+ source and n^+ drain.

film. At the surface, the Sentaurus potential at mid-channel closely matches that of the analytic model. But there is more source depletion in the surface potential of Sentaurus due to the effect of gate fringe field not considered in the analytic model.

2.4 Short Channel Effect

2.4.1 Potential profile and $T(E)$

Similar to MOSFET, the performance of a TFET will also be degraded as channel length shrinks, although the cause is different. Fig.2.11 shows the band diagram of a staggered heterojunction DG TFET. The zero energy reference is taken to be the valence band edge of the bulk source region. The diagram is made for a turned-on TFET biased in saturation. V_1 is the effective bandgap between the conduction band of channel and the valence band of source at the heterojunction boundary (x = 0). Δ and W_d are the

band bending and the width of depletion in the source region doped at a density N_a. V_0 represents the gate control of the channel conduction band that determines the tunneling window. V_2 is related to the drain bias. L is the channel length. The conduction band function V(x) holds the key to the TFET current.

The 2D potential in a double-gate (DG) TFET is obtained analytically by solving the boundary value problem of Poisson's equation with no charge as already indicated in section 2.1. The full solution is expressed as a series of eigenfunctions in equation 2.2 with discrete eigenvalues λ_n:

$$\psi(x) = V_g - \Delta\phi + \sum_{n=1}^{\infty} \left[\frac{b_n sinh(\pi(L-x)/\lambda_n) + c_n sinh(\pi x/\lambda_n)}{sinh(\pi L/\lambda_n)} \sin\left(\frac{n\pi}{2} + \frac{\pi y}{\lambda_n}\right) \right] \quad (2.20)$$

Here, y is in the depth direction with y = 0 at the center of the film. The constant term $V_{gs} - \Delta\phi$is the long channel potential. $\Delta\phi$ is the gate work function. The b_n series stem from the source boundary condition and the c_n series from the drain boundary condition [40]. The coefficients depend on the boundary values as well as on the film thickness and permittivity.

For the function V(x) in the short-channel TFET model in Fig.2.11, we approximate the full 2D potential solution, Equation 2.20, by a combination of only the n = 1 sinh factors and the constant term,

$$V(x) = V_0 \frac{\sinh[\pi(L-x)/\lambda]}{\pi L/\lambda} - V_0 + V_1 - \Delta - (V_2 - V_0 + V_1 - \Delta)\frac{\pi x\lambda}{\pi L\lambda} \quad (2.21)$$

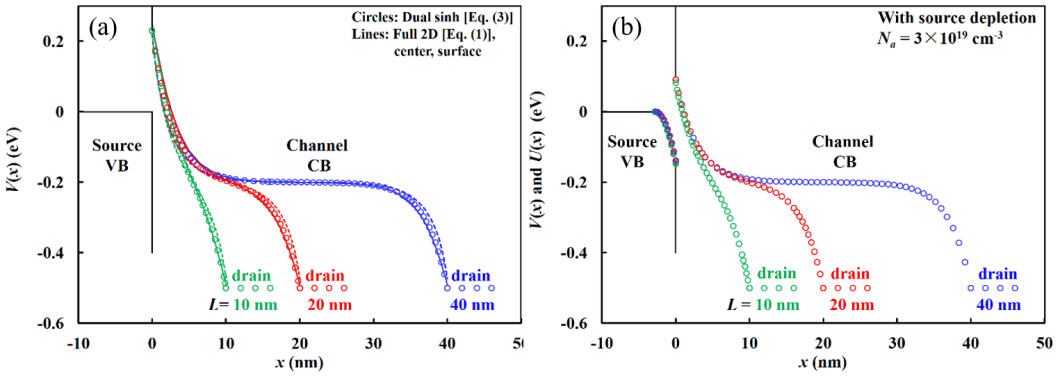

Figure 2.12: (a) Channel potential without source depletion. Circles are the dual sinh function of equation 2.21 with $\Delta = 0$, $V_1 = 0.23eV$, $V_0 = 0.43eV$, $V_2 = 0.5eV$, and $\lambda = 9nm$. Solid lines are $-q\psi(x,0)$ and dashed lines $-q\psi(x,t_s/2)$, both from equation 2.20 with n = 1, 3, 5, 7 terms. (b) Channel and source potential with source depletion of doping $N_a = 3\times10^{19}cm^{-3}$. Circles are from equation 2.21 and 2.11 coupled by equation 2.22. The same V_1, V_2, and $V_0+\Delta$ (= 0.43 eV) as in (a) are assumed.

Note that the coefficients, different from b_1 and c_1 in equation 2.20, are chosen to satisfy the depth independent source and drain boundary conditions in Fig.2.11, $V(0) = V_1 - \Delta$ and $V(L) = -V_2$. The three terms of V(x) in equation 2.21 represent the effects of source, gate, and drain on the channel potential. A similar three-term potential has been applied to nanowire TFETs [53], but with a scale length based on the parabolic potential model which does not satisfy 2D Poisson's equation for the entire region. We choose a material system of AlGaAsSb source and InGaAs channel that gives an effective bandgap of $V_1 = 0.23eV$. Fig.2.12(a) compares equation 2.20 and 2.21 for the example of $\lambda = 9nm$ ($t_s = 5nm$, $t_i = 2nm$) and $\Delta = 0$ for L = 40, 20, and 10 nm. It shows that the dual sinh function of equation 2.21 adequately captures the channel length dependence of the full 2D potential solution. The 10 nm potential curve reveals a thinning of the source barrier by the proximity of the drain—a hint of short-channel effect.

By applying the condition that the field is continuous from one side of the

heterojunction to the other (assuming no change of permittivity), we have

$$\frac{1}{q}\left|\frac{dV}{dx}\right|_{x=0} = \frac{\pi}{q\lambda}\frac{V_0\cosh(\pi L/\lambda)+(V_2-V_0+V_1-\Delta)}{\sinh(\pi L/\lambda)} = \frac{2\Delta}{qW_d} = \sqrt{\frac{2N_a\Delta}{\varepsilon_s}} \qquad (2.22)$$

where we employed the depletion approximation for the source, $W_d = \sqrt{2\varepsilon_s\Delta/(q^2N_a)}$. V_2 is determined by the drain voltage, V_{ds}. Note that the tunneling window starts to open when $V_0 = V_1 - \Delta$. If we define this condition to be $V_{gs} = 0$, then $qV_{gs} = V_0 - (V_1 - \Delta)$. This is valid under saturation conditions, or $V_{ds} > V_{gs}$, when the mobile charge in the channel is negligible so the gate direct modulates the channel potential. Implicitly assumed is a choice of the gate work function dependent on the band offset, the barrier height V_1 at the heterojunction, and the source doping. Substituting the above relation in equation 2.22 allows V_0 to be solved for given V_{gs}:

$$\frac{\pi}{q\lambda}\frac{V_0\cosh(\pi L/\lambda)+(V_2-V_0+V_1-\Delta)}{\sinh(\pi L/\lambda)} = \frac{2\Delta}{qW_d} = \sqrt{\frac{2N_a(qV_{gs}+V_1-V_0)}{\varepsilon_s}} \qquad (2.23)$$

Fig.2.12(b) shows the calculated V(x) and U(x) with a source doping N_a of $3\times10^{19}cm^{-3}$, for the same bias conditions and channel lengths as those in Fig.2.12(a). While it is straightforward to model the drain depletion effect in a similar manner, we chose to neglect it for simplicity since drain depletion has little or no effect on tunneling current.

The procedure of calculating transimission probability current density is the same as described in section 2.2, except that the V(x) in equation 2.14 is replaced by 2.21 and the WKB term for $V(x)$ needs to be evaluated numerically. Also note that for electron

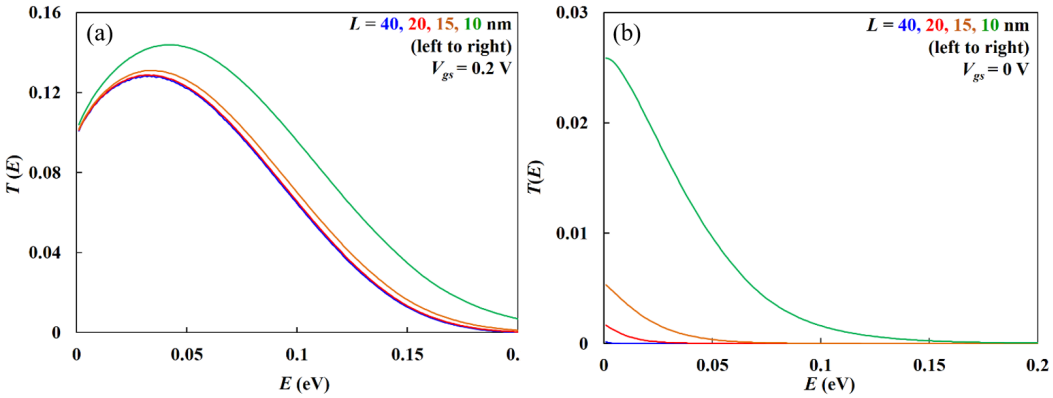

Figure 2.13: Tunneling probability versus (-) carrier energy for different channel lengths. The window for source to channel tunneling is 0.2 eV for (a) and 0 eV for (b). Other parameters are: $N_a = 3 \times 10^{19} cm^{-3}$, $V_1 = 0.23eV$, $V_2 = 0.5eV$, $\lambda = 9nm$, and $m = 0.1m_0$.

energies below $-\Delta$, there is no tunneling in the source and WKB term for $U(x)$ goes away.

Fig.2.13 shows an example of T(E) calculated for several different L, with a source doping of $N_a = 3 \times 10^{19} cm^{-3}$. The tunneling window in Fig.2.11 covers an energy range $0 \leq E \leq V_2$. The total flux of tunneling is proportional to the area under T(E). When $qV_{gs} = V_0 - (V_1 - \Delta) = 0.2eV$ in Fig.2.13(a), the conduction band of channel is well within the tunneling window and the area is only slightly sensitive to the channel length. Note that T(E) tends to peak at an energy $E = \Delta - V_1/2$ where the electron and hole tunneling barriers are about equal. However, when $V_{gs} = 0V$ in Fig.2.13(b), T(E = 0) and beyond consist only of tunneling from the source to the drain. The area under T(E) is very sensitive to L.

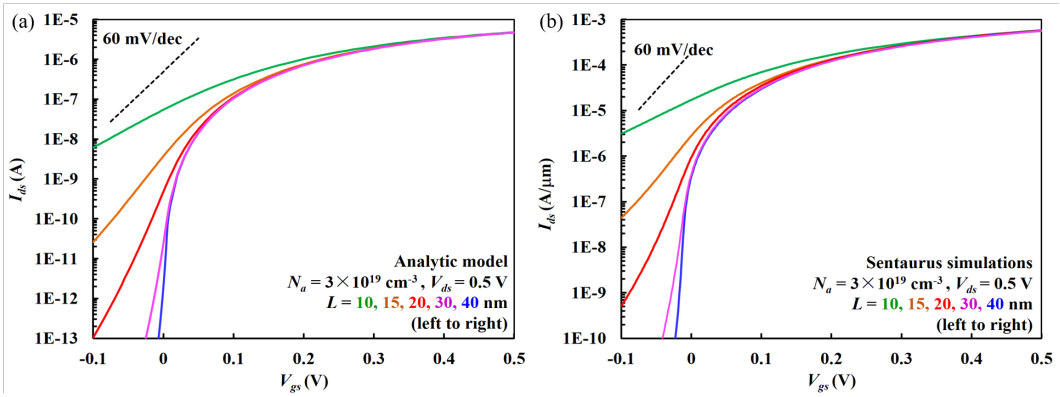

Figure 2.14: (a) Model generated high drain-bias $I_{ds} - V_{gs}$ characteristics for different values of L. Parameters N_a, V_1, λ, m are the same as Fig.2.13; $d_2 = 0$. (b) Sentaurus simulations with the same set of parameters.

2.4.2 Current characteristics

The current characteristics for short channel TFET are also calculated by Landauer equation described in Equation 2.6. The only difference is the inclusion of source-to-drain tunneling manifested in the upper bound of integral. Namely, the current integral covers the source-to-channel tunneling for $E \in (0, V_0 - V1 + \Delta)$ and the source-to-drain tunneling for $E \in (V_0 - V_1 + \Delta, V_2)$. The parameter V_2 in equation 2.21, which is also the upper bound of the current integral, can be expressed as $V_2 = qV_{ds} + d_1 + d_2$ where d_2 is the drain degeneracy.

$I_{ds} - V_{gs}$ characteristics generated by Landauer equation with $V_{ds} = 0.5V$ are plotted in Fig.2.14(a) for several different L. The same source doping, $N_a = 3 \times 10^{19} cm^{-3}$, as in Fig.2.13 is assumed; d_1 is calculated to be 0.024 eV from the Fermi integral $F_{1/2}(d_1/kT) = (\pi^{1/2}/2)(N_a/N_v)$ with an effective density of states $N_v = 2 \times 10^{19} cm^{-3}$. For long channel TFETs, the current is not sensitive to L. Below $L \approx 2\lambda = 18nm$, however, both the subthreshold slope and the off current, $I_{ds}(V_{gs} = 0)$, degrade rapidly. This is

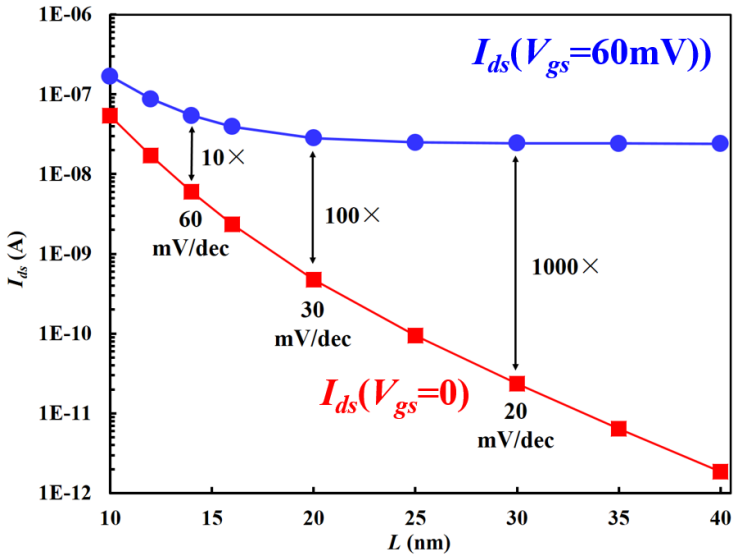

Figure 2.15: Currents at $V_{gs} = 0$ and $60mV$ from the data of Fig.2.14(a) versus L.

more clearly shown in Fig.2.15 by plotting $I_{ds}(V_{gs} = 0)$ and $I_{ds}(V_{gs} = 60mV)$ versus L. $I_{ds}(V_{gs} = 0)$ comes only from source-to-drain tunneling, which keeps on increasing toward shorter channel lengths. $I_{ds}(V_{gs} = 60mV)$ consists of both source-to-channel tunneling and source-to-drain tunneling but is dominated by the former. It is insensitive to L until $L \leq 2\lambda$ where thinning of the source-to-channel barrier sets in. The subthreshold current slope at any given L can be read from the ratio of the two currents in Fig.2.15. Below $L \approx 1.5\lambda$, the subthreshold swing can no longer beat 60 mV/decade, the kT/q limit.

Fig.2.14(b) shows the $I_{ds} - V_{gs}$ curves from Sentaurus simulations [42] under a similar set of parameters. They generally agree with the model results in Fig.2.14(a).

There is a distinctive difference between the SCE of TFETs and that of MOSFETs. In MOSFETs, the first-order effect of SCE is to cause a lower threshold voltage which shifts the entire $I_{ds} - V_{gs}$ curve negatively in a parallel fashion that both the off- and

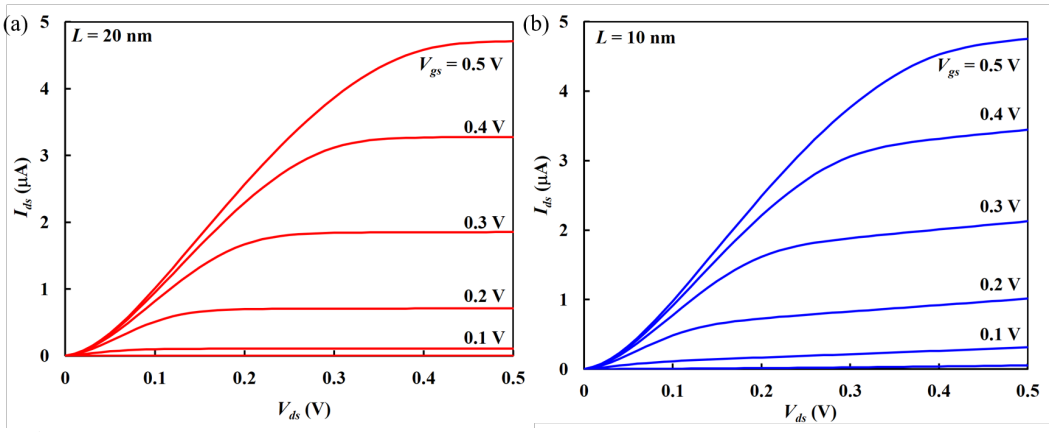

Figure 2.16: $I_{ds} - V_{ds}$ characteristics for (a) L = 20 nm and (b) 10 nm TFETs generated by the analytic model with de-bias. N_c and d_2 are the same as in Fig.2.10

the on-currents go up [40]. In TFETs, SCE mainly degrades the slope of $I_{ds} - V_{gs}$ near $V_{gs} = 0$, hence the off-current goes up sharply, while the on-current at large V_{gs} is hardly affected.

Output characteristics can also be calculated with de-bias effect included. Continuous $I_{ds} - V_{ds}$ characteristics are generated for L = 20 nm and 10 nm TFETs, as shown in Fig.2.16. Similar to short-channel MOSFETs, finite output conductance appears in the saturation region of the 10 nm TFET. It is due to the drain effect on the source-to-channel barrier, as noted before with the L = 10 nm curve (green) in Fig.2.12. This effect does not become significant until $L \approx \lambda$.

2.5 Dimensionality Dependence

In this section, we investigate the CV/I metric of 1D, 2D, and 3D TFETs as a function of supply voltage using an exponential potential profile (as solved in section 2.1)

from the scale length model. Approximate expressions of $I_{ds}(V_{gs})$ are derived with different power-law dependence on V_{gs} and effective mass.

2.5.1 1D, 2D, and 3D TFET models

In this study, we assume long channel approximation and thus an exponential barrier, $exp(-\pi x/\lambda)$ in the channel, with λ being the scale length related to the device thickness or radius as already demonstrated in section 2.1. Again, we define $V_{gs} = 0$ to be the condition $V_0 = V_1$ when the tunneling window from the source valence band to the channel conduction band starts to open. The TFET currents with 1D, 2D, or 3D density of states are given by [54]:

$$I_{1D} = \frac{2q}{h}\int (f_s - f_d)T(E)dE \tag{2.24}$$

$$I_{2D} = \frac{2q}{h}\frac{\sqrt{2\pi m}}{h}\int\int (f_s - f_d)T(E+E_\perp)\frac{dE_\perp}{\sqrt{\pi E_\perp}}dE \tag{2.25}$$

$$I_{3D} = \frac{2q}{h}\frac{2\pi m}{h^2}\int\int (f_s - f_d)T(E+E_\perp)dE_\perp dE \tag{2.26}$$

The WKB integral in the tunneling probability can be analytically evaluated for the exponential barrier derived in equation 2.5 for all the 3 cases. By expanding $T(E+E_\perp)$ to the first order of $E_\perp$ [55], the $E_\perp$ integration can be executed to consolidate all TFET currents to a single integral of the following general form (in proper units of A,

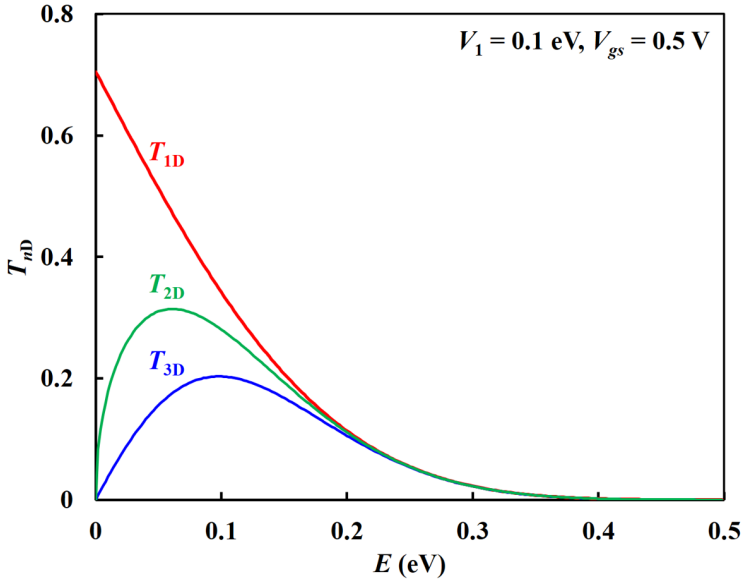

Figure 2.17: T_{nD} versus E. $m = 0.1m_0$ and $\lambda = 9nm$ are assumed throughout the section

A/m, and A/m^2 for I_{1D}, I_{2D}, and I_{3D}),

$$I_{nD} = \frac{2q}{h}\int_0^{V_0-V_1}(f_s - f_d)T_{nD}(E)\left[\frac{2\pi m E_t}{h^2}\right]^{(n-1)/2} dE \tag{2.27}$$

where n = 1, 2, 3. Here, $T_{1D}(E) = T(E)$, $T_{2D}(E) = T(E)erf[sqrtE/E_t]$, $T_{3D}(E) = T(E)[1–exp(-E/E_t)]$, with E_t given by:

$$\begin{aligned} E_t &= \left[-\frac{\sqrt{2m}}{\hbar}\int_0^l \frac{dx}{\sqrt{V(x)+E}}\right]^{-1} \\ &= \frac{h\sqrt{V_0 - E - V_1}}{4\lambda\sqrt{2m}\arcsin\sqrt{(E+V_1)/V_0}} \end{aligned} \tag{2.28}$$

Fig.2.17 plots T_{1D}, T_{2D}, and T_{3D} versus E. For 1D, T(E) is highest at $E = 0$. For 2D and 3D TFETs, however, because of the density of states factors due to $E_\perp$, the T_{2D} and T_{3D} products start at 0 at $E = 0$ then rise to a peak at $E > 0$, thus missing the

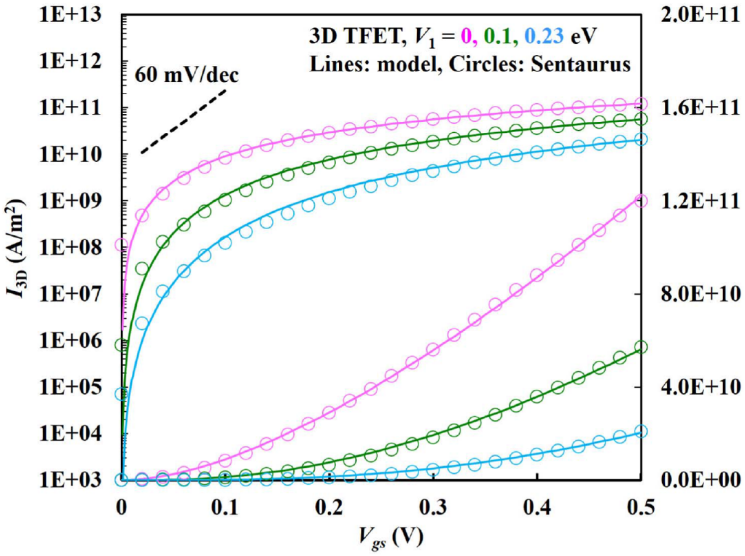

Figure 2.18: $I_{3D} - V_{gs}$ for three different bandgaps. Circles: Sentaurus simulation. The semiconductor is 5 nm thick, with 2 nm thick insulator on each side.

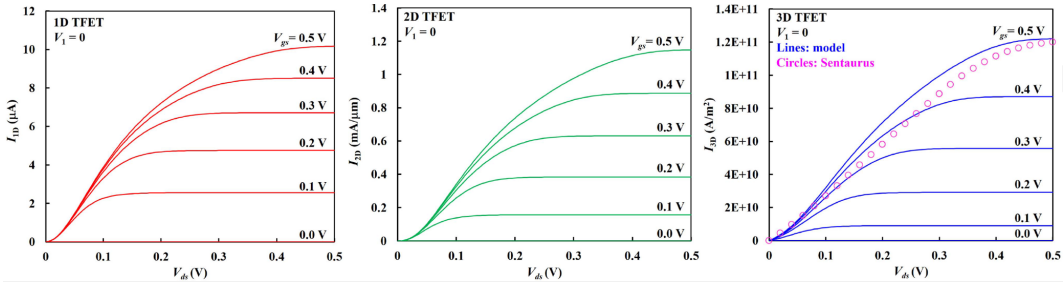

Figure 2.19: (a)I_{1D}–V_{ds}, (b)I_{2D}–V_{ds}, and I_{3D}–V_{ds} for zero-staggered bandgap. Sentaurus curve is shown for $V_{gs} = 0.5V$ with the 3-D TFET.

contribution at low E where the tunneling probability is the highest.

2.5.2 I-V Characteristics

In Fig.2.18, we plot model generated $I_{ds} - V_{gs}$ curves for 3D TFETs with $V_1 = 0.23eV$, $0.10eV$, and 0. The 3D model results are consistent with Sentaurus simulations. They quantify the gains in current from the narrower bandgap of the heterojunctions. The

Table 2.2: Contrast of 1D, 2D, and 3D TFET parameters.

	T_{nD} (E=0)	dT_{nD}/dE (E=0)	units of I_{nD}	$I_{nD} - m$ Dependence	$I_{nD} - V_{gs}$ Dependence
1D	> 0 max.	< 0	A	$\propto m^{-1/3}$	$\propto V_{gs}^{2/3}$
2D	0	∞	A/m	Indep. of m	$\propto V_{gs}$
3D	0	> 0	A/m^2	$\propto m^{1/2}$	$\propto V_{gs}^{3/2}$

highest current is obtained in the case of zero effective bandgap or $V_1 \to 0$. $V_1 < 0$ or broken gap TFETs are vulnerable to subthreshold swings $> 60mV/decade$ [46].

Expressions for the maximum currents of 1D, 2D, and 3D heterojunction TFETs can be derived in the limit of $V_1 \to 0$. By setting $f_s - f_d = 1$ (in saturation), the current integrals are numerically fitted to various powers of V_{gs}:

$$I_{1D}(V_1 = 0) \approx 0.74q \left(\frac{q^2}{mh\lambda^2} \right)^{1/3} V_{gs}^{2/3} \tag{2.29}$$

$$I_{2D}(V_1 = 0) \approx 0.58 \frac{q^2 V_{gs}}{\lambda h} \tag{2.30}$$

$$I_{3D}(V_1 = 0) \approx 0.47 \frac{q^2 \sqrt{mq} V_{gs}^{3/2}}{\lambda h^2} \tag{2.31}$$

The V_{gs} dependence can be summarized as $I_{nD} \propto V_{gs}^k$ where $k = (3/2)^{n-2}$ for all n = 1, 2, 3. Note that the $V_{gs}^{3/2}$ dependence of I_{3D} is the same as the saturation current of a ballistic MOSFET [56]. The sub-linear and super-linear V_{gs} dependence of 1D and 3D TFETs can be seen in the model generated $I_{ds} - V_{ds}$ plots in Fig.2.19. All maximum currents are $\propto 1/\lambda$ or nearly so, thus improve with scaling of the film thickness. The dependence on effective mass m (assumed isotropic) is mixed. I_{1D} goes up with lighter

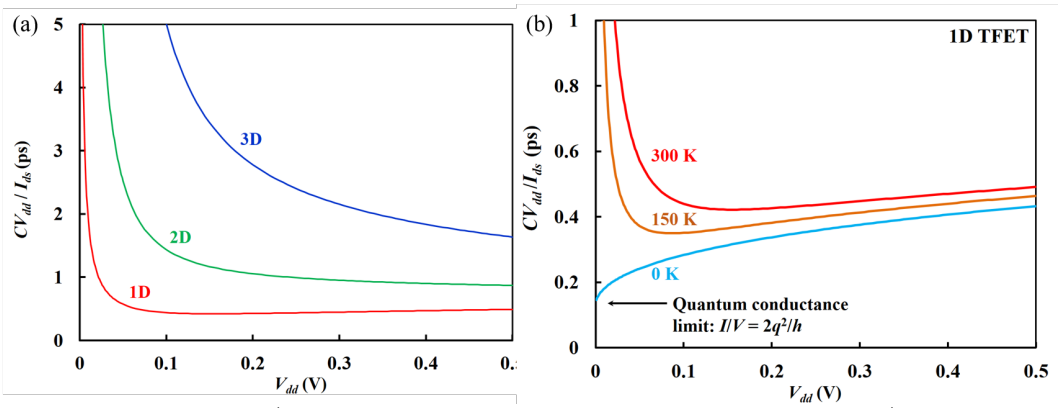

Figure 2.20: (a) CV/I versus V_{dd} for 1D, 2D, and 3D TFETs. $C = 2fF/\mu m$, $V_1 = 0$; (b)CV/I versus V_{dd} for 1D TFETs at three different temperatures. $V_1 = 0$.

m due to the tunneling mass in the WKB integral. I_{3D} increases with m where the density of states wins. I_{2D} is independent of m as the two effects cancel. A summary of contrast for 1D, 2D and 3D TFET parameters are shown in Table 2.2.

2.5.3 CV/I Assessment

Fig.2.20(a) plots CV_{dd}/I_{ds} ($V_{gs} = V_{ds} = V_{dd}$) calculated from equation 2.27 versus V_{dd} for n = 1, 2, 3. For 2D, I_{ds} is taken to be I_{2D} in A/m or $mA/\mu m$. For 3D, I_{ds} is I_{3D} times 5 nm, the semiconductor thickness. For 1D, I_{ds} is I_{1D} divided by 5 nm, assuming that one piece of 1D semiconductor can be placed per 5 nm width. C is assumed to be a constant, $2fF/\mu m$. For 3D TFETs, CV/I goes up as V_{dd} decreases, similar to the conventional MOSFETs. For 2D, CV/I is more or less flat. But for 1D, CV/I decreases as V_{dd} is reduced, implying that instead of delay-power tradeoff, both the delay and the power improve at lower voltages. A minimum CV/I is reached at $V_{dd} \approx 0.15V$ for 1D TFETs, shown in more detail in Fig.2.20(b). Below that CV/I goes up sharply because

of the kT transition width of the Fermi-Dirac distribution function [57], [58]. If the temperature is reduced to 150 K, the V_{dd} for minimum CV/I is also reduced by $2\times$ to $\approx 0.08V$. The zero temperature curve, for which $f_s - f_d = 1$, keeps on decreasing until reaching the quantum conductance limit of $I/V = 2q^2/h$. Thus the lower limit is $V_{dd} \approx 6kT/q$ for 1D TFETs without losing performance. The ultimate voltage scaling is achieved through scaling of dimension.

2.6 Conclusion

In this chapter, physics based analytic model for double gate TFET is studied by solving 2D Poisson's equation. It is also shown that the solution can be applied directly to a nanowire device with a separate definition of scale length, λ. Various aspects including channel barrier, source doping, de-bias effect, short channel effect and dimensionality dependence have been considered that affect the performance of the device. A compact, physics-based model could provide us with more physical insights within less simulation time, paving the roads for the performance optimization of TFET.

2.7 Future Work

The calculation for current density still involves one numerical integration for 1-D device and two numerical integrations for 2-D and 3-D devices. To build a physical and compact model suitable for circuit design purposes, analytic approximations for these

integration could be further explored in the future. Analytic charge model, which takes into accounts the quasi-static charge distributions at the three terminals, is also desired for AC and transient circuit simulations. A compact model with physical parameters instead of fitting parameters could optimize the circuit performance by tuning more effectively and efficiently.

2.8 Acknowledgment

Chapter 2, in full, is a re-organization of several papers worked in collaboration with Prof. Taur Yuan and Dr. Jianzhi Wu. 1. **J. Min**, J. Wu, Y. Taur, "Analysis of source doping effect in tunnel FETs with staggered bandgap", *IEEE Electron Dev. Lett.*, vol.36, pp.1094-1096, 2015. The dissertation author was the primary author of the paper. 2. Y. Taur, J. Wu, **J. Min**, "Dimensionality dependence of TFET performance down to 0.1V supply voltage", *IEEE Trans. Electron Dev.*, vol.63, pp.877-880, 2016. 3. J. Wu, **J. Min**, Y. Taur, "An analytic model for heterojunction and homojunction tunnel FETs with 3D density of states", *Device Research Conference*, pp.249-250, 2015. 4. Y. Taur, J. Wu, **J. Min**, "A Short-Channel I-V Model for 2-D MOSFETs", *IEEE Trans. Electron Dev.*, vol.63, no.6, pp.2550-2555, 2016. 5. J. Wu, **J. Min**, Y. Taur, "Short channel effects in tunnel FETs", *IEEE Trans. Electron Dev.*, vol.62, pp.3019-3024, 2015. 6. Y. Taur, J. Wu, **J. Min**, "An analytic model for heterojunction tunnel FETs with exponential barrier", *IEEE Trans. Electron Dev.*, vol. 62, pp. 1399-1404, 2015. The dissertation author was the co-author of the these papers to be included for the congruity of Chapter 2.

Chapter 3

Temperature dependence and Variability study on DG-TFET

This chapter provides an analysis of the intrinsic factors influencing the temperature dependence of the $I_{ds} - V_{ds} - V_{gs}$ characteristics of heterostructure Tunnel FETs based on GaSb/InAs tunneling junctions. The temperature dependence of energy bandgap, quantum confinement energy-shifts, and fermi-level position are quantified. There is significant cancellation among the various effects, such that the overall $I_{ds} - V_{ds} - V_{gs}$ characteristics are expected to have remarkably small temperature dependence, of the order of 10-20mV shift in V_{gs} over the temperature range of 0 to 125°C. Considerations are also discussed for representative extrinsic effects such as trap-assisted tunneling, which affect many experimental devices to a variable extent.

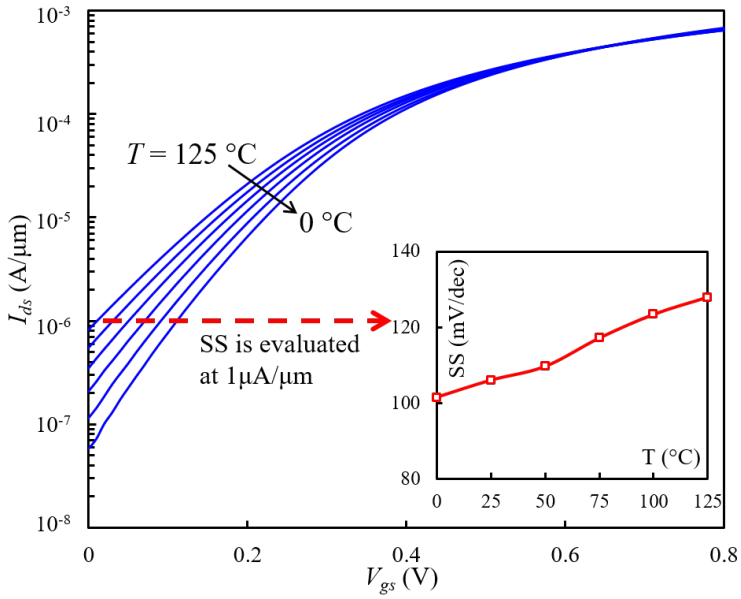

Figure 3.1: Representative $I_{ds} - V_{gs}$ for a 32nm Si nMOSFET as temperature varies from 0℃ to 125℃(25 degree steps), $V_{ds} = 0.5V$. Inset shows the subthreshold slope versus temperature evaluated at $1\mu A/\mu m$.

3.1 Introduction

TUNNEL FETs (TFETs) are under active study for potential application in digital, analog and microwave circuits operating with low power supply voltages and low power dissipation [59]–[64]. Their projected subthreshold swing of well below 60mV per decade permits TFETs to respond sensitively to small input signals. For conventional Si MOSFETs operating at low voltages below threshold V_{TH}, the drain current at a given V_{gs} and V_{ds} is highly temperature dependent. Representative curves are shown in Fig.3.1, corresponding to a 32nm nMOS device with $V_{ds} = 0.5V$. The inset of Fig.3.1 shows the temperature dependence of the subthreshold slope at a constant current level of $1\mu A/\mu m$. In the subthreshold regime, the V_{gs} needed to attain a given current level changes by as much as approximately 1mV per ℃, complicating circuit design. The

corresponding current at a given voltage in the subthreshold regime can change by 10 times. Temperature dependence for conventional MOSFETs results from the fact that current flow results from thermal activation of electrons over the barrier between source and channel, as well as from temperature dependent drift and diffusion in the channel. In TFETs, electrons reach the channel from the source by tunneling, which is in principle temperature independent, leading to expectations for considerably reduced temperature dependence of the current. On the other hand, in view of the increased sensitivity of drain current to V_{gs}, it is highly desirable that the temperature sensitivity of V_{th} (dV_{th}/dT) have a particularly small value, in order to maintain a small value of dId/dT at a fixed V_{gs}. In this paper, the factors that influence the temperature dependence of $I_{ds}vs.V_{gs}$ and V_{ds} in Tunnel FETs are examined.

The primary device type examined in this paper is a double-gate heterojunction TFET based on GaSb/InAs materials, although the issues and conclusions can be readily generalized to different device structures. Multiple effects are shown to influence the characteristics, which in general cause opposite temperature-induced changes. In this study, we first focus on temperature effects on intrinsic band-to-band tunneling (BTBT) and exclude the effect of trap-assisted tunneling (TAT) to reveal the fundamental limitations for TFETs. We then extend the discussion to include the effects that may be expected with non-ideal TAT current.

The paper is organized as follows. In the first section, the device structure is introduced along with the basic parameters used for simulations. In the second section, various factors that contribute to the temperature dependence of the threshold voltage are

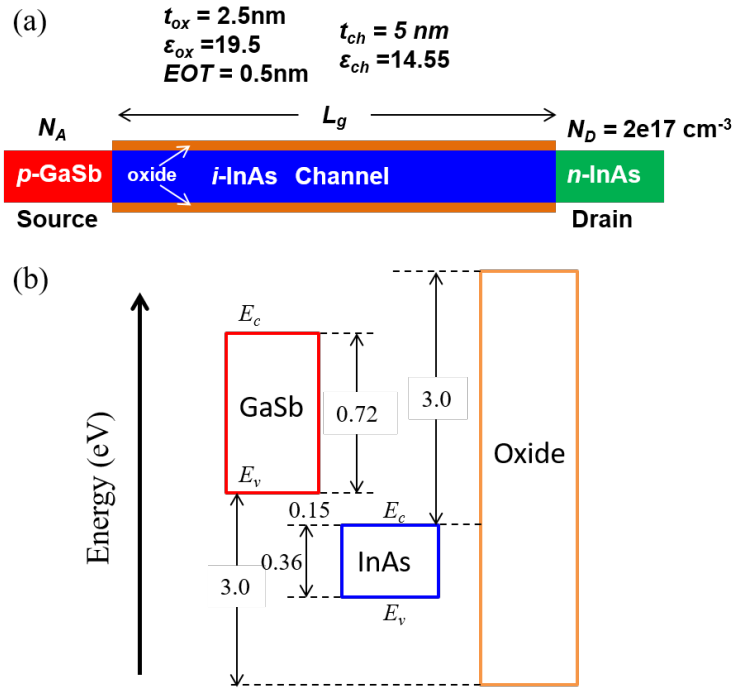

Figure 3.2: (a) Structure of simulated device and (b) schematic band alignment of bulk materials used in the device.

described, from a conceptual perspective. The discussion is further expanded with details on the temperature dependence of conduction band edge shift for channel, quantum confinement, and the Fermi level position with reference to the source valence band. Their corresponding influences on the tunneling bandgap, the threshold voltage and the $I_{ds} - V_{ds} - V_{gs}$) characteristics are presented in the third section. We expand our discussion to include the TAT and band tailing effects in the fourth section. The last section provides a summary of the work.

3.2 Device Structure and Model

A GaSb/InAs heterojunction double gate TFET is used as the prototype device for this study. The source is implemented with heavily doped p-type GaSb with heavy hole mass, $m_{hh} = 0.4m_0$ and light hole mass, $m_{lh} = 0.05m_0$ at 300 K [65], [66]. The channel is made of intrinsic InAs, with effective electron mass of $0.0225m_0$ at 300K [67]. A gate length of 20 nm and a device width of 5nm are set to maintain good electrostatics. On the drain side, a moderate doping of $2 \times 10^{17} cm^{-3}$ is used to avoid channel-to-drain tunneling in the off-state. An effective oxide thickness (EOT) of 0.5nm is used, achieved with a 2.5nm of high-k dielectric with dielectric constant of 19.5. I–V characteristics for devices of this structure have been previously reported [68]–[71]. In this work, detailed $I_{ds} - V_{ds} - V_{gs}$ curves are simulated using MATLAB. Fig.3.2(a) provides a schematic cross-section of the device, while the assumed band lineups of the different materials used within it are shown in Fig.3.2(b).

3.3 Temperature Dependent Factors

In order to determine the Id behavior of the device, it is important to consider the temperature effects on the band-diagram of the transistors, particularly the tunneling window, Egtun and threshold voltage, V_{TH}.

The threshold voltage V_{TH} for tunnel FET is defined as the minimum necessary V_{gs} bias to align lowest available state in the conduction band of the channel to the edge of valence band of the source. This definition is valid when no band tail is present. In such

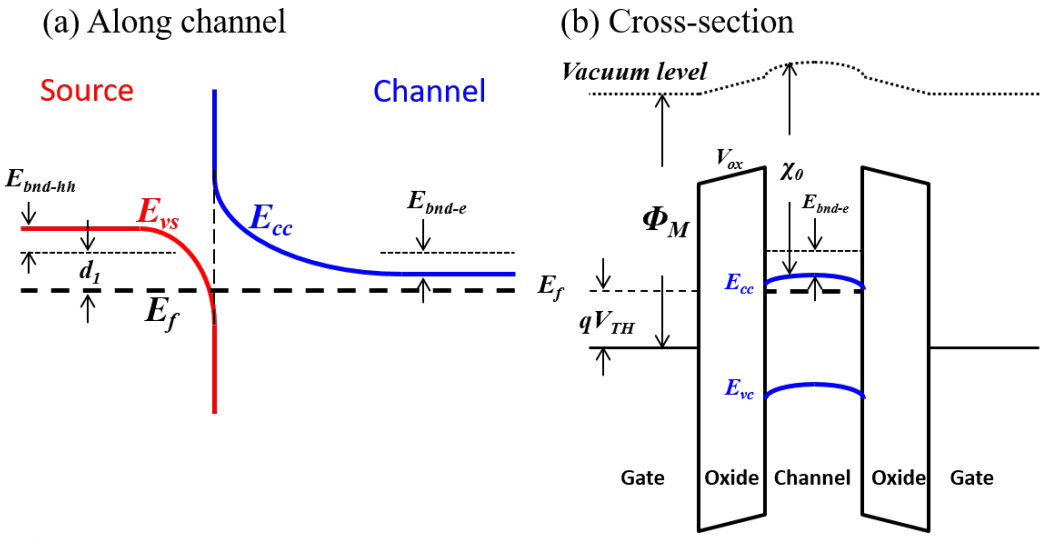

Figure 3.3: Band schematics of tunnel FET at (a) along the channel and (b) at cross section in threshold condition

a condition, a simple equation can be derived to determine the threshold voltage. Based on the schematic band diagram shown above, the threshold voltage may be expressed as:

$$V_{TH} = \frac{1}{q}[\Phi_M - \chi_0(T)] - d_1(T) + E_{bnd}(T) \tag{3.1}$$

Equation 3.1 has three temperature dependent terms: electron affinity (χ_0), Fermi level position with reference to source valence band edge (d_1), and the ground state energy level (E_{bnd}). The temperature dependence of the gate metal work function (Φ_M) is not considered in this paper.

To establish direct connection to the I-V characteristics of the TFET, we adopted the model provided by [68], where the effective tunneling band gap E_g^{tun} for heterojunction tunneling is shown to be an important parameter for ON-state current density. The

quantity is calculated by:

$$E_g^{tun} = \chi_0^{GaSb} + E_g^{GaSb} - \chi_0^{InAs} + E_{bnd-e} + E_{bnd-hh} \tag{3.2}$$

Given the small channel thickness considered in this study, the energy band gap term is not only affected by the displacement between the source valence band and channel conduction band edges , but also by the ground state energies due to the quantum confinement of carriers. Both parts are temperature dependent.

The different effects considered are discussed in detail below. The combined effect is used to calculate the change in threshold voltage V_{TH} and tunneling window. Two schematic band diagrams, one along the channel direction, and one perpendicular to the channel direction, are shown in Fig.3.3. The bias condition is set at $V_{gs} = V_{TH}$ and $V_{ds} = 0V$, such that the tunnel window is about to open. The quantity $d_1 = E_{vs} - E_{bnd-hh} - E_f$ is the Fermi-level position with reference to the edge of the source valence band; Φ_M is the work function of gate metal; χ_0 is electron affinity for channel material; E_{bnd-hh} and E_{bnd-e} are ground state energy levels due to quantum confinement effect for heavy holes in the source and for electrons in the channel; V_{ox} is voltage drop across the oxide. When the source is heavily doped, i.e. d_1 is significant comparing to kT, the channel will have little mobile charge at $V_{gs} = V_{TH}$ since E_f will be below the first bound state in the channel conduction band by the same amount as d_1. Thus, V_{ox} becomes negligible and can be approximated to be zero in evaluating V_{TH}, assuming the InAs body is lightly doped or undoped.

In the following, we provide detailed analysis of the individual factors that contribute to the temperature dependence of the threshold voltage, as indicated by equation 3.1.

3.3.1 Electron affinity in Channel, χ_0

With an increase of temperature, the band gap of semiconductor decreases due to inter-atomic spacing expansion as temperature increases and can be calculated by an empirical equation [72]:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T+\beta} \tag{3.3}$$

$E_g(0)$ is band gap at T=0K for the semiconductor, while α and β are empirical parameters that vary with the material. Following reported experimental results of [73], $\alpha = 2.76 - 4eV/K$ and $\beta = 83K$ for InAs and $\alpha = 3.78 - 4eV/K$ and $\beta = 94K$ for GaSb are used in our simulation. The band gap shrinkage can be considered as an action of closing the gap between valence band and conduction band. To take this into account when evaluating the temperature dependence of electron affinity, χ_0, we assigned a factor of 0.5 to account for the drop in conduction band energy as a function of temperature [74],

$$\chi_0(T) = \chi_0(0) - \frac{1}{2}\frac{\alpha T^2}{T+\beta} \tag{3.4}$$

(Yet the exact partitioning of the bandgap energy change between changes of conduction band and valence band energies in GaSb and InAs relative to the vacuum level is not known in detail). The temperature sensitivity of V_{TH} due to the electron

affinity can be readily derived as:

$$\frac{\partial}{\partial T}V_{TH}|_{d_1,E_{bnd}} = \frac{\alpha T^2 + 2\alpha\beta T}{2(T+\beta)^2} \tag{3.5}$$

3.3.2 Quantum confinement in the channel

In TFETs, quantum confinement plays an important role in determining the energy states in the conduction and valence bands, especially for the n-type III-V channel, owing to the small electron effective mass and the thin body. The temperature dependence of electron effective masses in III-V materials have been experimentally measured by magneto-phonon resonance (MPR) [67], [75], [76] and are relatively strong. Qualitatively speaking, with a decreased band gap value with increasing temperature, $k \cdot p$ theory predicts a decrease in effective mass. A linear function is adopted here to fit the experimental results of effective mass in [67], and further used to estimate the dependence of ground state energy on temperature. The fitting is graphically shown in Fig.3.4(a).

At elevated temperature, we expect an increase in ground state energy as effective mass decreases; this results in a higher threshold voltage. To calculate the bound state energies, a simple 1-D finite well model is applied for estimation of quantum confinement:

$$tan(\frac{\sqrt{2m^{\star}E_{bnd-e}}}{\hbar}\frac{t_{ch}}{2}) = \sqrt{\frac{\Phi_b - E_{bnd-e}}{E_{bnd-e}}} \tag{3.6}$$

In equation 3.6, $m^{\star}$ ($0.0225m_0$ @ 300K) is the temperature dependent effective mass of the channel; E_{bnd-e} is the conduction band bound state energy to be calculated;

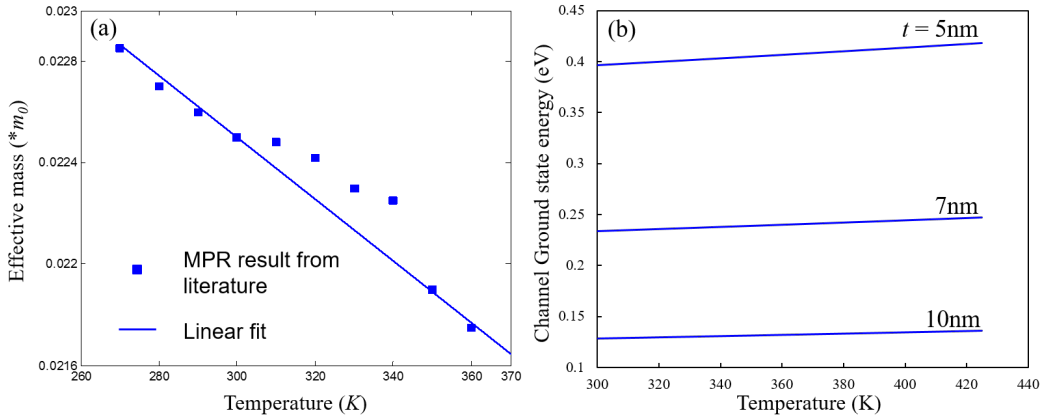

Figure 3.4: (a) Effective mass versus temperature from MPR result [67] and linear fitting and (b) Ground state energy (with respect to conduction band edge of channel) versus temperature for varying device thickness of t_{ch} = 5nm, 7nm and 10nm

t_{ch} is the thickness of the device (5nm 10nm); and Φ_b is the barrier height at channel/oxide interface (assumed to be 3.0eV). By numerically solving equation 3.6, with $m^\star$ as an implicit function of temperature, the solutions are shown in Fig.3.4(b) to characterize the T-dependence of the ground state energy (referenced to E_c edge).

The temperature sensitivity of the ground state energy, as shown in equation 3.1, contributes to the overall temperature dependence of the threshold voltage:

$$\frac{\partial}{\partial T} V_{TH}|_{d_1,\chi_0} = \frac{1}{q}\frac{d}{dT}(E_{bnd}) \tag{3.7}$$

The source side also experiences quantum confinement. However, it is not as pronounced as for the channel thanks to a much larger effective mass, m_h $0.4m_0$, for GaSb valence band. Consequently, the effect of quantum confinement from the channel dominates.

3.3.3 Fermi level position in source, d_1

Although the quantum confinement effect in the p-type source is much smaller than that in n-type channel region because of large effective mass, temperature dependent Fermi-Dirac distribution affects the Fermi level position in the source more significantly, because of its degenerate doping and relatively small N_v value. In 3D material, a $T^{3/2}$ dependence of effective density of states is added to account for temperature dependence on Fermi-Dirac distribution. In a highly-confined device, we consider the following two effects: 1) 2D density of states; 2) confined states of heavy holes and light holes, which need to be calculated separately. The equation to calculate the Fermi level position can thus be written as:

$$\begin{aligned} N_A^{2D} = &\frac{kT}{\pi\hbar^2} m_{hh}^{\star} ln(1+e^{(E_{hh0}-E_{fs})/kT}) + \frac{kT}{\pi\hbar^2} m_{hh}^{\star} ln(1+e^{(E_{hh1}-E_{fs})/kT}) \\ &+ \frac{kT}{\pi\hbar^2} m_{lh}^{\star} ln(1+e^{(E_{lh0}-E_{fs})/kT}) \end{aligned} \tag{3.8}$$

In equation 3.8, N_A^{2D} is fully ionized doping concentration in the confined device (in the unit of cm^{-2}); $m_{hh}^{\star}$ and $m_{lh}^{\star}$ represent heavy and light hole mass for source material (for GaSb, we use $0.4m_0$ and $0.05m_0$, respectively); E_{hh0} and E_{hh1} are the heavy hole ground state and 1^{st} excited state energy, respectively; E_{lh0} is the light hole ground state energy. We included the 1^{st} excited state of heavy hole in the Fermi level calculation because its corresponding energy is lower than light hole ground state. If we define E_{hh0} as the new effective valence band edge for the confined material, the Fermi level position in source reads $d_1 = E_{hh0} - E_{fs}$.Hence the change in threshold voltage due to the Fermi

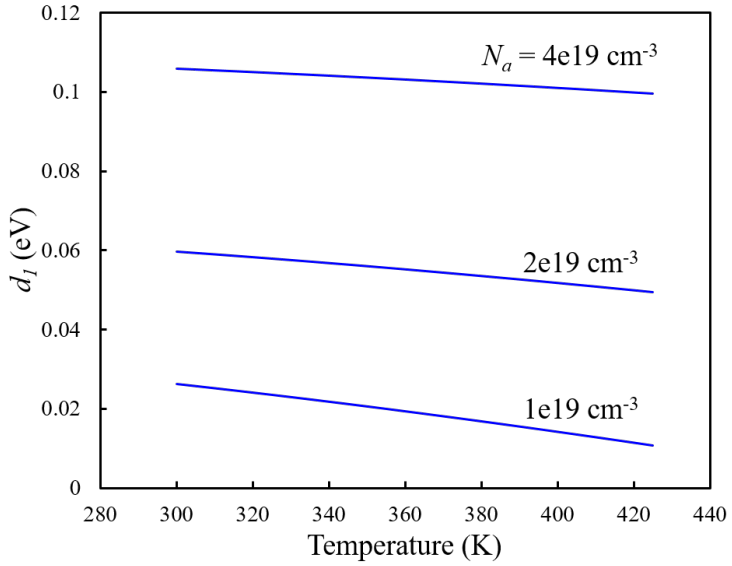

Figure 3.5: Fermi level positions against source valence band for varying temperature with different doping concentration

level position change is:

$$\frac{\partial}{\partial T} V_{TH}|_{E_{bnd},\chi_0} = \frac{1}{q}\frac{d}{dT}(d_1) \tag{3.9}$$

Higher doping concentration would cause less fluctuation in Fermi level with varying temperature. The effect is illustrated in Fig.3.5.

For a p-type TFET, the source is usually heavily n-doped. However, the effective mass of electron for III-V materials $m_e^\star$ is much smaller than heavy hole mass, typically by one order of magnitude, which implies much less dependence of d_1 on temperature with same source doping concentration. In a realistic design, however, the value of d_1 should be always kept around zero to achieve an optimized ON-state current by a lower source doping concentration [77], which implies a similar change of d_1 with respect to temperature in p-type TFET.

3.4 Temperature dependence of V_{TH}, E_g^{TUN}, and current characteristics

With all the factors above considered, we combine the contributions to assess the overall temperature dependence of V_{TH}.

$$\frac{d}{dT}V_{TH} = \frac{\alpha T^2 + 2\alpha\beta T}{2(T+\beta)^2} + \frac{1}{q}\frac{d}{dT}(E_{bnd}) + \frac{1}{q}\frac{d}{dT}(d_1) \tag{3.10}$$

The resultant temperature dependences of Vth due to each term are illustrated in Fig.3.6(a). Based on the previous analysis, term χ_0 is mostly material dependent and there is little degree of design freedom to be adjusted once material system is chosen. However, the contribution of quantum confinement can be tuned by device thickness, and that of d1 can be tuned by source doping level and device thickness.

To assess the temperature dependence of TFET current, we examine the temperature dependence of the proxy quantity, effective tunneling band gap, as described in equation 3.2. The temperature sensitivity of E_g^{tun} is shown in Fig.3.6(b). As is demonstrated, quantum confinement effect and bulk band gap shrinkage have an opposite temperature dependence and cancel out, yielding a weak tunnel gap dependence on temperature.

Taking into consideration the temperature dependence of threshold voltage (V_{TH}) and of effective tunnel bandgap, one may further derive the $I_{ds} - V_{gs}$ characteristics as follows (with $V_{ds} = 0.3V$ is used, as a representative case). Based on the equation 3.1

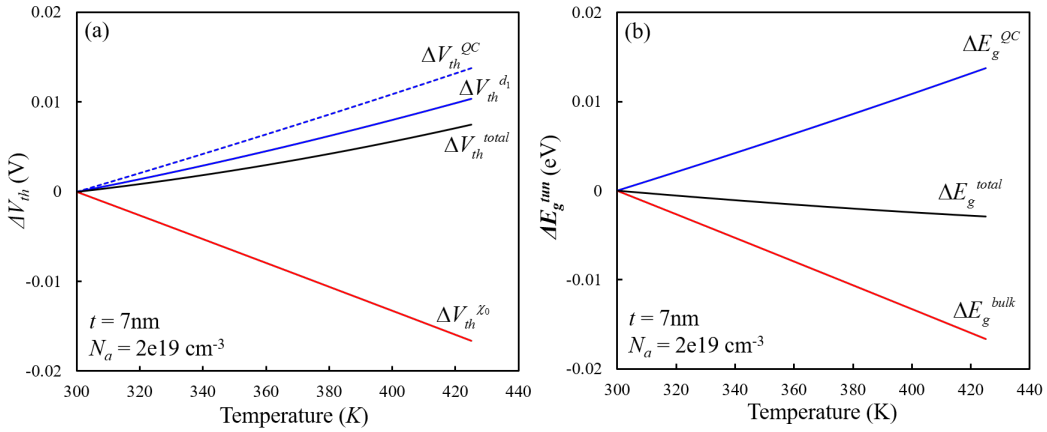

Figure 3.6: (a)Threshold voltage shift with respect to temperature from different contributions and total contribution: the quantum confinement (blue dashed line), the Fermi level position with respect to source valence band (blue solid line), the channel electron affinity (red solid line) and the total effect (black solid line) (b) Effective tunnel bandgap at heterojunction versus temperature with different contributions for t_{ch} = 7nm

and 3.2, it is possible to design a TFET device with minimal temperature dependence for key parameters like V_{TH} and E_g^{tun} by carefully choosing device thickness and source doping concentration, to employ the cancellation among the temperature dependences of various factors. In cases where we are more concerned about the leakage current range under varying temperature, V_{TH} will be the primary focus for design optimization. As shown in equation 3.10, both source doping and device thickness are potential adjustable parameters. However, source doping is also an important factor determining optimized ON-state current: overly low doping causes a high valence band barrier in the source and limits the tunneling probability while overly high doping depletes the electrons at the source: in either case non-optimal doping level causes a reduction in the ON-state current. Therefore, a viable design would first identify appropriate source doping level to ensure adequately optimized ON current. With this premise, the device thickness becomes

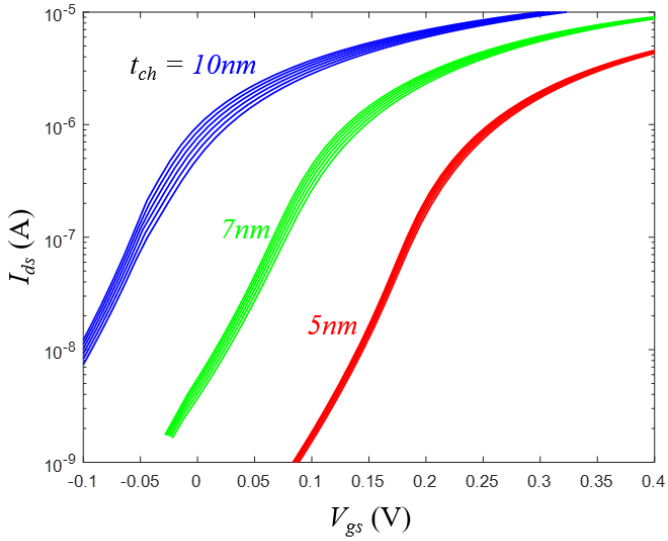

Figure 3.7: $I_{ds} - V_{gs}$ characteristics from T = 300K to 425K

the major parameter for V_{TH} optimization. Fig. 3.7 shows an optimization of V_{TH} with respect to temperature by a tuning of device thickness. The decrease of on-current with decreasing thickness comes from wider effective tunnel gap as quantum confinement effect becomes enhanced.

3.5 Extrinsic Effects and Bandtailing

Experimental results published by several groups have shown that trap-assisted tunneling (TAT) is a major concern in TFETs, leading to high OFF current, degradation of the sub-threshold slope, and strong temperature dependence of I-V characteristics [78]–[82]. The traps are extrinsic effects, which in principle can be minimized by decreasing the densities of trap states. The relevant traps include 1) defect states within the bandgaps of the materials used for source and channel; and 2) defects located at the interfaces

between the dielectrics and the semiconductors. Bulk oxide traps that interact with the channel may also play a role [83]. A general theory to describe the energy distributions and effect on tunneling current of these states is lacking.

Representative characteristics have been simulated in our work by considering that current flow proceeds by tunneling from a state in the valence band of the source to a trap state below the conduction band of the channel, followed by thermal excitation of the electron from the trap state to the conduction band. The temperature dependence of such a process is strongly influenced by the depth of the trap state relative to the conduction band of the channel. Representative I-V characteristics computed by Sentaurus [74] using dynamic nonlocal trap-assisted-tunneling physics are shown in Fig.3.8(a), using parameters $m_t = 0.1m_0$, $E_{trap} = 80meV$ below E_c of InAs. By assuming a cross-section of $\sigma = 10^{-14}cm^2$, thermal velocity of $v_{th} = 10^7 cm/s$ and trap volumetric density of $N_t = 10^{17}cm^{-3}$, an effective time constant of $\tau = (\sigma v_{th} N_t)^{-1} = 10^{-10}s$ is calculated. Simulations reveal that trap-assisted-tunneling mainly affects the current leakage floor, and has little effect on subthreshold-slope before turn on. The study reported in [84] also arrives at a similar conclusion when the trap density is small. By numerically varying the trap energy level at 300K with the same time constant, our simulations indicate that there exists a trap level which contributes most to the leakage current in Fig.3.8(b). In this case, a trap level 80meV below E_c of the channel contributes most to the leakage current. This is in analogy with the canonical Shockley-Read-Hall physics, where net generation / recombination rate will be maximized when E_{trap} is at the intrinsic level for $\tau_n = \tau_p$. In this case, the rate is determined by the balanced transport of electrons from source

E_v to traps, and from traps to channel E_c; the trap site which contributes most would lie somewhere in between source E_v and channel E_c, or equivalently in the middle of the tunnel band gap.

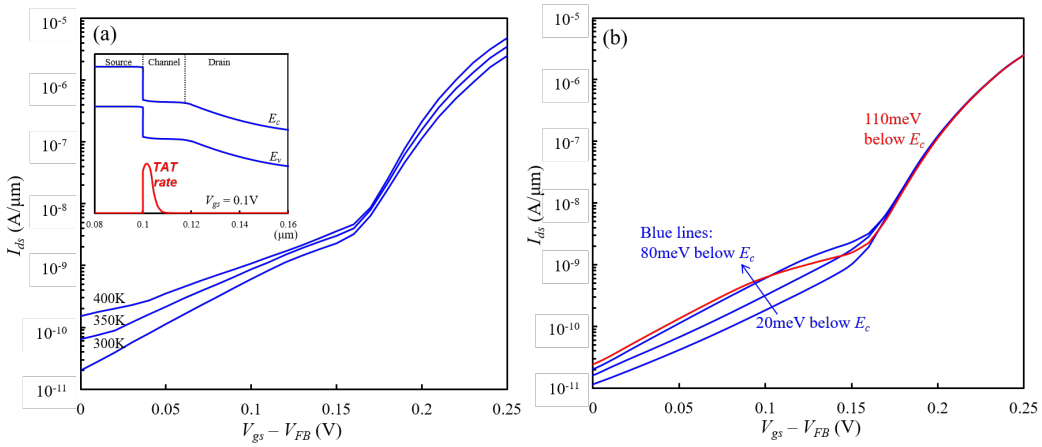

Figure 3.8: (a) Sentaurus simulation of $I_{ds} - V_{gs}$ characteristics from T = 300K to 400K including trap assisted tunneling physics for traps 80meV below channel E_c. Inset shows the band diagram at $V_{gs} = 0.1V, V_{ds} = 0.5V$ and trap-assisted tunneling rate along the channel. (b) $I_{ds} - V_{gs}$ curves with varying trap levels from 20meV to 110meV below channel E_c at 300K.

To relate these simulations to experimental results, we note that in [85], for Si/SiGe heterojunction TFETs, trap-assisted tunneling affects subthreshold slope greatly, unlike the present simulations. This is due to the relatively low I_{ON} contribution from band-to-band tunneling (BTBT) in the Si/SiGe case, resulting from the low tunneling probability in this system. In staggered band heterostructures, I_{ON} is increased to $10\mu A/\mu m$ or above, while TAT current still remains in the range of $1nA/\mu m$. We further note that for homo-junction Ge TFETs, it was shown that trap-assisted tunneling from bulk semiconductor traps has a small impact on overall TFET I-V characteristics. The influence from trap-assisted tunneling can be further suppressed by reducing the device

thickness to 5nm [86]. These experimental results from other material systems are consistent with our study in the hetero-junction TFET instance, in that the trap-assisted tunneling current does not significantly alter the subthreshold slope when there is sufficiently large on-state current; instead, it elevates the OFF-current floor. In addition to the TAT, traps can degrade the gate efficiency as in a standard MOSFET, by electrostatically shielding the gate potential from the channel. This is often considered to be a significant degradation factor for subthreshold swing [82], [86].

Besides the trap-assisted tunneling, band tail effects from other mechanisms could also degrade the sub-threshold slope. Although there have been a variety of studies describing band tails from heavy doping and from electron-phonon interactions [87], [88], their effect on the TFET characteristics remains to be studied both theoretically and experimentally and is beyond the scope of this paper.

3.6 Conclusion

In this paper, the effects of temperature on band-to-band tunneling mechanisms in a TFET have been described. The overall variation of current with temperature is dramatically lower than that of conventional MOSFETs. Moreover, there are design opportunities for further reduction of the temperature dependence of threshold voltage and of current at a given V_{gs} by device thickness and source doping. It is noted that for a thin body semiconductor (either double-gate or nanowire structure), the extra effect of quantum confinement on threshold voltage will counteract that of band gap shrinkage as

temperature increases. This provides an opportunity to optimize the threshold voltage-temperature dependence by tuning device thickness while still maintain a high ON-current by optimizing the source doping. Trap-assisted tunneling, an extrinsic temperature dependent effect originating from trap states, is also discussed. It mainly affects off-current leakage floor and does not affect the subthreshold slope in heterojunction TFET when I_{ON} is of order of magnitude $10\mu A/\mu m$ or above. Suppressing the trap density by reduced lattice mismatch and better dielectric growth technique could further bring down this effect.

3.7 Future Work

The temperature dependence observed in SS region experimentally for TFET usually extends from sub-threshold region to ON state, which is not observed in TAT simulation. In [89], the charging of traps is shown pulsed I-V measurement to be one of the degradation source for sub-threshold swing. A model to describe the temperature dependence of time constants for these traps could be developed and examined by experimental results in the future work.

3.8 Acknowledgment

Chapter 3, in full, is a reprint of the material as it appears in J. Electron Dev. Soc. **J. Min**, L. Wang, J. Wu, P. M. Asbeck, “Analysis of Temperature Dependent Effects on

I-V Characteristics of Heterostructure Tunnel Field Effect Transistors", *J. Electron Dev. Soc.*, vol.4, no.6, pp.416-423, 2016. The dissertation author was the primary author of the paper.

Chapter 4

Noise modeling of DG-TFET

In this chapter, an analysis and simulation approach is presented for the electrical noise generated by GaSb/InAs Heterojunction Tunneling FETs. Noise models are developed for both the tunneling junction between source and channel, and for the intrinsic channel region. The noise contributions from these regions are combined by using the impedance field method. High frequency (white) noise is considered as well as low frequency contributions associated with $1/f$ noise effects. Detailed simulations are carried out for a double gate tunneling field effect transistor where both tunneling and drift/diffusion transport are considered. It is shown that in the white noise regime, shot noise is suppressed due to the presence of drift/diffusion mechanism; comparisons are made with expectations for very short channel lengths. At low frequencies, mobility fluctuations are dominant in the linear region of device operation, while in the saturation region, carrier number fluctuations dominate.

4.1 Introduction

Tunnel FETs are under widespread development for low power integrated circuit applications [90]–[95]. They are projected to have very sharp subthreshold slopes (much less than 60 mV/decade variation), provide high values of transconductance g_m and g_m/I_{ds} at low values of drain current I_{ds}, and enable high performance operation at low values of drain-source voltage V_{ds}. It is projected that digital circuits implemented with TFETs will exhibit high performance with power supply voltages as low as 0.2-0.3V [90]. TFETs have also been projected to provide performance advantages over Si CMOSFETs in analog, microwave and mm-wave applications [96], [97]. A major consideration in such applications is the noise performance of the devices. The development of noise models is thus necessary to project the potential of the technology.

For devices operating at high frequencies, white noise predominates. The white noise of a tunneling device, such as tunneling diode, stems largely from the ballistic-like behavior of the tunneling process and can be modeled as shot noise [98]. Channel noise in FETs, in contrast, is typically regarded as thermally-induced diffusion noise in the white noise regime for long channel devices. The low frequency noise, which is usually identified as flicker noise, contributes little directly at high frequency due to its $1/f$ roll-off. However, in a variety of non-linear circuit applications including oscillators, mixers, and many power amplifiers, low frequency noise gets up-converted to the RF regime and contributes to degrading the circuit noise performance.

The modeling and measurement of tunnel FET noise has been recently reported

by Pandey et. al [99]. In their work, random telegraph noise, white noise and flicker noise from the tunnel junction have been evaluated and compared in detail with noise from Si finFETs. However, a full noise model enabling the quantitative estimation of the contribution of noise originating from both the tunnel junction and from the intrinsic channel has been lacking.

This paper presents a methodology for the analysis of both white and low frequency noise contributions in the TFETs. The impedance field method is developed for TFETs and used to combine the distinct noise contributions. Detailed numerical simulations are provided for a specific TFET device example, a GaSb/InAs heterostructure TFET, comprising a source-channel tunneling junction between GaSb and InAs, together with InAs-based channel and drain regions. For short gate length FETs, electron transport in the channel can be largely ballistic. In this paper, we additionally focus on devices with longer channel lengths, so that diffusion processes in the channel must also be considered. For low frequency noise, consideration is given to both mobility fluctuations, and the effects of charge exchange between the channel and states at the channel dielectric interface and in the bulk of the gate dielectric (oxide traps). It is found in the white noise calculation that the shot noise is partially suppressed in the presence of scattering events in the channel. For flicker noise, contribution comes predominantly from near the tunnel junction rather than across the channel in MOSFET case. The calculated values of S_{id}/I_{ds}^2 are proportional to g_m^2/Ids^2 (as expected for only number carrier fluctuation) as occurs for MOSFETs [100]. On the other hand, mobility fluctuation predominates in linear region.

The structure of the paper is as follows. In section II, structure and simulated I-V

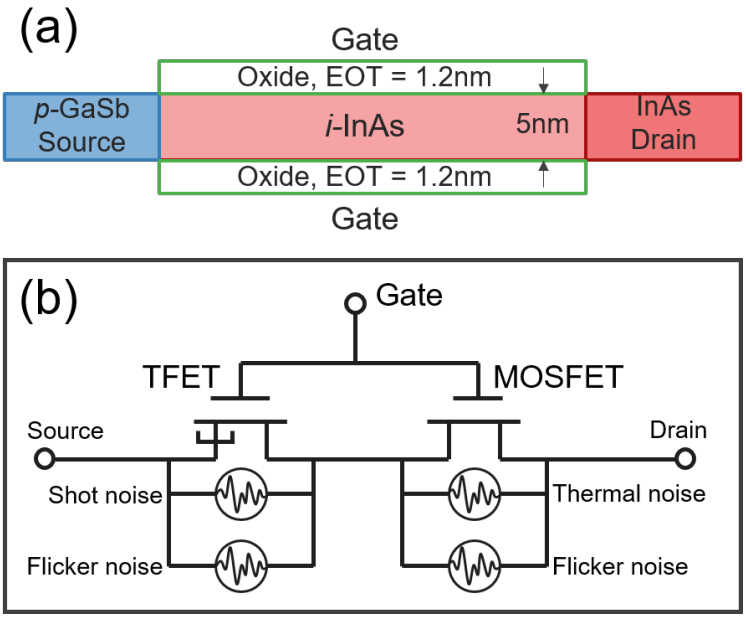

Figure 4.1: (a) Simulated structure for double gate heterostructure tunnel FET with p+ GaSb ($4 \times 10^{19} cm^{-3}$) as source and n+ InAs ($4 \times 10^{17} cm^{-3}$) as drain. The channel is intrinsic InAs, covered with 2.5 nm oxide with relative permittivity of 19.5 (EOT = 0.5nm). The device is 100 nm long and 5 nm thick if not specified. (b) Schematic circuit diagram of double gate tunnel FET with current fluctuation noise sources. The TFET component indicates the tunneling mechanisms of the electrons from source to the channel; the MOSFET component depicts the electrons drifting from channel region to the drain terminal afterwards. Each component consists of a frequency independent noise source and a frequency dependent one (flicker noise is exemplified here).

characteristics of the HTFET is first shown. Then, the methodology to calculate white noise by evaluating shot noise, thermal noise and impedance field is presented, followed by the noise characteristics for the HTFET simulated. In section IV, the methodology to evaluate flicker noise and its simulation results are detailed. Finally, conclusions are drawn in section VI.

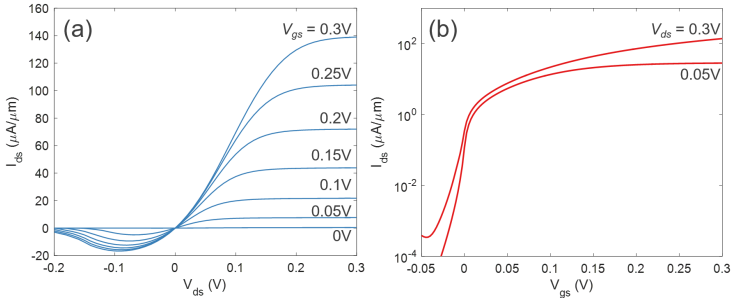

Figure 4.2: (a) Simulated results for $I_{ds} - V_{ds}$ characteristics and (b) simulated results for $I_{ds} - V_{gs}$ characteristics of a 40-nm double gate tunnel FET with channel mobility of 2000 cm^2/Vs

4.2 Structure and I-V Characteristics

To evaluate the noise performance with both mechanisms taken into account, the double gate structure depicted in Fig. 4.1(a) is simulated in Sentaurus. In this device, heavily p-type doped ($N_A = 4 \times 10^{19} cm^{-3}$) GaSb serves as source and InAs serves as n-type doped ($N_D = 2 * 10^{17} cm^{-3}$) drain and intrinsic channel. The effective oxide thickness (EOT) is set to 0.5nm, and the device thickness is 5nm. The bandgap of GaSb is 0.726 eV in bulk material, but for a device with 5nm thickness, the bandgap increased to 0.845 eV to account for lateral mode quantization. Similarly the 0.35 eV bandgap of InAs has been increased to 0.49 eV to account for the quantization effect. Sentaurus is used to simulate such device with non-local band-to-band tunneling physics and drift-diffusion physics turned on. A mobility of $2000 cm^2/Vs$ is assumed for the channel region of InAs. The I-V characteristics calculated from Sentaurus are then fitted by a serially connected TFET and FET components using ADS as depicted in Fig. 4.1(b), where TFET component is modeled by semi-empirical Notre Dame model [101] and FET component by analytic double gate 2D-FET model [102], [103]. The IV characteristics

generated by Sentaurus are illustrated in Fig. 4.2.

The noise performances are then evaluated by simplifying the physical model into a compact circuit model with two serially connected components, a tunneling FET component and a MOSFET component, each having its own noise sources. The equivalent circuit schematic of a double gate tunnel FET (TFET) is pictured in Fig. 4.1(b). This circuit is implemented in Verilog-A; numerical computations are done with a circuit simulator (ADS). Each component consists of one white noise source and one flicker noise source which can be analyzed individually before summing to obtain the overall result.

4.3 White Noise Calculation

An extensive study of tunnel FET noise modeling has been reported by Pandey et al [99]. Here, the noise contribution is considered purely from the tunneling mechanism. Thus, the analytic noise models adopted are based on pure shot noise for frequency independent noise and on Kane's model for frequency dependent noise. However, for representative TFETs, in addition to tunneling and ballistic transport, drift-diffusion mechanisms may also play an important role in TFET conduction. Due to the significant difference in conduction mechanisms, the formulations of white noise are different. The ballistic transport nature of tunneling leads to a shot noise, while that of drift-diffusion transport is better expressed as thermal noise in equilibrium state.

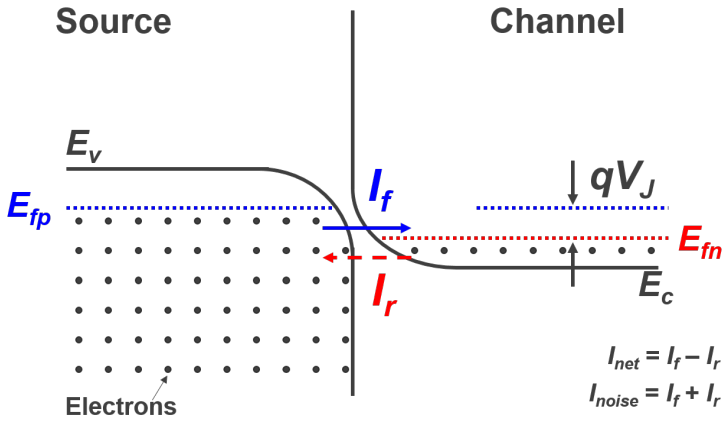

Figure 4.3: Schematic diagram shows the forward (blue solid arrow) and reverse tunneling (red dashed arrow) electrons. The net tunneling current is the subtraction of these two tunneling components ($Ids = If - Ir$), while the total noise is calculated by the addition of these two: $S_{id}^{shot} = 2q(I_f + I_r)\Delta f$. The junction voltage V_J is defined as the quasi-Fermi potential difference between source and channel.

4.3.1 Shot noise at tunnel junction

Shot noise can describe the statistical fluctuation of current associated with ballistic transport such as electron emission in Vacuum Tubes [104], ballistic FET [105] as well as tunneling junctions [98]. Shot noise occurs for charges arriving at a given terminal in packets of a fixed size q, with random arrival times that are independent of one another. The power spectral density of shot noise is frequently written as:

$$S_{id}^{shot} = 2qI_{DC} \tag{4.1}$$

Here I_{DC} denotes the average number of electrons reaching the terminal per unit time, usually associated with "DC current". I_{DC}, however, only accounts for unidirectional transport toward the terminal. If there is forward current I_f and reverse current

I_r, the DC or net current is the difference $I_f - I_r$, while their noise contributions are additive. Fig. 4.3, for example, shows the situation where both forward tunneling (indicated as blue arrow) and reverse tunneling (indicated as red arrow) events exist simultaneously. To evaluate the total shot noise, one first write down the current expressions for forward and reverse tunneling [98]:

$$I_f \propto \int_{E_c}^{E_v} f_v(E)\rho_v(E)T_{v\longrightarrow c}(1-f_c(E))\rho_c(E)dE \tag{4.2}$$

$$I_r \propto \int_{E_c}^{E_v} f_c(E)\rho_c(E)T_{c\longrightarrow v}(1-f_v(E))\rho_v(E)dE \tag{4.3}$$

The terms $f_v(E)$ and $f_c(E)$ are occupancy probability in valence and conduction band respectively; $\rho_v(E)$ and $\rho_c(E)$ are density of states in the two sides; $T_{c\leftarrow v}$ and $T_{v\leftarrow c}$ are transition probabilities between conduction and valence band and are assumed identical. When there is junction voltage V_J between the two terminals, $qV_J = E_{fv} - E_{fc}$, a simple relation between $f_c(E)(1-f_v(E))$ and $fv(E)*(1-fc(E))$ can be derived readily:

$$(1-f_c(E,E_{fc}))f_v(E,E_{fv}) = (1-f_v(E,E_{fv}))f_c(E,E_{fc})e^{qV_J/kT} \tag{4.4}$$

Since $exp(qV_J/kT)$ is independent of energy, it can be factored out of the integral to relate forward current density to reverse current density:

$$I_f = e^{qV_J/kT} \times I_r \tag{4.5}$$

The net current is thus:

$$I_{net} = I_f - I_r = (e^{qV_J/kT} - 1) \times I_r \tag{4.6}$$

The total current noise spectral density, on the other hand, is given by the sum of forward and reverse current contributions:

$$S_{id}^{shot} = 2q(I_f + I_r) = 2q(e^{qV_J/kT} - 1) \times I_r \tag{4.7}$$

It follows that

$$\frac{S_{id}^{shot}}{I_{net}} = 2q\frac{e^{qV_J/kT} + 1}{e^{qV_J/kT} - 1} = 2q\coth\frac{qV_J}{2kT} \tag{4.8}$$

For very low bias conditions ($V_J << 2kT/q$), $coth(qV_J/2kT)\ 2kT/qV_J$. This leads to the expression of thermal noise in an equilibrium state:

$$\frac{S_{id}^{shot}}{W} \approx 2qI_{net} \times \frac{2kT}{qV_J}\Delta f = 4kTG_{eff}\Delta f \tag{4.9}$$

4.3.2 Thermal noise in the channel

Thermal noise expression is valid when the device is in a quasi-thermal equilibrium state. In other words, drift-diffusion model is assumed. In general, shot noise is suppressed because the arrival times of different charge packets are no longer independent events [105]. Rather, by Coulomb interactions, Pauli Exclusion Principle or other interactions, the arrival of one electron into the channel from the source influences the

arrival of future electrons.

As the device length shrinks below carrier mean free path, the transport physics will shift from drift-diffusion to quasi-ballistic (countable scattering events) and finally to ballistic transport (no scattering). During this shift, the noise expression will also shift from thermal noise to shot noise.

The white noise in the channel is modeled directly using the thermal noise in MOSFET, whose expression is widely known as:

$$\frac{S_{id}^{thermal}}{W} = \frac{4kT\mu}{L^2}\int_0^L Q(x)dx\Delta f \tag{4.10}$$

The thermal noise of the MOSFET is proportional to the total charge inside the channel.

4.3.3 Impedance field method for white noise

The general framework of electrical noise analysis was first established by Shockley et. al and introduced as the impedance field method [106] which was then elaborated for a variety of semiconductor devices [107]. Firstly, noise sources (thermal noise, shot noise, generation/recombination noise, flicker noise) are evaluated on a mesoscopic level at each position in the device and are assumed to be independent. Then, each noise source at a given position is considered as a (small signal) Langevin force driving a noiseless PDE-based semiconductor model [107]. The induced fluctuations at the device terminals are then calculated. For a Langevin force chosen to be current, and the drain terminal

response chosen to be open circuit voltage, the position-dependent ratio between the two is termed "impedance field", which serves as a gain factor to relate each localized noise source to the drain terminal response. The method can be extended to other types of inputs and outputs, and the gain factor (corresponding to the "impedance field") is translated to different units. For example, if the Langevin force is chosen to be current, and the drain terminal response is chosen to be short circuit current, the gain factor becomes unitless.

For a MOSFET, the complicated PDE problem can be simplified to a 1-D conduction problem. If we are interested in the drain current fluctuation due to a current fluctuation in the channel, the impedance field reduces to a dimensionless current gain, and noise can be calculated in a circuit model approach [108].

To calculate respective contributions from the TFET and MOSFET components of the present device, a circuit model approach of impedance field method is applied here. Suppose the current expressions for TFET and MOSFET components are $I_{tun}(V_{gs}, V_{ds})$ and $I_{FET}(V_{gs}, V_{ds})$ respectively. At the junction where TFET and FET interconnect, a fluctuation of voltage will induce fluctuations of current density for both components in small signal regime. The small signal resistance values for the two components due to single interconnect voltage fluctuation can be expressed as:

$$r_{FET} = [\partial I_{FET}(V_{gs}, V_{ds})/\partial V_s]^{-1} \tag{4.11}$$

$$r_{tun} = [\partial I_{tun}(V_{gs}, V_{ds})/\partial V_d]^{-1} \tag{4.12}$$

It is worth noting that the small signal resistance value for TFET is due to the TFET drain terminal voltage fluctuation, while that for FET is due to FET source terminal voltage fluctuation because TFET drain terminal connects FET source terminal.

The appropriate resistance in the case of the TFET is calculated here using an analytic semi-empirical equation, after the analytic model is fitted to Sentaurus TCAD numerical results.

The appropriate resistance for the FET component can be calculated by solving the carrier charge density at the FET source terminal. In a charge based FET model, the current is proportional to the integration of charge throughout the channel with respect to quasi-fermi level:

$$I_{FET} = \frac{1}{L}\int_{V_s}^{V_d} \mu Q(V, V_{gs}) dV \tag{4.13}$$

Therefore, small signal resistance with respect to source terminal voltage, denoted as r_{FET} in the following context, can be simplified to:

$$r_{FET} = \left(\frac{\partial I_{FET}}{\partial V_s}\right)^{-1} = \frac{L}{\mu Q(V_s, V_g)} \tag{4.14}$$

Both r_{FET} and r_{TFET} are essential in calculating the current gain (namely impedance field) from noise source to drain terminal. For instance, to calculate the contribution of TFET shot noise contribution at the drain terminal, the shot noise current will encounter the TFET and FET component parallel connected assuming drain and source terminal are AC grounded. The noise current induces a voltage fluctuation at the interconnection, and ramifies into the two components according to the small signal resistance values as

calculated. The shot noise current flowing into drain terminal is attributed to that flowing into the FET component. Henceforth, the current fluctuation due to shot noise is:

$$\tilde{i}^{tun} = \frac{r_{tun}}{r_{tun} + r_{FET}} \tilde{i}^{shot} \tag{4.15}$$

The current noise spectral densities contribution from shot noise is

$$S_{id}^{tun} = \left(\frac{r_{tun}}{r_{tun} + r_{FET}} \right)^2 S_{id}^{shot} \tag{4.16}$$

Similarly, the current noise spectral density contribution from FET can be calculated in a similar manner. is the current fluctuation due to thermal noise of FET is attributed to the portion flowing into TFET component. This is because the current flowing into AC grounded drain will flow back into TFET component from AC grounded source, forming a closed circuit. The noise spectral density contribution from thermal noise is:

$$S_{id}^{FET} = \left(\frac{r_{FET}}{r_{tun} + r_{FET}} \right)^2 S_{id}^{thermal} \tag{4.17}$$

Eventually, total noise is the addition of these two contributions assuming they are independent noise sources:

$$S_{id}^{tot} = S_{id}^{tun} + S_{id}^{FET} \tag{4.18}$$

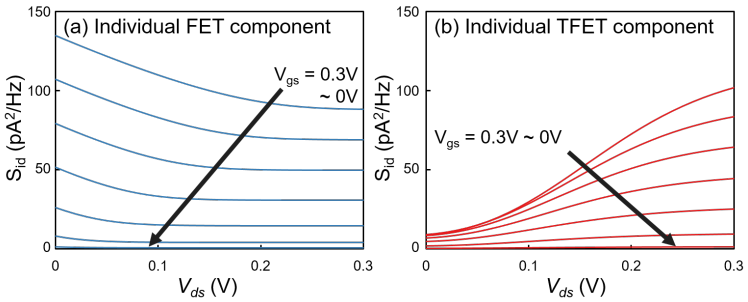

Figure 4.4: Current Noise spectral density of (a) an individual FET component and (b) an individual TFET component with same set of parameters used in the equivalent circuit with varying V_{gs} and V_{ds}.

4.3.4 Simulation Results and Discussions

White noise for a single TFET and a single FET device are evaluated individually first. As shown in Fig. 4.4(a), for a FET device with drift-diffusion physics, since the current noise spectral density is proportional to the total mobile charge within the channel, it will decreases until stabilizing to a certain level with V_{ds} increasing, indicating the depletion of carriers near drain terminal until saturation condition. On the other hand, a TFET device with tunneling physics shows an opposite trend of the spectral density with respect to V_{ds} as depicted in Fig. 4.4(b). This trend can be directly indicated from Equation 4.8 for shot noise.

Besides the noise source level, small signal resistances are necessary to evaluate the total noise for the serially connected circuit shown in Fig. 4.5. In Fig. 4.5 (a) and (b), we have shown small signal resistances for TFET component (r_{tun}) and FET component (rFET). It is noted that the resistance for r_{tun} is decreasing with V_{ds} while r_{FET} is increasing for both high and low V_{gs}. Thus, this results in an increasing trend for the scaling factor for FET noise contribution and decreasing trend for TFET noise

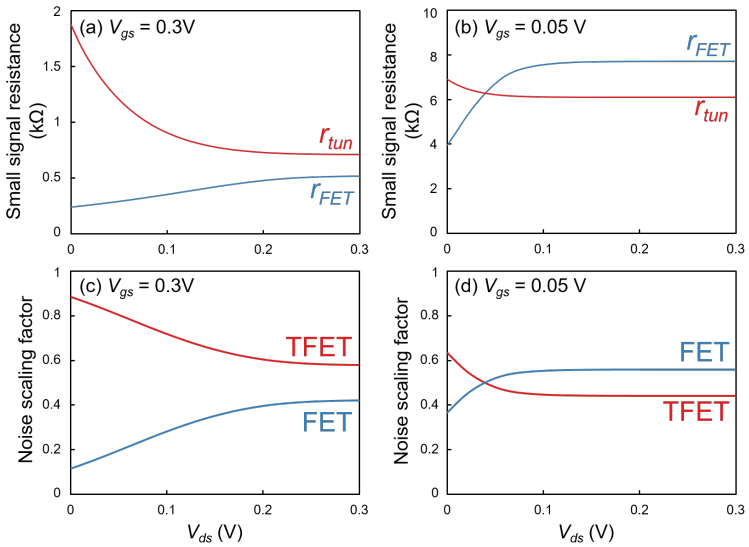

Figure 4.5: (a) and (b) Small signal resistance of FET (blue line) and tunneling component (red line) for impedance field method calculation in (a) $V_{gs} = 0.3V$ and (b) $V_{gs} = 0.05V$ (c) and (d) the calculated scaling factors for tunneling and FET component.

contribution, which is shown in Fig. 4.5 (c) and (d). It is noteworthy that the trends for source noise level are totally opposite to those for noise scaling factor.

Finally, total noise and contributions from each components are evaluated and shown in Fig. 4.6. At high V_{gs} (0.3V) condition, total noise increases with drain bias, while at low V_{gs} (0.05V) condition, the noise decreases with drain bias. In both cases, although tunneling FET component contributes more to total noise, while FET still contributes considerably. The trends for total noise are mainly determined by TFET for both cases. At high V_{gs}, the trend for TFET noise source level wins while at low V_{gs}, the trend for TFET noise scaling factor wins in the final trend of TFET noise contribution. In Fig. 4.7, calculated total noise is compared with $2qI_{ds}$ and $4kT\gamma g_m$. Shot noise suppression is observed for TFET just like in the case of a quasi-ballistic MOSFET [105].

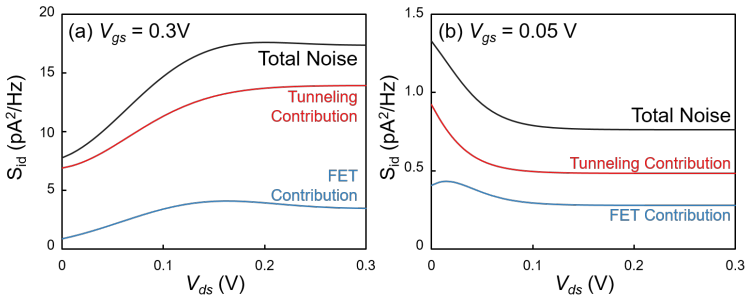

Figure 4.6: Current noise spectral density of a 100nm TFET device (black) and contributions from tunneling component (red) and FET component (blue) for (a) $V_{gs} = 0.3V$ and (b) $V_{gs} = 0.05V$

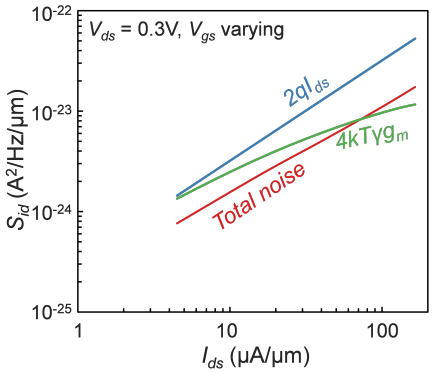

Figure 4.7: Current noise spectral density of a 100nm TFET device (red line) and its comparison with $2qI_{ds}$ (blue line) and $4kT\gamma g_m$ (green line).

4.4 Flicker Noise Calculation

4.4.1 Methodology

Low frequency noise is associated with number fluctuations and mobility fluctuations in conventional MOSFETs. In this work, we quantify these two effects in a double gate TFET by explicit simulation. Low frequency noise in a transistor is mostly due to the trapping/de-trapping of carriers between bands and trap states. For a trap state with density D_{it} and time constant τ_{it}, the number fluctuation spectral density function is a

Lorentzian function:

$$S_{\Delta N}^{it}(\omega) = \frac{2kTD_{it}\tau_{it}}{1+\omega^2\tau_{it}^2} \tag{4.19}$$

Single trap usually exists at the oxide/semiconductor interface and serves as the source of random telegraph noise (RTN) that has been observed in scaled TFET devices experimentally [92]. There are also traps in the oxide known as border traps, especially for III-V/high-k oxide interface [109], [110]. Unlike the traps at interface where electrons get trapped/de-trapped through thermal excitation, electrons tunnel into and out from the border traps and is much less temperature dependent. Assume a constant trap density N_{bt} and an exponential function of oxide depth for border traps time constants according to WKB approximation:

$$\tau(x) = \tau_0 e^{2\kappa x} \tag{4.20}$$

The term κ, namely the attenuation coefficient for electron wave function penetrating into oxide, is related to semiconductor/oxide barrier height Φ_B and effective electron mass $m^\star$ and reads

$$\kappa = \sqrt{\frac{2m^\star\Phi_B}{\hbar^2}} \tag{4.21}$$

The total noise spectral density function can therefore be summed up from a set of Lorentzian functions with varying time constants:

$$S_{\Delta N}^{1/f}(f) = \int_0^{t_{ox}} \frac{2kTN_{bt}\tau_0 e^{2\kappa x}}{1+\omega^2\tau_0^2 e^{4\kappa x}} dx\Delta f \tag{4.22}$$

The integration can be computed analytically and reads

$$\begin{aligned} S_{\Delta N}^{1/f}(f) &= \frac{2kTN_{bt}}{2\pi\kappa f}\left[\arctan(\tau_0\omega e^{2\kappa t_{ox}}) - \arctan(\tau_0\omega)\right]\Delta f \\ &= \frac{2kTN_{bt}}{4\kappa f}\Delta f \end{aligned} \tag{4.23}$$

The approximation is valid when $\omega\tau_0 << 1$. For high-k/III-V semiconductors, $\tau_0 \approx 10^{-10}s$ [110] and is well beyond the detect range of most of low frequency measurement instruments.

To relate the number fluctuation to current fluctuation in simulation, we detect the small signal response of drain current to change of fixed charges along the channel. To achieve so, a small amount of charge ΔQ is placed at the oxide/InAs interface at various positions of the channel to emulate the effect of trapping/de-trapping of electrons from oxide traps, and we calculate the resulting impact on drain current in Sentaurus. The quasi-statically calculated change of current ΔI due to this change of charge ΔQ is used to relate the fluctuations of charge at the interface with fluctuations of drain current. This can be considered as a slight modification of the impedance field method: rather than considering a fluctuation in potential at each position, we produce a fluctuation of charge, and in both cases evaluate the current at the drain terminal. Therefore, the flicker noise can be calculated by summing all the contributions from traps along the channel:

$$S_{id}^{1/f}(f) = \sum_{traps}\left(\frac{dI}{dN}\right)^2 S_{\Delta N}^{1/f} \tag{4.24}$$

In conventional short channel MOSFETs, mobility fluctuations additionally

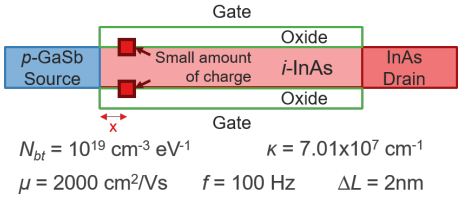

Figure 4.8: Schematic diagram of flicker noise calculation using Sentaurus device simulator. An oxide trap density of $10^{19} cm^{-3} eV^{-1}$ is assumed for noise level estimation

contribute to flicker noise [111]. The mobility fluctuations are mainly caused by the scattering mechanism from charges within the oxide. A unified expression that describes both number and mobility fluctuation has been developed [111] given by $[I_d(1/N(x)+\alpha\mu)]^2 S_{\Delta Nt}(x,f)$, where α is called the scattering coefficient that describes the mobility degradation with respect to charged oxide trap density. Mobility fluctuation term is also considered in this TFET flicker noise calculation when carrier concentrations are too high for number fluctuation to impact in linear region. An additional term $(1+\alpha\mu N(x))^2$ is added to the flicker noise calculation equation and written as:

$$S_{id}^{1/f-mob}(f) = \sum_{traps} \left[\frac{dI}{dN}(1+\alpha\mu N(x))\right]^2 S_{\Delta N}^{1/f} \tag{4.25}$$

The scattering coefficient α is estimated based on the simple equation derived by Ning and Sah [112] as $\alpha = \pi m_e q^3/16\varepsilon_{av}^2 hkT = 6\times10^{-16} Vs$.

In Fig. 4.8, a schematic diagram and parameters for simulations are illustrated. A border trap density of $10^{19}/cm^3/eV$ is assumed for the InAs/high-k oxide, which is a reasonable guess as indicated in [109], where an oxide trap density of $4.5\times10^{19} cm^{-3} eV^{-1}$ is extracted experimentally from InGaAs/Al_2O_3 MOS capacitor structure. The term κ,

namely the attenuation coefficient for electron wave function penetrating into oxide, is set to be $7.01 \times 10^7 cm^{-1}$ by assuming a barrier height of 3.7eV and effective electron mass in oxide as $0.5m_0$, close to what was reported in [113]. A typical mobility of $2000cm^2/Vs$ is assumed for InAs for this simulation. The frequency simulated is 100Hz.

4.4.2 Simulation Results Discussions

The flicker noise contribution along channel, ΔS_{id} is evaluated. Fig. 4.9 (a) indicates the significance of tunnel junction for flicker noise contribution. In both linear region and saturation region, the noise contributions that are 10 nm around tunnel junction are one to three orders of magnitude higher than those into the channel. This is mainly due to the drastic potential drop around tunnel junction [114], [115]. Furthermore, mobility fluctuation increases the noise characteristics in linear region by over 2 orders of magnitude, as opposed to less than 1 order of magnitude change in saturation region. This is derived from the difference of mobility fluctuation factor, $\alpha\mu N(x)$. In saturation region, channel is depleted of electrons and the mobility fluctuation is greatly suppressed. In linear region, on the other hand, electrons accumulate across the channel and increase the factor up to 10. The total flicker noise performances are calculated for varying bias conditions and are plotted in Fig. 4.9 (b). It is noteworthy that mobility fluctuation has become a main contributor in linear region as gate bias increases, canceling the decaying effect of number fluctuation when electrons are accumulated.

Fig. 4.10 illustrates the correlation between g_m^2/I_{ds}^2 and S_{id}/I_{ds}^2 for TFET.The agreement of these two physical quantities in the trend of change is also observed in

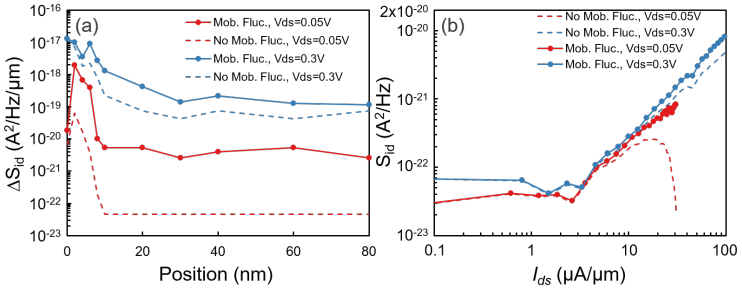

Figure 4.9: (a) Flicker noise contribution versus position in linear region and saturation region with and without mobility fluctuation factor considered. (b) Total flicker noise at drain terminal versus I_{ds} in linear region and saturation region with and without mobility fluctuation factor.

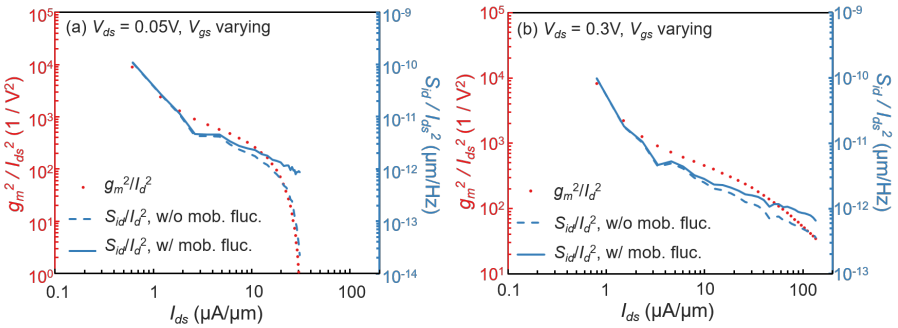

Figure 4.10: S_{id}/I_{ds}^2 (blue dashed for results without mobility fluctuation; blue solid lines for those with mobility fluctuation) and g_m^2/I_{ds}^2 (red dots) plotted on the same figure for (a) V_{ds} = 0.05V and (b) V_{ds} = 0.3V

MOSFET when carrier number fluctuation is dominating [100]. The correlation between gm and S_{id} may come from the effective capacitance between the trap states and gate terminal: $S_{id} = (dI_{ds}/dQ)2 * S_{\Delta N} = (dI_{ds}/dV_{gs})^2 * (dV_{gs}/dQ)^2 * S_{\Delta N} = (g_m/C_{eff})^2 * S_{\Delta N}$.

4.5 Discussion and Conclusion

In this paper, impedance field method has been developed for both white noise and flicker noise calculation, allowing straightforward evaluation of contributions from

different regions of the device.

For white noise calculation, an opposite trend of shot noise source characteristics against thermal noise source is eminent because of the increasing trend of current density for shot noise calculation and depletion of mobile carriers for thermal noise calculation. On the other hand, the small signal resistances trend used in impedance field method are also opposite: a decreasing trend of small signal resistance for tunnel component versus an increasing one for FET component with respect to drain bias. In this paper, a mobility of $2000 cm^2/Vs$ and a channel length of 100 nm TFET shows a non-trivial contribution from drift-diffusion in noise performance. The total noise trend is still dominated by tunneling and depends on noise source trend and small signal resistance trend. It is expected that if mobility is lower or channel length is even longer, thermal noise may dominate the total noise and a different characteristics from this paper is expected. In that case, however, TFET is not practical for high performance applications and thus is not discussed in detail.

Flicker noise is calculated in a different manner compared to white noise calculation. Again, tunnel region has contributed most to total flicker noise in both linear and saturation region. Especially, in linear region, the drop of number fluctuation effect is counteracted by mobility fluctuation effect. A strong correlation between flicker noise and current density is observed.

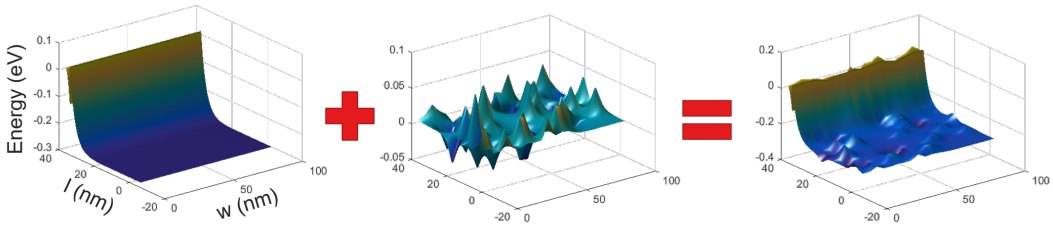

Figure 4.11: Addition of double gate analytic TFET potential profile in ON-state and potential fluctuations due to 40 traps results in a ”perturbed” potential profile for further current calculation.

4.6 Future Work

In the future, noise model proposed in this section could be improved as follows. For white noise, quasi-ballistic regime should be considered for MOSFET component when gate length is comparable to carrier mean free path of the semiconductor. Besides, the noise is no longer localized as in drift-diffusion regime and will converge to shot noise as gate lengths become smaller. A compact model to describe current and white noise characteristics of double-gate TFET with quasi-ballistic transport incorporated is then desired for circuit design purposes.

The frequency dependent noise, namely flicker noise (1/f) and random telegraph noise (RTN), can be further studied in terms of statistical model considering the randomness in position and number of the traps. In a highly scaled device, random telegraph noise (RTN) is more likely to be observed, and variations in performance among devices are much larger compared to a large device. To model a histogram of current densities using a vast number of devices with various trap configurations, an efficient physical model as described in Chapter 2 combined with a random trap generator could be an

option. The analytic potential profile at a certain bias condition could first be modified by a configuration of traps as illustrated for example, in Fig. 4.11. Then, current densities are calculated based on these ”perturbed” potential profiles. This methodology for noise and variation study could be further extended to single-trap (RTN analysis) and nanowire TFET case.

4.7 Acknowledgment

Chapter 4, in full, is a reprint of the publication to be submitted. **J. Min**, P.M.Asbeck, “Noise modeling and simulation of GaSb/InAs heterojunction tunneling field effect transistors with the impedance field method”, prepared for submission. The dissertation author was the primary author of the paper.

Chapter 5

Compact Modeling of Vertical TFET with Distributed Physics

In this chapter, distributed effects along the channel are investigated for 2-dimensional vertical tunnel FETs by developing a model based on a succession of unit cells along the channel, each of which includes lateral FET conduction and vertical tunnel conduction components. The distributed model shows that there are trade-offs between these two conduction mechanisms in both DC and RF characteristics. At DC, the overall device current is often limited by one of the two mechanisms, which is lateral conduction for many of the examples discussed in this paper. Channel length has opposite effects on current from the two mechanisms, so that ON-state current can typically be optimized by proper choice of channel length. Tunneling current density is highly nonuniform along the channel for long channel length. For RF applications, lateral conduction limitations increase the total input capacitance, particularly C_{gd}, and

can lead to capacitance peaking at specific bias voltages near device turn-on. Unlike lateral TFET design, scaling down the channel length significantly improves the cut-off frequency. The distributed model is implemented in Verilog-A and is directly useful for circuit simulations. Parasitic capacitances and contact resistances are also taken into account when evaluating RF characteristics for practical design purposes.

5.1 Introduction

Tunnel FETs have become candidates for low power, high frequency integrated electronic applications because of their potential for steep subthreshold slope (SS) and high transconductance at low voltage supplies [116]–[121]. They can be implemented with largely depleted channels in the saturation region of their $I_{ds} - V_{ds}$ curves, leading to low gate capacitance which is favorable for high frequency operation. In the conventional lateral tunneling structure, pictured in Fig.5.1(a), it is necessary to use thin channels in order to allow gate control over the full width of the channel. Thin channels also mitigate short channel effects by shielding the source junction from the drain voltage. However, thin channels also decrease the area available for tunneling current flow and thus the maximum current available. From the standpoint of fabrication, the lateral FET structure is typically achieved either by growing nanowires, or etching epi-layers into narrow pillars. The former method usually requires accurate metal deposition for gate and drain, while the latter often suffers from poor quality at the interfaces where etching occurred.

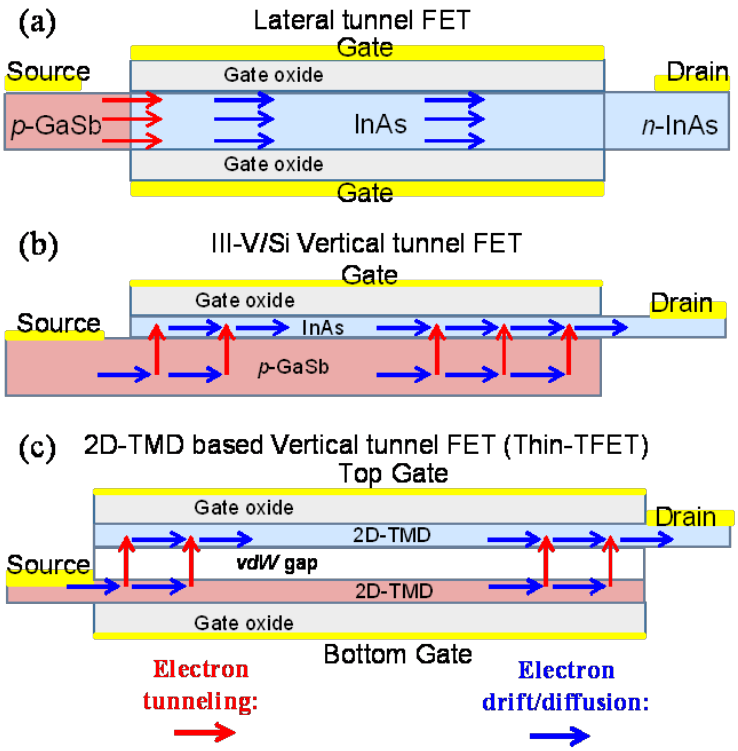

Figure 5.1: Structures and electron flow patterns of (a) lateral tunnel FET, (b) vertical tunnel FET with III/V materials or Si and (c) vertical tunnel FET with 2D-TMD materials. Red arrows represent electron tunneling current flow; blue arrows represent electron drift/diffusion current flow.

To cope with these issues, vertical tunneling FET structures, as pictured in Fig.5.1(b) and (c), have been proposed by several groups. For example, Xing's group has proposed the Thin-TFET modeled both physically [122] and using a neural network methodology [123]. It is composed of two transition metal di-chalcogenide (TMD) materials layered as a stack. The van der Waal's gap between the two layers serves as tunneling gap when the two layers are biased properly. Such structures have been experimentally tested as tunneling diodes by several groups [124], [125] and shown to have band-to-band tunneling characteristics. An electrically controlled carrier density in the source region could avoid dopant-induced band tails, enhancing the steep slope

characteristics of the device. Additionally, better electro-statics could be achieved in the vertical tunnel structure due to high gate efficiency to all controlled regions, as opposed to the lateral tunneling case where the middle of the channel has reduced gate control. Finally, no etching process is required at the tunneling junction, where process-induced defects could deteriorate the device performance. III-V and silicon/germanium based materials, which have more mature epi-growth techniques, have also been proposed for fabricating similar structures based on vertical tunneling [126]–[128]. Additional combinations of materials have also been demonstrated; for example in [129] germanium serves as the source layer and a 2D-layer of MoS_2 serves as the drain layer.

A significant consideration for vertical tunneling FETs is that the overall tunnel current tends to increase as the channel length is increased, because of the increased area available for tunneling. However, this paper shows that the lateral resistance in the drain layer and related voltage drops associated with the lateral conduction can limit the overall current for long channel lengths. In the saturation region, the drain layer of device becomes depleted of carriers, which results in a high lateral resistance; voltage along the drain layer then changes rapidly, which causes highly non-uniform tunneling current. In such a case, the assumption of uniform potential across the layer is not valid and leads to overestimates of the current density. The distributed effects introduce a complex dependence of ON-state current on channel length. The channel charging/discharging process also strongly depends on the channel carrier concentration profile and the extra resistive component due to lateral conduction. As a result, the RF characteristics are also strongly affected by device dimension. Under conditions when the channel carriers are

strongly accumulated before tunneling turn-on, a Miller effect intrinsic to the device can be observed. This paper presents a distributed model that can describe the non-uniformity of potential and tunneling current along the channel, which allows investigation of the joint effects of the vertical and horizontal limits on current flow. The model equations have been implemented in Verilog-A by using a set of serially connected unit elements to allow evaluating device and circuit performance with standard circuit simulators. Key results stemming from the distributed effects on DC, AC and RF characteristics are discussed in this paper.

This chapter proposes a compact model in Verilog-A which is compatible with circuit simulators by using a set of serially connected unit elements. The effect of lateral conduction is thus discussed in DC, AC and RF characteristics. To begin with, the device structure and equivalent circuit model is proposed followed by a detailed modeling on vertical and lateral conduction component.

5.2 Device Structure and Model Setup

The operation of an n-type vertical TFET can be described briefly as follows. As the top gate bias increases towards positive values, a tunneling window starts to open between the p-type source layer and the drain layer, and electrons begin to tunnel from source valence band to drain conduction band. In the linear region (when V_{ds} is small), only a small potential drop is expected from source terminal to drain terminal across the drain layer, since lateral conduction proceeds readily in the drain layer, which has

abundant carriers; as a result, the tunneling current density is relatively uniform along the channel. As the value of V_{ds} is increased, there is progressively more voltage drop across the drain layer associated with current flow from source to drain in the drain layer, due to limited lateral channel conduction. This changes the profile of tunneling current density along the channel, leading in general to significant non-uniformity.

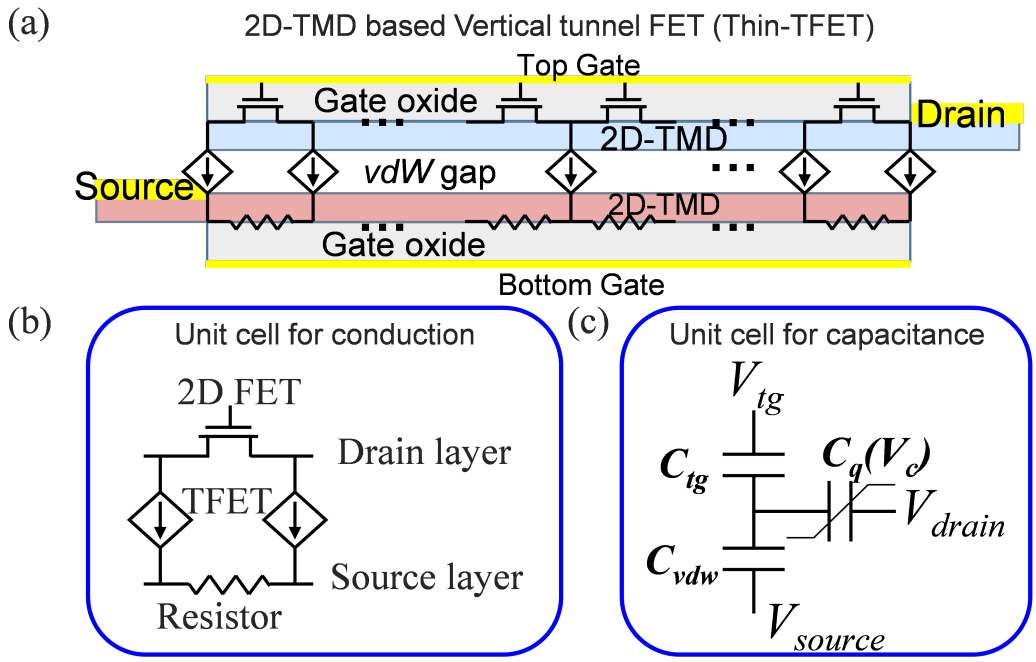

Figure 5.2: (a) Device structure and distributed circuit elements for a representative vertical tunnel FET. (b) Unit cells to model vertical and lateral conduction. Note that the tunneling component is also controlled by the gate of the 2D FET. (c) Unit cell to model small signal capacitance; quantum capacitance C_q is a nonlinear capacitor.

In the saturation region (high values of V_{ds}), the region of drain layer near the drain terminal becomes depleted, leading to more vacant conduction band states for tunneling from the source layer. The lateral FET starts to operate in saturation condition. The drain layer near source terminal is not depleted, however, and as a result, the tunneling current density near the source will be lower than near the drain terminal.

A distributed circuit is used to emulate the coupled conduction mechanisms, as shown in Fig.5.2(a). Each unit cell consists of lateral conduction modeled by FETs (for drain layers) and resistors (for source layers), and vertical tunneling between drain and source layer, modeled by a tunnel FET illustrated in Fig.5.2(b). Fig.5.2(c) shows a capacitive network unit cell which is connected to both sides of the unit element to emulate the distributed charge densities of the full device. Models for the unit components are described in the following sections.

5.2.1 Lateral conduction: Compact 2D FET model

To start with, 2D FET model, which governs the conduction in the lateral direction of drain layer is introduced. An analytic 2D-FET model is used to describe lateral conduction in the drain layer [130], [131] based on drift-diffusion mechanisms. It assumes quasi-equilibrium for carriers and validity of Fermi-Dirac statistics. A schematic diagram of a 2D FET structure with top and bottom gate is illustrated in Fig.5.3. Taking n-type material as an example, the equations that describe the electrostatics is as follows:

$$f_{c0} = \frac{1}{1 + e^{(-qVc - E0)/kT}} \tag{5.1}$$

$$Q_n = qD_0kT * ln(1 - f_{c0}) \tag{5.2}$$

$$C_q = -\frac{dQ_n}{dVc} = q^2 D_0 f_{c0} \tag{5.3}$$

$$V_p = \frac{Q_n}{C_T + C_B} - Vc + \frac{C_T(V_{gs} - V_{gs0})}{C_T + C_B} + \frac{C_B(V_{bs} - V_{bs0})}{C_T + C_B} \tag{5.4}$$

$$\frac{dV_p}{dV_c} = -(1 + \frac{C_q}{C_T + C_B}) \tag{5.5}$$

With the electrostatics, and assuming drift-diffusion physics without velocity saturation and CLM physics, the current could be expressed as the gradient of quasi-Fermi level. Finally, by integration with respect to position along the channel, the current density can be expressed by two integrations:

$$I_{DS} = -\frac{q\mu D_0 kT}{L}(\int_{V_{cd}}^{V_{cs}} ln(1 - f_{c0})dV_c + \frac{q^2 D_0}{C_T + C_B}\int_{V_{cd}}^{V_{cs}} ln(1 - f_{c0}) f_{c0} dV_c) \tag{5.6}$$

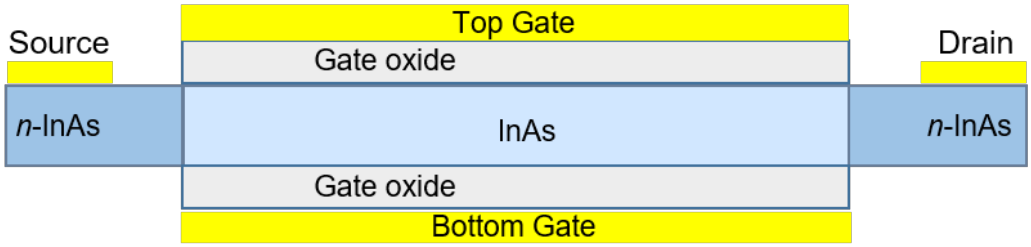

Figure 5.3: Schematic diagram of a double gate 2D-FET

The second term is closely related to drift mechanism and its integration has analytic form by manipulating the identity:

$$f_{c0}(1 - f_{c0})dV_c = \frac{kT}{q} df_{c0} \tag{5.7}$$

This term is coined as drift term K_{drift} and its final form is:

$$K_{drift} = \frac{q\mu D_0 kT}{L}\frac{q^2 D_0}{C_T + C_B}\frac{kT}{q}((ln(1 - f_{c0}(V_{cs})))^2 - (ln(1 - f_{c0}(V_{cd})))^2) \tag{5.8}$$

The first term of integration known as diffusion term K_{diff}, however, does not have analytic integration form. To cope with, a piecewise function with continuous 3rd derivative is proposed to approximate this integration. A detailed derivation and its math form is shown in the Appendix A. The form of Term1 for either v_{cs} or v_{cd} are:

$$\mu D_0 (kT)^2 \begin{cases} \frac{v_c^2+v_{c2}^2}{2} - \frac{v_{c2}^3}{3\alpha} + 2(e^{-v_{c2}} + \frac{\zeta}{4}e^{-2v_{c2}}) + \\ \quad 2v_{c2}(e^{-v_{c2}} + \frac{\zeta}{2}e^{-2v_{c2}}) + (e^{-v_c} + \frac{\zeta}{4}e^{-2v_c}) & v_c \geq v_{c2} \\ -\frac{(v_c+v_{c2})^2(-v_c+2v_{c2}-3\alpha)}{12\alpha} + \\ \quad \frac{\zeta}{4}e^{-2v_{c2}}(1+2v_c+2v_{c2}) + e^{-v_{c2}}(1+v_c+v_{c2}) & v_{c2} \geq v_c \geq -v_{c2} \\ e^{v_c} + \frac{\zeta}{4}e^{2v_c} & v_c \leq -v_{c2} \end{cases}$$

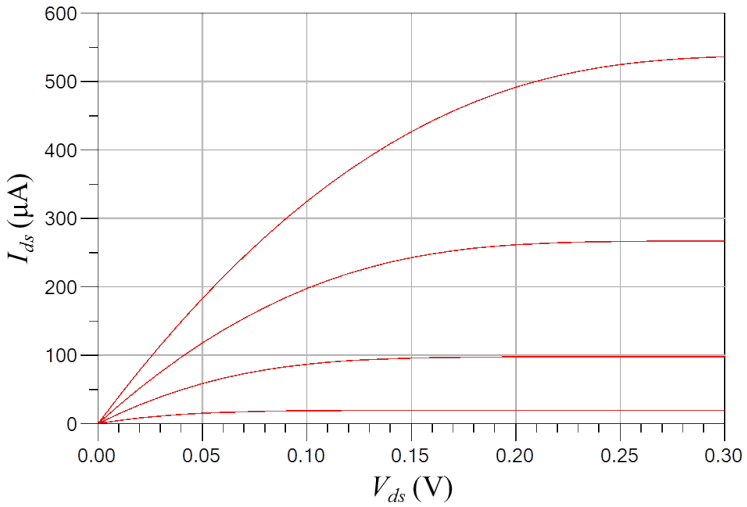

Figure 5.4: $I_{ds} - V_{ds}$ curves for a 2D-FET

The parameters are set to $v_{c2} = 0.858$, $\alpha = 2.358$ and $\zeta = -0.5896$ and is independent on device or temperature. The normalized value is $v_c = \frac{V_c}{kT/q}$ Therefore, the

current expression is:

$$I_{DS} = K_{drift} + K_{diffusion} \tag{5.9}$$

Such model is achieved in both MATLAB and Verilog-A. An example of $I_{ds} - V_{ds}$ characteristics are illustrated as in Fig.5.4.

5.2.2 Smooth Charge model

For any three terminal devices, the small signal characteristics can be fully described by a Y-matrix as:

$$Y = \begin{bmatrix} Y_{gg} & Y_{gd} \\ Y_{dg} & Y_{dd} \end{bmatrix} \tag{5.10}$$

The source side is not needed in the matrix because they are linearly dependent on the other two terminals. A conventional way of modeling small signal characteristics for FET is using an equivalent circuit. Equivalent capacitances are connected between gate and source (known as C_{gs}), and gate and drain (known as C_{gd}). It should however be distinguished from the capacitances defined from matrix elements. An equivalent circuit is intuitive and could cast physical insights. However, there are several obstacles to adopt the conventional equivalent circuit to 2D-FET:

1. DOS capacitance is non-linear, which was not considered in Si-based device due to its large effective mass. In a 2D material, DOS is limited and could thus limit the capacitance value.

2. Equivalent circuit model works perfect for small signal analysis, but is not suitable

for large signal, non-linear or transient analysis, where time-domain is more considered. Furthermore, verilog-A prefers smooth charge based model instead of capacitance based model. Such requirement allows a good convergence in time-domain analysis.

3. An accurate expression is lacking for all the small signal elements, which could be different from 3D Si-MOSFET case.

4. For a distributive TFET model we are about to model, equivalent circuit will become even complicated, and again has limited applications.

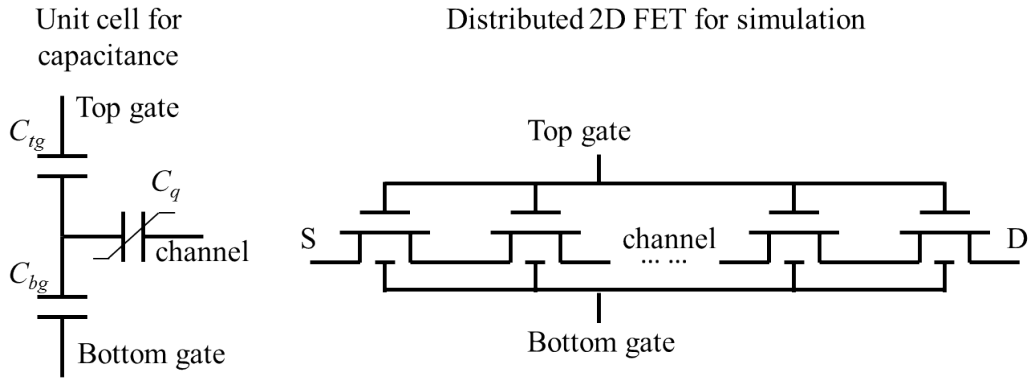

Figure 5.5: Distributed 2D FET for accurate capacitance modeling

Therefore, we determine to use a distributive charge based model, with the help of Verilog-A and ADS to simulate the small signal characteristics of the 2D FET. The charge at a certain position in the channel can be described as the equivalent circuit below. Such equivalent circuit is attached to all unit elements, with terminal 1 connected to channel, terminal 2 to top gate and terminal 3 to back gate. An example unit cell capacitance network and the distributed connection is shown in Fig.5.5.

For the unit cell, we just need to express charge for two terminals, and the rest could be obtained by charge neutrality condition. In Verilog-A code, since V_c is already obtained in current characteristics, it is not hard to express the top and back gate charge as:

$$Q_{tg} = C_{tg}(V_{tg} - V_p - V_{tg0} - V_c) \tag{5.11}$$

$$Q_{bg} = C_{tg}(V_{bg} - V_p - V_{bg0} - V_c) \tag{5.12}$$

$$Q_{ch} = -(Q_{tg} + Q_{bg}) \tag{5.13}$$

In Verilog-A, $V_{tg} - V_p$ and $V_{bg} - V_p$ are voltage difference between terminals, assuming V_p as reference. The small signal results, including capacitance and conductance are illustrated in Fig.5.6 ($L = 100nm$, $W = 1\mu m$). Transconductance, g_m is confirmed by non-distributive model.

5.2.3 Vertical conduction: Semi-empirical TFET model

A semi-empirical TFET model originally developed by Notre Dame university is adopted to simulate the vertical tunneling mechanisms[132]. The main body of the equation is based on Kane's formalism:

$$j_{tun}(V_{gs}, V_{ds}) = a * f(V_{ds}) * V_{TW}(V_{gs}, V_{ds}) * F(V_{gs}, V_{ds}) * e^{-b/F(V_{gs}, V_{ds})} \tag{5.14}$$

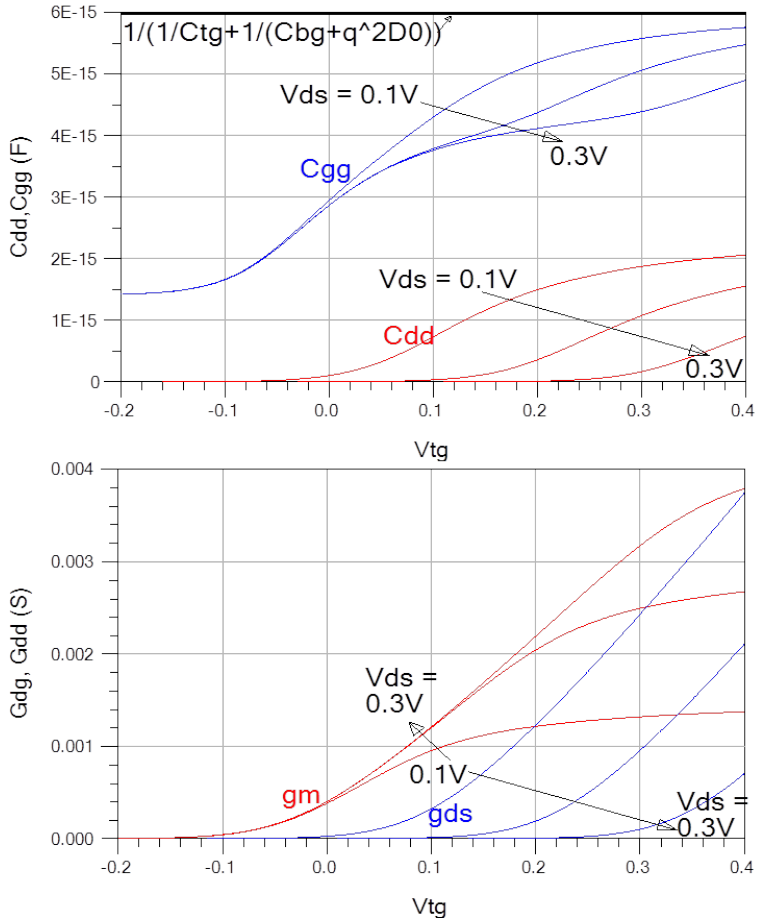

Figure 5.6: Small signal characteristics for 2D FET with distributed capacitive network

In this equation, a and b are material dependent parameters, and are defined as:

$$a = \frac{q^3}{8\pi^2\hbar^2}\sqrt{\frac{2m_R^*}{E_g}} \tag{5.15}$$

$$b = \frac{4\sqrt{m_R^* E_g^3}}{3q\hbar} \tag{5.16}$$

The term $f(V_ds)$ roughly represents the effect of cancellation of forward and reverse tunneling current at low V_{ds} condition. It describes the $I_{ds} - V_{ds}$ turn-on characteristics

and is expressed as:

$$f(V_{ds}) = \frac{1 - e^{-V_{ds}/\Gamma}}{1 + e^{(V_{THDS} - V_{ds})/\Gamma}} \tag{5.17}$$

For large V_{ds}, this function tends to 1; when $V_{ds} = 0$, f goes to zero; finally the function tends to go to a finite negative value as V_{ds} becomes negative. The term is a function of V_{gs}:

$$V_{THDS}(V_{gs}) = \frac{1}{2}\lambda[\tanh(\alpha_{THDS}(V_{gs} - V_{off})) + 1] \tag{5.18}$$

It is noteworthy that V_{gs} also controls the superlinear turn-on of $I_{ds}vs.V_{ds}$ through the parameter, V_{THDS}. A larger value of V_{THDS} will result in stronger superlinearity for $I_{ds} - V_{ds}$. $F(V_{gs}, V_{ds})$ is the electric field at the tunnel junction. It could be approximated by a linear relationship with V_{ds} and V_{gs}:

$$F(V_{gs}, V_{ds}) = F_0(1 + \gamma_1 V_{ds} + \gamma_2 V_{gs}) \tag{5.19}$$

The final term for this equation is V_{TW}, the tunneling window term, and requires some special attention. Generally, the tunneling window is controlled solely by gate bias, V_{gs} in saturation. In linear region, however, the tunneling window will also be modified by drain bias V_{ds} when carrier concentration in the channel is high enough to alter the potential distribution, which is also known as de-biasing effect[133]. Therefore, this could be expressed as two terms that is determined by V_{gs} and V_{ds} separately:

$$V_{TW}(V_{gs}, V_{ds}) = U ln(1 + e^{\frac{(V_{gs} - V_{th})}{U}}) * \frac{1}{2}(\tanh(\frac{V_{ds} - V_{NDRoff}}{V_{NDR0}}) + 1) \tag{5.20}$$

The dependence of V_{TW} on V_{ds} together with the term $f(V_{ds})$ could emulate not only the super-linear turn-on characteristics, but also the negative differential resistance region when $V_{ds} < 0$. Term $U = U(V_{gs})$ is only determined by gate bias, which has the expression as:

$$U = U_{min} + \frac{1}{2}U_a(\tanh(\frac{V_{gs} - V_{th}}{V_{U0}}) + 1) \tag{5.21}$$

This model could be fitted to a double gate hetero-junction TFET with GaSb/InAs tunnel junction simulated by Sentaurus. The fitted result of $I_{ds} - V_{gs}$ and $I_{ds} - V_{ds}$ characteristics are shown in Fig.5.7. Both negative differential resistance (NDR) region and turn-on region have good fitting, and the derivative at $V_{ds} = 0V$ is also smooth, which is a desirable feature for small signal and transient simulation.

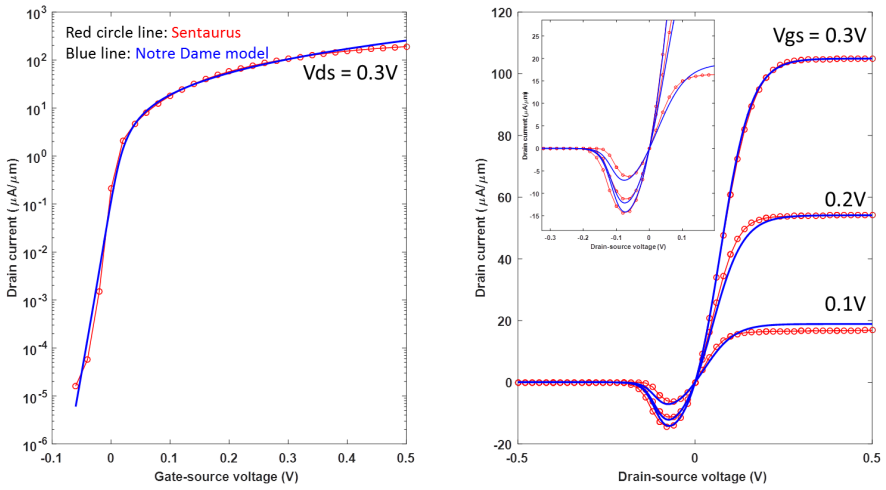

Figure 5.7: Analytic semi-empirical model fitted to Sentaurus simulation

5.2.4 Solving the Distributed physics

To confirm the results with circuit simulator, a MATLAB program is developed to solve the distributed circuit model at high precision. To begin with, the equivalent circuit shown in Fig.5.2 can be simplified to the node flow illustrated in Fig.5.8. Each

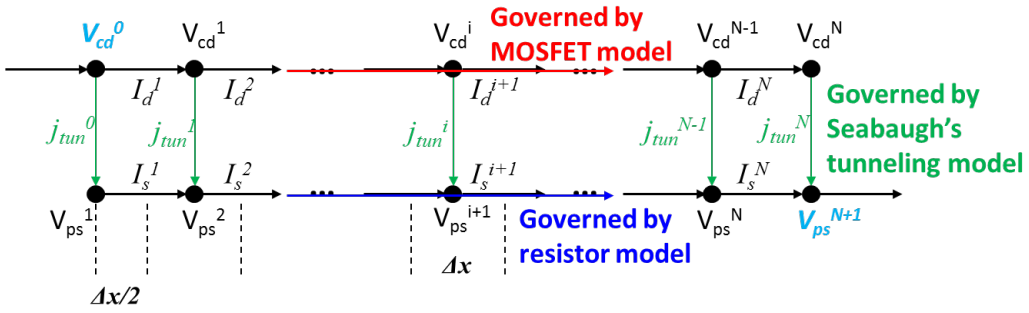

Figure 5.8: Simplified flow schematic of Vertical TFET

node has three current flows: two from lateral conduction and one from vertical tunneling. KCL is then applied to each node. If N grids are defined along the channel, there will be 2N unknown potentials (N for drain layer and N for source layer). One could formulate 2N non-linear equations that describe the current continuity at each junction. Thus, the solution could be found by Newton's iteration method, as will be detailed in the following paragraphs. The KCL equations (namely, current continuity equations) can be separated into two groups: drain and source layer respectively:

$$Drain: \begin{cases} I_d^2 - I_d^1 + j_{tun}^1 \Delta x = 0 \\ I_d^3 - I_d^2 + j_{tun}^2 \Delta x = 0 \\ \ldots \\ I_d^{i+1} - I_d^i + j_{tun}^i \Delta x = 0 \\ \ldots \\ I_d^N - I_d^{N-1} + j_{tun}^{N-1} \Delta x = 0 \\ -I_d^N + j_{tun}^N \Delta x/2 = 0 \end{cases} \tag{5.22}$$

$$Source: \begin{cases} -I_s^1 + j_{tun}^0 \Delta x/2 = 0 \\ I_s^1 - I_s^2 + j_{tun}^1 \Delta x = 0 \\ \ldots \\ I_s^{i-1} - I_s^i + j_{tun}^{i-1} \Delta x = 0 \\ \ldots \\ I_s^{N-1} - I_s^N + j_{tun}^{N-1} \Delta x = 0 \end{cases} \tag{5.23}$$

The lateral current I_d^i is modeled by the analytic model described in 2D FET section, while the vertical current j_{tun}^i is modeled by semi-empirical model also mentioned. The

non-linear equation set could thus be expressed as:

$$F_D^i(V_{cd}^{i-1}, V_{cd}^i, V_{cd}^{i+1}, V_{ps}^{i+1}) = \begin{cases} -I_d(V_{cd}^{i-1}, V_{cd}^i) + \\ \qquad j_{tun}(V_{cd}^i, V_{ps}^{i+1})\Delta x/2 = 0 \qquad i = N \\ I_d(V_{cd}^i, V_{cd}^{i+1}) - I_d(V_{cd}^{i-1}, V_{cd}^i) + \\ \qquad j_{tun}(V_{cd}^i, V_{ps}^{i+1})\Delta x = 0 \qquad i \neq N \end{cases} \tag{5.24}$$

$$F_S^i(V_{ps}^{i-1}, V_{ps}^i, V_{ps}^{i+1}, V_{cd}^{i-1}) = \begin{cases} -I_s(V_{ps}^i, V_{ps}^{i+1}) + \\ \qquad j_{tun}(V_{cd}^{i-1}, V_{ps}^i)\Delta x/2 = 0 \qquad i = 1 \\ I_s(V_{ps}^{i-1}, V_{ps}^i) - I_s(V_{ps}^i, V_{ps}^{i+1}) + \\ \qquad j_{tun}(V_{cd}^{i-1}, V_{ps}^i)\Delta x = 0 \qquad i \neq 1 \end{cases} \tag{5.25}$$

The unknowns are $\{V_{ps}^i\}$ and $\{V_{cd}^i\}$, and can be expressed as an unknown vector:

$$V = [\vec{V}_{cd}, \vec{V}_{ps}]^T \tag{5.26}$$

And the equations also expressed as a vector:

$$F = [\vec{F}_D, \vec{F}_S]^T = \vec{0} \tag{5.27}$$

The Jacobian Matrix elements could be defined as:

$$a_D^i = \frac{\partial F_D^i}{\partial V_{cd}^i} \qquad b_D^i = \frac{\partial F_D^i}{\partial V_{cd}^{i-1}} \qquad c_D^i = \frac{\partial F_D^i}{\partial V_{cd}^{i+1}} \qquad \beta_D^i = \frac{\partial F_D^i}{\partial V_{ps}^{i+1}} \tag{5.28}$$

$$a_S^i = \frac{\partial F_S^i}{\partial V_{ps}^i} \qquad b_S^i = \frac{\partial F_S^i}{\partial V_{ps}^{i-1}} \qquad c_S^i = \frac{\partial F_S^i}{\partial V_{ps}^{i+1}} \qquad \beta_S^i = \frac{\partial F_S^i}{\partial V_{cd}^{i-1}} \tag{5.29}$$

The Jacobian matrix is thus formulated as:

$$J = \begin{bmatrix} a_D^1 & c_D^1 & 0 & \dots & 0 & \beta_D^1 & 0 & 0 & \dots & 0 \\ b_D^2 & a_D^2 & c_D^2 & \dots & 0 & 0 & \beta_D^2 & 0 & \dots & 0 \\ 0 & b_D^3 & a_D^2 & \dots & 0 & 0 & 0 & \beta_D^3 & \dots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \dots & a_D^N & 0 & 0 & 0 & \dots & \beta_D^N \\ \beta_S^1 & 0 & 0 & \dots & 0 & a_S^1 & c_S^1 & 0 & \dots & 0 \\ 0 & \beta_S^2 & 0 & \dots & 0 & b_S^2 & a_S^2 & c_S^2 & \dots & 0 \\ 0 & 0 & \beta_S^3 & \dots & 0 & 0 & b_S^3 & a_S^2 & \dots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \dots & \beta_S^N & 0 & 0 & 0 & \dots & a_S^N \end{bmatrix} \tag{5.30}$$

Finally, Newton's iteration is used to search for the result:

$$V^{(k+1)} = V^{(k)} - [J^{(k)}]^{-1} * F^{(k)} \tag{5.31}$$

The term k represents the iteration steps. The criteria for convergence is defined when the

maximum change of potential in the updated solution is smaller than a certain value ε:

$$max\{|[J^{(k)}]^{-1} * F^{(k)}|\} < \varepsilon \tag{5.32}$$

5.3 Parameter setup

The parameter set and representative values are summarized in Table . The values of mobility for lateral conduction may vary from material to material. 2D-TMD based FETs have been demonstrated to have a field-effect mobility ranging from several tens to about $200 cm^2/Vs$ [134]–[136] at room temperature. In this paper, as a representative example we choose $SnSe_2$ as drain layer and WSe_2 as source layer, using for both a mobility of $250 cm^2/Vs$ for lateral conduction unless otherwise specified. The parameters for the vertical tunnel FET are fitted to the physics-based n-type Thin-TFET ($SnSe_2/WSe_2$) model reported in [122] with 0.35nm van der Waal's gap and lattices for the 2 layers perfectly aligned (assumed for optimized current conduction). It should be noted that theoretically a slight increase as small as 0.3 nm in the van der Waal's gap thickness will decrease the current density by one order of magnitude. Without confirmation from experiments, it is often treated as a fitting parameter within a reasonable range. Rotational asymmetry may be another factor that degrades current density for vertical TFETs built by 2D materials including both TMDs [137] and graphene [138].

The system of equations has been solved by MATLAB with 300 unit cells serially

Table 5.1: Dimensions and physical parameters used for vertical tunnel FET simulation with distributed physics.

Dimensions					
L	100nm	t_{TG}	1nm	t_{TJ}	0.35nm
W	$1\mu m$	ε_{TG}	3.9	ε_{TJ}	1
Lateral Conductionn		Vertical Tunneling (Notre Dame Model)			
V_{gs0}	-0.55V	m^{TUN}	$0.2m_0$	F_0	1MV/cm
V_{vdw0}	-0.3V	V_{off}	-0.173V	E_g^{TUN}	0.2eV
m_e^{DRN}	$0.3m_0$	λ	1V	U_{min}	4.4mV
E_g^{DRN}	1.0eV	α_{THDS}	$-4.26V^{-1}$	U_a	0.9V
μ^{DRN}	$250cm^2/Vs$	Γ	6.6mV	U_{V0}	0.03V
N^{SRC}	$10^{13}cm^{-2}$	V_{th}^{TUN}	0.124V	V_{off}^{NDR}	0.056V
μ^{SRC}	$250cm^2/Vs$	γ_2	$0.05V^{-1}$	V_0^{NDR}	0.058V
		γ_1	$0\,V^{-1}$		

connected. As aforementioned, the problem becomes a set of coupled current continuity equations in MATLAB whose Jacobian matrix dimensions are determined by the number of unit cells. The system has also been solved using Advanced Design System (ADS), a circuit simulator for RF, microwave and high speed applications, with 10 unit cells serially connected. The basic models for vertical and lateral conduction utilized in ADS are compiled by Verilog-A code with analytic expressions integrated to guarantee a high level of calculation efficiency.

5.4 Profile of potential, current and charge

The vertical tunneling current density is largely controlled by 2 factors: the tunneling window and the difference of quasi-Fermi levels between source and drain layer. Generally speaking, the former factor is controlled by the gate bias and the latter

factor by the drain bias. In the saturation region, the large difference of quasi-Fermi levels between source and drain layers will deplete the drain layer such that empty states in the drain are available for electrons from the source layer to tunnel to. However, the lateral 2D-FET component is also affected by the depletion of drain layer: the more depleted the drain layer is, the higher its resistivity and therefore the lower its lateral current will be. These two conduction mechanisms compete with each other until a steady state current is reached. In Fig.5.9(b), a variety of distribution profiles in ON-state

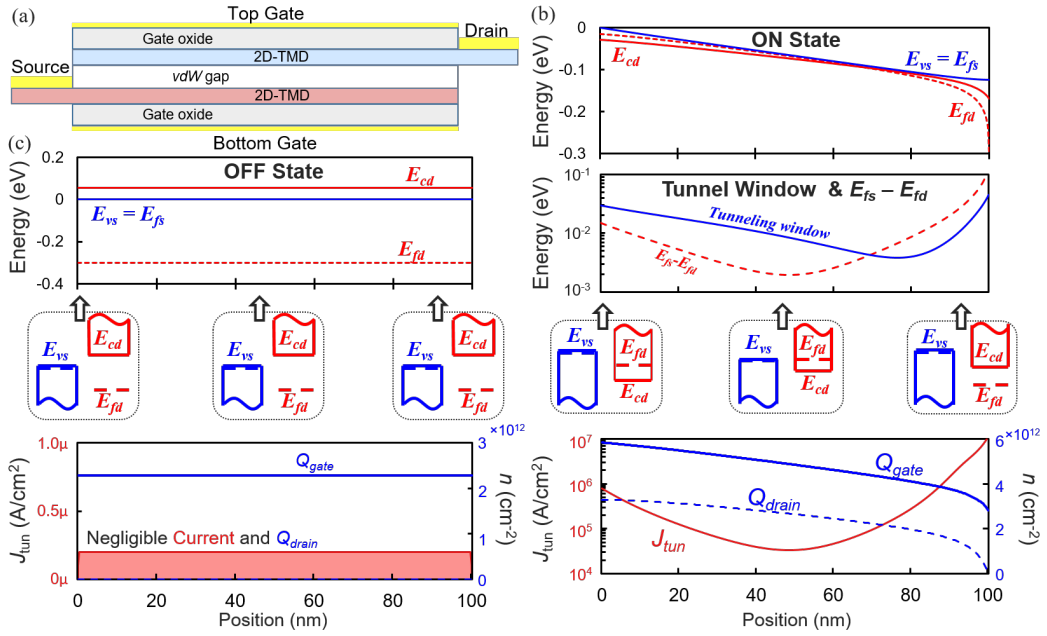

Figure 5.9: (a) Device structure. (b) On state profiles at $V_{gs} = 0.3V, V_{ds} = 0.3V$: band diagram; tunnel window and fermi level difference between two layers; drain layer carrier concentration Q_{drain} (blue dashed lines), gate charge Q_{gate} (blue solid line) and tunnel current density Jtun profile. Schematic band alignments near source terminal, in mid channel and near drain terminal are also plotted. (c) Off state profiles at $V_{gs} = 0V, V_{ds} = 0.3V$: band diagrams for drain and source; gate charge concentration Qgate and tunnel current density J_{tun} profile. Schematic band alignment across the channel is also plotted.

($V_{gs} = 0.3V, V_{ds} = 0.3V$) are shown, along with a corresponding structure of the vertical

TFET in Fig.5.9(a). Band alignments at three different positions along the channel are also illustrated. It can be found that both tunnel window and quasi-Fermi level difference are larger near source and drain terminals than in mid-channel. This results in higher tunnel current contributions near source and drain terminals. It is noted that near the source terminal, the carriers in the drain layer are not fully depleted and therefore there is less net tunnel current contribution than near the drain terminal. Low mobility necessitates a higher carrier concentration in the drain layer to maintain a balance between vertical and lateral conduction. On the other hand, infinite mobility results in a fully depleted and equi-potential drain layer while allowing conduction of the tunnel current. In the mid-channel region the quasi-Fermi levels in drain and source layers almost line up, thus this region contributes negligible tunnel current even though the tunnel window opens. Under this bias condition, the E-field near drain terminal is calculated to be 0.13MV/cm.

In Fig.5.9(c), illustrating the OFF state ($V_{gs} = 0V, V_{ds} = 0.3V$), the tunneling windows closes through the device, and the current tunneling from source layer to drain layer is very small. The band alignment does not vary along the channel, as also shown in the schematics in Fig.5.9(c). There is little voltage drop laterally because of the extremely low lateral current flow in the OFF state. Ideally when the tunneling window closes, there is no tunneling current and the two layers should be isolated. In practice, leakage mechanisms such as band tails or trap assisted tunneling (TAT) could happen even when there is no tunneling window. The semi-empirical model has taken that into account with an Urbach factor that controls the current around subthreshold region [132].

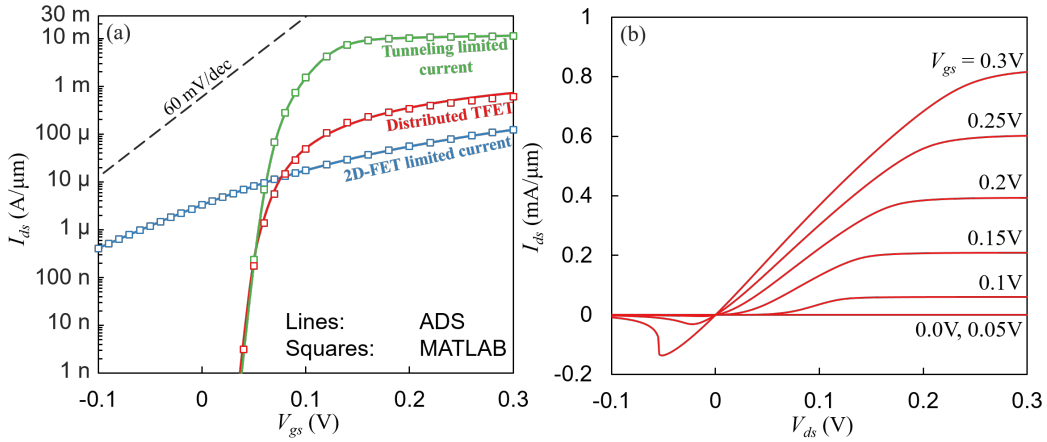

Figure 5.10: (a) $I_{ds} - V_{gs}$ characteristics for 2D-FET model (blue), TFET model (green), and vertical TFET distributed model (red). Lines are generated by MATLAB and circles are generated by ADS. (b) $I_{ds} - V_{ds}$ characteristics for vertical TFET distributed model simulated by ADS.

5.5 DC Characteristics

5.5.1 Current characteristics

DC characteristics have been calculated both within the ADS framework using 10 unit cells and within MATLAB using 300 unit cells, and results are in good agreement. Fig.5.10(a) shows the $I_{ds} - V_{gs}$ curves for the nominal parameter set. Also plotted in Fig.5.10(a) is the tunneling-limited current, which is the aggregate tunneling current between source and drain assuming equi-potentials for these layers; and 2D-FET-limited current, which is the lateral conduction current along the drain layer without any distributed tunneling current from the source layer, and ideal current supply on the source side of the drain layer. It can be seen that in the sub-threshold region, the tunneling limited current is much lower than the 2D-FET limited current. The distributed vertical TFET characteristics follow the tunneling limited current and preserve the steep subthreshold

slope. On the other hand, in the ON state, where the tunneling-limited current is much higher than the 2D-FET limited current, the distributed vertical TFET is limited by lateral conduction.

$I_{ds} - V_{ds}$ characteristics are shown in Fig.5.10(b) for the distributed model. The figure includes behavior at negative V_{ds}, for which there is a negative resistance region well-known in tunneling FETs. It is noted that here the negative differential resistance region is tilted due to series resistance stemming from lateral conduction of both source layer and drain layer.

5.5.2 Competition: Lateral v.s. Vertical conduction

To further characterize the effects of lateral conduction on DC characteristics, ON-state and OFF-state (at fixed bias conditions) current densities versus gate length are plotted in Fig.5.11(a) and (b) using two sets of parameters. The first set is the same as stated in section III based on the assumed TMD material system. TMD materials are expected to reach an intrinsic mobility up to $500 cm^2/Vs$ based on density functional theory formalism [139], therefore, a mobility of $250 cm^2/Vs$ is a reasonable estimate. The second set of parameters has a higher mobility of $2000 cm^2/Vs$, which is closer to a III-V-based material (such as a 15nm layer of InAs achieving field-effect mobility up to $2300 cm^2/Vs$ [140]). Both plots show opposite trends of current variation with decreasing gate length for the limiting mechanisms: 2D-FET-limited current is inversely proportional to channel length for long channel FETs, while tunneling-limited current is proportional to channel length. Although short channel effect and velocity saturation will

prevent the channel length proportionality from being strictly valid as it scales down, the overall trend of increasing current with decreasing gate length will still hold.

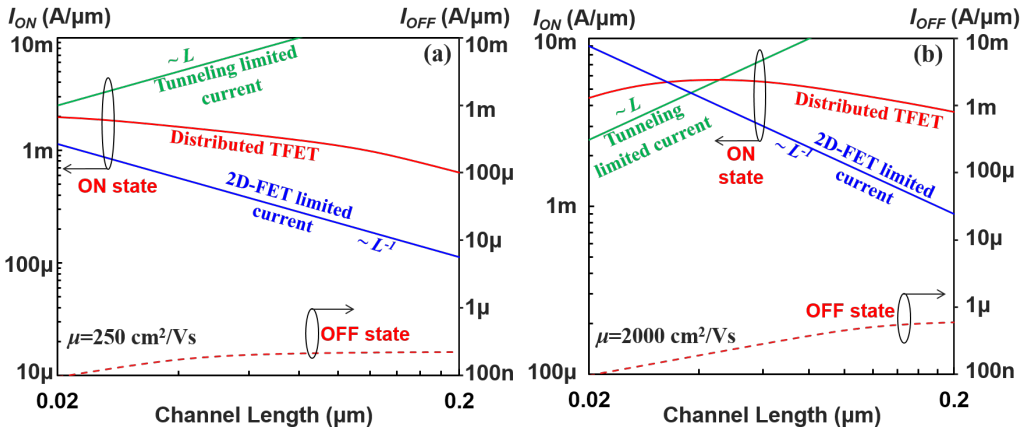

Figure 5.11: ON state current ($V_{gs} = V_{ds} = 0.3V$, solid lines for left y-axis) versus channel length L_g for pure tunneling model (green), pure 2D FET model (blue) and vertical tunnel FET model with distributed physics (red) with mobility of (a) $250cm^2/Vs$ and (b) $2000cm^2/Vs$. OFF state current curves at $V_{gs} = 0.05V$ are also plotted with red dashed lines to indicate leakage performance vs channel length.

Furthermore, thanks to the ultra-thin body of the 2D material, the FET device is rather resistant to short channel effects [141]. The figure shows that the trend for the overall distributed model follows the mechanism with lower current density. Thus, when $\mu = 250cm^2/Vs$, the 2D-FET limited current is always less than the tunneling limited current, and the distributed model follows the trend of the pure 2D-FET of increasing current as gate length shrinks down to 20nm in Fig.5.11(a). On the other hand, when $\mu = 2000cm^2/Vs$ in Fig.5.11(b), the tunneling-limited current is lower than the 2D-FET limited current below $L_g = 40nm$, and here the overall current of the distributed model decreases with decreasing channel length, following the trend of tunneling-limited current. Beyond 40 nm, increasing channel length decreases the current for distributed

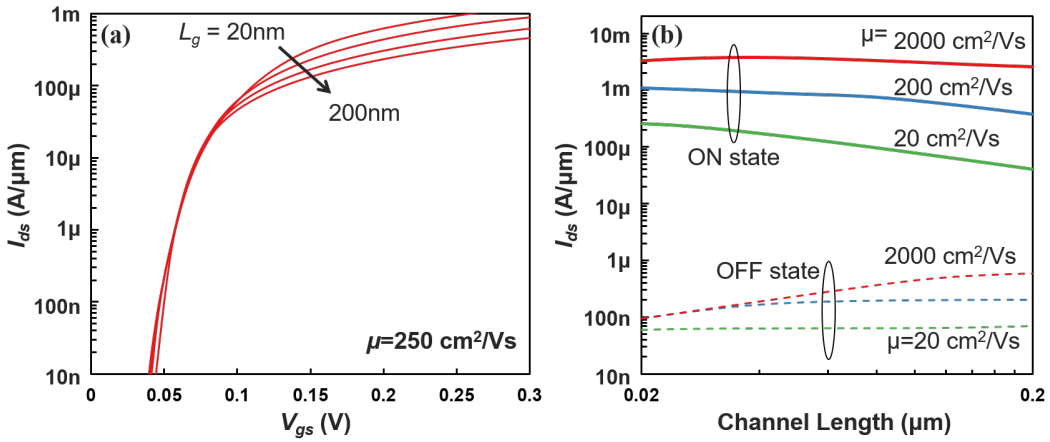

Figure 5.12: (a) $I_{ds} - V_{gs}$ characteristics with varying gate lengths in saturation condition ($V_{ds} = 0.3V$); (b) I_{ON}/I_{OFF} v.s. L_g with varying mobilities of $2000cm^2/Vs$ (red), $200cm^2/Vs$ (blue) and $20cm^2/Vs$ (green) showing shorter gate lengths give lower leakage current

model, following the trend of 2D-FET-limited current. It is found that the OFF-state current always scales up with increasing channel length. This is because the tunneling mechanism is the bottleneck of conduction in the subthreshold region. Hence, in terms of ON/OFF ratio, a vertical tunnel device with shorter gate length is more desirable. In Fig.5.12(a), the plot illustrates a convergence of OFF-state current for devices with different channel length's while ON-state current varies. A more practical mobility of $20cm^2/Vs$ for TMD material is also simulated and compared with the ideal TMD mobility of $200cm^2/Vs$ and III-V MOSFET mobility of $2000cm^2/Vs$ in Fig.5.12(b).

The simulations indicate that channel length can be an important parameter for optimizing the ON-state current of the vertical TFETs. They also show that the dependence of overall current on channel length follows the limiting conduction mechanism with smaller current density. It is expected that if the tunneling-limited component is more than one order of magnitude lower than the lateral conduction limited component,

the effect of the 2D FET conduction limit is not significant. This corresponds to the case discussed in [142].

5.6 AC and RF Characteristics

AC characteristics have been calculated by incorporating the capacitance network of Fig.5.2(c) together with the DC components in each unit cell. As noted in the figure, the capacitance network includes the quantum capacitance $C_q = dQ_n/dV_c = q^2 D_0 f_c(V_c)$ which is a nonlinear function of V_c, and in general varies considerably along the channel.

For any two port device, the small signal characteristics can be described by the corresponding Y-matrix:

$$\begin{bmatrix} i_g \\ i_d \end{bmatrix} = \begin{bmatrix} Y_{gg} & Y_{gd} \\ Y_{dg} & Y_{dd} \end{bmatrix} \begin{bmatrix} v_g \\ v_d \end{bmatrix} \tag{5.33}$$

The matrix elements can be described as a sum of real parts (conductances and transconductances) and imaginary parts (capacitances and transcapacitances):

$$Y_{mn} = G_{mn}(\omega) + j\omega C_{mn}(\omega) \tag{5.34}$$

The subscript m and n represents g (for gate) or d (for drain). Note that C_{gd} derived in this manner from the Y-matrix with distributed physics is more complex than the case for a simple C_{gd} bridged between gate and drain in a lumped equivalent circuit model. It is still an important parameter for circuit effects, such as the Miller effect on input capacitance.

The capacitance values are calculated quasi-statically:

$$C_{mn}(\omega) = \frac{dQ_m}{dV_n} \tag{5.35}$$

5.6.1 Intrinsic AC characteristics

The overall small signal capacitances at different biases are shown in Fig.5.13 by ADS circuit simulator and MATLAB fine grid simulation. Again, good agreement is obtained between circuit simulation and MATLAB simulation. It is also noted that a peak of C_{gg} occurs around the turn-on condition. This is due to the Miller multiplication effect: When the drain layer is abundant with carriers before turn-on at high V_{ds}, the carriers will quickly be depleted once the device is turned on. Therefore, increasing the V_{gs} will result in a decrease in potential at drain layer, thus causing such a spike. After turning on, the potential distribution becomes relatively stable in saturation and the capacitance drops back until carrier accumulates again at high V_{gs} in linear region.

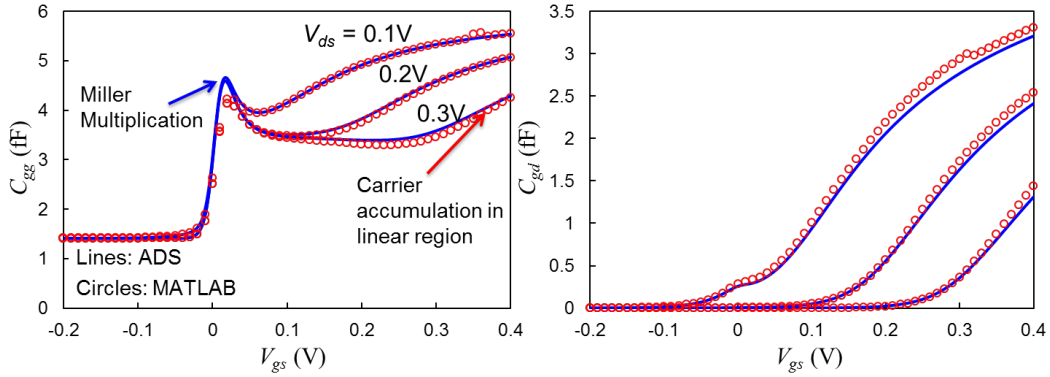

Figure 5.13: (a): $C_{gg} - V_{gs}$ for distributed Vertical TFET model by ADS (blue lines) and MATLAB (red circles). (b): $C_{gd} - V_{gs}$ for distributed Vertical TFET model by ADS (blue lines) and MATLAB (red circles).

A variety of behaviors of C_{mn} vs bias can be found depending on the threshold voltages for tunneling V_{th}^{TUN} and for lateral conduction V_{th}^{FET}. The overall small signal capacitances at different biases are shown in Fig.5.14 using the ADS circuit simulator with different tunneling threshold voltages V_{th}^{TUN} chosen to be 0.12V and 0.2V, with V_{th}^{FET} fixed at -0.06V (V_{th}^{FET} is defined to correspond to FET limited current = $1\mu A/\mu m$). Practically, both V_{th}^{TUN} and V_{th}^{FET} are dependent on physical parameters such as metal work function, oxide thickness and design choices. Fig.5.14 also shows an asymptotic curve of capacitance as mobility approaches infinity with V_{th}^{TUN} = 0.12V. The asymptotic curve shows the extreme condition when lateral conductivity is so high that a uniform drain layer potential is formed. Such a condition is assumed in [122] and our capacitance results are in reasonable agreement with the results in [123] after scaling to the same gate length.

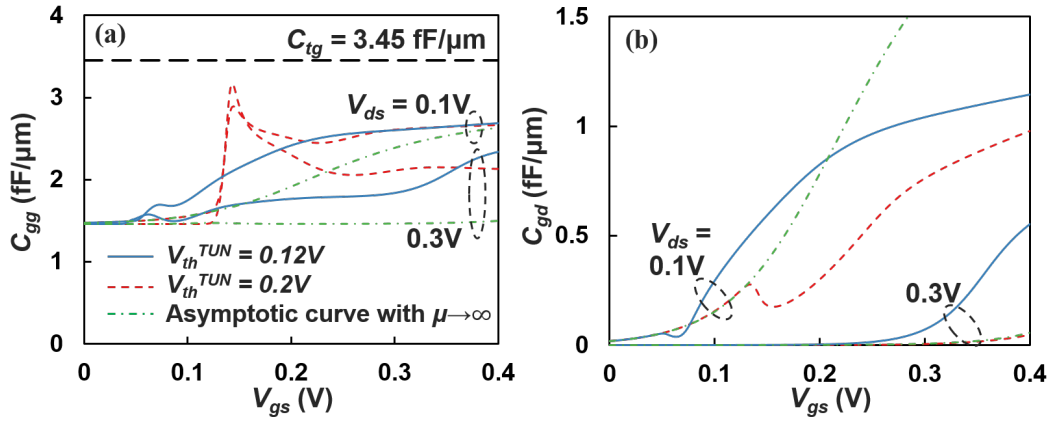

Figure 5.14: (a): Small signal capacitance (a) C_{gg} and (b) C_{gd} simulated with different tunnel component threshold voltages: 0.12V (solid blue lines), 0.2V (red dashed lines) and different V_{ds} values: 0.1V and 0.3V. Curves for mobility asymptotically approaching infinity with 0.12V threshold voltage are also shown (green dash-dot line). Top gate dielectric capacitance is also shown ($L_g = 100nm$).

It can be observed in Fig.5.14(a) that the gate capacitance for the case of infinite mobility is lower than for the case of realistic lateral conduction mobility. For the case of asymptotically high mobility, carriers do not accumulate in the drain layer. As soon as they tunnel into it, they are swept by drift out the drain terminal; only carriers in the source layer carriers contribute to the total capacitance. When mobility is finite, carriers accumulate in the drain layer even in the saturation condition, as is already depicted in Fig.5.9(b). Thus, they produce an extra capacitance contribution to C_{gg} compared to the asymptotic mobility curve. This effect is further enhanced when the tunnel device turns on at a higher voltage (higher V_{th}^{TUN}).

It is noteworthy that the curve with $V_{th}^{TUN} = 0.2V$ in Fig.5.14(a) shows a peak at V_{gs} around the turn-on condition for tunneling. This peak of C_{gg} is caused by the compound effect of lateral and vertical conduction. For V_{gs} values below turn-on, the drain layer is an equipotential and exhibits a relatively high carrier density; tunneling limited conduction with a very low current value dominates the transport. Once the device is turned on, the drain layer becomes depleted by the positive drain bias, inducing a decrease of potential in the drain layer. These opposite trends of change in gate bias and drain layer potential result in an enhancement in input capacitance similar to the Miller-multiplication effect. This feedback effect is less prominent if carriers accumulate to a lesser extent when the current is turned on, as shown in Fig.5.14(a) for V_{th}^{TUN} = 0.12V.

C_{gd} with infinite mobility is greater than with finite mobility in the linear region, as shown in Fig.5.14(b). This is because the drain layer charge can be easily modulated

by drain voltage when carriers are accumulated and the drain is extremely conductive. In the saturation region, lateral conduction induces higher Cgd compared to the asymptotic curve, which may be a concern for an enhanced Miller effect for practical operation.

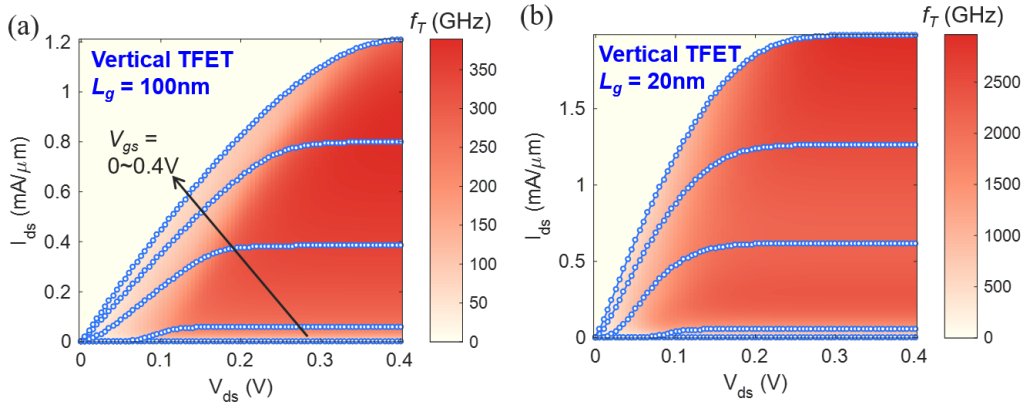

Figure 5.15: Comparison of intrinsic f_T for vertical TFET with (a) 100nm and (b) 20nm gate length

5.6.2 Intrinsic RF characteristics

With the appropriate modeling of both current and charge, intrinsic RF characteristics could be illustrated by evaluating the cut-off frequency f_T using the equation:

$$f_T = \frac{g_m}{2\pi C_{gg}} \tag{5.36}$$

To study the RF performance of vertical TFETs, a comparison of vertical tunnel devices ($\mu = 250 cm^2/Vs$ for both drain and source layer) with varying gate length (100nm and 20nm) is made in Fig.5.15 by plotting the color maps of f_T overlaid with $I_{ds} - V_{ds}$ characteristics. The f_T colormap is useful to reveal physical limiting factors for high

performance devices as well as to determine the optimized operation region. As is illustrated in Fig.5.15, a drastic improvement in intrinsic cut-off frequency is accomplished for vertical TFET design by shrinking down the gate length (350GHz to 2THz).

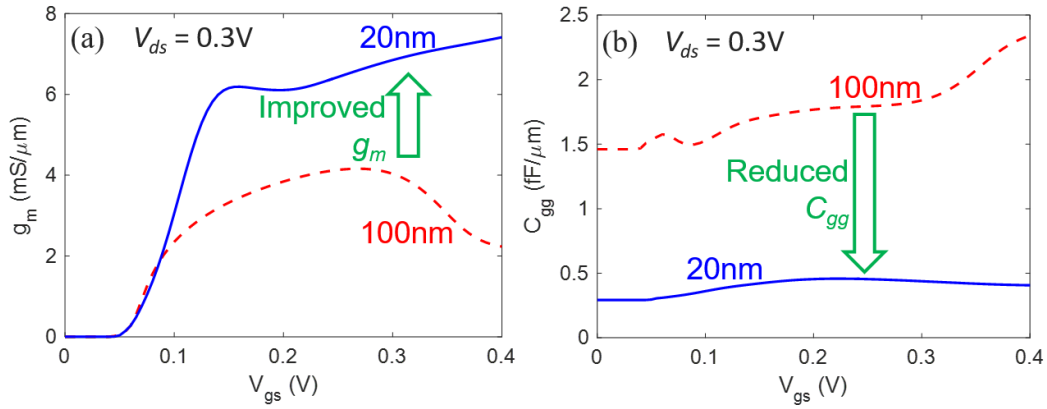

Figure 5.16: (a) Transconductance and (b) input capacitance of vertical TFET with 100 nm (red dashed lines) and 20 nm (blue solid lines)

To further explain enhanced performance of intrinsic f_T with shrinking gate length for vertical tunnel FET design, transconductance (gm) and input capacitance (Cgg) are plotted versus gate bias at fixed V_{ds} = 0.3V in Fig.5.16. An improvement in transconductance gm ($\times$1.5 times approximately @ 0.3V) and a decrease in capacitance ($1.7fF/\mu m$ versus $0.5fF/\mu m$ @ 0.3V) together contribute to the improvement in cut-off frequency. The improvement in transconductance originates from the predominance of lateral conduction when $\mu = 250cm^2/Vs$ as stated in section V. The high capacitance value of the 100 nm vertical TFET mainly originates from the non-depleted drain layer in saturation, degrading the speed for the vertical TFET. Shrinking gate length will effectively shrink the area that accumulates carriers for the vertical TFET structure, and consequently leads to a much lower input capacitance. On the contrary, for lateral

Table 5.2: Dimensions and parameters for parasitic elements

H_{SD}	200nm	H_{tg}	150nm
t_{sp}	20nm	t_{ox}	0.5nm
t_{bg}	27nm	$L_{S,D}$	100nm
W	$1\mu m$	L_g	100nm
ε_{ox}	3.9	ε_{spacer}	2.7
C_{xtg}	0.148fF	C_{xbg}	0.148fF
R_g	12.5Ω	$R_{s,d}$	100Ω

TFET structures, transconductance and capacitance are more weakly dependent on gate channel length [133]. It is noteworthy that scaling the gate length down will not improve the transconductance gm necessarily, especially when vertical conduction becomes the limiting mechanism. But C_{gg} should always scale down with decreasing gate length. In the asymptotic limit of infinite mobility, transconductance g_m and input capacitance C_{gg} will both scale linearly with gate length. The intrinsic cut-off frequency thus becomes independent of the gate length, Lg.

5.6.3 Extrinsic RF characteristics with parasitic elements

Despite the drastic improvement in intrinsic f_T from gate length scaling, extrinsic elements will finally become the bottleneck for improvement. To appropriately take these into account, a list of extrinsic elements such as parasitic capacitance and contact resistance values are tabulated in Table 5.2. A schematic diagram showing the relationship between the elements and the device structure is also pictured in the inset of Fig.5.17. The parasitic capacitance values are estimated according to Boeuf et al. [143], with the device dimensions also listed in Fig.5.17. Note that channel length Lg has little effect on

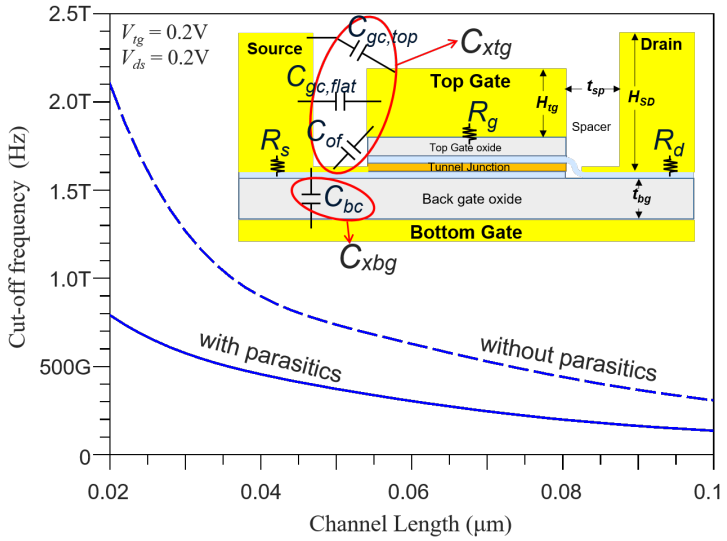

Figure 5.17: Cutoff frequency (f_T) v.s. Lg with and without the consideration of parasitic elements (Inset: Schematics diagram of parasitic elements considered)

parasitic capacitance (less than 10% when varying from 20nm to 100nm) and the largest value when Lg = 100nm was chosen. The cut-off frequency with varying gate length at $V_{gs} = V_{ds} = 0.2V$ in Fig.5.17 clearly illustrates the limiting effect from extrinsic elements at shorter gate length. The extrinsic f_T evaluated at 20nm reads 800GHz at this bias condition, which is desirable for low power high frequency applications. The vertical tunnel FET cutoff frequency at V_{gs} = V_{ds} = 0.2V is 600GHz. This can be compared to a 25nm gate length finFET with f_T =300 GHz reported in [144] with slightly higher parasitics of $0.5fF/\mu m$. The finFET uses a higher bias of V_{gs} = 0.5V and has higher power consumption.

Note that channel length L_g has little dependence on parasitic capacitance (less than 10% when varying from 20nm to 100nm) and a larger value case when $L_g = 100nm$ is applied for all cases. The cut-off frequency with varying gate length at $V_{gs} = V_{ds} = 0.3V$

is illustrated in Fig.5.17(b). It clearly illustrates the limiting effect from extrinsic elements at shorter gate length, when the RF performance is more favorable. The extrinsic f_T evaluated at 20nm reads 400GHz at such bias condition.

5.7 Conclusion

In this chapter, the effect of distributed physics on vertical tunnel FETs is studied for DC, AC and RF characteristics. Because of the competing mechanisms for lateral and vertical conduction, there exists an optimized channel length for highest DC current. The distributed physics for vertical TFET also results in high capacitance value in saturation with long channel length and not fully depleted drain layer in saturation. Shorter gate length will improve the RF performance by drastically reducing the capacitance without the degradation in transconductance, which is different from the lateral TFET design case. Even after the inclusion of extrinsic elements, the cut-off frequency could still be improved significantly by shrinking the gate length, which is desirable for low power high frequency applications.

5.8 Future Work

Implementation of Verilog-A model for vertical TFET grants circuit designs based on TFET. Two examples of circuit applications are demonstrated for vertical TFET with distributed physics. The circuits are built and simulated using ADS.

5.8.1 Inverter chain with Fan-out of 4

Inverter chain is a circuit that could reveal the speed of an inverter. In this section, CMOS-like inverters which contain p-type and n-type Veritcal TFET with symmetric performance are used to construct the inverter chain. Chain with Fan-out of 4 is chosen to achieve a more practical condition. The schematic circuit diagram for the inverter chain is shown in Fig.5.18(a). Two gate lengths, 100nm and 20nm are chosen for comparison which illustrates transient waveforms of V_{in}/V_{out} at different stages, as shown in Fig.5.18(b). As could be seen, the delay per inverter is just $8.8ps$ for 20nm gate

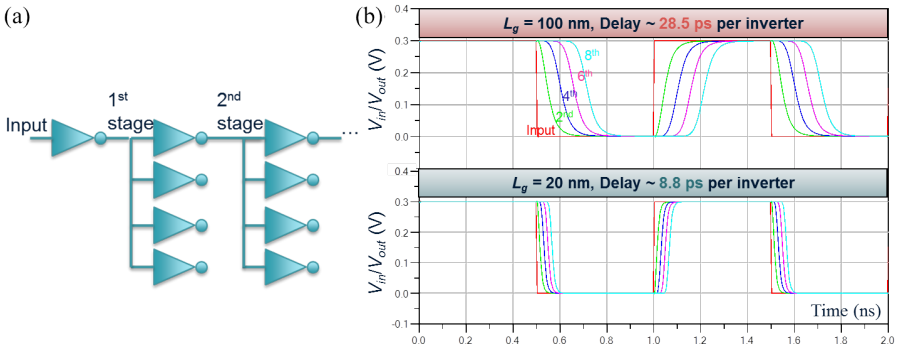

Figure 5.18: (a) Schematic circuit diagram of inverter chain with Fan-out of 4. (b) Transient waveforms for voltage at each stage with $L_g = 100nm$ and $20nm$ respectively.

length device, while that for 10nm device is 28.5ps. This is in line with the extrinsic RF characteristics trend: when L_g scales down to 20nm, the speed of the device is increasing. The power dissipation per inverter is $90\mu W$ while the delay power product is calculated to be $0.8fJ$ at $V_{DD} = 0.3V$.

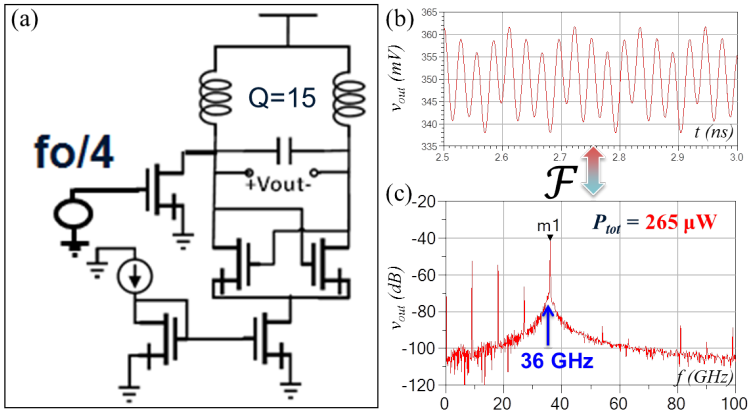

Figure 5.19: (a) Schematic circuit diagram of LC Oscillator with injection locking. (b) Transient waveforms for output signal. (c) Frequency spectrum for output signal

5.8.2 LC Oscillator with injection locking

A second example circuit is an LC oscillator with injection locking. The example circuit diagram is shown in Fig.5.19(a). The input signal is peaked at 9GHz, and the output signal is shown in Fig.5.19(b) in time domain and Fig.5.19(c) in frequency domain. The total power consumption for this circuit is calculated to be $265\mu W$.

5.9 Acknowledgment

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Chapter 6

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Appendix A

Analytic approximations for K_{diff} of 2D-FET

A.1 Derivation for K_{diff} with continuous 4^{th} order derivative

The K_{diff} for p-type 2D-FET can be written as:

$$\begin{aligned} K_{diff} &= -\frac{q\mu D_0 kT}{L}\left(\int_{V_{cd}}^{V_{cs}} ln(f_{v0}(V_c))dV_c\right) \\ &= -\frac{\mu D_0 (kT)^2}{L}\left(\int_{v_{cd}}^{v_{cs}}\int_{v_c}^{\infty}(1-f_{v0}(v))dvdv_c\right) \end{aligned} \tag{A.1}$$

Note that $ln(f_{v0})$ can be expressed in terms of integration of $1-f_{v0}$ and $v_c = qV_c/kT$. Then f_{c0} can be further expressed by piece-wise approximation that are integrable:

$$1-f_{v0}(v_c)=\begin{cases}1-\left(e^{v_c}+\zeta e^{2v_c}\right) & v_c \leqslant -v_{c2}\\ (1-v_c/\alpha)/2 & -v_{c2} \leqslant v_c \leqslant v_{c2}\\ \left(e^{-v_c}+\zeta e^{-2v_c}\right) & v_c \geqslant v_{c2}\end{cases} \tag{A.2}$$

A straight line is used to approximate the transition from 0 to 1; exponential, e^{-v_c} to represents Maxwell-Boltzman distribution. There is an extra exponential term, ζe^{-2vc}, to stitch the transition smoothly. As is stated, there are three parameters to be determined, ζ, α, v_{c2}, all independent of temperature, and is not variant upon different materials. This feature makes it very desirable for compact modeling.

To solve three unknowns, three independent equations are needed: the continuity conditions for 0^{th}, 1^{st} and 2^{nd} derivatives at $v_c = v_{c2}$. The continuity conditions will be automatically satisfied at $v_c = -v_{c2}$ thanks to the symmetry of the piece-wise expression. The resulted equations are thus obtained:

$$\begin{cases}-\frac{v_{c2}-\alpha}{2\alpha} = e^{-v_{c2}}+\zeta e^{-2v_{c2}} & 0^{th}\ order\ derivative\\ -\frac{1}{2\alpha} = -e^{-v_{c2}}-2\zeta e^{-2v_{c2}} & 1^{st}\ order\ derivative\\ 0 = e^{-v_{c2}}+4\zeta e^{-2v_{c2}} & 2^{nd}\ order\ derivative\end{cases} \tag{A.3}$$

It can be easily deducted from the last equation that:

$$\zeta e^{-v_{c2}} = -\frac{1}{4} \tag{A.4}$$

This can be put into the first two equations to get rid of ζ:

$$\begin{cases} -\frac{v_{c2}-\alpha}{2\alpha} = \frac{4}{5}e^{-v_{c2}} & 0^{th}\ order\ derivative \\ -\frac{1}{2\alpha} = -\frac{1}{2}e^{-v_{c2}} & 1^{st}\ order\ derivative \end{cases} \tag{A.5}$$

Take the ratio of these two equations, and $v_{c2}-\alpha$ can be easily obtained:

$$v_{c2} = \alpha - \frac{3}{2} \tag{A.6}$$

Substitute this into 0^{th} order derivative continuity equation, a transcendental equation for α can be derived and solved:

$$-\frac{3}{2} = \ln(\alpha) - \alpha \tag{A.7}$$

There are two solutions solved numerically from this equation:

$$\alpha \approx \begin{cases} 0.302 \\ 2.358 \end{cases} \tag{A.8}$$

Note that v_{c2} should be greater than zero in the previous assumption to make the range of piece-wise function non-trivial and that $v_{c2} = \alpha - 3/2$. Therefore, $\alpha > 3/2$ is required and the first solution, $\alpha = 0.302$, can be excluded. The α and v_{c2} are determined

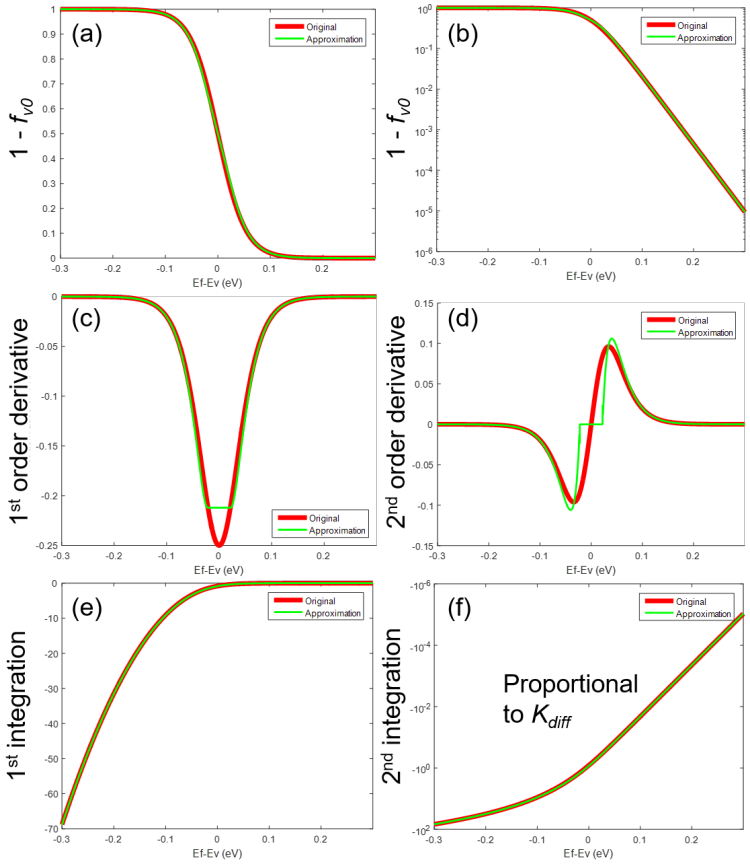

Figure A.1: Comparison of piece-wise approximation with original Fermi-Dirac distributions in (a) linear scale, (b) log scale, (c) 1^{st} order derivative, (d) 2^{nd} order derivative, (e) first integration (namely $\ln(1-f_{v0})$) and (f) second integration (proportional to K_{diff})

as:

$$\alpha = 2.358 \tag{A.9}$$

$$v_{c2} = \alpha - 3/2 = 0.858 \tag{A.10}$$

Finally, the term ζ can be determined as:

$$\zeta = -\frac{1}{4}e^{v_{c2}} \approx -0.5896 \tag{A.11}$$

The agreement of approximated expression and its first and second derivatives with the original Fermi-Dirac distributions are illustrated in Fig A.1(a)-(d).

The piece-wise function can be integrated analytically, and K_{diff} is the result of integration by two times which are then used in chapter 5:

$$\begin{cases} \frac{v_c^2+v_{c2}^2}{2} - \frac{v_{c2}^3}{3\alpha} + 2(e^{-v_{c2}} + \frac{\zeta}{4}e^{-2v_{c2}}) + & \\ \qquad 2v_{c2}(e^{-v_{c2}} + \frac{\zeta}{2}e^{-2v_{c2}}) + (e^{-v_c} + \frac{\zeta}{4}e^{-2v_c}) & v_c \geq v_{c2} \\ -\frac{(v_c+v_{c2})^2(-v_c+2v_{c2}-3\alpha)}{12\alpha} + & \\ \qquad \frac{\zeta}{4}e^{-2v_{c2}}(1+2v_c+2v_{c2}) + e^{-v_{c2}}(1+v_c+v_{c2}) & v_{c2} \geq v_c \geq -v_{c2} \\ e^{v_c} + \frac{\zeta}{4}e^{2v_c} & v_c \leq -v_{c2} \end{cases} \tag{A.12}$$

Good agreement is obtained with numerical integration results as shown in Fig A.1(e) and (f). The error peaks at $v_c = 0$ with a value less than 4%. Note that although the extracted parameters are material and temperature in-dependent, the error could be temperature dependent as the approximation become less accurate with elevating temperature conditions.

A.2 Derivation for K_{diff} with continuous 5^{th} order derivative

Further improvement could be implemented by adding a third power term in the transition region to mimic the parabolic first order derivative result.

$$1-f_{v0}(v_c)=\begin{cases}1-\left(e^{v_c}+\zeta e^{2v_c}\right) & v_c\leqslant -v_{c2}\\ \left(1-v_c/\alpha-v_c^3/\beta\right)/2 & -v_{c2}\leqslant v_c\leqslant v_{c2}\\ \left(e^{-v_c}+\zeta e^{-2v_c}\right) & v_c\geqslant v_{c2}\end{cases} \tag{A.13}$$

Now, there are four unknowns, and the equations are the continuity equations up to the 3^{rd} derivative:

$$\begin{cases}\frac{1}{2}\left(1-\frac{v_{c2}}{\alpha}-\frac{v_{c2}^3}{\beta}\right)=e^{-v_{c2}}+\zeta e^{-2v_{c2}} & 0^{th}\ order\ derivative\\ \frac{1}{2}\left(-\frac{1}{\alpha}-\frac{3v_{c2}^2}{\beta}\right)=-e^{-v_{c2}}-2\zeta e^{-2v_{c2}} & 1^{st}\ order\ derivative\\ \frac{1}{2}\left(-\frac{6v_{c2}}{\beta}\right)=e^{-v_{c2}}+4\zeta e^{-2v_{c2}} & 2^{nd}\ order\ derivative\\ \frac{1}{2}\left(-\frac{6}{\beta}\right)=-e^{-v_{c2}}-8\zeta e^{-2v_{c2}} & 3^{rd}\ order\ derivative\end{cases} \tag{A.14}$$

The solutions are calculated numerically:

$$\begin{cases}v_{c2}=1.4145 & \beta=-47.26\\ \alpha=2.1748 & \zeta=-0.6486\end{cases} \tag{A.15}$$

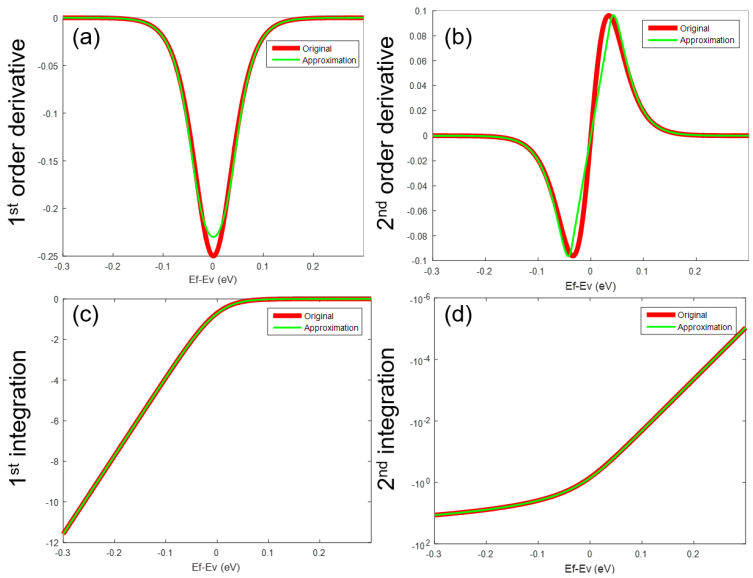

Figure A.2: Comparison of 3rd order derivative continuous piece-wise approximation with original Fermi-Dirac distributions of (a) 1^{st} order derivative, (b) 2^{nd} order derivative, (c) 1^{st} integration and (d) 2^{nd} integration

The first and second derivatives of $1 - f_{v0}$ is compared with original expression in Fig A.2. It can be seen that the 2^{nd} derivative agrees much better than that shown in Fig A.1(d). The error is about 1% better compared to the previous case. The newly

calculated analytic expression for the double integration reads:

$$\begin{cases} \frac{v_c^2}{2} - \left(e^{v_c} + \frac{\zeta}{4}e^{2v_c}\right) + \left(e^{-v_c} + \frac{\zeta}{4}e^{-2v_c}\right) + \left(\frac{v_{c2}^2}{2} - \frac{v_{c2}^3}{3\alpha} - \frac{v_{c2}^5}{5\beta}\right) & \\ \quad +2\left(e^{-v_{c2}} + \frac{\zeta}{2}e^{-2v_{c2}}\right)v_{c2} + \left(e^{-v_{c2}} + \frac{\zeta}{4}e^{-2v_{c2}}\right) & v_c \leqslant -v_{c2} \\ \frac{1}{2}\left(\frac{v_c^2}{2} - \frac{v_c^3}{6\alpha} - \frac{v_c^5}{20\beta}\right) - \frac{1}{2}\left(\frac{v_{c2}^2}{2} - \frac{v_{c2}^3}{6\alpha} - \frac{v_{c2}^5}{20\beta}\right) + \left(e^{-v_{c2}} + \frac{\zeta}{4}e^{-2v_{c2}}\right) & \\ \quad -\left[\frac{1}{2}\left(v_{c2} - \frac{v_{c2}^2}{2\alpha} - \frac{v_{c2}^4}{4\beta}\right) + \left(e^{v_{c2}} + \frac{\zeta}{2}e^{-2v_{c2}}\right)\right](v_c - v_{c2}) & -v_{c2} \leqslant v_c \leqslant v_{c2} \\ e^{-v_c} + \frac{\zeta}{4}e^{-2v_c} & v_c \geqslant v_{c2} \end{cases} \tag{A.16}$$

Appendix B

Verilog-A Code for vertical TFET unit elements

B.1 Notre Dame Model

```
/* ---------------- 2015-Aug-05 --------------
This Verilog-A describes IV of a tunnel FET device using Seabaugh's
    semiempirical model
Reference:
- H.Lu, J.W.Kim, D.Esseni, and A.Seabaugh, "Continuous semiempirical
    model for the current-voltage characteristics of tunnel fets"
  2014 15th International Conference on Ultimate Integration on
      Silicon (ULIS), pp25-28
/* ---------------- 2015-Aug-21 --------------
Adding P-FET device to enable both types
- type = "n"            from{"n","p"};
/* ---------------- 2016-May-11 --------------
- Modify U function and VTW function to produce continuous derivative
     of Id-Vgs and NDR region
Author: Jie Min
Advisor: Peter M. Asbeck
Affiliation: University of California, San Diego
---------------------------------------------- */
`include "disciplines.vams"
`include "constants.vams"

`define m0 9.1e-31
`define q 1.6e-19

module SeabaughTunnel(s,d,g);

inout s,d,g;
```

```
electrical s,d,g;
branch(d,s)             ds;
branch(g,s)             gs;

/************ Parameter Definition **********************
type     Type of tunnel FET     [n or p type]
mr               tunnel mass    [*m0]
Eg               Effective tunnel bandgap       [eV]
Tch              Device thickness       [um]
W                Device width   [um]
Gamma    Turn-on Superlinearity [V]
lambda   [V]
Voff     [V]
Vth              Threshold voltage      [V]
ga1              Vds-E field factor     [V^-1]
ga2              Vgs-E field factor     [V^-1]
F0               E-field at zero Vgs and Vds    [V/m]
Umin     min U in SS    [V]
Ua      [V]
U_V0     change of SS with Vgs  [V]
NDR_Voff Off-set in Vds for gVds        [V]
NDR_V0   change of gVds with Vds        [V]
*****************************************************/
// Note: to define an symmetric n/p FET, just change type to "p"
   without changing other parameters
parameter string type = "n"             from {"n","p"};
parameter real mr = 0.0218              from (0:inf);
parameter real Eg = 0.16                from (0:inf);
parameter real Tch = 5e-3               from (0:inf);
parameter real W = 1                    from (0:inf);

parameter real Gamma = 0.04344  from (0:inf);
parameter real lambda = 0.2464  from (-inf:inf);
parameter real alpha_THDS = -4.61       from (-inf:inf);
parameter real Voff = 0         from (-inf:inf);
parameter real Vth = 0.01627    from (-inf:inf);
parameter real ga2 = 1.241              from [0:inf);
parameter real ga1 = 0                  from [0:inf);
parameter real F0 = 3.522e7             from (0:inf);
// For Modified U function
parameter real Umin = 0.0064    from (0:inf);
parameter real Ua = 0.0035              from (0:inf);
parameter real U_V0 = 0.0245    from (-inf:inf);
// For modified VTW
parameter real NDR_Voff = -0.1111       from (-inf:inf);
parameter real NDR_V0 = 0.03558         from (0:inf);

real kT,hbar;
real vgs,vds;
real mR,gVds, a,b,F,U,VTW,f,VthDS,sign, Ids;
real vgse,vdse,Delta, Vmin;
analog begin
        Delta = 5;
        Vmin = 0.001;
        if (type == "n")
                sign = 1;
        else if (type == "p")
                sign = -1;

        vgs = V(gs)*sign;
        vds = V(ds)*sign;
// To prevent F to go to negative:
        vgse = Vmin*(1+0.5*vgs/Vmin+sqrt(Delta*Delta+(0.5*vgs/Vmin-1)
           *(0.5*vgs/Vmin-1)));
```

```
        vdse = Vmin*(1+0.5*vds/Vmin+sqrt(Delta*Delta+(0.5*vds/Vmin-1)
            *(0.5*vds/Vmin-1)));

        kT = `P_K*300;
        hbar = 6.63e-34/2/3.14;

        mR = `m0*mr;
        a = (W*1e-6)*(Tch*1e-6)*pow(`q,3)/8/pow(`M_PI,2)/pow(hbar,2)*
            sqrt(2*mR/Eg/`q);
        b = 4*sqrt(2*mR)*sqrt(pow(Eg,3)*`q)/3/hbar;
        F = F0*(1+ga1*vdse+ga2*vgse);
// F = F0*(1+ga1*vds+ga2*vgs);
        U = Umin + Ua * (tanh((vgs-Vth)/U_V0)+1)/2;

        gVds = (tanh((vds-NDR_Voff)/NDR_V0)+1)/2;
        VTW = U * ln(1+exp((vgs-Vth)/U)) * gVds;
// VthDS = lambda*tanh((vgs-Voff));
        VthDS = lambda/2*(1+tanh(alpha_THDS*(vgs-Voff)));
        f = (1-exp(-vds/Gamma))/(1+exp((VthDS-vds)/Gamma));
        Ids = a*f*VTW*F*exp(-b/F);
        I(ds) <+ sign*Ids;              // [A] Tunnel current
        I(ds) <+ white_noise(abs(2*`P_Q*Ids/tanh((vds*`P_Q)/2/kT)),"
            shot");             // [A^2/Hz]
// I(ds) <+ white_noise(abs(2*`P_Q*Ids),"shot");                // [A
    ^2/Hz]
        I(gs) <+ 0;

end
endmodule
```

B.2 2-D FET Model

```
/* ---------------- 2015-Aug-05 -------------
This Verilog-A describes IV of a 2D N-MOSFET device with top and
    bottom gate contact
- source (s), drain (d), top gate (g), bottom gate (b)
/* ---------------- 2015-Aug-21 -------------
Adding 2D P-MOSFET device to enable both types of device
- type = "n"            from{"n","p"}
Author: Jie Min
Advisor: Peter M. Asbeck
Affiliation: University of California, San Diego
---------------------------------------------- */
/* ---------------- 2016-Jul-01 -------------
- Modifying SS60 for continuous transconductance
---------------------------------------------- */
`include "disciplines.vams"
`include "constants.vams"

`define m0 9.1e-31
`define q 1.6e-19
module FET2D(s,d,g,b);

inout s,d,g,b;
electrical s,d,g,b;
branch(d,s)             ds;
branch(g,s)             gs;
branch(b,s)             bs;

/************ Parameter Definition ************************
```

```
type     type of MOSFET
W                Channel width
                   [um]
L                Channel length
                   [um]
tt               Top gate thickness
                   [m]
tb               Bottom gate thickness
           [m]
epst_r   Top gate permittivity                                    [1]
tb               Bottom gate permittivity
           [1]
Vgs0
                           [V]
Vbs0
                           [V]
m_r              DOS effective mass/m0
           [1]
Eg               Band gap
                           [eV]
mu               Electron mobility
                   [m^2/Vs]
*********************************************************/
parameter string type = "n"                       from {"n","p"};
parameter real W=1                                        from (0:inf);
parameter real L=0.1                              from (0:inf);
parameter real tt = 17.5e-9                       from (0:inf);
parameter real tb = 270e-9                        from (0:inf);
parameter real epst_r = 12.5            from (0:inf);
parameter real epsb_r = 3.9                       from (0:inf);
parameter real Vgs0 = -1                          from (-inf:inf);
parameter real Vbs0 = -1                          from (-inf:inf);
parameter real m_r = 0.64                         from (0:inf);
parameter real Eg = 1.64                          from (0:inf);
parameter real mu = 250e-4                        from (0:inf);

// Fermi-dirac distribution function
analog function real f0;
input Vc,E0,kT,type;
real Vc,E0,kT;
string type;
begin
        if (type == "n") begin
                f0 = 1/(1+exp((-`q*Vc+E0)/kT));
        end
        else if (type == "p") begin
                f0 = 1/(1+exp((-`q*Vc-E0)/kT));
        end
end
endfunction

// Absolute function
analog function real absolute;
input x;
real x;
begin
        if(x>=0)
                absolute = x;
        else
                absolute = -x;
end
endfunction

// Newton's method to find Vc from bias condition and parameters
```

```
analog function real FindVc;
input Vp,Vgs,Vbs,Ct,Cb,D0,E0,Vgs0,Vbs0,kT,type;
real Vp,Vgs,Vbs,Ct,Cb,D0,E0,Vgs0,Vbs0,kT;
string type;
real nVp, nVgs, nVbs,nVgs0,nVbs0,nVc,Vc,Cq0,flag,itr,F,Fprime;
begin
        nVgs = Vgs*`q/kT;
        nVbs = Vbs*`q/kT;
        nVp = Vp*`q/kT;
        nVgs0 = Vgs0*`q/kT;
        nVbs0 = Vbs0*`q/kT;
        Cq0 = `q*`q*D0;
        nVc = Ct/(Ct+Cb)*(nVgs-nVp-nVgs0)+Cb/(Ct+Cb)*(nVbs-nVp-nVbs0)
            ;
        flag = 0;               // flag determines whether it meets
            Convergence requirement
        itr = 0;
        if (type == "n") begin
                while(flag == 0) begin
                        Vc = nVc/`q*kT;
                        F = (Ct+Cb)/Cq0*nVc-ln(1-f0(Vc,E0,kT,type))-
                            Ct/Cq0*(nVgs-nVp-nVgs0)-Cb/Cq0*(nVbs-nVp-
                            nVbs0);
                        Fprime = (Ct+Cb)/Cq0+f0(Vc,E0,kT,type);
                        nVc = nVc-F/Fprime;
                        if (absolute(F/Fprime)<0.0001)
                                flag=1;
                        if (flag==0) begin
                                itr = itr+1;
                                if (itr>20) begin
                                        flag = -1;
                                        $display("Iteration step
                                            greater than 20. Exit
                                            Newton itration");
                                end
                        end
                end
        end
        if (type == "p") begin
                while(flag == 0) begin
                        Vc = nVc/`q*kT;
                        F = (Ct+Cb)/Cq0*nVc+ln(f0(Vc,E0,kT,type))-Ct/
                            Cq0*(nVgs-nVp-nVgs0)-Cb/Cq0*(nVbs-nVp-
                            nVbs0);
                        Fprime = (Ct+Cb)/Cq0+(1-f0(Vc,E0,kT,type));
                        nVc = nVc-F/Fprime;
                        if (absolute(F/Fprime)<0.0001)
                                flag=1;
                        if (flag==0) begin
                                itr = itr+1;
                                if (itr>20) begin
                                        flag = -1;
                                        $display("Iteration step
                                            greater than 20. Exit
                                            Newton itration");
                                end
                        end
                end
        end
        Vc = nVc/`q*kT;
        FindVc = Vc;
end
endfunction
```

```
// Function to calculate diffusion current component in Drift-
   diffusion model, showing 60mV/dec in SS region
analog function real SS60;
input Vc,E0,kT,type;
real Vc,E0,kT;
// real temp,tempQ;
string type;
real alpha,dv,zeta,vc1,vc2,vc,sign;
begin
if (type == "n") begin
        // sign = 1
        alpha = +2.358;
        zeta = -0.5896;
        dv = -1.5;
        vc = (Vc-E0/`q)/kT*`q;
        vc2 = alpha+dv;
        vc1 = -vc2;
        if (vc >= vc2) begin
                SS60 = +((vc*vc+vc2*vc2)/2-vc2*vc2*vc2/3/alpha+2*(1+
                   vc2)*(exp(-vc2)+zeta/4*exp(-2*vc2)) - (exp(-vc)+
                   zeta/4*exp(-2*vc))+vc2*zeta/2*exp(-2*vc2));
        end
        else if (vc>vc1 && vc<vc2) begin
                SS60 = +(-(-vc-vc2)*(-vc-vc2)*(-vc+2*vc2-3*alpha)/12/
                   alpha+zeta/4*exp(-2*vc2)*(1+2*vc+2*vc2)+ exp(-vc2)
                   *(1+vc+vc2));
        end
        else
                SS60 = +(exp(vc)+0.25*zeta*exp(2*vc));
end
else if (type == "p") begin
        alpha = 2.358;
        zeta = -0.5896;
        dv = -1.5;
        vc = (Vc+E0/`q)/kT*`q;
        vc2 = alpha+dv;
        vc1 = -vc2;
        if (vc<=vc1)
                SS60 = +((vc*vc+vc2*vc2)/2-vc2*vc2*vc2/3/alpha+2*(1+
                   vc2)*(exp(-vc2)+zeta/4*exp(-2*vc2)) - (exp(vc)+
                   zeta/4*exp(2*vc))+vc2*zeta/2*exp(-2*vc2));
        else if(vc>vc1 && vc<vc2)
                SS60 = +(-(vc-vc2)*(vc-vc2)*(vc+2*vc2-3*alpha)/12/
                   alpha+zeta/4*exp(-2*vc2)*(1-2*vc+2*vc2)+ exp(-vc2)
                   *(1-vc+vc2));
        else
                SS60 = +(exp(-vc)+0.25*zeta*exp(-2*vc));
        end
end
endfunction

real kT,hbar;
real vgs,vbs,vds;
real Term1,Term2;
real E0,D0,Ct,Cb,Qs,Qd,Qtot;
real polarity,IdTerm1,IdTerm2;
real vcd = 0;
real vcs = 0;
analog begin
        vgs = V(gs);
        vbs = V(bs);
        vds = V(ds);

// Initialize vcd and vcs
```

```
        vcd = vds;
        vcs = vds;

        kT = `P_K*300;
        hbar = 6.63e-34/2/3.14;
        D0 = m_r*`m0/`M_PI/hbar/hbar;
        Ct = epst_r*`P_EPS0/tt;
        Cb = epsb_r*`P_EPS0/tb;
        E0 = `q*Eg/2;
// Calculate Vc, the difference between local Ei and Ef
        vcs = FindVc(0,vgs,vbs,Ct,Cb,D0,E0,Vgs0,Vbs0,kT,type);
        vcd = FindVc(vds,vgs,vbs,Ct,Cb,D0,E0,Vgs0,Vbs0,kT,type);
// Calculate charge at source and charge at drain
        Qs = `q*D0*kT*ln(1-f0(vcs,E0,kT,type));
        Qd = `q*D0*kT*ln(1-f0(vcd,E0,kT,type));
        Qtot = (Qs+Qd)/2;

        Term1 = (SS60(vcd,E0,kT,type)-SS60(vcs,E0,kT,type));
        if (type == "n") begin
                Term2 = D0/(Ct+Cb)*(pow(ln(1-f0(vcd,E0,kT,type)),2)-
                   pow(ln(1-f0(vcs,E0,kT,type)),2))/2*(pow(`q,2));
        end
        else if (type == "p") begin
                Term2 = D0/(Ct+Cb)*(pow(ln(f0(vcd,E0,kT,type)),2)-pow
                   (ln(f0(vcs,E0,kT,type)),2))/2*(pow(`q,2));
        end

        if (type == "n")
                polarity=-1;
        else if(type == "p")
                polarity=1;

        IdTerm1 = polarity*mu*(W*1e-6)/(L*1e-6)*D0*kT*kT*(Term1);
        IdTerm2 = polarity*mu*(W*1e-6)/(L*1e-6)*D0*kT*kT*(Term2);
        I(ds) <+ polarity*mu*(W*1e-6)/(L*1e-6)*D0*kT*kT*(Term1+Term2)
           ;                    // [A]
        I(ds) <+ white_noise(polarity*(W*1e-6)/(L*1e-6)*4*`P_K*300*mu
           *Qtot,"thermal");          // [A^2/Hz]
        I(bs) <+ 0;
        I(gs) <+ 0;
end
endmodule
```

B.3 2-D FET Capacitance Model

```
/* ---------------- 2015-Aug-05 --------------
This Verilog-A describes capacitance network for an intersection of 2
   D MOSFET
- There are three terminals: top gate (g), bottom gate (b), and
   channel potential (s)
- Quantum capacitance is taken into consideration implicitly by
   taking into account the effect of "vcs"
- "vcs" can be considered as the voltage drop across "quantum
   capacitance"
/* ---------------- 2015-Aug-21 --------------
Adding 2D P-MOSFET device to enable both types of device
- type = "n"            from{"n","p"};
Author: Jie Min
Advisor: Peter M. Asbeck
Affiliation: University of California, San Diego
```

```
---------------------------------------------- */

`include "disciplines.vams"
`include "constants.vams"

`define m0 9.1e-31
`define q 1.6e-19
module FET2D_CNetwork(s,g,b);

inout s,g,b;
electrical s,g,b;
branch(g,s)             gs;
branch(b,s)             bs;

/************ Parameter Definition ************************
type     type of MOSFET
W                Channel width
                   [um]
L                Channel length
                   [um]
tt               Top gate thickness
                   [m]
tb               Bottom gate thickness
          [m]
epst_r   Top gate permittivity                                  [1]
tb               Bottom gate permittivity
          [1]
Vgs0
                           [V]
Vbs0
                           [V]
m_r      DOS effective mass/m0                                  [1]
Eg               Band gap
                           [eV]
mu               Electron mobility
                   [m^2/Vs]
*********************************************************/
parameter string type = "n"                     from {"n","p"};
parameter real W = 1                            from (0:inf);
parameter real L=0.1                            from (0:inf);
parameter real tt = 17.5e-9                     from (0:inf);
parameter real tb = 270e-9                      from (0:inf);
parameter real epst_r = 12.5            from (0:inf);
parameter real epsb_r = 3.9                     from (0:inf);
parameter real Vgs0 = -1                        from (-inf:inf);
parameter real Vbs0 = -1                        from (-inf:inf);
parameter real m_r = 0.64                       from (0:inf);
parameter real Eg = 1.64                        from (0:inf);
parameter real mu = 250e-4                      from (0:inf);

// Fermi-dirac distribution function
analog function real f0;
input Vc,E0,kT,type;
real Vc,E0,kT;
string type;
begin
        if (type == "n") begin
                f0 = 1/(1+exp((-`q*Vc+E0)/kT));
        end
        else if (type == "p") begin
                f0 = 1/(1+exp((-`q*Vc-E0)/kT));
        end
end
endfunction
```

```
analog function real absolute;
input x;
real x;
begin
        if(x>=0)
                absolute = x;
        else
                absolute = -x;
end
endfunction

analog function real FindVc;
input Vp,Vgs,Vbs,Ct,Cb,D0,E0,Vgs0,Vbs0,kT,type;
real Vp,Vgs,Vbs,Ct,Cb,D0,E0,Vgs0,Vbs0,kT;
string type;
real nVp, nVgs, nVbs,nVgs0,nVbs0,nVc,Vc,Cq0,flag,itr,F,Fprime;
begin
        nVgs = Vgs*`q/kT;
        nVbs = Vbs*`q/kT;
        nVp = Vp*`q/kT;
        nVgs0 = Vgs0*`q/kT;
        nVbs0 = Vbs0*`q/kT;
        Cq0 = `q*`q*D0;
        nVc = Ct/(Ct+Cb)*(nVgs-nVp-nVgs0)+Cb/(Ct+Cb)*(nVbs-nVp-nVbs0)
            ;
        flag = 0;               // flag determines whether it meets
            Convergence requirement
        itr = 0;
        if (type == "n") begin
                while(flag == 0) begin
                        Vc = nVc/`q*kT;
                        F = (Ct+Cb)/Cq0*nVc-ln(1-f0(Vc,E0,kT,type))-
                            Ct/Cq0*(nVgs-nVp-nVgs0)-Cb/Cq0*(nVbs-nVp-
                            nVbs0);
                        Fprime = (Ct+Cb)/Cq0+f0(Vc,E0,kT,type);
                        nVc = nVc-F/Fprime;
                        if (absolute(F/Fprime)<0.001)
                                flag=1;
                        if (flag==0) begin
                                itr = itr+1;
                                if (itr>20) begin
                                        flag = -1;
                                        $display("Iteration step
                                            greater than 20. Exit
                                            Newton itration");
                                end
                        end
                end
        end
        if (type == "p") begin
                while(flag == 0) begin
                        Vc = nVc/`q*kT;
                        F = (Ct+Cb)/Cq0*nVc+ln(f0(Vc,E0,kT,type))-Ct/
                            Cq0*(nVgs-nVp-nVgs0)-Cb/Cq0*(nVbs-nVp-
                            nVbs0);
                        Fprime = (Ct+Cb)/Cq0+(1-f0(Vc,E0,kT,type));
                        nVc = nVc-F/Fprime;
                        if (absolute(F/Fprime)<0.001)
                                flag=1;
                        if (flag==0) begin
                                itr = itr+1;
                                if (itr>20) begin
                                        flag = -1;
```

```
        $display("Iteration step greater than 20. Exit Newton
           itration");
                                end
                        end
                end
        end
        Vc = nVc/`q*kT;
        FindVc = Vc;
end
endfunction

real kT,hbar;
real vgs,vbs;
real E0,D0,Ct,Cb,Qg,Qb;
real vcd = 0;
real vcs = 0;
analog begin
        vgs = V(gs);
        vbs = V(bs);

// Initializing vcs
        vcs = 0;
        kT = `P_K*300;
        hbar = 6.63e-34/2/3.14;
        D0 = m_r*`m0/`M_PI/hbar/hbar;
        Ct = epst_r*`P_EPS0/tt;
        Cb = epsb_r*`P_EPS0/tb;
        E0 = `q*Eg/2;
// Calculate Vc, the difference between local Ei and Ef
        vcs = FindVc(0,vgs,vbs,Ct,Cb,D0,E0,Vgs0,Vbs0,kT,type);
// Calculate charge at top and back gate
        Qg = Ct*(vgs-Vgs0-vcs)*(L*1e-6)*(W*1e-6);
        Qb = Cb*(vbs-Vbs0-vcs)*(L*1e-6)*(W*1e-6);

// AC current is the derivative of Qb and Qg
        I(bs) <+ ddt(Qb);
        I(gs) <+ ddt(Qg);

end
endmodule
```