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A 24-Channel Digitizer with a JESD204B Compliant Serial Interface for High-Speed Detectors

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***Abstract*— A 24-channel application specific integrated circuit (ASIC) for the readout of high-speed CMOS active pixel sensors for charged particle detection is presented. The chip comprises 24 preamplifiers, 24 distinct 12-bit, 25 MSPS Pipelined Analog-to-Digital Converters (ADCs) with self-calibration, an internal PLL, and a 3 Gbps serial interface that conforms to the JESD204B standard. To simplify interfacing with a variety of sensors, the ASIC also includes an automatic offset calibration loop. The high-level of integration of the ASIC reduces overall system cost and area, and exploiting the signal characteristics of the image sensor allows the ADC to be optimized for reduced power dissipation. The use of an integrated serializer and an industry standard protocol simplifies integration of the ASIC into a complete camera system. The ASIC, called the High-Speed Image Preprocessor Targeted for Electron Readout, or HIPSTER, with a die area of 64.26 mm^2, is packaged in a 480-ball BGA and is fabricated in 180 nm CMOS technology. HIPSTER achieves typical DNL < 0.55 LSB, input-referred thermal noise of 114.5 µV-rms, and a BER of better than 10^{-14}. The power dissipation is 98 mW / channel.**

Index Terms—Mixed-Signal IC Design; Data Conversion; Solid-State Imaging; CMOS Image Sensors

I. Introduction

High-speed CMOS image sensors are becoming increasingly important in scientific imaging applications. The ability to make movies of dynamic processes is helping to enable new science. Key applications of high-speed image sensors include material science, medical imaging and electron microscopy. The clear trend in image sensor design is to implement column-parallel arrays of Analog-to-Digital Converters (ADCs) on the same die as the imaging array [1]. However, for many scientific applications, maximizing imaging area is critical, and off-chip digitization both maximizes the imaging area and provides the highest overall framerate [2]. It is also important that the readout electronics are low noise to accommodate high dynamic range sensors.

In this work we report a highly integrated 24-channel image sensor readout Application-Specific Integrated Circuit (ASIC) intended for reading out high-speed image sensors with analog signal outputs. The ASIC includes 24 channels of programmable preamplifiers and ADCs, automatic calibration of the sensor DC offset and ADC linearity, and six programmable 3 Gbps high-speed serial interfaces that conform to the JESD204B protocol standard.

Due to the high level of integration in the ASIC, power dissipation is an important consideration. We use several techniques to reduce the power of the ASIC. First, the front-end preamplifiers use a resistively loaded open-loop topology. This is possible because the target application of the ASIC is readout of high-speed CMOS image sensors for charged particle detection. Because these sensors have a thin sensitive volume, the deposited energy has significant fluctuations [3]. This means only moderate linearity is required for the readout and this fact is exploited to reduce the power dissipation of the ASIC. Second, the ADC employs a simple calibration to allow the use of lower gain internal amplifiers than would be required if the full ADC performance were determined by raw analog performance. Finally, the ASIC serializer includes a transmit equalization function that allows the output buffer current to be lowered, further reducing power dissipation.

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II. HIPSTER

A. Chip Architecture

A block diagram of the ASIC, titled the High-Speed Image Preprocessor Targeted for Electron Readout, or HIPSTER, is shown in Fig. 1. The chip comprises 24 identical channels. Each channel contains a programmable gain amplifier (PGA) with an offset-correction input. This allows a wide variety of CMOS image sensors to be read out using HIPSTER. Each PGA is followed by a calibrated 12-bit, 25 MSPS Pipelined ADC. The output of each ADC is combined in packets and serialized by a 3 Gbps transmitter that conforms to the JESD204B standard. HIPSTER also includes a programmable PLL-based frequency synthesizer that generates clocks for the ADCs, the digital logic, and the serial interface. The chip is configured using a Serial-Peripheral Interface (SPI).

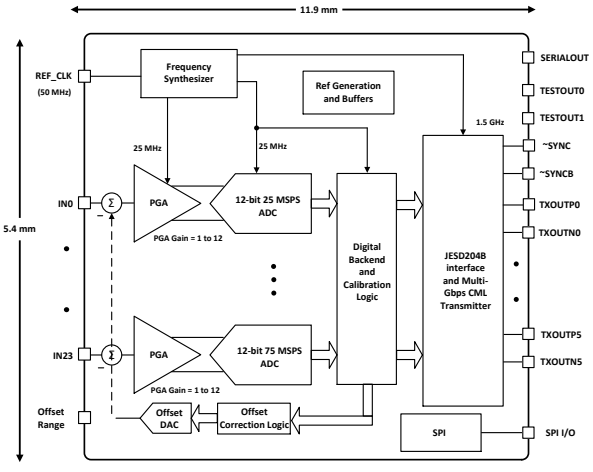

Fig. 1. HIPSTER ADC ASIC block diagram.

B. Programable Gain Amplifer

In order to deal with challenging noise specifications, the analog front end of HIPSTER is designed to maximize the dynamic range of the ADC by including a PGA to provide gain before the ADC. A block diagram of the PGA is shown in Fig. 2. The PGA performs three functions. First, it maps the image sensor's signal range to the dynamic range of the ADC through selectable gain and an automatic offset calibration loop that allows HIPSTER to adapt to the different DC output levels of different image sensors. Second, the PGA provides a sample-and-hold function for the following ADC. Third, the PGA provides the necessary single-ended-to-differential conversion function to match the fully differential ADC input to the inherently single-ended output of the CMOS image sensor.

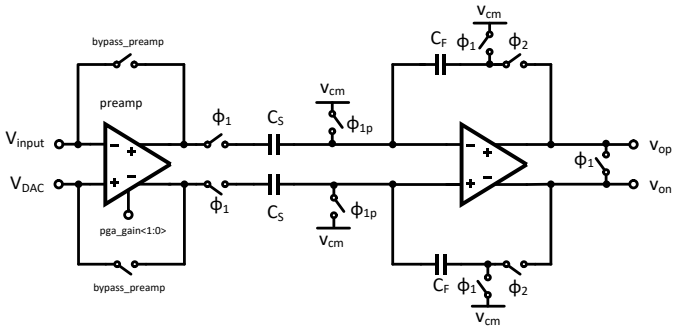

Fig. 2. Programmable Gain Amplifier implemented as a continuous-time preamplifier followed by switched-capacitor Sample-and-Hold.

The PGA is implemented as a continuous-time preamplifier followed by a switched-capacitor Sample-and-Hold amplifier that uses a two-phase non-overlapping clock. The continuous-time preamplifier, implemented as an open-loop preamplifier with selectable gain, provides single-ended to differential conversion. The continuous-time preamplifier can be bypassed, in which case the single-ended to differential conversion is done by the Sample-and-Hold stage. The schematic of the continuous-time preamplifier is shown in Fig. 3.

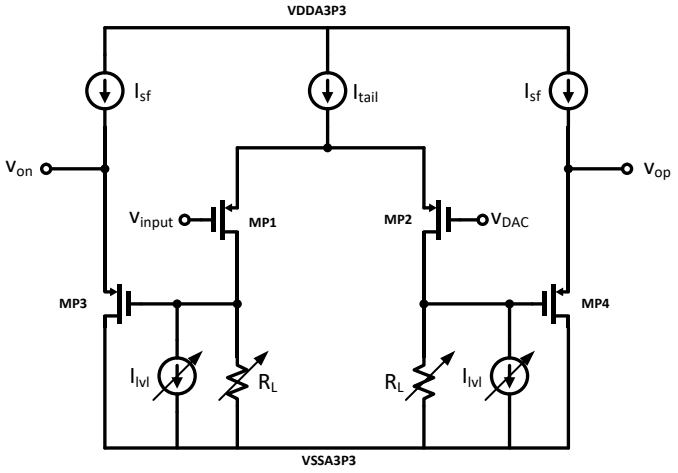

Fig. 3. Open-Loop Preamplifier.

The continuous-time, open-loop PGA preamplifier consists of a resistively loaded differential pair driving two source-follower buffers. Adjustable current sources in parallel with the variable resistors provide level shifting.

A continuous-time preamplifier was chosen for the PGA for two reasons. First, a continuous-time circuit provides a well-behaved load to the image sensor output driver and isolates the image sensor from switched-capacitor induced kickback. Second, and more importantly, it is possible to achieve lower noise performance using a resistively loaded differential pair than it is with a switched capacitor stage for a given power dissipation. Since the rms noise of a switched-capacitor circuit is proportional to $\sqrt{kT/C}$, achieving an rms noise of 50 μV-rms would require a capacitor of at least 1.6 pF. Therefore, to meet the challenging noise specifications at a practical power level, the PGA preamplifier is implemented using continuous-time techniques.

C. Offset Calibration Loop

While the use of a PGA as the front end of HIPSTER relaxes the noise requirements on the ADC, it also has the effect of exacerbating offset issues because any offset between the sensor output and the input common-mode level sees gain before it is digitized. This can limit the achievable dynamic range of the system; therefore HIPSTER includes an automatic offset cancellation capability.

Many CMOS Active Pixel Sensor imagers provide dark pixels that provide a reference level that can be used to drive the offset correction. However, charge injection causes differences between the reference level output and the pixel output of up to 500 mV in practice. Therefore, the offset correction in HIPSTER is programmable. A block diagram of the offset correction loop is shown in Fig. 4.

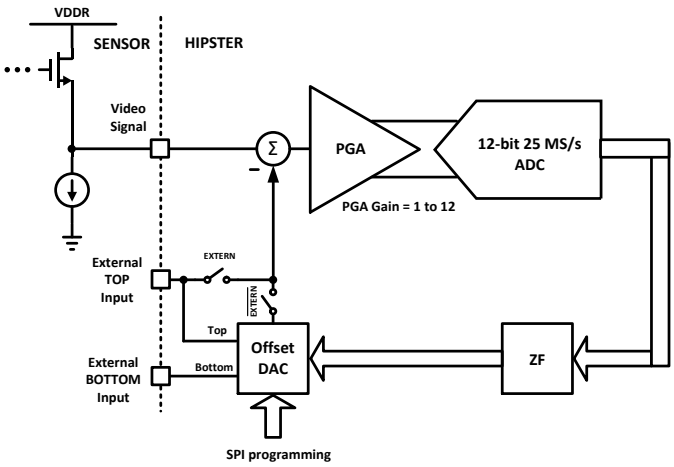

Fig. 4. Offset-Calibration Loop Block Diagram.

The offset-calibration loop uses a simple zero-forcing algorithm [4]. The sensor output is connected to the analog channel and the digital output of the ADC is processed by a zero-forcing block (labeled ZF) that drives a DAC to subtract the estimated offset from the PGA input. This feedback loop drives the offset seen by the ADC to zero. For this to work, the

sensor must not be exposed to light during calibration. The dynamic range of the Offset DAC is programmable via the external TOP and BOTTOM connections to accommodate a wide variety of sensor DC voltage levels. The residual offset between channels is dominated by the resolution of the Offset DAC as the raw offset of the various channels is on the level of mV. The offset of the PGA itself is sampled on C_S (see Fig. 2) and removed so the inherent offset of each channel is small (in other words the offset of interest is the offset between the sensor output and the HIPSTER common-mode input level).

As example of why automatic offset calibration is important, if the offset of a channel is 200 mV relative to the input common-mode voltage, and the PGA gain is 4, the offset at the input of the ADC is 800 mV. Since the full-scale range of the ADC is 3 Vpp-diff, this offset would eat up over a quarter of the system's dynamic range without offset-calibration.

While it is possible for this calibration to be done entirely internal to HIPSTER, it is still important to monitor the ADC outputs to ensure that the offset level is not changing during normal operation because of temperature changes, for example. The Offset DAC itself is somewhat sensitive to temperature variations (on the order of 0.1% per degree C). To address these potential issues, the correction loop can be implemented partially in software (the ZF block) if desired. In this mode, the offset DAC values can be calculated in software and then loaded into HIPSTER through the SPI and the on-chip zero-forcing loop can be disabled. This also opens the possibility of more advanced convergence algorithms (such as those based on gradient descent) to be used if required.

To provide maximum flexibility, the Offset DAC output for each channel can be overwritten by a single analog input common to each channel. This analog voltage should be lower noise than the overall input-referred noise specification as the noise is injected at the input of the analog front end.

D. Analog-to-Digital Converter

The ADC used in this work is a 12-bit, 25 MSPS Pipelined ADC optimized for low-noise and differential nonlinearity (DNL) performance. Because the sensors themselves are nonlinear, the specification on the integral nonlinearity (INL) is greatly relaxed. The relaxed INL specification allows the use of lower-gain and lower-power internal amplifiers than would be required if good INL were important.

The ADC was developed using a modular architecture that allowed rapid design and layout via semi-automated software scripts. The design details of the ADC as well as performance measurements for the fabricated ADC itself are reported in [5]. The ADC consists of 15 unit cells of 1.5 bits/stage. The 15 stages provide 16 bits of raw data per conversion. The additional resolution is required by the calibration used to compensate for capacitor mismatch and low op-amp gain. The ADC is calibrated using a simple foreground approach that measures the closed-loop gains of the stages [6].

The ADC reference voltages are generated using a simple CMOS reference circuit and buffered on-chip using class A amplifiers. The schematic for the reference buffers used is shown in [5].

E. Frequency Synthesizer

HIPSTER uses an on-chip frequency synthesizer to generate the required clocks for the ADC, the digital logic, and the high-speed serial data transmitter. The core of the frequency synthesizer is a phase-locked-loop (PLL) that is implemented using a ring-oscillator-based voltage controlled oscillator (VCO).

A block diagram of the frequency synthesizer is shown in Fig. 5. The divide ratio is programmable to enable different JESD204B lane configurations.

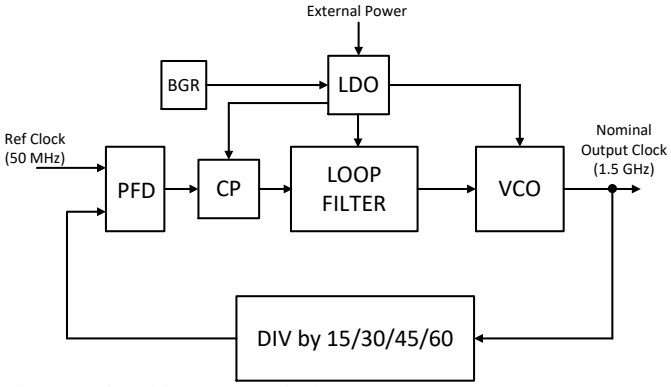

Fig. 5. PLL-based frequency synthesizer.

In the nominal locked condition, the VCO runs at 1.5 GHz. This is the speed required to achieve a data rate of 3 Gbps with the Double Data Rate (DDR) transmitter topology used in HIPSTER. During operation, the output of the frequency divider block is compared to the 50 MHz reference clock by the phase-frequency detector (PFD). The PFD drives a charge pump (CP) whose output is a packet of charge proportional to the phase difference between the divided down clock and the reference clock. The charge pump output is integrated by a loop filter to generate a voltage that controls the VCO frequency. This voltage is continually adjusted by the loop until the VCO is tuned to the desired output frequency. The low dropout voltage regulators (LDOs) and bandgap reference (BGR) supply clean power to the CP, loop filter, and VCO in order to reduce output jitter.

The Voltage Controlled Oscillator (VCO) generates the synthesized high-frequency clock. For lowest phase noise, an LC-based VCO is typically used because its higher Q gives it lower phase noise than a wideband ring oscillator [7]. A ring-oscillator VCO is chosen for HIPSTER for three main reasons. First, it is simpler so is more likely to work in first silicon. Second, a ring oscillator VCO has a wider tuning range than an LC oscillator [7]. Third, it is easier to tune a ring-oscillator over a wide range than it is to tune an LC oscillator. Because there is a strong desire for HIPSTER to be as flexible as possible, and analysis indicated that the phase noise of a ring

oscillator was sufficiently low in this 180 nm CMOS process to meet communication speed and bit-error-rate requirements, a ring oscillator VCO makes sense here. For improved process independence, the VCO delay cells are implemented using replica biasing [8].

To maintain sufficiently good phase performance, the PLL VCO requires a stable supply voltage. To provide a stable supply voltage, HIPSTER uses an on-chip low-dropout voltage regulator (LDO). The LDO is implemented using a standard architecture [9].

F. Digital Backend

A block diagram of the Digital Backend of the HIPSTER ASIC is shown in Fig. 6. The chip is configured using the SPI. All the configuration and calibration registers share a single internal 24-bit bus. Both the SPI and the calibration logic can write to the calibration registers, which allows both on-chip and off-chip calibration of the ADC and channel offset. Race conditions from clock domain crossings are avoided through the use of a mailbox register. The mailbox register is an intermediate dual-port register than allows both the SPI and the finite state machines that calibrate the ADC interact with the register file (on-chip memory) safely.

The raw digital ADC decision bits are transformed into corrected bits using the correction logic, the output of which is sent to the JESD204B encoding logic.

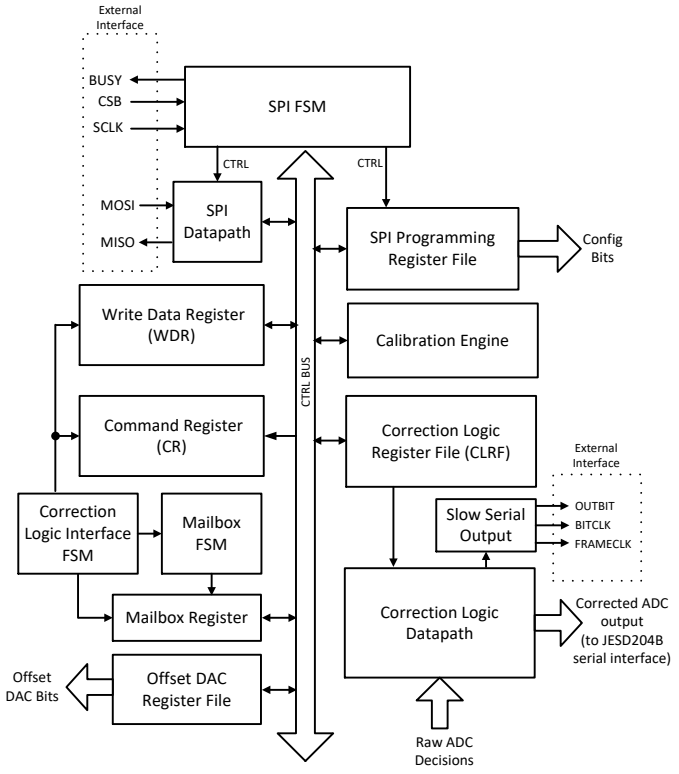

Fig. 6. HIPSTER Digital Backend Logic

The Digital Backend also includes a test and evaluation interface called the Slow Serial Output (SSO). The SSO is shown in Fig. 7. Any individual ADC output can be examined before or after calibration using a simple CMOS clock-forwarded protocol that does not depend on the JESD204B encoding or the high-speed multi-Gb serial transmitter. The SSO is intended as a debugging interface. It operated as expected but was not used in the evaluation of HIPSTER as the high-speed interface was functional on first-silicon.

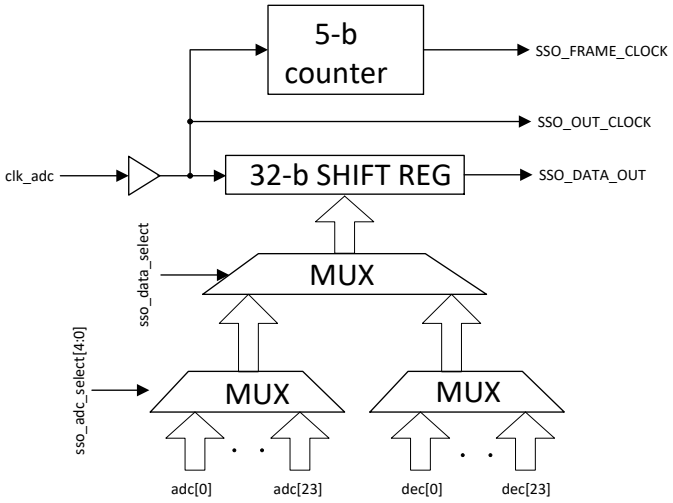

Fig. 7. Slow Serial Output (SSO) for ADC test and evaluation

G. JESD204B Transmit Encoder

HIPSTER uses a custom implementation of the JESD204B protocol, an established industry protocol for serial communication between data converters and processors. The protocol includes facilities for DC balancing (8b/10b coding), channel bonding, link synchronization, data scrambling, and diagnostics [10]. Using the JESD204B protocol enables HIPSTER to leverage proven techniques for data converter serial readout and simplifies system integration.

A block diagram of the JESD204B interface where 24 channels of ADC data are matched to a variable number of physical transmit lanes is shown in Fig. 8.

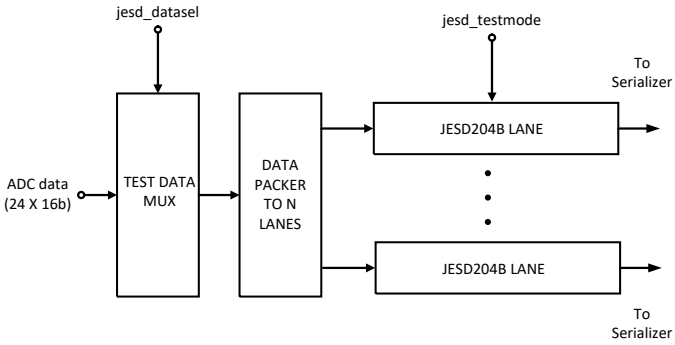

Fig. 8. JESD204B Transmit Interface.

24 channels of 16-bit ADC data (recall the uncorrected output of the ADC is 16 bits) are sent to a mux that allows injection of test ADC data directly into the JESD204B interface. A data packer reduces the ADC data to 12-bits and assigns the data to the number of JESD204B lanes used. Using a variable number of transmit lanes increases the flexibility of HIPSTER by reducing the required amount of interconnect when maximum speed is not required. A block diagram of a single JESD204B lane is shown in Fig. 9.

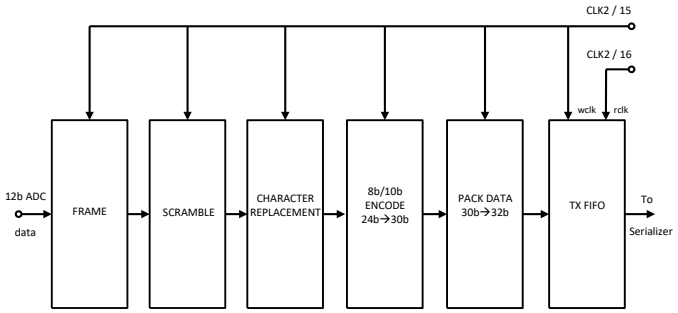

Fig. 9. JESD204B Lane.

The JESD204B lane operates as follows. The calibrated 12-bit ADC data is placed into frames and optionally scrambled. Character replacement is then performed per the JESD204B standard. Each two ADC words are interpreted as three bytes to undergo 8b/10b coding. The data is then packed into 32-bit words and the clock rate is adjusted using a TX FIFO to simplify interface to the custom serializer.

Significant Built-In Self-Test (BIST) capabilities are designed into the HIPSTER JESD204B interface. In addition to a test mode, the JESD204B interface can be configured to transmit configurable simulated ADC or random data. Besides ASIC evaluation, these modes could be useful in full camera evaluation or testing.

H. Serial Digital Transmitter

The transmitter block serializes and drives digital bits off HIPSTER. It is designed for high-performance and pushes the capability of the 180 nm CMOS process used. Because HIPSTER is intended for use in compact cameras, the expected drive length required of the transmitter is limited. However, simulations of the expected attenuation and dispersion of the channel indicated that transmit equalization was required.

A block diagram of the transmitter is shown in Fig. 10.

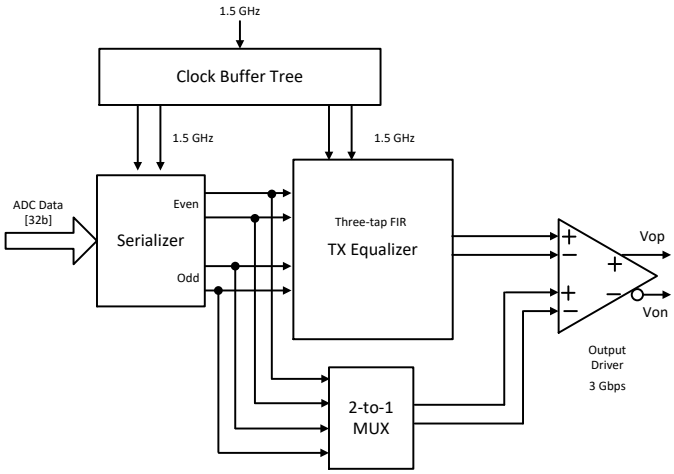

Fig. 10. HIPSTER Digital Transmitter

The inputs to the transmitter are a high-frequency clock generated by the PLL, 32-bit wide data words from the JESD204B lane logic, and various configuration bits. The serializer converts the data to two high-speed serial bit streams (even and odd bits). These serialized bit streams then go through a three-stage Finite Impulse Response (FIR) equalizer that equalizes the signals and combines them into a single bit stream. The FIR equalizer is designed to mitigate intersymbol interference by correcting dispersion in the channel. The raw and equalized signals are then sent through a driver which, through a wired-OR connection, transmits one of them off chip. The raw signal is capable of higher speeds but the equalized signal will be better able to handle dispersion and reflection issues due to the PCB system-level interconnect. All the digital blocks in Fig. 15 are implemented in high-speed current-mode logic (CML) except for the Serializer which is implemented using a combination of CMOS and CML.

To maximize the datarate, the transmitter uses Double Data Rate (DDR) signaling, a scheme in which output bits are updated on both the rising and the falling edge of the master clock.

A block diagram of the multiplexer-based serializer used in HIPSTER is shown in Fig. 11 [11]. The first stage is a CMOS 32-to-16 MUX and the second stage is a CMOS 16-to-8 MUX. Together, these MUXes reduce the 32-bit output words of the JESD204B Protocol Logic to 8-bits at a four times higher rate. The 16-to-8 MUX also includes buffers that convert the data from single-ended CMOS logic levels to differential CML logic levels. The data is then further multiplexed by CML 2-to-1 MUXes that separate the data into even and odd bit streams. These bit streams are then sent to the Transmit Equalizer before being launched by the output driver.

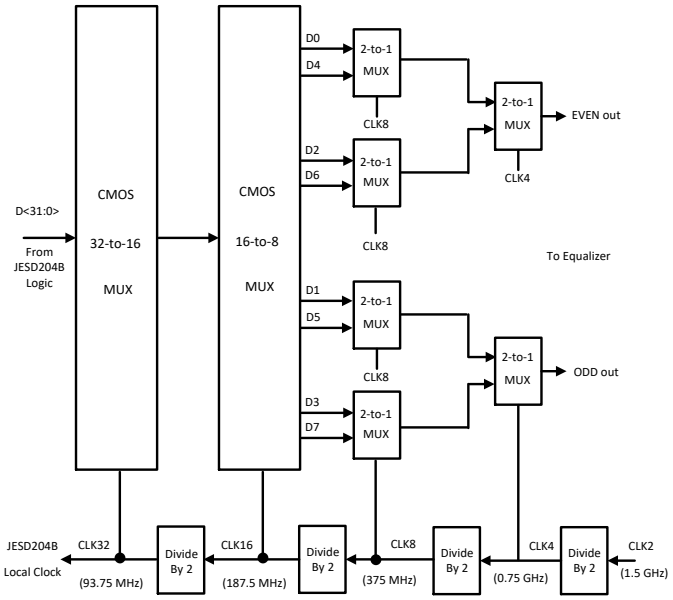

Fig. 11. Multiplexer-Based Serializer

Each rank of the multiplexer operates on a different frequency clock. These clocks are internally generated in the serializer by series-connected divide-by-2 blocks. CLK2 is the half-rate clock used to drive the equalizer (its frequency is one-half the bitrate). The clock is continually divided down until the CLK32 clock is sent to the JESD204B protocol logic.

The Transmit Equalizer that combines the bit streams and provides the required equalization is shown in Fig. 12 [12].

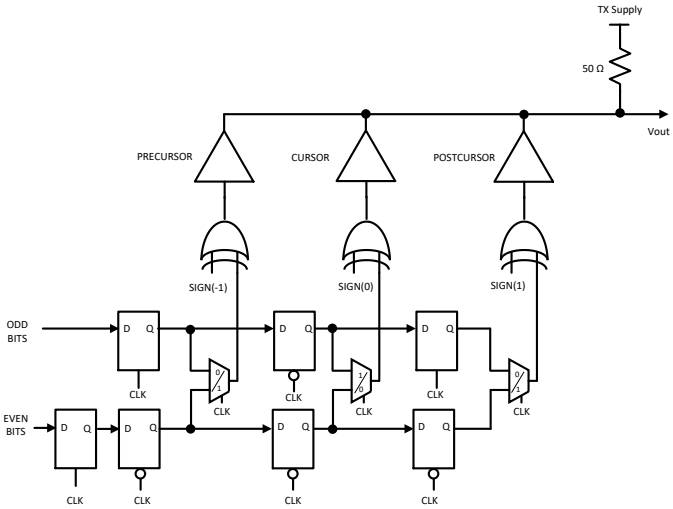

Fig. 12. Transmit Equalizer

The fully differential signal path is shown in single-ended form here for clarity. The equalizer is a baud-rate CML-based design comprising a 3-tap feed-forward equalizer (FFE) with per-tap polarity control. It is implemented using unit-delays and a high-speed current-steering DAC. The z-domain transfer function of the equalizer is

$$W(z) = a_0 + a_1 z^{-1} + a_2 z^{-2}$$

The coefficients a_0, a_1, and a_2 correspond to the weights of the precursor, cursor, and postcursor taps, respectively. By including both a precursor and a postcursor tap, this equalizer can mitigate both precursor and postcursor intersymbol interference [13].

Half-rate serial odd and even bit streams enter the equalizer on the left of Fig. 12. The latches and multiplexers are clocked with the PLL output clock. When the clock is high, odd bits are put on the output bus and when the clock is low, even bits are placed on the output bus. To accommodate this timing scheme, the even bits are clocked out of phase compared to the odd bits.

HIPSTER was implemented in 180 nm CMOS technology and fabricated at a commercial foundry. A photograph of the 24-channel prototype is shown in Fig. 13 [5]. The die measures 11.9 mm by 5.4 mm for a total area of 64.26 mm^2. The logic and Gb transmitter operate on a 1.8 V supply and the front-end analog and mixed-signal circuits operate on a 3.3 V supply to maximize dynamic range. The chip is packaged in a custom 480-ball BGA to minimize required PCB area.

To isolate the sensitive analog circuits from digital interference, the digital backend was placed into a deep n-well. In addition, the analog and high-speed transmitter sections were surrounded by both n- and p-type guard rings. Key signal lines and ADC capacitors were shielded by ground planes to reduce noise pickup.

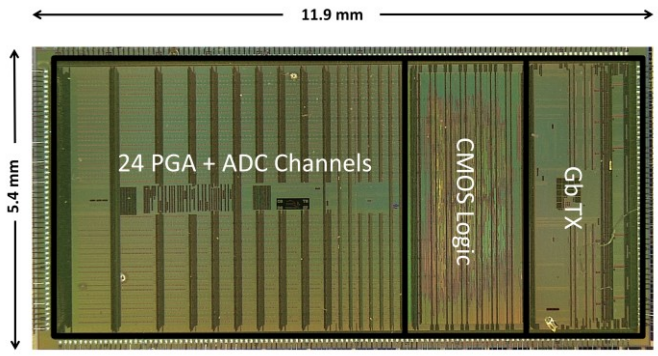

Fig. 13. HIPSTER die photograph.

III. Measured Results

For the analog and mixed-signal portions of the chip, the key performance measures are noise, differential linearity, and crosstalk. The measured noise in ADC codes for a typical channel (PGA + ADC) in nominal conditions with all 24 channels active is shown in Fig. 14. The front-end was configured with its nominal gain of 8.0. The noise measurement was made by connecting a heavily filtered DC voltage to the HIPSTER and recording the ADC output codes. The input-referred noise is then the rms voltage calculated from the samples divided by the gain before the ADC [14]. As HIPSTER was fully functional on first-silicon, all measured data was acquired using an active data lane using the JESD204B protocol.

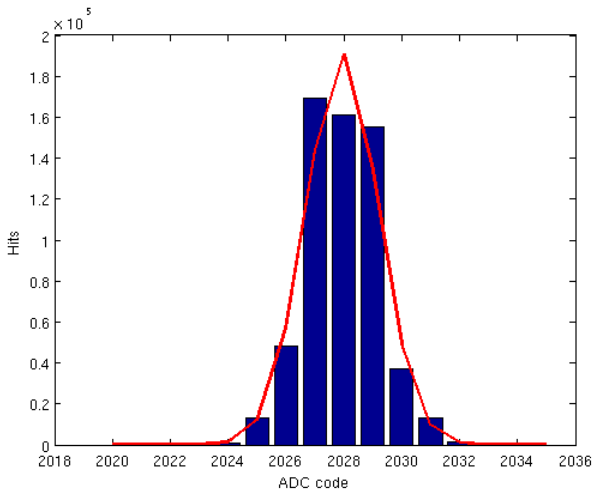

Fig. 14. HIPSTER channel measured noise.

The rms value of this measurement is approximately 1.25 LSB which corresponds to 114.5 µV-rms when referred to the channel input. The rms noise of the ADC alone is 0.9 LSB (or 660 µV-rms because the ADC input range is 3 Vpp-diff). Assuming the noise of the front end is not correlated with the ADC noise, this means the noise of the front end alone is 80 µV-rms, which is comparable to the ADC noise (when referred to the input). We observed a spread in ADC noise across channels of approximately 5%.

The differential linearity of a typical full channel (PGA + ADC) is shown in Fig 15. The peak differential nonlinearity is 0.55 / -0.43 LSB which is comparable to the linearity of the ADC alone (0.54 LSB) [5]. This result indicates that the overall linearity of the channel is limited by the DNL of the ADC. We found the peak DNL varied by about 0.25 LSB across channels, but no missing codes were observed (after calibration).

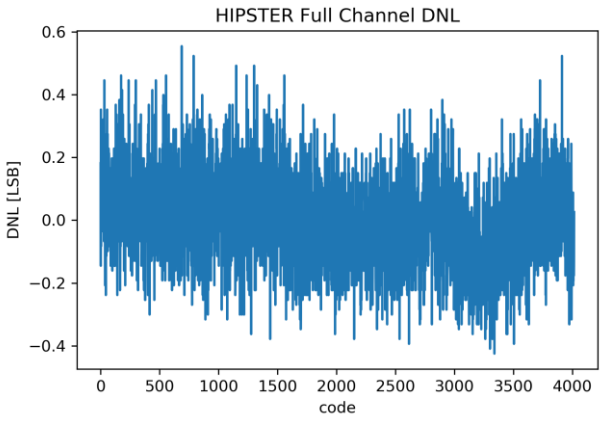

Fig. 15. Differential Nonlinearity of HIPSTER channel (including both the PGA and ADC).

Measurements were made both of high and low frequency crosstalk. To measure low-frequency crosstalk a high-amplitude sinewave was input to one channel and the digital codes of the adjacent channels were observed. The measured crosstalk was approximately -65 dB. There was no significant difference between the full channel and the measurements of the ADC alone, indicating the crosstalk is dominated by crosstalk between the ADC channels [5].

To measure the high-frequency crosstalk, a 1 V step was applied to the front end and the ADC codes of adjacent channels were monitored. Again, the measured crosstalk of approximately -45 dB was only slightly worse than for the ADC alone, indicating again that the ADC dominates crosstalk performance. Because the ADC consumes the most power in the channel by far, it is likely the crosstalk is due to coupling through the power rails as the ADC channels are well isolated in the physical layout.

HIPSTER uses a ring oscillator to implement the VCO in order to maintain flexibility when interfacing various sensors. A plot of the VCO output as a function of applied control voltage is shown in Fig. 16. The result shows it is possible to tune the VCO from 0 to approximately 3 GHz which gives plenty of margin for the target nominal frequency of 1.5 GHz (to support a data rate of 3 Gbps). The gain of the VCO, K_{VCO}, is approximately 3 GHz/V over its useful range.

An oscilloscope photograph of the digital output of HIPSTER is shown in Fig. 17. In this measurement, low impedance probes were soldered directly to the test PCB to minimize the impact of the measurement apparatus on the performance of the ASIC.

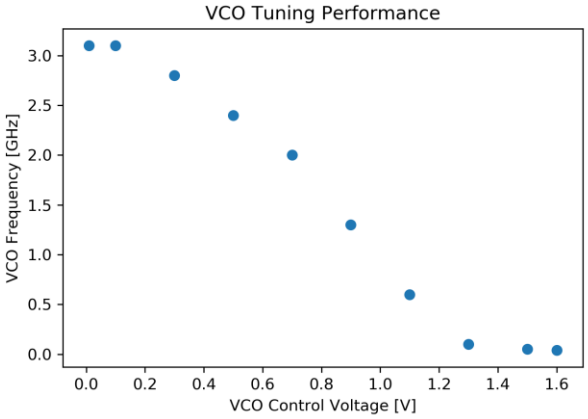

Fig. 16. Measured VCO tuning range.

The top trace is the 50 MHz reference clock (the ringing is due to the scope probe). The second trace is the differential 1.5 GHz transmit clock and the bottom trace is the digital output of the chip (the chip is transmitting a repeating pseudo-random pattern). It is unclear if the wandering common-mode level of the transmit clock is due to the clock itself or the on-chip buffer amplifier because the common-mode level of the data itself appears more stable.

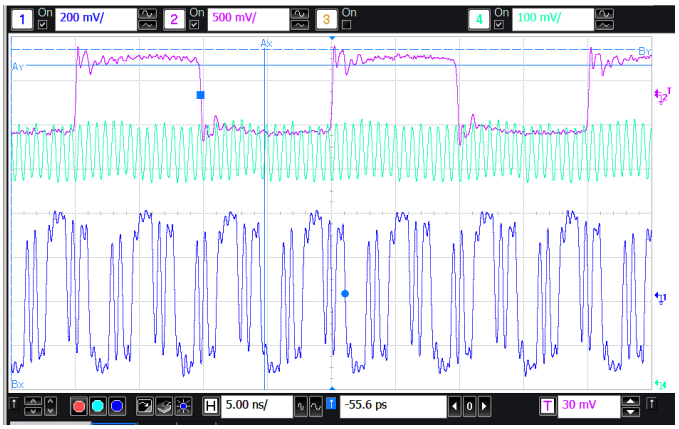

Fig. 17. Measured HIPSTER high-speed digital output at 3 Gbps.

An eye diagram measured after a PCB trace approximating the trace that HIPSTER would be expected to drive in a practical system is shown in Fig. 18. In this test the serializer was configured to operate at 4.5 Gbps to explore the limitations of the chip. The transmit equalizer was adjusted here to maximize the opening of the eye. The top trace is the data (with oscilloscope persistence applied to build up the eye) and the bottom trace is the transmit clock (through a buffer). There is a clear odd/even dependence in the width of the eye opening that made it difficult for the receiver to lock onto the transmit channel. We were able to reproduce the odd/even dependence in simulation and have determined the error is unequal on-chip trace lengths in the odd and even datapaths.

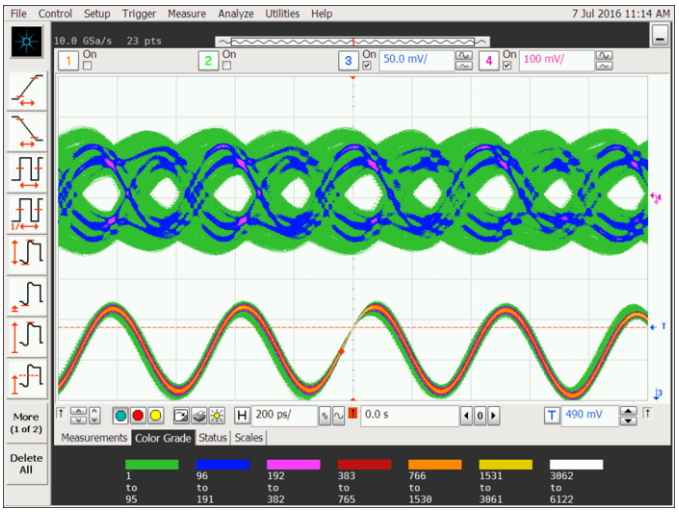

Fig. 18. Eye Diagram for 4.5 Gbps operation.

The communication between HIPSTER and an FPGA containing a commercial JESD204B RX module was tested. The physical distance between HIPSTER and the FPGA was similar to the distance expected in a practical camera implementation. HIPSTER was able to establish a link and transmitted a full day of pseudo-random data at 3 Gbps over several cm of FR-4 without a bit-error, giving an upper bound of the Bit-Error Rate (BER) of approximately 10^{-14}.

In nominal conditions, HIPSTER dissipates approximately 2.35 W (or 98 mW / channel). Of this, about 1.68 W is dissipated in the ADC array (or 70 mW / ADC), 350 mW is dissipated in the PLL, clock distribution network, and serial transmitter, and 320 mW (or 13.3 mW / channel) is dissipated in the PGAs. This power dissipation depends heavily on the use case, however. Especially in the TX block, the power consumed depends on whether equalization is used, the speed of the data transmission, and what bias currents are needed in the CML logic to drive the expected load.

Measured results of HIPSTER are summarized in Table 1.

TABLE I. MEASURED RESULTS

HIPSTER Summary: 3.3 V, 1.8 V and 25° C		
	Value	Units
Number of Channels	24	-
Sampling Rate	25	MHz
ADC Resolution	12	bits
Output Data Rate	3	Gbps
Input-Referred RMS Noise	114.5	µV
Adjacent Channel Crosstalk (response to an input step)	< -45	dB
Differential Linearity	0.55 / -0.43	LSB
Power Dissipation (total)	2.35	W
CMOS Technology	180	nm
Die Area	64.26	mm^2

IV. CONCLUSION

A 24-channel front end and ADC array for readout of charged-particle CMOS image sensors is presented. The ASIC achieves sustained communications at 3 Gbps with a BER of better than 10^{-14}. The 24 independent 12-bit ADCs operate at 25 MSPS with good differential linearity and noise. HIPSTER demonstrates that high-speed CMOS image sensors with analog outputs can be read out with high levels of integration and a low per-channel power dissipation of 98 mW per channel. The measured input-referred noise when the front end is configured in its nominal condition is 114.5 µV-rms. The high level of integration and low power dissipation of HIPSTER enables the implementation of compact, lower-cost high-speed charged-particle imaging systems.

REFERENCES

[1] Y. Char, J. Cheon, S. Lim, M. Kwon, K. Yoo, W. Jung, D.-H. Lee, S. Ham, and G. Han, "A 2.1 MPixel 120 Frame/s CMOS Image Sensor with Column-Parallel ΣΔ ADC Architecture", *IEEE J. Solid-State Circuits*, vol. 46, no. 1, pp. 236–247, January 2011.

[2] M. El-Desouki, M.J. Deen, Q. Fang, L. Liu, F. Tse, and D. Armstrong, "CMOS Image Sensors for High Speed Applications," *Sensors*, vol. 9, no. 1, pp. 430-444, January 2009.

[3] Denes, P. et al., "Active Pixel Sensors for Electron Microscopy," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip*., vol. 579, pp. 891-894, May 2005.

[4] M.H. Hayes, *Statistical Digital Signal Processing and Modeling*, New York: John Wiley & Sons, 1996

[5] C.R. Grace. E. Fong, D. Gnani, T. Stezelberger, H. von der Lippe, P. Denes, "A Modular Architecture for the Semi-Automatic Design and Layout of Pipelined ADC Arrays," *IEEE Nuclear Science Symposium Conference Record*, November 2017.

[6] A.N Karanicolas, H.S. Lee, and K.L. Bacrania, "A 15-b 1-Msample/s digitally self-calibrated ADC," *IEEE J. Solid-State Circuits*, vol. 28, no. 12, pp. 1207–1215, December 1993.

[7] T.H. Lee, *The Design of Radio Frequency Integrated Circuits*, New York: Cambridge University Press, 2003

[8] J. Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques," *IEEE J. Solid-State Circuits*, vol. 31, no. 11, pp. 1723-1732, November 1996.

[9] R.J. Baker, *CMOS Circuit Design, Layout, and Simulation*, New York: Wiley-IEEE Press, 2010

[10] Analog Devices, Inc. "Slay Your System Dragons with JESD204B", Technical Article MS-2503, 2013

[11] T. Beukema, et al. "A 6.4 Gb/s CMOS SerDes Core with Feed-Forward and Decision-Feedback Equalization," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2633–2643, December 2005.

[12] J. Bulzacchelli, et al. "A 10-Gb/s 5-Tap DFE/4-Tap FFE Transciver in 90-nm CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2885–2900, December 2006.

[13] J.W.M. Bergmans, *Digital Baseband Tranmission and Recording*, Dordrecht: Kluwer Academic Publishers, 1996

[14] M. Burns and G.W. Roberts, *An Introduction to Mixed-Signal IC Test and Measurement*, New York: Oxford University Press, 2001