UNIVERSITY OF CALIFORNIA, SAN DIEGO

Zinc Oxide Thin Film Transistor Pressure Sensors

A Dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Applied Physics)

by

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Professor Jie Xiang

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The Dissertation of Siarhei Vishniakou is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

University of California, San Diego

2016

DEDICATION

To my grandfather, Грищенко Михаил Филлипович.

EPIGRAPH

Excellence is the result of caring more than others think is wise,

risking more than others think is safe,

dreaming more than others think is practical,

and expecting more than others think is possible.

—Winston Churchill

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Chapter 3, in full, is a reprint of the material as it appears in Scientific Reports, 3 (2013). Siarhei Vishniakou, Brian W. Lewis, Xiaofan Niu, Alireza Kargar, Ke Sun, Michael Kalajian, Namseok Park, Muchuan Yang, Yi Jing, Paul Brochu, Zhelin Sun, Chun Li, Truong Nguyen, Qibing Pei, and Deli Wang. Tactile feedback display with spatial and temporal resolutions, Nature Publishing Group (2013). The dissertation author was the primary investigator and author of this paper.

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ABSTRACT OF THE DISSERTATION

Zinc Oxide Thin Film Transistor Pressure Sensors

by

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Doctor of Philosophy in Electrical Engineering (Applied Physics)

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Professor Shadi Dayeh, Chair

We have developed zinc oxide thin film transistors with a unique device architecture that exhibit robust and high-performance pressure sensing while maintaining transparency for next generation pressure-sensitive touchscreen displays. We systematically studied and optimized the material growth and device fabrication for improved device performance. We then fabricated top and bottom gate TFTs using both top and bottom contact geometries and identified the optimal device architecture to attain high pressure sensitivity while maintaining excellent transistor performance. Simultaneous operation of a single device as a switch and a pressure sensor allows

simple integration of sensors into arrays without the addition of external switching elements. The all-solid-state sensors are capable of measuring steady-state pressure and transient pressure variations. The sensing mechanism stems from the piezoelectric characteristics of RF sputtered ZnO. When zinc oxide is used as the channel material in thin film transistors, its piezoelectric property results in a shift of the transistor threshold voltage upon pressure application. This shift causes a modulation of the drain current flowing through the transistor at a steady bias. A linear dependence of the current change with the applied pressure is observed. Our first-generation TFTs together with a readout circuit built on a breadboard allow discrete pressure measurements from a single sensor at a frequency of 2 kHz. We demonstrated the operation of a transparent 8x8 pressure sensor array fabricated on glass, and the integrated system of pressure sensors and actuators for the recording and reproduction of touch. We further advanced our pressure sensors by studying the effects of sputtering gas, substrate temperature, and seeding layer on the ZnO film properties. The second-generation devices achieved an on-off ratio of 10^5 and allowed us to successfully demonstrate a larger, 16x16 array. We designed a complete system for real-time pressure signal acquisition and display, including read-out electronics, mechanical integration, electrical connections, and display software for signal visualization. We measured the latency of the pressure sensors to be less than 1 ms and the recovery time to be less than 20 ms. The new pressure-sensing technology enables the development of force-sensitive touchscreens that will make possible new mobile applications with a richer user-machine interface.

Chapter 1

Introduction

1.1 Summary

Since the rise of popularity of smartphones in early 2000s, touchscreens have become the de-facto user-machine interface standard for portable electronics. When smartphones with capacitive touchscreens became popular, a new standard for user interfaces was created, keyboards were removed from most phone designs, and gestures such as swiping became popular. Most modern touchscreen devices use a capacitive technology, where a charge present on a finger causes a change in the capacitance value measured by transparent conductive electrodes positioned on top of the display. Capacitive touchscreens are capable of accurately mapping the spatial locations of applied pressures, but not the magnitude of applied pressures. Therefore, they cannot distinguish between a light and a hard press. The lack of this additional dimension of pressure means that some mobile apps are not currently possible - force scrolling, 3D space navigation, realistic DJing, and gaming. The incorporation of pressure sensitive materials into flexible displays can lead to functionality that adds another dimension

to the machine-user interaction. Furthermore, the integration of such elements on flexible and transparent thin polymer layers has an enabling potential to realize smart and interactive displays at unprecedented resolution and functionalities.

The primary interest of our work lies in the transparent piezoelectric semiconductors, and, specifically, in zinc oxide. In the 1960s, piezoelectric semiconductors were evaluated for transducer applications, due to their ability of having a wide range of resistivity. ZnO was shown to be among the most promising materials from the group that includes cadmium sulfide (CdS), cadmium selenide (CdSe), gallium arsenide (GaAs), and ZnO [Hic05]. The focus of this research is zinc oxide thin film. Zinc oxide thin films can be deposited using a variety of methods, including sputtering [VLN$^+$13], pulsed laser deposition (PLD) [BZD$^+$13] [BLN08], atomic layer deposition (ALD) [MZJ10], sol-gel spin coating [PSS$^+$13], and others.

We report a novel zinc oxide (ZnO) device that acts as a transistor and a pressure sensor simultaneously [NWKH13], thereby allowing seamless integration onto displays without the need to place additional addressing electronics or individual electrode connections. ZnO film, 60-150 nm thick, is deposited using RF sputtering, and serves as the channel material in a TFT. ALD-deposited aluminum oxide (Al_2O_3) serves as the passivation layer and the gate dielectric. We have investigated a variety of materials, including metals and transparent conductive oxides, for making the source and drain contacts to the devices. We have also tested several substrates, including SiO_2 on Si wafers, standard microscope glass slides, and fused silica glass wafers. Using a pulsed measurement technique, we were able to obtain a stable current measurement as a function of time. Pressure applied on top of the TFT causes an increase in the drain current. The current increase is present as long as the

pressure is applied, and it is linearly proportional to the applied pressure. The device latency is less than 1 ms and recovery time is less than 20 ms. Upon application of pressure on top of the ZnO TFT, generated piezoelectric charges at the surface of the TFT create additional conducting channels that either enhance or decrease the gate voltage depending on the direction of the applied pressure and the film polarity. The piezoelectric charge density shifts the threshold voltage and contributes to the drain current, allowing well defined gradual changes with incremental pressure increase. The demonstrated pressure sensor can be easily integrated into an array without the need to place an additional switching element next to every pixel. The readout circuit can be completely eliminated from the screen and, using a circuit built on a breadboard, we are able to achieve a resolution of a few kPa, which is on par with a gentle touch. We will report the optimization of composition and thickness of the dielectric layers and the device functionality on a flexible substrate which we believe could become a competitive alternative to replacing the existing touchscreen pressure sensor technology.

1.2 Thesis structure

This dissertation is organized as follows. First, an overview of the touchscreens, pressure sensitive touchscreens, and pressure sensing technologies is provided. The remainder of the dissertation focuses on the zinc oxide thin film transistor pressure sensors (ZnO TFT-PS). The principle of operation of the ZnO TFT is provided. The fabrication and measurement techniques are then separately outlined in the following chapter, in order to provide sufficient background and allow for a continuous flow of the subsequent information. Next, the initial work on the bottom-gate ZnO:N_2 TFTs

is presented. This work is followed by a description of the optimization experiments that we have performed in order to improve the device performance. The second generation of the ZnO:O_2 TFT pressure sensors with top and bottom gate is then described. The discussion of the future work summarizes this dissertation.

1.3 Touchscreens today

We encounter touchscreens on a daily basis, whether its through smartphones, tablets, or even checkout kiosks at the grocery stores. These touchscreens provide an intuitive interface to these devices by allowing the user to press directly on the display. While these touchscreens are sensitive to touch, they cannot detect how hard the user is pressing. The capacitive technology used in those devices can detect the location of press, but not the amount of force. Therefore, there is currently a third dimension of force missing from the user interface. This problem is being extensively pursued by groups in public and private institutions on a global scale. Pressure sensing would be an important new feature for new touchscreens and better user interface. Beyond touchscreens, high density pressure sensors would also have significant impact for the work of neurosurgeons, where they could pave the road for tactile feedback-enabled remote operations. In the following subsections, various potential applications of pressure-sensitive touchscreens are reviewed.

1.3.1 Music software/hardware

There are specialized audio keyboard apps for tablets that are of interest to DJs. A touchscren or touchpad with a low latency and force sensitivity can enable action-based keys to emulate real-world analog instruments, such as a piano. There are

currently some products already providing so-called "velocity pads" - non-transparent square buttons - in the DJ mixing and sound production equipment. Music device manufacturers have employed various non-transparent technologies in their products to achieve these effects. Some of the approaches include Hall effect transducers, piezoresistive force sensors, and capacitive force sensors. However, these technologies can still be improved by reducing the sensor cost, increasing the sensitivity and sensor density, and making the devices transparent.

1.3.2 Computer-aided design (CAD)

When working with 3D space on a screen, navigation through space is difficult. The typical gestures like tap and swipe do not provide enough complexity to perform the operations of panning, zooming, and rotating a 3D space. With pressure-enabled touch, it is possible to create new gestures to enable such applications. For example, one could press hard with one finger to create an anchor, and use the other finger to rotate through the space. Another problem is selection of a particular piece or block in a multi-part object. As an example, consider a large cube that consists of multiple small cubes. To select one of the innermost constituents, it could be possible to press harder on the screen until the selection reaches the desired element. With visual feedback, humans should be capable of controlling multiple levels of force. In our preliminary lab tests, we reliably achieved at least three distinct pressure levels by pressing on the sensor with a stylus, without any visual feedback provided.

1.3.3 Educational software

Educational apps for children can help develop better writing habits. When first learning to write, a child might hold the pen in an inconvenient way, which could result in bad penmanship. Capturing the pressure applied at each point while writing can provide a feedback to the child, and instruct him or her to apply pressure differently, improving the hand-writing habits.

1.3.4 Gaming

Gaming is a large component of the mobile app industry, with multiple new games coming out regularly, both by hobbyists and major corporations. New controls on the smartphone will allow advanced games. One example is car racing. Using force touch technology, it is possible to use two fingers constantly maintaining contact with the bottom of the screen to control the game. The corners of the screen could be programmed to serve as acceleration and deceleration buttons, or they can be used for turning the wheel. Another alternative is to press hard with both fingers for speed up and slow down, and press hard with one and light with another to turn.

1.3.5 Secure signature capture

The concept of secure signature capture has been described at least as early as 2009 [XYL09]. The idea is to record the pressure applied by the user when the signature is being written, in addition to the shape of the signature itself. It might be possible to fake the shape of the signature itself, but it is more difficult to forge the signing pressure along with the signature. This could provide an additional layer for security.

1.3.6 User interface

User interface has already been expanded past a standard touch by the Android and iOS interfaces. Objects can currently be moved by pressing them and holding until the edit mode is enabled. Next, the object can be dragged and the user can exit the edit mode by clicking to the side of the active area. With force touch, a regular tap can be used to activate the object, while a force touch can be used to enter the edit mode. Next, the object can be dragged to the new location. Finally, with pressure-sensitive touch, two interaction methods are now possible. One outcome is to cancel the move to the new location by simply releasing the finger. This action will make the object being dragged to snap back to original position. To fix the object at the new position, the action of pinning is introduced. The new position of an object being dragged can be made permanent by pinning the object at the new location. The action of pinning consists of making permanent contact with the screen, the pressing harder with the finger at a certain location, in a pulse-like action.

1.4 Capacitive touchscreens

When touchscreen technology first started to become popular, two major sensing technologies emerged - capacitive and resistive[BB10]. Resistive touch was the most popular at first. However, due to inferior sensitivity and shorter lifespan, as well as limited support for multitouch, capacitive touchscreens have become the de-facto standard for touch-enabled displays.

Capacitive touchscreens are the most common type of touchscreens used at the time of writing of this thesis. A projected capacitive touchscreen consists of a

layer of electrodes, an insulating layer, and another layer of electrodes perpendicular to the first layer. The structure is shown in Figure 1.1. The electrodes are composed of transparent conductor (typically, indium tin oxide) and are deposited by sputtering. They can be patterned by either screen printing, photolithography, or laser etching. A typical touchscreen is connected in an array fashion, and operates as follows: first, a column is selected. First row is selected and the capacitance is measured between the row electrode and the column electrode. Next, another row is selected, and the capacitance is measured again, now in a new location. After all rows are scanned, the column is switched, and the scan is repeated [BO10]. This provides point-by-point information about touch location, a property that enables multi-touch. Due to each cross-point of the electrodes is physically fixed on the display, there is no coordinate drift, and the location of each touch can be precisely determined. Typically, the data from each location is interpolated to get a more accurate touch position.

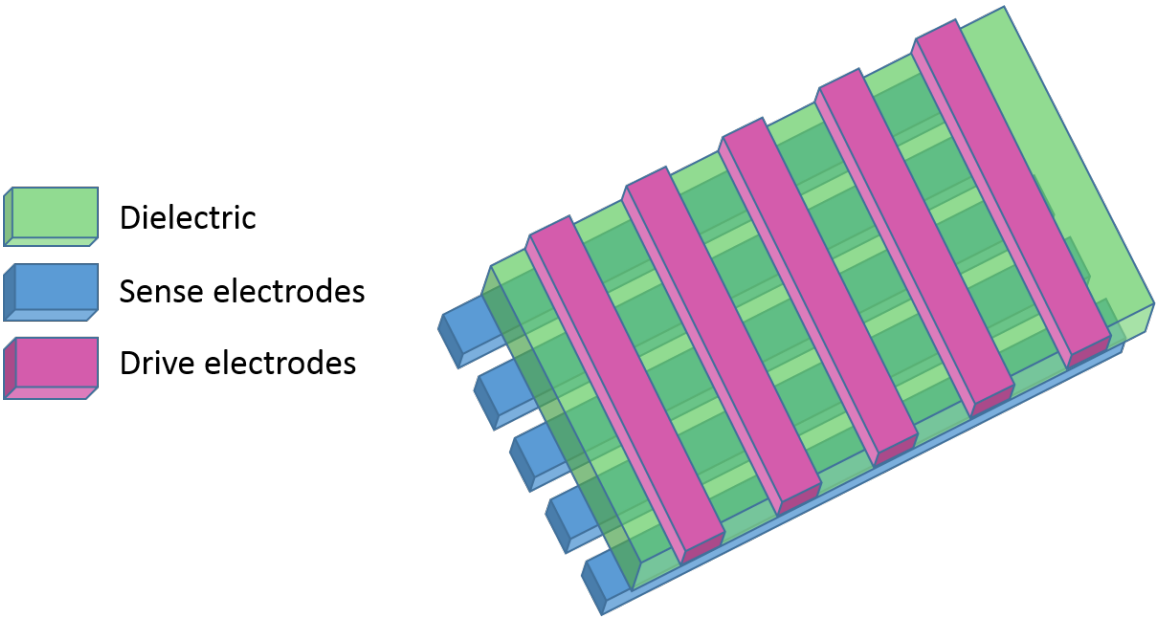


Figure 1.1: Structure of a projected capacitive touchscreen. Two layers of electrodes are arranged in a row and column fashion, and separated by an insulating layer.

1.5 Pressure sensitive touchscreens

A pressure sensitive touchscreen technology allows the detection of the location of touch as well as the amount of applied force. Ideally, the point-by-point pressure information is provided, in order to let the applications process such motions as simultaneous light press with one finger and hard press with another, or even the motion of rolling of a finger on the screen.

The strong market need for a pressure sensitive touchscreen technology is driven by two factors. First, the original equipment manufacturers (OEMs) are constantly seeking differentiation from the competition, and are eager to introduce new features into their phones and tablets. Second, the pressure-sensitive touch will expand the device functionality for users. For example, at a discussion with the Design lab at UCSD on March 10, 2015, students mentioned that one feature currently missing from their touch-enabled devices is the pen operation. They would like the ability to easily take hand-written notes on their devices, using any pen-like object. Pressure sensitive touchscreens can enable such functionality.

1.5.1 Force-enabled touchscreen smarthphones

As of late September, 2015, there are at least two force-enabled smartphones on the market, the Apple iPhone 6s and the Huawei Mate S, and more OEMs are rumored to be working on their own implementation of this functionality. Technology used by Apple is called 3D Touch. The force is measured by a matrix of capacitive pressure sensors located underneath the display. The location of touch is measured by a conventional capacitive touchscreen placed on top of the display. In this sensing method, the display is allowed to deflect due to press, and the force is measured by

the change of capacitance at the bottom sensors. In its present form, the addition of this new capability to the phone results in an increase of display assembly weight by more than double the original amount. This has caused the new iPhone model to be, for the first time, heavier than its predecessor.

The technology found in the Huawei Mate S smartphone appears to be capacitive as well. There is a scale function on the smartphone that allows the user to measure weight of objects, with certain limitations. The object must be conductive and have a weight between 100g and 400g. These requirements suggest that some kind of modified capacitive technology is being utilized.

1.5.2 Commercial pressure sensors

A number of startup companies aim to create a commercial pressure-sensitive capability for touchscreens and utilize a large variety of pressure sensing techniques. Technologies like infrared sources and detectors, MEMS strain sensors, piezoelectric sensors, quantum tunneling composite materials, surface acoustic waves, and many others have been attempted to realize pressure sensitivity.

NextInput Nextinput, founded in 2012, developed a MEMS pressure sensor technology that can be used on the corners of a display in order to either determine the location of a single touch, or, if used together with a capacitive touchscreen, to determine the location of touch and the magnitudes of pressures at each touch point. The resulting system can achieve sub-millimeter spatial resolution and sub-millinewton force resolution. The device fabrication is entirely Si-based, and includes the process of etching a mesa structure for receiving the applied stress and transferring it to piezoresistive sensors located on the backside [CD15]. Because the device is based on

a silicon process, it is not transparent, and therefore must be placed underneath the display. One advantage of this approach is that the display remains unobstructed by the added force sensitivity, and therefore, the added sensors do not degrade the image quality.

Cambridge Touch Technologies Another interesting approach is presented by the Cambridge Touch technologies, Inc. The company has been active since at least 2012, and seeks to utilize the capacitive touchscreens together with pressure sensors to achieve a "3-dimensional" touch experience [NLCC13]. The patent filed by Nathan et al and assigned to the company in 2013 describes a pressure sensing layer positioned on top of the display and between the driving and sensing electrodes for the capacitive touchscreen. The piezoelectric layer acts as a dielectric material, while still creating a voltage due to applied pressure. To address these pressure sensing elements, it appears that either individual connections to each pixel are necessary, or a switching TFT must be employed. The advantage of this pressure sensing method is the availability of very sensitive capacitive touchscreen to enable the device operation using very light touch. At the same time, the pressure sensing layer can provide the force information, and it can be argued that for some applications, the spatial resolution of force does not need to be very high. The main drawbacks include the manufacturing cost of using both a capacitive layer and the pressure sensing layer, as well as the lack of an intuitive array operation of the devices. The scaling of this approach is hindered by the requirement of individually routing each pixel. This pressure sensing approach does not scale well because sensors require individually routed connections. Doubling the number of elements would double the number of traces, which could be problematic due to space and the mechanical integration of these sensors into consumer electronics

devices.

Samsung Corporation Samsung Corporation has filed a patent in 2014 on the use of piezoresistive materials to create a pressure-sensitive touchscreen [LHCN14]. The piezoresistive material is patterned in a grid formation, with each sensor having a separate electrical connection. The resistance of each pad is measured by the touch controller, and the resulting value is used to determine the location of touch as well as the amount of force. Some of the possible piezoresistive materials cited in this application are graphene and carbon nanotubes.

1.6 State-of-the-art pressure sensors

Among pressure sensing techniques recently pursued by the researchers have been organic transistors with structured-PDMS gate dielectrics [MTS+10], zinc oxide nanowires (Section 1.6.1), pressure-variable resistors [All14], pressure-variable capacitors [LVT+11], and other approaches.

Rubrene-based OTFT Professor Zhenan Bao's group at Stanford University has been very active in the development of various pressure sensing technologies, mainly variations of the capacitive pressure sensing. One of the reports describes the development of highly sensitive pressure sensors using organic rubrene-based thin film transistors with structured PDMS gate dielectrics [MTS+10]. When pressure is applied, the distance between the gate electrode and the channel changes. Due to the micro-structuring of the PDMS layer, the change is more pronounced, and the recovery time of the layer is improved. When the effective gate dielectric thickness changes,

the drain current is altered. The change is proportional to the pressure applied. Due to the large dielectric thickness, the device operational voltage is 80V. The device relaxation times are on the order of milliseconds.

CNT film In 2011, Professor Zhenan Bao's group has reported on the development of transparent pressure sensors based carbon nanotube films [LVT+11]. The proposed technique is to modify the typical capacitive pressure sensing by replacing the conducting electrodes with carbon nanotubes, and changing the dielectric layer to an elastic layer that can deform with applied pressure. When pressure is applied, the deformation of the dielectric produces a change in the capacitance at the crossing points of the rows and columns of carbon nanotubes. The carbon nanotube material enables the stretchability and flexibility of the entire device. The pressure resolution achieved is 50 kPa, with the available measurement range of up to 1 MPa. Unfortunately, the recovery time was not reported due to the use of an LCR meter for the measurement of the capacitance.

Conductive traces Conductance-based pressure sensors were reported by Kaltenbrunner et al in 2013 [KSR+13]. A plurality of inter-digitated conductive traces are patterned on a substrate, and form a single sensor pad. When an object comes into contact with the pad, it creates conductive pathways between the traces, and therefore results in the change of resistance. When the contact area increases, more traces are shorted, and the resistance decreases. This works as a contact sensor, with some correlation to pressure, assuming that the contact is made with a conductive object. The work also features an impressive device fabrication. The devices are built on ultra-thin (about 1 μm) polyimide (PI) sheets. The gate dielectric is a mere 20 nm of

amorphous aluminum oxide, and the device is quite robust, and operates even after being crumpled.

1.6.1 Recent developments with zinc oxide pressure sensors

Many structures using ZnO have been used to record pressure by taking advantage of the ZnO piezoelectric property.

nZnO-pGaN heterostructures Professor Zhong Lin Wang's group at Georgia Tech has reported on various device geometries for zinc oxide pressure sensing, with the main focus placed on the nanowire structures. A hybrid nanowire heterostructure composed of n-type ZnO and p-type GaN is used to convert mechanical (pressure) energy directly into electromagnetic (light) energy [PDZ+13]. The term "piezo-phototronics" has been developed to describe the device operation [ZW12]. A thin film of p-GaN is grown on sapphire, and the n-type vertical ZnO nanowires are grown on top. The structure is filled with PMMA and a top contact ITO layer is deposited. When a bias voltage of 6-10V is applied to the structure, each nanowire emits light at the wavelength of about 420 nm upon stress. This pressure imaging method allows extremely high spatial resolution of less than 3 μm, with response time of about 90 ms. Commercialization of such technology is likely hindered by the need for a high-resolution CCD camera for image processing positioned underneath the device, as well as the requirement of using a sapphire substrate with MOCVD-grown GaN. The more recent report by this group describes a similar device structure with the p-GaN layer replaced by a p-polymer, PEDOT:PSS, which allows the fabrication of the sensor on a flexible substrate [BWD+15]. However, the semiconductive PEDOT:PSS is not transparent, which precludes its use in pressure-sensitive touchscreen applications.

Individually addressable ZnO nanowires Professor Zhong Lin Wang's group also reported on the use of individually-addressable zinc oxide nanowires for pressure sensors [WWW13]. They have used a novel two-terminal device architecture, with electrode connections for source and drain. The gate voltage comes solely from the piezoelectric effect. The typical device operation involves selecting a row and a column and reading out the resulting value of the current. The device showed excellent sensitivity of about 2 μA per 3.5 kPa, with a maximum pressure sensing range of up to 40 kPa. The rise time is about 150 ms.

ZnO nanowires with MgO layer Very recently, Liao et al [LYL+15] have demonstrated that ZnO nanowires can be used to detect a force of 3.5 gf (gf is the force created by a mass of 1 gram). The device structure consisted of vertical ZnO nanowires with top and bottom FTO contacts, with the modification that a thin layer of MgO is inserted in series with the top contact layer. A single pressure sensor was reported, with the response time of 128 ms.

1.7 Patent protection of the ZnO technology

A search on Google Patents for "ZnO TFT" excluding "IGZO" produces over 1000 results as of August, 2015. Main topics of the patents are methods of manufacturing of ZnO TFT, the transparency of the resulting devices, p-type ZnO and using ZnO TFT as the addressing elements for display applications. An etch-stop layer process using titanium metal has been claimed in [BL14], where a thin Ti metal layer is deposited on top of ZnO thin film. Afterwards, the Ti layer is patterned using conventional photolithography with some etching process. Finally, Ti layer is made

insulating by annealing in air or oxygen ambient at temperatures up to 200 °C. An interesting pressure sensing method using ZnO film is claimed in [JPN+14]. To create a sensor, piezoelectric crystals are embedded into the gate dielectric. Then, the drain current is monitored. With the proper driving conditions of the device, polarization value can be determined, and therefore the applied pressure is extracted.

1.8 Human pressure sensitivity

We use five senses to perceive the world: sight, hearing, touch, smell, and taste. Sight and hearing constitute 94 % of our cognitive perception [SKR11]. When it became possible to record and reproduce audio and visual information, the world was dramatically transformed. First, the ability to record and replay sound enabled radio and telephones, and provided fast information sharing between people over large distances. Later, the ability to record and replay images led to the emergence of movie theaters and enabled the commercialization of TV. These technologies are now utilized by most people on a regular basis. However, the senses of sight, smell, and taste so far have not been recorded and reproduced, and this shortcoming means that a complete virtual reality cannot yet be achieved. Some research advances have been made to record pressure/touch, temperature, smell (electronic nose) [WYN05], [FL95], [PSNG06], and taste [LBL+14]. On the other hand, the fake touch stimuli can already be provided to humans by sending electrical signals to the appropriate nerves [BDT+13]. This ability, together with a dense array of force sensors positioned on a prosthetic arm, could allow for the development of artificial appendages.

Force feedback systems Force recording and reproduction, specifically, can enable an entire set of new devices. For example, a glove with built-in force sensors and transducers can be used to learn how to play golf. First, the professional players' club holding habits can be recorded and analyzed. Next, a newcomer can wear a glove, and the glove can be used to provide feedback regarding the proper amount of pressure at each point. If the newcomer is not holding the glove properly, then the system will inform the user, so that adjustments can be made instantaneously. This idea can further be extended to enable actions like virtual handshakes for remote meetings.

Another example is remote surgery. If a doctor is not immediately available, he or she can perform a surgery virtually by manipulating the tools through a machine. The patient has to be situated in a room with the necessary equipment, but the doctor only needs access to a control station that is remote connected to the surgery equipment through a network. Force sensors will provide doctor with a sense of "feel" for the material that he or she is working with, in addition to the visual feedback that is already easily attainable. A high resolution and refresh rate array of force sensors and actuators on both the doctor's hand and on the remote machine and patient can help improve the ease of conducting remote surgical procedures.

This could also be useful during physical therapy, particularly massage. Flexible pressure sensor array could record the amount of force applied by the hands of the masseuse, and correlate the force with verbal feedback from the client. This data could be used to find the optimal force for best client response to be utilized for training of new practitioners, or to create client-based guidelines for substitute practitioners.

The sense of touch components Touch sensation itself consists of several parts, which are contact, pressure, pain, hot, and cold. In 1 square centimeter of skin, there

are about 100-200 pain receptors, 15 for pressure, 6 for cold, and 1 for warmth [Tou14]. On the palm, there are about 100-200 pressure spots per square centimeter [WC91].

A 1990 study published by Dellon et al [DMD92] lists the threshold of human pressure sensitivity at the level of 0.1 grams per mm^2. This pressure is equivalent to about 1 kPa:

$$\frac{\frac{1kg}{1000g} \times 0.1g \times 9.8\frac{m}{s^2}}{10^{-6}m^2} \approxeq \frac{10^{-3}N}{10^{-6}m^2} = 1kPa$$

A pressure of 1 kPa is equivalent to a weight of 10 gram pressing on an area of 1 square centimeter. This is consistent with the basic tests with weights that we have performed in our laboratory as a sanity check, where a weight of 10 g with an area smaller than 1 cm^2 was applied to the back of the hand and to the index finger, while the human subject verbally responded whether that object can be felt.

A study by Wheat et al.[Whe04] has revealed that a human index finger can perceive the difference between forces from 1 N to 5 N over at least five levels. Normal force was applied to the fingers of 8 different subjects using a custom-built apparatus, and the subjects were asked to assign a scale for the force, in comparing it to the reference force of 3 N. A linear relationship between the perceived force and the applied force has been observed for all of the experiment participants.

1.9 Conclusion

We discussed in this chapter several pressure sensitive technologies and how their potential to enable new applications in various sectors, such as health-care and human-machine interfaces. We anticipate that the technological advances resulting from this Ph.D. research work and reported in this dissertation will provide significant

performance and cost advantages for disruptive touchscreen applications. In the remainder of this dissertation, we will overview and discuss the fundamental physics and the interface technology that we set up to demonstrate a fully functional 16x16 pressure sensor array, with the highest spatiotemporal resolution to date.

Chapter 2

Theory of device operation

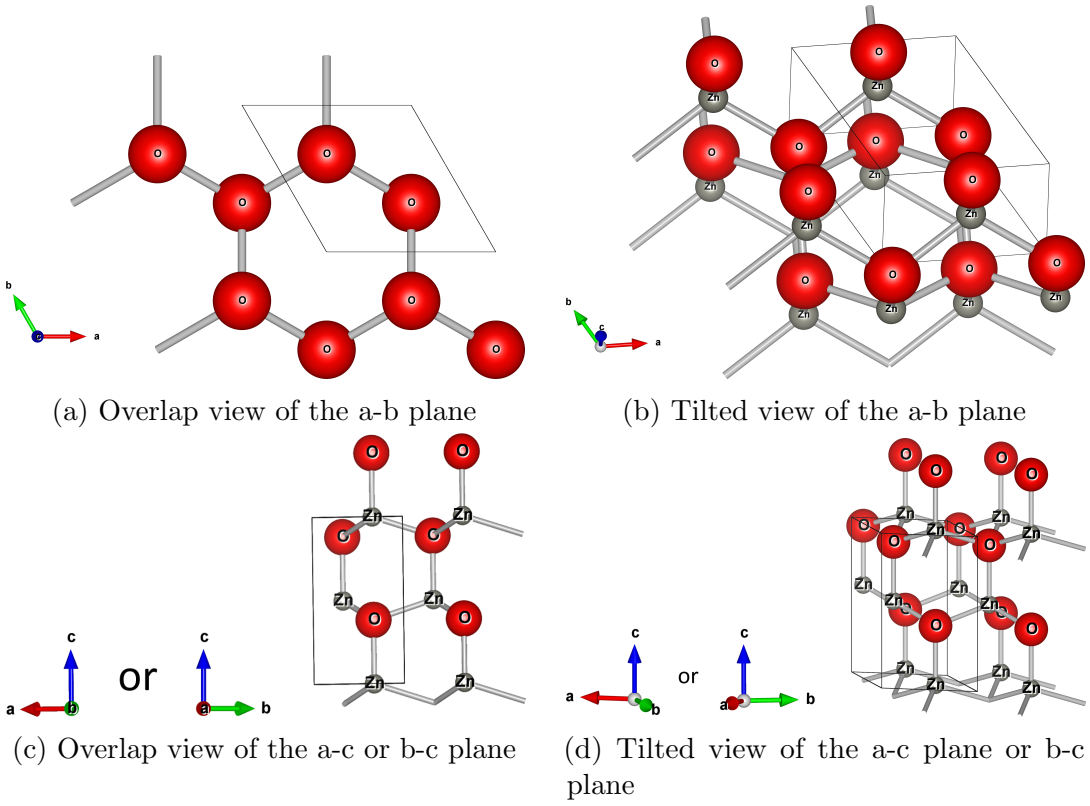
Our goal is to find or develop a pressure sensitive technology to address the current needs of the market. A successful pressure sensor must be transparent, be sensitive to even the lightest touch, have a small size and be able to get integrated into high-density arrays. Due to the high density requirement, the device also must be able to support a high speed operation. The standard approach to create a matrix of pressure sensors is to use a transducer, such as a piezoresistive or a piezoelectric element, together with a transistor, such as a thin-film transistor, in order to address the sensor element and prevent the cross-talk between neighboring elements and between pixels that are positioned on the same line. We devised a novel device architecture to achieve a pressure-sensing and a switching ability in a single pressure-sensitive thin-film transistor. Our primary invention is the use of an oriented transparent piezoelectric semiconducting material as the channel layer in a thin-film transistor. In the following sections the device operation is explained in detail. Our material of choice — zinc oxide — has all of the desired attributes: transparent, piezoelectric, semiconducting, cheap, and easily deposited. We start by discussing the fundamental

physical properties of zinc oxide.

2.1 ZnO crystal structure and piezoelectric effect

Zinc oxide is a piezoelectric semiconductor. It has a wide bandgap of 3.3 eV [JdW09], which means that ZnO does not absorb light in the visible spectrum and it is therefore transparent. ZnO exists in several crystal structures: wurtzite, zincblende, and rocksalt [MÖ08]. Under standard conditions (standard temperature and pressure), ZnO films are typically found in the wurtzite configuration. This work is centered around the wurtzite phase of ZnO crystals. This crystal consists of two interpenetrating hexagonal lattices of zinc and oxygen, displaced from each other along the c-axis by 3/8. As a result, the top view of the ZnO crystal only shows a single kind of atom, since the remaining atoms are positioned directly underneath them, as can be seen in Figure 2.1. In addition, each of the sublattices is arranged according to the hexagonal close-packed principle. The ZnO is a tetrahedrally bonded semiconductor, with each atom bonded to four neighboring atoms of the other kind. The lattice constant c is the distance between the neighboring Zn atoms in the c-axis direction (note, without accounting for the hexagonal close packing geometry), and the typical value is c = 5.2 Å [MÖ08]. The in-plane lattice constant a = 3.2 Å is the distance between the neighboring Zn atoms in the a-b plane.

ZnO is also piezoelectric, and has a relatively large piezoelectric constant compared to other materials. The bulk value of piezoelectric coefficient for ZnO is $d_{33} = 9.93\ \frac{pm}{V}$ [Wan04]. For comparison, GaN has a smaller d_{33} value of 3.1 $\frac{pm}{V}$, or $d_{33} = 2.38\ \frac{pm}{V}$ [LCSC00]. Another drawback of GaN is that it cannot be easily deposited to create a thin-film transistor. On the other hand, the d_{33} constant of PZT



(a) Overlap view of the a-b plane

(b) Tilted view of the a-b plane

(c) Overlap view of the a-c or b-c plane

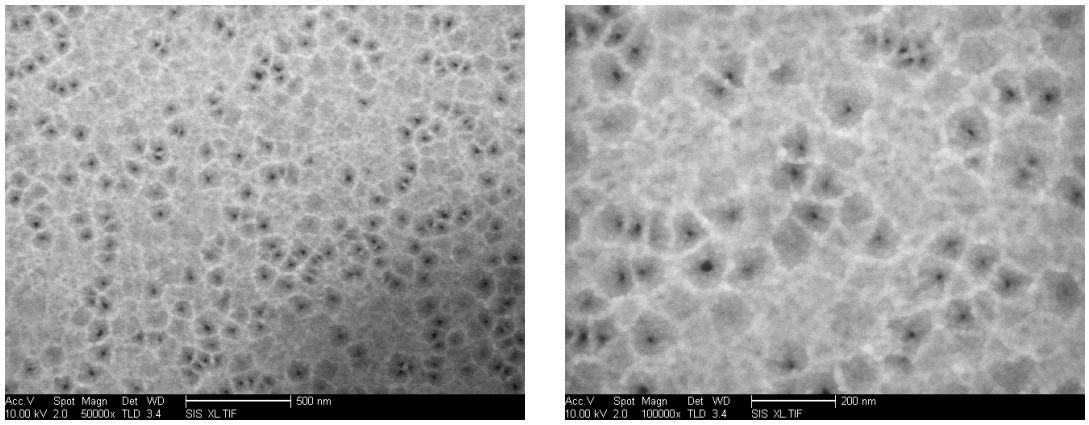
(d) Tilted view of the a-c plane or b-c plane

Figure 2.1: ZnO crystal structure - views of basis planes.

material varies based on the deposition method, but can range in value between $d_{33} = 180\ \frac{pm}{V}$ [PCR+02] to $374\ \frac{pm}{V}$ [GCS13], which is significantly larger than ZnO. However, the PZT material is not a semiconductor.

Bulk crystals of ZnO are typically grown by hydrothermal method, vapor/sublimation growth, and melt growth [ACZ+10]. In practice, it is virtually impossible to obtain large single crystal films of zinc oxide by sputtering. Instead, polycrystalline films are typically observed, with grains merging together during the film growth. This causes a smaller experimental piezoelectric constant of deposited ZnO film as compared to the literature values.

Sputtered ZnO thin film tends to have a preferential c-axis orientation, with the c-axis pointing perpendicular to the substrate. Figure 2.1 shows the crystal structure



(a) 50,000x magnification (b) 100,000x magnification

Figure 2.2: High-resolution SEM image of ZnO film grown at 600°C. Film typically grows with c-axis perpendicular to the substrate.

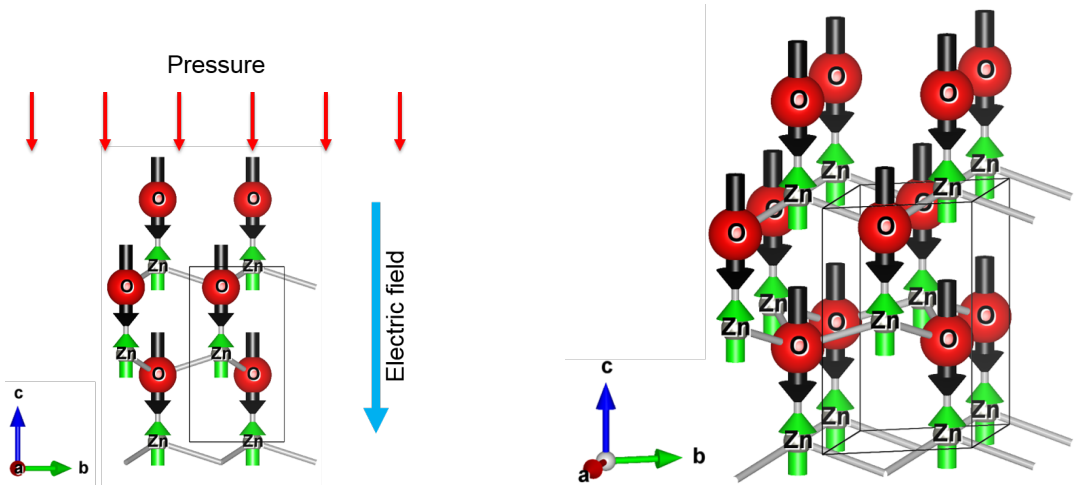
of the wurtzite zinc oxide from different viewing directions. The a-b plane is shown in Figure 2.1a. Because of the film orientation, this can be considered to be the "looking down" onto the substrate view. Although the ZnO film typically grows with c-axis perpendicular to the substrate, it does not have inherent x-y orientation, due to the substrate rotation in the sputtering chamber. The views of the a-b and b-c planes shown in Figure 2.1c can be considered a cross-section, or a side view, of a certain grain inside the ZnO film. The direct views of the crystal planes in Figures 2.1a and 2.1c show multiple atoms overlapping. However, the entire crystal structure cannot be seen from this angle. The slightly tilted views in Figures 2.1d and 2.1b illustrate the stacking of the zinc and oxygen atoms ZnO crystal structure. In the wurtzite lattice, the a-b and b-c planes are identical, so only one image is shown here, with the two possible axis positions highlighted. Interestingly, the hexagonal crystal symmetry is preserved at microscale, as can be seen on a high-resolution SEM image in Figure 2.2 of a very thin ZnO film grown at high temperature.

Due to the lack of crystal symmetry in a wurtzite structure, a spontaneous

polarization is always present in a zinc oxide thin film. When film is stressed, or, alternatively, when pressure is applied on top of the film, an additional piezoelectric polarization field is created inside the crystal.

When the pressure is applied, the lattice constants a and c change their values, and therefore the crystal lattice is deformed [WJ07]. In addition, the two zinc and oxygen sublattices shift with respect to each other. This distorts the net dipole moment in the c-direction, resulting in an electric field in response to pressure [CPRB94]. Figure 2.3 shows a side view of ZnO crystal, just like in previous sketches in Figure 2.1c. The c-axis is pointing vertically. When pressure is applied, the lattice of the ZnO changes. Both of the lattice parameters, a and c, change, and also the Zn- and O- sublattices shift. To simplify the discussion, we can suppose that the oxygen atoms shift down and the zinc atoms shift up, as shown in Figure 2.3. In the side view, the atoms in the lattice overlap. However, this effect happens in the entire plane, as shown in the slightly tilted view in Figure 2.3b. The net effect is the change of the ionic bond length, which gives rise to a non-zero dipole moment, resulting in an electric field in response to pressure.

Grain orientation The discussion above highlights the importance of the crystal alignment inside the film and its effect on film properties. As mentioned earlier, the ZnO film is polycrystalline, and consists of many grains of nearly-crystalline zinc oxide. However, not all crystals will be perfectly aligned in the vertical direction, and some of the grains might be slightly tilted relative to others. This can be learned from the rocking curve measurement of x-ray diffraction. To perform a rocking measurement, a regular theta - two theta scan is first performed to identify the position of the diffraction peak of interest. Once the peak is identified, the position of the two theta



(a) Overlap side view (b) Angled side view

Figure 2.3: A simplified picture of the crystal response due to pressure. The resulting action can be visualized as a relative shift of Zn and O atoms toward each other.

is fixed at the location of the maximum intensity for the peak. Next, the stage is "rocked", or tilted with respect to the fixed beam and detector, and the intensity is read. It is expected that for well-oriented films, the resulting graph will have a very narrow peak at the zero rocking angle, and will drop off sharply to either side of the peak. If the resulting peak is broad, then there are multiple grains that are slightly misoriented with respect to the vector perpendicular to the substrate.

2.2 Piezoelectricity of ZnO and relevant equations

The relationships between piezoelectric constants, charges, and electric fields are explained in detail by Moheimani et al in [MF06]. When a piezoelectric film is used as a sensor, strain is applied externally to the device, and electric field is created inside the film as a result. The electric field causes a buildup of charges on either side. The equation for electromechanical action in linear piezoelectric materials can

be written as:

$$D_m = d_{mi}\sigma_i + \epsilon^{\sigma}_{ik}E_k \tag{2.1}$$

Here,

$\vec{E}$ is the applied electric field (zero in this case),

d is the piezoelectric strain matrix, with the units of $\frac{m}{V}$

σ is the stress tensor, with units of Pa

ϵ is the permittivity measured at constant stress, in $\frac{F}{m}$

$\vec{D}$ is the electric displacement, with units of $\left[\frac{C}{m^2}\right]$

Without externally applied electric field, the equation can be rewritten in scalar form for force applied in the z direction only:

$$D_3 = \sigma_3 d_{33} \tag{2.2}$$

Next, we can substitute $D = \epsilon E_{piezo}$ [Gri99], where E_{piezo} is the electric field developed inside the material due to the applied pressure, to get:

$$d_{33} = \frac{\epsilon E_{piezo}}{\sigma_3} \tag{2.3}$$

It is important to distinguish E_{piezo} from E in equation 2.1. E_{piezo} is the electric field that appears in response to pressure, and E is the externally applied electric field. The units for d_{33} are $\frac{m}{V}$:

$$[d_{33}] = \frac{\frac{F}{m}V}{\frac{N}{m^2}m} = \frac{FV}{N} = \frac{C}{N} = \frac{m}{V} \tag{2.4}$$

To calculate the piezoelectric strain constant for ZnO, it is necessary to know the electric field that is developed inside due to pressure, as well as the permittivity of the ZnO film. For our application, σ_3 is the vertical pressure (force per unit area) applied on top of the device.

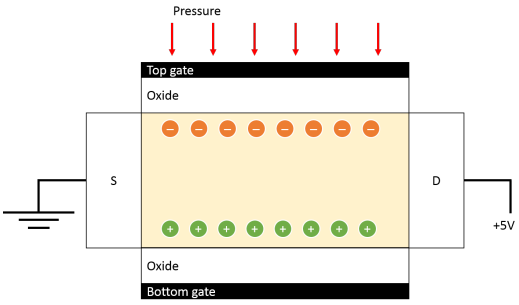
The relative dielectric constant of reactively sputtered ZnO has been determined by Cheng et al [CDZ+09] to be around 13.4. The classic semiconductor text by Sze [SN06] only provides this value for the rocksalt phase of the ZnO crystal, which is listed as 9.0. In the "Properties of Materials" book by Newnham[New04], the d_{33} value for wurtzite ZnO is listed as 12.4 $\frac{pC}{N}$.

2.3 Pressure sensing device operation

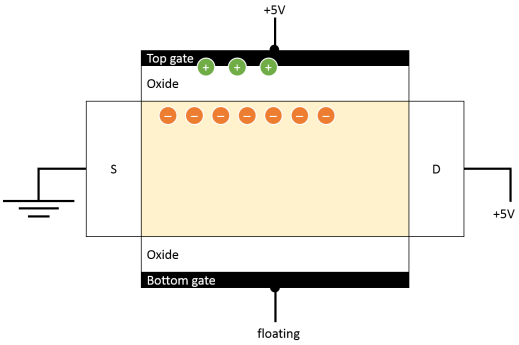
We developed transparent thin film transistor pressure sensors based on ZnO TFT with a piezoelectric channel.

A simplified device schematic is shown in Figure 2.4. The zinc oxide material forms the channel of a thin-film transistor. Suppose ZnO is grown in such a way that the bottom surface is oxygen-terminated, and the c-axis is pointing up. When pressure is applied, positive charges are developed in the bottom of the channel and negative charges are found at the top of the channel, due to the piezoelectric action and the resulting vertical electric field that is created inside the ZnO channel (Figure 2.4a). On the other hand, when positive voltage is applied to the top gate electrode, then this potential causes positive charges to appear at the gate electrode, and negative charges to appear at the top of the semiconductor channel (Figure 2.4b).

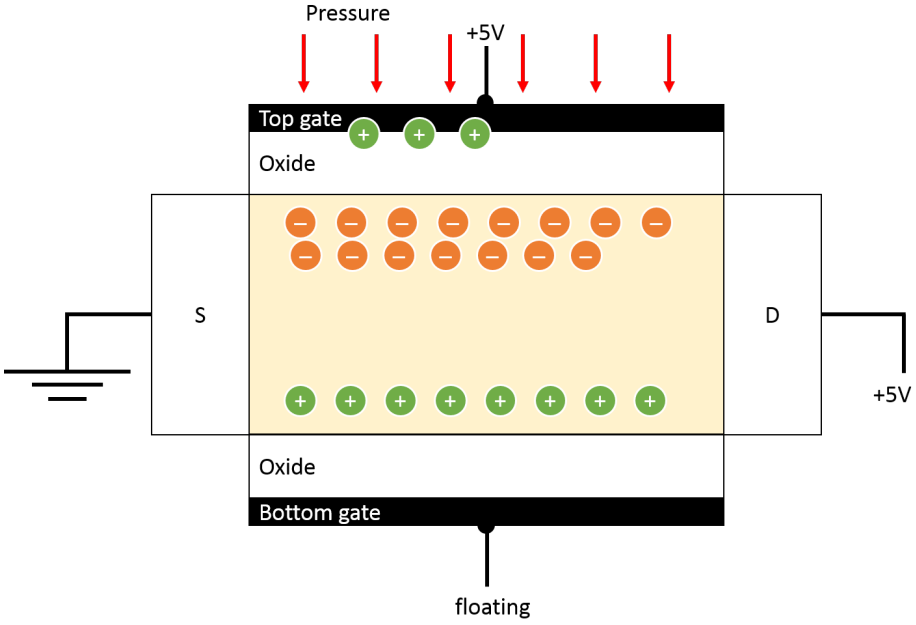
In our device configuration, the two effects are happening simultaneously. When pressure is applied while the TFT is biased in the on state, the drain current



(a) Piezoelectric charges created due to pressure



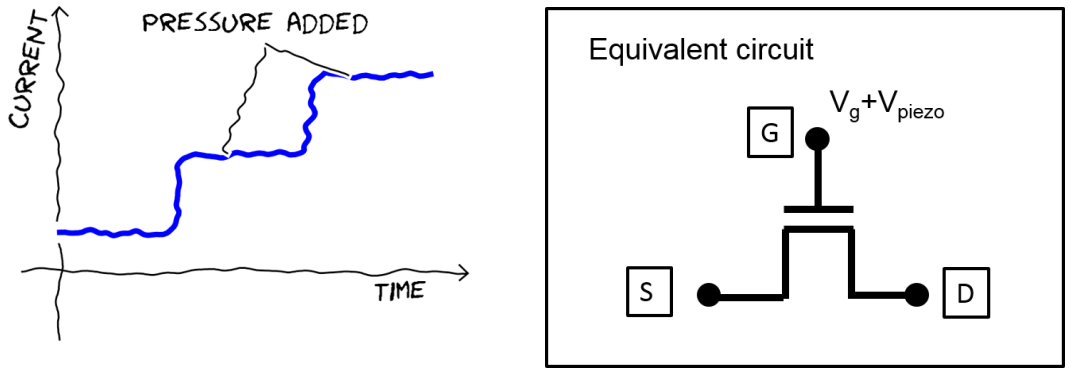
(b) Gate voltage application creates charges inside the channel



(c) The piezoelectric effect combined with the external bias

Figure 2.4: Schematic of device operation. (a) Pressure applied to the device creates piezoelectric charge distribution inside the semiconducting channel. (b) Positive voltage applied to the gate electrode induces positive charges on the metal-dielectric interface, and negative charges in the top portion of the channel. (c) The two effects happen independently from each other, and the result is the superposition of the two actions.

flowing close to the semiconductor/gate dielectric surface increases, since there are now contributions to negative charge from both the external biasing and the applied pressure. This is illustrated in Figure 2.4c. The corresponding behavior of current as a



(a) Sketch of current vs time characteristic

(b) The effect of simultaneous external biasing and the applied pressure

Figure 2.5: Circuit-level effect of applied pressure. (a) Current as a function of time at a steady bias. When pressure is exerted on top of the device, current increases with each weight addition. (b) Equivalent circuit for the ZnO TFT pressure sensor. The action of pressing on top of the device can be visualized as the superposition of a piezoelectric voltage with the gate voltage.

function of time at a steady TFT bias is shown in Figure 2.5a. Initially, current stays constant. However, when pressure is applied, the current increases. When pressure is applied further, the current increases even more. From the circuit perspective, the TFT is a three-terminal device. The effect of applying pressure is electrically equivalent to increasing the gate voltage. This can be represented in the circuit as two voltages superimposed on each other: the gate voltage and the voltage due to piezoelectric effect, as shown in Figure 2.5b.

2.3.1 Signal amplification

Much like a typical field-effect transistor, the operational principle of the ZnO TFT pressure sensor is the amplification of a small voltage through the transistor field-effect property. The small voltage created when pressure is applied due to the piezoelectric effect is converted to a large source-drain current. The benefit of our

proposed approach compared to typical piezoelectric sensor is that the amplification happens inside the sensing element itself. Here, the pressure is converted to a small voltage and is amplified to a large current. In a typical piezoelectric sensor, the pressure is converted to small voltage that then gets routed out to the measurement circuitry and needs to be amplified off site. In the ZnO TFT-PS, secondary amplification can be done by the measurement circuit after the initial gain has already been achieved by the TFT operation.

2.4 ZnO dopants

ZnO is naturally n-type, and sputtered ZnO thin films will exhibit n-type characteristics even if not intentionally doped. ZnO material can be doped by H [dW00], In [BMVP$^+$14], Ga [FRS$^+$08], Al [AKKC11], and F [CLL$^+$15], which are all n-type dopants for ZnO.

Nitrogen [PCR$^+$02], copper [SBML15], and lithium [WTPW14] can be p-type dopants for ZnO. However, p-type doping of ZnO material has not yet been achieved in a reliable and repeatable manner. The p-type conduction of ZnO has long been considered the "holy grail" of ZnO research. This goal remains elusive, as it is very difficult to achieve stable p-type conduction in ZnO thin film. Although single-scan electrical measurements might demonstrate p-type film properties, additional measurements typically result in the degradation and further disappearance of p-type behavior. Stable p-n junctions using only ZnO have been previously reported by Hazra and Basu in 2005-2006 [HB05],[HB06], however, the diode performance shown was poor and there has been a lack of follow-up reports. The interest of p-type ZnO remains to this day. Xiang et al. [XWZ$^+$07] reported growth of single-crystal phosphorous doped

ZnO nanowires. The nanowires were grown by chemical vapor deposition (CVD) and phosphorous pentoxide gas was used as the dopant source. The p-type conductivity was confirmed by FET measurements made on single-nanowire FET devices. Nitrogen is the most commonly used p-type dopant for ZnO material [Jan10]. Tu et al has included nitrogen gas during RF sputtering of ZnO to achieve p-type film evaluated by Hall effect measurements [TSM06]. At the same time, there have been multiple publications claiming p-type conductivity due to nitrogen incorporation [WYC14], and other group I (Li) and group V (N, P, As, Sb) elements [Mak10]. Another attempted approach was to oxidize zinc nitride thin film in high purity oxygen atmosphere to create pure zinc oxide [JSL10]. The resulting ZnO thin films were characterized as p-type by Hall measurement, with the Hall mobility of 0.7 $\frac{cm^2}{Vs}$.

2.5 Material selection

There are several attributes that make ZnO our material of choice. The requirement from the principle of operation above is that the zinc oxide is a transparent piezoelectric semiconductor. A survey of most of the common materials that can be reasonably deposited as a thin film is shown in 2.6. Some materials are transparent semiconductors, but do not have the piezoelectric properties. Some materials, like PZT, are piezoelectric, but are not semiconductors. The three materials that fit all three criteria are ZnO, GaN, and CdSe. Other important advantages are that ZnO is the cheapest material on the list, it is well-studied, and it can be easily deposited by sputtering. Sputtering is also the tool that is being used today to deposit the ITO film used to fabricate capacitive touchscreens. Gallium nitride deposition conditions are very demanding, and require expensive equipment. Scaling of GaN is currently

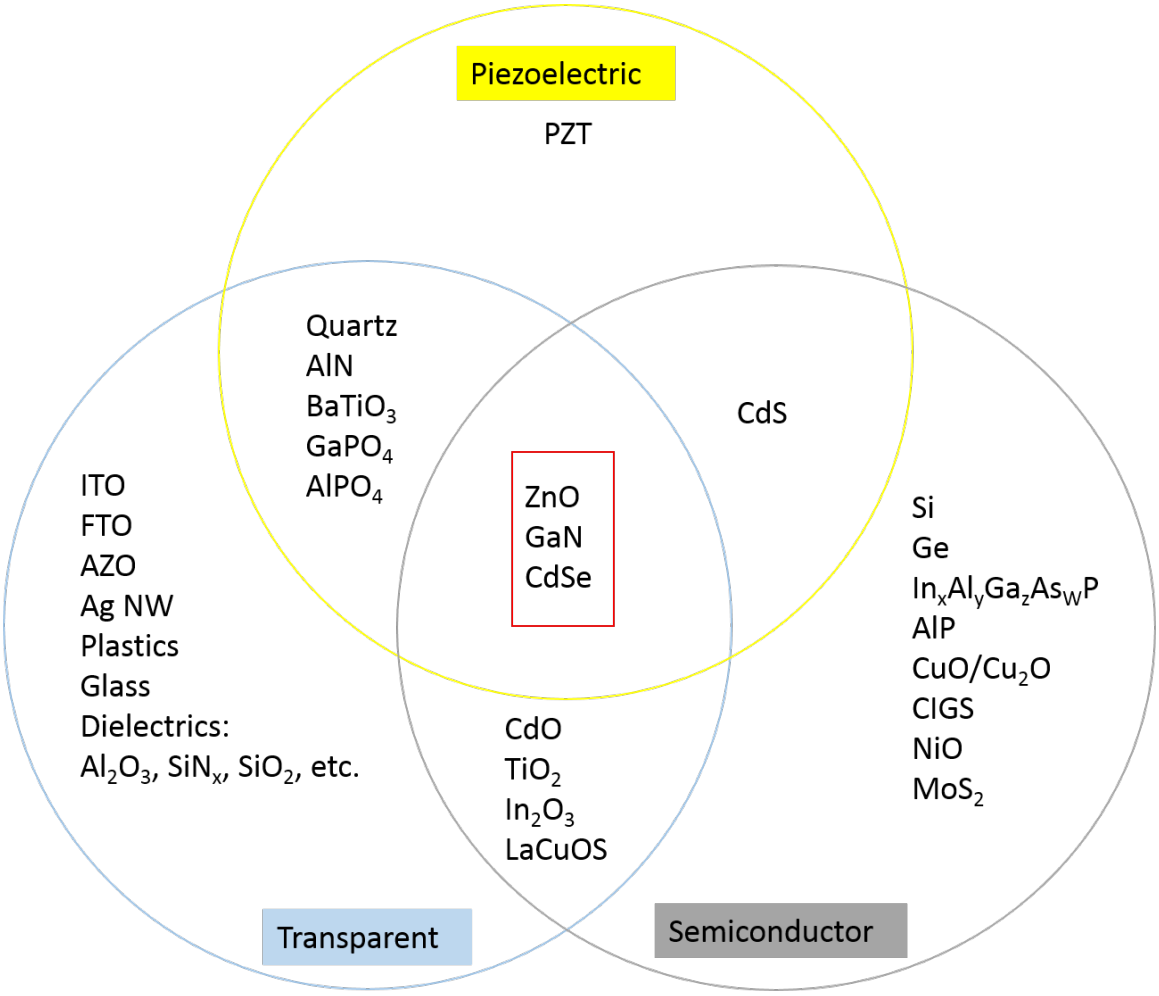


Figure 2.6: Example materials that can exist as thin films are surveyed by three properties - transparent, semiconducting, and piezoelectric. Some materials have only 1 or two of those properties, while only three materials possess all three - ZnO, GaN, and CdSe.

cost-prohibitive. CdSe TFTs have been used in displays since at least 1973 [Kuo13], and have been demonstrated to achieve mobility of 45 $\frac{cm^2}{Vs}$ and on-off ratio of 10^7 [MRSP89]. On the other hand, cadmium is expensive and toxic [Nor84]. Thin film of thermally grown CdSe have been shown to possess c-axis orientation [YBO13], and therefore it is possible that CdSe could be another material that can be used to achieve the same sensing method discussed here. In addition, the bulk value of band-gap for as-deposited CdSe is 2.3 eV, but shifts to 1.7 eV after annealing into the

hexagonal phase [KL04]. That means that the hexagonal phase of CdSe films would not be transparent in the visible spectrum.

2.6 Zinc oxide thin-film transistor operation

There are multiple challenges in fabricating a ZnO TFT. This is partially due to the large design space of the device. From the architecture point of view, there are multiple variables that can be tuned to create a thin-film transistor. Some of the variables include the active layer thickness, the substrate material, the annealing conditions, passivation layer material, and the contact material. There are also considerations like the positioning of the layers, such as top gate or bottom gate, top contact or bottom contact. For the active layer itself, the sputtering process is incredibly complicated, and there are a number of variables that can dramatically affect the resulting film. Among the variables are sputtering pressure, base pressure, RF power, gas composition, substrate temperature, substrate-to-target distance. It is even possible to come up with techniques like multi-layer growth. This results in a vast number of sputtering configurations. For example, even if 3 values are investigated for each of the 5 parameters, then this would require investigation of the properties from 243 runs. Furthermore, if a crystalline material is being grown by sputtering, then it might be necessary to optimize the growth in such a way as to reduce the number of grain boundaries, or perhaps at least improve their properties. Finally, the zinc oxide material itself is easily affected by multiple chemicals. Zinc oxide can be etched in either acidic or basic solutions. If left long enough, it can even be dissolved in water [OSH89]. The zinc oxide surface can also easily absorb water. But despite these vulnerabilities, there have been multiple reports of unpassivated ZnO TFT, with

the top surface of ZnO open to the environment [HNW03] [YKSDH$^+$09] [FBP$^+$05].

Thin-film transistor theory

To a first approximation, a thin film transistor behaves similar to a classic MOSFET device. The drain current of a MOSFET depends on the channel mobility, bias conditions, such as drain voltage and gate voltage, the threshold voltage, and the capacitance of the dielectric. The general device operation is governed by [Pie96]:

$$\begin{aligned} I_D &= 0 && (V_G < V_T) \\ V_{Dsat} &= V_G - V_T \\ I_D &= \frac{Z\bar{\mu_n}C_o}{L}\left[(V_G - V_T)V_D - \frac{V_D^2}{2}\right] && \begin{pmatrix} 0 \le V_D \le V_{Dsat} \\ V_G \ge V_T \end{pmatrix} \\ I_D &= I_{Dsat} = \frac{Z\bar{\mu_n}C_o}{2L}(V_G - V_T)^2 && (V_D > V_{Dsat}) \end{aligned} \tag{2.5}$$

Mobility extraction

Carrier mobility inside a crystal is a measure of the carrier velocity as a function of applied electric field. Higher mobility values indicate that the electrons (in an n-type device) can move faster inside the channel, thus allowing higher operational frequencies of the device. Mobility is negatively impacted by the scattering inside the channel, which can be caused by defects such as charged impurities or dislocations, and grain boundaries in polycrystalline materials. As a result, mobility extracted from experimental results is indicative of the film quality and device fabrication method, and will differ from the intrinsic bulk crystal mobility [New04]. Various types of mobility values can be extracted for the ZnO TFT, including field-effect,

saturation, and effective mobility [JP11]. The field effect mobility can be found using the transconductance at low values of V_d [FBM12]:

$$\mu_{FE} = \frac{\frac{dI_d}{dV_g}}{C_i \frac{W}{L} V_d} = \frac{g_m}{C_i \frac{W}{L} V_d} \tag{2.6}$$

To remove the dependence of the mobility value on the specific mobility extraction method, and to enable the fitting of multiple measurements of device characteristics taken at different conditions, we employed a different approach of extracting the mobility of the TFT. Instead of selecting a specific approximation to the MOSFET drain current equation 2.5, we use the entire equation to fit the experimental FET curves. Selecting two parameters as unknown, mobility and the threshold voltage, we can use numerical optimization methods to find the best fitting curve of the entire I_d-V_d or I_d-V_g measurement. Using the initial guess values at mobility of 0.1 $\frac{cm^s}{Vs}$ and threshold voltage at 0V, we are able to consistently find the best fitting values utilizing the entire set of data points, without having to manually select the "flattest" region, or the portion of the "on" state. The entire fitting script was implemented in Python, and is made publicly available at the address listed in the Appendix.

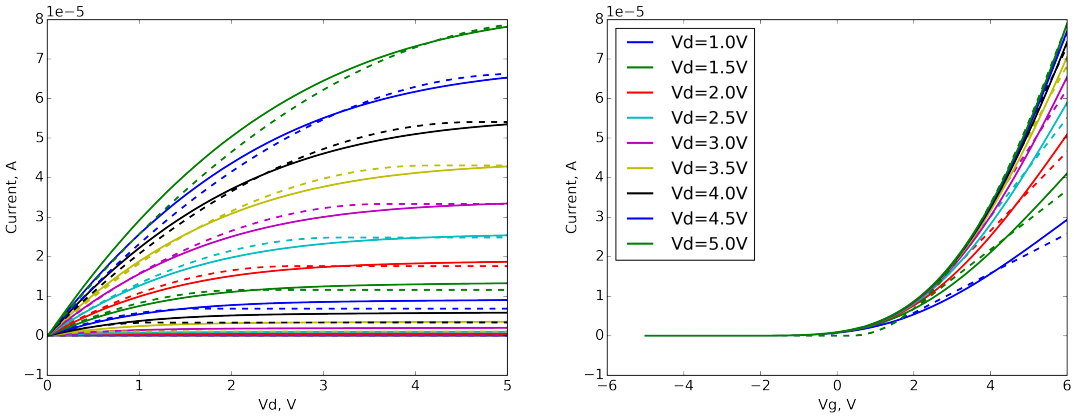
Several device parameters must be known in order to fit for mobility, and they include gate capacitance, gate dielectric thickness, device geometrical properties, and dielectric constant of gate insulator. The geometrical properties of TFTs on the mask layout with 8 devices of 6 pads are listed in Table 2.1.

An example of the data fitting for Sample 46 is shown in Figure 2.7. The device mobility was found to be 2.7 $\frac{cm^2}{Vs}$ and the threshold voltage was 0.34V. To validate

Table 2.1: Device parameters used in Mask Design 2 for 8 devices, 6 pads per device

Pad number	W, μm	L, μm	W/L	Contact width, μm	Gate-channel overlap, μm
1	1000	100	10	10	2
2	500	50	10	10	2
3	200	20	10	10	2
4	100	10	10	10	2
5	80	8	10	10	2
6	50	5	10	10	2

the mobility extraction method, the actual measurement data was compared to the fitted data using the calculated parameters. It can be seen from Figure 2.7 that the method fits the data well for both I_d-V_d and I_d-V_g type measurements. The following parameters were used for this device: gate oxide thickness of 50 nm (material: Al_2O_3), relative gate oxide dielectric constant of 10.3, and the ratio of width to length, $\frac{W}{L} = 10$.



(a) I_d-V_d measurement. V_g is measured in 0.5V steps. Green curve is for V_g=+6.0V

(b) I_d-V_g measurement

Figure 2.7: Comparison of actual field-effect measurement data (solid curves) to the fitted data (dashed curves) using the extracted mobility and threshold voltage values.

2.6.1 Measurement circuit

The drain current of the ZnO TFT is modulated by the pressure applied on top of the device. Monitoring the drain current as a function of time allows the detection of touch events in real time. When the device is maintained at a fixed bias, the same measurement setup that is used for FET characterization can be utilized to measure current vs time. For example, the gate and drain voltages are fixed such that the device is in the on state. This could be V_d=+2.5V and V_g=+5V, which would result in a current of several microamperes, depending on the particular device geometry, and TFT materials used.

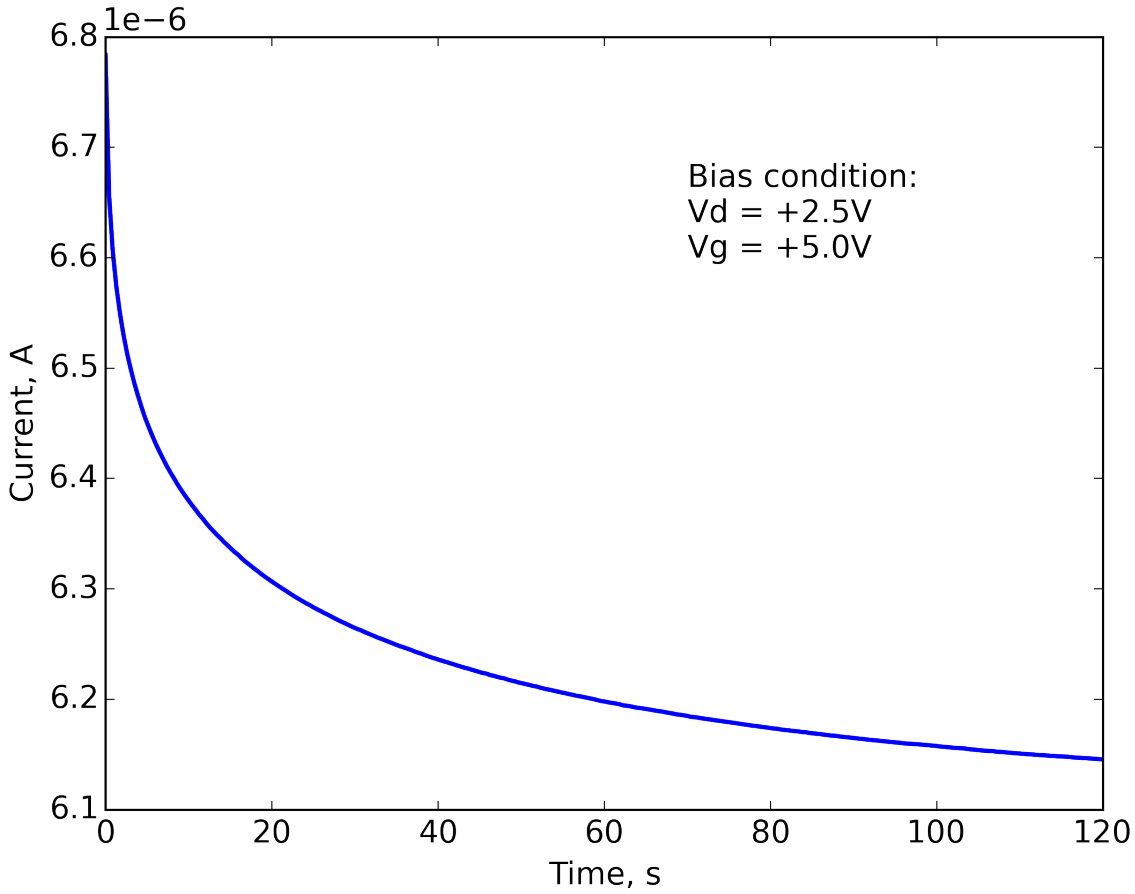


Figure 2.8: Current as a function of time at a steady bias. The current does not settle even after 60 s of measurement.

However, at constant bias, the current does not stay constant. Figure 2.8 shows the current measured as a function of time for a constant bias. The current value is changing from 6.8 μA to 6.2 μA over the time period of 120 s. The drifting does not stop even with the longer measurement times of several hours. It has been shown [EDLP10] that pulsed measurement technique can be used to reduce the hysteresis effects in carbon nanotube (CNT) devices. We employ a similar technique here to measure the drain current of a ZnO TFT.

Pulsed measurement

ZnO TFT is a three-terminal device, and therefore, there are 3 ways of doing the pulsed measurements:

1. Constant V_d, pulsed V_g
2. Constant V_g, pulsed V_d
3. Pulsed V_d, pulsed V_g

The primary focus in these experiments was method 1, where the drain voltage is fixed, and the gate voltage is pulsed. If a ZnO TFT array is to be measured, either mode 1 or mode 3 is possible. Mode 2 can never be used, since in an array, multiple devices will be sharing the same V_d, but will have different V_g connections. So, they would need to be turned off by the V_g signal, as each device is selected sequentially. Mode 1 is possible in an array, because multiple detectors can be placed to provide one per each row. In that case, each detector can be applying a constant V_d signal to the entire row, while the gate voltage is pulsed. If a single detector is used to measure the entire TFT array, then the rows of the array are multiplexed, and drain voltage is

applied to every row sequentially. Both gate voltages and drain voltages are pulsed, and mode 3 is applicable. More precisely, when the measurement of a selected row of the array is completed, the connection goes to open circuit (or to high resistance, as limited by the multiplexer). To make the measurement more stable, it is possible to briefly ground the row to discharge any devices, and then toggle to open circuit. If a device has a high on-off ratio, then the pulsing of V_d should not make a difference (from the power perspective), because in the off state, the current flowing through the device should be very low.

Measurement of device current The need for custom measurement logic creates an additional challenge for the I_d current measurements. For FET characterization, the Keithley 6487 picoammeter was used. This device is only suitable for low-speed measurements, and cannot be used for ultra-short integration times and situations where timing must be precisely controlled, and data needs to be reported as soon as it is measured. Therefore, custom approaches were employed for current measurements. Two methods of measuring currents were used: transimpedance amplifier, and op-amp integrator. The basic method of measuring a current requires the placement of a small sense resistor in series with the current being measured. The voltage reading is taken across the sense resistor, and current can be calculated using Ohm's law, $I = \frac{V_{sense}}{R_{sense}}$. This method, however, requires that the sense resistor is small, and only works well for large currents. Another drawback of this method is that the sense resistor causes a potential drop in the circuit, and therefore, perturbs the measured current value. For these reasons, the typical sense resistor cannot be utilized for our purposes. However, this technique is commonly used in the industry for measuring larger (mA-level) currents, by system architects in order to characterize the power

drawn by various components of a complex electronic device.

Transimpedance amplifier A transimpedance amplifier is the standard method for measurement of current that does not perturb the detector bias conditions. The circuit is shown in Figure 2.9. An op-amp is connected in a negative feedback configuration, with a feedback resistor positioned between the negative input terminal and the output terminal. The positive input terminal is typically held at ground. Next, the input current is connected to the negative input terminal, and this point serves as the virtual ground (as determined by the positive input terminal) to the device under test.

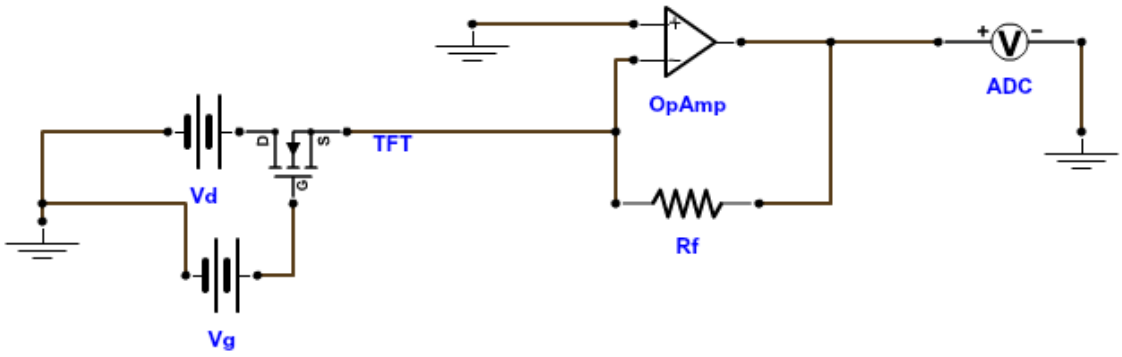


Figure 2.9: Transimpedance amplifier circuit.

The operation of this circuit can be explained by following simple steps for the op-amp circuit analysis approach:

1. The potentials at the positive and negative input terminals are equal. The positive input terminal is grounded, so the potential at the negative input terminal is a virtual ground.

2. There is no current flowing into the negative input terminal, since the op-amp has a large input impedance at its terminals, and therefore can be considered

as open-circuit. As a result, the current flowing through the feedback resistor is equal to the current flowing through the measured device. The direction of current flow is from the op-amp output terminal into the op-amp negative input terminal, and, separately, from the negative input terminal into the device being measured.

3. Under these biasing conditions, the transistor must have the other terminal connected to a negative drain bias voltage in order to keep the op-amp output above ground. Otherwise, the op-amp must be powered by a dual-supply, and would produce a negative output voltage.

4. The measured current can be calculated as $I_{measured} = \frac{V_{output}}{R_{feedback}}$.

To remove the requirement 3, a different circuit was designed by Cooper Levy to enable the single supply operation, as well as to simplify the connections, and center the output voltage between the supply rails. In the new approach, the positive input terminal is connected to +2.5V, or to the middle of the supply rails. The biasing voltage can be achieved by using a simple resistor divider with two identical resistors, potentially with a high impedance to minimize the current draw. As a result, the negative input terminal will now become 2.5V instead of ground, and will provide the required drain bias to the measured transistor. This other transistor terminal will become the source and should be tied to ground. This approach eliminates the requirement of using an additional supply for drain bias, as well as enables the single-supply operation. The working range is reduced, however, to half of the supply voltage range. This technique also prevents the independent control of the drain voltage, since the ideal drain voltage in this scheme would be equal to one half of the

supply voltage. The benefits of the transimpedance amplifier are speed and ease of implementation.

The op-amp integrator circuit The integrator circuit can be used to improve the transimpedance amplifier technique by adding an analog summing feature in place of the feedback resistor. An example integrator circuit is shown in Figure 2.10. In this technique, the feedback resistor is replaced with a capacitor. The current flowing through the measured device will now flow into the capacitor and will charge the capacitor. The capacitor voltage becomes dependent on time. Assuming a constant

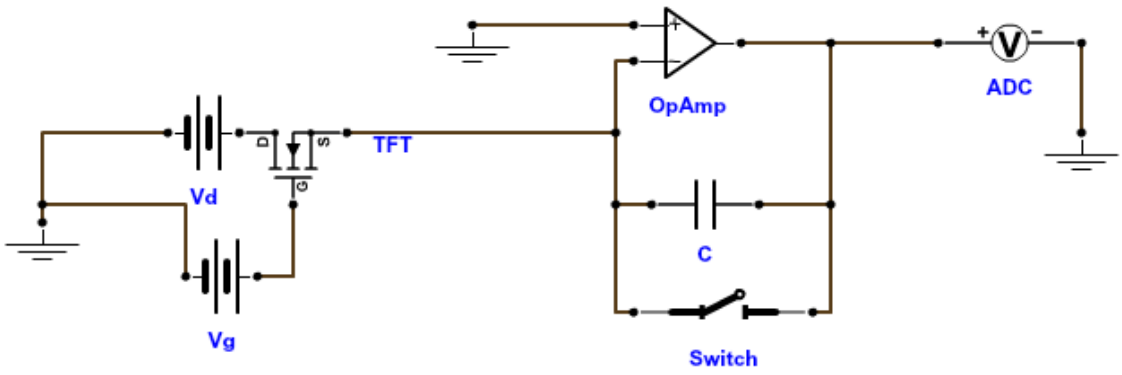


Figure 2.10: Op-amp integrator circuit.

current, the output voltage can be calculated as

$$V_{out} = \frac{I_{measured} t}{C}, \tag{2.7}$$

with the initial condition of zero charge at $t = 0$. In the context of TFT current measurements, the timing is as follows:

1. Initially, gate is set to low (device is off), and there is no charge on the capacitor.

2. Gate is set to high (such that the device is biased into the on state). Charge begins to accumulate on the capacitor and the output voltage can be found according to equation 2.7.

3. The developed output voltage is read out by the ADC. This must occur before V_{out} reaches the positive supply rail. Otherwise, the output will saturate.

4. After the voltage value is read out, the gate voltage is set to low to turn the device off.

5. The capacitor is discharged.

The last step 5 is necessary in order to restore the initial condition that the charge is zero when the integration starts. To achieve this, a voltage-controlled switch must be placed parallel to the capacitor.

Current cancellation Successful and accurate detection of pressure requires the measurement of a small change of current, on the order of few tens of nanoamperes, on a large baseline current value, on the order of few tens or hundreds of microamperes. If the current is first converted to voltage, and then canceled, the gain of the converter cannot be made arbitrarily large, since the detector will be saturated by the large current baseline. If, however, current is subtracted from the beginning, then a large gain can be used in order to amplify the current differences deviating from a small value. A simple technique devised by my colleague, Cooper Levy, enables the analog current cancellation. In this method, a digital-to-analog converter is used together with a resistor to supply the cancellation current to the summing point of the op-amp. A 10-bit DAC is sufficient to achieve good level of current cancellation, together with

a resistor value of around 30 kOhm. The DAC can be controlled by computer and can be used to calibrate the current offsets for multiple devices, which is useful in the case of array measurements. An example transimpedance amplified circuit with analog current cancellation is shown in Figure 2.11.

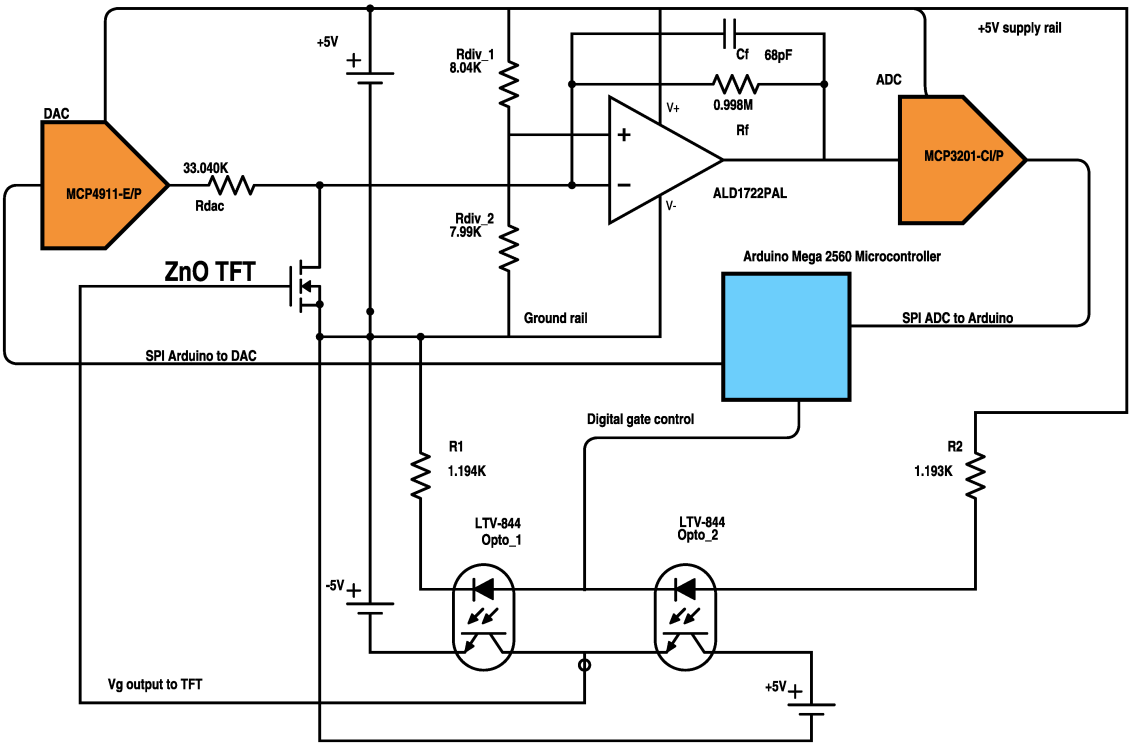


Figure 2.11: Transimpedance amplifier with analog current cancellation.

2.7 TFT array as applicable to touchscreens

Influence of device parameters on touchscreen performance The on and off currents play an important role in the touchscreen performance. The off current itself does not influence the device ability to sense pressure. However, it affects the measurement results in two ways. First, when array is in operation, the off current is flowing through all devices located on the same row. That means, for an 8x8 array

with a single detector, 7 devices have the off current flowing through them at all times. This would add to the total baseline current of the active device, and require a higher cancellation current supplied by the detector, which could limit the available precision in current canceling. A higher on current would also have the same effect. The difference is that a higher on current would typically also result in a higher current change due to pressure, and therefore a high on current is desired.

Second, a high off current will unnecessarily increase the power consumption. For example, the power drawn by the touch/force sensors can be calculated as follows:

$$P_{singledetector} = V_d * ((n-1) * I_{off} + I_{on}), \tag{2.8}$$

and

$$P_{ndetectors} = n * P_{singledetector}, \tag{2.9}$$

where the size of the array is $n \times n$, V_d is the drain voltage, I_{off} is the off current of a single sensor, and I_{on} is the on current of a single sensor. These equations are simple, because timing is not taken into account. In practical operation, devices are not biased in the on state for the entire time. There will be a delay between the current device, and the next device, which is caused by the switching delay, various addition/subtraction operations, and the ADC conversion times. This equation represents an upper bound on the touchscreen driver power, and in practice, the off current plays a more significant role than computed here.

From the pressure sensing point of view, the off current is not important, and the only significant device metric is the slope of the I_d -V_g curve at the gate voltage at the desired on-state bias during the device operation. Therefore, even if the off current

is large, slope can still be large, and there will be a large change of current happening due to pressure (which is desired). However, for a large touchscreen, perhaps 100 sensors by 100 sensors, the off current will be multiplied by a factor of 99 when power is calculated in the Equation 2.8. The situation is worse for multiple detectors, where the off current will be multiplied by a factor of $9900 \approx 10^4$. Therefore, a low off current is desired, and a reasonable value is perhaps 1 nA. In that case, for large 100x100 array, the total off current will be $10^{-9}A * 10^4 * 5V \approx 50\mu W$, a small, but non-negligible amount of power lost.

In comparison, a pressure-sensing TFT in the on state consumes tens of μA at 2.5V, which is on par with the off devices, and is on the order of 40 μW. With 100 detector lines, the sensors will draw a total of 4 mW of on-power and 0.04 μW of off power.

Chapter 3

Bottom-gate ZnO:N_2 TFT pressure sensors

Previous chapters provided a broad framework for pressure sensor technology based on ZnO TFT and the design considerations from a bottom-up (material and device) point of view. In this chapter, we focus on the practical device architecture that describes the material deposition sequence and properties.

To create a transparent TFT, all of the constituent layers of the device must be transparent. For our ZnO TFTs, we have chosen glass slides as the transparent and temperature-tolerant substrate. ITO was the transparent conductor of choice, as it is well-understood, has low resistance, and is easily deposited by sputtering. Silicon nitride (SiN_x) was used as the gate dielectric due to its high relative permittivity and the availability of conformal thin film growth.

The structure of the first set of our devices is shown in Figure 3.1. We start with glass substrate, followed by the deposition of either ITO or aluminum (for easier processing) as a gate electrode. Next, SiN_x gate dielectric is deposited by PECVD.

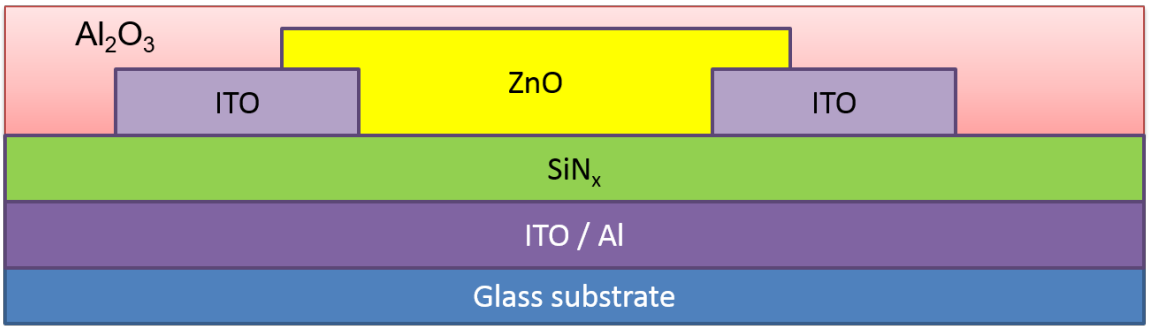
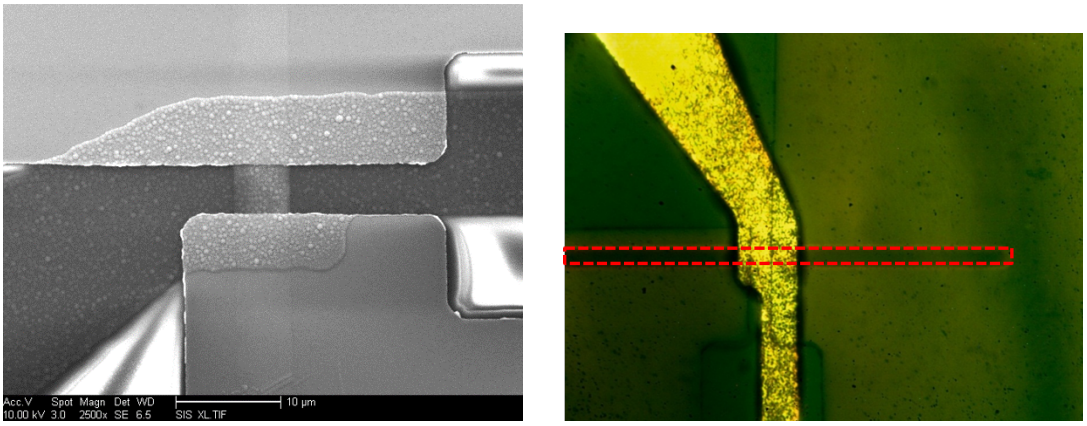


Figure 3.1: The device structure of ZnO:N_2 TFT pressure sensor. Bottom gate, bottom contact structure is built on a glass substrate.



(a) SEM image (b) Optical image

Figure 3.2: Images of 5 μm x 5 μm device. The gate electrode material is aluminum. The channel region is clearly visible in the SEM, and is highlighted by dashed lines in the optical image.

After, the ITO source and drain regions are patterned by lift-off. The zinc oxide thin film is next grown by sputtering, and patterned by lift-off. Finally, the entire device is passivated by a layer of aluminum oxide deposited by ALD. An SEM image of the device is shown in Figure 3.2a. The active area dimensions are only 5 μm x 5 μm. In the Figure 3.2a, optical image of the same device is shown. The ZnO channel is highlighted by dashed red line for clarity.

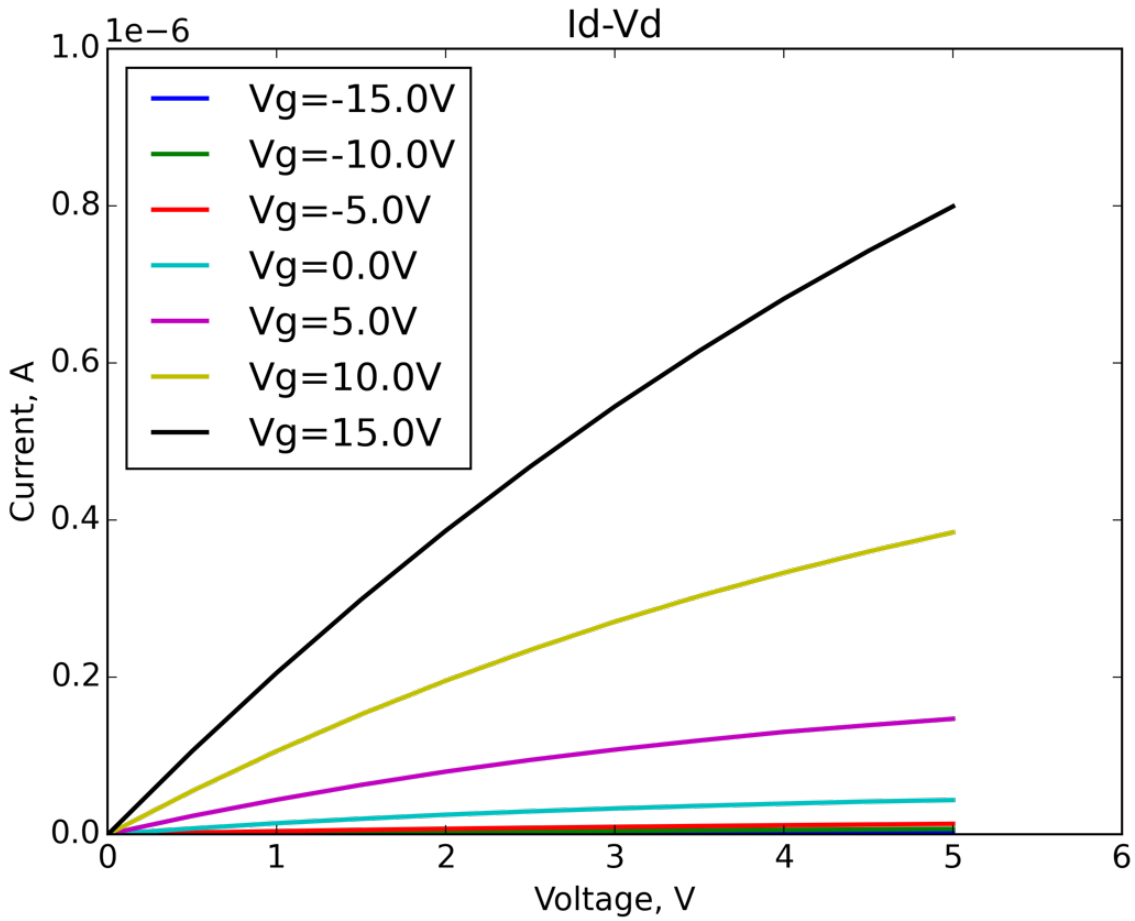
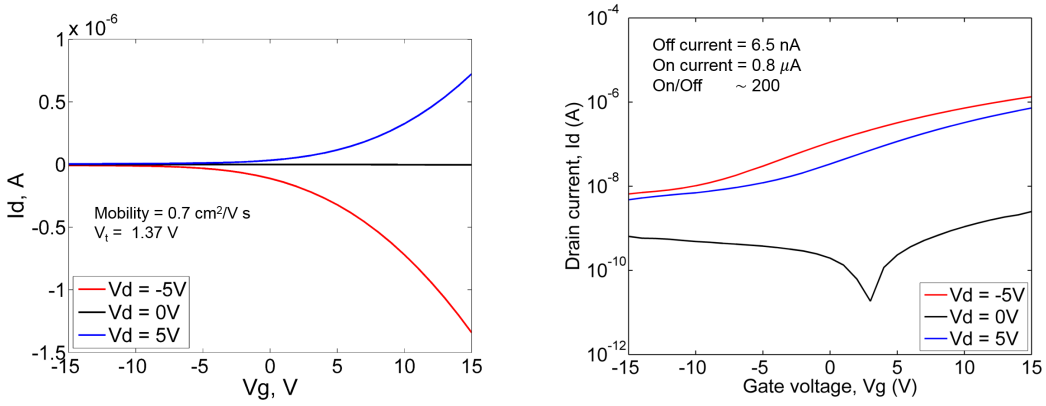


Figure 3.3: The output curve of a typical ZnO:N_2 TFT pressure sensor. The ZnO film is n-type.

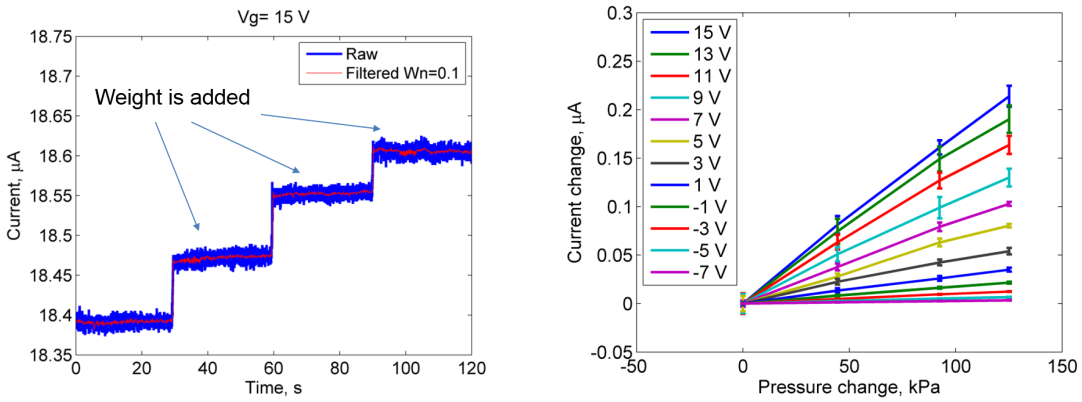


(a) Linear I_d-V_g (b) Log I_d-V_g

Figure 3.4: The linear (a) and log scale (b) transfer curves of ZnO:N_2 TFT pressure sensors. The ZnO film shows a mobility of 0.7 $\frac{cm^2}{Vs}$ and an I_{max}/I_{min} ratio of about 200.

3.1 FET characteristics

The device FET characteristics are shown in Figure 3.3. The drain current increases with more positive gate voltage applied, which suggests that the ZnO film is an n-type semiconductor. As mentioned earlier, nitrogen is a p-type dopant for ZnO. There are several reasons for the n-type nature of the film. It used to be commonly perceived that the as-deposited ZnO thin film has O vacancies, which act as donors. However, it has been shown that the O vacancies are actually deep donors, and cannot account for the level of n-type conductivity observed in undoped films [JdW05]. The n-type conductivity could be caused by the incorporation of impurity species, such as hydrogen, into the lattice, which act as electron donors. It has been shown that hydrogen is an n-type dopant for ZnO. Hydrogen molecules are small, and it can be difficult to pump out residual hydrogen from the sputtering chamber [dW00]. Another possibility is that structural defects in the film act as n-type dopant centers [MÖ08]. Most likely in our device, the nitrogen species counterdopes the native n-type conductivity arising from impurities and defects. The absence of nitrogen would mean that the electron concentration would be very high, and the film would be difficult to turn off. For our device, the operating voltage is from +15V to -15V, which is already large, and not optimal for portable device applications, which are typically powered by a 5V battery. The transfer characteristics of the device are shown in Figure 3.3. The device mobility has been extracted by fitting the entire curve to the standard MOSFET equations. The mobility is 0.7 $\frac{cm^2}{Vs}$ and the threshold voltage is 1.37V. From the log-scale plot, the off current is determined to be about 6.5 nA and the on current is 0.8 μA. The device I_{max}/I_{min} ratio is about 200.



(a) Current vs time with pressure applied

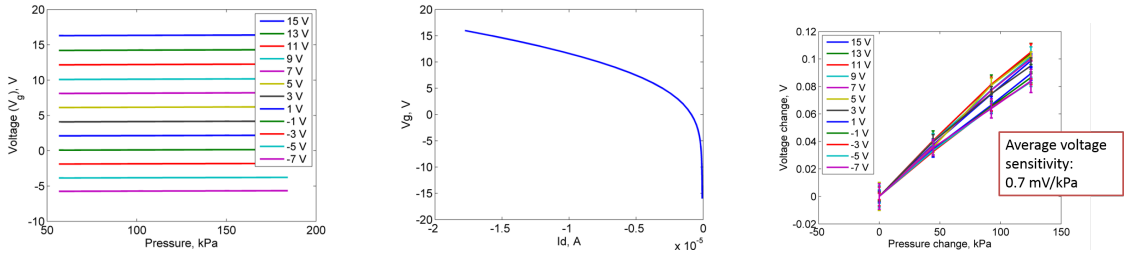
(b) Current change vs pressure at different V_g

Figure 3.5: (a) Current increases with each weight as it is added on top of the TFT. (b) Current changes linearly with pressure.

3.2 Pressure sensing with ZnO TFT

Next, we performed the pressure characterization of the device. The plot of current as a function of time is shown in Figure 3.5a. Three weights of similar mass are added in 30 s intervals. The current increases with added weight. This change of current can be plotted as a function of the applied pressure. This graph is shown in Figure 3.5b. Similar curves were collected at various gate bias conditions. The change of current gets smaller as the gate voltage decreases. Referring back to the previous visualization of the pressure action, this graph can be thought of as the mapping of the slope of the I_d-V_d graph. If the device is biased in a region where the I_d-V_g graph has a large slope, then small variations in the gate voltage caused by the applied pressure will result in large changes of the drain current. Alternatively, when the device is biased in a region with flat I_d-V_g curve, then the pressure application will not have a significant effect on the drain current.

The I_d-V_g graph can now be used to look up the values of equivalent gate



(a) Equivalent gate voltage as a function of pressure

(b) Flipped I_d-V_g curve for look-up of voltage values

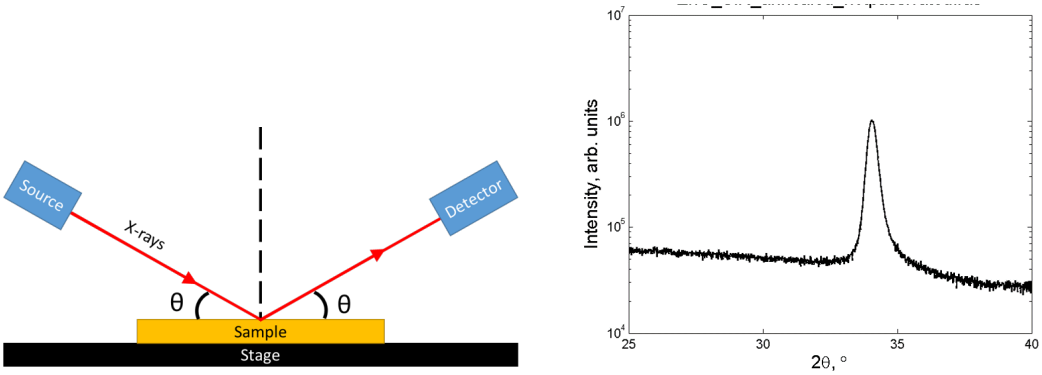
(c) First-generation ZnO TFT effective voltage sensitivity

Figure 3.6: The method of extracting the effective change of gate voltage as a function of pressure. First, current as a function of time is converted to the effective gate voltage as a function of time (a). To convert between current and voltage, the I_d-V_g plot is flipped (b) and the current values are looked up on this curve. Finally, the effective voltage change is plotted as a function of applied pressure.

voltage at a given drain current. Then the graph of drain current as a function of time with pressure applied for different V_g biases can be converted to a graph of gate voltage as a function of time, which would include the change of gate voltage due to pressure. This extraction process is illustrated in Figure 3.6. The equivalent change of gate voltage as a function of pressure is shown in Figure 3.6c. Although this is plotted for multiple values of V_g, the change of voltage does not seem to depend on the bias gate voltage. This is expected, because the piezoelectric effect should be independent of the external biasing of the TFT. The extracted voltage sensitivity is 0.7 mV/kPa.

3.3 XRD imaging of ZnO thin films

In order for the proposed pressure sensing mechanism to be valid, the ZnO film must grow with the c-axis oriented perpendicular to the substrate, such that the applied pressure is normal to the c-plane. With the help of Prof. Oleg Shpyrko's group in the Physics Department, we have been able to confirm the orientation of the



(a) XRD measurement setup (b) XRD scan results for ZnO thin film

Figure 3.7: Theta-two theta XRD measurements of ZnO thin films.

deposited films by analyzing ZnO thin films using X-ray diffraction (XRD). The XRD measurement setup is shown in Figure 3.7. The measured sample is positioned on a stage, and the X-ray source is placed at an angle θ to the substrate. The incoming X-rays interfere with the sample's crystal planes, and cause constructive or destructive interference in the reflected intensity of the X-rays. The intensity is picked up by the detector placed at an angle θ. According to Bragg's law, the distance between the crystal planes determines the angle at which the diffraction peak will be observed. For the ZnO c-axis oriented films, the inter-planar distance is equal to about 5.2Å, which corresponds to a diffraction peak at about 34°. The relevant peak observed by our measurement is shown in Figure 3.7b. The results indicate strong crystallinity of the deposited films, as well as the c-axis orientation of the grains.

3.4 ZnO TFT array

After the single pressure sensor has been developed and characterized, we have proceeded to fabricate an 8x8 array of pressure sensors on glass. Every device acts as a switch and a pressure sensor simultaneously, and this property allows the devices to be

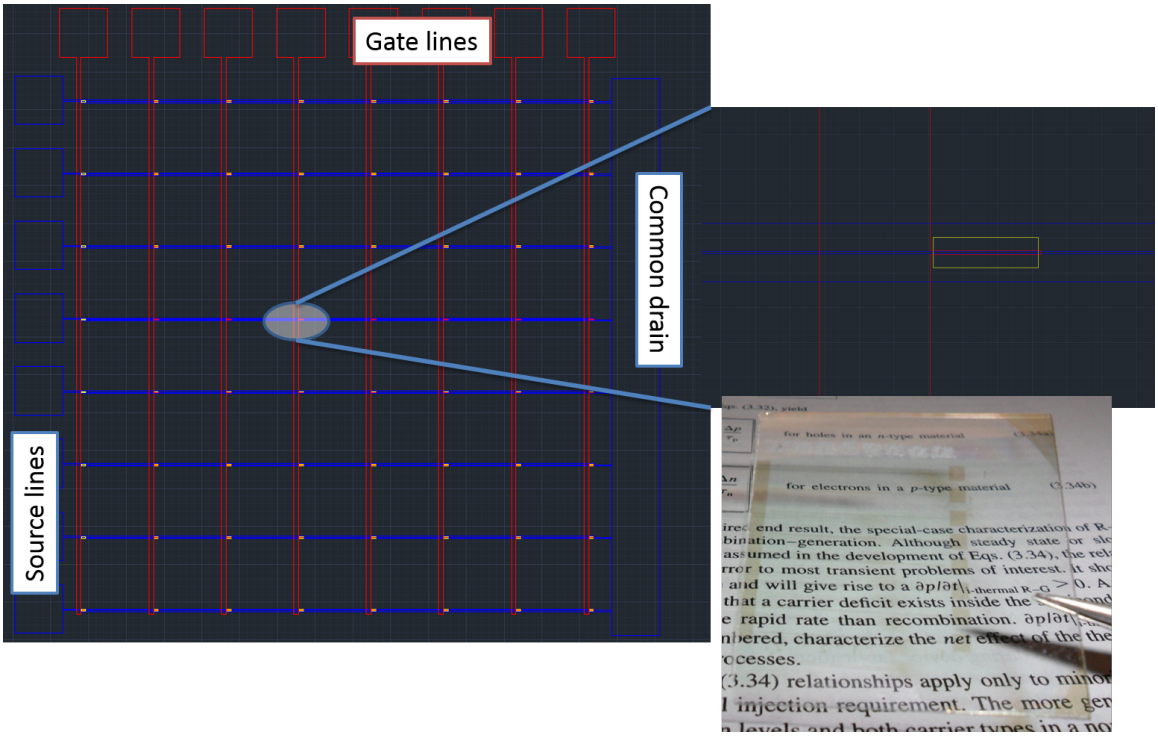
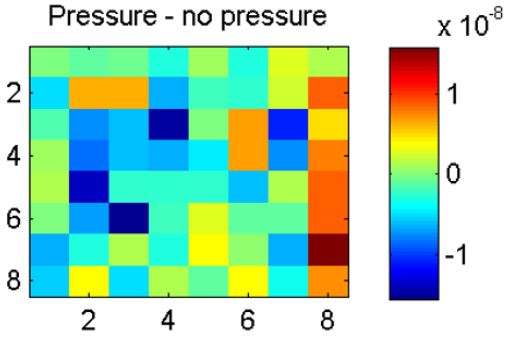


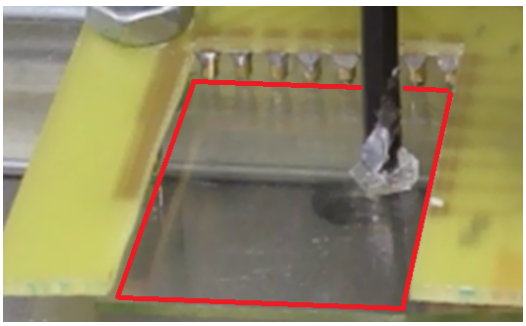
Figure 3.8: Snapshot of the 8x8 array layout. Optical image of the fabricated device is shown in bottom right corner. A single pixel has W/L ratio of 10.

connected in a row-and-column fashion, while maintaining the ability to isolate a single pixel in the array. The layout for the 8x8 array is shown in Figure 3.8, and bottom right frame shows an optical image of the fabricated device on glass. For the 8x8 array, there are 8 gate electrodes, 8 drain electrodes, and one common source electrode, which is usually held at the ground potential. In a typical measurement approach, a single pixel is isolated by setting the appropriate biases to the gate columns, and selecting the drain connection of interest via a multiplexer. The current through one pixel is measured, and then the current of the next next pixel is measured, until the whole array is scanned.

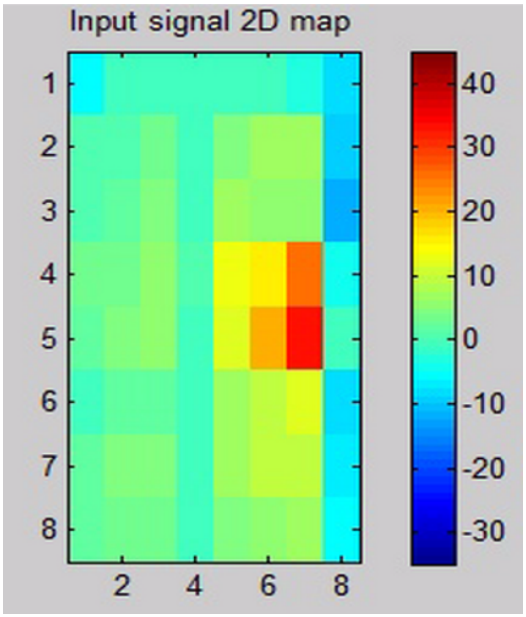
To detect pressure, a reference measurement is first taken with the advance knowledge that there is no pressure applied. This frame of 8x8 (64) measurements is called the baseline. The baseline is stored in computer memory. During the operation



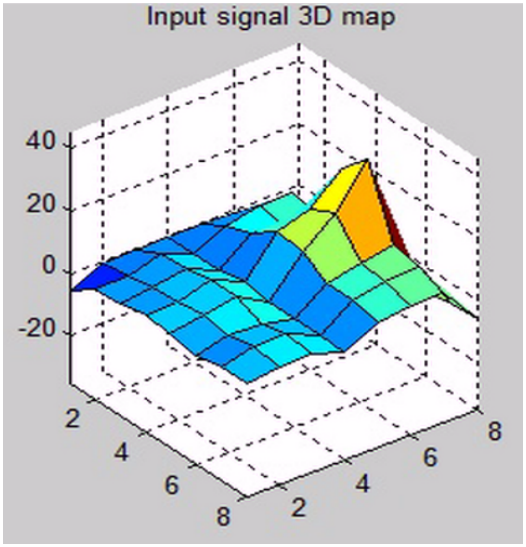
(a) No pressure is applied. Noise is about 10^{-8} A



(b) Insulating object pressing in the middle right location of the array

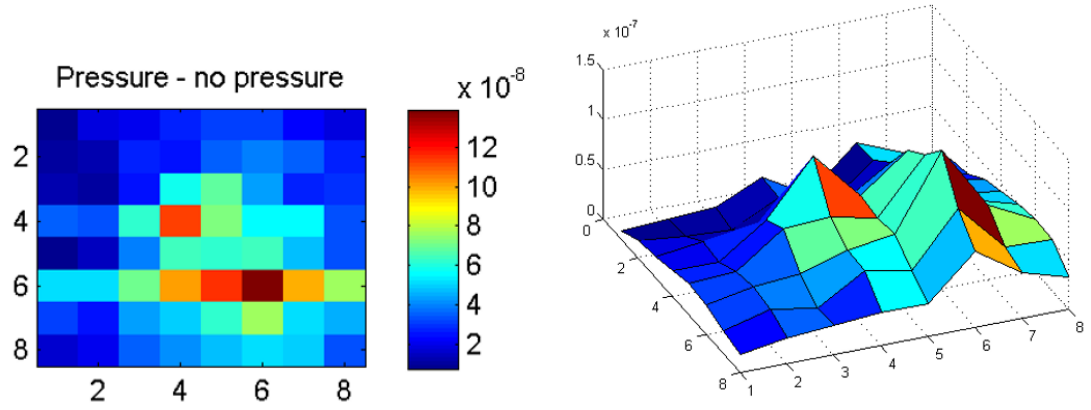


(c) 2D color map of applied pressure



(d) 3D surface map of applied pressure

Figure 3.9: Sensing of a single object pressing on the ZnO TFT-PS array.



(a) Color map (b) Surface map

Figure 3.10: 2D color map (a) and 3D surface map (b) of the measured currents on the array of pressure sensors. Two objects are pressing on the array in the corresponding locations.

of the device, new measurements are continuously taken from the array, and the measured frame is subtracted from the baseline. The difference is plotted as a 2-dimensional color map, or as a 3-dimensional surface map. Figure 3.9a shows the measurement result of the device without any pressure applied. When no pressure is applied, there are no significant changes of current in any of the pixels. The current varies by itself due to noise, which is on the order of 10 nA.

Next, an insulating object is used to apply pressure (by hand) onto the force sensing array. We used a PDMS-coated metal rod in order to apply pressure, as shown in Figure 3.9b. The device has not been covered by hard coating, and therefore a soft object was used to prevent scratching. The measurement results of a single object pressing on the sensor array are shown in Figure 3.9. The signal of several hundred nanoamperes is due to relative high pressure applied on the device. If the system noise is significantly less, then it becomes possible to measure smaller changes of current, and therefore increase the pressure sensitivity. For example, capacitive touchscreen drivers typically measure current changes that are on the order of nanoamperes. We

have also demonstrated that the sensors in the array are independent. Two objects are used to press on the device. The pressure increase happens in the corresponding locations, as can be seen from both the 2D heat map and from the 3D surface plot in Figure 3.10. In the context of multi-touch, the device can support an arbitrary number of pressure points, since each pixel is independent.

3.5 Acknowledgements

Chapter 3, in full, is a reprint of the material as it appears in Scientific Reports, 3 (2013). Siarhei Vishniakou, Brian W. Lewis, Xiaofan Niu, Alireza Kargar, Ke Sun, Michael Kalajian, Namseok Park, Muchuan Yang, Yi Jing, Paul Brochu, Zhelin Sun, Chun Li, Truong Nguyen, Qibing Pei, and Deli Wang. Tactile feedback display with spatial and temporal resolutions, Nature Publishing Group (2013). The dissertation author was the primary investigator and author of this paper.

Chapter 4

ZnO TFT optimization

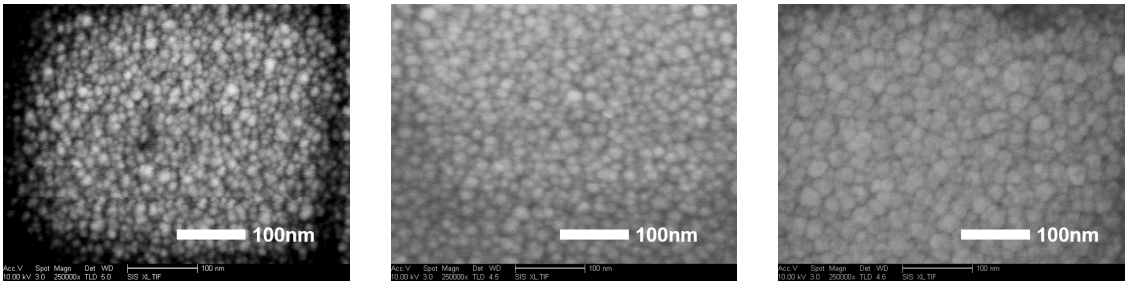
After the successful demonstration of working ZnO TFT pressure sensors and pressure sensor array, we sought to improve the TFT performance by optimizing the film properties. We will show the results here for various device optimizations. The objective is to increase the pressure response and improve the switching characteristics of the ZnO TFT-PS. The transistor action in ZnO TFT is to amplify the small piezoelectric voltage created due to pressure into a large change of channel current. One way to improve the pressure sensing qualities and the transistor performance simultaneously is to improve the transconductance parameter g_m. In a MISFET, the small-signal transconductance g_m is defined as

$$g_m = \frac{\partial I_d}{\partial V_g}\,, \tag{4.1}$$

where I_d is the transistor drain current, and V_g is the gate voltage. The transconductance can be increased by thinning down the semiconductor channel layer in order to improve the electrostatic control of the channel by the applied gate voltage. Another

way to increase g_m is to change the sputtering conditions to grow a ZnO film with less defects, different doping profiles, or less structural defects and therefore reduced scattering. Another way is to improve the contact between metal and semiconductor. The output signal due to pressure can also be made larger by increasing the crystallinity of the zinc oxide layer, in order to have a higher voltage for a given pressure. The crystallinity can be increased by growing larger grains, more aligned grains, or by having less grains of opposing polarity. From the commercial point of view, device can be also optimized by using cheaper materials to lower the manufacturing costs. Finally, for the touchscreen applications, optical properties must also be considered, where a device with maximum transparency is desired, such that the interference with the picture created by the display underneath the touchscreen is minimized.

4.1 ZnO thickness study



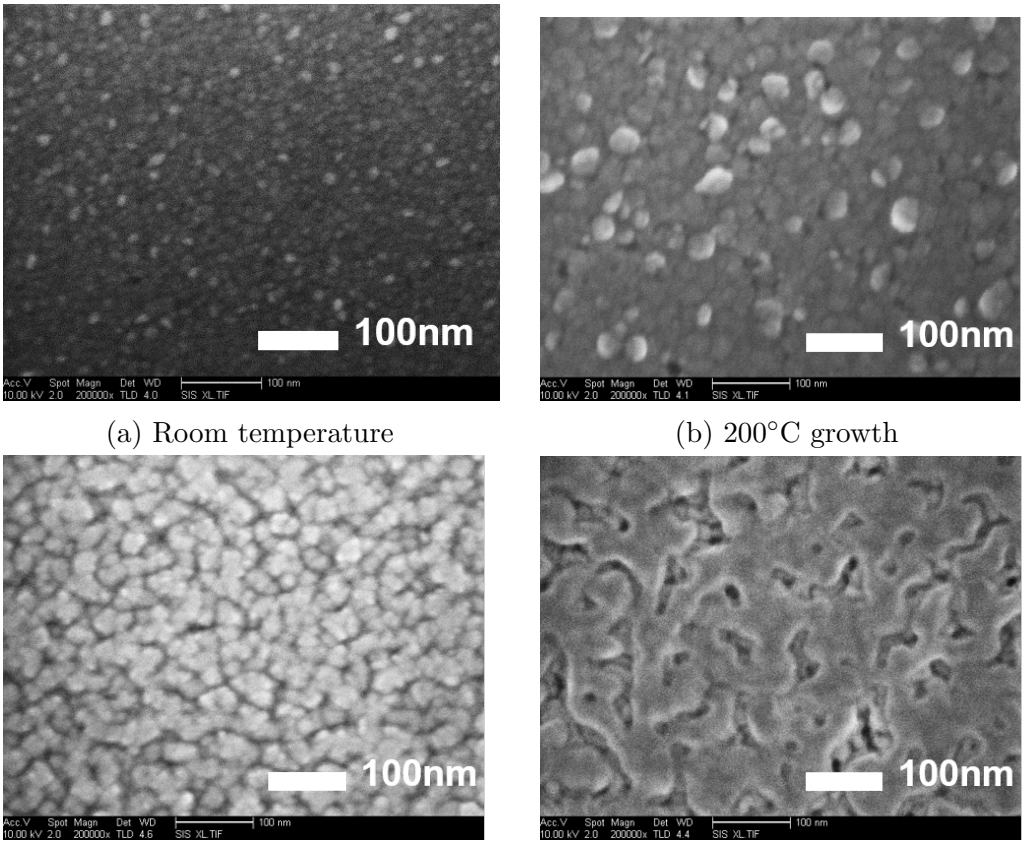
(a) 30 nm thickness (b) 60 nm thickness (c) 90 nm thickness

Figure 4.1: High-resolution SEM image of ZnO film grown to various thicknesses. Film starts to coalesce at the 60 nm thickness.

We first studied the effect of reducing film thickness. It is desired that the grains are completely coalesced, so that a continuous ZnO film is formed. The films are checked using scanning electron microscopy (SEM). The top-view SEM images were taken for films grown with 30 nm, 60 nm, and 90 nm thickness. The results are

shown in Figure 4.1. The grains are coalesced at 60 nm, while at the lower thickness of 30 nm, island-like uncoalesced film is observed. The thickness of 60 nm was chosen as the target value for subsequent experiments.

4.2 Substrate temperature study



(a) Room temperature (b) 200°C growth

(c) 400°C growth (d) 400°C growth + annealing at 600°C

Figure 4.2: High-resolution SEM images of ZnO films grown at different substrate temperatures. Higher growth temperature results in a smoother film with larger grains.

The next variable we investigated was the substrate temperature. This is the temperature of the sample during sputtering. Films were grown at room temperature, 200°C, 400°C, and 600°C. For the 600°C film growth, we found that the film is not

uniform, with some areas having no visible growth. This suggests that a thermodynamic limit has been reached, and at that temperature the ZnO is also actively desorbed from the surface. Therefore, instead of growing at 600°C, the sample was grown at 400°C and then annealed at 600°C. The SEM images are shown in Figure 4.2. The annealed film resembles a continuous layer of ZnO. While as-grown films were coalesced, the film grown at 400°C has multiple grains of about 30-50 nm, and the grains appear quite uniform. The film grown at 200°C also has large grains, with some of the grains misplaced. The grains in the sample grown at room temperature are quite small.

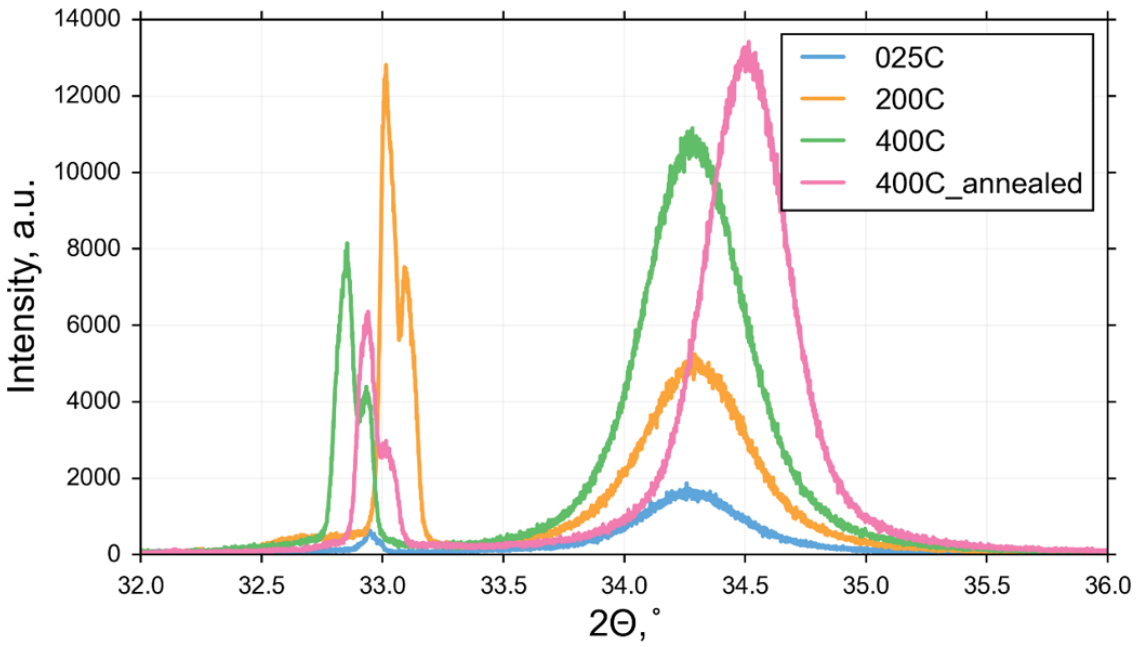


Figure 4.3: X-ray diffraction measurements of ZnO thin films grown at different substrate temperatures.

We used XRD to further characterize the crystallinity of the films. The results are plotted in Figure 4.3 and analysis of the peaks is summarized in Table 4.1.

[5]calculated by Scherrer formula 6.1

Table 4.1: Summary of the results of substrate temperature variation

Temperature, °C	Deposition rate, $\frac{Å}{s}$	(0002) Peak, °	FWHM, °	Grain size [5], nm	Lattice constant c, Å
Room temp	nominal	34.28	0.49	17	5.23
200	medium	34.30	0.51	16	5.23
400	slow	34.29	0.49	17	5.23
400 annealed	n/a	34.51	0.41	20	5.20

The double peak near 33° is due to substrate, as confirmed by the measurement of a reference sample without any ZnO film deposited. The ZnO (0002) peak is near 34.3°, and shifts to around 34.51° degrees after annealing. This corresponds to the ZnO lattice constant c decreasing from 5.23Å to 5.20Å. Therefore, annealing might be causing a reduction in the lattice strain, as well as the rearrangement of atoms into the thermodynamically more favorable position. Another possible explanation for this behavior is that the nitrogen atoms at this temperature are leaving the ZnO lattice, and thus the films approach the "bulk" value of the c axis constant. We have also noted that the deposition rate of ZnO decreases as the temperature increases, and the sputtering times were adjusted accordingly in order to create films of the same thickness.

Our film deposition results are in close agreement to the values published by Sivoththaman in the arXiv article[JS14]. However, the peak locations and the resulting calculated c axis constants are quite different from other reported values [Ji10]. The c axis lattice constant for bulk ZnO is 5.2Å. In comparison, zinc nitride has cubic crystal structure with a lattice constant of 9.78Å [KTS93]. The larger calculated lattice constant in our results could indicate the presence of nitrogen atoms in the ZnO lattice, effectively making it an alloy zinc oxinitride film.

The increased deposition temperature from 100°C to 400°C has also been shown to improve the crystallinity of the pulsed laser deposition-grown ZnO thin films [BL11].

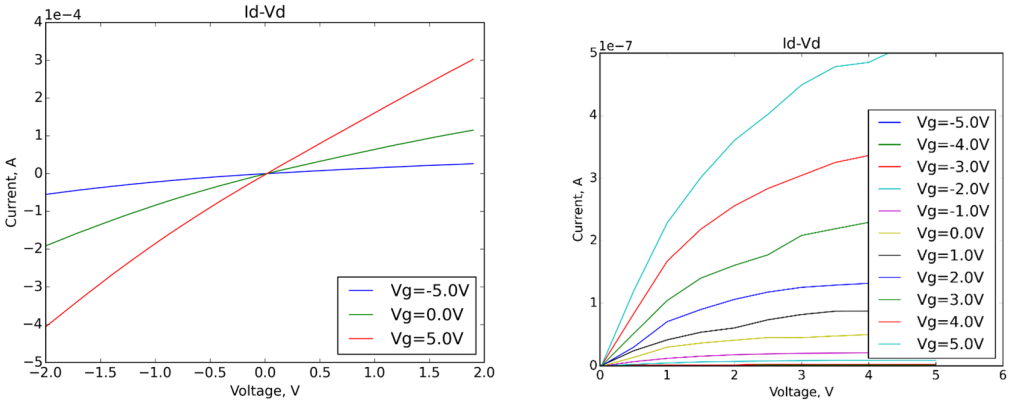
As the temperature increases, the XRD peak intensity increases, which is consistent with our observations in the SEM images. There is a trade-off involved in the substrate temperature variation. The structural properties of the film are improving with higher temperature. However, higher temperature also means more expensive processing and limits the choice of possible substrates. Most flexible substrates are usually limited to 200°C, while the maximum temperature for PEN is 150°C, and for PET it is 120°C [LNWO11]. In the case of ZnO TFT, the film grown at 200°C is the best compromise between the film properties and the low temperature.

4.3 Sputtering gas optimization

Improving the on-off ratio of the device will reduce the power consumption of the TFT and simplify the read-out electronics by lowering the total current flowing through the detector. The on-off ratio is usually also co-dependent on film mobility. We have investigated the effects of the two common gases during ZnO sputtering, oxygen and nitrogen, on the morphology and electrical properties of the ZnO TFT.

4.3.1 I-V measurements

When the TFT device was fabricated with the N_2 sputtering gas, we found that it was not possible to turn off the device. Under a negative gate bias, there is still a large off current flowing, resulting in on/off ratios of below 10. This indicates a high conductivity of the ZnO channel under that condition. Therefore, the sputtering



(a) ZnO:N_2 TFT (b) ZnO:O_2 TFT

Figure 4.4: I_d-V_d measurements of ZnO TFTs sputtered with N_2 and O_2 gases. The off-currents are low for the ZnO:O_2 device.

gas was switched from N_2 to O_2. Although nitrogen is a p-type dopant of ZnO as was shown earlier, there is likely a large amount of unwanted dopants that are still incorporated into the crystal lattice. The addition of the oxygen gas into the fabrication flow results in a more resistive film having a low off current.

4.3.2 XRD measurements

The films were further characterized by XRD, and the measurement results are summarized in Figure 4.5. To improve the film uniformity, we have included a seed layer grown at room temperature into the films. In the case of nitrogen gas, it appears that the seed layer degrades the film morphology, since the grains become less oriented and smaller. However, the film grown with oxygen gas has a stronger peak, indicating better crystallinity.

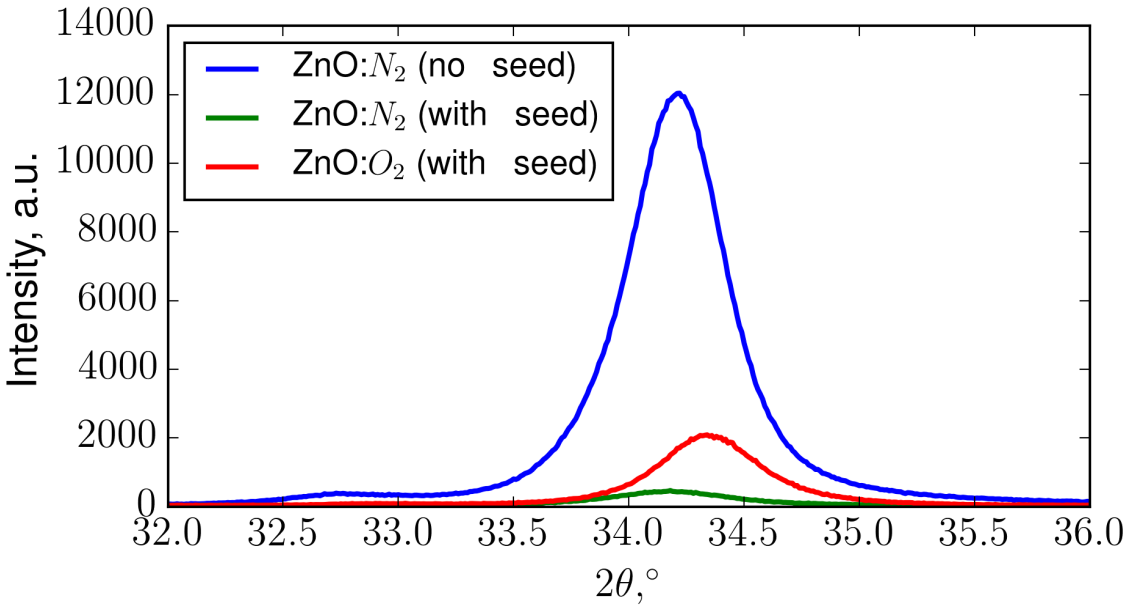
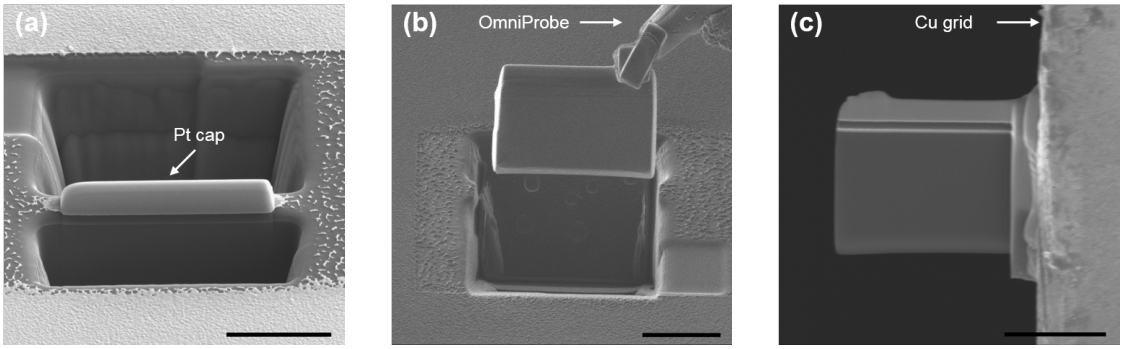


Figure 4.5: X-ray diffraction measurements of ZnO thin films grown with different sputtering gases.

4.3.3 TEM measurements

The same films were also characterized by transmission electron microscopy (TEM). TEM samples were prepared by focus ion-beam (FIB) milling and in-situ lift-out (INLO) process, as shown in Figure 4.6. Prior to FIB milling, 400 nm SiN_x and 50 nm Pt were deposited on top of the sample to prevent damage to the area of interest by the ion beam. The FIB and INLO process utilized here follow conventional procedures [GKS+05], in which a 30 keV Ga beam was used for rough milling and reduced voltage (5 keV) was used for fine milling. In-situ lift-out of sample lamellae was done by OmniProbe, and transferred onto Cu TEM grid for imaging.

The crystalline structure of sputtered ZnO layers was characterized by an FEI Tecnai F30 transmission electron microscope (TEM). Due to the polycrystalline nature of sputtered ZnO thin film, the TEM sample lamellae were aligned according to the [110] zone axis of Si substrate. The results for the ZnO:N_2 films with no seed layer



(a) FIB cut trenches

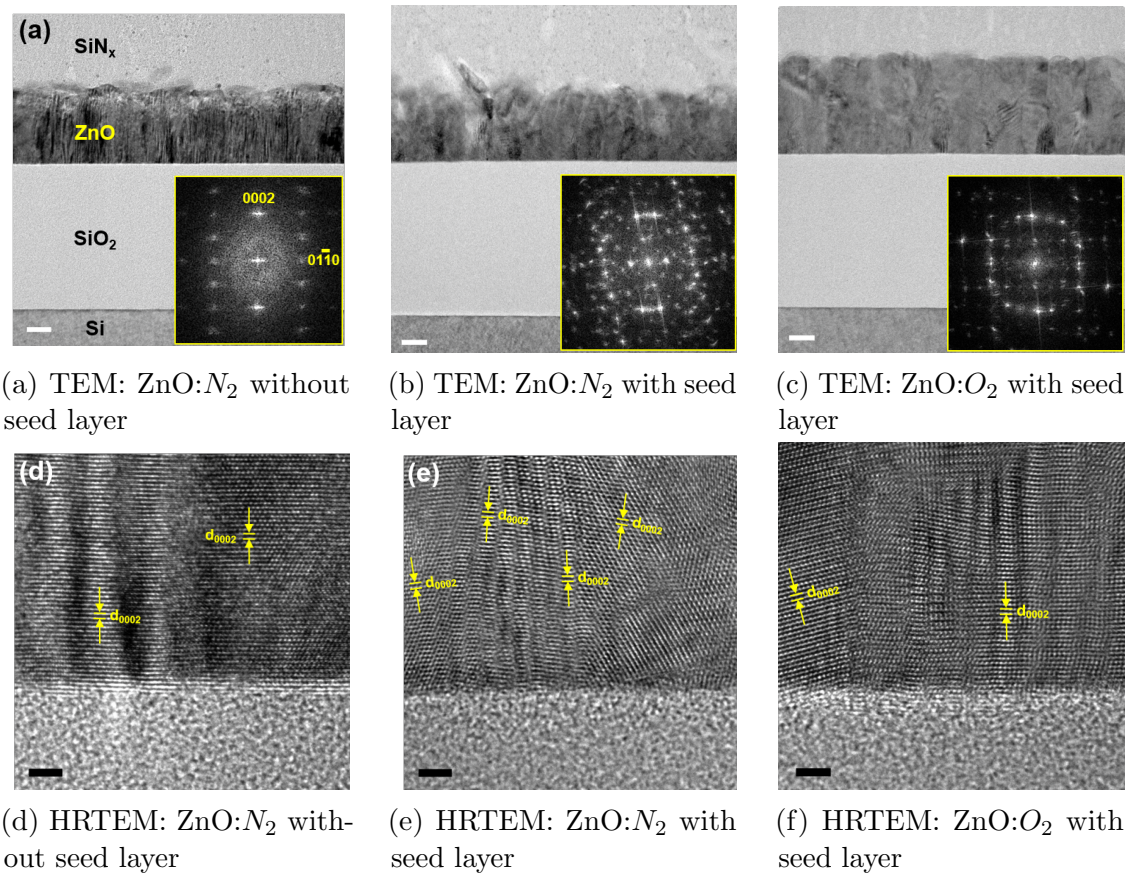
(b) In-situ liftout of sample lamellae by OmniProbe

(c) Sample lamellae transferred onto Cu TEM grid

Figure 4.6: TEM sample preparation. Scale bars are 5 μm.

are shown in Figure 4.7a and 4.7d. Darker contrast in Figure 4.7a indicates that most of the grains are aligned well along the [2-1-10] zone axis of ZnO. HRTEM image in Figure 4.7d shows that most of the grains have the [0001] facets perpendicular to the substrate, though some dark fringes are caused by the interference of multiple grain boundaries. The measurements for the ZnO:N_2 film with seed layer are shown in Figure 4.7b and 4.7e. Multiple small grains (see HRTEM in Figure 4.7e) from the seed layer have random orientations, leading to the scattered diffraction patterns shown in Figure 4.7b insert. This is consistent with the lowest XRD peak among these three samples. The images of the ZnO:O_2 films grown with seed layers are shown in Figure 4.7c and 4.7f. Multiple small grains (see HRTEM in Figure 4.7f) from the seed layer have nearly aligned orientations.

It can be concluded from the SEM, XRD, and TEM characterization of ZnO films that sputtering gases not only affect the conductivity and the doping level of the channel, but also change the morphology of the grains.



(a) TEM: ZnO:N_2 without seed layer

(b) TEM: ZnO:N_2 with seed layer

(c) TEM: ZnO:O_2 with seed layer

(d) HRTEM: ZnO:N_2 without seed layer

(e) HRTEM: ZnO:N_2 with seed layer

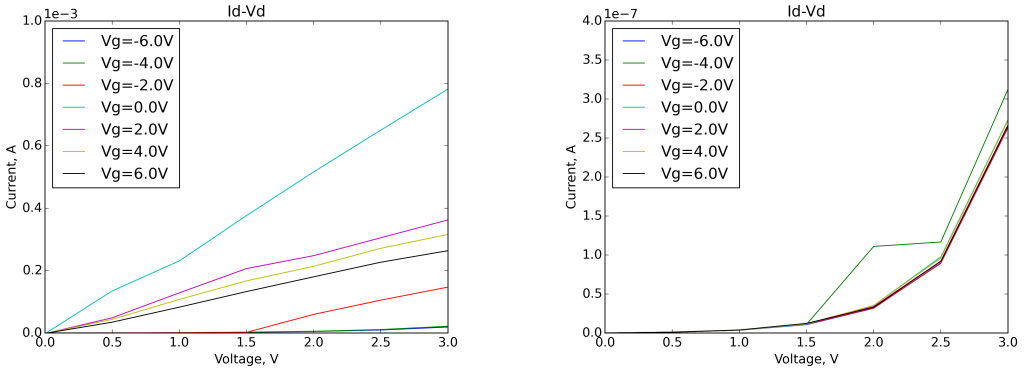
(f) HRTEM: ZnO:O_2 with seed layer

Figure 4.7: TEM characterization of sputtered ZnO films. Scale bars are 20nm for (a)-(c), and 2nm for (d)-(f)

4.4 Contact materials

Throughout this work, we used ITO as the material of choice to make the Ohmic contact to ZnO. On the other hand, significant portion of the touchscreen cost is due to material cost of the ITO, and recently, there has been significant interest in replacing this material with an alternative. Other approaches, such as Ag NW, CNTs, and cheaper metal oxides have been utilized as transparent or nearly transparent (due to small trace width) conductors. In general, indium and tin are expensive and rare, and zinc-based materials are inexpensive. The main disadvantage of AZO is its lower conductivity as compared to ITO. This is one of the main reasons it has not been able

to replace ITO. However, in the ZnO TFT pressure sensor, most of the resistive drop (MΩ-level) occurs in the sensor itself. In that case, the line resistance (few kΩ to 10 kΩ) does not affect the operation of the sensor. Therefore, the device is not as sensitive to resistive drops in the lines compared to the standard capacitance approaches. This makes ZnO TFT an excellent alternative to reducing the touchscreen cost by utilizing cheaper materials, as long as the contact between the conductor and ZnO is Ohmic. Among other possible Ohmic contact materials are Ag [YWZ+13], Al/Au [KML+09], Al [BSG+12], AZO, and many other materials.



(a) As-deposited (b) Annealed 5min 250°C in N_2 gas

Figure 4.8: I_d-V_d measurement on ZnO TFT sample with Al contacts. After annealing, the contact deteriorates.

We have also studied the effect of various contact materials on the TFT performance. The three materials that we considered were aluminum, indium tin oxide (ITO), and aluminum-doped zinc oxide (AZO). Table 4.2 shows the film resistivity and contact resistance for the Al and ITO contacts to ZnO. The data was obtained using the standard TLM method of film patterning and extraction of resistivities from the I-V measurements.

Our experiments showed that aluminum is a good contact to ZnO, with contact

Table 4.2: Comparison of Al and ITO contacts to ZnO

Material	ZnO:N_2 film resistivity, Ω×m	Contact resistance, $\Omega \times cm^2$
Al	4.2×10^{-3}	1.0×10^{-1}
ITO	4.1×10^{-3}	1.8×10^{0}

resistance about 10x lower than that for ITO. However, we also found that aluminum contact strongly degrades when device is annealed in N_2 gas as shown in Figure 4.8. This data suggests that the use of Al contacts limits the maximum allowed processing temperature, and could prevent the successful fabrication of TFT with bottom contact. If the ZnO layer is to be grown at an elevated temperature, the contact would be annealed during the deposition and an Ohmic behavior will not be obtained. In addition, the high temperatures during the gate dielectric layer deposition would not be possible. Therefore, aluminum is not a suitable choice for the contact for this fabrication flow.

We also briefly considered the possibility of using the AZO contact materials. ZnO TFTs with AZO contacts have shown good transistor characteristics, but the observed currents were lower than those for ITO. It is possible that a few faults that were encountered during the fabrication of the AZO devices have limited the device performance. Further study is necessary to determine the viability of using AZO. The main benefit of using the AZO material is low cost. Future work can include further consideration of AZO as the Ohmic contact replacement in ZnO TFT.

4.5 Interface between ZnO and the dielectric

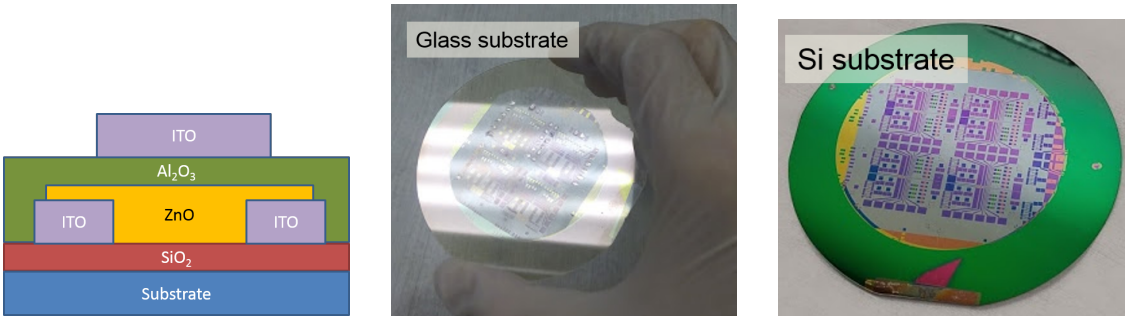
In a TFT structure, there are two channel interfaces present. One interface is between the substrate and the ZnO, and another is between the ZnO channel and the

above gate dielectric. Both of these interfaces play an important role in the device operation, and can be engineered to achieve the desired device performance. The function of the lower interface is to facilitate the growth of the polycrystalline ZnO film during sputtering. The influence of the substrate can be somewhat removed by including a seed layer in the fabrication flow. However, the influence of substrate must always be taken into account when the process is transferred onto a new target material. The upper interface can influence the channel mobility, since it the top gate architecture most of the current would be flowing close to that region. Throughout the experiments, we found that the ZnO films are very sensitive to ambient environment. Although multiple reports have been published where ZnO film is subjected to air, photoresist developer, water, and other chemicals, we have found that it is necessary to passivate the ZnO surface immediately after the film deposition in order to avoid the influence from external factors. If the film is left as is, the electrical measurement results will likely be inconsistent, or the device might show degradation over time. Our observations are consistent with the report on degradation of ZnO:N films by Bar et al [BAS$^+$09]. The TFT devices were passivated by growing a thin dielectric film on top of the ZnO layer immediately after the ZnO growth. The omission of this step could cause an unwanted reaction with ambient, which could modify the ZnO properties and potentially contribute to the surface trap states, creating a conductive layer at the top. Several materials can be used for this purpose. We have compared the passivation effects of sputtered silicon oxide (SiO_2) and ALD-grown aluminum oxide (Al_2O_3). Both films used were about 10 nm thick. We found that aluminum oxide film serves as the best passivation layer for zinc oxide, and results in a repeatable and reliable device measurements.

Chapter 5

Bottom- and top-gate ZnO:O_2 TFT pressure sensors

We have optimized the ZnO thin films by studying the effects of sputtering parameters on film morphology. We have investigated such parameters as the substrate deposition temperature, sputtering gas, and film thickness. We have also considered various contact materials. These optimizations were incorporated into the TFT device structure. We demonstrate in this chapter the improvement of device switching characteristics and pressure sensing performance by the integration of the optimizations into the process flow. We report the performance of top gate and bottom gate ZnO:O_2 TFTs on various substrates and the successful demonstration of 16x16 pressure sensor arrays.



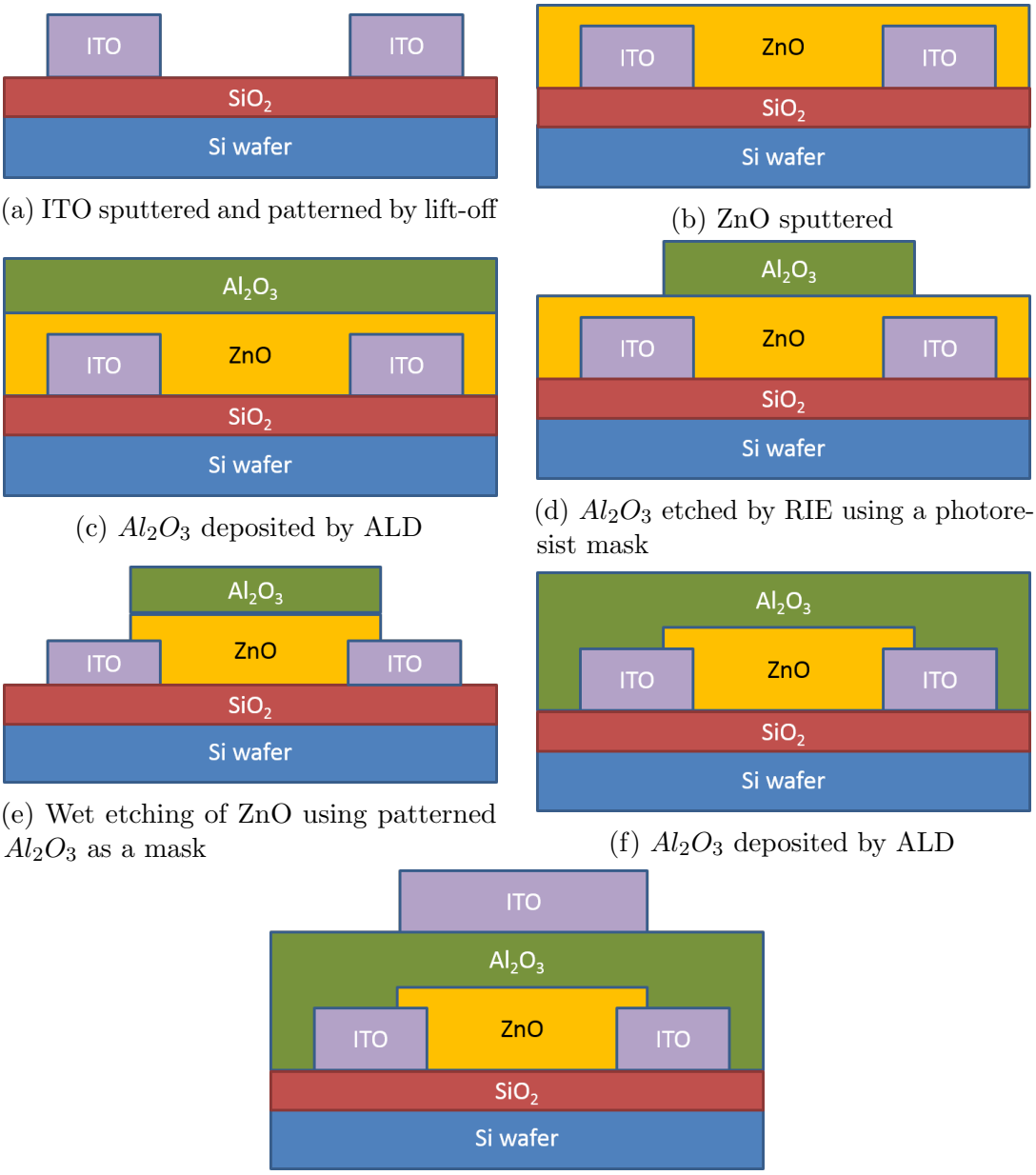
(a) Device structure (b) ZnO TFT on glass (c) ZnO TFT on Si wafer

Figure 5.1: Device structure and images of devices fabricated on glass and Si wafers with 3" diameter.

5.1 Device structure

The new TFT structure shown in Figure 5.1. Although initial devices were made on glass, these devices were also made on a silicon wafer in order to use the substrate as a bottom gate. In this structure, ITO contacts are patterned on thermally grown SiO_2 layer, and then the ZnO film is grown. Aluminum oxide is used as the gate dielectric, and the ITO gate is positioned on top of the channel. This structure allows the use of dual-gate geometry. The gate electrode can be either the Si wafer substrate, or the top ITO layer. Measuring each of the gates separately will allow us to characterize the film at different interfaces, one with silicon oxide, and one with aluminum oxide. Figure 5.1c shows a photograph of the device made on silicon substrate, and Figure 5.1b shows a photograph of the device fabricated on glass substrate.

The detailed device fabrication process is shown in Figure 5.2. First, ITO is sputtered and patterned via lift-off (Figure 5.2a). Next, the ZnO film is sputtered, followed by the deposition of Al_2O_3 by ALD. Next, the Al_2O_3 layer is etched by RIE, which creates a mask for etching ZnO. The ZnO is patterned by wet etching with the



(a) ITO sputtered and patterned by lift-off

(b) ZnO sputtered

(c) Al_2O_3 deposited by ALD

(d) Al_2O_3 etched by RIE using a photoresist mask

(e) Wet etching of ZnO using patterned Al_2O_3 as a mask

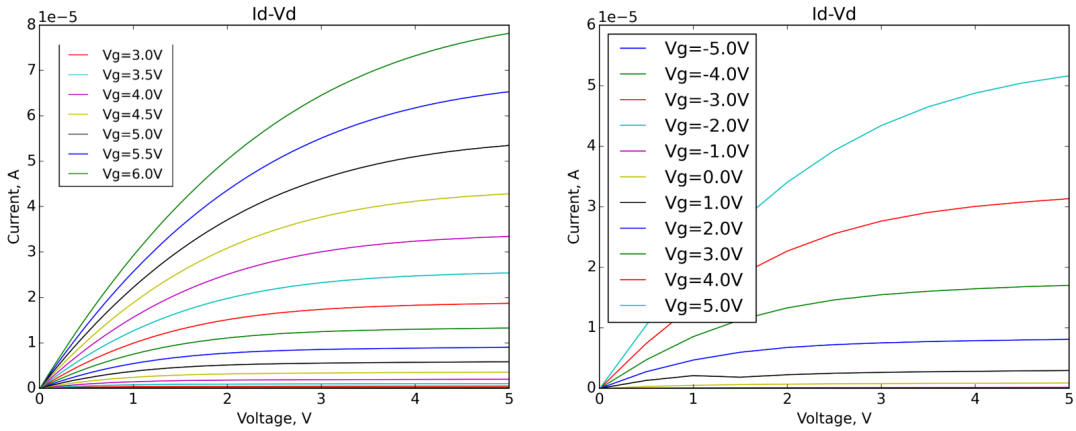
(f) Al_2O_3 deposited by ALD

(g) ITO sputtered and patterned by lift-off

Figure 5.2: Device fabrication flow for bottom- and top-gate ZnO TFT.

Al_2O_3 mask (Figure 5.2b), and then Al_2O_3 is grown again to isolate the ITO contacts from the top-most gate electrode ITO layer. Finally, the gate layer of sputtered ITO is deposited by lift-off.

5.2 FET characteristics



(a) Top gate (b) Bottom gate

Figure 5.3: I_d-V_d with top gate and bottom gate configurations for optimized ZnO:O_2 TFT device.

The FET measurements of the second generation thin film transistor pressure sensors are shown in Figure 5.3. The devices are fabricated on Si wafer. Two sets of I-V curves are possible, for those using the top ITO electrode as gate, and for the silicon wafer being used as the gate electrode. Both configurations show excellent transistor characteristics, with large on current of about 80 μA. The films are still n-type.

The ZnO:O_2 TFT devices have mobility of 2.7 $\frac{cm^2}{Vs}$, and an even higher mobility for the bottom gate configuration. The I_{max}/I_{min} ratio of the devices is now 10^4 to 10^5, with very low off currents achieved. Also, the new devices operate at +5V to -5V, compared to previous values of +15V to -15V.

5.3 Timing measurements

We now will investigate the timing measurements of the second-generation devices. The importance of timing can be highlighted by reviewing the process of touch handling on an Android system. A touch event is processed as follows. First, the user touches the touchscreen. Depending on where in the scan cycle the touchscreen currently is, it may take between 1 ms and 34 ms to process the touch by the touchscreen. In the absolute best scenario, the user presses onto the spot on a touchscreen that is the last to be measured during a frame, and the touch is certainly distinguished above noise. In the absolute worst case, the scan is currently at the beginning, and touch occurs in an area that has just been scanned. In addition, touch may not always be recognized on a first scan, and a second scan may be required to ensure that touch occurred. The scan rate numbers reported above are calculated assuming that the touchscreen is operating at 60 Hz refresh rate. Next, the signal must be processed by the host touch driver, which can add another 2-3 ms delay. After this point, the signal goes into the software, including the event management layer of the Android operating system, which will relay the touch event to the currently running application. Supposing that the only role of the application is to just draw a simple shape on the screen in response to touch, the application now needs to employ the graphics framework to generate the image in response to touch, and send the data to the host display driver. This can introduce another 50 ms of delay. Finally, the display operating at 60 Hz draws the image. The entire signal route from the moment of touch can take upwards of 100 ms. When a touchscreen is designed at the hardware level, the goal is to speed up the first two components of the event stack the touchscreen itself, and the touch host driver.

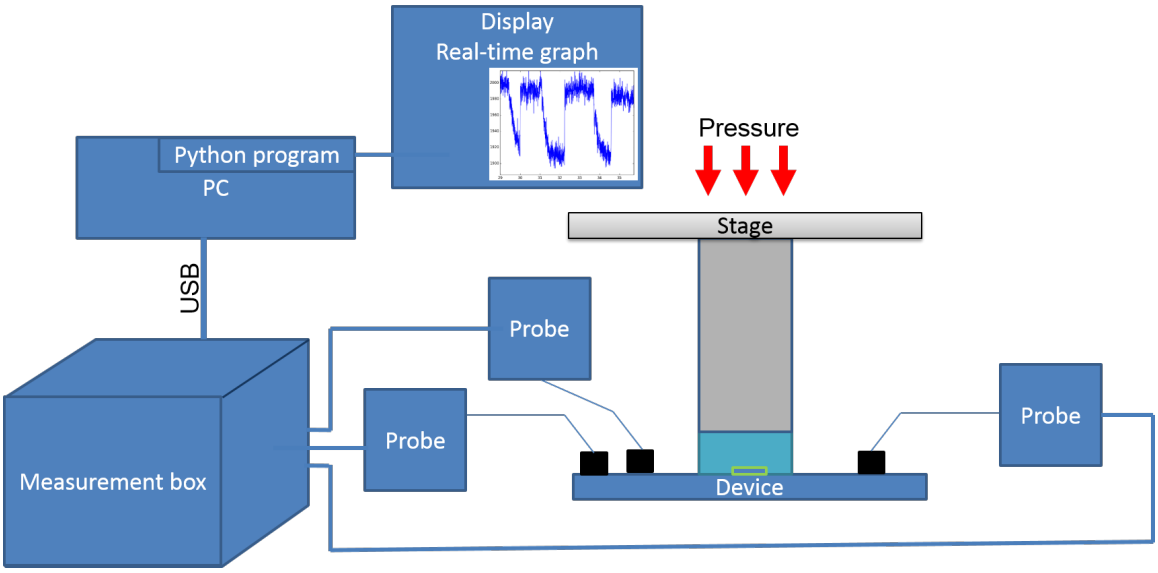


Figure 5.4: Measurement setup for single pressure sensor testing.

The measurement setup for the ZnO TFT pressure sensors is shown in Figure 5.4. In an analogy with the Android phone example, the stage is positioned on top of the pressure sensor. When pressure is applied, the sensor receives the touch information. The information is then processed by the measurement box, which is connected to a PC using the USB connection. The computer running a Python program receives the touch information, and creates a real-time graph of the applied pressure. The optical image of the initial part of the setup is shown in Figure 5.5. A square piece of plexiglass in positioned atop the pressure sensor to precisely define the area of applied pressure. The metal rod connects the plexiglass to the stage (not shown) where the pressure is applied. The example device in the image is a ZnO TFT pressure sensor fabricated on silicon wafer.

The timing characteristics of the bottom and top gate configurations are shown in Figure 5.6. The blue curve in the oscilloscope waveform in the image is the gate voltage. For the majority of time, gate voltage is low and the device is off. When the

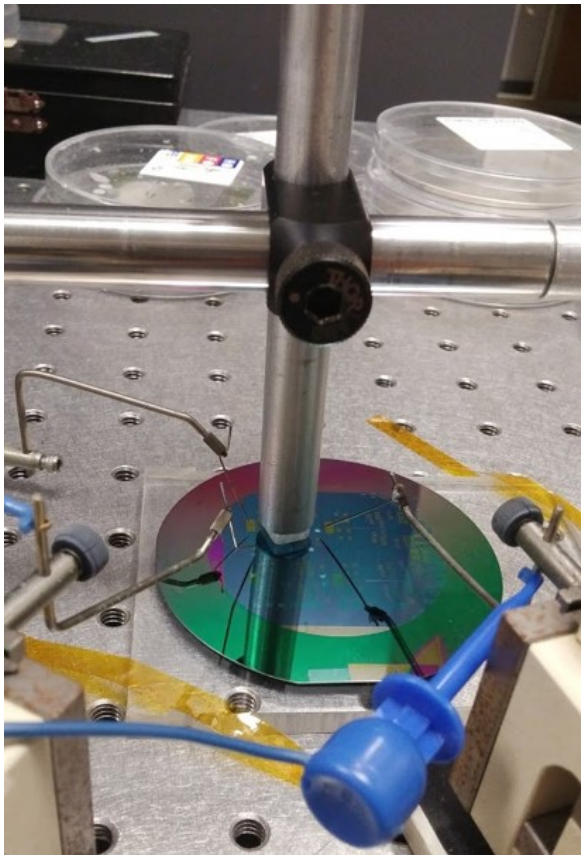
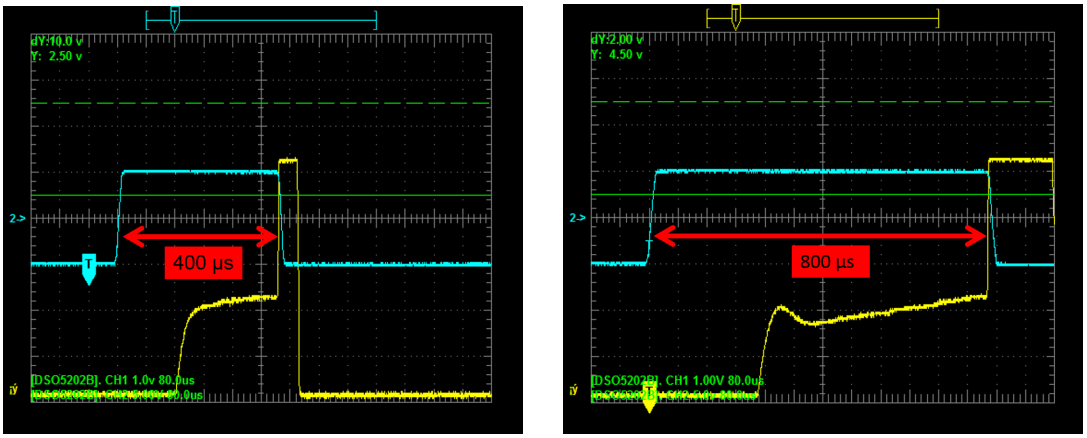


Figure 5.5: Photo of a pressure sensor under test. The sensor is connected by standard probe needles, and weight is applied through the metal rod positioned over the pressure sensor.

measurement starts, device is turned on by the rising gate voltage. The yellow curve is the drain current converted to a voltage via the transimpedance amplifier. It takes about 200 μs for the drain current to start rising. After 300 μs, the output reaches a stable value, and the ADC sampling takes place. When the ADC acquisition is completed, the gate voltage is set low and the current drops. The initial delay in the output is likely caused by the through-hole mount op-amp used for the measurement, together with a large capacitance present in the device. The ALD1722 operational amplifier has the open-loop voltage gain of 1000 at the frequency of 1 kHz. Such a low gain results in the lag that is observed in the oscilloscope. Still, this configuration



(a) Top gate (b) Bottom gate

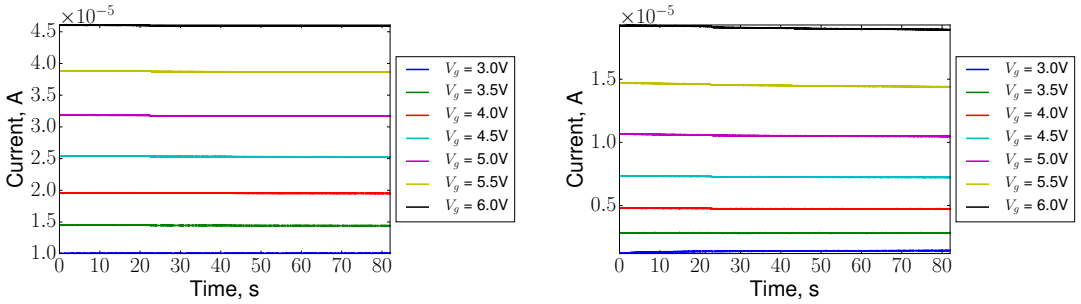
Figure 5.6: Measurement waveform for top gate and bottom gate device configurations. Bottom gate timing needed to be increased compared to top gate to achieve acceptable levels. This is likely due to a large capacitance created by the Si wafer.

allows us to achieve greater than 2 kHz sampling rate of the pressure signal. For the bottom gate device configuration, there is a larger delay in timing. The total measurement time must be now increased to 800 μs. The initial delay is longer, and the current does not rise as quickly. This is likely due to the fact that the bottom gate electrode is the Si wafer. In this case the additional capacitance caused by the large overlap of the Si wafer with the source and drain electrodes likely poses a problem for the op-amp in driving the load.

Another factor contributing to the op-amp response lag could be the gate-source or gate-drain capacitance. When the gate swings to high from the low state, it creates charge in the TFT gate capacitor, which then must be removed by the op-amp before the op-amp is able to settle at the correct value. The charge is removed by the op-amp through the large feedback 1 MΩ resistor, which means that the cancellation current has to be on the order of microamps. Therefore, if the gate capacitance associated with the TFT is roughly 1 nF, then it could take 0.5 ms to change the output voltage

by 1V.

The pulsed measurement setup was also modified to include a programmable voltage source, which allows the capture of the transfer curve using the pulsed conditions. Top gate and bottom gate transfer curves before and after pressure measurements were collected to ensure that applied pressure does not cause a degradation of the electrical properties of the device. The comparison of the collected data shows no significant variations in the device behavior caused by the previously applied pressure.

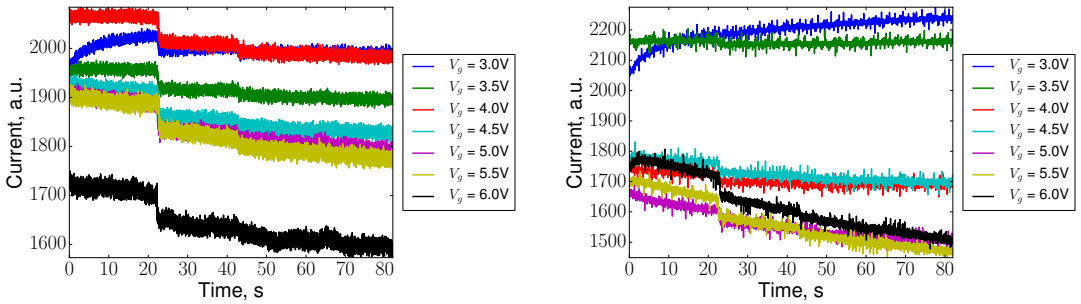


(a) Top gate (b) Bottom gate

Figure 5.7: Current as a function of time for top gate and bottom gate configurations at various gate voltage biases. Pressure is applied on top of the device. The change of current is small, and therefore, not easily distinguishable at this scale.

Similarly to the first generation of the TFT devices, current vs time curves were collected as pressure was applied to the device in both top and bottom gate configuration, as shown in Figure 5.7.

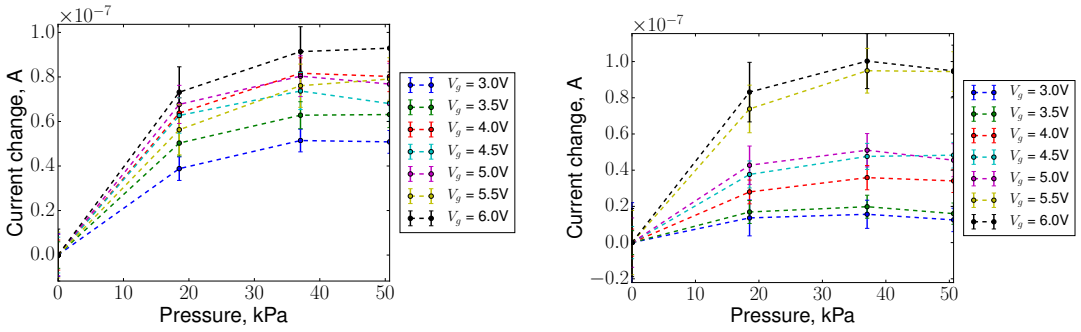
Figure 5.8 shows the curves shifted with respect to each other in order to present all of the curves in the same graph. Compared to the previously reported results of first-generation devices, the current drift is observed even in the pulsed mode. For some gate voltages, the drift is directed upwards, while for other gate voltages the drift is directed downwards. The drift is most likely caused by the heating of the sample, or by the mobile ions that are present in the device. Since the current levels are



(a) Top gate (b) Bottom gate

Figure 5.8: ADC values reported by the microcontroller. This is identical to the current-time plot, but each of the curves has a different DAC shift (not shown). This allows the comparison of multiple curves on the same graph window.

higher compared to the ZnO:N_2 TFTs, most likely a faster timing is required to obtain drift-free current characteristics. This phenomenon is also present in other TFTs. For example, Jiang et al [JRS+15] found that using a pulsed measurement with MoS_2 TFTs helps prevent Joule heating typically observed with DC bias measurements.

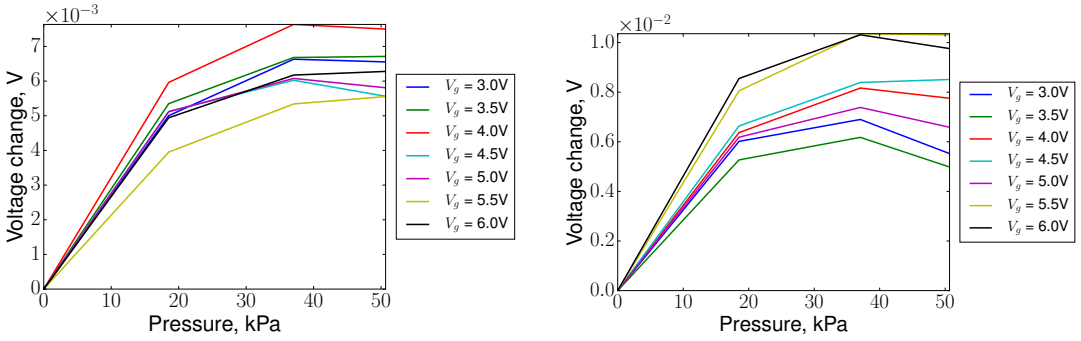


(a) Top gate (b) Bottom gate

Figure 5.9: Current change as a function of pressure. The ZnO film responds to applied pressure in a non-linear fashion.

To precisely measure the amount of current change as a function of pressure, the drift was accounted for by a linear approximation. The result is shown in Figure 5.9. For both configurations, a non-linear response of current due to applied pressure is observed. One of the future goals is to identifying the cause of this behavior, as

well as repeating the fabrication of these samples to confirm the reproducibility of these results.



(a) Top gate (b) Bottom gate

Figure 5.10: Equivalent gate voltage change due to pressure for top gate and bottom gate configurations.

The equivalent gate voltage due to pressure was extracted similarly to the previously described procedure, and the data is shown in Figure 5.10. The non-linearity in the measured current also translates to a non-linearity in the equivalent voltage. However, for the voltage, it must be noted that this data can be strongly affected by the current drift, since the values of the drain current may not correspond to those measured for the transfer curve.

Finally, the latency of a pressure sensor is a critical metric that could prevent otherwise strong technologies from practical utilization. Latency is the time delay between the event of physical application of force on top of sensor, and the registration of the touch event by the sensor itself. Latency cannot be measured without the knowledge of the actual time that an object exerted force to the sensor. We used a technique suggested by Cyril Lance to characterize the latency of the ZnO TFT pressure sensors.

Two voltage inputs channels were used simultaneously to record the output

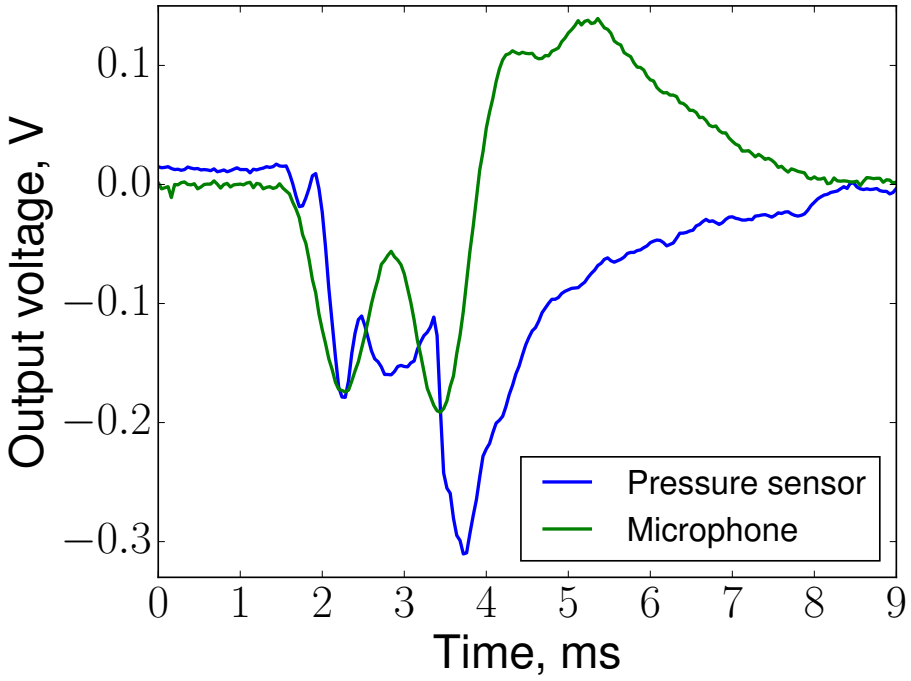


Figure 5.11: Latency characterization of ZnO TFT pressure sensor.

voltage produced by a studio microphone (channel 1), and the output of a current preamplifier (Ithaco 1211) connected to the ZnO TFT-PS. A stage is constantly pressing on the ZnO sensor. The microphone is used by manually hit the stage, thus providing a source of sudden impact to the transistor. The microphone produces an output voltage immediately upon impact, and can be considered the reference signal, indicating the time at which the ZnO sensor was hit. The resulting measurement is shown in Figure 5.11. It can be seen that the ZnO sensor responds to pressure within 1 ms of the actual impact. Therefore, we estimate that an upper bound of the ZnO TFT pressure sensor latency is 1 ms. This is considerably faster than other common pressure sensor devices, especially those involving moving parts.

A fast recovery time is also an important force sensor requirement. To test the device recovery time, current was measured as a function of time, as shown in Figure 5.12. During the measurement, stage was pressed with a finger for a short amount of

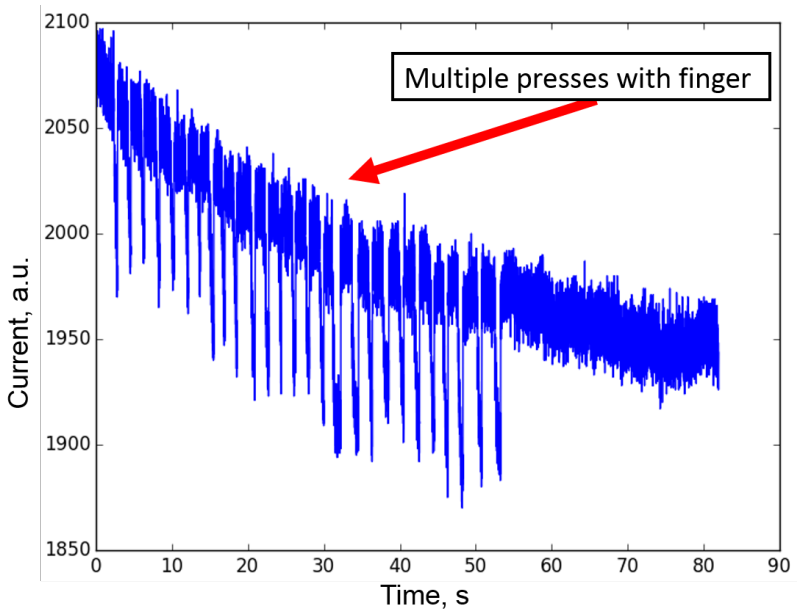
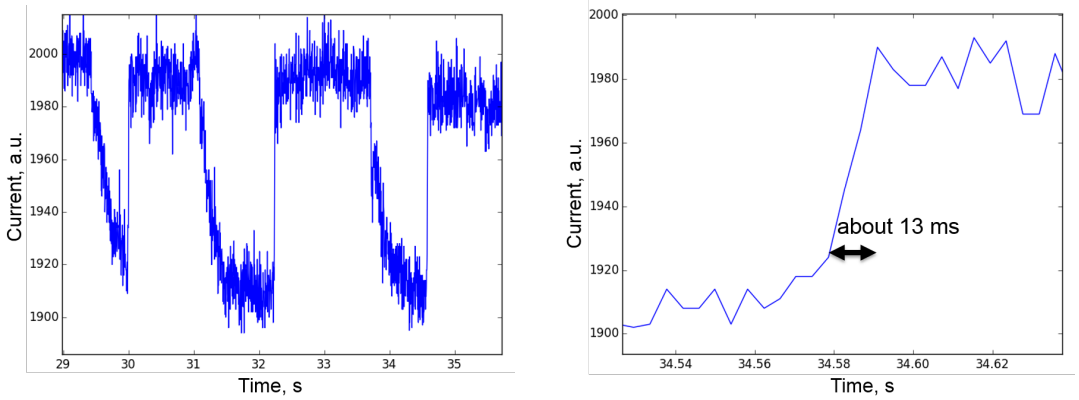


Figure 5.12: Estimation of recovery time for ZnO TFT pressure sensor.

time, and then finger was quickly released from the stage. The goal was to obtain the shortest possible time that it takes for the current to return to the original level after the finger is released. This technique does not allow the determination of the sensor delay due to changing pressure, but it does provide an upper bound on the recovery time of the device.



(a) Zoom 1 (b) Zoom 2

Figure 5.13: Zoom-in view of one of the variable pressure regions. The recovery time is less than 15 ms.

Multiple pressure pulses were examined. One of the shortest observed pulses took only 13 ms to return to the original baseline level, as seen in Figure 5.13. The actual device recovery time may be shorter, since the finger itself may not be able to remove the pressure infinitely fast.

5.4 16x16 array of pressure sensors

To demonstrate the improved scalability of the ZnO:O_2 TFT pressure sensors, we have developed a layout for a 16x16 array. The process also included a contact metallization step using Ti/Au materials to make Ohmic contact to ITO. The devices were then connected to a flexible circuit cable using anisotropic conductive film (ACF) bonding. Due to the remaining current drift of the ZnO TFT, and a high gain of the transimpedance amplifier (10^6), it is not sufficient to set a single DAC value for current canceling. The changing drain current would still cause an overload of the op-amp output due to the high gain. Therefore, a new circuit was designed to measure larger currents that is capable of real-time gain calibration. The schematic is shown in Figure 5.14. A new phase is now introduced into the measurement timing by the addition of the low-gain stage. The circuit operates as follows. First, the DAC output is disabled in order to route the entire transistor current through the amplifier feedback. Next the SPST switch SW1 is closed to select the low-gain mode. In this mode, the entire TFT current is measured under a low gain on the order of 10^4, and therefore the output is not overloaded at the op-amp rails. After the low-gain mode is selected, the ADC is used to measure the output voltage. This measurement value is now used to calculate the appropriate value for DAC output in order to cancel the TFT current. The DAC output is now set and enabled. Next, the switch SW1 is opened to select the high

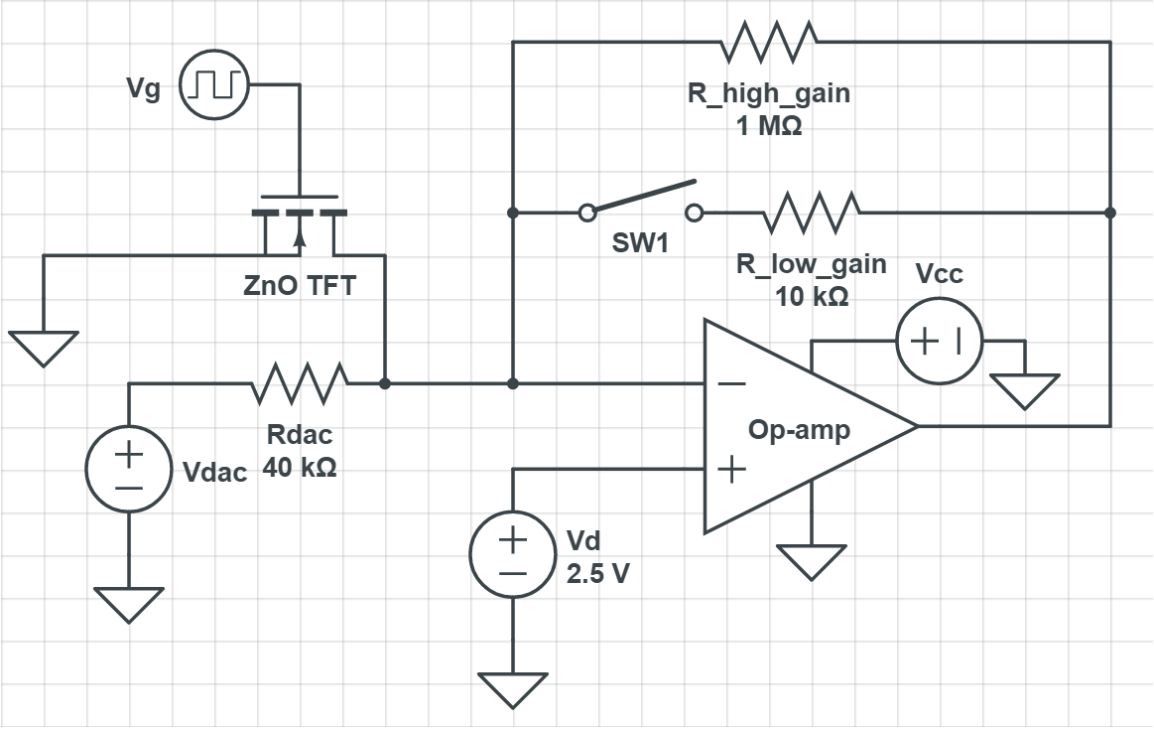
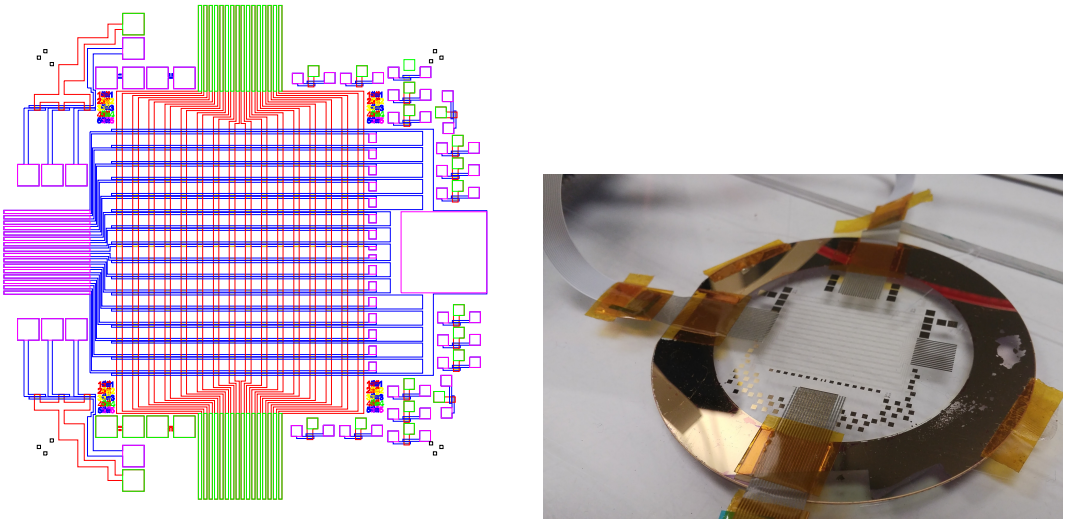


Figure 5.14: Transimpedance amplifier with variable gain.

gain mode. Since the most of the current is now subtracted, the high-gain mode is ensured to produce an output away from the op-amp rails.

The mask layout for the 16x16 array is shown in Figure 5.15a. Compared to the previous array, two additional masking layers have been added to this design. Previously, a direct connection to ITO using the spring-loaded Au-coated pins was utilized to make an electrical connection to the sample. This has caused difficulties in obtaining a good contact when the etching of dielectric over the ITO layer did not complete or created a film of residue on the surface. The new process allows the use of hydrofluoric acid (HF) or a BOE solution for etching the Al_2O_3 layer to create vias to the metal pads. We have not observed any degradation of the Ti/Au metal layer by the wet etching, and these materials were selected due to superior adhesion and conductive properties. Silver, which is the more common metal used to make contacts

in industry, would also be an acceptable material due to its resistance to HF solutions [LBBT12].



(a) Array layout (b) Array with attached ribbon cables

Figure 5.15: Layout (a) and optical image (b) of a 16x16 array of ZnO TFT pressure sensors.

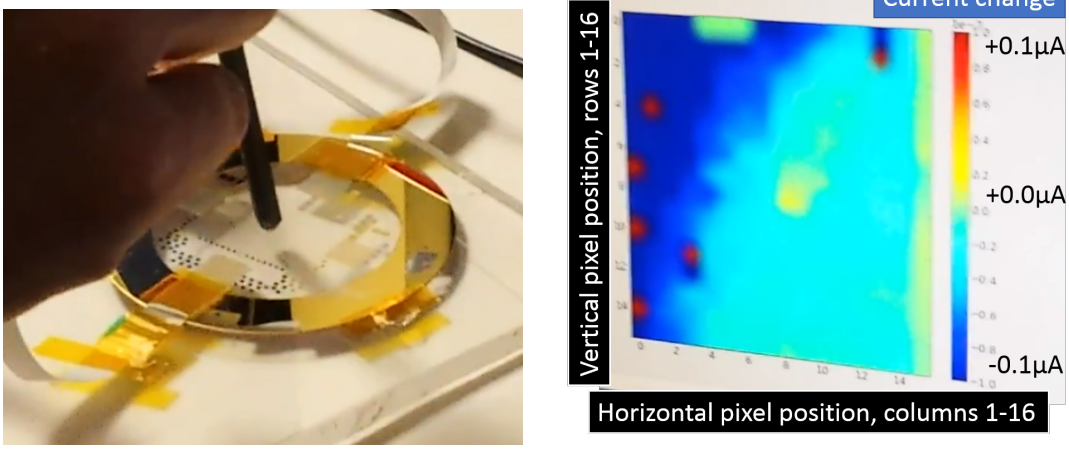
The contact metallization pads were positioned far from the active device area to ensure that any fabrication faults in these layers cannot affect the transistors, and would not result in shorts between the source/drain layers and the gate layer. The 0.5 mm pitch ACF bonding pattern with rectangular pads was selected as the connection of choice. A pattern with this pitch can be aligned visually without special equipment, and various PCB connectors for this size are easily obtained. The ACF bonding was done by hand by my colleague, Mehran Ganji, using a hotplate at 165°C and a glass-press method. The resulting device is shown in Figure 5.15. The flexible cables are 6" in length and accommodate 16 channels with a 0.5 mm pitch.

A snapshot of real-time device operation is shown in Figure 5.16. With the higher sensor density of 16x16, it is easier to localize the applied pressure, even though the current is being measured using a breadboard, which contributes to higher noise

and parasitic capacitances. We observed a difference in the current drift of pressure sensors between two different corners of the device area. This has also been confirmed by the FET measurements of single device patterns in the corners of the chip, which showed high variation of the maximum drain current at the same bias conditions. The variation is most likely caused by the non-uniform heating of the substrate during sputtering. One of our future goals is to identify the cause of non-uniform FET performance and eliminate it. Another interesting avenue of investigation is to test the effects of protective materials placed on top of the sensors. The majority of consumer electronics devices use cover glass, typically a chemically hardened glass with 0.7 mm thickness, to protect the display from scratches and impact. However, in the capacitive sensor approach, no contact is required, and the electric field extends through the glass, not affecting the sensitivity. In the pressure sensor scenario, the thick cover glass has the potential of spreading the force and therefore a reduced signal would reach the force sensor, and the registered pressure map would not have the same amount of localization as could be achieved if the sensors were pressed directly. The pressure effects could be simulated with mechanical modeling and compared to actual measured results. This would allow to account for the variation across the screen, where the pressure would be spread differently in the corners of the display compared to the center.

5.5 Summary

The key device performance parameters from each of the generations are summarized in Table 5.1. The 2nd generation devices have several advantages over the



(a) Insulating object pressing on the array in the center

(b) Color map of applied pressure on computer screen

Figure 5.16: Snapshot of real-time operation of 16x16 pressure sensor array.

Table 5.1: Comparison of key device characteristics between the first and second generation of ZnO TFT pressure sensors

Parameter	1st generation device ($ZnO:N_2$)	2nd generation device ($ZnO:O_2$)
Max process temperature, °C	350	200
Typical I_{max}/I_{min} ratio	100	10^4 - 10^5
Mobility, $\frac{cm^2}{Vs}$	0.7	2.7 (bottom gate: 16.5)
Operating voltage, V	-20...+20	-5...+5
Sensitivity, nA/kPa	1.5	4 (bottom gate: 4.5)
Sensitivity, mV/kPa	0.7	0.27 (bottom gate: 0.39)
Threshold voltage, V	1.37	0.34

first generation, including lower processing temperatures, better I_{max}/I_{min} ratio, higher channel mobility, lower operational voltages, and higher current sensitivity. However, the 2nd generation devices currently suffer from current drift and non-linear current response due to pressure. This issue still needs to be addressed in order to achieve an ideal pressure sensor. However, even in the current condition, the device can be used to cover a 5.5 screen with 2.3 mm spaced touch sensors and will be able to provide a 60 Hz refresh rate using a 64-channel ADC. We have developed and characterized

a new type of pressure sensor. The device was fabricated in the cleanroom, and we studied the physical characteristics of the pressure sensors. In many cases, custom measurement setups were necessary to obtain the desired data, since such devices have not yet been created to the best of our knowledge. The first generation TFT devices were using N_2 sputter gas for the ZnO deposition, showed linear pressure response, but had poor on-off ratio and channel mobility. The second-generation devices were deposited using O_2 gas, and displayed excellent switching characteristics, as well as high sensitivity to pressure. However, the non-linear pressure response still remains a challenge that should be solved with the proper film optimizations.

Chapter 6

Materials and methods

This chapter describes the semiconductor fabrication techniques that were used to fabricate the ZnO TFT pressure sensors. We start with the deposition methods, and describe the specifics of the sputtering process for the growth of zinc oxide and other conducting and insulating films used during the experiments. We also discuss the patterning and characterization methods utilized to debug and optimize the device performance.

6.1 Deposition processes

This section describes the thin-film deposition techniques used for fabricating various devices reported in this research.

6.1.1 Atomic layer deposition (ALD)

Atomic layer deposition is a technique that allows the growth of highly conformal films. A wide variety of dielectrics, semiconductors, and metals can be deposited by the

ALD process [JHB14]. ALD is mainly used to deposit dielectrics, such as aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), and titanium oxide (TiO_2), although it is possible to deposit semiconductors such as zinc oxide (ZnO). Recently, even methods of metal deposition, such as Ag [KNH$^+$11] and Pt [DRDC$^+$13] have been reported. A typical setup of an ALD machine is shown in Figure 6.1.

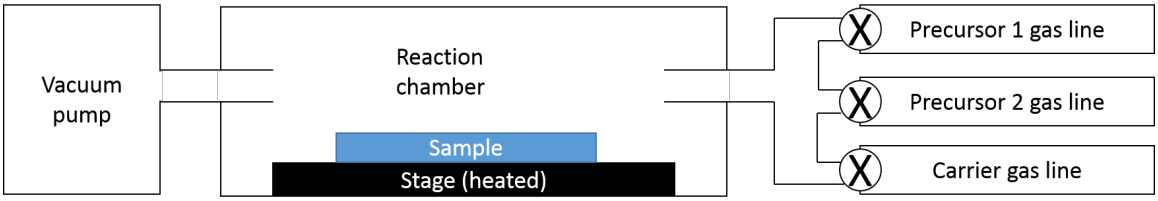
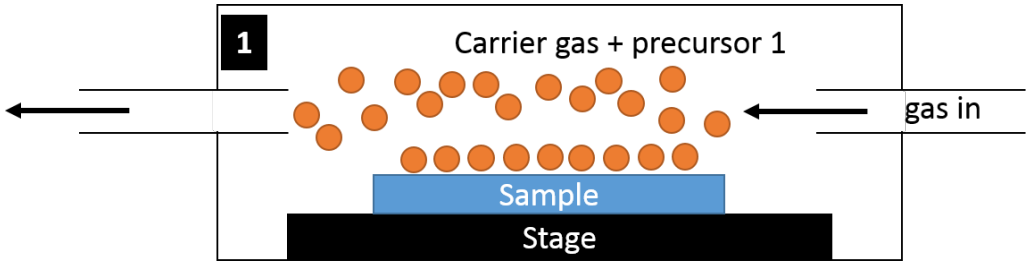
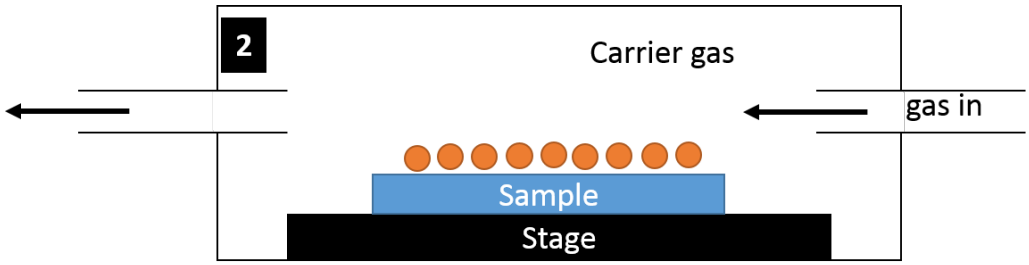


Figure 6.1: The schematic of a typical ALD machine.

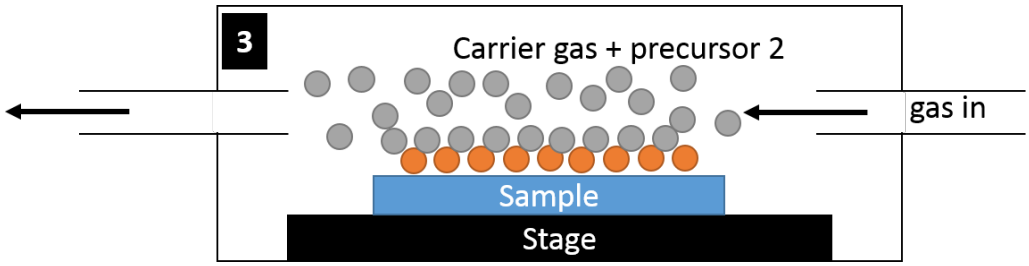
The deposition process is described in Figure 6.2. A carrier gas, which is typically Ar or N_2, is continuously flown through the reactor. To deposit the desired material, precursor 1 is added to the carrier gas flow. The precursor gas could be trimethylaluminum (TMA) for Al_2O_3 deposition, or hafnium tetrachloride ($HfCl_4$) for HfO_2 deposition. Next, the precursor flow is stopped, and the precursor is purged by the carrier gas. The only remaining precursor molecules in the reactor are stuck in a single molecule layer on the sample surfaces (and on any hard surface in the reactor). To cause the reaction to occur, second precursor, which is typically water for both aluminum oxide and hafnium oxide depositions, is introduced into the chamber. Next, the reaction between two precursors occurs on the surface of the sample. The process is conformal, so that the entire surface area of the sample is coated with the deposited material. Due to the introduction of the reaction gases sequentially, there is no reaction occurring in the middle of the chamber. The reaction only takes place on the hard surfaces inside the reaction chamber.



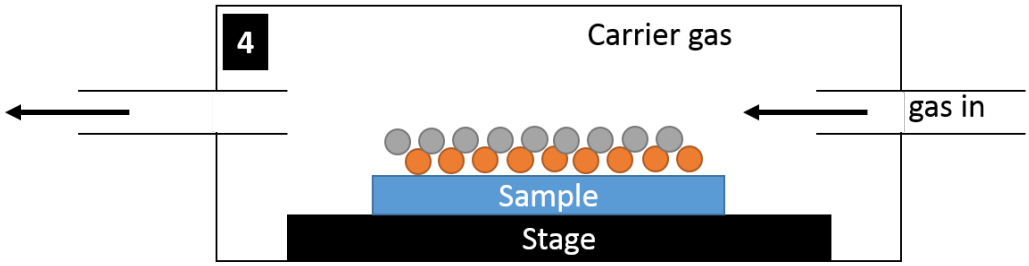
(a) First precursor is introduced into the chamber by mixing with the carrier gas.



(b) The flow of the first precursor is stopped, and only the carrier gas is flowing. At this point, the remaining precursor molecules are attached as a single layer on the surface of the rigid objects in the chamber, including the sample.



(c) A second precursor gas is introduced by mixing with the carrier gas.



(d) The second precursor gas flow is stopped, and the reaction between the precursor gases takes place. As a result, a single layer of the desired material is deposited conformally on the sample and the surrounding hard surface inside the chamber.

Figure 6.2: The atomic layer deposition process.

For the films grown by ALD in this work, we have used the Beneq TFS200, which had recipes developed for deposition of Al_2O_3, TiO_2, HfO_2, and ZnO. The Al_2O_3 film deposition conditions are as follows: thermal mode, 200°C, N_2 carrier gas. A typical Al_2O_3 film produced by ALD method has a dielectric constant of 10.3 [YSR13].

6.1.2 Sputtering

Sputtering is the process of physical bombardment of a solid target material with inert atoms. This results in removal of small particles or atoms from the target and the subsequent deposition of these atoms onto the substrate. RF sputtering is typically used to deposit dielectrics and semiconductors, since the ac signal prevents charge buildup on the target surfaces. Although RF process can also be used to deposit metals, conductive targets are typically deposited using DC sputtering due to lower process cost and simpler setup. In this work, majority of the materials were deposited by RF sputtering, so in this subsection, the RF machines will be described. A typical RF sputter-down machine configuration is shown in Figure 6.3. The sample is positioned on a rotating plate inside a vacuum chamber. The chamber is pumped to a base pressure prior to deposition. Next, a gas flow is introduced inside the chamber, and the vacuum pump is continuously pumping to maintain a fixed chamber pressure. The steady-state sputtering pressure can be varied by either changing the rate of the gas flow using the mass flow controller, or by introducing a variable valve next to the vacuum pump connection to the chamber. A target is positioned above (and sometimes, at an angle to) the substrate. The target is bonded on the back to a copper or elastomer bonding plate in order to achieve a good electrical connection to

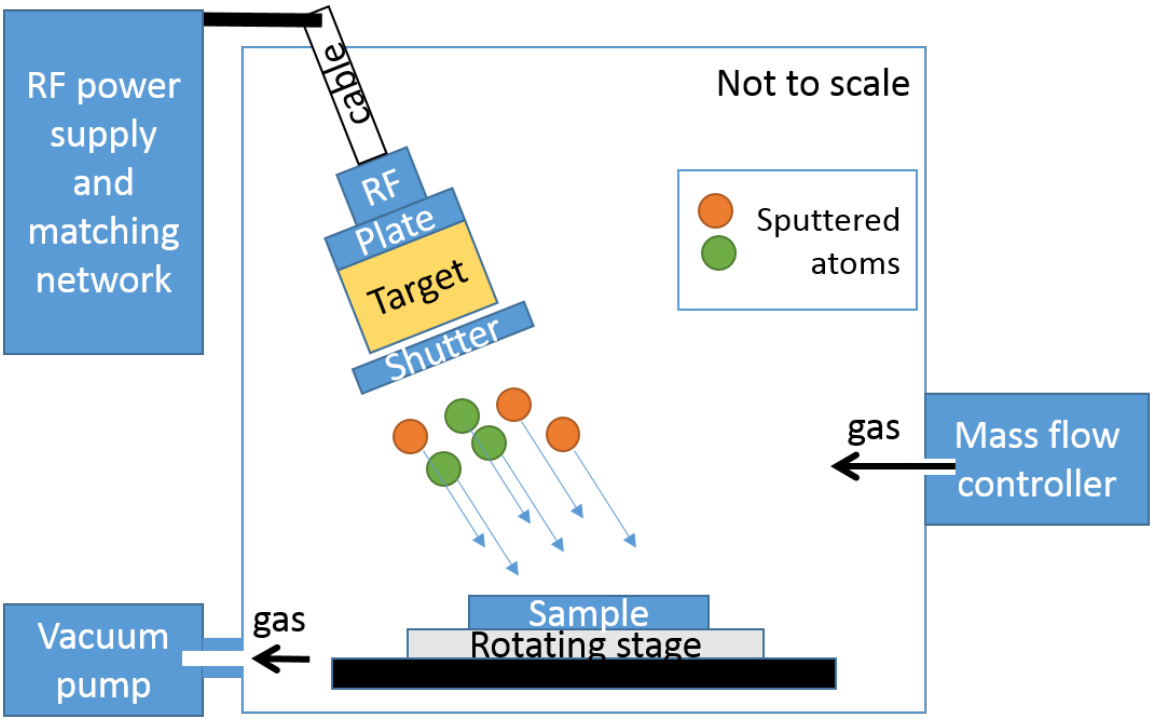


Figure 6.3: The schematic of a typical sputter-down deposition machine.

the high-voltage cable. The matched RF power supply delivers alternating potential to the target. The supply typically operates at 13.56 MHz [Lab13]. This has become the standard RF sputtering frequency due to the international spectrum licensing agreements, and less interference with signals at other frequencies. The alternating frequency applied to the target results in bombardment of the target with electrons and ions from the plasma, mostly due to the ionization of the sputtering gas. Due to the high signal frequency, the ions cannot respond and remain relatively stationary, while the electrons are able to move fast and end up bombarding the target, creating ionized particles. It is typical to also include a magnet behind the target in order to confine the plasma to the vicinity of the target. A standard procedure for igniting the plasma is as follows: vacuum pump is disconnected to allow a temporary increase of pressure inside the chamber; the power is applied to the target; at this point, plasma

should ignite; next, then vacuum pump is reconnected in order to achieve the desired working pressure. With the RF sputtering systems, there is a strong possibility of cracking of the target due to sudden application of power to the backing plate and the slow thermal response of the target material. Therefore, the initial power applied to target is usually small, 50W - 100W, and then gets gradually ramped up to the desired value. Likewise, a sudden drop in the chamber pressure may extinguish the plasma. Once the plasma is lit, chamber pressure is slowly ramped down to the desired deposition pressure.

Significance of sputtering parameters on film growth

Sputtering is a complicated process with a very large design space. Due to the practical impossibility of investigating every possible combination of deposition parameters, some researchers even refer to sputtering process as "dark magic" and recommend only slight modifications of the sputtering conditions once the desired film properties are achieved. A brief discussion of the most influential parameters is given here to provide a deeper understanding of the process.

Substrate temperature The substrate can be heated to various temperatures during the deposition. The temperature can range from room temperature to about 600 °C. Elevated substrate temperatures prohibit the use of photoresist in order to pattern the film during liftoff. For any experiments involving substrate temperature effects investigation, it means that the film can only be patterned by etching. This is an important process limitation that must be taken into account during experiment design.

Distance between substrate and target The distance between the sputtering target and the substrate (D_{TS}) significantly affects the deposition process. As the distance increases, the deposition rate decreases [JB04] and the uniformity increases. Larger distance also means that electrons arrive at the surface with smaller energy, thus influencing the film growth dynamics at the surface. For example, [HHAC09] reported that for Al-Zr doped ZnO films, distance between substrate and target affects both electrical and optical properties, including film crystallinity, resistivity, and transmittance. Initial decrease of substrate-to-target distance first results in improved transmittance and decreased electrical resistivity, while further decrease again deteriorates film properties. Williams et al [WFA$^+$13] investigated the influence of substrate bias and the distance from substrate to target on the polarity of the ZnO films. They found that at a larger distance between substrate and target, the substrate bias did not have an influence on the film polarity. However, at a shorter distance, they have been able to successfully control the polarity of the films. Although the exact mechanism of the polarity control is not clear, the electric potentials inside the sputtering chamber might be different at various substrate-to-targets distances. After reviewing the reports on the influence of the distance between substrate and target, the following conclusions and recommendations can be made for the development of a new sputtering process. This parameter appears to have many effects on the deposited films and it may not be possible to predict the resulting film properties, so it is best to avoid this variation. First, the minimum distance between substrate and target that still allows the desired deposition uniformity over the required sample size should be chosen. Next, the sputtering process should be optimized by varying the other sputter parameters. Finally, the substrate-to-target distance can be adjusted

(gradually increased) in order to fine-tune the desired effects. In some sputtering machines, the D_{TS} is fixed altogether, and no variation is allowed.

Base pressure A critical parameter for the deposition of semiconducting thin films using sputtering is the base pressure. The base pressure is the vacuum level inside the chamber that is achieved prior to the introduction of the sputtering gas inside the chamber. For semiconducting films, doping has dramatic effects on the film resistivity. For example, the introduction of 1 dopant atom in every 10^8 semiconductor atoms can have a drastic effect on film resistivity in silicon. The base pressure can be considered as an indication of the "impurity" of the sputtered film. For compound semiconductors like zinc oxide, the introduction of the impurities can result in either defects or a change of electrical conductivity. It is typical to expect the sputtered ZnO films to contain a certain level of impurities. However, if there exists a run-to-run variation in the base pressure, then this parameter alone can contribute to vastly different device performance between the batches of samples.

Sputtering gas Sputtering gas acts as a source of atoms that are used to bombard the target. This action creates a plasma that ejects atoms from the surface of the target. To avoid the reaction between sputtering gas and target material, it is common to use inert gases for sputtering that do not participate in the film growth, such as argon and xenon. Besides physical sputtering, gas can also play a role in the film growth itself. This process is called reactive sputtering. In that case, the gas is allowed to react with the target material and can be incorporated into the lattice of the grown film. For example, zinc oxide thin films can be sputter deposited using at least three distinct approaches:

1. RF sputtering from a ZnO target with an inert sputtering gas
2. RF sputtering from a ZnO target in an atmosphere consisting of an inert gas mixed with a chemically active gas, most typically oxygen.
3. DC sputtering from a pure Zn target in an oxygen sputtering gas.

Although ZnO TFTs prepared by sputtering ZnO in a pure Ar environment have been reported [Nan13], it is more common to introduce additional gases, especially oxygen, during sputtering in order to improve the film quality. The ZnO films deposited in a pure inert atmosphere from a ZnO target are typically very conductive. Historically, it has been widely believed that this was caused by the oxygen vacancies in the deposited film [JdW09]. However, it has since been shown that oxygen vacancies in ZnO are in fact deep donors and cannot contribute significantly to the n-type conduction observed in the deposited films. The conduction is most likely caused by the incorporation of hydrogen into the ZnO lattice, which acts as a shallow dopant. Even with a low base pressure, it is difficult to remove the hydrogen contaminants from the sputtering chamber. As a result, ZnO films are typically deposited by RF sputtering using a mixed inert gas and oxygen environment. The added oxygen may or may not influence the oxygen vacancy concentration. However, it makes it less likely for the hydrogen and other impurities to get absorbed into the lattice, thus decreasing the concentration of unintentional dopants.

Sputtering pressure Sputtering pressure is the gas pressure inside the chamber during the sputtering process. Sputtering pressure can be as low as 0.1 mT [Mus98], and can go as high as 100 mT [NMK$^+$99]. The typical range of RF sputtering pressure is between 2 mT and 10 mT. Increasing the sputtering pressure generally tends to

increase the deposition rate [PH72] for RF sputtering.

RF power As a general rule, increasing the RF power during deposition results in the increase of film growth rate. However, this parameter also influences electrical properties of the deposited films. For example, Fortunato et al have varied the RF power for deposition of ZnO thin films from 50W to 175W, and showed that the film resistivity peaks at about 100W [FPP+04]. Ismail and Abdullah [IA13] studied the XRD spectra of RF sputtered ZnO, and found that the strongest c-axis peak is obtained at 175W, and the lowest FWHM value is achieved at a power of 200W. They also reported a decrease in the optical bandgap with increasing RF power. Han et al [HWZ+11] found that at the power of 100W, the highest mobility of ZnO is achieved for their setup at 34 $\frac{cm^2}{Vs}$.

Zinc oxide thin film sputtering

Zinc oxide thin film deposition can be qualitatively divided into three stages: seed stage, transition stage,and the steady-state stage. This is illustrated in Figure 5 of [RdSA+12]. When the film first starts growing on a bare substrate, there are no zinc atoms present on the surface. Under the specified deposition conditions, film with thickness of 9 nm possesses little crystal structure. Next stage in the film growth is the establishment of crystal structure. The atoms that are arriving on the substrate encounter existing zinc and oxygen atoms already on the surface. Small crystals start to form at each site where originally just a zinc or oxygen atom is present. As the deposition continues, the crystals grow larger and merge, thus creating a polycrystalline thin film. The same reference [RdSA+12] shows that for films between 42 nm thick and 103 nm thick, the c-axis XRD peak is starting to become noticeable.

Finally, as the growth continues, the newly arriving atoms adhere to the established underlying crystal structure of the film, and therefore crystal quality is improving more slowly. Thicker films typically have better crystallinity than thinner films, since as the film grows, the new layers can use the underlying layers at the template for lattice growth.

Substrate temperature effect on the crystallinity of ZnO thin films Substrate temperature during sputtering has a significant effect on the thin film properties and the crystal structure. In general, higher substrate temperature results in a slower growth rate, but may help obtain higher-quality films. This parameter is discussed at length in Section 4.2.

Substrate material effect on the ZnO TFT performance Substrate material also affects the ZnO film growth, and, as a result, the ZnO TFT. This is especially important in the bottom gate devices, where the substrate must be a dielectric that can be deposited, as opposed to top gate devices, where a simple glass wafer can be used as the base layer for ZnO growth. It is not possible to provide a set of materials that would serve as a good substrate for ZnO growth, since this depends on the particular sputtering machine setup, and the device fabrication process. For example, Nishii [NHT+03] has shown that the silicon nitride substrate does not result in good TFT performance when ZnO is deposited by the pulsed laser deposition (PLD) method. On the other hand, Remashan et al. [RCPJ10] have demonstrated high-performance ZnO TFTs on silicon nitride substrates for ZnO film deposited by the metal-organic chemical vapor deposition (MOCVD) method.

In this work, two types of substrates have been used - PECVD SiN_x and

silicon oxide. The silicon oxide substrates have shown more consistent results, so most of the work has been focused on this material. For the silicon oxide substrates, both thermally-grown SiO_2 on Si and fused silica wafers have been used with similar success. We have not noticed a significant difference between glass and thermally grown SiO_2. If the difference exists, it was likely reduced by the use of the seed layer for the ZnO thin film depositions.

Indium tin oxide film sputtering

ITO films were deposited by sputtering from an ITO target, under the following conditions: power of 300W, Ar flow of 50 sccm, chamber pressure at 4.8 mT. The primary goal of this work was to demonstrate the concept of pressure sensing using the new device structure. As a result, the ITO films have not been optimized to achieve the maximum possible transmissivity and conductivity. However, we observed that as-sputtered ITO films (room temperature) can be annealed on a hot plate at 350 °C for 1 min to achieve greatly improved optical and electrical film properties. Typical conductivity of commercially available ITO films is on the order of 1×10^{-4} Ωcm [Min05].

Aluminum-doped zinc oxide sputtering

AZO films were deposited from an Al-doped (2%) ZnO target, at the power of 200W. The gas flow was Ar with the rate of 32 sccm, resulting in chamber pressure of around 2.0 mT. Deposition rate was determined to be about 8 nm per minute. Aluminum-doped zinc oxide is a transparent conductor, and has been frequency proposed as one of the possible replacements for ITO. The main advantage is cost:

the ITO sputtering targets can cost 3-6 times higher than AZO sputtering targets.

6.2 Film patterning

6.2.1 Photolithography

Photolithography is the standard micropatterning process utilized for device fabrication. In this work, both negative resists and positive resists have been used to pattern the devices.

Negative photoresist

Negative photoresist is hardened by the UV radiation. The exposed areas of the photoresist remain, and the unexposed get washed away by the developer solution. NR9-1500PY photoresist was used as the negative photoresist in this work.

NR9 1500PY negative photoresist recipe for Si substrate

1. Spin-coating at 4000 rpm for 40 s, with ACL (acceleration)=33
2. Pre-bake on hotplate at 150°C for 1 min
3. Exposure for 8.6 s using MA6 mask aligner with 11 $\frac{mW}{cm^2}$
4. Post-bake on hotplate at 100°C for 1 min
5. Develop in RD6 for 13s, no agitation
6. DI water rinse and drying

7. If the resist is to be used for lift-off process, the samples need to be baked again just prior to deposition at $100°C$ for 1 min. This drives out the moisture from the resist and facilitates the lift-off process.

The function of the second baking step (post-bake) is to cross-link the exposed areas. If this step is omitted, the entire film will be developed away (both exposed and unexposed).

Positive photoresist

Positive photoresist becomes soluble in developer upon exposure to UV radiation. The exposed areas get washed away by the developing solution, while the blocked off areas remain. The AZ 1518 photoresist was used as the positive photoresist in this work.

AZ 1518 positive photoresist recipe for Si substrate

1. Spin-coating at 4000 rpm for 40 s, with ACL (acceleration)=33
2. Pre-bake on hotplate at $115°C$ for 1 min
3. Exposure for 9 s using MA6 mask aligner with 11 $\frac{mW}{cm^2}$
4. Develop in AZ 300 for 25 s, with agitation
5. DI water rinse and drying

Note that there is no post-baking step for the positive photoresist, as compared to the negative photoresist.

An interesting method of using positive photoresist is reported by Mourey [MZJ10]. They report a "Self-Aligned-Gate" method of fabricating the TFT. In their

work, the ZnO TFT has a bottom gate structure. After the ZnO film deposition, the positive photoresist is applied on top. Next, the film is exposed from the back of the substrate. The gate electrode acts as the photolithography mask, blocking the UV light from exposing the areas directly aligned with the electrode. Note that even if gate is made of AZO and ITO, this method could still work, provided that the gate material has sufficiently high absorption in the spectrum of the exposure light. Although this method can be used to isolate the devices, the resulting structure will still suffer from the widened channel, since there will be zinc oxide film underneath all areas that are covered by the gate electrode. That means that the layout of the chip will be more vulnerable to process variations, depending on how far does the current spread away from the source and drain contacts.

Lift-off patterning

A typical patterning technique used in this work was lift-off. The liftoff process can be used to create patterns on a wide variety of films, including metals, semiconductors, and dielectric. Liftoff is explained visually in Figure 6.4. As a rule of thumb, the thickness of photoresist for successful lift-off must be at least three times larger than the desired film thickness of the deposited material. First, the photoresist is spin-coated, exposed, and develop to create the negative of the desired pattern on the substrate. Next, the thin film of interest is deposited. After deposition, the device is submerged in acetone, and is often left overnight. It can also be helpful to lightly scratch the edge of the continuous photoresist pattern in order to facilitate the penetration of acetone underneath the deposited film.

After the device is allowed to soak, it is rinsed under acetone flow to remove

the unwanted film. Next, the device is placed into a new acetone bath, and sonicated in order to clean any remaining photoresist residue. When the process is finished, the desired pattern will remain on the sample.

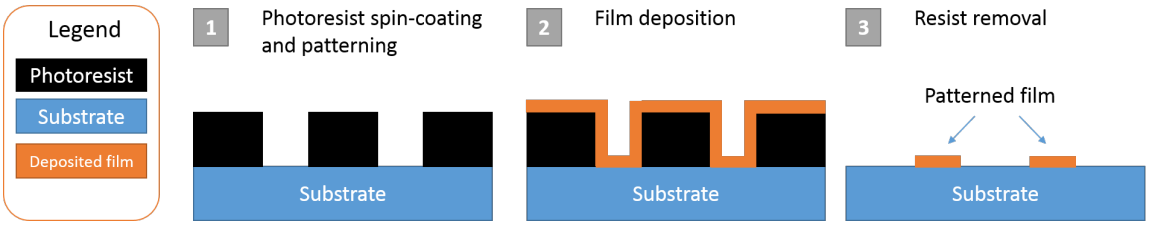


Figure 6.4: Simplified diagram of lift-off patterning process.

One of the limitations of the liftoff process is the film deposition temperature. Because the maximum temperature that the resist can tolerate is on the order of 150°C, substrate cannot be heated above that temperature during deposition. In fact, during electron beam deposition, evaporated material often heats the resist to the point that it degrades, and becomes insoluble. This prevents successful liftoff of the unwanted areas of the deposited film.

Patterning of conformal films presents another problem for lift-off photolithography. A conformal deposition process results in the film growth on the sidewalls of the patterned photoresist. During liftoff, this sidewall growth may not be properly inhibited, and can cause electrical shorts between the current and the subsequent layers [Nat15]. Sputtering is an example of a conformal coating that may cause such problems. Typically, sputtering targets are off-center relative to the stage, and the stage rotates. Such configuration allows a straight path of the deposited ions from the target onto the sidewalls of the patterned resist. To alleviate this problem, a modified photolithography technique has been proposed and patented. To break the film continuity during deposition, an additional film is introduced to complement the

top photoresist. The lower film (which could be another photoresist with a higher development rate, or a native or thin grown oxide) is etched deeper than the top layer, resulting in an isolated island of deposited material in the opened areas of the desired pattern [LQL+98]. The resulting film is not continuous, and smooth patterns with a low degree of roughness can be achieved.

6.2.2 Etching

Etching is a standard microfabrication technique that involves removing the unwanted areas of a deposited material, typically used in combination of a photoresist mask. Dry etching uses plasma to etch the sample, while wet etching is a reaction between the deposited film and a solution.

Dry etching

Reactive ion etching (RIE) is a common etching technique. It is also referred to as "dry etching". The tool used in these experiments was Oxford Plasmalab 80 RIE. Etching process is similar to the sputtering process. Sample to be etched is placed into a vacuum chamber and gets pumped to a base pressure of around 10^{-6} - 10^{-5} Torr. Next, an etching gas is introduced and plasma is lit above the sample. The gas inside the chamber becomes ionized and turns into a mix of radicals, free electrons, and neutral atoms. Radicals (for example, the fluorine ion F^-) react with the material from the sample and form volatile compounds. These compounds then get pumped out of the chamber by the vacuum pump, resulting in the removal of material from the substrate. RIE typically produces vertical etching profiles, due to the mostly vertical motion of radicals from the top of the chamber to the sample. The

main advantage of RIE is the precisely controlled etching rates, the ease of adjusting etching recipes, and the availability of a vast variety of etching chemistries. The major disadvantage of the RIE is the high cost associated with both the equipment setup and the machine operation, and the time associated with bringing the sample under vacuum.

Wet etching

Wet etching is a method of removal of material from the sample using a reactive solution. Wet etching is the cheapest and simplest method of patterning a film. The sample is submerged into a solution. The solution reacts with the material from the sample, forming a soluble compound. The etching process is typically isotropic, and the etching time can be adjusted in order to get the etch to the desired depth. It is also possible to intentionally overetch the film to obtain the chamfer shape of the edges in order to prevent shorts between two conductive layers separated by dielectric.

ZnO film etching Zinc oxide can be wet etched in either acidic or basic environments. Because the film is highly sensitive, it is important to use a low concentration of the etching agent. For this work, hydrochloric acid was used to pattern the ZnO films. The recipe that was used is shown in Table 6.1. Etching rate will be highly

Table 6.1: Wet etching of ZnO using dilute hydrochloric acid

HCl amount, ml	H_2O amount, ml	Etch rate, $\frac{nm}{s}$
1	1000	≈ 6

dependent on the method of manufacturing of ZnO film.

ITO wet etching ITO film can also be patterned by wet etching using HCl solution. In comparison to ZnO, however, the concentration needs to be higher to obtain a practical etching rate. As-sputtered ITO films can be readily etched in a 1 HCl : 9 H_2O solution. The resulting etch rate is approximately 110 nm for 1.5 min. It is important to etch the ITO film prior to the annealing, because the annealed ITO film requires a significantly higher concentration of HCl in order to obtain an acceptable etch rate.

6.2.3 Shadow mask

Shadow masks can also be used to pattern films if deposition methods like sputtering or e-beam evaporation are used. Although shadow mask has not been used in this research, it is an important technique that must be mentioned, as it provides significant potential cost-savings over photolithography. Chiang et al [CWH$^+$05] have used shadow mask to fabricate zinc-tin oxide thin film transistors. They were using channel dimensions of W/L=7100 μm/1500 μm, and have achieved mobilities in excess of 20 $\frac{cm^2}{Vs}$.

6.3 Characterization techniques

6.3.1 X-ray diffraction (XRD)

X-ray diffraction is a standard characterization technique used to detect the crystal structure of a material. This method was used to characterize the crystallinity of the sputtered ZnO thin films. Once the peak corresponding to a crystal plane of interest is identified, the crystallite size can be estimated by the Scherrer formula

[Cul78]:

$$D = \frac{K\lambda}{\beta cos\theta}\,, \tag{6.1}$$

where K is the shape factor for an average crystallite (around 0.91 for ZnO) [DFL$^+$07], λ is the wavelength of the X-ray source, β is the full-width at half-maximum in radians, and θ is the angle at which the diffraction peak is observed. For our XRD measurements, the wavelength of Cu K_α peak was used, which is 0.15418 nm.

The lattice constant c can be determined from the XRD measurements using Bragg's Law [FH13]:

$$n\lambda = 2d\sin\theta \tag{6.2}$$

$$d = \frac{n\lambda}{2\sin\theta} \tag{6.3}$$

For the (002) plane of ZnO, the lattice constant c therefore can be calculated according to:

$$c = \frac{nl\lambda}{2\sin\theta} = \frac{n\lambda}{\sin\theta} \tag{6.4}$$

The distance between the planes can be found using the equation 6.5 [LGR$^+$11] [OH96].

$$d = \frac{1}{\sqrt{\frac{4}{3a^2}(h^2+hk+k^2)+\frac{l^2}{c^2}}} \tag{6.5}$$

For a plane perpendicular to the c axis, $h = k = 0$ and $d = \frac{c}{l}$. Also, $l = odd$ is forbidden, therefore $l = 2$. Then the plane index is (0, 0, 2), and $d = \frac{c}{l} = \frac{c}{2}$.

6.3.2 Imaging

The standard SEM and TEM high-resolution microscopes were used to characterize the ZnO films. Sample preparation, where needed, included wafer cutting, thin

metal layer deposition, bonding to conductive tape, and focused ion beam milling.

The SEM images were obtained using FEI XL30 scanning electron microscope with the FEI Sirion column, which enables very high resolution imaging at low KV. Ultra-high resolution is possible using UHR mode and the Through Lens Detector. The TEM images were obtained be the Tecnai F30 transmission electron microscope.

6.4 Thermal oxidation of Si wafers

Dry thermal oxidation was used to grow an insulating SiO_2 layer for the device fabrication. Silicon (100) wafers were purchased from El-Cat (manufactured by "Prolog Semicor", Kiev, Ukraine), with p-type (boron) doping, resistivity between 0.001 - 0.005 $\frac{\Omega}{cm}$, and thickness of 380 $\pm$ 25 μm.

Thermally grown silicon oxide on highly doped Si wafers also served as the gate dielectric layer for ZnO TFTs fabricated on Si substrates. The necessary growth time can be calculated using a convenient online tool at http://www.cleanroom.byu.edu/OxideTimeCalc.phtml. The growth parameters were: temperature - 1000 °C, O_2 gas flow - 10 sccm, desired thickness - 100 nm, time - 3 hours and 13 minutes. Front and back dummy wafers were placed on the oxidation boat to ensure the oxide growth uniformity for the samples of interest.

Chapter 7

Future work

Plenty of research remains to be completed on the zinc oxide transistor pressure sensors prior to successful commercialization. A lot of desired experiments require systematic brute-force study approaches for successful completion. The results are likely to be highly machine-dependent, and therefore optimization might best be done directly on the commercial equipment if these devices are of deeper interest. There are several major areas of interest:

7.1 Optical properties

Transmittance improvement is a key study that needs to be completed for a successful touchscreen application of the ZnO TFT-PS. This includes the improvement of individual device layers, such as ZnO, ITO, AZO, gate dielectric, and any additional protective coatings, as well as the optimization of the relative film thicknesses to minimize the reflective index mismatch-induced scattering. It is important to remember that the device itself is small, and so not all areas will have the same material stack.

For example, the dielectric material may coat the entire substrate, while the ZnO will only be located in isolated channels, potentially as small as 5 μm x 5 μm. Thus, improvement of the ZnO-dielectric stack might not result in the best optical performance in the majority of the substrate. On the other hand, depending on the commercial application of the devices, it might not even be necessary to work on the optical properties. If the dimensions are made sufficiently small, it might be possible to develop an in-cell architecture, by integrating the ZnO TFT into the backplane of the active matrix of the display, or, alternatively, aligning the ZnO TFT directly above the blackmatrix layers. Still, it has been shown that optical properties are highly related to the electrical properties, so the optimization of electrical properties alone could be sufficient. For example, Fortunato et al [FPP$^+$04] have reported that ZnO films with highest resistivity also have the highest optical transmittance. They were able to obtain 90% transmittance by optimizing the sputtering deposition power.

7.2 Electrical properties

The mobility of the deposited films can further be improved, up to at least 70 $\frac{cm^2}{Vs}$ [FPP$^+$04]. This will greatly benefit the portability of the device, allow lower power operation, and enable faster switching speeds. Faster switching also means higher frame rates, which is useful beyond touchscreen applications in areas such as robotics. Lower operational voltage would also allow easier integration with the mobile devices, where voltages are typically limited to 0V to +5V scale, and negative voltages are usually also not available.

7.3 Cost

Cost of device manufacturing is typically the lowest priority at the research level, but it is usually listed as the top three key criteria by the industry professionals when a new technology is being considered. The typical cost driving factors for a ZnO TFT process, in no particular order, are: number of deposited layers, cost of patterning (feature size), target materials, deposition time, deposition temperature, vacuum levels.

One of the important potential cost savings for our device can be achieved by replacing the ITO conductive layers with AZO. According to a report from US Department of Energy, the cost of ITO is about 25% of the cost of AZO, and Zn material is about 10 times cheaper than In [And13]. Table 7.1 shows the cost of the elements comprising the three materials of interest. Indium and tin are rare earth materials that are significantly more expensive than aluminum and zinc. To make this replacement successful, a number of other factors must be considered, including the optical and electrical properties of the films.

Table 7.1: Comparison of cost and abundance of metals used to make ITO and AZO sputtering targets. Data shown for aluminum, indium, tin, and zinc. From these materials, aluminum and zinc are the cheapest and most abundant. Indium and tin are expensive and rare.

Metal	Price, USD per ton [1]	Abundance in Earth's crust [2]	World production (tons) [3]
Aluminum	1.6K	8.1%	13724K (primary)
Indium	300K	0.000016%	820 [4]
Tin	16K	0.00022%	244K
Zinc	1.8K	0.0078%	820K

It is difficult to compare the properties of AZO and ITO thin films, because they are highly dependent on the film growth methods and the post-growth treatment, such as annealing. Furthermore, the raw material composition does not identically correspond to the stoichiometry or the conductivity of the deposited film, and there are multiple optimizations reported by researchers to improve the deposited films' characteristics. Therefore, various reports can provide different film characteristics for the same material. For example, in our lab, ITO has inferior transmittance compared to AZO. However, according to information listed on the Advanced Energy company website, the ITO film has better transmission [Ene]. A presentation compiled by IDTech on ITO listed the AZO film as having 50% higher resistivity compared to the ITO [Zer12].

ITO films are not suitable for flexible substrates; thin ITO films increase sheet resistance by 1000% after 300 cycles of bending to a 8.9 mm diameter [AHLS11]. Although flexible ITO has been demonstrated [WCHL13] and even commercialized (see FITOS [FIT]), the price of ITO still continues to drive flexible electrode research towards new materials. The AZO film can be made compatible with bendable electronics. AZO films with thickness of about 100 nm deposited by PLD with original resistance of 300 $\frac{\Omega}{\square}$ increase their resistance by 34 % (up to 400 $\frac{\Omega}{\square}$) after 200 bending cycles on 25mm diameter cylinder [SZSG14]. Hybrid structures like AZO/Ag/AZO [JPKL13] [GYS+14] or AZO/Ag NW/AZO [HSF+15] have been also demonstrated to possess good mechanical properties.

[1]Source: www.metalprices.com, prices are approximate, current as of August-September 2015
[2]Source: http://www.periodictable.com/Properties/A/CrustAbundance.an.log.html
[3]Source: statista.com, data from 2014
[4]Source: http://minerals.usgs.gov, 2014 data

7.4 Mechanical properties

It is necessary to investigate the stability of the devices due to mechanical stress. Any commercialization effort of the ZnO TFT pressure sensor technology would be concerned with longevity of the device. In particular, the following items are of interest:

1. How many times can pressure be applied on top of the device before breakage?
2. What is the maximum pressure that the device can withstand?
3. Can the device pass the "steel ball drop" test?
4. What is the effect of anti-scratch hard coating on the ZnO TFT pressure sensitivity?

Also, the device fabrication on flexible substrate must be demonstrated, characterized, and optimized. This would include the development of crack-free conductors and insulators that are capable of bending and/or stretching without a degradation in electrical properties.

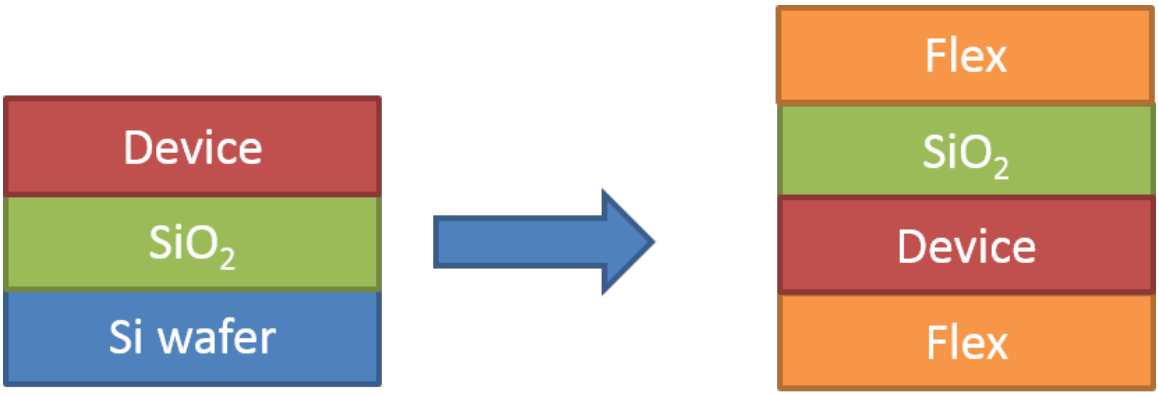


Figure 7.1: Process of transferring the ZnO TFT onto flexible substrates.

We have briefly looked into the possibility of transferring the devices to flexible substrate. The process developed in our lab allows the fabrication of devices on Si wafers, with the subsequent spin-coating of a flexible material, such as polyimide, on top of the device, the etching of Si carrier wafer, and the coating of the resulting exposed silicon oxide layer on the backside. The final desired device structure is shown in Figure 7.1. On-going efforts include the fabrication of flexible arrays of ZnO thin film transistor pressure sensors.

Appendix A

Code listings

Customized device characterization and data analysis was required throughout the research, and computer code has been written in a variety of programming languages to accomplish these tasks. This has included, in part:

FET measurement - Visual C++

A general-purpose GUI program for capturing the I-V (2 terminal), I_d-V_d (3 terminal), I_d-V_g (3 terminal), and I-t (3 terminal) characteristics using the measurement components available in our lab: Keithley 6487 picoammeter, NI-6030E Data Acquisition System, and the optical table along with probes. This program has been used for longer than 5 years to characterize all of our fabricated devices, and eventually was also adopted by other projects in the research group. This program has been subsequently rewritten in Python using the Qt GUI toolkit for improved cross-platform compatibility, better plotting and data saving capability, and easier code maintenance. The Visual C++ version is no longer in use. The source code for the measurement GUI tool has been made publicly available via github.com, and can be found at the following location: https:

//github.com/vishniakou/scientific-instruments/tree/master/fet_measurement

C-V measurement - Python

A command-line based Python program (typically launched using Spyder) for measuring the C-V characteristics using HP 4284A LCR meter. The program includes a control class for the LCR meter, and the routines for performing C-V sweeps at multiple frequencies, and C-f sweeps at multiple biases, as well as the C-t (capacitance over time) measurements at a fixed bias. The source code for the measurement script has been made publicly available via github.com, and can be found at the following location: https://github.com/vishniakou/scientific-instruments/tree/master/agilent4284a

ADC MCP3201 - Arduino

Arduino code for interacting with the MCP3201 ADC chip using the SPI library. The source code for the program has been made publicly available via github.com, and can be found at the following location: https://github.com/vishniakou/arduino-circuits/tree/master/ADC_MCP3201

DAC MCP4911 - Arduino

Arduino code for interacting with the MCP4911 DAC chip using the SPI library. The source code for the program has been made publicly available via github.com, and can be found at the following location: https://github.com/vishniakou/arduino-circuits/tree/master/DAC_MCP4911

DAQ card NI-6030E

Python control class for interacting with the NI 6030E data acquisition board. The device is interfaced through the PyDAQmx library. The source code for the

program has been made publicly available via github.com, and can be found at the following location: https://github.com/vishniakou/scientific-instruments/blob/master/ni6030e.py

Mobility fitting script

Python script to perform numerical optimization in order to find the best-fit value for threshold voltage and mobility from the measured I_d-V_d or I_d-V_g data. The source code for the script is publicly available via github.com, and can be found at the following address: https://github.com/vishniakou/device-analysis/blob/master/mobility_extraction.py

Bibliography

[ACZ+10] Vitaliy Avrutin, Gene Cantwell, Jizhi Zhang, J J Song, Donald J Silversmith, and Hadis Morkoç. Bulk ZnO: Current status, challenges, and prospects. *Proceedings of the IEEE*, 98(7):1339–1350, jul 2010.

[AHLS11] Khalid Alzoubi, Mohammad M. Hamasha, Susan Lu, and Bahgat Sammakia. Bending fatigue study of sputtered ITO on flexible substrate. *J. Display Technol.*, 7(11):593–600, nov 2011.

[AKKC11] Cheol Hyoun Ahn, Bo Hyun Kong, Hyoungsub Kim, and Hyung Koun Cho. Improved electrical stability in the al doped ZnO thin-film-transistors grown by atomic layer deposition. *Journal of The Electrochemical Society*, 158(2):H170, 2011.

[All14] Ranulfo Allen. Scalable, transparent, flexible, thin-film pressure sensors utilizing ultrasoft elastomers. Presented at the 2014 MRS Fall Meeting, 2014.

[And13] Andre Anders. Low-cost solutions for dynamic window materials. http://energy.gov/sites/prod/files/2013/12/f5/emrgtech19_anders_040413.pdf, 2013. Online pdf presentation, accessed 2015-08-11.

[BAS+09] M. Bar, K.-S. Ahn, S. Shet, Y. Yan, L. Weinhardt, O. Fuchs, M. Blum, S. Pookpanratana, K. George, W. Yang, J. D. Denlinger, M. Al-Jassim, and C. Heske. Impact of air exposure on the chemical and electronic structure of ZnO:zn[sub 3]n[sub 2] thin films. *Appl. Phys. Lett.*, 94(1):012110, 2009.

[BB10] Mudit Ratana Bhalla and Anand Vardhan Bhalla. Comparative study of various touchscreen technologies. *International Journal of Computer Applications*, 6(8):12–18, sep 2010.

[BDT+13] J. A. Berg, J. F. Dammann, F. V. Tenore, G. A. Tabot, J. L. Boback, L. R. Manfredi, M. L. Peterson, K. D. Katyal, M. S. Johannes, A. Makhlin, R. Wilcox, R. K. Franklin, R. J. Vogelstein, N. G. Hatsopoulos, and S. J. Bensmaia. Behavioral demonstration of a somatosensory

neuroprosthesis. *IEEE Trans. Neural Syst. Rehabil. Eng.*, 21(3):500–507, may 2013.

[BL11] Burhan Bayraktaroglu and Kevin Leedy. Ordered nanocrystalline ZnO films for high speed and transparent thin film transistors. In *2011 11th IEEE International Conference on Nanotechnology*. Institute of Electrical & Electronics Engineers (IEEE), aug 2011.

[BL14] B. Bayraktaroglu and K. Leedy. Fabrication method for zno thin film transistors using etch-stop layer, may 2014. US Patent 8,728,861.

[BLN08] Burhan Bayraktaroglu, Kevin Leedy, and Robert Neidhard. Microwave ZnO thin-film transistors. *IEEE Electron Device Lett.*, 29(9):1024–1026, sep 2008.

[BMVP+14] Rajesh Biswal, Arturo Maldonado, Jaime Vega-Pérez, Dwight Acosta, and María De La Luz Olvera. Indium doped zinc oxide thin films deposited by ultrasonic chemical spray technique, starting from zinc acetylacetonate and indium chloride. *Materials*, 7(7):5038–5046, jul 2014.

[BO10] G. Barrett and R. Omote. Projected-capacitive touch technology. *Information Display*, 26(3):16–21, mar 2010.

[BSG+12] Sarbani Basu, Pramod K. Singh, C. Ghanshyam, Pawan Kapur, and Yeong-Her Wang. Active layer thickness effects on the on-state current and pulse measurement at room temperature on deposited zinc oxide thin-film transistors. *Journal of Electronic Materials*, 41(9):2362–2368, may 2012.

[BWD+15] Rongrong Bao, Chunfeng Wang, Lin Dong, Ruomeng Yu, Kun Zhao, Zhong Lin Wang, and Caofeng Pan. Flexible and controllable piezophototronic pressure mapping sensor matrix by ZnO NW/p-polymer LED array. *Adv. Funct. Mater.*, 25(19):2884–2891, mar 2015.

[BZD+13] L. J. Brillson, Z. Zhang, D. R. Doutt, D. C. Look, B. G. Svensson, A. Yu. Kuznetsov, and F. Tuomisto. Interplay of dopants and native point defects in ZnO. *Phys. Status Solidi B*, jul 2013.

[CD15] I. Campbell and R. Diestelhorst. Microelectromechanical load sensor and methods of manufacturing the same, may 2015. US Patent 9,032,818.

[CDZ+09] W X Cheng, A L Ding, X S Zheng, P S Qiu, and X Y He. Optical and electrical properties of ZnO nanocrystalline textured films prepared by DC reactive magnetron sputtering. *J. Phys.: Conf. Ser.*, 152:012036, mar 2009.

[CLL+15] Jingjing Chang, Zhenhua Lin, Ming Lin, Chunxiang Zhu, Jie Zhang, and Jishan Wu. Solution processed f doped ZnO (ZnO:f) for thin film transistors and improved stability through co-doping with alkali metals. *J. Mater. Chem. C*, 3(8):1787–1793, 2015.

[CPRB94] Andrea Dal Corso, Michel Posternak, Raffaele Resta, and Alfonso Baldereschi. Ab initio study of piezoelectricity and spontaneous polarization in ZnO. *Phys. Rev. B*, 50(15):10715–10721, oct 1994.

[Cul78] B.D. Cullity. *Elements of X-ray Diffraction*. Addison-Wesley series in metallurgy and materials. Addison-Wesley Publishing Company, 1978.

[CWH+05] H. Q. Chiang, J. F. Wager, R. L. Hoffman, J. Jeong, and D. A. Keszler. High mobility transparent thin-film transistors with amorphous zinc tin oxide channel layer. *Appl. Phys. Lett.*, 86(1):013503, 2005.

[DFL+07] W.L. Dang, Y.Q. Fu, J.K. Luo, A.J. Flewitt, and W.I. Milne. Deposition and characterization of sputtered ZnO films. *Superlattices and Microstructures*, 42(1-6):89–93, jul 2007.

[DMD92] E. S. Dellon, R. Mourey, and A. L. Dellon. Human pressure perception values for constant and moving one- and two-point discrimination. *Plast. Reconstr. Surg.*, 90(1):112–117, Jul 1992.

[DRDC+13] Jolien Dendooven, Ranjith K. Ramachandran, Kilian Devloo-Casier, Geert Rampelberg, Matthias Filez, Hilde Poelman, Guy B. Marin, Emiliano Fonda, and Christophe Detavernier. Low-temperature atomic layer deposition of platinum using (methylcyclopentadienyl)trimethylplatinum and ozone. *J. Phys. Chem. C*, 117(40):20557–20561, oct 2013.

[dW00] Chris G. Van de Walle. Hydrogen as a cause of doping in zinc oxide. *Phys. Rev. Lett.*, 85(5):1012–1015, jul 2000.

[EDLP10] David Estrada, Sumit Dutta, Albert Liao, and Eric Pop. Reduction of hysteresis for carbon nanotube mobility measurements using pulsed characterization. *Nanotechnology*, 21(8):085702, jan 2010.

[Ene] Advanced Energy. Solar applications faq. Company website FAQ page [Accessed: 2016-03-16].

[FBM12] E. Fortunato, P. Barquinha, and R. Martins. Oxide semiconductor thin-film transistors: A review of recent advances. *Adv. Mater.*, 24(22):2945–2986, may 2012.

[FBP+05] E. Fortunato, P. Barquinha, A. Pimentel, A. Gonçalves, A. Marques, L. Pereira, and R. Martins. Recent advances in ZnO transparent thin film transistors. *Thin Solid Films*, 487(1-2):205–211, sep 2005.

[FH13] Brent Fultz and James Howe. Diffraction and the x-ray powder diffractometer. In *Transmission Electron Microscopy and Diffractometry of Materials*, pages 1–57. Springer Science + Business Media, 2013.

[FIT] FITOS. Flexible ito solutions. Company website [Accessed: 2015-09-12].

[FL95] M. S. Freund and N. S. Lewis. A chemically diverse conducting polymer-based "electronic nose". *Proceedings of the National Academy of Sciences*, 92(7):2652–2656, mar 1995.

[FPP+04] E. Fortunato, A. Pimentel, L. Pereira, A. Gonçalves, G. Lavareda, H. Águas, I. Ferreira, C.N. Carvalho, and R. Martins. High field-effect mobility zinc oxide thin film transistors produced at room temperature. *Journal of Non-Crystalline Solids*, 338-340:806–809, jun 2004.

[FRS+08] E Fortunato, L Raniero, L Silva, A Goncalves, A Pimentel, P Barquinha, H Aguas, L Pereira, G Goncalves, and I Ferreira. Highly stable transparent and conducting gallium-doped zinc oxide thin films for photovoltaic applications. *Solar Energy Materials and Solar Cells*, 92(12):1605–1610, dec 2008.

[GCS13] Qing Guo, G. Z. Cao, and I. Y. Shen. Measurements of piezoelectric coefficient d 33 of lead zirconate titanate thin films using a mini force hammer. *J. Vib. Acoust.*, 135(1):011003, feb 2013.

[GKS+05] L. A. Giannuzzi, B. W. Kempshall, S. M. Schwarz, J. K. Lomness, B. I. Prenitzer, and F. A. Stevie. *Introduction to Focused Ion Beams: Instrumentation, Theory, Techniques and Practice*, chapter FIB Lift-Out Specimen Preparation Techniques, pages 201–228. Springer US, Boston, MA, 2005.

[Gri99] David J. Griffiths. *Introduction to Electrodynamics (3rd Edition)*. Prentice Hall, 1999.

[GYS+14] Angus R. Gentle, Soniya D. Yambem, Geoff B. Smith, Paul L. Burn, and Paul Meredith. Optimized multilayer indium-free electrodes for organic photovoltaics. *Phys. Status Solidi A*, 212(2):348–355, oct 2014.

[HB05] S.K. Hazra and S. Basu. ZnO p–n junctions produced by a new route. *Solid-State Electronics*, 49(7):1158–1162, jul 2005.

[HB06] S.K. Hazra and S. Basu. Hydrogen sensitivity of ZnO p–n homojunctions. *Sensors and Actuators B: Chemical*, 117(1):177–182, sep 2006.

[HHAC09] Zhang Huafu, Liu Hanfa, Zhou Aiping, and Yuan Changkun. Influence of the distance between target and substrate on the properties of transparent conducting al–zr co-doped zinc oxide thin films. *Journal of Semiconductors*, 30(11):113002, nov 2009.

[Hic05] F.S. Hickernell. The piezoelectric semiconductor and acoustoelectronic device development in the sixties. *IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control*, 52(5):737–745, may 2005.

[HNW03] R. L. Hoffman, B. J. Norris, and J. F. Wager. ZnO-based transparent thin-film transistors. *Appl. Phys. Lett.*, 82(5):733, 2003.

[HSF+15] Qijin Huang, Wenfeng Shen, Xingzhong Fang, Guofei Chen, Ye Yang, Jinhua Huang, Ruiqin Tan, and Weijie Song. Highly thermostable, flexible, transparent, and conductive films on polyimide substrate with an AZO/AgNW/AZO structure. *ACS Appl. Mater. Interfaces*, 7(7):4299–4305, feb 2015.

[HWZ+11] DeDong Han, Yi Wang, ShengDong Zhang, Lei Sun, RuQi Han, Satoru Matsumoto, and Yuji Ino. Influence of sputtering power on properties of ZnO thin films fabricated by RF sputtering in room temperature. *Science China Information Sciences*, 55(4):951–955, jul 2011.

[IA13] A. Ismail and M.J. Abdullah. The structural and optical properties of ZnO thin films prepared at different RF sputtering power. *Journal of King Saud University - Science*, 25(3):209–215, jul 2013.

[Jan10] Anderson Janotti. Defects and doping in oxides: What we have learned so far, 02 2010. Talk by Janotti at Stanford [Accessed: 2015 09 05].

[JB04] S.H. Jeong and J.H. Boo. Influence of target-to-substrate distance on the properties of AZO films grown by RF magnetron sputtering. *Thin Solid Films*, 447-448:105–110, jan 2004.

[JdW05] Anderson Janotti and Chris G. Van de Walle. Oxygen vacancies in ZnO. *Appl. Phys. Lett.*, 87(12):122102, 2005.

[JdW09] Anderson Janotti and Chris G Van de Walle. Fundamentals of zinc oxide as a semiconductor. *Rep. Prog. Phys.*, 72(12):126501, oct 2009.

[JHB14] Richard W. Johnson, Adam Hultqvist, and Stacey F. Bent. A brief review of atomic layer deposition: from fundamentals to applications. *Materials Today*, 17(5):236–246, jun 2014.

[Ji10] Wook Ryu Ji. Dependence of optical anisotropy of ZnO thin filmson the structural properties. *J. Korean Phys. Soc.*, 57(21):389, aug 2010.

[JP11] C. Jagadish and S.J. Pearton. *Zinc Oxide Bulk, Thin Films and Nanostructures: Processing, Properties, and Applications*. Elsevier Science, 2011.

[JPKL13] Yu Sup Jung, Yong Seo Park, Kyung Hwan Kim, and Won-Jae Lee. Properties of azo/ag/azo multilayer thin film deposited on polyethersulfone substrate. *Transactions on Electrical and Electronic Materials*, 14(1):9–11, feb 2013.

[JPN+14] S.H. Jeon, J.J. Park, T.T. Nguyen, J.H. Bae, K.E. Byun, N.E. LEE, D. KIM, and Q.T. TRAN. Pressure sensor and pressure sensing method, mar 2014. US Patent App. 14/018,505.

[JRS+15] C. Jiang, S. L. Rumyantsev, R. Samnakay, M. S. Shur, and A. A. Balandin. High-temperature performance of MoS2 thin-film transistors: Direct current and pulse current-voltage characteristics. *J. Appl. Phys.*, 117(6):064301, feb 2015.

[JS14] Navid M. S. Jahed and Siva Sivoththaman. Systematic control of carrier concentration and resisitivity in rf sputtered zinc oxide thin films, 2014.

[JSL10] Zhang Jun, Xue Shuwen, and Shao Lexi. P-type ZnO thin films prepared by in situ oxidation of DC sputtered zn 3 n 2 :ga. *Journal of Semiconductors*, 31(4):043001, apr 2010.

[KL04] R B Kale and C D Lokhande. Band gap shift, structural characterization and phase transformation of CdSe thin films from nanocrystalline cubic to nanorod hexagonal on air annealing. *Semiconductor Science and Technology*, 20(1):1–9, nov 2004.

[KML+09] J.H. Kim, J.Y. Moon, H.S. Lee, W.S. Han, H.K. Cho, J.Y. Lee, and H.S. Kim. Al/au ohmic contact to n-ZnO by dc sputtering. *Materials Science and Engineering: B*, 165(1-2):77–79, nov 2009.

[KNH+11] Maarit Kariniemi, Jaakko Niinisto, Timo Hatanpaa, Marianna Kemell, Timo Sajavaara, Mikko Ritala, and Markku Leskela. Plasma-enhanced atomic layer deposition of silver thin films. *Chemistry of Materials*, 23(11):2901–2907, jun 2011.

[KSR+13] Martin Kaltenbrunner, Tsuyoshi Sekitani, Jonathan Reeder, Tomoyuki Yokota, Kazunori Kuribara, Takeyoshi Tokuhara, Michael Drack, Reinhard Schwödiauer, Ingrid Graz, Simona Bauer-Gogonea, Siegfried Bauer, and Takao Someya. An ultra-lightweight design for imperceptible plastic electronics. *Nature*, 499(7459):458–463, jul 2013.

[KTS93] K. Kuriyama, Yukimi Takahashi, and F. Sunohara. Optical band gap of zn 3 n 2 films. *Phys. Rev. B*, 48(4):2781–2782, jul 1993.

[Kuo13] Yue Kuo. Thin film transistor technologypast, present, and future. *The Electrochemical Society Interface*, 2013.

[Lab13] Penn State Applied Research Laboratory. Ac sputtering. https://www.arl.psu.edu/mm_mp_ac_sputtering.php, 2013. Accessed: 2015-09-04.

[LBBT12] Hing Wah Lee, Daniel C. S. Bien, Siti Aishah Mohamad Badaruddin, and Aun Shih Teh. Silver (ag) as a novel masking material in glass etching for microfluidics applications. *Microsystem Technologies*, 19(2):253–259, jun 2012.

[LBL+14] S.V. Litvinenko, D. Bielobrov, V. Lysenko, T. Nychyporuk, and V.A. Skryshevsky. Might silicon surface be used for electronic tongue application? *ACS Appl. Mater. Interfaces*, 6(21):18440–18444, nov 2014.

[LCSC00] C. M. Lueng, H. L. W. Chan, C. Surya, and C. L. Choy. Piezoelectric coefficient of aluminum nitride and gallium nitride. *J. Appl. Phys.*, 88(9):5360, 2000.

[LGR+11] Masihhur R. Laskar, Tapas Ganguli, A. A. Rahman, Amlan Mukherjee, Nirupam Hatui, M. R. Gokhale, and Arnab Bhattacharya. Distorted wurtzite unit cells: Determination of lattice parameters of nonpolar a-plane AlGaN and estimation of solid phase al content. *J. Appl. Phys.*, 109(1):013107, 2011.

[LHCN14] K. Lee, W.K. Hong, M.S. Choi, and S. Nam. Touch display apparatus sensing touch force, February 27 2014. US Patent App. 13/763,451.

[LNWO11] Flora M. Li, Arokia Nathan, Yiliang Wu, and Beng S. Ong. *Organic Thin Film Transistor Integration*. Wiley-Blackwell, apr 2011.

[LQL+98] K. Lee, T. Quach, D. Li, L.D. Hou, S. Chung, and T.Y. Chi. Process for providing clean lift-off of sputtered thin film layers, January 6 1998. US Patent 5,705,432.

[LVT+11] Darren J. Lipomi, Michael Vosgueritchian, Benjamin C-K. Tee, Sondra L. Hellstrom, Jennifer A. Lee, Courtney H. Fox, and Zhenan Bao. Skin-like pressure and strain sensors based on transparent elastic films of carbon nanotubes. *Nature Nanotech*, 6(12):788–792, oct 2011.

[LYL+15] Xinqin Liao, Xiaoqin Yan, Pei Lin, Shengnan Lu, Yuan Tian, and Yue Zhang. Enhanced performance of ZnO piezotronic pressure sensor through electron-tunneling modulation of MgO nanolayer. *ACS Appl. Mater. Interfaces*, 7(3):1602–1607, jan 2015.

[Mak10] Oleg Maksimov. Recent advances and novel approaches of p-type doping of zinc oxide, 2010.

[MF06] S.O. Reza Moheimani and Andrew J. Fleming. *Piezoelectric Transducers for Vibration Control and Damping (Advances in Industrial Control)*. Springer, 2006.

[Min05] Tadatsugu Minami. Transparent conducting oxide semiconductors for transparent electrodes. *Semiconductor Science and Technology*, 20(4):S35–S44, mar 2005.

[MÖ08] H. Morkoç and Ü. Özgür. *Zinc Oxide: Fundamentals, Materials and Device Technology*. Wiley, 2008.

[MRSP89] G. Moersch, P. Rava, F. Schwarz, and A. Paccagnella. Thin-film transistors with sputtered CdSe as semiconductor. *IEEE Trans. Electron Devices*, 36(2):449–451, 1989.

[MTS+10] Stefan C. B. Mannsfeld, Benjamin C-K. Tee, Randall M. Stoltenberg, Christopher V. H-H. Chen, Soumendra Barman, Beinn V. O. Muir, Anatoliy N. Sokolov, Colin Reese, and Zhenan Bao. Highly sensitive flexible pressure sensors with microstructured rubber dielectric layers. *Nature Materials*, 9(10):859–864, sep 2010.

[Mus98] J Musil. Low-pressure magnetron sputtering. *Vacuum*, 50(3-4):363–372, jul 1998.

[MZJ10] D.A. Mourey, D.A. Zhao, and T.N. Jackson. Self-aligned-gate ZnO TFT circuits. *IEEE Electron Device Lett.*, 31(4):326–328, apr 2010.

[Nan13] Xiao Nan. Thin-film transistors fabricated using sputter deposition of zno. Master's thesis, Rochester Institute of Technology, 07 2013.

[Nat15] D. Natelson. *Nanostructures and Nanotechnology*. Cambridge University Press, 2015.

[New04] R.E. Newnham. *Properties of Materials : Anisotropy, Symmetry, Structure: Anisotropy, Symmetry, Structure*. OUP Oxford, 2004.

[NHT+03] Junya Nishii, Faruque M. Hossain, Shingo Takagi, Tetsuya Aita, Koji Saikusa, Yuji Ohmaki, Isao Ohkubo, Shuya Kishimoto, Akira Ohtomo, Tomoteru Fukumura, Fumihiro Matsukura, Yuzo Ohno, Hideomi Koinuma, Hideo Ohno, and Masashi Kawasaki. High mobility thin film transistors with transparent ZnO channels. *Jpn. J. Appl. Phys.*, 42(Part 2, No. 4A):L347–L349, apr 2003.

[NLCC13] A. Nathan, J.C.S. Lai, S.B. Cha, and C. Church. Pressure sensing display device, October 10 2013. WO Patent App. PCT/CA2013/000,326.

[NMK+99] Hiroyuki Naoe, Yuzuru Mitani, Toshiyuki Kitagawa, Satoru Kishida, Fumihiko Toda, and Heizo Tokutaka. Ba1-xRbxBiOy thin films prepared by rf magnetron sputtering. In *Advances in Superconductivity XI*, pages 1055–1058. Springer Science + Business Media, 1999.

[Nor84] Gunnar F. Nordberg. Chelating agents and cadmium toxicity: Problems and prospects. *Environmental Health Perspectives*, 54:213–218, 1984.

[NWKH13] T. Nguyen, D. Wang, Y.O. KIM, and W. Ha. Systems and devices for recording and reproducing senses, March 28 2013. WO Patent App. PCT/US2012/035,305.

[OH96] M. O'Keeffe and B.G. Hyde. *Crystal Structures, No. 1: Patterns & Symmetry*. Crystal Structures. Mineralogical Society of America, 1996.

[OSH89] OSHA. Zinc oxide in workplace atmosphere, mar 1989.

[PCR+02] Gun-Tae Park, Jong-Jin Choi, Jungho Ryu, Huiqing Fan, and Hyoun-Ee Kim. Measurement of piezoelectric coefficients of lead zirconate titanate thin films by strain-monitoring pneumatic loading method. *Appl. Phys. Lett.*, 80(24):4606, 2002.

[PDZ+13] Caofeng Pan, Lin Dong, Guang Zhu, Simiao Niu, Ruomeng Yu, Qing Yang, Ying Liu, and Zhong Lin Wang. High-resolution electroluminescent imaging of pressure distribution using a piezoelectric nanowire LED array. *Nature Photonics*, 7(9):752–758, aug 2013.

[PH72] CRD Priestland and S.D. Hersee. The effects of pressure on the deposition rate in rf sputtering processes. *Vacuum*, 22(3):103–106, mar 1972.

[Pie96] R.F. Pierret. *Semiconductor Device Fundamentals*. Addison-Wesley, 1996.

[PSNG06] T.C. Pearce, S.S. Schiffman, H.T. Nagle, and J.W. Gardner. *Handbook of Machine Olfaction: Electronic Nose Technology*. Wiley, 2006.

[PSS+13] Namseok Park, Ke Sun, Zhelin Sun, Yi Jing, and Deli Wang. High efficiency NiO/ZnO heterojunction UV photodiode by sol–gel processing. *Journal of Materials Chemistry C*, 1(44):7333, 2013.

[RCPJ10] K. Remashan, Y. S. Choi, S. J. Park, and J. H. Jang. Enhanced performance of MOCVD ZnO TFTs on glass substrates with nitrogen-rich silicon nitride gate dielectric. *Journal of The Electrochemical Society*, 157(1):H60, 2010.

[RdSA+12] A M Rosa, E P da Silva, E Amorim, M Chaves, A C Catto, P N Lisboa-Filho, and J R R Bortoleto. Growth evolution of ZnO thin films deposited by RF magnetron sputtering. *J. Phys.: Conf. Ser.*, 370:012020, jun 2012.

[SBML15] Mohammad Suja, Sunayna B. Bashar, Muhammad M. Morshed, and Jianlin Liu. Realization of cu-doped p-type ZnO thin films by molecular beam epitaxy. *ACS Appl. Mater. Interfaces*, 7(16):8894–8899, apr 2015.

[SKR11] H.D. Stolovitch, E.J. Keeps, and M.J. Rosenberg. *Telling Ain't Training*. ASTD Press, 2011.

[SN06] Simon M. Sze and Kwok K. Ng. *Physics of Semiconductor Devices*. Wiley-Interscience, 2006.

[SZSG14] Maciej Sibiński, Katarzyna Znajdek, Mirosław Sawczak, and Michał Górski. AZO layers deposited by PLD method as flexible transparent emitter electrodes for solar cells. *Microelectronic Engineering*, 127:57–60, sep 2014.

[Tou14] Bbc science and nature - human body and mind - nervous system layer. http://www.bbc.co.uk/science/humanbody/body/factfiles/touch/touch.shtml, 2014. Accessed: 2016-02-12.

[TSM06] Ming-Lung Tu, Yan-Kuin Su, and Chun-Yang Ma. Nitrogen-doped p-type ZnO films prepared from nitrogen gas radio-frequency magnetron sputtering. *J. Appl. Phys.*, 100(5):053705, 2006.

[VLN+13] Siarhei Vishniakou, Brian W. Lewis, Xiaofan Niu, Alireza Kargar, Ke Sun, Michael Kalajian, Namseok Park, Muchuan Yang, Yi Jing, Paul Brochu, Zhelin Sun, Chun Li, Truong Nguyen, Qibing Pei, and Deli Wang. Tactile feedback display with spatial and temporal resolutions. *Sci. Rep.*, 3, aug 2013.

[Wan04] Zhong Lin Wang. Zinc oxide nanostructures: growth, properties and applications. *Journal of Physics: Condensed Matter*, 16(25):R829–R858, jun 2004.

[WC91] W.D. Willis and R.E. Coggeshall. *Sensory Mechanisms of the Spinal Cord*. A Wiley-Interscience Publication. Springer, 1991.

[WCHL13] John Lawton West, Miko Cakmak, Tsang-Min Huang, and Da-Wei Lee. Uni-axial cracking of ITO to form row and column electrodes for roll to roll production of flexible displays and electronics. *MRS Proc.*, 1529, jan 2013.

[WFA+13] Jesse R. Williams, Hirokazu Furukawa, Yutaka Adachi, Sergey Grachev, Elin Sondergard, and Naoki Ohashi. Polarity control of intrinsic ZnO films using substrate bias. *Appl. Phys. Lett.*, 103(4):042107, 2013.

[Whe04] H. E. Wheat. Human ability to scale and discriminate forces typical of those occurring during grasp and manipulation. *Journal of Neuroscience*, 24(13):3394–3401, mar 2004.

[WJ07] C. Wood and D. Jena. *Polarization Effects in Semiconductors: From Ab Initio Theory to Device Applications*. Springer US, 2007.

[WTPW14] Bing Wang, Lidan Tang, Shujing Peng, and Jianzhong Wang. Structural, optical and electrical properties of li-doped ZnO thin films influenced by annealing temperature. *J. Wuhan Univ. Technol.-Mat. Sci. Edit.*, 29(5):873–876, oct 2014.

[WWW13] W. Wu, X. Wen, and Z. L. Wang. Taxel-addressable matrix of vertical-nanowire piezotronic transistors for active and adaptive tactile imaging. *Science*, 340(6135):952–957, apr 2013.

[WYC14] ZhanWu Wang, Yonggao Yue, and Yan Cao. Preparation and properties of nitrogen doped p-type zinc oxide films by reactive magnetron sputtering. *Vacuum*, 101:313–316, mar 2014.

[WYN05] Bartosz Wyszynski, Takao Yamanaka, and Takamichi Nakamoto. Recording and reproducing citrus flavors using odor recorder. *Sensors and Actuators B: Chemical*, 106(1):388–393, apr 2005.

[XWZ+07] Bin Xiang, Pengwei Wang, Xingzheng Zhang, Shadi. A. Dayeh, David P. R. Aplin, Cesare Soci, Dapeng Yu, and Deli Wang. Rational synthesis of p-type zinc oxide nanowire arrays using simple chemical vapor deposition. *Nano Letters*, 7(2):323–328, feb 2007.

[XYL09] Songhua Xu, Wenxia Yang, and Francis C.M. Lau. A visualization based approach for digital signature authentication. *Computer Graphics Forum*, 28(3):935–942, jun 2009.

[YBO13] M.H. Yükselici, A. Aşıkoğlu Bozkurt, and B. Can Ömür. A detailed examination of the growth of CdSe thin films through structural and optical characterization. *Materials Research Bulletin*, 48(7):2442–2449, jul 2013.

[YKSDH+09] Moon Yeon-Keon, Lee Sih, Kim Do-Hyun, Lee Je-Hun, Jeong Chang-Oh, and Park Jong-Wan. Characteristics of ZnO based TFT using la2o3 high-k dielectrics. *J. Korean Phys. Soc.*, 55(51):1906, nov 2009.

[YSR13] Jiro Yota, Hong Shen, and Ravi Ramanathan. Characterization of atomic layer deposition HfO2, al2o3, and plasma-enhanced chemical vapor deposition si3n4 as metal–insulator–metal capacitor dielectric for GaAs HBT technology. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, 31(1):01A134, 2013.

[YWZ+13] Fengpo Yan, Yonghao Wang, Jiye Zhang, Zhang Lin, Jinsheng Zheng, and Feng Huang. Schottky or ohmic metal-semiconductor contact: Influence on photocatalytic efficiency of ag/ZnO and pt/ZnO model systems. *ChemSusChem*, 7(1):101–104, nov 2013.

[Zer12] Harry Zervos. The market for touch screens and ito replacement, 2012.

[ZW12] Yan Zhang and Zhong Lin Wang. Theory of piezo-phototronics for light-emitting diodes. *Adv. Mater.*, 24(34):4712–4718, mar 2012.