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Design of a Quick Startup Crystal Oscillator Circuit With Automatic Injection Frequency Calibration



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# Design of a Quick Startup Crystal Oscillator Circuit With Automatic Injection Frequency Calibration

A thesis submitted in partial satisfaction
of the requirements for the degree
Master of Science in Electrical and Computer Science

by

Haris Suhail

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ABSTRACT OF THE THESIS

Design of a Quick Startup Crystal Oscillator Circuit With Automatic Injection Frequency Calibration

by

Haris Suhail
Master of Science in Electrical and Computer Science
University of California, Los Angeles, 2021
Professor Sudhakar Pamarti, Chair

High-quality factor crystal oscillator circuits have long startup times which result in an increase in the average power consumption of duty-cycled systems. By injecting energy into a crystal for a precisely calculated time, the startup time can be significantly improved. This, however, requires that an injection frequency within 6000 ppm of the crystal's resonant frequency is available on chip. As such, for the precisely timed injection technique, each chip requires factory calibration of the ring oscillators to achieve the required accuracy. In this work we propose a re-configurable delay line which can be used to quickly match the period of a reference signal and can be reconfigured as a ring oscillator after the delay has been matched. Using this re-configurable delay line, we further propose a self-calibration scheme that uses the ringing voltage-step response of the crystal as a reference signal for the proposed delay-line. The delay line, after locking and re-configuring as a ring oscillator, provides injection signal to energize the crystal for quick startup.

The thesis of Haris Suhail is approved.

Chih-Kong Ken Yang

Subramanian S. Iyer

Sudhakar Pamarti, Committee Chair

University of California, Los Angeles

2021

*To my parents . . .*

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# CHAPTER 1

# Introduction

## 1.1 Motivation

The advent of energy-constrained applications such as Internet-of-Things (IoT), biomedical, implantable, and wearable devices, many of which are operated with small batteries, require the use of Ultra-Low-Power (ULP) radios. The power reduction in ULPs is achieved by aggressive duty cycling of the radio between the on and off state. One main factor that limits the energy saving benefits of duty cycling is the *start-up time* of the system. As will be shown, the startup time of such a system is limited by the start-up time of the crystal oscillator, which provides the low phase noise reference signal for radio operations. If left to start-up on its own, a crystal oscillator, owing to its high quality factor Q, will start up in several milliseconds. This time can be significantly longer than the active time of the radio. This increases the average power consumption. Therefore, it is important to have a quick starting reference oscillator which can predictably start up in a short time. One common technique to speed up this start-up is to energize the crystal with a injection signal prior to connecting it to an oscillator circuit. While this technique has shown success, it often requires the availability of an accurate injection source on chip. The accuracy requirement on the injection signal's frequency is generally very high. As such, simple ring oscillator circuits (which can start-up quickly) can't always be used for injection without individual factory calibration of each chip. This is a very expensive solution but is necessary due to the large variability of the ring oscillators frequency over process-voltage-temperature (PVT) variations. This thesis addresses the challenge of having the required accurate injection frequency for quick-startup

energy injection techniques by proposing a quickly re-configurable delay line and a scheme to acquire and lock the injection frequency from the crystal without starting up the entire oscillator circuity.

## 1.2 Thesis Outline

The outline of this thesis is as follows. Chapter 2 gives a summary of crystal resonators and oscillator circuits, their startup times, and the techniques that have been developed in order to hasten the startup. Chapter 3 outlines the details of the re-congfigurable delay line / ring oscillator. Chapter 4 goes over the proposed scheme that is used to automatically calibrate the injection frequency source. Chapter 5 goes over the specific circuit implementation of the proposed system in TSMC 65nm technology. Chapter 6 presents the results and conclusions from this work.

# CHAPTER 2

# Background of quick start-up techniques

High Quality (High-Q) crystal oscillators are used to generate the clock signal in analog and digital systems. Their ubiquitous use in electronic systems is because of their unparalleled precision and stability. Crystal oscillators, such as those based on quartz crystals, can achieve this due to the high-Q. However, this high-Q also makes these crystals extremely slow at startup. This chapter introduces the basics of quartz crystals and discusses the start-up time of these crystal resonator circuits. Then the prior literature of the techniques used to speed-up the startup time is reviewed.

## 2.1 Crystal Model

A crystal, such as a quartz crystal, converts between mechanical and electrical energy through the piezoelectric effect. By applying an alternating voltage across the crystal, the crystal can be made to physically vibrate. Maximum amplitude vibrations occur are the crystal's resonant frequency. High Quality (Q) is a desirable feature of quartz crystals. In mechanical terms, Q is the ratio of energy stored in the crystal to the energy loss per cycle. Electrically, Q is given by:

$$Q = \frac{2\pi f L_m}{R_m} \tag{2.1}$$

Where $L_m$ and $R_m$ are the motional inductance and resistance of the crystal. A high Q crystal will lose little energy during oscillations, and commercial crystals can have Q ranging

from 20,000 to 200,000. Crystals have different parallel and series resonant frequencies and can be tuned to produce the required frequency at one of the two resonances. Most oscillators operate in parallel resonant mode [2].

For electrical analysis, an electrical dual model is used which translates the mechanical properties of the crystal to an electrical model. That model is shown in Figure 2.1.

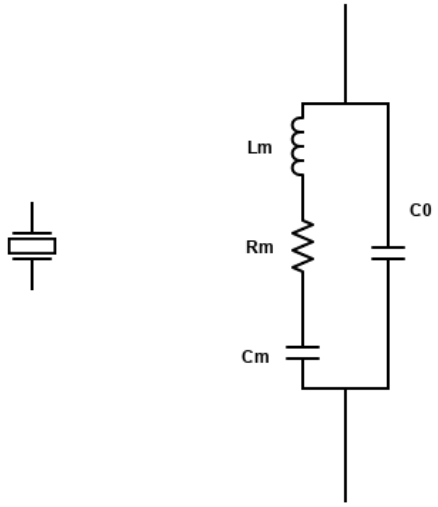


Figure 2.1: Schematic symbol of crystal (left) and its equivalent electrical model (right)

Here $L_m$ is called the motional inductance of the crystal, and is determined by the motional mass of the crystal during oscillation. $C_m$ is the crystal's motional capacitance and its value is determined by the crystal's stiffness. $R_m$ is the motional resistance of the crystal and it is related to the mechanical energy loss during oscillation. In this model, the series resonance frequency is given by:

$$\omega_m = \frac{1}{\sqrt{L_m C_m}} \tag{2.2}$$

The parallel resonance frequency is, in turn, given by:

$$\omega_p = \frac{1}{\sqrt{L_m C_m}} \cdot \sqrt{1 + \frac{C_m}{C_0}} \tag{2.3}$$

The relative separation between the series and parallel resonant frequencies is typically very small since $\frac{C_m}{C_0} \ll 1$. Within this range of frequencies, the crystal behaves as an effective inductor that resonates with an external capacitance to produce steady-state oscillations [3].

## 2.2 Start-up time of High-Q crystal oscillators

In order to have sustained oscillations, the crystal needs an active circuit to compensate for the loss in energy during oscillations, as shown in 2.2. This active circuit provides a effective negative resistance that compensates for the energy loss caused by $R_m$.

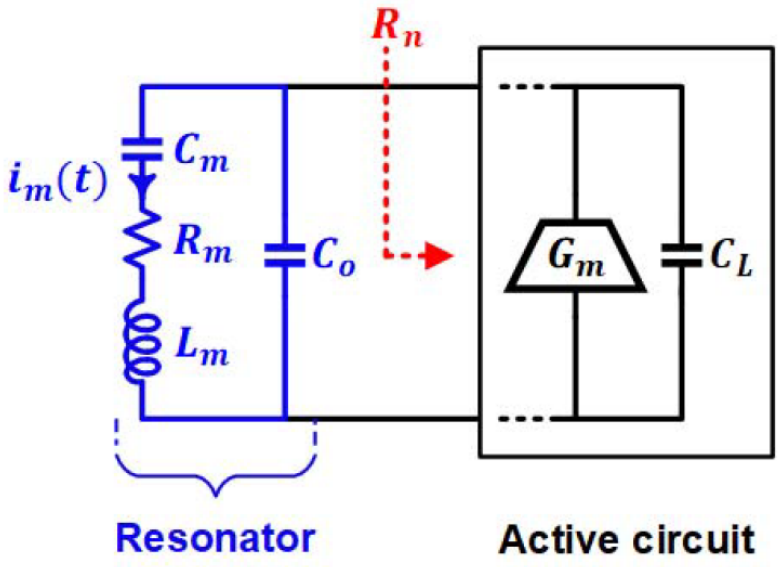


Figure 2.2: For sustained oscillations, the resonator needs an active circuit connected to it that presents an effective negative resistance, $R_n$

If the current in the motional branch of the crystal is denoted by $I_m(t)$, then it is shown in [4] that starting off with some amount of motional current, $I_m(0)$, the motional current will increase according to the time constant of the crystal oscillator circuit, as shown in the equation below:

$$|I_m(t)| = |I_m(0)|.e^{\frac{t}{\tau}} \tag{2.4}$$

where $\tau$ is the time constant of the circuit. If the effective negative resistance of the active circuit is given by $R_n$, then $\tau$ is given by:

$$\tau = \frac{-2L_m}{R_m + R_n} \tag{2.5}$$

Owing to the very large Q of crystal resonators, the the time constant is very large. A 10 Mhz crystal, as an example, can take a few milliseconds to start up. In constrast, startup times of other circuit blocks such as low-dropout regulators and phase-locked loops is usually less than $10\mu$s [3]. Startup time is therefore dominated by the crystal oscillator circuit.

## 2.3 Prior Art

It is evident that the slow start-up of crystal oscillators circuits significantly limits the energy savings of low power systems. As such, many techniques have been developed to improve this startup time. One method attempts to reduce the value of $\tau$ in equation 2.5 by increasing the transconductance of the active circuit and thereby increasing the negative resistance contribution [5]. The capacitive loading of the resonator can also be reduced [6]. However, these techniques achieve only limited improvements and they still rely on the circuit noise to start the oscillator which can make the start up time unpredictable and heavily dependent on PVT.

Another common method to start up the oscillator quickly is pre-energization, whereby the resonator is energized with a signal from an injection oscillator prior to being connected to an oscillator circuit. However, there is still a significant transient time after the energy injection, and the start up time is very sensitive to the difference between the injection frequency, $w_{inj}$, and the resonator's resonant frequency, $w_m$. In order to try to reduce

this dependency on injection signal frequency, researchers have tried frequency chirping [5] and frequency dithering [7] centered around the resonant frequency of the crystal, but with limited success. Such method have high power usage, as only a narrow band of frequencies in the chirp can actually energize the crystal.

In [1] the authors presented a technique that employs conventional single-frequency pre-energization, but only for a precisely controlled time. That technique reduced the startup time by 15x compared to prior art and is based on the realization that the amount of energy that is injected into the crystal is dependent on both the injection frequency and the injection time. When a crystal oscillator starts up and is in steady state, there is a steady state current flowing in the motional branch of the crystal, which we will refer to as the steady state motional current. If a crystal is energized using an injection frequency, its motional current increases steadily as shown in figure 2.3. If the injection is terminated exactly at the time when this current has increased to the steady state value, then the start-up time can be reduced significantly. If the injection time is lower than the optimal injection time, the motional current will have to build up to its steady state slowly. Likewise, if the injection time is longer than the optimal injection time, the crystal will 'over energize' and its motional current would have to be reduced slowly to the steady state value. This is shown pictorially in figure 2.3 from [1] . In order to make the system less dependent on PVT, the authors of [1] also made the injection amplitude track the steady state voltage swing of the oscillator. As a result of this, their system can operate over a temperature range of $-40°C$ to $85°C$. However, their technique requires a precise injection source, within $\pm 6000$ ppm of the resonant frequency of the crystal. This would require per-chip calibration of the injection ring oscillator, which is an expensive solution.

In [8], the authors addressed the problem of having the accurate injection frequency source in order to energize the crystal. Instead of using a ring oscillator as an injection source, the frequency information was extracted from the step response of the crystal. This was done by applying a voltage step to the crystal which results in a ringing current response.

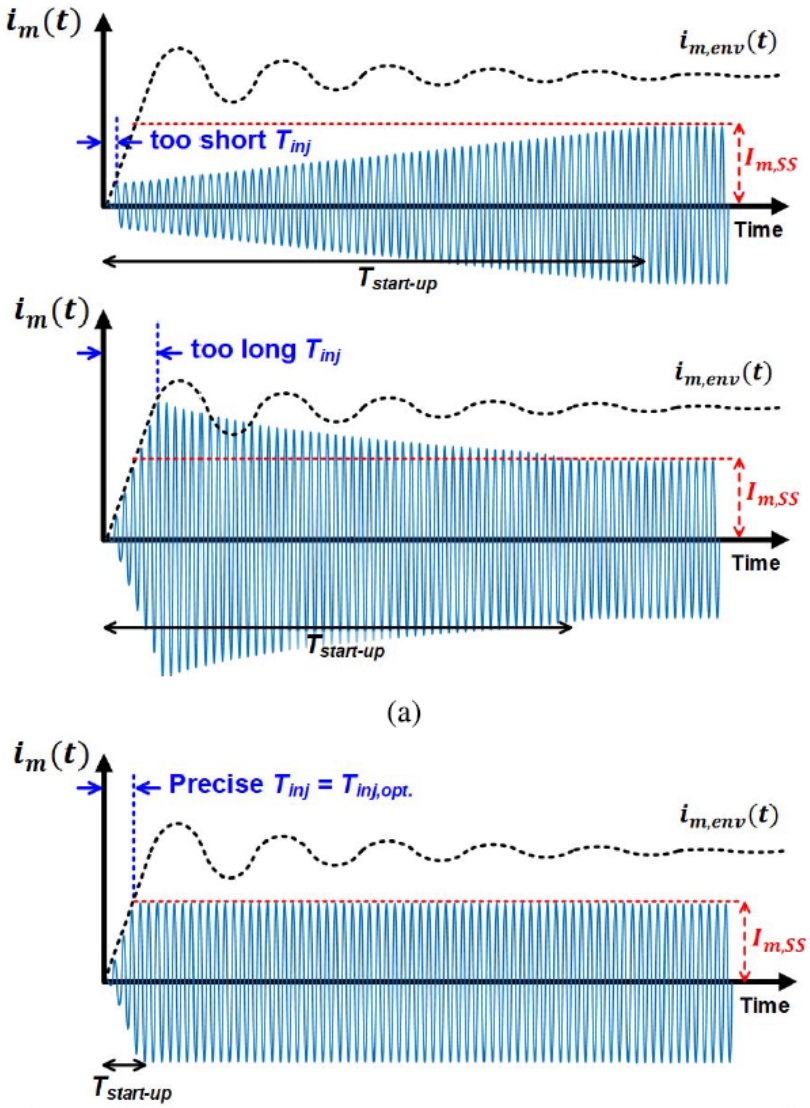


Figure 2.3: Plots from [1] showing the effect of different injection times while energizing the crystal

The zero-crossings of this response was detected using comparators in order to 'self time' the injection signal. Their startup time, however, is three times larger than what had been achieved by [1]. This is because of a large 'self timing' frequency mismatch which can vary a lot with noise.

In [9], the authors used impedance guided chirp injection to find the right injection frequency.

This involves applying a frequency chirp and monitoring the impedance presented by the crystal. When the chirp frequency approaches the resonance frequency of the crystal, the impedance drops and the chirp is stopped at that frequency. This frequency is then used to energize the crystal. Their start-up time and energy are, however, much higher compared to [1] and [8] due to the high circuit complexity and the long time taken for the initial impedance guided frequency searching.

## 2.4 Contribution of this work

As discussed in the previous section, the precisely timed injection technique developed in [1] outperforms any previous work by a significant margin. While that work does save upon energy and startup time, it still requires a very precise injection frequency source in order to work properly. Shown in Figure 2.4 is a plot from [1] showing how the startup time varies as the mismatch between the injection frequency and the resonant frequency of the crystal changes. As is evident, the technique proposed by the authors of [1] can only work reliably if the injection frequency is within $\pm 6000 ppm$ This injection frequency can be 1) external to the chip or 2) from an oscillator in the chip. In either case, a very accurate injection source needs to be present. If the injection source is a ring oscillator, it inevitably requires tuning of the ring oscillator so that the required accuracy is met. However, since ring oscillator's oscillation frequency can vary widely over process variations, calibration is needed for each chip. This is a very expensive solution that can significantly increase manufacturing cost. In this work, we address this challenge by:

- Presenting a re-configurable delay line/Ring oscillator that can lock to a reference signal within 10 cycles with a accuracy required by the application (1000ppm in this work)
- Presenting a technique to obtain a reference signal from a crystal using its voltage step response and quickly locking an on-chip oscillator to this ringing response.

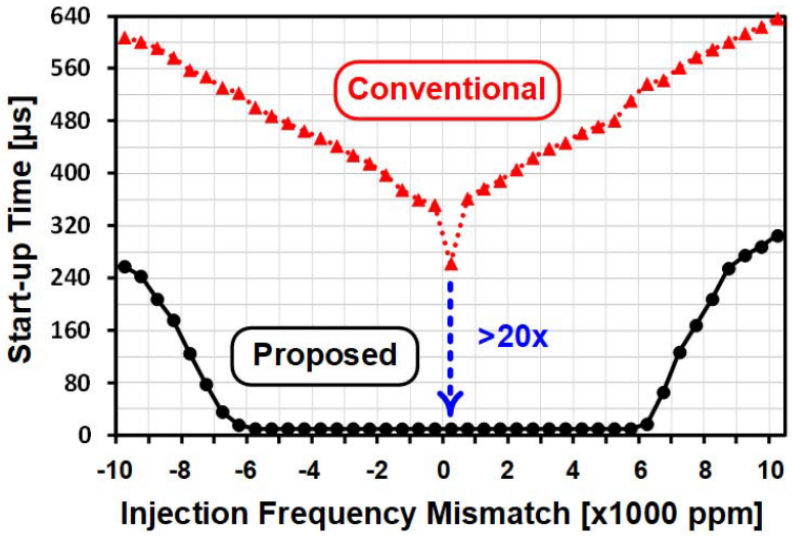


Figure 2.4: Plots from [1] showing allowed mismatch for the precisely timed injection technique

# CHAPTER 3

## Re-configurable Delay Line and Ring Oscillator

Presented in this chapter is a delay line/ring oscillator that can be used to lock to a reference frequency very quickly. This is a thermometric-ally weighted delay line with multiple coarse-fine sub stages and can be reconfigured as a ring oscillator. A block level overview of just one sub-stage of the delay line is given in Figure 3.1. As shown, the delay-line has the following features:

1. chain of delay elements. One delay element is labelled as 4 in figure 3.1.
2. flip-flops to monitor the propagation of an input signal along the delay line, labelled as 3 in figure 3.1.
3. mechanism to change the total delay along the delay line using a multiplexer that can connect any internal node of the delay line to the output. This multiplexer is labelled as 5 in figure 3.1.
4. mechanism to reconfigure the delay line into a ring oscillator by connecting its input to output through a switch, labelled as 6 in figure 3.1.
5. digital circuit to control the various switches, labelled as 2 in figure 3.1.

The full delay line is composed of a number of sub stages. Shown in figure 3.1 is just one such sub stage. The primary delay element in the delay line is a current starved buffer, which is made up of two current starved inverters. This delay element, labelled as 4, produces the required delay needed by a particular sub-stage of the the delay line. The current through

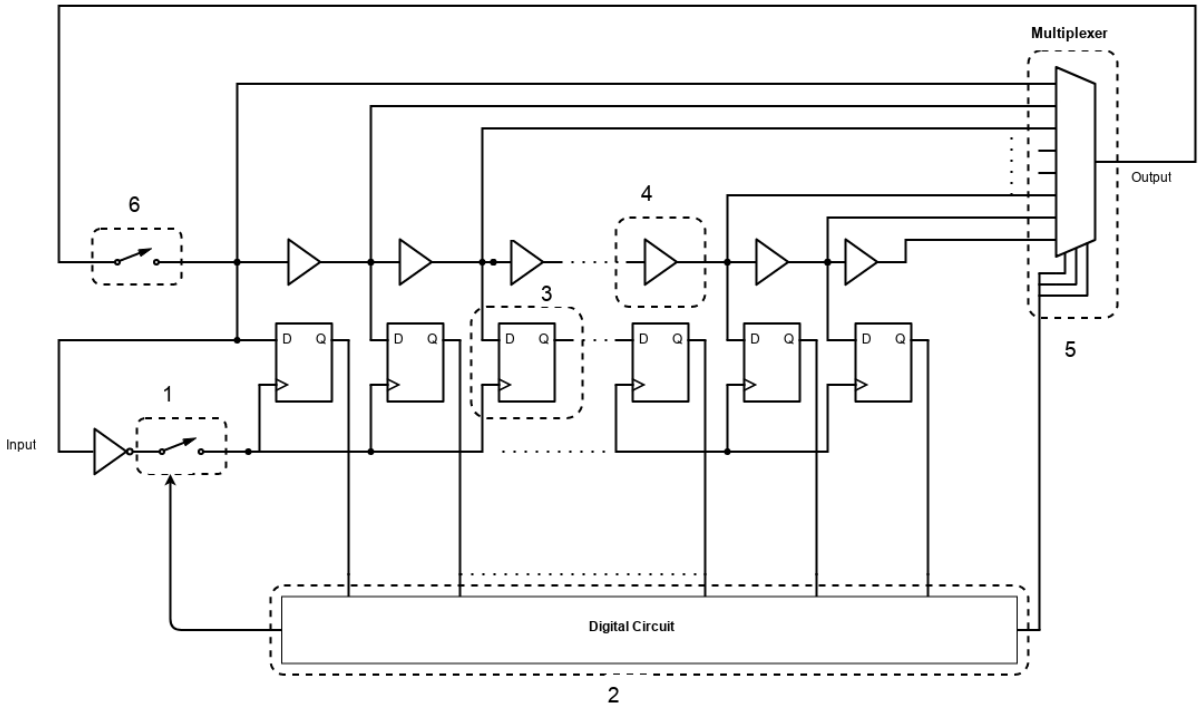


Figure 3.1: Block diagram of one sub-stage of a delay line

the buffer is set according to how much delay is needed, and it is set at design time. The required delay depends on the resolution required for that sub-stage of the delay line.

The delay of this delay line can be reconfigured and matched to be equal to the period of a reference signal that is applied to it at the node labelled as 'input' in figure 3.1. This is done by using a chain of flip-flops, one of which is labelled as 3. As shown in figure 3.1, a switch (labelled as 1) is initially open to prevent the first rising-edge from the input from triggering the flip flops. This is to ensure that the first edge is only used to propagate a signal through the delay line. As the first rising-edge propagates through the delay line, the digital circuit closes the switch 1. Therefore, the next rising-edge from the input will trigger all flip-flops at the same time. The output from the flip-flops would then contain information about how far the signal travelled through the delay line from the first rising-edge to the second (half period delay can be matched by making the flip-flop negative edge triggered). The digital

circuit, labelled as 2 in figure 3.1, has as a priority decoder that takes in a **thermometer code** that would be produced by the chain of flip-flops and output a multiplexer control code that would select the internal node in the delay line that most closely matches the period of the input signal. That way, the output of the multiplexer will be set such that the delay from the input of the delay line to the output of the multiplexer is equal to the period of the input signal to within the resolution of the delay line. The clock to the digital circuit is an inverted version of the same amplified crystal ringing response so that it does not need a separate clock source. The output of the multiplexer can then be passed to a finer sub-stage to produce more precise delays. Once the delay of the delay-line has been configured to match that of the input reference signal, the switch 6 can then close the loop and reconfigure the delay line into a ring oscillator. Note that as each delay element in the delay line itself is non-inverting, an inverter is needed in the feedback path. Since the total delay of the delay-line had been matched to the input reference signal, the ring oscillator will oscillate at half the input frequency.

To match the delay of the input signal, there are two possibilities: the delay of the delay-line can be matched to the period of the input signal or it can be matched to half the period of the input signal. The delay line is to be reconfigured as a ring oscillator and the frequency of the delay line is given by equation 3.1.

$$f_{osc,ring} = \frac{1}{2 * D * N} \tag{3.1}$$

Where $D$ is the delay of one delay-element in the ring oscillator and $N$ is the total number of delay-elements. So $D_{total} = D * N$ would correspond to the total delay of all the delay elements in the ring oscillator. In order to make sure that when the delay line is reconfigured as a ring oscillator it oscillates at the frequency of the input signal the delay line's delay must be matched to half the period of the input signal such that $D_{total} = \frac{T_{input}}{2}$ and :

$$f_{osc,ring} = \frac{1}{2 * D_{total}} = \frac{1}{2 * \frac{T_{input}}{2}} = \frac{1}{T_{input}} = f_{input} \tag{3.2}$$

where $T_{input}$ is the period of the input signal and $f_{input}$ is the input frequency. However,

matching the delay of the delay line to half the period of the input signal will make the system very susceptible to duty cycle variations in the input. This can, for example, be caused by offsets in the front-end amplifier. In order to remedy this problem, this work matches the delay of the delay line to the full period of the input signal and then doubles the frequency using XOR gate. This is done by XOR-ing the signal from the output of the ring oscillator with an internal node of the ring oscillator that has about half the delay compared to the full ring oscillator. This is shown in 3.2 for a input rising edge at time t = 0.

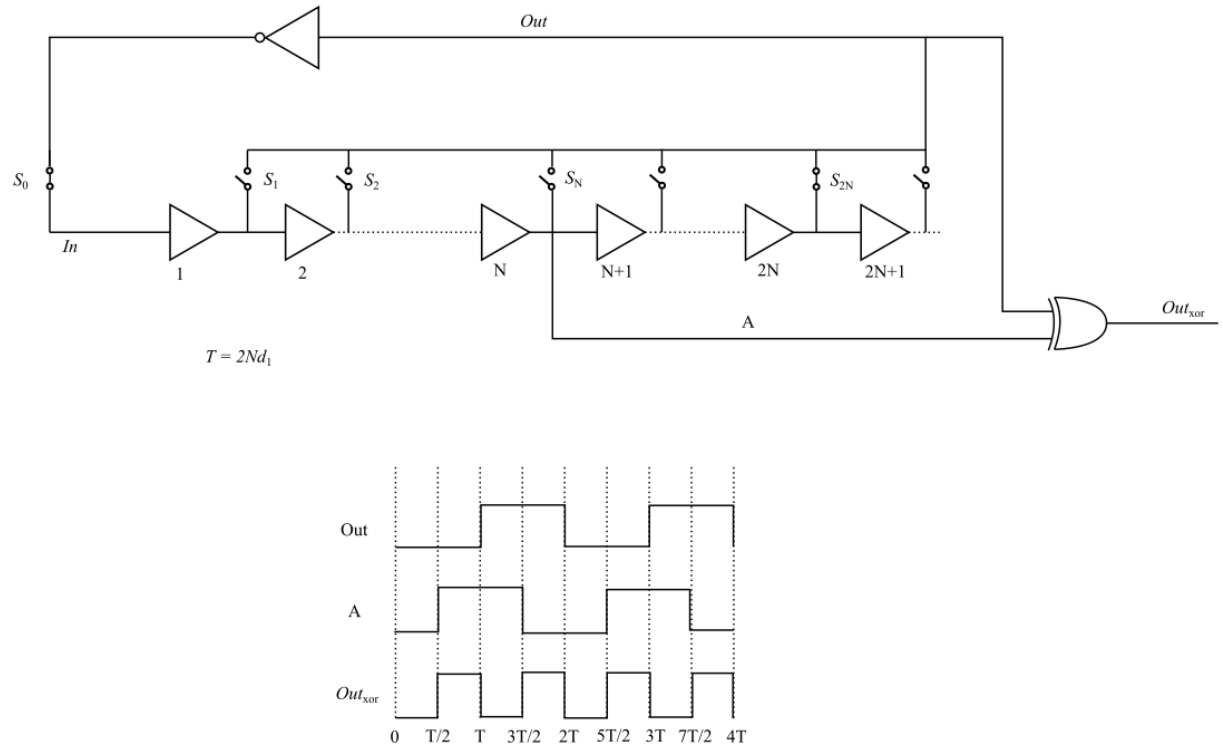


Figure 3.2: Frequency doubling

# CHAPTER 4

# Automatic calibration of injection frequency

This chapter describes a method for automatically adjusting the frequency of an injection oscillator to match the crystal resonance frequency very closely. This is done before starting the crystal oscillator, by observing the ringing response of the crystal (or high-Q) resonator to a voltage step and adjusting the frequency of an injection oscillator to match that of the ringing response. The adjusted injection source is then used to energize the crystal according to the precisely timed injection technique presented in [1] and [3].

## 4.1 Voltage Step Response of a Crystal

This work aims to extract the crystal's resonant frequency information from its step response so it is important to understand how a crystal responds to a voltage step. When a voltage step of value $V_{step}$ is applied across a crystal, the equivalent electrical model of the crystal, as shown in figure 4.1, tells us that a sinusoidal ringing motional current will be produced. Through analysis (given in section 7.1), it can be shown that the initial amplitude of the motional current, $|I_m|_{peak}$ and the its ringing frequency, $\omega_m$ will be equal to:

$$|I_m|_{peak} \approx V_{step}\sqrt{\frac{C_m}{L_m}} \tag{4.1}$$

$$\omega_m \approx \frac{1}{\sqrt{L_m C_m}} \tag{4.2}$$

The approximations are made based on the fact that the Q of the crystal is really high. As an example, consider the 10 MHz crystal from TXC, 7M-10.000MAHV-T . The typical

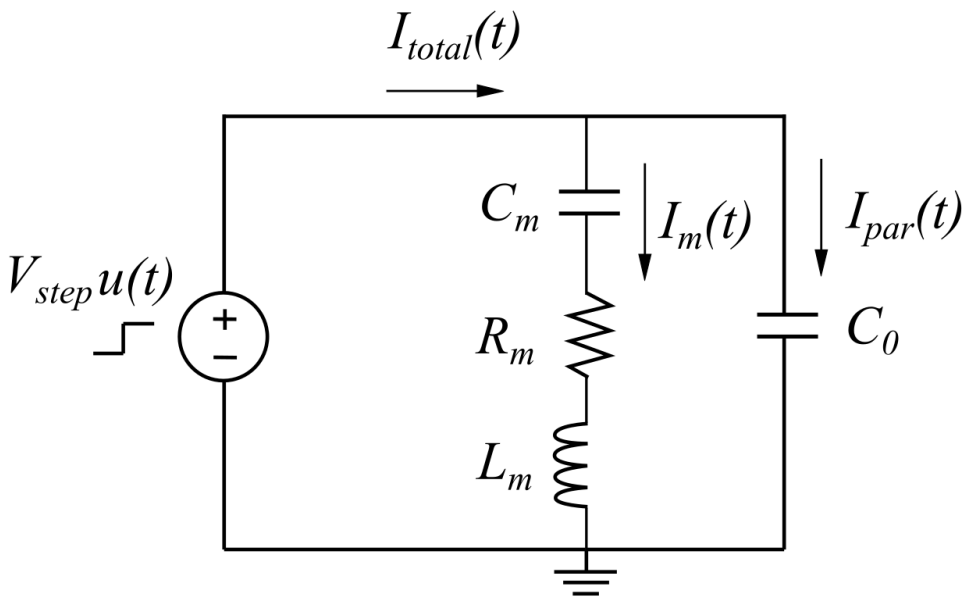


Figure 4.1: Schematic of voltage step applied to a crystal

values for this crystal, as given in its data sheet, are $R_m = 100$, $C_m = 10fF$, $L_m = 25.3mH$, and $C_0 = 5pF$. Based on these numbers, if a step voltage of 1V is applied to this crystal, it will produce a ringing motional current response that will start at an amplitude of $628.7nA$ and will then die down slowly. MATLAB simulation for the step response of the transfer function of TXC, 7M-10.000MAHV-T is shown in Figure 4.2.

There are two properties of this ringing response that are useful for this work:

- The frequency of the ringing current response is very close to the series resonant frequency of the crystal. This is due to the high-Q of the crystal.
- The amplitude of the ringing current decays very slowly. This is again due to the high-Q of the crystal. That is, the energy lost in $R_m$ in each oscillation is significantly lower than the energy stored in $L_m$.

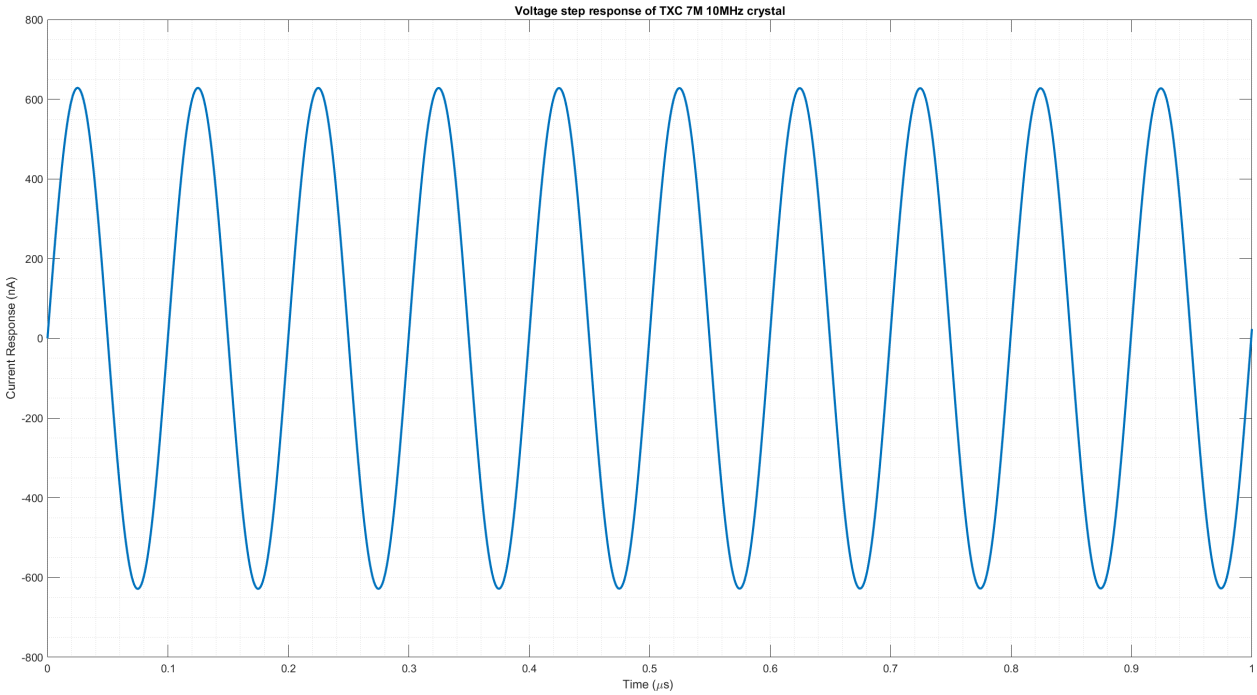


Figure 4.2: MATLAB simulation for the step response of the transfer function of TXC, 7M-10.000MAHV-T with a voltage step of 1 V

However, the above discussion is limited to the *motional current* in the crystal. The actual current that is flowing out of the terminals of the crystal (and as such the only current that can be detected by external circuitry) is the sum of the motional current *and* the current flowing through the parasitic capacitance path ($C_0$ in Figure 2.1). To analyze this total current, we can consider the following key points:

- A large current will flow through the crystal's parasitic capacitor, $C_0$, in response to the voltage step. However, that current will only flow *while* the voltage is changing, and as such it will flow for a very short time.

- Due to the very high-Q, the motional branch can be *treated as a sinusoidal current source* for the first 10s of cycles.

- Any external circuitry that is connected to the crystal in order to detect its ringing

current response will present some resistance. That resistance and the crystal's parasitic capacitor, $C_0$, form a low pass filter. As such, any analysis done on an amplifier used to detect this current must take into account the effect of this low pass filter.

## 4.2 Proposed System overview

A simplified block diagram of the complete system is shown in 4.3. Only the frequency matching system is shown here - the pierce oscillator is excluded. Broadly, the system has the following three parts: 1) A trans-impedance amplifier TIA to amplify the step response of the crystal, 2) A re-configurable delay line/ring oscillator to match the frequency of the amplified ringing response and 3) a digital block to control the various switches. The system starts powered down - the oscillator is turned off and both terminals of the crystal are grounded. When the start signal is received, the following steps are executed:

1. Apply a voltage step to the crystal.
2. Use a TIA to amplify the ringing current response of the crystal.
3. Within 10 cycles, match the delay of a delay line to the period of this ringing response. Turn off the TIA when this matching is complete.
4. When period of the delay line has been matched to a reasonable accuracy, reconfigure the delay line as a ring oscillator.
5. The reconfigured ring oscillator will oscillate at half the resonant frequency of the crystal. Double this frequency using a XOR gate and use this to energize the crystal.
6. Energize the crystal for a precisely calculated time as shown in [1].
7. After the required time, turn off the ring oscillator and reconnect the crystal to a pierce oscillator. The oscillator will now startup very quickly with out the need for calibrating the ring oscillator before hand.

The above steps will now be explained in detail. Presented in Figure 4.3 is the overall block diagram of the system. It consists of an amplifier, a delay line and digital circuit (per block details given in a later section). The crystal starts with a 0 V differnetial voltage across it.

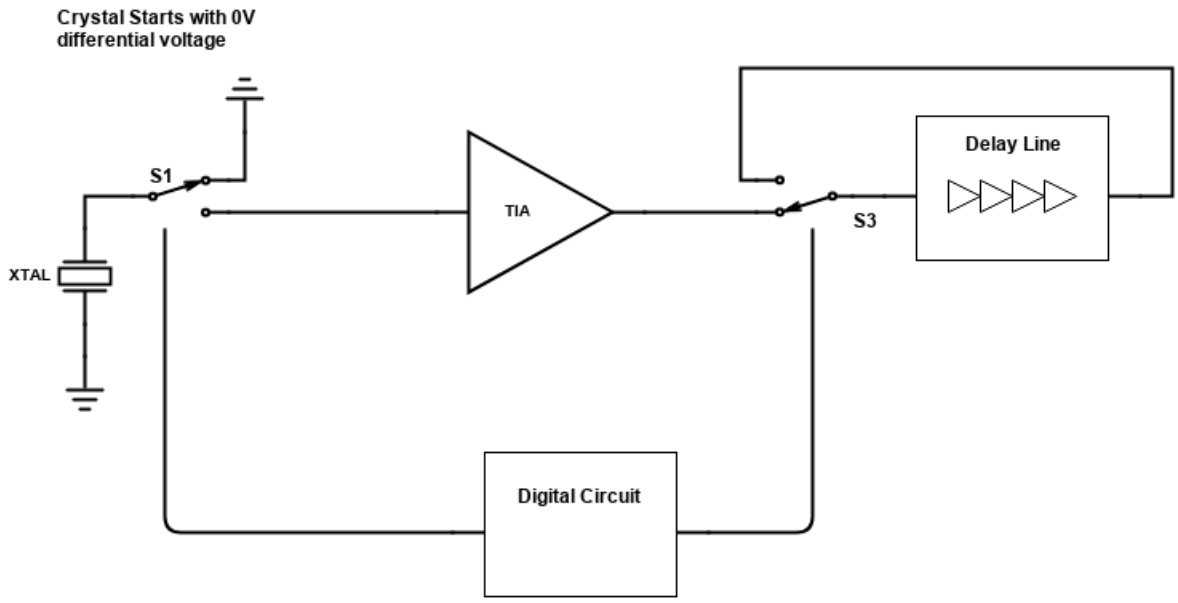


Figure 4.3: Step 1: Crystal starts at zero differential voltage and is not oscillating or ringing.

Then, as depicted in Figure 4.4, a start signal connects the crystal to the input terminal of a TIA, thereby applying a voltage step. This voltage step will be equal to the input common mode voltage of the TIA. As a result of this voltage step, the crystal responds by producing a sinusoidal current that rings at the crystal's resonant frequency. Due to the high Q of the crystal, this response decays very slowly. The sinusoidal ringing response of the crystal is amplified with a TIA that has been designed to keep the noise and jitter low. Timing jitter will create error in delay of the locked delay-line described below. The TIA is designed to

keep rms jitter to less than about 0.1% of the crystal resonance period.

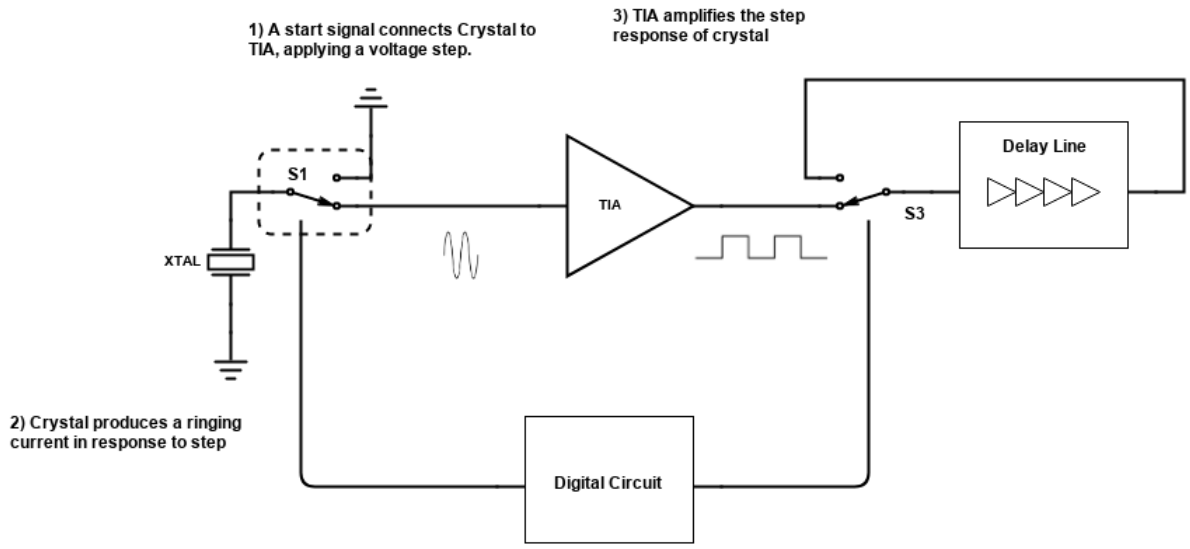


Figure 4.4: Step 2: A voltage step is applied across the crystal. This produces a ringing current.

Next, as depicted in Figure 4.5, this amplified signal is used to configure a delay-line such that the delay-line's delay is equal to the period of the amplified signal from the crystal.

Finally, as depicted in Figure 4.6, once the delay of the delay line is matched as per the above method, the delay line is reconfigured as a ring oscillator that oscillates at half the crystal's resonant frequency (with a resolution determined by the last stage of the delay line). This frequency is doubled using a XOR gate. The output of this configured ring oscillator is then used to energize the crystal to achieve quick startup of the crystal oscillator circuit.

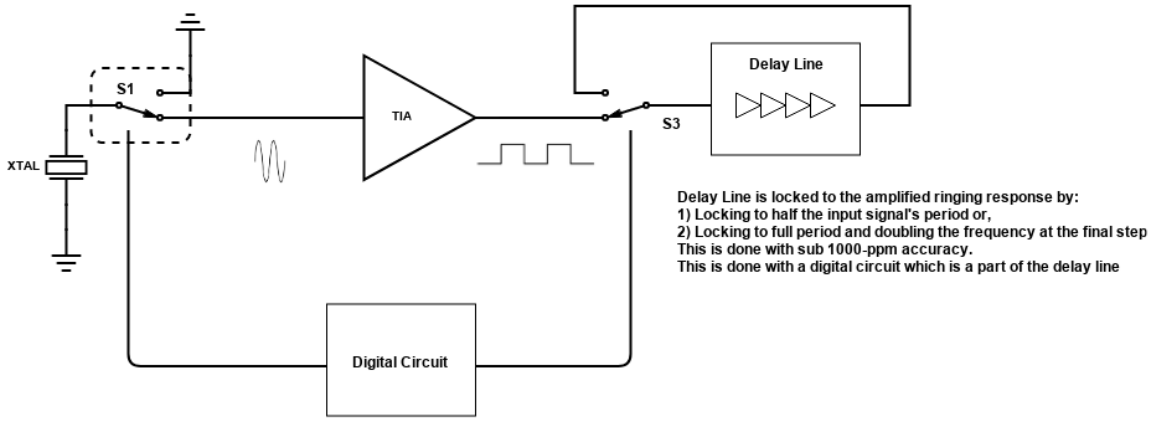


Figure 4.5: Step 3: The amplified ringing response is used to match the delay of a delay line to the period of the ringing response

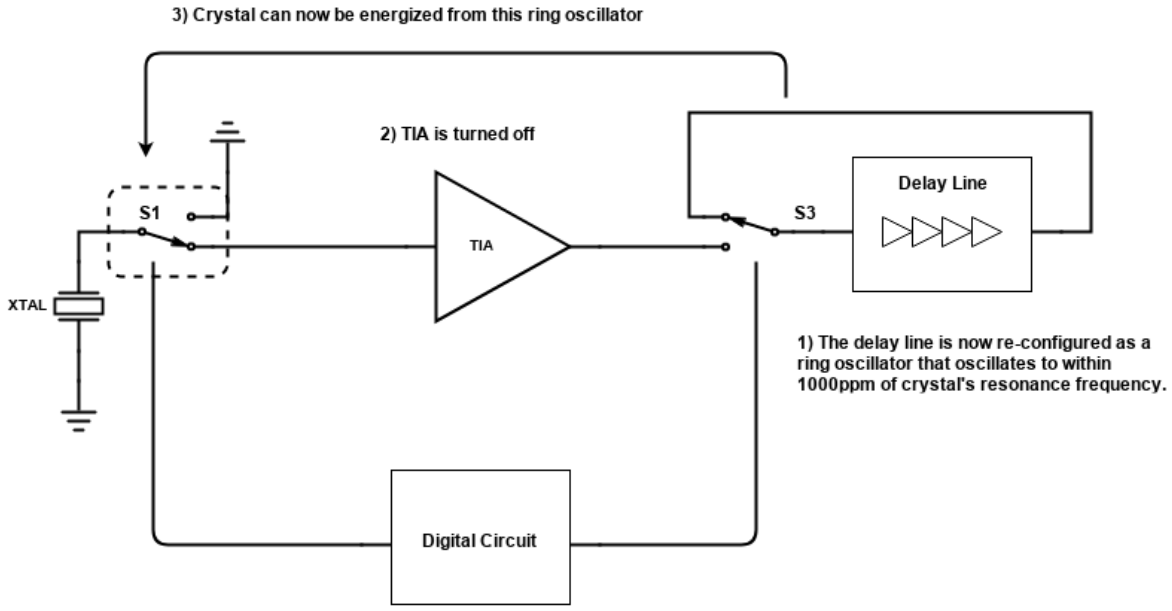


Figure 4.6: Step 4: The delay line is reconfigured as a ring oscillator and is then used to energize the crystal

## 4.3 System Components

### 4.3.1 Front End Amplifier

The purpose of the amplifier is to amplify the small ringing current from the crystal and to make it usable as a reference signal to match the delay of the following delay line. The requirements from the front end amplifier are as follows. The amplifier must be able to amplify the ringing current of the crystal and provide a voltage signal. As such, a TIA will be logical choice for this amplifier. Secondly, the amplifier must have low noise. The exact requirements on the noise is dictated by the jitter requirement of the injection signal. The jitter requirement is in turn determined by the target crystal frequency. As an example, in this work, a 10 MHz crystal is targeted. This frequency corresponds to a period of 0.1us and the target rms jitter is set to 100 ps (corresponding to a 1000 ppm frequency error). With this rms jitter, 99% of startups will be within 3000 ppm of the target frequency. So for the 10 MHz system targeted towards TXC, 7M-10.000MAHV-T in this work, the amplifier must be able to amplify a input current signal as small as 400nA with jitter as low as 100ps. The bandwidth must be at least equal to the resonant frequency of the crystal. Details of the implementation of the front end amplifier in 65nm TSMC technology are given later.

### 4.3.2 Delay Line and Ring oscillator

The reconfigurable delay line presented earlier is used to lock to the frequency of the input signal. With the amplified ringing response from the crystal as a reference, the delay along the delay line is adjusted so that it matches the period of the reference. Then, the delay line is reconfigured as a ring oscillator that oscillates at half the reference frequency (or equal to the reference frequency). The most important specifications of the delay line are it's range and resolution. The resolution is determined by the delay of the delay element in the delay line. For example, if the delay line has delay-elements with a delay of 100ps, the delay along the delay line can be changed by 100ps increments or decrements by adding or

removing some delay elements digitally. The range of the delay line is the maximum delay it can produce, and that is determined by the delay of the delay-elements times the number of delay elements. For example, since the 10MHz frequency targeted in this work requires 100ps resolution, the delay of the delay-element can be set to 100ps. However, in order to produce the 100ns range needed to capture the period of a 10MHz signal, $\frac{100ns}{100ps} = 1000$ delay-elements will be needed!

In order to get both the range and resolution needed with a reasonable number of delay-elements, the delay line is implemented as three separate sub-stages, each with finer resolution. A two sub-stage example is shown in 4.7. The first sub-stage is the coarsest, and it is what sets the range of the entire system. For example, a first stage with a per-delay-element delay of 8ns will need only $\frac{100ns}{8ns} = 13$ delay-elements. The next sub-stage has a finer resolution of 0.8ns. This sub-stage should have a range that can span the delay on *at least one delay-element of the previous stage*. The total delay along a delay line with three sub-stages is given by:

$$D_{total} = D_1N_1 + D_2N_2 + D_3N_3$$

Where $D_x$ is the delay of the delay element of the $x^{th}$ sub-stage and $N_x$ is the number of delay elements in the delay path of the $x^{th}$ sub-stage.

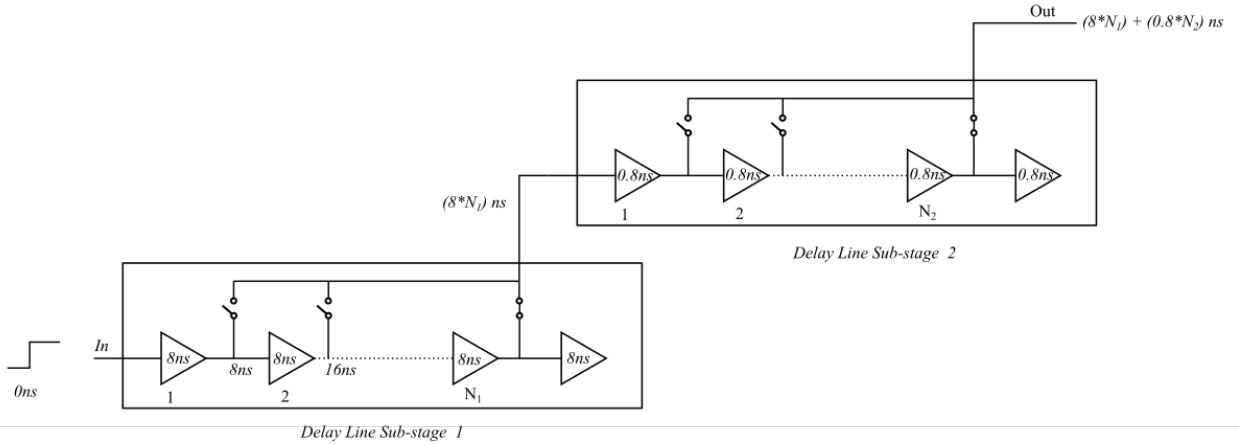


Figure 4.7: Example of a two stage delay line

### 4.3.3 Pierce oscillator and precisely timed injection

In this work, the pierce oscillator and the quick startup circuitry is derived from the technique described in [3] and [1] called precisely timed injection. Precisely timed injection relies on the fact that "the amount of energy injected into the crystal device is determined not just by the frequency of the injected signal, $\omega_{inj}$, but also, just as significantly, by the duration of injection, $T_{inj}$". As illustrated in Figure 2.3, there is a particular injection duration, $T_{inj} = T_c$, that results in the fastest start-up. The preferred injection duration, $T_c$, is the time it takes for the envelope of the driven crystal's motional current ($i_{X,env}$) to reach the crystal oscillator's eventual steady-state current amplitude, $i_{X,SS}$. For shorter (longer) $T_{inj}$, upon disengaging the injection oscillator, the crystal's motional current, $i_X$, has to sluggishly build up (decay down) to the steady-state value resulting in long start-up times. The precise injection duration, $T_c$, can be shown (in [1]) to be:

$$T_c = \frac{2L_m.i_{X,SS}}{V_d}$$

where $L_m$ is the crystal's motional inductance and $V_d$ is the injection (ring) oscillator's drive amplitude.

The block diagram of the precisely timed injection quick start-up oscillator is shown in 4.8. The crystal oscillator is implemented in a pierce configuration. During start-up, after the automatic injection frequency calibration described in the earlier section, the reconfigured ring oscillator injects energy into the crystal through the buffer whose amplitude is set by the PTAT voltage source. This makes $V_d$ track $V_{X,SS}$ over temperature. By counting an appropriate number $N_c$ of full cycles of the ring oscillator, the timer connects the crystal to the ring oscillator (with in the frequency calibration block) for a fixed duration of $T_c$ during which the energy in the crystal builds up to its steady state value.

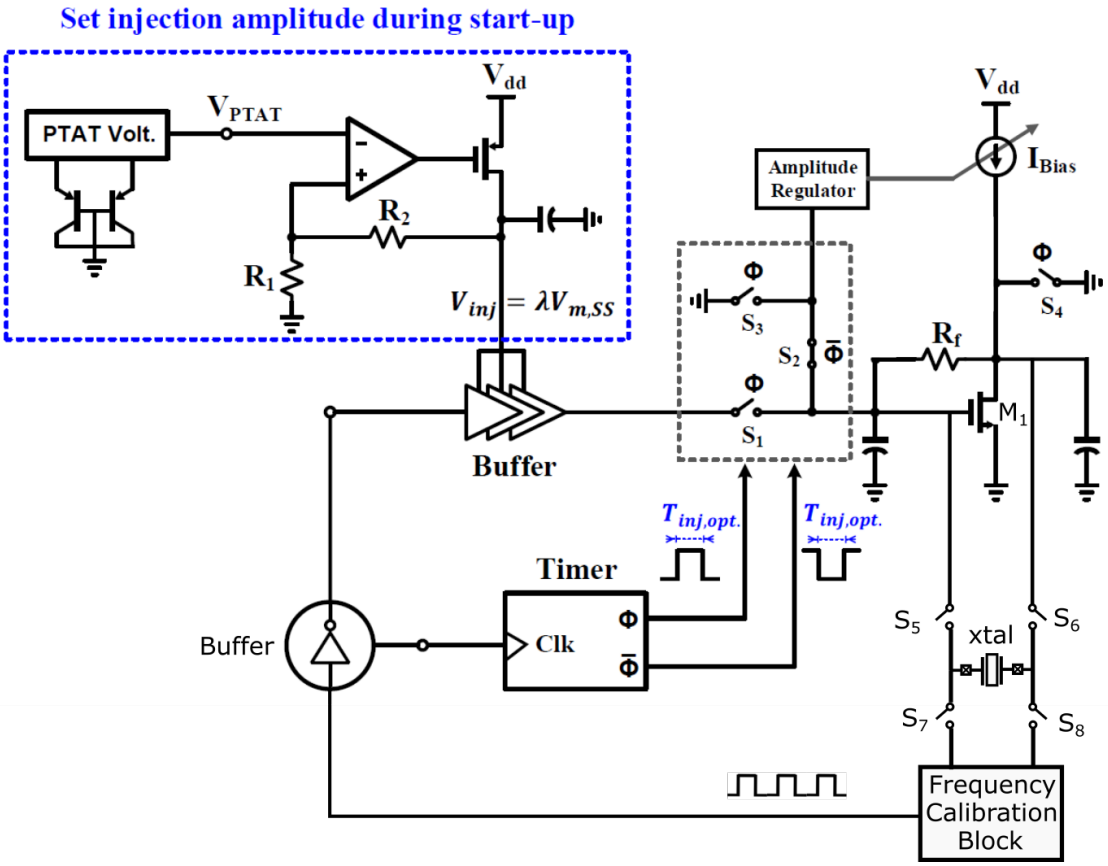


Figure 4.8: Block diagram of complete system

# CHAPTER 5

# Design and implementation

## 5.1 Front end amplifier

### 5.1.1 Overview

One way to amplify the current signal from the crystal is to pass it through a resistor and then amplify the resulting voltage using one or more amplifier stages. This is depicted in Figure 5.1 where initially, switch S1 is closed and S2 open to apply the voltage step to the crystal, and then the switches invert their positions to pass the current from the crystal through the resistor. Figure 5.2 shows the same circuit after the step has been applied, and without the switches and voltage source. The crystal has been replaced by its equivalent model on the left, with $Cm$, $Rm$, and $Lm$ being the motional capacitance, resistance, and inductance of the crystal respectively. $C_0$ is the parasitic capacitance. Since the current step response of the crystal decays slowly, it can be represented as a sinusoidal current source with a frequency equal to the resonant frequency of the crystal and the peak amplitude equal to $|I_m|_{peak} \approx V_{step}\sqrt{\frac{C_m}{L_m}}$, as explained in Chapter 3. This is the circuit shown on the right side of figure 5.2.

Using the approximation in figure 5.2, we can calculate the noise and jitter of this setup and see if it meets the requirements from this circuit. The first thing to consider is the bandwidth, determined by $R_1$ and $C_0$. The bandwidth should be greater than the crystal's resonant frequency, $f_m$, so:

$$BW = \frac{1}{2\pi R_1 C_0} > f_m \tag{5.1}$$

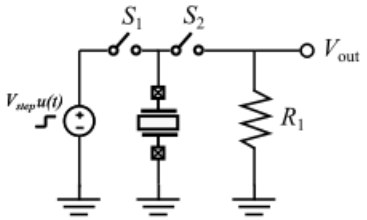


Figure 5.1: Application of a voltage step with a resistor, R1, to convert the current response to a voltage

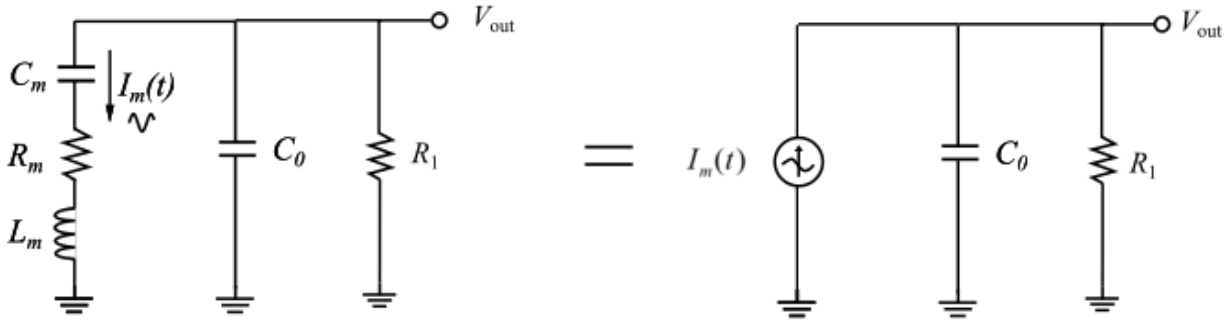


Figure 5.2: Equivalent model for a step response of a crystal with a resistor, R1, to convert the current response to a voltage

For the 10 MHz crystal targeted in this work, $Cm = 10fF$, $Rm = 100\Omega$, $Lm = 25.3H$ and $C_0 = 5pF$. These numbers and equation 5.1 gives an upper limit on the resistance value to be 3182 Ω. We can choose a resistance value of 1500 Ω to be within the required bandwidth. With $R_1 = 1500\ \Omega$, we can calculate the total noise and jitter presented by this circuit. The output RMS noise is given by equation 5.2:

$$V_{n,out,rms} = \sqrt{\frac{kT}{C_0}} \tag{5.2}$$

In turn, the RMS jitter (which is the ratio of the integrated output noise and the signal slope at threhold crossing) would be given by:

$$j_{rms} = \frac{\sqrt{\frac{kT}{C_0}}}{2\pi f_m |V_{out}|_{peak}} \tag{5.3}$$

Using the typical numbers presented earlier, the RMS jitter comes out to be 1ns, which is 10 times larger than what is required for a 1000 ppm accuracy. This is without even including the noise of the subsequent amplifying stages. As such, this simple solution can not be used. Increasing the resistance value here can reduce the jitter by increasing the amplitude of the output voltage swing, but this can't be done due to the bandwidth limitation. A solution to this problem is to use a amplifier arranged in a trans-impedance configuration, as shown in Figure 5.3.

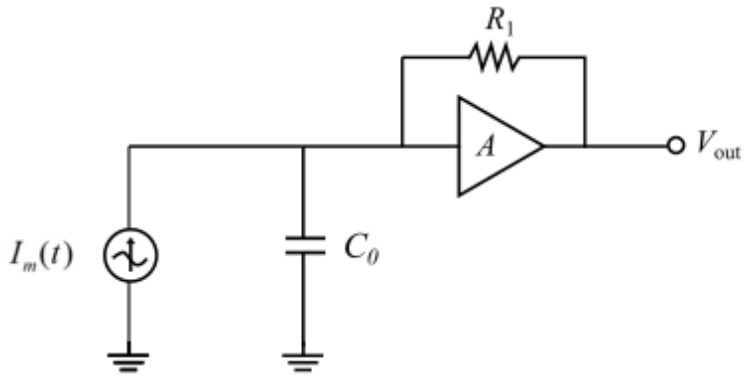


Figure 5.3: Model of a crystal, after application of a step response, connected to a TIA

The trans-impedance gain of the circuit, G, in 5.3 is given by:

$$G = \frac{A}{1+A}.\frac{R_1}{1+\frac{sC_0R_1}{1+A}} \approx \frac{R_1}{1+\frac{sC_0R_1}{1+A}}$$

Where the approximation is valid for large voltage gain, $A \gg 1$. We can see from this gain equation that the voltage gain also extends the input bandwidth by a factor of $1 + A$ by reducing the effective resistance seen by the current source. The limit on the resistance value is now more relaxed and is given by the following equation:

$$R_1 < \frac{1+A}{2\pi C_0 f_m}$$

The output noise (due to the resistor only) is now given by:

$$\overline{V_{out,n}^2} = \left[\frac{A}{1+A}\right]^2 \cdot \left[\frac{kT(1+A)}{C_0}\right] \approx \frac{kT(1+A)}{C_0}$$

Where the approximation is again based on the assumption of $A \gg 1$. The squared RMS jitter is given by the integrated output noise divided by the signal slope at the threshold, therefore:

$$j_{rms}^2 = \frac{\overline{V_{out,n}^2}}{(2\pi f_m I_{m,amp} G)^2}$$

Here, we can select the resistance to be $R_1 = \frac{1+A}{2\pi C_0 f_m}$, which is the largest resistance value allowed by the bandwidth limiting equation. This resistance value means that the bandwidth is equal to the input resonant frequency, so the effective gain will be scaled by a factor of -3dB (0.707). We can plug in this selected value of $R_1$, together with the equation for $V_{out,n}^2$ into the jitter equation. This results in:

$$j_{rms}^2 = \frac{\frac{kT(1+A)}{C_0}}{(2\pi f_m I_{m,amp} * \frac{1+A}{2\pi C_0 f_m} * 0.7)^2}$$

$$j_{rms}^2 = \frac{0.49kTC_0}{{I_{m,amp}}^2(1+A)}$$

Therefore with a TIA configuration, **jitter can be reduced by increasing the amplifier voltage gain**.

### 5.1.2 Design

Presented in Figure 5.4 is the final schematic of the front-end-amplifier. It consists of two stages - the first stage comprises of $M_1$, $M_2$, $M_3$ and $M_4$. $M_1$ and $M_4$ are the gain transistors and $M_3$ and $M_4$ are cascode transistors that are added to increase the voltage gain by increasing the output resistance by cascode ressitance boosting. $R_1$ is the self biasing resistor that biases this first stage as a TIA. $C_1$ is added for stability. Switch $S_1$-$S_4$ are used for the

| Component | W/L (um/um) | gm (mS) | gds (uS) |
|---|---|---|---|
| M1 | 114/0.360 | 7.7 | 362 |
| M2 | 280/0.30 | 10.9 | 441 |
| M3 | 72/0.3 | 10.2 | 296 |
| M4 | 36/0.36 | 6.9 | 536 |
| M5 | 7/0.3 | 0.40 | 10.3 |
| M6 | 7/0.3 | 0.40 | 10.8 |
| M7 | 5/0.130 | 0.660 | 18.5 |
| M8 | 5/0.130 | 0.660 | 19.4 |
| M9 | 3/0.120 | 0.815 | 140 |
| R1 | 145 K$\Omega$ – 250$K\Omega$ | | |
| C1 | 50 fF | | |

Table 5.1: Component aspect ratios and operating point parameters for the amplifier shown in Figure 5.4

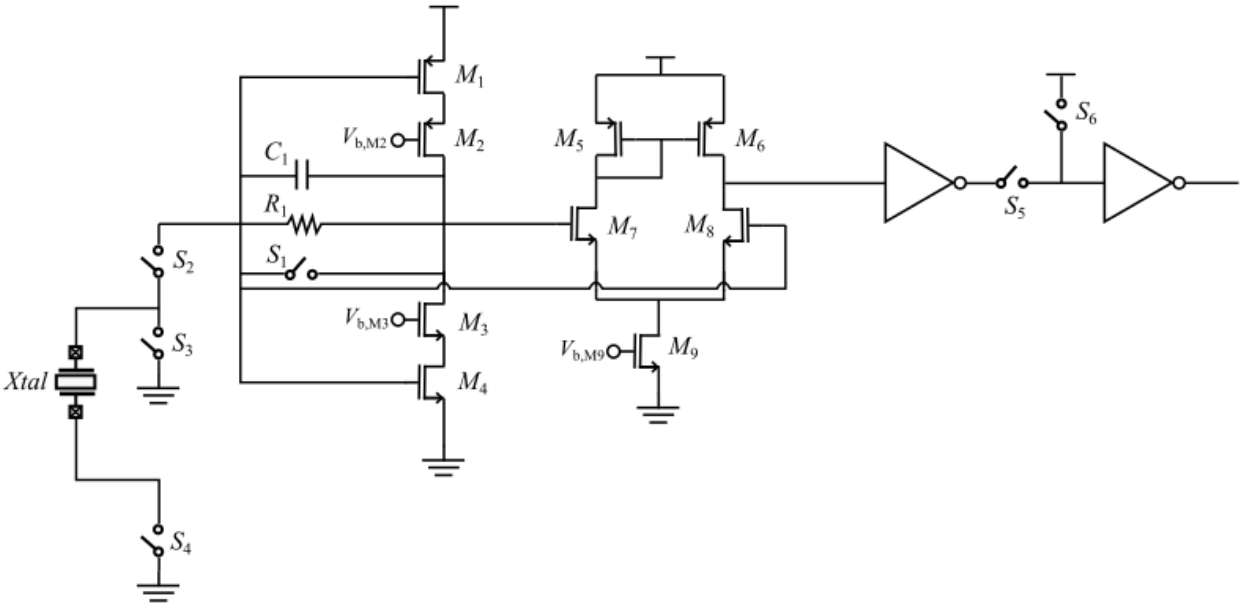


Figure 5.4: Schematic of the final TIA and second stage amplifier stage.

application of voltage step to the crystal. The control signals for these switches are generated by a separate, short delay-line circuit that switches $S_1$-$S_4$ (implemented as transmission gates) at the appropriate times.

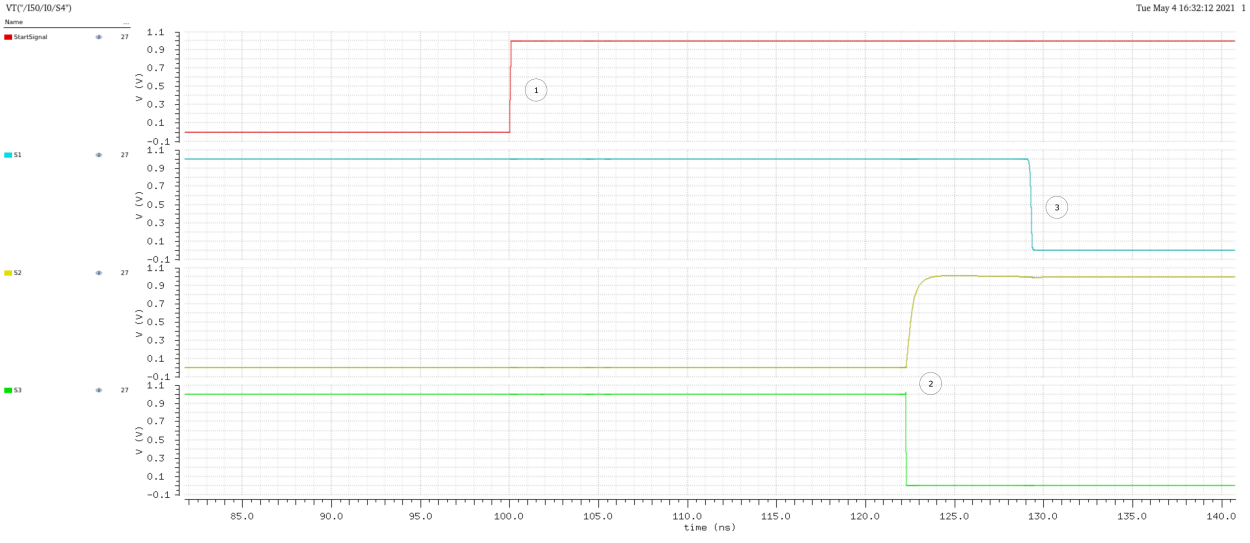


Figure 5.5: Switch triggering pattern for voltage step application.

Figure 5.5 shows the switch control signal pattern for the switches. A high value means that the switch is closed/shorted. At **1** in figure 5.5, a trigger signal is applied. This trigger signal turns on the amplifier circuitry, and allows some time, in between 20ns and 25 ns, for the amplifier to start up and settle. This settling is made faster by the fact that the switch S1 starts closed, and as such the input impedance presented by the TIA is very low. After this settling time, as shown as **2** in figure 5.5, switch $S_3$ is openend and $S_2$ is closed. As a result, one terminal of the crystal is now connected to the input of the amplifier and a voltage step equal to the input common mode of the TIA, which is nominally $\frac{Vdd}{2}$ is applied to the crystal. At this point, switch $S_1$ is still closed, so the input impedance presented by the TIA is low, allowing for a rapid step transition. Then, as shown as **3** in figure 5.5, switch $S_1$ now opens. This occurs after about 10ns of switch $S_3$ and $S_2$ transitioning, allowing enough time for the application of the voltage step. When $S_1$ opens, the gain of the TIA is now set by the resistor, $R_1$.

The second stage is a differential voltage amplifier. This amplifier does not limit the noise of the circuit, as most of the noise is determined by the first stage (owing to its very high gain). The purpose of this stage is to amplify the signal to a large enough value such that is reliably switches the following inverters. The input common mode for the second stage is $\frac{Vdd}{2}$ and is equal to the preceding TIA's output and input common mode. The second stage amplifies the signal **across** the preceeding TIA. This is because the input of the TIA swings only negligibly owing to its low input resistance and the low value of step current from the crystal. $S_5$ and $S_6$ are used to control the output of the amplifier, to disconnect is when it is off. The inverters at the end buffer the signal and convert the output into a square wave. Considering the first stage, the output impedance is given by:

$$r_{out} = ro_p||ro_n \approx \frac{gm_2}{gds_2.gds_1}||\frac{gm_3}{gds_3.gds_4} = 33K\Omega$$

where $ro_p$ and $ro_n$ are the output impedances of the PMOS and NMOS side respectively. The effective output resistance, $r_{out}$, using number from Table 5.1, is 33KΩ. Together with an effective gm of $(gm_1 + gm_4)$, the voltage gain of the first stage is:

$$A_V = (gm_1 + gm_4).(r_{out}) = 479 = 53.6dB$$

Since $A_V \gg 1$, the TIA gain is then given by:

$$A_{TIA} \approx R_1 = 250K\Omega = 108dB$$

The bandwidth, in turn, is determined by the input impedance of the first stage, the parasitic capacitance of the crystal, $C_p$, and the miller multiplied capacitance, $C_1 * (A_V + 1)$

$$f_{BW} \approx \frac{1}{2\pi.\frac{R_1}{A_V}.(C_p + (A_V + 1).C_1)} = 10.6MHz$$

The main noise contributing components in the first stage are the resistor, $R_1$, and transistors, $M_1$ and $M_4$. The resistor, $R_1$, noise transfer function to the output of the first stage is given by:

$$\frac{V_{out}}{I_n|_{R_1}} = \frac{sC_p + gm_{eff}}{(\frac{1}{r_{out}} + sC_L)(\frac{1}{R_1} + s(C_p + C_1)) + s(C_p + gm_{eff})(sC_1 + \frac{1}{R_1})}$$

Where $gm_{eff}$ is the effective gm of the first stage, $C_L$ is the capacitive load on the first stage amplifier, and the remaining parameters are as defined earlier. The MOS, $M_1$ and $M_4$, noise transfer function to the output of the first stage is given by:

$$\frac{V_{out}}{I_n|_{M_1+M_4}} = \frac{1 + s(C_p + C_1)R_1}{(\frac{1}{r_{out}} + sC_L)(\frac{1}{R_1} + s(C_p + C_1)) + s(C_p + gm_{eff})(sC_1 + \frac{1}{R_1})}$$

The derivations for the noise transfer functions are given in section 7.1. The MATLAB plots for the noise transfer functions are shown in 5.6. The RMS jitter value obtained from MATLAB is 108 ps.

### 5.1.3 Simulation Results

The simulated trans-impedance gain and bandwidth is close to the calculated values and are shown in AC smulation results in Figure 5.7.

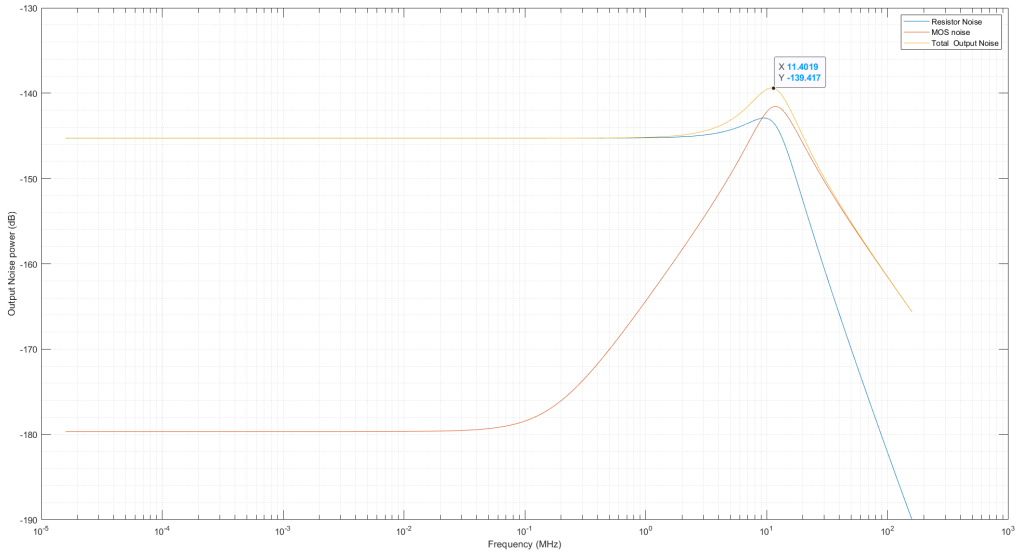


Figure 5.6: Amplifier stage 1 noise plots plotted on MATLAB with an integrated RMS jitter of 108ps

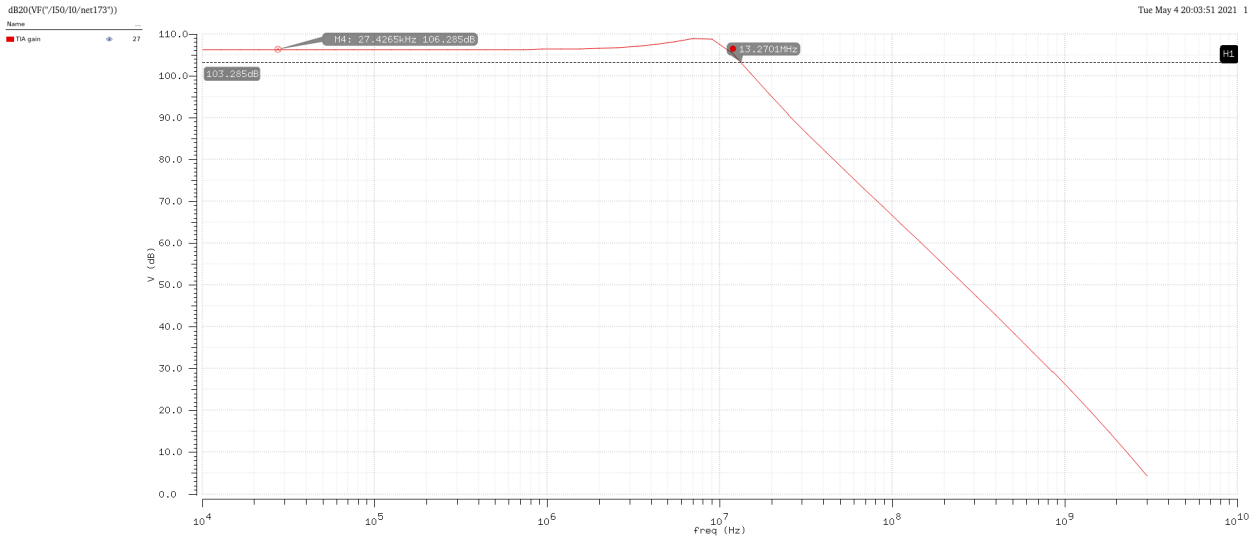


Figure 5.7: TIA simulated transimpedance gain

The simulated output noise of the first stage is shown in Figure 5.8 and matches what is expected from the MATLAB calculations of Figure 5.6. The total output jitter is also close

to what was expected from the integration of the noise transfer function on MATLAB, and is shown in Figure 5.9. The output jitter from PSS and PNOISE simuation is found to be 117.5ps. Note that the first stage was expected to add 108ps of jitter. After inclusion of all noise sources and amplifier stages, the final jitter is 117.5ps, showing that most of the jitter contribution is from $R_1$, $M_1$ and $M_4$ of the first stage.

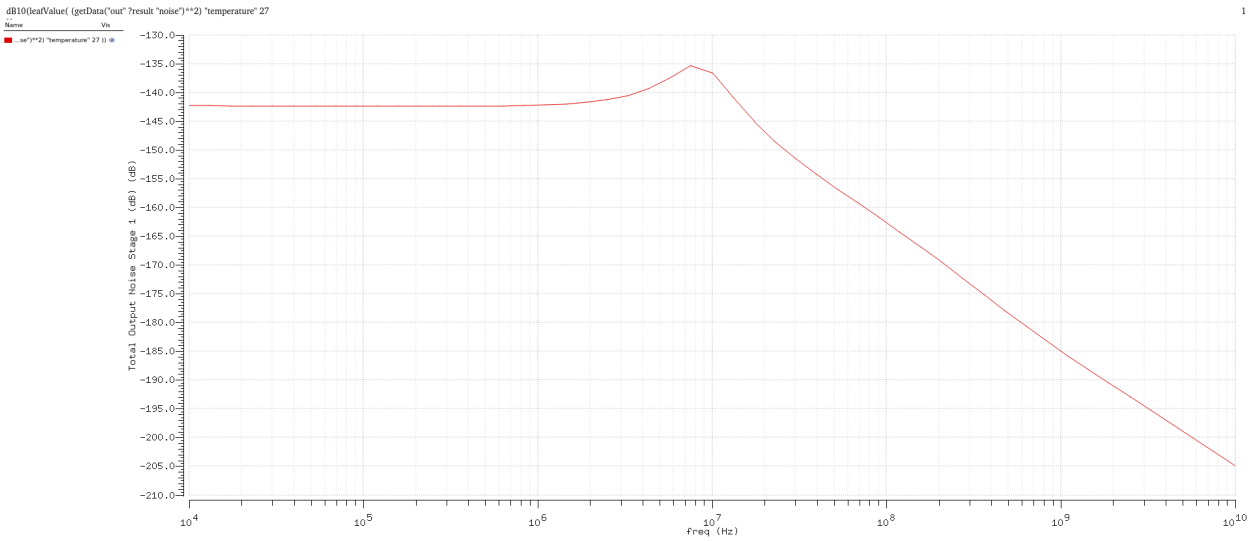


Figure 5.8: TIA total output noise

Shown in Figure 5.10 is the simulated transient output response of the complete amplifier when it is connected to a model of 10 MHz, TXC, 7M-10.000MAHV-T crystal, in presence of transient noise from 100Hz to 5GHz. The voltage waveforms at different points along the amplifier is shown.

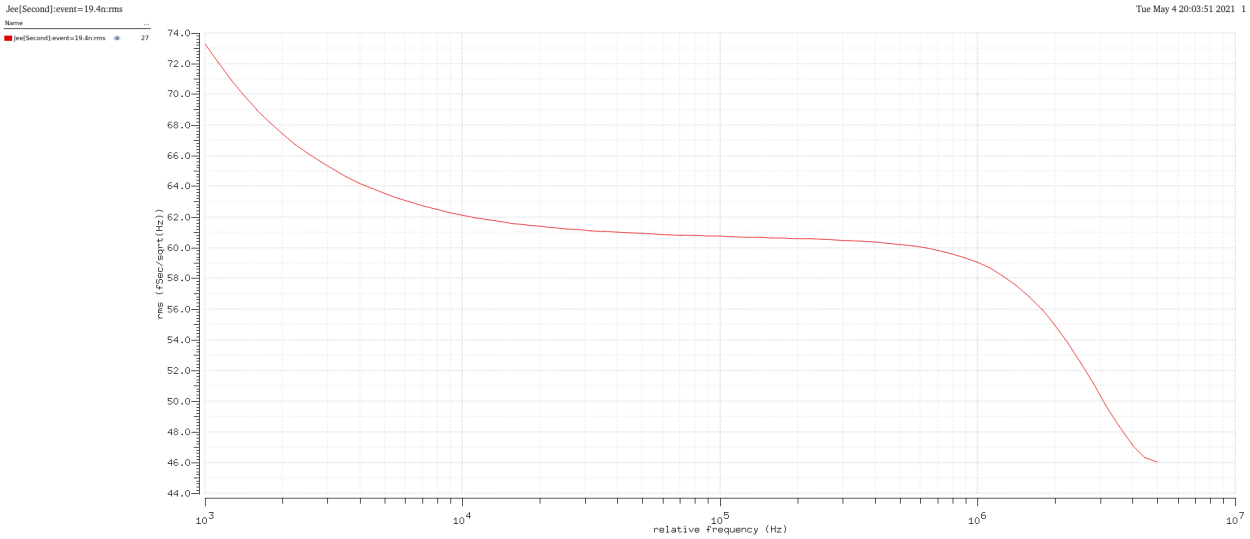


Figure 5.9: TIA simulated jitter gain, integrated rms jitter 117.5ps

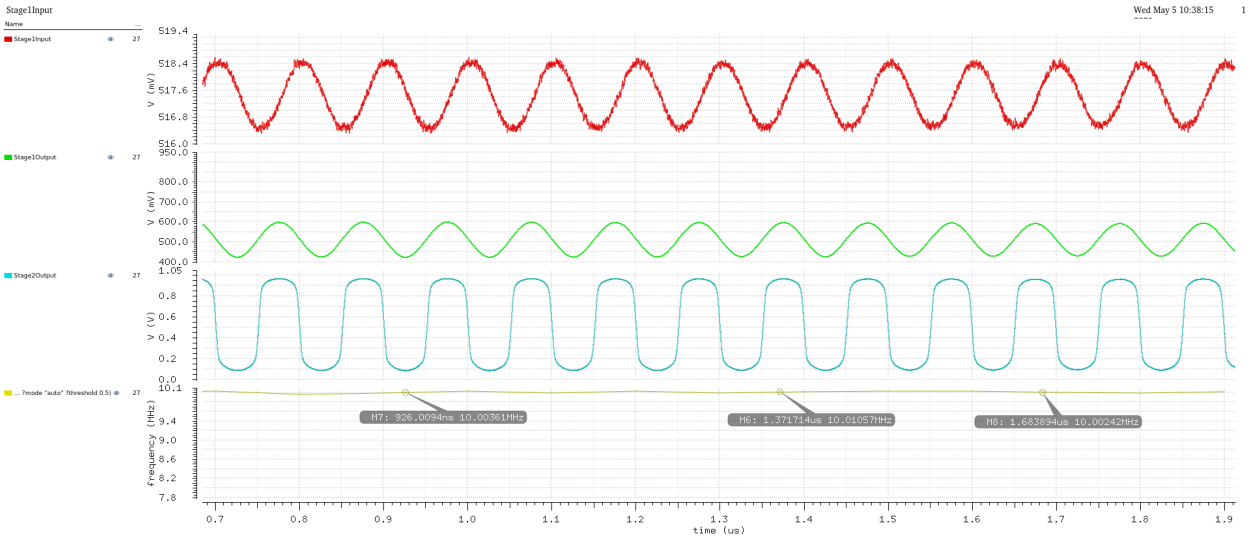


Figure 5.10: Simulated Transient Response of the TIA with a 10MHz TXC, 7M-10.000MAHV-T crystal model **with transient noise** from 100Hz to 5GHz. From Top to Bottom: 1) Input voltage at the TIA 2) Output voltage of the first stage 3) Output voltage of the second stage 4) Frequnecy of the output signal

## 5.2 Delay line and ring oscillator

### 5.2.1 Design

The block diagram of the delay line has already been explained in chapter 3. For the design in this work a 10Mhz crystal is targetted, which allows at most a 100 picosecond delay error in the driving signal to achieve a sub 1000 ppm accuracy. In order to get both the range and precision required, the delay line is implement in a three stage, course-fine-finer implementation. The delay-element delay of the first, second and third stage is set to be $8ns$, $800ps$, and $80ps$ respectively. The number of delay-elements and the delay per delay-elements for the first delay-line stage is such that it can produce a total delay of more than the period of the input signal. The resolution of the final delay-line stage sets the resolution of the overall system. Each successive stage has a total delay that is more than the delay of each individual delay-element of the last stage in order to ensure enough overlap. The delay numbers used for the 10MHz system are shown in 5.11. Since each delay line stage requires 2 cycles for locking, the three stages take 6 cycles to lock. More stages can be added for better accuracy at the expense of more time required for locking. After the locking is complete, the delay-line is reconfigured as a ring oscillator. However, since the delay of the delay-line is configured to be equal to the period of the input signal, the final frequency that the reconfigured delay-line ring oscillator will produce will be equal to half the resonance frequency of the crystal. A frequency-doubler is therefore required. The final frequency is doubled by using the output node and an internal node of the delay line connected through a XOR gate.

The delay element used in the delay line is a buffer made up of two current staved inverters as shown in Figure 5.12. By changing the starved current, I, and the load capacitances, $C_1$ and $C_2$, the delay of the buffer can be changed. This buffer is used in all three stages of the delay line, with different current values in order to produce the different delays required by the delay line stages.

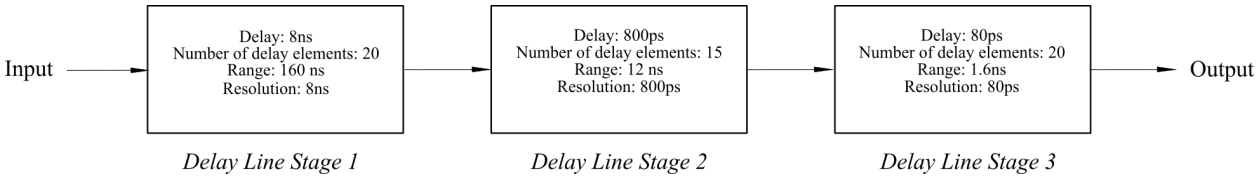


Figure 5.11: Delays, range, and resolution of each of the three substages of the total delay line for the 10 MHz system

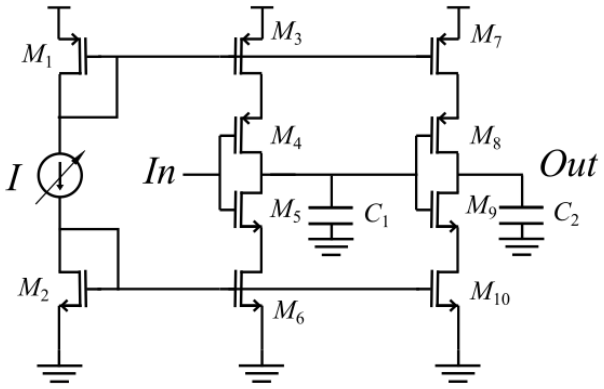


Figure 5.12: Current Starved buffer, the main delay element of the delay line

Presented in Figure 5.13 is the schematic of the multiplexer for an $N$ stage delay line. The nodes labelled $In < 0 >$ to $In < N - 1 >$ are the inputs of the multiplexer, i.e. the internal nodes of the delay line are connected to these nodes. The nodes, $ctrl < 0 >$ through $ctrl < N - 1 >$ is what controls the multiplexers output.

Before the delay line is 'locked', the digital circuit will open switch $S_2$ and close $S_1$ in all slices. Because of this, as the input signal propagates, the inputs will start to rise one by one. $In < 0 >$ will rise first, followed by $In < 1 >$ after a delay equal to the delay of the delay line's delay element, then $In < 2 >$ and so on. This rising will propagate in each slice, through $I_1$, $S_1$, $I_2$ and then the flip flop. The capacitance, $C_{dummy}$, is added for delay matching such that the capacitance at the output of $S_1$ is equal to the capacitance of the high fan-out output of $S_2$. This will ensure that the delay is the same in both the

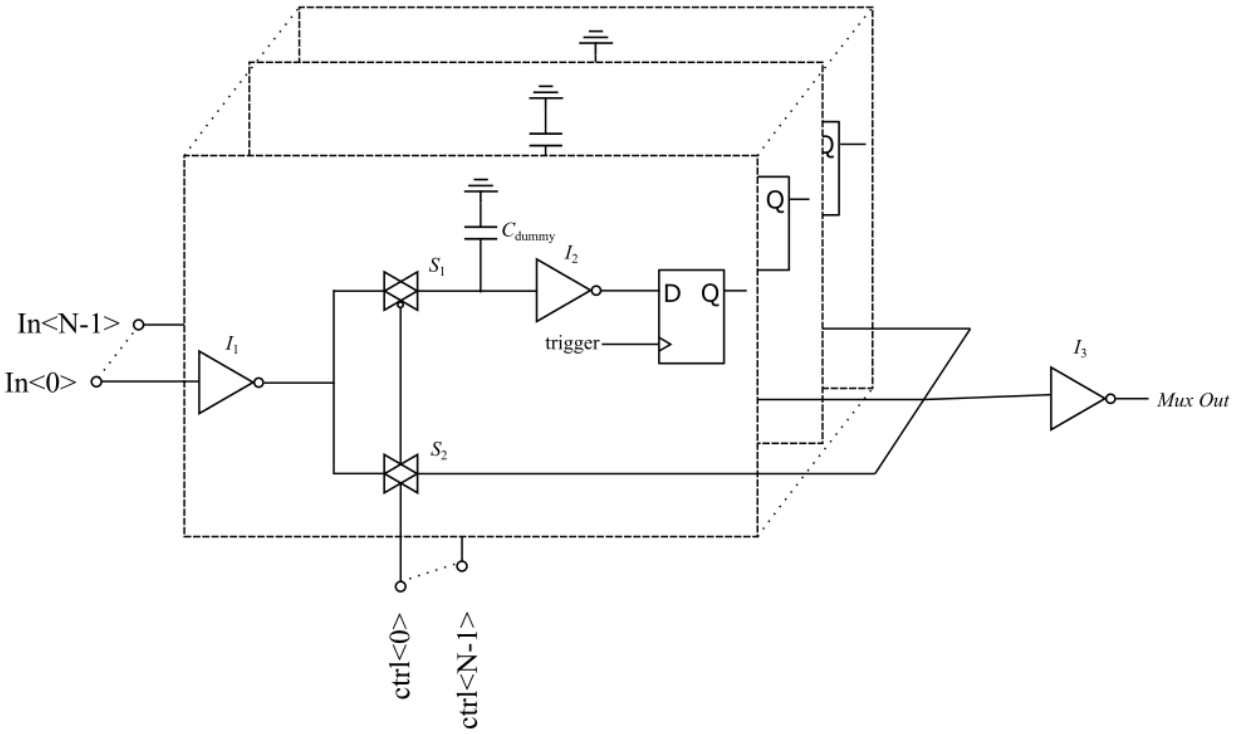


Figure 5.13: Delay matched multiplexer used for re-configuring the delay line

top and bottom path. This is essential as we do not want the delay to change after the multiplexer has switched. Each flip-flop in 5.13 is clocked by the same signal, labelled as *trigger*, which comes from the input signal itself. The first rising edge from the input only propagates through the delay line. This propagating signal also appears at the input of the flip-flops associated with the internal nodes of the delay line. The next rising edge triggers all flip-flops, and the output of the flip-flop then contains information about how far the signal has propagated through the delay-line. The output of the flip-flops goes to a digital circuit which sets the control signals of the multiplexer, so as to allow the multiplexer to pass the node that most closely matches the period of the input signal.

### 5.2.2 Simulation results

Shown in 5.14 is a simulation of the first stage of the delay line. Here, the delay of each current staved buffer is 5.2ns and the input signal has a frequency of 10MHz (100ns period). Therefore, we expect the signal to travel through $\left\lfloor \frac{100ns}{5.2ns} \right\rfloor = 19$ stages in one period. Here, we see that right before the second rising edge of the input, the output of the $19^{th}$ current-starved buffer of the delay line goes high, however the $20^{th}$ buffer's output is still low. This is latched onto the flip-flop due to the second rising edge of the input. The digital circuit then sets the mux to pass the $19^{th}$ node of the delay line to the output of the first delay-line stage. As a result, the delay set by the first stage of the delay line is $5.2 * 19 = 98.8ns$.

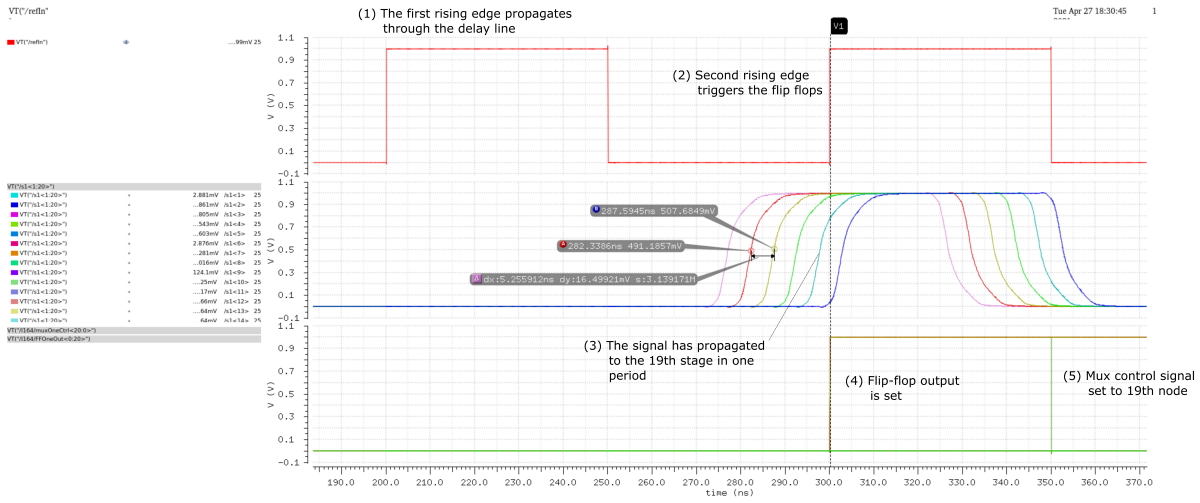


Figure 5.14: Simulation of stage 1 of the delay line

Shown in 5.15 is the output of the three stages of the delay line. On the top, in red, is the input reference signal. The three stages of the delay-line add more delay to the line until the delay matches that of the period of the input. At 0.8us, the delay line is reconfigured as a ring oscillator. As can be seen, the top (red) reference signal is turned off and yet the three stages keep oscillating at the same frequency as the reference signal. The locking occurs within 6 cycles.

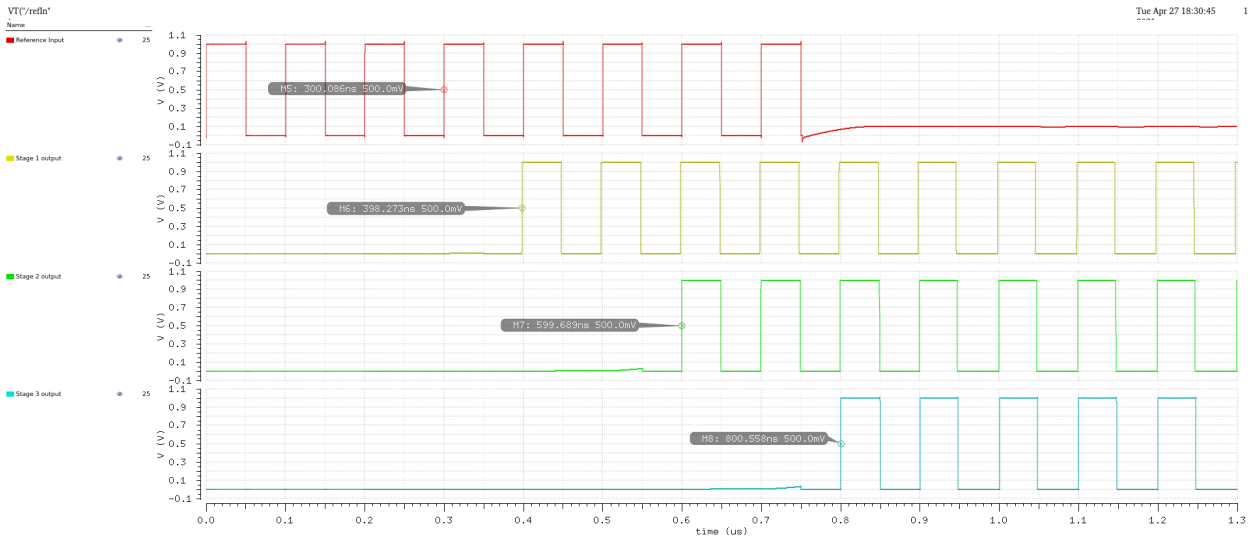


Figure 5.15: Simulation output of the three stages of the delay line

# CHAPTER 6

# Results and conclusions

## 6.1 Simulation Results

The complete system has been designed in TSMC 65nm technology (Layout shown in Figure 6.4). This section shows the simulation results and the next section deals with die measurement results.

6.1 shows some of the main signals from the system level simulation. On the top in yellow is the trigger signal that activates the system and starts the locking (label 1). The next trace in blue shows the differential voltage across the crystal and at label 2, a voltage step is applied across the crystal. Next, shown in red is the motional current through the crystal and as shown by label 3, the voltage step causes a ringing current response. The next trace in green shows the output of amplifier, and label 4 shows the amplified ringing response. At label 5, the amplifier turns off. The last trace shows the output of the delay line, and at label 6, the delay line is locked and reconfigured as a ring oscillator and starts producing an oscillating output. This is then used to energize the crystal which can be seen by the square wave across the crystal (blue trace) after 1.1$\mu$s and also by the ramp-up in the motional current (red trace) after 1.1$\mu$s.

Figure 6.2 shows how the motional current of the crystal grows in the full system. At 0.1$\mu$s, the trigger signal is applied. That causes a voltage step to be applied across the crystal, resulting in a ringing current response from 0.1$\mu$s to 1.1$\mu$s. Within this 1$\mu$s, the delay of the delay line is matched to the period of the crystal's period and then it is reconfigured as

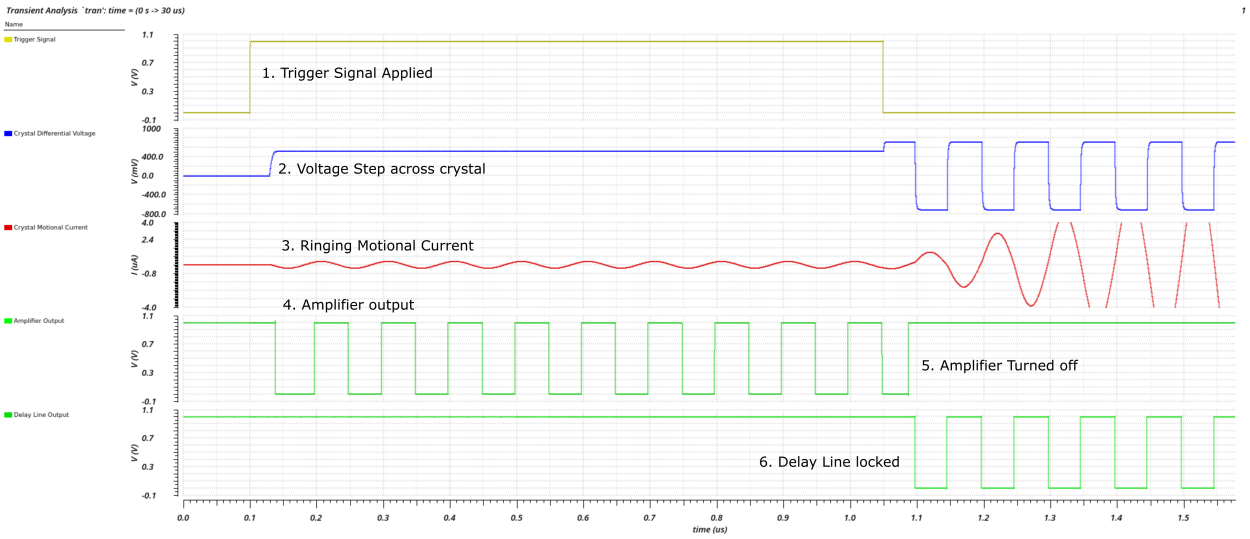


Figure 6.1: Automatic frequency calibration - Full system simulation

a ring oscillator. Starting from 1.1$\mu$s, the signal from this ring oscillator is used to energize the crystal. This energization can be seen by the motional current's rise from 1.1$\mu$s to 8.6$\mu$s. This 8.6$\mu$s is the injection time calculated according to [3]. Since the motional current envelope does not fall or rise after 8.6$\mu$s, it shows that the motional current has risen to it's steady state value in this time.

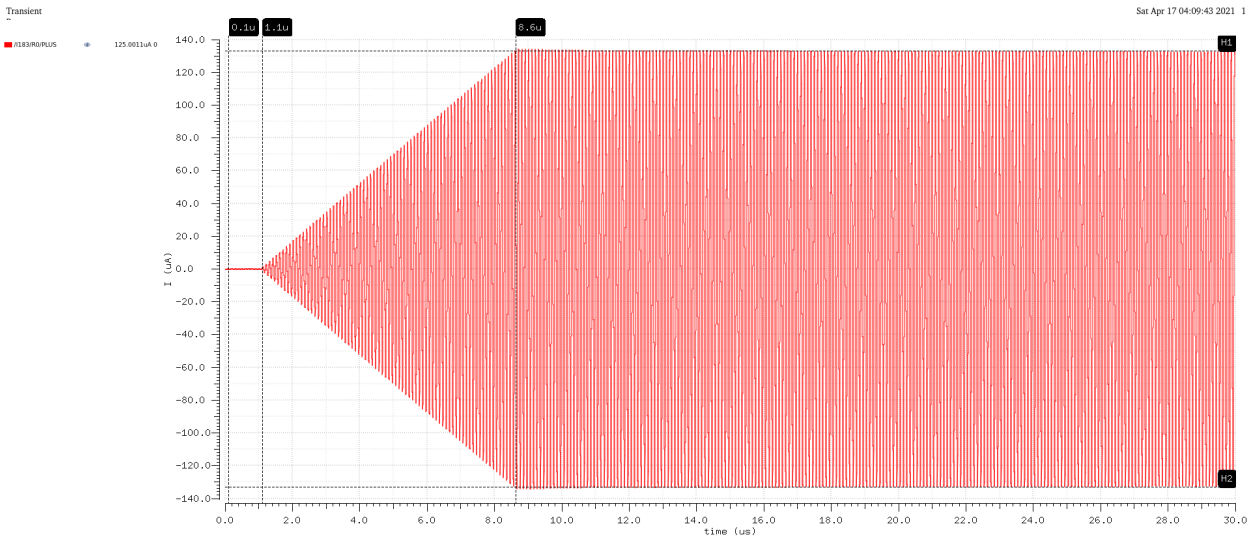


Figure 6.2: Crystal Motional Current - Full system simulation

| | $I_{avg}(\mu A)$ | Active Time ($\mu$s) | Energy (nJ) |
|---|---|---|---|
| Amplifier | 1500 | 0.95 | 1.42 |
| Delay Line | 236 | 8.5 | 2 |
| PTAT Regulator | 87 | 8.6 | 0.7 |
| Digital Circuit | - | - | 0.1 |
| Buffer | 1350 | 7.5 | 10.1 |
| Total | | | 14.32 |

Table 6.1: Simulated power consumption

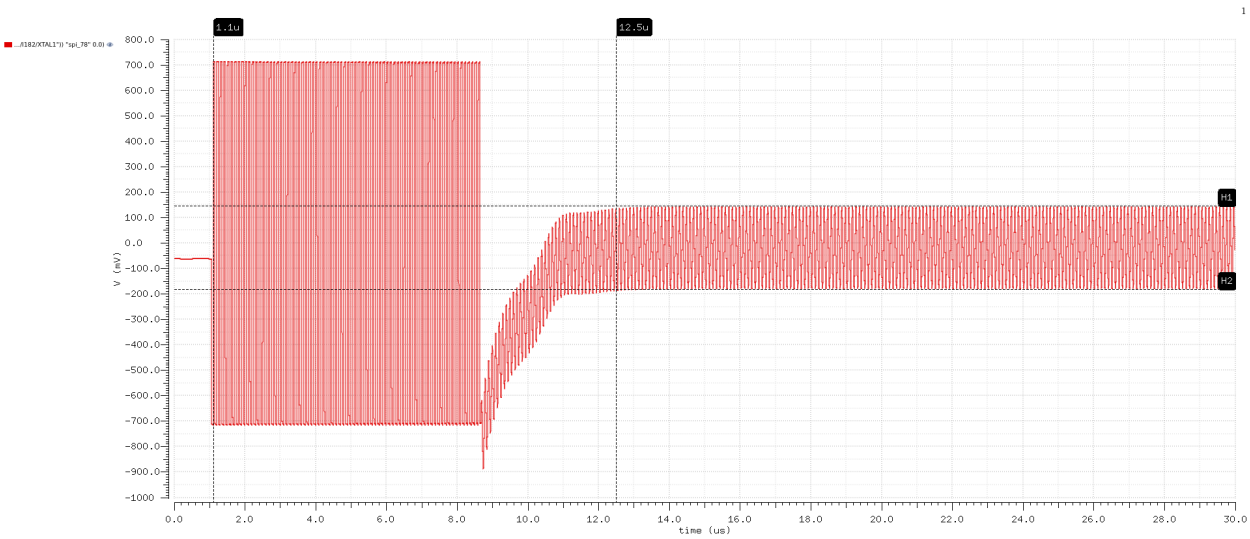


Figure 6.3: Crystal differential Voltage - Full system simulation

Figure 6.3 shows the differential voltage across the crystal. From 0.1$\mu$s to 1.1$\mu$s, the delay line is matched and reconfigured as a delay line. From 1.1$\mu$s to 8.6$\mu$s, the output of the ring oscillator is used to energize the crystal. This is shown by the ±700mV square wave. This ±700mV is generated by the PTAT voltage regulator. As can be seen, the startup time is a total of 124 cycles. There is only a 10 cycle overhead in order to lock the delay line and reconfigure.

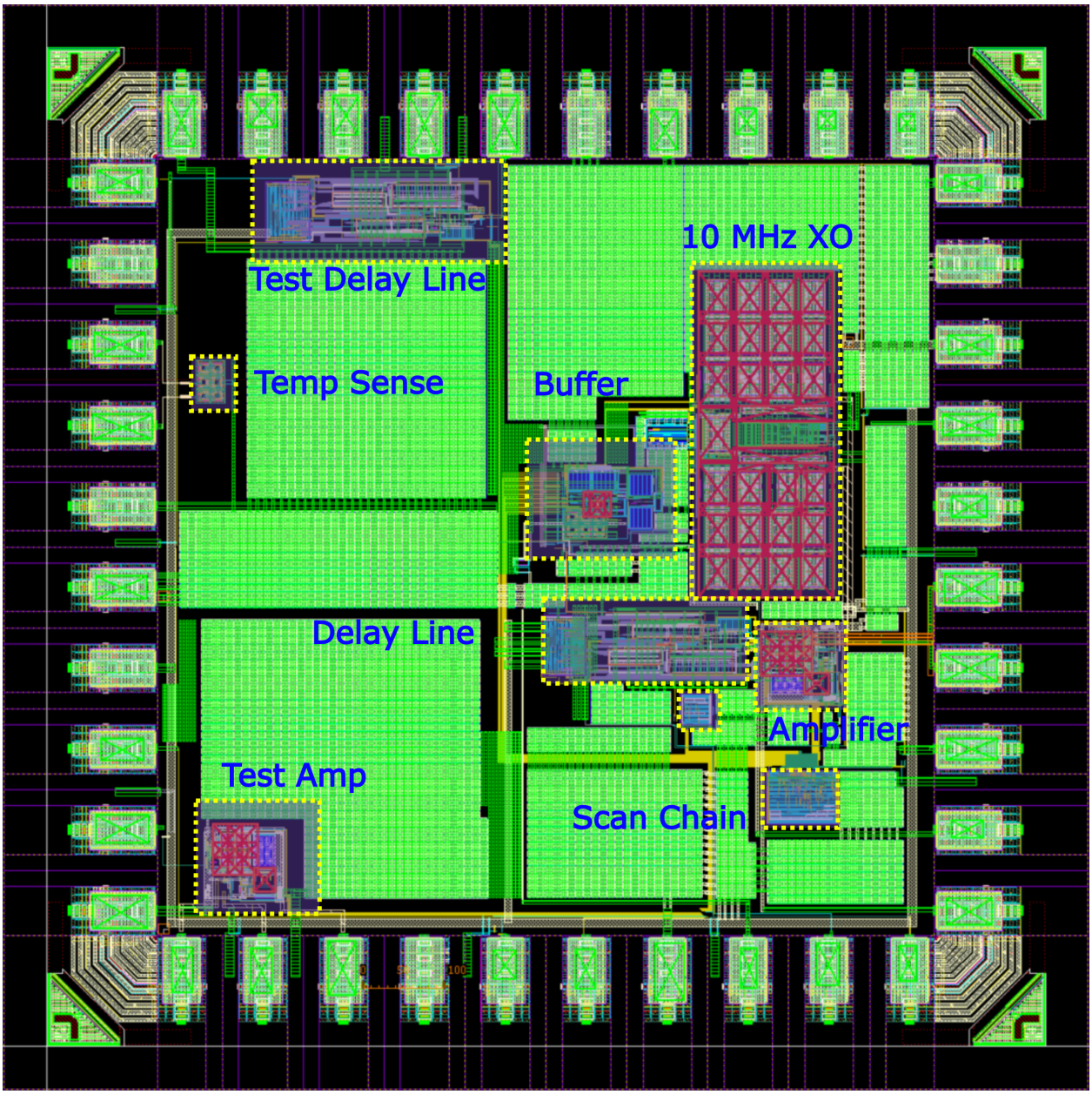


Figure 6.4: Chip Layout

Table 6.1 shows the simulated power consumption. As shown in the comparison in 6.1, this works achieves startup in 10 more cycles than in [1] while consuming and extra 2.32 nJ of energy. This work, however, does not require individual calibration of the injection ring oscillator. Compared to [8], this work achieves a roughly 3x better startup time, while

| | This Work* | [1] | [8] | [9] |
|---|---|---|---|---|
| **Technique** | Precisely Timed Injection with automatic frequency calibration | Precisely Timed Injection | Self Timed Injection | Impedance Guided Chirp Injection |
| **Technology** | 65nm | 65nm | 22nm | 22nm |
| **Frequency (MHz)** | 10 | 1.8/10/50 | 24 | 12 |
| **Start-up time (us)** | 12.4 | 64/11/2.2 | 15 | 101 |
| **Start-up time (cycles)** | 124 | 118/113/110 | 360 | 1208 |
| **Start-up Energy (nJ)** | 14.32 | 11.6/12/9.4 | 4.4 | 45.5 |
| **Calibration Required?** | No | Yes | No | No |

Table 6.2: Comparison of this work with prior art (*These are simulation results only)

consuming about 3x more start-up power.

## 6.2 Measurements

The IC contains several sub structures for ease of testing. The three main test structures are the stand alone delay line (i.e. a delay line that can lock to an external signal), a stand alone amplifier (which can apply a voltage step to a crystal and check its response), and finally the complete system with all components required for quick startup. Presented here are the testing results from two key blocks of the system - the delayline/ring oscillator and the TIA.

Figure 6.5 shows the stand alone delay line's output in the green trace at the bottom being locked by an external 10MHz signal (not shown). The purple trace on the top is the reset signal, which is active low. When it goes high, the delay line starts locking to the

external signal. As can be seen, the delay line locks after 6 cycles of being enabled and produces a 10 MHz signal even after the external driving signal is turned off. Note that the peak-peak amplitude of the shown ring oscillator output is less than 1V due to attenuation of the test equipment - the IC itself produces a full-rail signal.

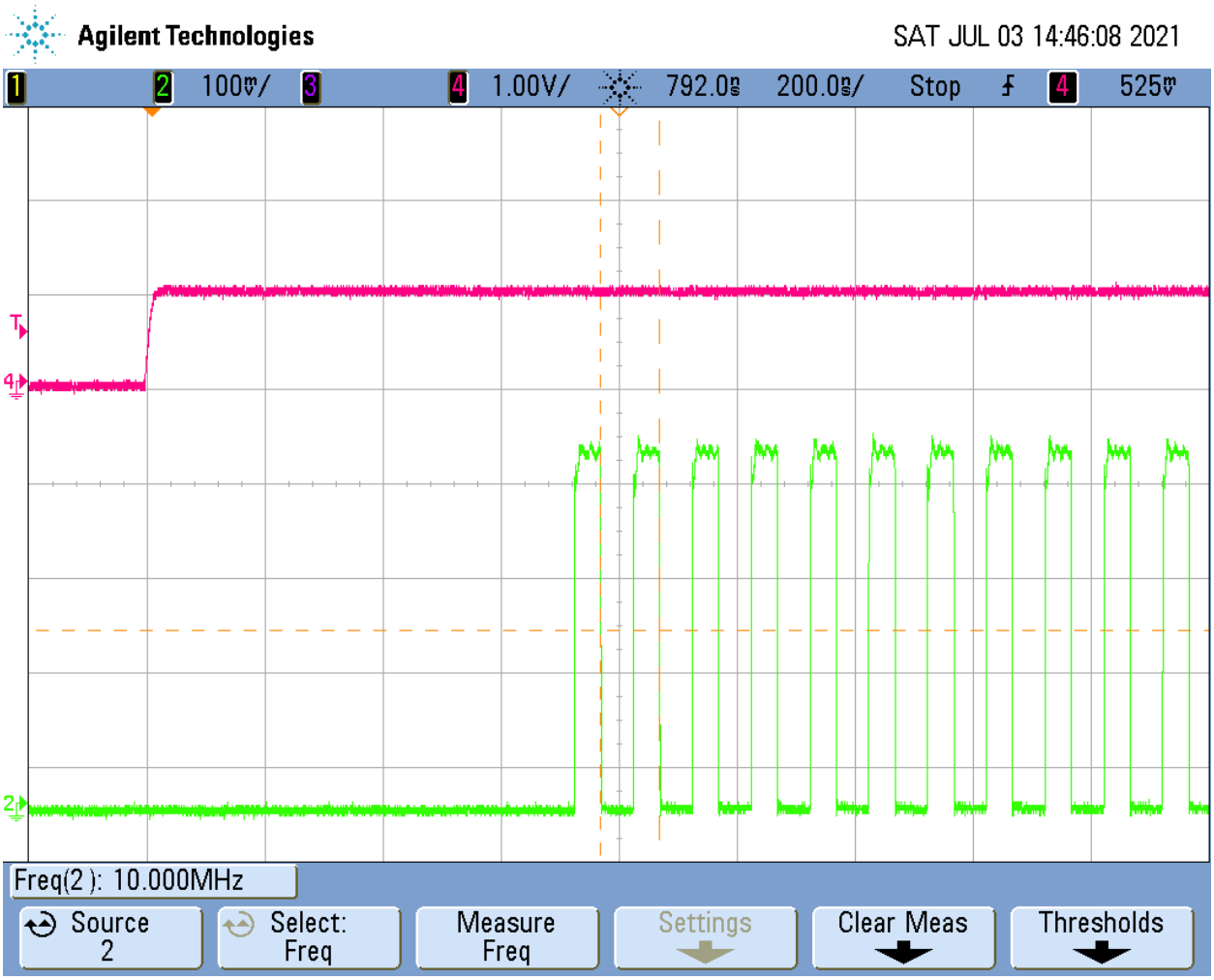


Figure 6.5: Stand alone delay line locking to an external 10MHz signal

Figure 6.6 shows the output of the stand alone amplifier. This amplifier is connected to a crystal on which it applies a voltage step and amplifies the ringing current response. The output is initially high but then goes low when the trigger signal is applied. At this point, the amplifier is turned on. For about 300 ns after that, the output remains low and

that is the DC settling time of the amplifier. After that, the amplifier starts amplifying the ringing response. The jitter produced by the amplifier is higher than expected from simulation and calculation, and debugging is on going to find the cause. Full system results are not presented as due to an unknown bug, the full system does not operate. Debugging is under progress.

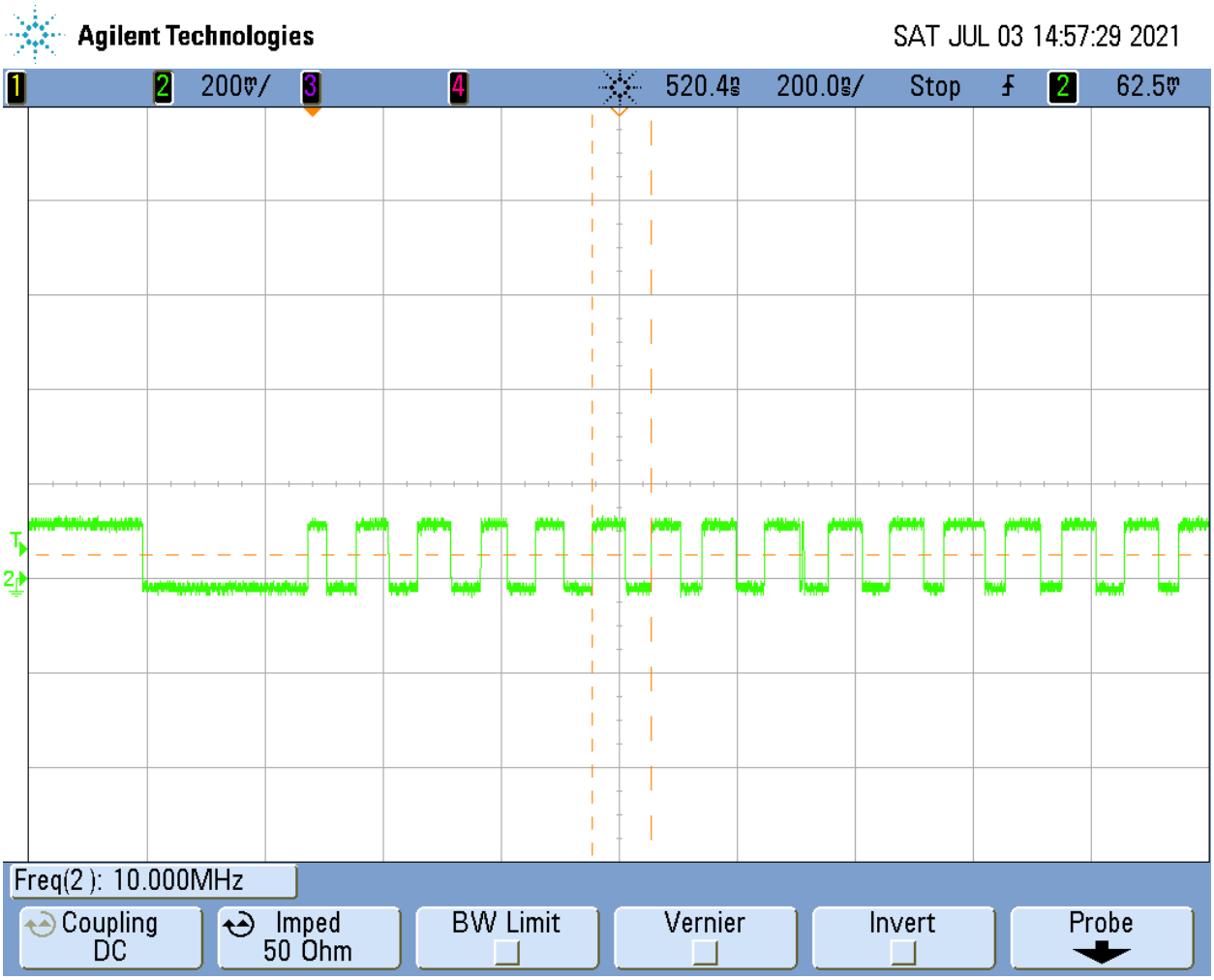


Figure 6.6: Stand alone amplifier producing a ringing response from the crystal

## 6.3 Conclusion and Future work

Previous implementations of quick startup using injection require per-chip calibration or need more startup time than the theoretical minimum due to injection frequency mismatch. This thesis presents a method that can acquire the injection frequency information from the crystal without starting it up. The proposed system is designed in TSMC 65nm and this thesis presents the circuit design of the chip. Testing results of some key blocks are presented and debugging is on going for the full chip. Future work can explore extending this idea to different frequency crystals and different oscillator types.

# CHAPTER 7

# Appendices

## 7.1 Appendix A - Crystal Step Response

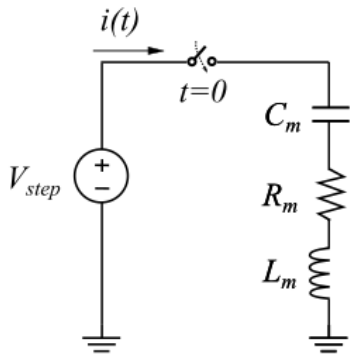


Figure 7.1: Crystal Step Response calculation

Applying KVL to the circuit of figure 7.1 will result in the following differential equations:

$$V_{step} = i(t)R_m + L_m\frac{di(t)}{dt} + \frac{1}{C_m}\int_0^t i(\tau)d\tau$$

$$\frac{d^2i(t)}{dt^2} + \frac{di(t)}{dt}\frac{R_m}{L_m} + \frac{1}{L_mC_m}i(t) = 0$$

The natural frequency and the damping factor are therefore given by:

$$\omega_0 = \frac{1}{\sqrt{L_mC_m}}$$

$$\xi = \frac{R}{2}\sqrt{\frac{C_m}{L_m}}$$

Since $Q \gg 1$, the damping factor is much less than 1, and the response will be underdamped. The general solution of an underdamped system is given as:

$$i(t) = 2\,|k|\,e^{-\delta t}\cos(\omega t + \angle k)$$

Where $\delta = \xi\omega_0 = \frac{R_m}{2L_m}$ and $\omega = \omega_0\sqrt{1-\xi^2}$. Because of High Q:

$$\omega = \frac{1}{\sqrt{L_m C_m}}\sqrt{1 - \frac{\omega R_m C_m}{4}.\frac{1}{Q}} \approx \frac{1}{\sqrt{L_m C_m}}$$

Using initial conditions, $i(0) = 0$, and $\frac{di(0)}{dt} = \frac{V_{step}}{L_m}$, we can find the boundary values as follows:

$$i(0) = 2\,|k|\cos(k) = 0$$

$$\angle k = 90^\circ$$

and:

$$\frac{di(0)}{dt} = \frac{V_{step}}{L_m} = -2\,|k|\,\delta\cos(k) - 2\,|k|\,\omega\sin(\angle k)$$

Since $\omega$ is very small because of the high Q, the cosine term can be neglected compared to the sin term:

$$\frac{V_{step}}{L_m} \approx -2\,|\angle k|\,\omega\sin(k) = -2\,|k|\,\frac{1}{\sqrt{L_m C_m}}\sin(90^\circ)$$

$$|k| = \frac{V_{step}}{2}\sqrt{\frac{L_m}{C_m}}$$

## 7.2 Appendix B - TIA noise calculations

Given in 7.2 is the small signal model of the TIA, together with feedback resistor noise given as:

$$\overline{{I_n}^2} = \frac{4kT\gamma}{R_{FB}}$$

Using KCL at the input and output node, we can obtain equations 7.1 and 7.2.

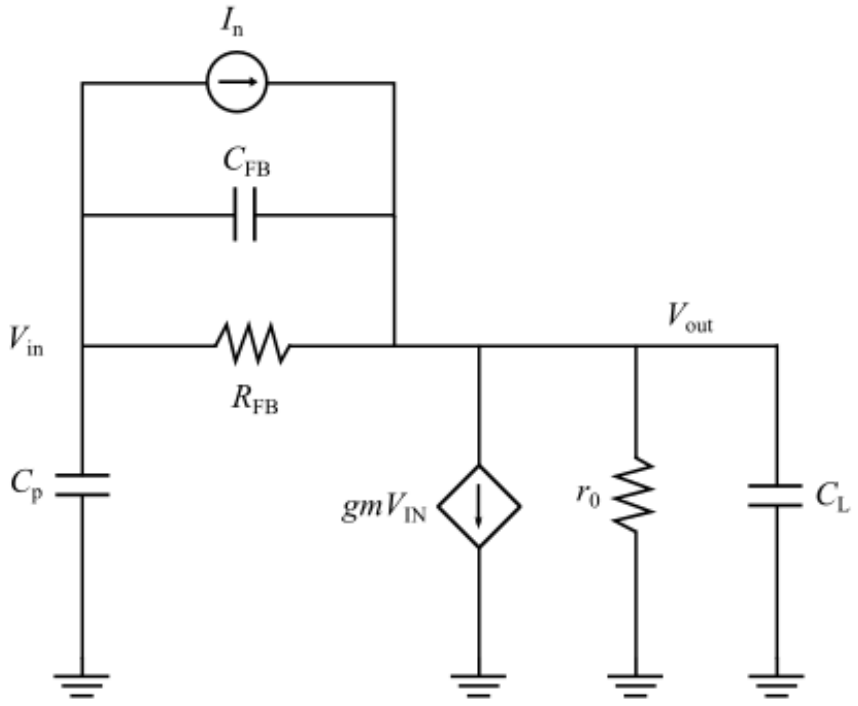


Figure 7.2: Feedback resistor noise circuit schematic used for noise transfer function calculation

$$sV_{in}C_p + gmV_{in} + \frac{V_{out}}{r_o} + sC_LV_{out} = 0 \tag{7.1}$$

$$I_n + (V_{in} - V_{out})(sC_{FB}) + \frac{(V_{in} - V_{out})}{R_{FB}} + sC_pV_{in} = 0 \tag{7.2}$$

Combining equations 7.1 and 7.2, we obtain:

$$\frac{V_{out}}{I_n|_{R_1}} = \frac{sC_p + gm_{eff}}{(\frac{1}{r_{out}} + sC_L)(\frac{1}{R_1} + s(C_p + C_1)) + s(C_p + gm_{eff})(sC_1 + \frac{1}{R_1})}$$

Given in 7.3 is the small signal model of the TIA, together with MOS thermal noise given as:

$$\overline{I_n{}^2} = 4kT\gamma gm$$

Using KCL at the input and output node, we can obtain equations 7.3 and 7.4.

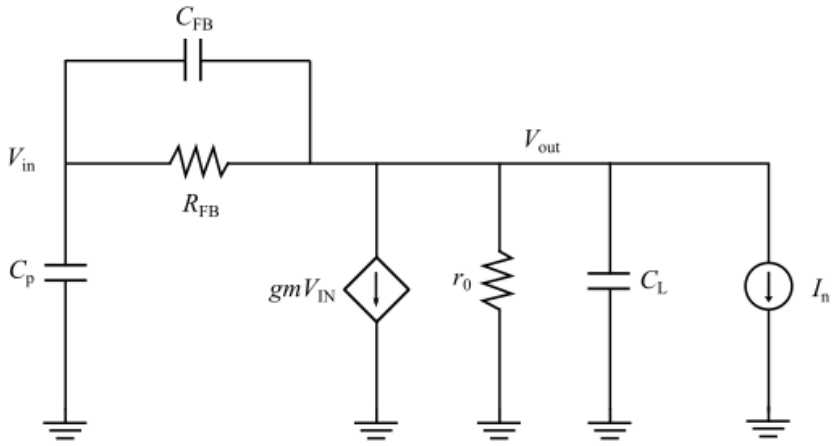


Figure 7.3: MOS noise circuit schematic used for noise transfer function calculation

$$sV_{in}C_p + gmV_{in} + \frac{V_{out}}{r_o} + sC_LV_{out} + I_n = 0 \tag{7.3}$$

$$sC_{in}V_{in} = (V_{out} - V_{in})(\frac{1}{R_{FB}} + sC_{FB}) \tag{7.4}$$

Combining equations 7.3 and 7.4, we obtain:

$$\frac{V_{out}}{I_n|_{M_1+M_4}} = \frac{1 + s(C_p + C_1)R_1}{(\frac{1}{r_{out}} + sC_L)(\frac{1}{R_1} + s(C_p + C_1)) + s(C_p + gm_{eff})(sC_1 + \frac{1}{R_1})}$$

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