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# Heterogeneous integration of a III–V quantum dot laser on high thermal conductivity silicon carbide

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## Abstract

Heat accumulation prevents semiconductor lasers from operating at their full potential. This can be addressed through heterogeneous integration of a III–V laser stack onto non-native substrate materials with high thermal conductivity. Here, we demonstrate III–V quantum dot lasers heterogeneously integrated on silicon carbide (SiC) substrates with high temperature stability. A large  $T_0$  of 221 K with a relatively temperature-insensitive operation occurs near room temperature, while lasing is sustained up to 105°C. The SiC platform presents a unique and ideal candidate for realizing monolithic integration of optoelectronics, quantum, and nonlinear photonics.

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**Introduction.** Heterogeneous integration of III–V epitaxial material with non-native substrates has the potential to create equally or better performing devices than those previously demonstrated using only III–V materials. In recent years, commercialization prospects have promoted heterogeneous integration on silicon and silicon-on-insulator (SOI) wafers, owing to the low-cost and scalable manufacturing potential of CMOS-compatible platforms [1]. However, other potential non-native substrate materials with beneficial thermal or optical properties remain as yet less explored.

The III–V quantum dot (QD) laser is a particularly interesting candidate for heterogeneous integration, owing to its inherent structural advantages over quantum well (QW) counterparts, including superior defect tolerance and thermal stability of optical gain [2–4]. In addition to the superior performance seen in simple Fabry–Pérot cavity lasers, the QD active region enables development of complex photonic light sources, such as microring lasers [5], distributed feedback (DFB) lasers [6–8], coupled cavity tunable lasers [9], and photonic crystal lasers [10].

QD lasers as-grown on native substrate are limited by the thermal properties and fabrication constraints of a III–V platform, such as lower processing temperatures and incompatibility with silicon-based passive components. Despite tremendous progress in heteroepitaxial growth technique, ongoing efforts in direct monolithic growth of III–V material on silicon substrate have yet to match the performance of native-grown devices [3,4,11]. By contrast, heterogeneous integration methods enable placement of fully functional, high-performance native-grown QD lasers on a non-native substrate compatible with other critical photonic components. Recently, heterogeneous methods produced record high-speed DFB QD lasers bonded to silicon substrate [7,8]. This successful transfer of QD lasers indicates a corresponding refinement of the fabrication methods for heterogeneously integrated photonic devices. A natural next step is to bring QD lasers to additional non-native platforms, with the potential to enhance device and chip-scale performance.

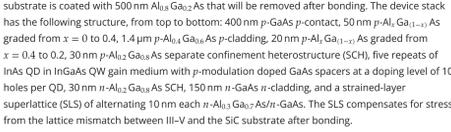
The push toward integrated photonic technologies drives an increasing demand for high-power light sources that can be densely packed within a small volume. In particular, datacenter interconnects for telecommunications require co-packaged optics and electronics in close proximity. These combined devices can generate considerable heat during operation; for instance, a single application-specific integrated circuit (ASIC) switch can consume over 200 W power [12]. Increased thermal load within a laser chip with high device density alters optical output, diminishes performance, and degrades overall device lifetime. This creates a trade-off between high packing density and effective laser performance, which in turn poses considerable difficulty when adapting photonic light sources to applications with limited physical space.

Heat accumulation can be mitigated by using the substrate as a heatsink, but the effectiveness of this method depends on the thermal conductivity of the substrate material. Compared with native GaAs substrate with a thermal conductivity of 0.55 W/cm·K at 300 K [13] and undoped silicon with a higher thermal conductivity of 1.3 W/cm·K at 300 K [14], SiC possesses an impressively high thermal conductivity of 4.9 W/cm·K at 300 K [15]. In addition, SiC has high breakdown voltage ( $3 \times 10^4$  V/cm) [16], high optical damage threshold (80 GW/cm<sup>2</sup>) [17], and nonlinear effects at the second order (30 pm/V) and third order ( $10^{-18}$  m<sup>2</sup>/W) [18,19], which make the SiC platform a unique and ideal candidate for multi-component integration.

Pioneering work proposed the III–V on SiC photonics platform, where InP and InGaAsP waveguides were successfully transferred to bulk SiC substrate [20]. Further characterization of III–V bonded to SiC revealed heat dissipation improvement by a factor of nine, as well as reduced thermal stress of InP films on SiC, compared with silicon or SOI substrates [21]. While properties of III–V lasers on heterogeneously bonded silicon platforms have been extensively studied [1,22,23], there has been limited research regarding III–V lasers integrated on SiC substrates. Recent studies in membrane device processing show promising high-speed performance of membrane lasers on SiC substrate operated under direct modulation [24]. Preliminary work also shows that the SiC platform enables production of photonic crystals [25], nonlinear microresonators [19], and long-coherence spin-defect based photonics for quantum computing [19,26]. Moving forward, comprehensive research in the work flow to heterogeneously integrate III–V lasers onto SiC is needed.

In this study, we use chip-scale heterogeneous integration to bond InAs QD lasers onto high thermal conductivity SiC substrate. These Fabry–Pérot lasers emit in the Q-band at room temperature and sustain lasing up to 105°C, with a relatively temperature-insensitive characteristic temperature  $T_0$  of 221 K. Additionally, these devices begin to lase with threshold current density as low as 223 A/cm<sup>2</sup>. Although this first demonstration of QD lasers on SiC still allows significant room for improvement in output power levels, this can be addressed in future iterations with modification of the optical mode profile and QD active region. The low-threshold current density and temperature-insensitive performance of these lasers indicates high potential for the use of thermally conductive SiC in further laser applications.

Molecular beam epitaxy (MBE) is used to grow a III–V laser structure on a native (001) GaAs substrate. This structure targets the center of the gain spectrum within the Q-band at 1300 nm wavelength. Figure 1 shows, schematically, the epitaxial structure as-grown. The (001) GaAs substrate is coated with 500 nm Al<sub>0.4</sub>Ga<sub>0.6</sub>As that will be removed after bonding. The device stack has the following structure, from top to bottom: 400 nm p-GaAs p-contact, 50 nm p-Al<sub>0.4</sub>Ga<sub>0.6</sub>As graded from  $x = 0$  to 0.4, 1.4 μm p-Al<sub>0.4</sub>Ga<sub>0.6</sub>As p-cladding, 20 nm p-Al<sub>0.4</sub>Ga<sub>0.6</sub>As. As graded from  $x = 0.4$  to 0.2, 30 nm p-Al<sub>0.4</sub>Ga<sub>0.6</sub>As separate confinement heterostructure (SCH), five repeats of InAs QD in InGaAs QW gain medium with p-modulation doped GaAs spacers at a doping level of 10 holes per QD, 30 nm n-Al<sub>0.4</sub>Ga<sub>0.6</sub>As SCH, 150 nm n-GaAs n-cladding, and a strained-layer superlattice (SLS) of alternating 10 nm each n-Al<sub>0.4</sub>Ga<sub>0.6</sub>As/n-GaAs. The SLS compensates for stress from the lattice mismatch between III–V and the SiC substrate after bonding.



**Fig. 1.** Processing steps from bonded wafer to complete device. (a) SiC substrate. (b) Substrate is etched to create vertical channels (VCs) before bonding. A top view is imaged using scanning electron microscopy. (c) III–V laser stack epitaxially grown on native GaAs is bonded to SiC substrate. (d) Device mesas are defined and etched, resulting in the laser material structure. (e) Cross sectional schematic, scanning electron micrograph of completed laser, and simulated normalized intensity profile of optical mode.

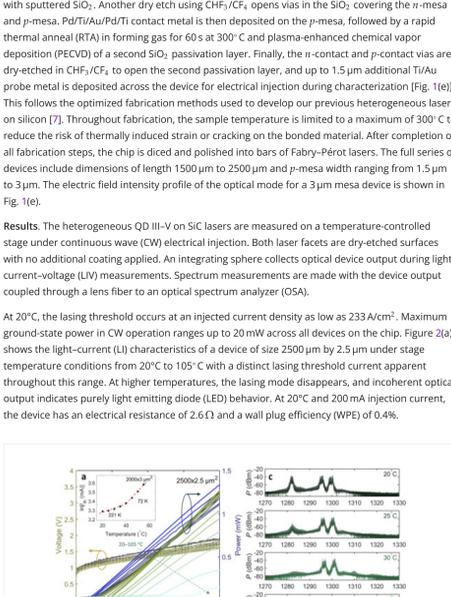
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The initial substrate is a commercially available, semi-insulating 2 in. 6H-SiC (0001) wafer doped with vanadium to a vendor-specified resistivity over  $10^3$  Ω·cm. The fresh SiC wafer is prepared for bonding by dry etching a grid-shaped pattern of vertical channels (VCs) across the top surface with 50 μm pitch in both directions, as shown schematically and imaged in Figs. 1(a) and 1(b), respectively. This dry etching is done through inductively coupled plasma (ICP) reactive ion etching (RIE) with SF<sub>6</sub> gas. Directly before bonding, the as-grown III–V material and VC-patterned SiC wafer surfaces are prepared with N-methyl-2-pyrrolidone (NMP) solution, followed by oxygen plasma ashing and piranha acid cleaning. The III–V laser stack as-grown on native GaAs is flip-chip bonded onto the SiC wafer with a 3 nm SiO<sub>2</sub> interlayer, and the structure is subsequently annealed at 100°C for 18–24 h to relieve residual stress after bonding [Fig. 1(c)]. After returning to room temperature, the coefficient of thermal expansion difference between the substrate and the bonded film results in a tensile strained III–V stack. The VC pattern in the SiC/III–V interface allows any trapped gases from this bonding step to escape during subsequent processing stages. After bonding, the GaAs growth wafer and AlGaAs buffer are polished away during the substrate removal step.

The initial laser profiles are patterned using photolithography and a two-step Cl<sub>2</sub>/N<sub>2</sub> dry etch. The first dry etch defines the p-mesa and laser facets, while the second etch creates the wider n-mesa [Fig. 1(d)]. Pd/Ge/Au/Ti contact metal is deposited along the n-mesa. The structure is passivated with sputtered SiO<sub>2</sub>. Another dry etch using CHF<sub>3</sub>/CF<sub>4</sub> opens vias in the SiO<sub>2</sub> covering the n-mesa and p-mesa. Pd/Ti/Au/Pd/Ti contact metal is then deposited on the p-mesa, followed by a rapid thermal anneal (RTA) in forming gas for 60 s at 300°C and plasma-enhanced chemical vapor deposition (PECVD) of a second SiO<sub>2</sub> passivation layer. Finally, the n-contact and p-contact vias are dry-etched in CHF<sub>3</sub>/CF<sub>4</sub> to open the second passivation layer, and up to 1.5 μm additional Ti/Au probe metal is deposited across the device for electrical injection during characterization [Fig. 1(e)]. This follows the optimized fabrication methods used to develop our previous heterogeneous lasers on silicon [7]. Throughout fabrication, the sample temperature is limited to a maximum of 300°C to reduce the risk of thermally induced strain or cracking on the bonded material. After completion of all fabrication steps, the chip is diced and polished into bars of Fabry–Pérot lasers. The full series of devices include dimensions of length 1500 μm to 2500 μm and p-mesa width ranging from 1.5 μm to 3 μm. The electric field intensity profile of the optical mode for a 3 μm mesa device is shown in Fig. 1(e).

**Results.** The heterogeneous QD III–V on SiC lasers are measured on a temperature-controlled stage under continuous wave (CW) electrical injection. Both laser facets are dry-etched surfaces with no additional coating applied. An integrating sphere collects optical device output during light-current-voltage (LIV) measurements. Spectrum measurements are made with the device output coupled through a lens fiber to an optical spectrum analyzer (OSA).

At 20°C, the lasing threshold occurs at an injected current density as low as 233 A/cm<sup>2</sup>. Maximum ground-state power in CW operation ranges up to 20 mW across all devices on the chip. Figure 2(a) shows the light-current (LI) characteristics of a device of size 2500 μm by 2.5 μm under stage temperature conditions from 20°C to 105°C with a distinct lasing threshold current apparent throughout this range. At higher temperatures, the lasing mode disappears, and incoherent optical output indicates purely light emitting diode (LED) behavior. At 20°C and 200 mA injection current, the device has an electrical resistance of 2.6 Ω and a wall plug efficiency (WPE) of 0.4%.



**Fig. 2.** (a) Light-current-voltage (LIV) characteristics during continuous wave (CW) operation at stage temperature from 20°C to 105°C. Inset: Threshold current has characteristic temperature  $T_0 = 221$  K between 20°C and 40°C. (b) Thermal and injection current induced spectrum redshift of a ground-state peak in a 1500 μm by 3 μm device held at either 20°C constant temperature or 100 mA constant injection current. (c) Spectra under varied temperature for the device in (b) under 100 mA injection current.

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Commercially available InAs QD lasers on native GaAs substrate have maximum lasing temperature specifications between 10°C and 200°C [27], with reported results up to 220°C and characteristic temperature  $T_0 = 170$  K [28]. On non-native silicon substrate, five-layer InAs QD Fabry–Pérot lasers with equivalent p-modulation doping have been reported with maximum lasing temperatures of 36°C to 119°C under CW operation [29]. More recently,  $T_0 = 167$  K was achieved on silicon with comparable maximum lasing around 110°C [30]. Although the SiC laser maximum temperature is lower, owing to limited optical gain, the higher  $T_0$  of 221 K indicates reduction in temperature sensitivity compared with native GaAs and non-native silicon substrates. The operating temperature improvements demonstrated between the inception and maturity of silicon-substrate lasers shows the progress slope inherent to any new platform, suggesting potential for improvement in SiC laser performance with further study.

Lasing peaks occur between 1290 nm and 1305 nm during standard 20°C operation. The ground state is typically centered at 1300 nm with the first excited state emerging at 1295 nm. Spectra taken at varying temperatures and a fixed injection current of 100 mA indicate a thermal redshift of 0.106 nm/°C when tracking the same peak across temperatures. Spectra taken at a fixed temperature of 20°C and varying injection current indicate a current-driven redshift of 5.64 nm/A when tracking the same peak across currents [Fig. 2(b)].

At distinct currents beyond threshold, the emission spectra of these devices show two or more injection peaks. In Fig. 2(c), changing the temperature from 20°C to 45°C at a constant injection current of 100 mA generates between two and four peaks. It is unclear why the spectra show a number of sparse peaks, given the Fabry–Pérot device design, but this might indicate unintentional internal reflection from the optical defects that interfere with the laser cavity or facet mirrors. The facets of these III–V on SiC devices appear intact when imaged, as seen in Fig. 1(e). Nevertheless, the multi-peak spectra might indicate a need for further process refinement to optimize device geometry and reflectivity.

**Conclusion.** SiC substrate is an ideal candidate for heterogeneous integration of QD lasers, owing to its high inherent thermal conductivity, as well as the prevalence of nonlinear and quantum computing technologies already established on the SiC platform. In this study, we show that InAs/GaAs QD lasers can be successfully transferred to SiC substrate through flip-chip bonding. The SiC-bonded lasers achieve a low lasing threshold current density of 233 A/cm<sup>2</sup> and promising thermal characteristics. A high  $T_0$  of 221 K indicates a thermally insensitive operation regime near room temperature, and laser operation is sustained up to 105°C environmental temperature. This Fabry–Pérot laser demonstration presents a preliminary success in III–V light source integration on a SiC platform.

Further work developing the bonding process and testing device reliability will be essential to achieve performance comparable with state-of-the-art heterogeneous integration of III–V on silicon substrate. With an optimized bonding procedure, the SiC platform will enable integration of III–V light sources with more technology-specific applications, such as DFB or comb lasers for telecommunications. This study's successful demonstration of bonded QD lasers on the SiC platform represents a first step toward that eventually, setting the foundation for future integrated photonic technologies that enhance on-chip light source performance using SiC material properties.

Beyond leveraging the improved thermal conductivity of the SiC platform, further extensions include combining these QD lasers with the nonlinear resonators and quantum computing technologies unique to the SiC platform. For instance, DFB lasers could enable direct on-chip control over spin-defect qubits in SiC. Overall, adding heterogeneous III–V components to existing quantum computing systems merges the advantages of devices optimized for each platform. This, in turn, promotes the development of photonic circuits where all necessary components coexist within a single chip.

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## Disclosures

The authors declare no conflicts of interest.

## Data availability

Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

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