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Journal

Optics Express, 19(15)

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Publication Date

2011-07-08

Peer reviewed

Low-loss Si$_3$N$_4$ arrayed-waveguide grating (de)multiplexer using nano-core optical waveguides

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Abstract: A 16-channel 200GHz arrayed-waveguide grating (AWG) (de)-multiplexer is demonstrated experimentally by utilizing Si$_3$N$_4$ buried optical waveguides, which have 50nm-thick Si$_3$N$_4$ cores and a 15µm-thick SiO$_2$ cladding. The structure with an ultra-thin core layer helps to reduce the scattering due to the sidewall roughness and consequently shows very low loss of about 0.4~0.8dB/m. When using this type of optical waveguide for an AWG (de)multiplexer, there is no problem associated with gap refill using the upper-cladding material even when choosing a small (e.g., 1.0 µm) gap between adjacent arrayed waveguides, which helps to reduce the transition loss between the FPR (free-propagation region) and the arrayed waveguides. Therefore, the demonstrated AWG (de)multiplexer based on the present Si$_3$N$_4$ buried optical waveguides has a low on-chip loss. The fabricated AWG (de)multiplexer is characterized in two wavelength ranges around 1310nm and 1550nm, respectively. It shows that the crosstalk from adjacent and non-adjacent channels are about −30dB, and −40dB, respectively, at the wavelength range of 1310nm. The Si$_3$N$_4$ AWG (de)multiplexer has a temperature dependence of about 0.011nm/°C, which is close to that of a pure SiO$_2$ AWG device.

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OCIS codes: (130.0130) Integrated Optics; (230.7390) Waveguides, planar.

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1. Introduction

As a promising technology for expanding the capacity of an optical communication system, wavelength division multiplexing (WDM) has been used widely in many applications, including optical communications. As a typical integrated (de)multiplexer used in a WDM system, the arrayed-waveguide grating (AWG) is important for many DWDM systems and modules [1,2]. In addition, AWGs have also been used for optical sensing [3] and optical spectrometers [4]. Therefore, significant effort has been made to develop high-performance AWGs based on various materials and waveguide structures, e.g., silica-on-Si buried waveguides [5,6], polymer waveguides [7,8], InP ridge waveguides [9], large silicon-on-insulator (SOI) ridge waveguides [10] as well as SOI (silicon-on-insulator) nanowires [11,12]. Silica AWG has been commercialized because of its high performance. However, the bending radius is usually very large because of the low index-contrast, which is not good for a high integration density. In contrast, SOI-nanowire has an ultra-high index contrast, which enables a micro-scale bending, and consequently ultrasmall SOI-nanowire AWGs have been intensively studied in the past years [11-12]. The drawback is that the SOI-nanowire AWG needs very high resolution fabrication technology and usually has a high insertion loss and high crosstalk. As an alternative platform with a moderate index contrast, Si$_3$N$_4$ waveguide is of interest [13-14]. In this paper, we demonstrate an AWG based on Si$_3$N$_4$ waveguides with a nano-core layer.

For AWGs, low loss is highly desirable, especially for applications in which low power consumption is required. When an AWG is connected with fibers, the fiber-to-chip coupling loss is one of the major loss origins, especially if the waveguide mode is not well-matched to the fiber mode. Nevertheless, this coupling loss could be minimized by using various mode converters [15]. On the other hand, for an AWG integrated with other components on the same chip, the on-chip loss is usually more important. Therefore, in this paper we focus on the AWG's on-chip loss, which includes the material loss, bending loss, waveguide scattering loss, and the transition loss between the FPR (free propagation region) and the arrayed waveguides. Usually the material loss can be minimized in the desired wavelength range by choosing the material appropriately. The bending loss can be reduced simply by choosing a large bending radius (even though small bending radius is desired to obtain a small footprint). Thus, in order to achieve a low-loss AWG, a reduction of the waveguide scattering and transition losses is essential.

The scattering loss can be reduced significantly by minimizing the roughness with an improved fabrication technology (especially the etching process). On the other hand, the

scattering loss also depends on the optical field distribution, which can be modified by designing the waveguide structure. Since the top and bottom surfaces for a planar optical waveguide are much smoother than the sidewalls, the scattering loss is usually dominated by the sidewall roughness. It is expected to have a reduced scattering loss if a nano-scale core layer is used. In Ref [16], we reported a low loss of 0.03dB/cm at 1550nm for 2-mm bend radius by using a buried optical waveguide which has a wide but ultra-thin Si_3N_4 core ($2\mu m \times 80nm$). This provides a promising way to realize low-loss large-scale photonic integration circuits. In this paper, we demonstrate a low-loss AWG (de)multiplexer by using a thinner, lower loss optical waveguide with a 50nm-thick SiN core layer, and a loss of about 0.4~0.8dB/m [17].

As mentioned earlier, the transition loss between the FPR and the arrayed waveguides is another important origin for the on-chip loss of an AWG [6,18]. The transition loss is due to a field mismatch between the FPR and the arrayed waveguides because there are gaps between arrayed waveguides and the gap size is limited by the fabrication process. First, one usually cannot obtain a zero-gap because of the resolution limit of UV lithography. A potential solution is using e-beam lithography [18], which could make nano-scale gaps; however, the fabrication becomes very expensive and inefficient. For SiO_2-on-Si AWGs in particular, the gaps are usually not allowed to be narrower than $2\mu m$ (which is not limited by UV lithography) so that one could refill the upper-cladding material into the gaps without voids. In order to reduce the transition loss, there are several approaches, e.g., using a double-etch technology, which has been used for AWGs based on InP waveguides [9], and SOI nanowires [11]. Another similar approach of using vertical tapers is introduced at the junctions and the transition loss could be reduced by 1dB [6]. However, the fabrication is not easy.

The waveguide reported in this paper has an ultra-thin core layer, and so it becomes very easy to refill the upper-cladding material into the gaps even when the gap width is reduced to less than $2\mu m$. Considering the resolution limitation of the UV-lithography process, in our design we choose 1-μm-wide gaps, and a low-loss AWG is achieved as the experimental results show below. In addition, the ultra-thin core layer allows a singlemode optical waveguide to be as wide as several microns even though the Si_3N_4 core has much higher refractive index than the SiO_2 cladding. Since a wider optical waveguide is more tolerant to the width variation, the present wide Si_3N_4 optical waveguide also helps to obtain a low-crosstalk AWG (de)multiplexer. Table 1 shows a comparison for AWGs on various platforms, including SiO_2, SOI, InP, polymer as well as Si_3N_4 in the present paper. From this comparison, one sees that the present Si_3N_4 platform is a good option for realizing AWGs with good performances.
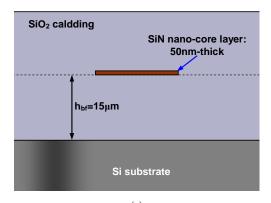
Table 1. Comparison for AWGs on various platforms.

	(non)adjacent crosstalk	on-chip loss	Channel number ×channel spacing	Waveguide size	Footprint
SiO_2 WG [6]	~−40dB	0.75dB	$32 \times 100GHz$	$6\mu m \times 6\mu m$	–
Polymer buried WG [7]	~−25dB	~8dB	$8 \times 400GHz$	$6\mu m \times 6\mu m$	$6.4cm \times 1.4cm$
Polymer strip WG [8]	~−20dB	~5dB	$23 \times 400GHz$	$2\mu m \times 1.5\mu m$	$0.22cm \times 0.47cm$
InP [9]	~−12dB	<5dB	$4 \times 400GHz$	$2\mu m \times 0.72\mu m$	$230\mu m \times 330\mu m$
SOI rib WG [10]	~−22	~6dB	$4 \times 240GHz$	$- \times 5\mu m$	$2.7cm \times 2.7cm$
SOI nanowire [12]	~−12dB	~3dB	$9 \times 400GHz$	$500nm \times 220nm$	$134\mu m \times 115\mu m$
SiN WG (this work)	<−30dB (~−40dB)	~<0.5dB	$16 \times 200GHz$	$5.5\mu m \times 50nm$	$2cm \times 1.5cm$

2. Design, fabrication and characterization

Figure 1(a) shows the cross section of the present buried Si_3N_4 optical waveguides, which have a wide and ultrathin Si_3N_4 core (about 50nm thick). The SiO_2 lower-cladding has a

thickness of 15μm to avoid any leakage loss to the substrate. The SiO_2 upper-cladding is also 15μm-thick to make the waveguide symmetrical. The waveguides and devices were fabricated with LioniX BV's TriPleXTM technology [16]. The process begins with the thermal oxidation of a standard silicon wafer form the lower cladding. This is followed by LPCVD deposition of stoichiometric Si3N4. A single photolithography step is then performed followed by reactive ion etching to form the ridge waveguide. Finally, a thick SiO2 layer is deposited using plasma-enhanced CVD (PECVD) to complete the upper cladding layer. The refractive indices for the Si_3N_4 core and SiO_2 cladding are about 1.99 and 1.45, respectively. In this structure, the sidewall area is very small and consequently the overlap of the optical field with the sidewall is minimized, which is helpful to reduce the scattering loss from the roughness of the sidewall. Figure 1 (b) and 1(c) show the profiles for TE- and TM- polarized fundamental mode fields, which are from the full-vectorial FEM (finite-element method) mode solver. For the present Si_3N_4 waveguide, the TM polarized mode has a much weaker confinement than the TE polarized mode. Consequently the bending loss of TM polarization is much higher than TE polarization. Therefore, in this paper we only consider operation with TE polarization.
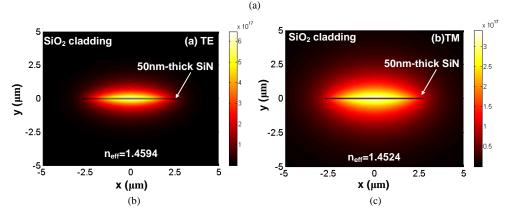

(a)

(b)   (c)

Fig. 1. (a). The cross section of the present low-loss buried optical waveguide with a 50nm-thick Si_3N_4 core; (b) the mode profile of the TE-polarized fundamental mode; (c) the mode profile of the TM-polarized fundamental mode.

For the AWG design, we choose the following parameters: the central wavelength λ_0 = 1550nm, the channel number N_{ch} = 16 and the channel spacing $\Delta\lambda_{ch}$ = 1.6nm (200GHz), the number of arrayed waveguides N_{WG} = 150, the diffraction order m = 60, the FPR length L_{FPR} = 3000μm, and the end separation of the output waveguides d_g = 20μm. Figure 2 shows the layout of the designed AWG (de)multiplexer. Two reference waveguides are put at the bottom of the AWG for normalizing the AWG's response. The total size is about 2cm × 1.5cm, which is comparable to a conventional SiO_2 AWG. It is possible to reduce the footprint by choosing

a relatively thick Si_3N_4 core layer (e.g., 100nm~200nm) so that the minimal bending radius could be reduced to sub-millimeter. Here we choose the Si_3N_4 thickness as 50nm in order to be compatible to the design for ultra-low loss waveguiding in the same wafer.
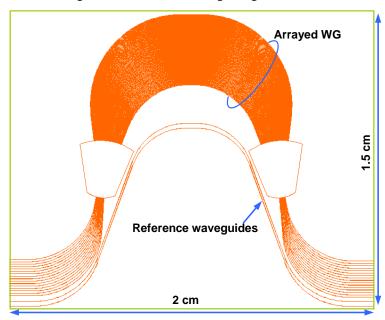

Fig. 2. The layout of the designed AWG (de)multiplexer.

In order to characterize the fabricated AWG, we use a measurement setup consisting of a free-space optical system with a bulk polarizer to have a TE-polarized input light at the input side [19]. A lens fiber was used for the coupling and the coupling loss is less than 2dB/facet for a 5.5μm-wide input/output waveguide. Figure 3(a) shows the measured spectral responses in the wavelength range from 1510nm to 1610nm by using a tunable laser and a photodetector. The tunable laser was tuned with a step of 0.1nm. The responses are normalized by the transmission of the reference waveguide. It can be seen that the spectral response is repeated over a wavelength span, which is called free spectral range (FSR). The FSR is about 25.3nm for the AWG device. The channel spacing is about 1.58nm, which is very close to the designed value (1.6nm). Therefore, there are 16 channels available in a FSR. From the normalized responses shown in Fig. 3(a), it can be seen that the excess loss of the fabricated AWG is low (almost zero for the central channel), which is mainly due to the small gap between the arrayed waveguides and good refilling of the upper-cladding layer because of the core layer is very thin. Figure 3(b) shows the responses of the central channel (#8). From this figure, one can see that the crosstalk from the adjacent channels is about −25dB while the non-adjacent crosstalk is as low as −30dB. We also note that there are two significant sidelobes at both sides of the major peak. These two sidelobes are due to the coupling between the adjacent output waveguides.
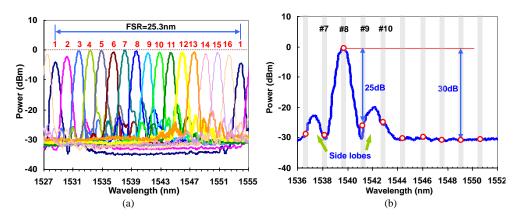
Fig. 3. (a). The measured spectral responses of all the channels in the wavelength range around 1550nm; (b) the response for channel
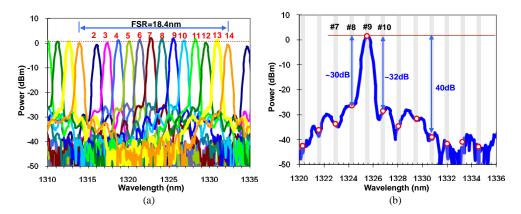

Fig. 4. (a). The measured spectral responses of all the channels in the wavelength range around 1310nm; (b) the response for channel #9. The OSA resolution is 0.1nm in the measurement.

When the wavelength becomes shorter, the optical confinement of the Si_3N_4 optical waveguide becomes stronger and consequently the coupling between adjacent output waveguides is reduced. Therefore the sidelobes are expected to be smaller. Here we also measure the AWG's responses in a short wavelength range from 1280nm to 1360nm by using an ASE light source along with an optical spectral analyzer (OSA) whose resolution is 0.1nm. Figure 4(a) shows the measured spectral responses of all the channels in the wavelength range from 1310nm to 1335nm. These spectral responses are normalized by the transmission of the reference waveguide. In this case, the FSR of the AWG becomes 18.4nm because of the shorter operation wavelength and the channel spacing is about 1.34nm, which is smaller than that in the wavelength range around 1550nm. Consequently, only 13 channels are available in a FSR. The central channels have very low excess loss. For the outer channels, the loss is higher due to the envelope of the far field [20]. Figure 4(b) shows the response of the central channel. From this figure, one sees that the crosstalk from the adjacent channel is less than –30dB, and the non-adjacent channel crosstalk is about –40dB.

We also characterize the temperature dependence of the presented AWG.

Figure 5(a) shows the measured spectral response of the central channel (#9) when the substrate temperature is set as 10, 40, 70, and 100°C, respectively. It can be seen that the central wavelength increases as the temperature increases. Since the present Si_3N_4 waveguide has a 50nm-thick core surrounded by a thick SiO_2 cladding, most power of the fundamental

mode is confined in the SiO_2 cladding and consequently the thermal performance is expected to be very similar to a pure SiO_2 buried waveguide.

Figure 5(b) shows the central wavelength as the temperature varies. And the slope is about $\Delta\lambda/\Delta T = 0.011$ nm/°C, which is very close to that of an AWG based on pure SiO_2 buried waveguides as expected.
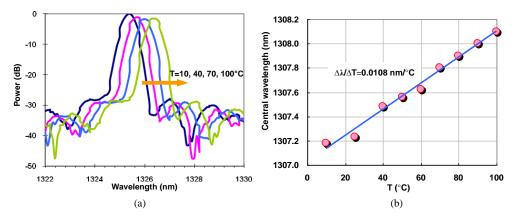

Fig. 5. (a). The spectral response of channel #9 as the temperature varies; (b) the central wavelength of channel #9 as the temperature increases from 10 to 100°C.

3. Conclusions

In this paper, we have demonstrated a low-loss, low-crosstalk AWG (de)multiplexer by using Si_3N_4 buried optical waveguides. The presented AWG (de)multiplexer has 16 channels and the channel spacing is 200GHz (i.e., 1.6nm). The singlemode Si_3N_4 optical waveguide used here has a 5.5μm × 50nm Si_3N_4 core and a 15μm-thick SiO_2 cladding. With such a structure, the Si_3N_4 optical waveguide has a very low scattering loss due to small mode overlap with the sidewall roughness. For the design of an AWG (de)multiplexer, we have chosen a small gap (about 1μm-wide) between adjacent arrayed waveguides to reduce the transition loss between the FPR and the arrayed waveguides. The fabricated AWG (de)multiplexer has been characterized in two wavelength ranges around 1310nm, and 1550nm, respectively. At the shorter wavelength range, the optical confinement becomes stronger and consequently the crosstalk is lower than that at longer wavelengths. It has shown that the crosstalk of adjacent and non-adjacent channels are about –30dB, and –40dB, respectively, at the wavelength range of 1310nm. The design could be optimized further to improve the AWG performance at longer wavelength by choosing a thicker core (e.g., 100~200nm). Finally we have also characterized the temperature dependence of the fabricated Si_3N_4 AWG (de)multiplexer and the temperature dependence is about 0.011nm/°C, which is close to that of a pure SiO_2 AWG device because most power of the fundamental mode is confined in the SiO_2 cladding.

Acknowledgements