Title
III-V semiconductor nanowire lasers on silicon

Author
Kim, Hyunseok

Publication Date
2018

Peer reviewed|Thesis/dissertation

UNIVERSITY OF CALIFORNIA

Los Angeles

III-V semiconductor nanowire lasers on silicon

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in Electrical Engineering

by

Hyunseok Kim

2018

ABSTRACT OF THE DISSERTATION

III-V semiconductor nanowire lasers on silicon

by

Hyunseok Kim

Doctor of Philosophy in Electrical Engineering

University of California, Los Angeles, 2018

Professor Diana L. Huffaker, Chair

Chip-scale integrated light sources are a crucial component in a broad range of photonics applications. III-V semiconductor nanowire emitters have gained attention as a fascinating approach due to their superior material properties, extremely compact size, and capability to grow directly on lattice-mismatched substrates including silicon. However, their practical applications are still in the early stages due to the difficulties in achieving high-performance nanowire emitters and integrating nanowire emitters with photonic platforms. In this dissertation, we demonstrate III-V nanowire-based lasers monolithically integrated on silicon-on-insulator (SOI) platforms, which can be potentially employed for chip-scale optical communications and photonic integrated circuits. For this, selective-area epitaxy of InGaAs nanowires on 3D structured SOI platforms is developed by catalyst-free metal-organic chemical vapor deposition. Nanowires are precisely positioned on 3D structures, including waveguides and gratings, with nearly 100 % nanowire

growth yield and wide bandgap tuning ranges. Next, nanowire array-based bottom-up photonic crystal cavities are demonstrated on SOI substrates. InGaAs/InGaP core/shell nanowire arrays form 1D and 2D photonic crystal cavities on SOI layers, and single-mode room-temperature lasing from these bottom-up cavities is achieved by optically pumping the nanowire arrays. We also show that the nanowire array lasers are effectively coupled with SOI waveguides, which is achieved by integrating bottom-up nanowires on pre-patterned SOI platforms. The lasing wavelengths of nanowire array lasers are in the ranges of 1,100–1,440 nm, which covers telecommunication wavelengths, all operating at room temperature. It is also shown that arrays of proposed lasers with individually tunable wavelengths can be integrated on a single chip by lithographically tuning the cavity geometries. In summary, the III-V nanowire lasers on silicon demonstrated in this dissertation represent a new platform for ultracompact and energy-efficient light sources for silicon photonics and unambiguously point the way toward practical and functional nanowire lasers.

This dissertation of Hyunseok Kim is approved.

Robert N. Candler

Benjamin S. Williams

Mark S. Goorsky

Diana L. Huffaker, Committee Chair

University of California, Los Angeles

2018

Table of Contents

List of Figures

Figure 2.8 30° tilted SEM images of GaAs nanowires grown on Si at different under various temperature. The nanohole diameter is 60 nm. (a) 695 °C, (b) 685 °C, (c) 675 °C, (d) 665 °C, (e) 655 °C. Scale bar, 2 μm. Insets show higher magnification images of each nanowire.

Figure 2.9 30° tilted SEM images of GaAs nanowires grown on Si at 655 °C at various precursor flows. The nanohole diameter is 60 nm. The partial pressure of TEGa and the growth time are (a) 7.22×10^{-7} mol/min for 30 minutes, (b) 5.01×10^{-7} mol/min for 40 minutes, and (c) 3.91×10^{-7} mol/min for 50 minutes, whereas V/III ratio is kept at 106. Scale bar, 2 μm. Insets show higher magnification images of each nanowire.

Figure 2.10 30° tilted SEM images of InAs nanowires grown on Si at 595 °C under various As treatment conditions. The nanohole diameter is 50 nm. 5 minutes of As treatment by flowing TBAs of 9.79×10^{-5} mol/min at (a) 400 °C and (b) 595 °C. (c) As treatment at 595 °C for 5 minutes by flowing 4.89×10^{-4} mol/min. (d) No As treatment. Scale bar, 1 μm.

Figure 2.11 30° tilted SEM images of InAs nanowires grown on Si at 610 °C under various TMIn flow rate. The nanohole diameter is 50 nm and TBAs flow is 9.79×10^{-5} mol/min for all growths. TMIn flow is linearly decreased from (a) to (f), where the flow rates are (a) 1.08×10^{-5} mol/min, (b) 9.45×10^{-6} mol/min, (c) 8.10×10^{-6} mol/min, (d) 6.75×10^{-6} mol/min, (e) 5.40×10^{-6} mol/min, and (f) 4.05×10^{-6} mol/min . Scale bar, 2 μm.

Figure 2.12 30° tilted SEM images of InAs nanowires grown on Si at various temperatures. TMIn and TBAs flow rates are 5.40×10^{-6} mol/min and 9.79×10^{-5} mol/min for all growths. The growth temperatures are (a) 595 °C, (b) 610 °C, and (c) 620 °C. Scale bar, 2 μm.

Figure 2.13 Temperature-dependent photoluminescence of InAs nanowires plotted in (a) relative and (b) normalized scales.

Figure 2.14 30° tilted SEM images of InGaAs nanowires grown on SOI at 670 °C. The TMGa, TMIn and TBAs flow rates are 5.53×10^{-6} mol/min, 1.83×10^{-6} mol/min, and 9.79×10^{-5} mol/min, respectively. Nanohole diameters are (a) 40 nm, (b) 50 nm, (c) 90 nm, and (d) 130 nm. Scale bar, 5 μm.

Figure 2.15 30° tilted SEM images of InGaAs nanowires with various material compositions grown on SOI at 670 °C. Nanohole diameters are 40 nm. Gas phase In/(In+Ga) composition is (a) 25 %, (b) 38 %, (c) 43 %, and (d) 48 %. Scale bar, 5 μm.

Figure 2.16 (a) Normalized photoluminescence spectra of InGaAs nanowire arrays grown by different In/(In+Ga) flux measured at 77 K. (b) In/(In+Ga) composition of InGaAs nanowire as a function of In/(In+Ga) flux.

Figure 2.17 (a) 30° tilted SEM images of InGaAs nanowires grown on a GaAs substrate. Scale bar, 5 μm. (b) Close-up image of dashed box in (a). Scale bar, 500 nm.

Figure 2.18 30° tilted SEM images of InGaAs nanowires grown on an SOI substrate. Nanohole diameters are (a) 50 nm and (b) 70 nm. Scale bar, 1 μm.

Figure 2.19 30° tilted SEM images of InGaAs nanowires grown on an SOI substrate by inserting GaAs seeding. Nanohole diameters are (a) 50 nm and (b) 70 nm. Scale bar, 1 μm.

Figure 2.20 30° tilted SEM images of InGaAs nanowires grown on an SOI substrate under various V/III flow rate ratio. The nanohole diameter is 70 nm and the V/III ratio is (a) 32, (b) 49, and (c) 69. Scale bar, 1 μm.

Figure 2.21 30° tilted SEM images of InGaAs nanowires grown on an SOI substrate under various material compositions. Gas phase indium compositions and growth temperatures are (a) 30 % at 680 °C, (b) 40 % at 665 °C, (c) 45 % at 655 °C, and (d) 45 % at 635 °C. Scale bar, 1 μm.

Figure 2.22 Schematic of the setup for photoluminescence measurements (drawing not to scale). The same objective lens is used to focus the pump laser onto nanowires and to collect the emission from nanowires.

Figure 2.23 Normalized PL spectra of InGaAs nanowire arrays shown in Figure 2.21.

Figure 2.24 PL spectra of an InGaAs nanowire array plotted in (a) normalized and (b) relative scales. Inset: FWHM of nanowires (red dots) compared with theoretical temperature-dependent linewidths of band-to-band transition (blue line).

Figure 2.25 Schematic illustrations of InGaAs nanowires on SOI platform. (a) Nanowire arrays on planar SOI, (b) nanowire arrays on a grating structure, and (c) a single nanowire on a waveguide structure.

Figure 2.26 Fabrication process for InGaAs nanowires on SOI platform.

Figure 2.27 30° tilted SEM images of fabricated 3D structured SOI. Nanoholes patterned on (a) 1D gratings and (b) 2D gratings. (Lower) Close-up images of dashed area. Scale bar, 500 nm.

Figure 2.28 30° tilted SEM images of nanowires grown on 3D structured SOI. (a) InAs nanowires and (b) GaAs nanowires. Scale bars, 1 μm.

Figure 2.29 SEM images of InGaAs nanowires on an SOI platform. Nanowire arrays on planar areas with (a) 1000 nm pitch and (b) 500 nm pitch. Insets in (a) and (b) show magnified images of nanowires in each array. (c) Nanowire array on a grating structure. (d) Single nanowire on an SOI waveguide structure. All images are tilted 30° from the normal view.

Figure 2.30 (a) Cross-sectional SEM images of an InGaAs nanowire array on a grating structure viewed at an angle. (b) Magnified SEM image of the dashed box in (a) viewed at a horizontal direction. (c) Cross-sectional TEM image of a middle part of a nanowire. (d) TEM image of bottom part of a nanowire. (e) Magnified TEM image of the dashed box in (d).

Figure 2.31 SEM images of (a) a single InGaAs nanowire on an SOI waveguide and (b) a waveguide edge. The length of the waveguide is 500 m. Spectrally integrated images measured on (c) the nanowire region and (d) the waveguide edge by optically pumping the nanowire. (e) Photoluminescence spectra measured on the nanowire region and the waveguide edge at room temperature. The emission from the waveguide edge is magnified 30 times for visibility. All scale-bars in (a-d) represent 2 m.

Figure 3.1 (a) Schematic of the nanowire array cavity. (b) Dependence of the number of total nanowires (N) on the cavity Q. (c) Dependence of the SOI layer thickness (t) on the cavity Q, and (d) electric field intensity profiles showing worse confinement at larger t.

Figure 3.2 30˚-tilted SEM images of an InGaAs/InGaP core/shell nanowire array laser. Scale bar, 500 nm.

Figure 3.3 (a) Photoluminescence spectra of a nanowire array laser with increasing pump power, showing the transition from spontaneous emission to lasing. (b) integrated emission intensities of the stimulated emission (filled blue circle) and spontaneous emission (filled red circle), and cavity peak linewidth (open circle). Inset: light-light curve of the lasing peak shown in a linear scale. (c) Emission patterns measured by a commercial 2D focal plane array detector. Interference patterns are observed above the lasing threshold. Scale bars, 5 μm.

Figure 3.4 (a) The PL spectrum of nanowires and the calculated spectrum ($In_{0.2}GaAs$ with the relaxation energy of 0.15 eV) showing the fit. (b) Calculated peak gain and logarithmic material gain model as a function of carrier density.

Figure 3.5 (a) Rate equation modellings for various spontaneous emission factors (β). The L-L curve calculated with β = 0.0065 and Q = 1,150 fits the best with experimental data. (b) Double-logarithmic L-L curve measured by homogeneously pumping entire nanowires. β = 0.0043 and Q = 1,970 fits the best with experimental data. Inset: Experimental L-L curve shown in a linear scale.

Figure 3.6 Schematic illustrations of the 7 × 7 nanopillar PhC laser with InGaAs/InGaP core-shell structures on an SOI substrate with an SOI layer thickness of *t*. *d* and *p* indicate the diameter and the pitch of nanopillars, respectively.

Figure 3.7 (a) TM mode photonic band structure of the square lattice nanopillar array. The grey area denotes the region above the light line in air. (b) $|E|^2$ field profiles of the first band-edge mode (blue circle in (a)) calculated by the FDTD method.

Figure 3.8 (a) Calculated Q factors and resonant wavelengths as a function of *t* in 7 × 7 nanopillar arrays and (b) a function of an array size at *t* = 40 nm.

Figure 3.9 (a) 30° tilted and enlarged SEM images of as-grown InGaAs/InGaP core-shell nanowires with d = 130 nm, p = 350 nm, and a height of 800 nm. (b) Top-view SEM image showing uniformly grown nanopillar array.

Figure 3.10 (a) Room-temperature emission spectra at various pump powers. The laser peak at a wavelength of 1057 nm steeply increases above threshold. (b) L–L curve of the nanowire array band-edge laser with a threshold of ~45 μJ/cm^2 (filled red circles) and corresponding spectral linewidth (filled blue circles). Integrated intensities are obtained by Gaussian fitting of the spectra. Inset: L–L curve on a linear scale. Optical images of the laser emission below threshold (c) and above threshold (d). Interference fringe patterns are captured above threshold.

Figure 3.11 Measured angle-resolved lasing mode images as a function of the polarization angle. Left: horizontal polarization. Center: vertical polarization. Right: 45˚ tilted polarization. The lasing mode images clearly show the angle-dependence because the laser emission is azimuthally polarized.

Figure 3.12 Diameter-dependent emission spectra of 2D photonic crystal lasers measured at room-temperature plotted in a log scale. Lasing up to a telecommunication wavelength of 1300 nm (d = 170 nm and p = 400 nm) is obtained.

Figure 4.1 Schematic of the nanowire array cavity on SOI mesas.

Figure 4.2 (a) Dependence of the trench depth (d) on the cavity Q, and (b)electric field intensity profiles showing worse confinement at smaller d. (c) Dependence of the mesa width (w) on the cavity Q, and (d) related electric field intensity profiles.

Figure 4.3 (a) SOI mesas with nanoholes. (b) GaAs seeding in nanoholes, followed by (c) InGaAs nanowire growth. Scale bar, 500 nm.

Figure 4.4 (a) Schematic of a nanowire array laser attached to a waveguide. (b) 30˚-tilted SEM images of a nanowire array cavity integrated with a waveguide and an output coupler (upper), and a close-up image of the nanowire array in the dashed box (lower). Scale bars, 5 mm (upper) and 500 nm (lower).

Figure 4.5 (a) TEM image of the nanowire cross-section. (b) Photon counts along the radial direction (A-A'), and (c) In and As compositions calculated from the photon counts. (d) In/(In+Ga) composition along the axial direction (B-B') and (e) (C-C').

Figure 4.6 (a) PL spectra of InGaAs nanowires with and without InGaP surface passivation measured at room temperature. (b) Time-resolved photoluminescence measurement of InGaAs/InGaP core/shell nanowires.

Figure 4.7 (a) Photoluminescence spectra of the laser below (red) and above (blue) the threshold. Inset: light-light curve of the lasing peak in a linear scale, indicating the lasing threshold around 100 $\mu J/cm^2$. (b) Electric field profiles (|E|) of observed cavity modes.

Figure 4.8 (a) Emission patterns of a nanowire array laser coupled with an SOI waveguide, exhibiting interference patterns above the lasing threshold. Scale bars, 5 μm. (b) Photoluminescence spectra measured on top of a nanowire array (red line) and on top of an output coupler (blue line) below the lasing threshold (left) and above the lasing threshold (right), indicating that the cavity peaks are effectively coupled to the waveguide.

Figure 4.9 (a) Coupled mode profiles of fundamental cavity mode and higher modes. (b) PL spectra measured at different pump positions and fixed pump fluence (88 μJ/cm^2), showing changes in relative intensities between the cavity peaks.

Figure 4.10 (a) Dependence of the number of nanowires constituting the cavity (N) on the coupling efficiency and cavity Q. (b) Electric field intensity profiles of waveguide-coupled cavity mode when N=18 (upper), and the same field profiles rescaled to show that the energy is dominantly dissipated through the waveguide (lower).

Figure 4.11 Schematic illustration of a nanowire array cavity with a fundamental cavity mode wavelength at 1,310 nm. The dimensions are p = 350 nm, d = 180 nm, and h = 700 nm.

Figure 4.12 Cavity Q factor as a function of the number of nanowires constituting reflector sections when the trench depth is 180 nm.

Figure 4.13 (a) Electric field profiles (E_z) of a fundamental TM-mode in xz-plane, and (b) a horizontal cross-section along the white dashed line in (a), both showing that the field is tightly confined in nanowires. A cavity Q of 134,000 and a resonant wavelength of 1,310 nm is obtained when p = 350 nm, d = 180 nm, and h = 700 nm.

Figure 4.14 (a) 35° tilted SEM images of a nanowire array cavity, and (b) a close-up view, showing high uniformity and smooth sidewalls. (c) Top-view SEM image showing the nanowires aligned to a <110> direction of the silicon layer. (d) Cross-sectional SEM image of nanowires on a patterned SOI substrate measured by slicing the sample by focused ion beam (FIB) etching. Scale bars, 500 nm

Figure 4.15 (a) Lasing spectra of nanowire array cavities on each sample. Inset: emission pattern above lasing threshold showing an interference fringe pattern. Scale bar, 5 μm. (c) L-L curves of nanobeam lasers in b. Lasing thresholds are estimated to be around 80−110 μJ/cm^2 from the linear fitting. Inset: L-L curves plotted in double-logarithmic scale.

Figure 4.16 Relative PL intensities of InGaAs nanowire arrays with different material compositions, which are measured at a low pump fluence of 2.8 μJ/cm^2.

Figure 4.17 (a) Pump power-dependent PL spectra of the $In_{0.42}Ga_{0.58}As$ nanowire array laser, plotted in a log-scale. Spontaneous emission is clamped above the threshold, and SMSR of 13 dB is achieved at the pump fluence of 242 μJ/cm^2. (b) PL spectra of a nanowire array that does not form a cavity, showing that the spontaneous emission is not clamped by increasing the pump power. (c) Double-logarithmic L-L curve of the nanowire array laser showing an S-shape response and a sudden decrease of linewidth around lasing threshold.

Figure 4.18 L-L curve plotted together with various β. The best fitting is achieved at β = 0.16 and Q = 495.

Figure 4.19 (a) Lasing spectra of seven $In_{0.33}Ga_{0.67}As$ nanobeam laser arrays grown on two samples. A spontaneous emission spectrum (grey line) is also shown for a reference. (b) Measured lasing wavelengths of nanobeam lasers (filled stars) plotted together with FDTD simulations (lines). Nanobeam cavities which have not reached lasing (open starts) are also shown for comparison.

List of Tables

Acknowledgements

First of all, I would like to thank my advisor and the committee chair, Prof. Diana L. Huffaker, for her devoted guidance on my Ph.D. study for four years. She always provided me with valuable and insightful inputs on my research, and granted me privileged opportunities to participate in multiple projects and tasks. I also appreciate the support from other committee members, Prof. Mark S. Goorsky, Prof. Benjamin S. Williams, and Prof. Robert N. Candler.

I particularly thank Dr. Wook-Jae Lee, who has been a great mentor of mine. He always tried to transfer his knowledge, skills and ideas to me as much as possible, which tremendously motivated and strengthened me in many aspects. Special thanks should also be given to previous group members, Dr. Adam C. Scofield and Dr. Pradeep Senanayake, for spending their precious times to train and guide me. I am grateful for my group members, Dr. Baolai Liang, Dr. Ramesh Babu Laghumavarapu, Dr. Alan C. Farrell, Dr. Bor-Chau Juang, Dingkun Ren, and Ting-Yuan Chang, who have always been willing to give me advices and help my research. I also appreciate the technical support of all ISNC, nanolab, and ECE department staffs.

I would like to acknowledge the financial support of Dr. Gernot Pomrenke of Air Force Office of Scientific Research (AFOSR), which covered most of the budget for my Ph.D. research. I also acknowledge the funding support from Dr. Dominique M. Dagenais of National Science Foundation (NSF), Dr. Jung Jin Ju of Electronics and Telecommunications Research Institute (ETRI) in Korea, and Sêr Cymru National Research Network in Advanced Engineering and Materials.

Finally, and most importantly, I would like to thank the tremendous love and endless support of my parents and my sister.

Vita

EDUCATION

Ph.D. (*in progress*)	University of California, Los Angeles Electrical Engineering	2014 - 2018
M.S.	Seoul National University Electrical Engineering and Computer Science	2011 – 2013
B.S.	Seoul National University Electrical Engineering	2005 - 2011

SELECTED PUBLICATIONS

Hyunseok Kim, Dingkun Ren, Alan Farrell, and Diana L. Huffaker, "Catalyst-free selective-area epitaxy of GaAs nanowires by metal-organic chemical vapor deposition using triethylgallium", ***Nanotechnology***, 29, p. 085601, 2018

Wook-Jae Lee*, **Hyunseok Kim***, Jong-Bum You, and Diana L. Huffaker, "Ultracompact Bottom-up Photonic Crystal Lasers on Silicon-on-Insulator", ***Scientific Reports***, 7, p. 9543, 2017

Hyunseok Kim, Wook-Jae Lee, Alan C. Farrell, Akshay Balgarkashi, and Diana L. Huffaker, "Telecom-Wavelength Bottom-up Nanobeam Lasers on Silicon-on-Insulator", ***Nano Letters***, 17(9), pp. 5244-5250, 2017

Hyunseok Kim, Wook-Jae Lee, Alan C. Farrell, Juan S. D. Morales, Pradeep Senanayake, Sergey V. Prikhodko, Tomasz J. Ochalski, and Diana L. Huffaker, "Monolithic InGaAs nanowire array lasers on silicon-on-insulator operating at room temperature", ***Nano Letters***, 17(6), pp. 3465-3470, 2017

Shiyu Xie, **Hyunseok Kim**, Wook-Jae Lee, Alan C. Farrell, John P. David, and Diana L. Huffaker, "InAs/InAsP core/shell nanowire photodiode on a Si substrate", ***Nano Advances***, 1, 110-114, 2016

Hyunseok Kim, Alan C. Farrell, Pradeep Senanayake, Wook-Jae Lee, and Diana L. Huffaker, "Monolithically Integrated InGaAs Nanowires on 3D Structured Silicon-on-Insulator as a New Platform for Full Optical Links", ***Nano Letters***, 16(3), pp. 1833-1839, 2016

Wook-Jae Lee, **Hyunseok Kim**, Alan C. Farrell, Pradeep Senanayake, and Diana L. Huffaker, "Nanopillar array band-edge laser cavities on silicon-on-insulator for monolithic integrated light sources", ***Applied Physics Letters***, 108, p. 081108, 2016.

Katarzyna Komolibus, Adam C. Scofield, Kamil Gradkowski, Tomasz J. Ochalski, **Hyunseok Kim**, Diana L. Huffaker, and Guillaume Huyet, "Improved room-temperature luminescence of core-shell InGaAs/GaAs nanopillars via lattice-matched passivation", ***Applied Physics Letters***, 108, p. 061104, 2016.

CONFERENCE PRESENTATIONS

Hyunseok Kim, Ting-Yuan Chang, Wook-Jae Lee, and Diana L. Huffaker, "III-V Nanowire Heterostructures on Silicon-on-Insulator for Silicon Photonics Applications", *E-MRS 2018 Spring Meeting,* Strasbourg, France, June 2018

Hyunseok Kim, Wook-Jae Lee, Alan C. Farrell, Pradeep Senanayake, and Diana L. Huffaker,, "Bottom-up Nanobeam Laser on Silicon-on-Insulator", *SPIE Photonics West*, San Francisco, United States, February 2017

Hyunseok Kim, Wook-Jae Lee, Alan C. Farrell, Pradeep Senanayake, and Diana L. Huffaker,, "III-V Nanowire Photonic Crystal Cavity Monolithically Integrated on Silicon-on-Insulator", *2016 MRS Fall Meeting*, Boston, United States, November 2016

1. Introduction

1.1 Background

In 2016, humans created 16.1 zetabyte (16.1 trillion gigabyte) of new data, and the number will grow tenfold, to 163 zetabyte, by 2025[1]. In order to address such massive data transfer, power consumption and bandwidth of interconnects appear to be the main barriers to next-generation data centers as well as high-performance computing (HPC) environments[2]. Due to ohmic loss and RC delay of copper wires, electrical interconnects are becoming the main source of bottlenecks even in short-reach communication levels, in terms of both power consumption and bandwidths.

Optical interconnects, on the other hand, offer large communication bandwidth and energy-efficient communications, since optical signal has much higher frequency (several hundred terahertz) and can be transmitted in low-loss waveguides such as optical fibers. It is therefore not surprising that researchers have been actively pursuing the goal of adapting the optical interconnects in short-reach data communication levels and replacing electrical interconnects with optical counterparts. Nowadays, optical interconnects are regarded as the enabling components for on-chip and chip-to-chip optical communication implemented in future mobile, data centers, and Internet of Things (IoT).

Silicon photonics has gained much attention as a platform for optical communications and photonic integrated circuits, with all components built on silicon or silicon-on-insulator (SOI) via monolithic or hybrid integration[3]. Active and passive optical components, including waveguides, modulators, filters and input/output grating couplers, can be integrated on these

silicon-based platforms by exploiting mature CMOS infrastructures. SOI substrates are composed of three layers − a silicon layer, a buried oxide (BOX) layer, and a thick silicon layer for handling. The SOI is especially attractive in silicon photonics since low-loss silicon waveguides can be easily formed by simple dry etching processes. This is enabled by the BOX layer with low refractive index ($n \sim 1.45$) which ensures total internal reflection.

Many academic and industrial R&D groups including IBM, Intel, Infinera, and Mellanox Technologies have been pursuing the goal of inter- and intrachip interconnects to fulfill the increasing demand for big data transport. While the accomplishments to date in this field are impressive and diverse, the energy-to-data efficiency of interconnects is currently limited to several- or sub- pJ/bit levels, which is primarily dominated by the energy dissipation from on-chip lasers[4]. International Technology Roadmap for Semiconductors (ITRS) predicts that the next generation interconnects should have the switching bandwidth per unit be scaled from the current 40 Gbit/sec to 400 Gbit/sec by 2025, while the power consumption per unit is required to be constant over the period[5]. Therefore, an on-chip platform for transmitting and computing big data with an aggregate bandwidth would require a point-to-point wavelength division multiplexed (WDM) network interconnected with ~ 10,000 optical links with an energy-to-data ratio of < 10 fJ/bit. Unfortunately, current state-of-the-art architectures for optical interconnects cannot meet these stringent requirements for energy-efficiency and link density[6].

There have been several approaches proposed to realize the integration of lasers on silicon and SOI platforms. Wafer bonding of III-V lasers, such as InGaAs or InGaAsP-based distributed feedback (DFB) lasers and distributed Bragg reflector (DBR) lasers, is a commercially available technique to form hybrid lasers[7, 8]. However, these lasers need to be grown on III-V wafers which is costly, and the size of III-V wafers does not scale with Si or SOI substrates. As an another

approach, germanium lasers on silicon made by bandgap engineering have attracted much attention in recent years due to the ease of monolithic integration and their compatibility with the CMOS process[9, 10]. However, the optical gain of germanium lasers is poor and needs to be further improved for practical applications. Lastly, direct heteroepitaxy of III-V materials on silicon or SOI has also been also actively investigated to form on-chip lasers[11, 12]. The most critical issue in heteroepitaxy is huge mismatches in lattice constants and thermal expansion coefficients between III-V materials and silicon, which result in the formation of high density of threading dislocations, misfit dislocations and antiphase boundaries[13]. These defects significantly degrade the carrier lifetime and quantum efficiency of materials, which leads to poor device performance or even prevents the device from achieving lasing. Growing thick metamorphic buffer layers is known to help reducing the density of dislocations, and room-temperature lasing is achieved from III-V quantum dot lasers on silicon by this approach[12]. However, the need of thick buffer layer which is typically several micrometers or more makes the monolithic lasers which is fabricated by this approach difficult to couple with SOI waveguides, since the optical mode of laser is far above the substrate. Also, bottom contact cannot be made on silicon or SOI since the material quality of buffer layers is poor. Therefore, it is necessary to develop a fundamentally new approach to resolve the limitations and drawbacks of currently employed heterogeneous integration techniques.

1.2 Significance and overview

In this work, III-V nanowires are employed to form functional and efficient optoelectronic devices on silicon platforms. The nanowires are directly integrated on silicon or SOI by selective-area heteroepitaxy, which eliminates the need for thick buffer layers or foreign III-V substrates. Although III-V nanowires are epitaxially grown on Si which has highly mismatched lattice

constant without any buffer, extremely small interface area between nanowires and Si helps effectively reducing and relaxing the strain, and enables monolithic integration of high-quality III-V nanowires on Si. Since nanowires exhibit nanoscale footprints, it is obvious that nanowire-based devices could be manufactured in extremely compact sizes. Furthermore, such nanoscale geometries could be adopted to design novel photonic and plasmonic architectures, which could dramatically enhance the performance of these nanoscale devices.

One of the most important requirements to achieve such nanowire-based devices is integrating nanowires which have desired properties and characteristics. To be more specific, dimensional properties such as the diameter, height and pitch of nanowires should be precisely matched to the design, and also the material properties such as the material composition, doping, and defects should be engineered for high-performance devices. The growth of various III-V nanowires and nanowire heterostructures on silicon is demonstrated in Chapter 2. Advancing from the growth on planar substrates, nanowire growth on pre-patterned SOI platforms is also achieved, which provides a practical method to integrate nanowire-based devices on silicon chips.

Selective-area epitaxy on SOI platforms offers a unique and novel approach to form bottom-up photonic crystal cavities composed of nanowires, by exploiting the capability to control the position and geometry of nanowires. Periodically arranged nanowires can form 1D or 2D photonic crystals, and artificial defects can be simultaneously embedded by locally modulating the periodicity or geometry of nanowires. III-V semiconductors have high refractive index, which is typically larger than 3, and this ensures high index contrast between III-V nanowires and surrounding environment (*e.g.* $n = 1.0$ for air and $n \sim 1.45$ for SiO_2). Such a high index contrast is essential for tightly confining the optical cavity mode in a small volume and achieving high cavity quality (Q) factor. Also, the BOX layer of SOI substrates helps reducing the leakage of light

through the substrate. On the other hand, silicon has high refractive index of 3.7, and this makes it difficult to form photonic crystal cavities on bare Si substrates. In Chapter 3, 1D and 2D photonic crystal lasers are demonstrated by integrating InGaAs nanowire arrays on SOI substrates. A thin SOI layer is employed in this design to achieve high *Q* factor by minimizing the leakage of optical fields through the SOI layer. Room-temperature lasing is achieved by optical pumping from both 1D and 2D photonic crystal lasers at low threshold pump power.

To employ nanowire lasers in communications, it is crucial that the output from nanowire lasers is coupled to optical fibers or waveguides for transmission. Especially, coupling the laser to SOI waveguides is ideal for realizing chip-scale optical links, because other components such as modulators, amplifiers and detectors can be integrated on the same chip. In Chapter 4, the integration of nanowire photonic crystal lasers with SOI waveguides is demonstrated. The growth of nanowire arrays on pre-patterned SOI substrates enables achieving high cavity *Q* on 220 nm-thick SOI substrates, by forming mesas around each nanowire to reduce the leakage of fields though silicon. SOI waveguides and output couplers are integrated with nanowire array lasers, and room-temperature lasing and efficient coupling of lasing emission into waveguides are observed by optical pumping. The lasing wavelength spans from 1,100 nm to 1,440 nm, which covers O-band telecom wavelengths. The lasing wavelengths are determined by the cavity geometry such as the diameter, height and pitch of nanowires, and by tuning these geometries, multiple lasers with different lasing wavelengths are simultaneously integrated on a single chip by tuning the diameter and pitch. These results shows the possibility for wavelength-division multiplexing (WDM), substantiating that the outcome presented in this dissertation provides a realistic approach toward nanowire lasers for silicon photonics.

2. Integration of nanowires on silicon

2.1 Overview

Semiconductor nanowires typically have diameters of several tens or hundred nanometers, while the diameter varies from several hundred nanometers to several millimeters. Various semiconductor materials can be synthesized to form nanowires, and they are regarded as promising building blocks for next-generation electronic[14], photonic[15], biochemical[16], and mechanical devices[17]. Nanowire-based devices and platforms are attractive due to numerous features of nanowires, such as their small volume, low-dimensional properties, large surface-to-volume ratio, high crystal quality, and their capability for heterogeneous integration.

III-V semiconductor nanowires are one of the most actively studied types of semiconductor nanowires. III-V nanowires typically exhibit direct-bandgap properties with few exceptions, and their bandgaps are in the range of visible to long-wavelength infrared, which extends to ultraviolet wavelengths if III-nitride family is included. These properties make III-V nanowires fascinating for photonic devices, and combined with their high carrier mobility, they are also attractive in realizing nanoelectronic and optoelectronic devices. The growth of III-V nanowires on lattice-mismatched substrates such as group IV semiconductors (silicon and germanium) and other III-V substrates have been achieved without forming threading dislocations, which is owing to an extremely small interface area between the nanowires and substrates[13]. On silicon, which is technologically the most versatile and universal platforms, III-V nanowire-based ultracompact devices including vertical transistors[18], light-emitting diodes[19], nanolasers[20], solar cells[21], and photodetectors[22] have been demonstrated, which proves the effectiveness of nanowire

approach for monolithic device integration on silicon.

The most common method to grow free-standing nanowires is the vapor-liquid-solid (VLS) method using gold as a catalyst. Au nanoparticles or nanomembranes form supersaturated droplets at a high temperature, and nanowires grow by the precipitation at the liquid/solid interface. Although this method is a well-understood and widely employed technique, Au is incorporated in nanowires and substrates during the growth[23], and this is an especially serious problem when grown on Si substrates since deep-level traps are formed in Si by Au impurities[24]. Because of this, a self-catalyzed VLS method is proposed as an alternative approach, in which group-III droplets are formed by flowing only group-III sources, followed by a nanowire growth employing these droplets as seed particles [25].

The vapor-solid (VS) method, on the other hand, is a catalyst-free growth technique which does not employ any foreign or self-formed catalysts. Nanowires are grown by the adsorption of vapor-phase atoms and their diffusion on surfaces in the VS method[26]. This VS growth can arise either on a specified position of the crystal surface by selective-area epitaxy (SAE)[27, 28] or on random positions of the substrate[29]. The SAE technique, which controls the nanowire growth sites by depositing a dielectric film and exposing nanoholes, is particularly useful in the applications requiring precise arrangement of nanowires such as photonic crystal devices[30] and plasmonic devices[31]. Since the growth is governed by diffusion of adatoms, it is also possible to grow core/multishell or axial heterostructures by controlling the growth condition[32].

In this chapter, we demonstrate the growth of GaAs, InAs, and InGaAs nanowires on silicon platforms. Growth strategies to achieve high vertical growth yield in these nanowires are introduced, and also a composition tuning of InGaAs nanowires and in-situ passivation by InGaP shell are demonstrated. We also show the growth of nanowires on pre-patterned silicon and SOI

platforms, and this is proven to be a crucial technique to integrate nanowire-based devices with silicon photonic platforms in Chapter 4.

2.2 Growth of nanowires on silicon

2.2.1 GaAs nanowires on silicon

GaAs nanowires are attractive in the field of electronics and optoelectronics because GaAs is a direct-bandgap material with high electron mobility emitting at near-infrared wavelengths. The VS SAE of GaAs nanowires has been typically conducted using metal-organic chemical vapor deposition (MOCVD) systems, and various GaAs nanowire-based devices including light-emitting diodes[19], solar cells[33], lasers[34], field-effect transistors[18], and photodetectors[35] are reported using the VS SAE method. Although trimethylgallium (TMGa) and triethylgallium (TEGa) are two most commonly used precursors for the epitaxy of planar GaAs, GaAs nanowires are typically grown by using TMGa sources [19, 34, 36, 37] and the use of TEGa sources is limited[38]. In fact, TEGa is known to have much lower decomposition temperature and also much lower vapor pressure than TMGa, which make TEGa to be more suitable than TMGa when low growth temperature or slow growth rate is desirable[39, 40]. More importantly, the concentration of carbon impurities in GaAs can be significantly reduced when TEGa is used, regardless of the group-V precursors used[39, 41]. Despite these advantages, there have been no studies on GaAs nanowires grown by a SAE technique using a TEGa source. In this chapter, we demonstrate SAE of GaAs nanowires using TEGa and tertiarybutylarsine (TBAs) sources.

Lightly p-doped (Boron, 10−20 Ω-cm) Si (111) wafers are utilized to grow GaAs nanowires. First, 20 nm-thick silicon nitride films are deposited on Si wafers as growth masks by

low-pressure chemical vapor deposition (LPCVD). Stoichiometric deposition condition at 700 ℃ is used to form Si_3N_4 masks. Then, nanoholes are patterned by electron-beam lithography. For this, ZEP520A e-beam resist is diluted with ZEP-A thinner with 1 : 2 ratio and spin-coated at 4000 rpm for 45 seconds. The resist is pre-baked at 180 ℃ for 2 minutes, which results in an approximate resist thickness of 90 nm and exposed by electron beam using Vistec EBPG 5000+ES equipment with the writing resolution of 5 nm and the dose of 550 μC/cm^2. The resist is then developed using ZED-N50 at room temperature for 2 minutes. Next, the substrate is dry-etched to expose nanoholes for SAE using an inductive reactive-ion etching (RIE) equipment, Oxford Plasmalab 80 Plus. For the nanohole etching, CHF_3 of 98 sccm and O_2 of 2 sccm is supplied for 160 seconds at a chamber pressure of 35 mTorr and RF power of 50 W. After the etching, the wafer is diced into 7 × 7 mm^2 size pieces, where AZ5214 resist is spin-coated on the wafer to protect the wafer from dicing particles. After the dicing, the photoresist and e-beam resist are cleaned by wet processes using acetone, NMP and piranha solutions, in sequence, and then by O_2 plasma using Matrix Plasma Asher. A scanning-electron microscopy (SEM) image of prepared sample is shown in Figure 2.1.

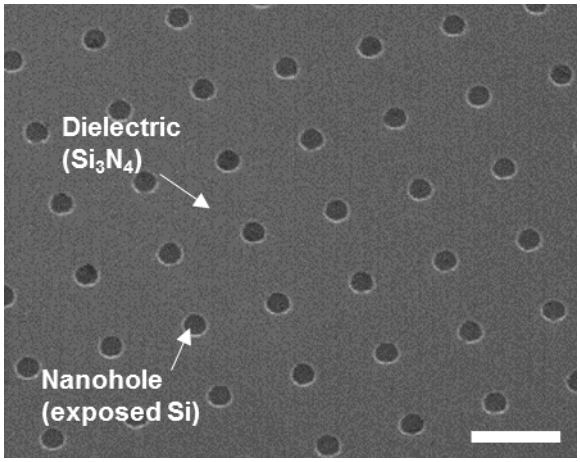

Figure 2.1 30° tilted SEM images of typical nanoholes patterned on silicon. Scale bar, 500 nm.

A low-pressure (60 Torr) vertical MOCVD reactor (Emcore D-75) is used for the growth of nanowires, and hydrogen is used as a carrier gas. Si samples are cleaned by a 6:1 buffered oxide etch (BOE) solution for 30 s followed by water rinsing and drying to remove native oxide right before loading the sample into the reactor. Si pieces are held at 860 °C in the reactor for 10 min under hydrogen ambient to remove native oxide which might have been formed while transferring the sample to the reactor. It should be noted that growing vertical nanowires on Si substrates is not straightforward because GaAs nanowires tend to grow along <111>B directions whereas Si does not exhibit polarity. Nanowires can therefore grow along any of the four exposed <111> directions, which is composed of one vertical <111> direction and three angled <111> directions. To control the growth orientation, TBAs is supplied with a molar flow rate of 7.93×10^{-5} mol/min before initiating the nanowire growth to terminate the exposed Si(111) surface by arsenic and form a (111)B-like surface[42].

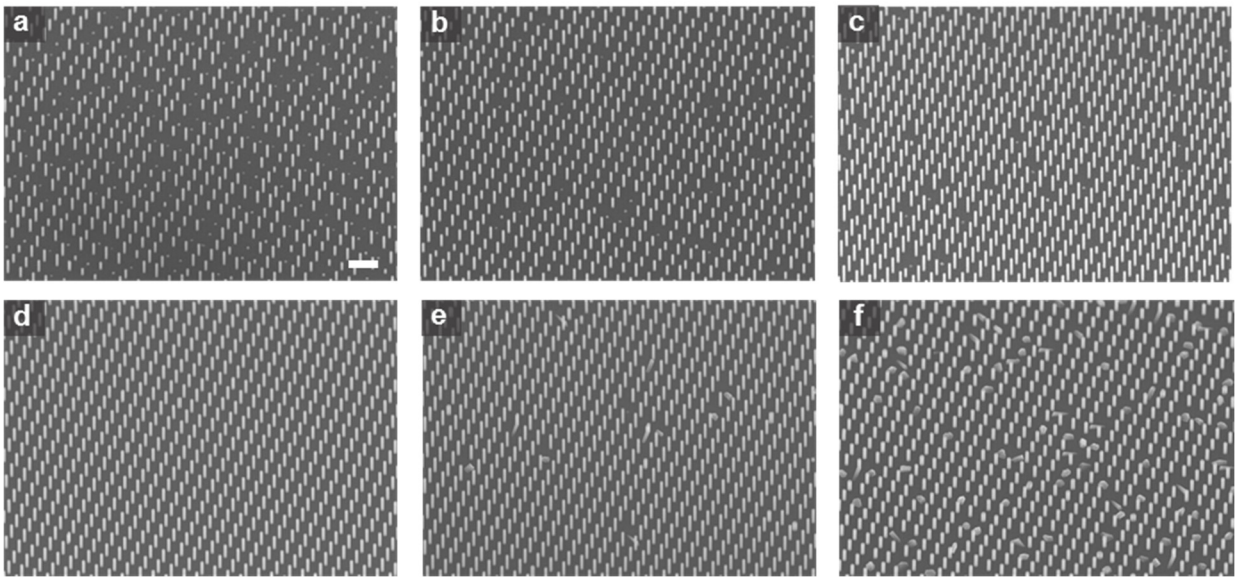

Figure 2.2 30° tilted SEM images of GaAs nanowires grown on Si under various temperatures. The temperatures are (a) 740 °C, (b) 725 °C, (c) 710 °C, (d) 700 °C, (e) 690 °C, (f) 680 °C. The diameter of nanohole openings is 70 nm for all arrays. Scale bar, 1 μm.

The GaAs nanowires are grown on Si under various growth temperatures. As an example, the growth from nanoholes with the diameter of 70 nm and the pitch of 500 nm is shown in Figure 2.2. TBAs is first supplied for 10 min at the growth temperature, followed by the initiation of nanowire growth by turning on TEGa. The TEGa flow rate is fixed to 8.03×10^{-7} mol/min regardless of the growth temperature, and nanowires are grown for 14 minutes. When the temperature is high, the height of nanowires is non-uniform and a significant portion grows as a short stub. The uniformity of nanowires increases by decreasing the temperature, and the vertical growth yield of nanowires reaches close to 100 % at the growth temperature of 700 °C, as depicted in Figure 2.2(d). However, at temperatures lower than 700 °C, the growth along angled <111> directions starts to evolve. The portion of angled nanowires and polycrystalline structures is further increased by decreasing the temperature down to 680 °C. This is attributed to the non-polar nature of Si, whereas angled nanowires are not observed on GaAs substrates regardless of the growth temperatures.

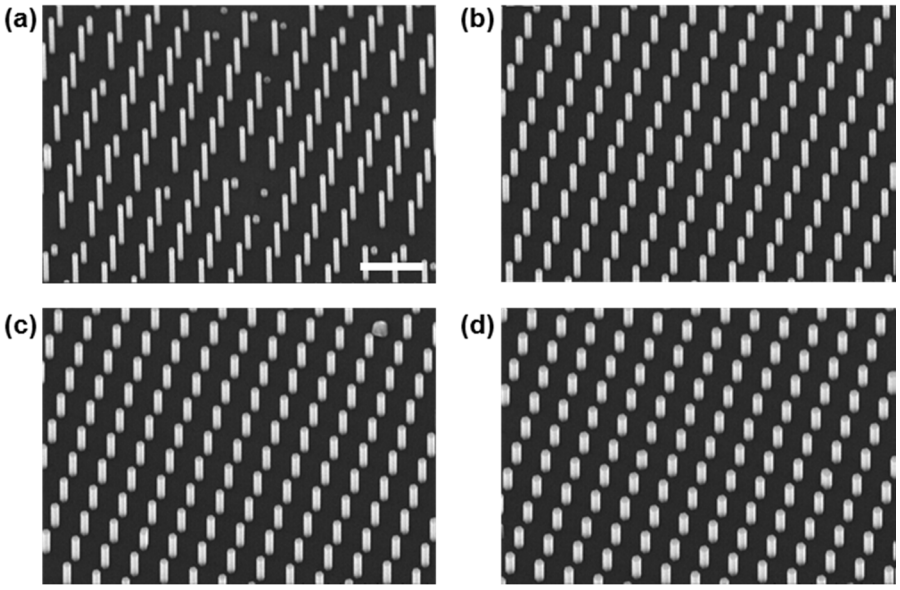

Figure 2.3 30° tilted SEM images of GaAs nanowires grown on Si at 700 °C. The nanohole diameter is (a) 50 nm, (b) 70 nm, (c) 90 nm, (d) 110 nm. Scale bar, 1 μm.

The effect of hole sizes on the vertical growth yield of GaAs nanowires is also studied by patterning nanoholes with different diameters on the same piece. Figure 2.3 shows the SEM images of GaAs nanowires grown for 14 minutes at 700 °C, but from different sizes of nanoholes. Although the growth from 70 nm holes are uniform with 100 % growth yield (Figure 2.3(b)), the growth from smaller holes results in the formation of short stubs (Figure 2.3(a)), which is similar to the growth from larger diameter hole at higher growth temperature, as in Figure 2.2(a-c). The nanowires grown from larger holes show smaller heights and larger diameters, which is typically observed from III-V nanowire grown by SAE techniques[28, 42]. Figure 2.4 shows the nanowire morphology at higher growth temperature of 710 °C. It is more clearly observed that the portion of short stubs is larger at small diameter nanohole arrays, as shown in Figure 2.4(a). The short stubs are not anymore observed from small diameter holes when the temperature is lowered to 680 °C, as shown in Figure 2.5(a), but significant portion of nanowires grows along angled <111>

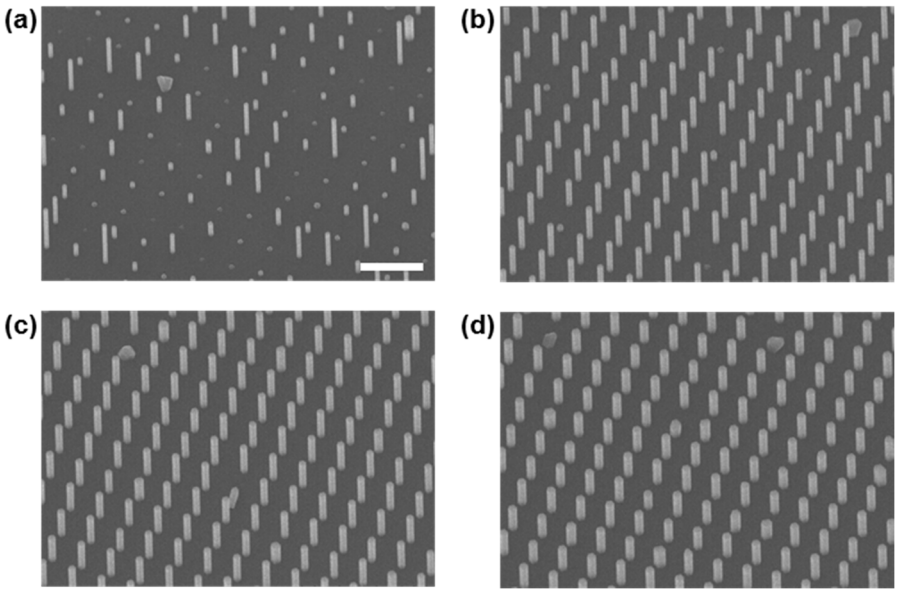

Figure 2.4 30° tilted SEM images of GaAs nanowires grown on Si at 710 °C. The nanohole diameter is (a) 50 nm, (b) 70 nm, (c) 90 nm, (d) 110 nm. Scale bar, 1 μm.

directions regardless of the hole diameter.

The effect of arsenic surface treatment before initiating the GaAs nanowire growth is also studied

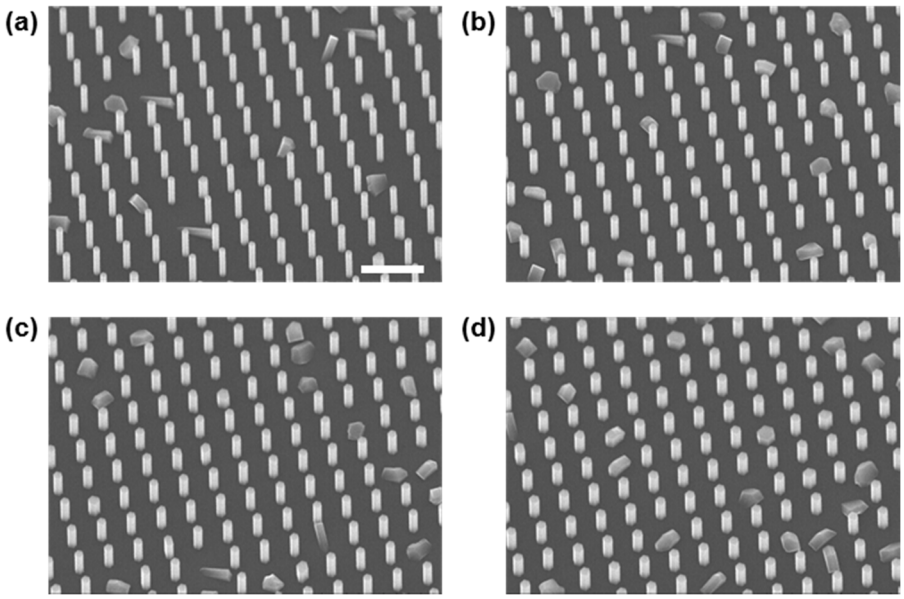

Figure 2.5 30° tilted SEM images of GaAs nanowires grown on Si at 680 °C. The nanohole diameter is (a) 50 nm, (b) 70 nm, (c) 90 nm, (d) 110 nm. Scale bar, 1 μm.

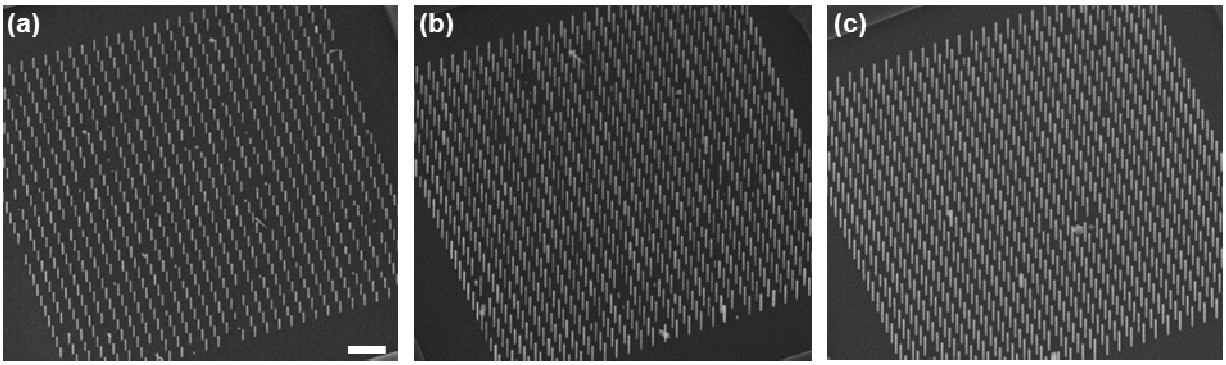

Figure 2.6 30° tilted SEM images of GaAs nanowires grown on Si at 695 °C under various As treatment conditions. The nanohole diameter is 60 nm. (a) 10 minutes of As treatment, (b) 5 minutes of As treatment, (c) No As treatment. Scale bar, 2 μm.

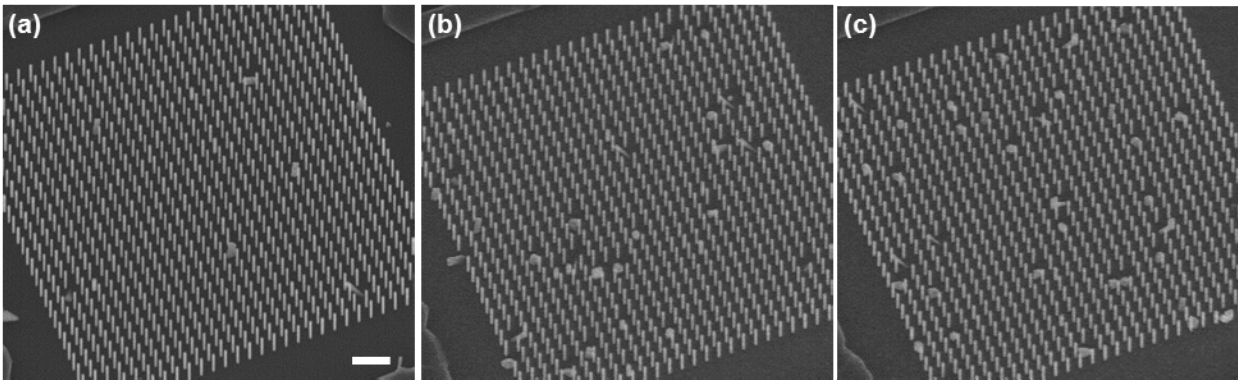

Figure 2.7 30° tilted SEM images of GaAs nanowires grown on Si at 695 °C without As treatment. The nanohole diameter is (a) 60 nm, (b) 70 nm, (c) 80 nm. Scale bar, 2 μm.

by varying the treatment condition. Interestingly, the growth yield shows different trends depending on the nanohole sizes. When the nanohole diameter is as small as 50 nm, the portion of short stubs decreases by reducing the As treatment duration from 10 minutes to 5 minutes (Figure 2.6(a-b)), and further decreased when the As treatment step is removed and TEGa and TBAs are turned on simultaneously (Figure 2.6(c)). However, the vertical growth yield from larger holes becomes worse, as shown in Figure 2.7. In other words, arsenic treatment degrades the growth yields when nanoholes are small, while improves the yields when nanoholes get larger. Although further study is required to understand the origin of such trends, it could be due to the formation of arsenic trimers on nanoholes which varies depending on the hole openings[37].

The growth temperature of GaAs nanowires is a critical parameter that affects the aspect ratio of as-grown nanowires. The growth temperature is varied from 695 °C to 655 °C, whereas TEGa and TMAs flow are kept constant at 7.22×10^{-7} mol/min and 7.93×10^{-5} mol/min, respectively, corresponding to a V/III flow rate ratio of 106. TEGa and TBAs are turned on simultaneously without surface As treatment, and nanowires are grown for 30 minutes. As shown in Figure 2.8, the vertical growth yields are close to 100 % in this temperature range, but the

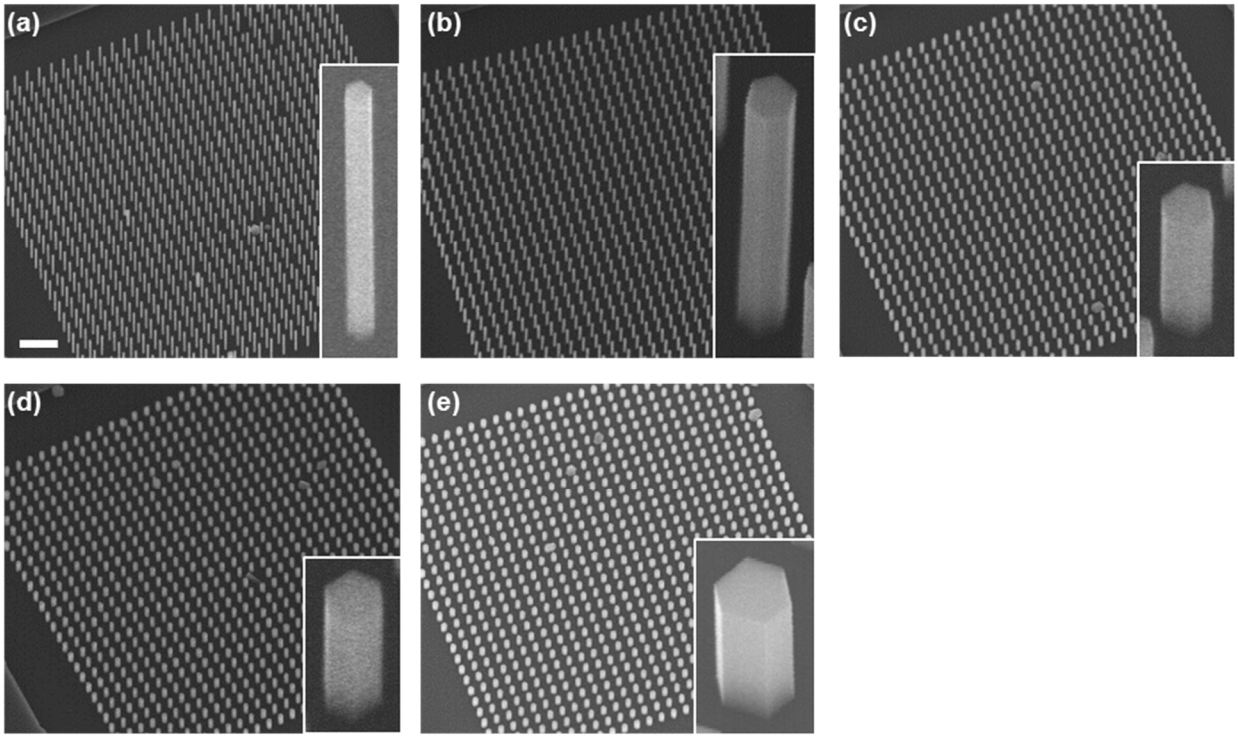

Figure 2.8 30° tilted SEM images of GaAs nanowires grown on Si at different under various temperature. The nanohole diameter is 60 nm. (a) 695 °C, (b) 685 °C, (c) 675 °C, (d) 665 °C, (e) 655 °C. Scale bar, 2 μm. Insets show higher magnification images of each nanowire.

vertical to radial growth rate of nanowires is significantly varied by the growth temperature. At 695 °C, the nanowires exhibit a height of 1950 nm and a diameter of 112 nm, which corresponds to the vertical-to-radial growth rate ratio of 37. The ratio decreases gradually by decreasing the growth temperature, resulting in the ratio of 3.3 at 655 °C (h = 660 nm, d = 262 nm). These results can be explained by considering the growth temperature of epitaxial thin films. The optimum growth temperature of GaAs thin films are typically much lower than the growth temperature of nanowires, and the aspect ratio of nanowires decreases at low temperature since the temperature is closer to the growth temperature of thin films.

The aspect ratio of GaAs nanowires can be also controlled by adjusting the molar flow rate.

The SEM images in Figure 2.9 show GaAs nanowires grown at 655 °C under various flow rates.

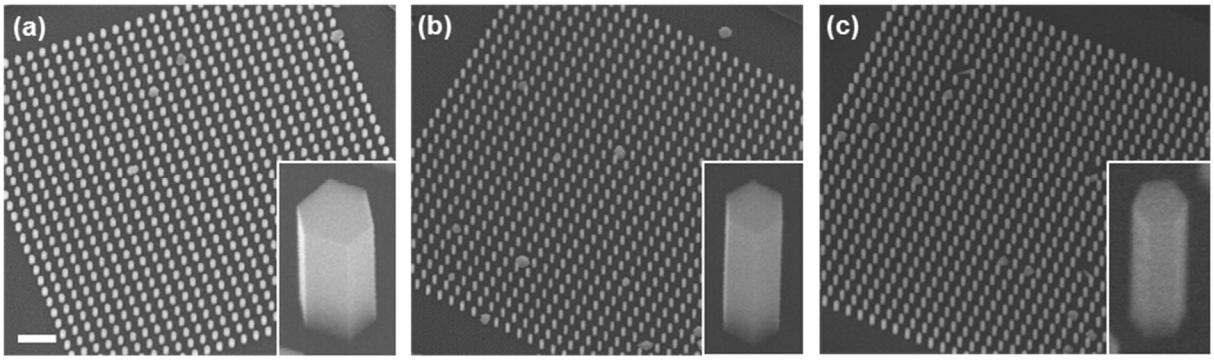

Figure 2.9 30° tilted SEM images of GaAs nanowires grown on Si at 655 °C at various precursor flows. The nanohole diameter is 60 nm. The partial pressure of TEGa and the growth time are (a) 7.22 × 10^{-7} mol/min for 30 minutes, (b) 5.01 × 10^{-7} mol/min for 40 minutes, and (c) 3.91 × 10^{-7} mol/min for 50 minutes, whereas V/III ratio is kept at 106. Scale bar, 2 μm. Insets show higher magnification images of each nanowire.

The TEGa flow rate is decreased from 7.22 × 10^{-7} mol/min (Figure 2.9(a)) to 3.91 × 10^{-7} mol/min (Figure 2.9(c)), where the TBAs flow rate is adjusted accordingly to keep the V/III ratio at 106. The nanowire growth duration is increased from 30 minutes to 50 minutes when the flow rate is decreased. The vertical to radial growth rate ratio increased from 3.3 (h = 660 nm and d = 262 nm, Figure 2.9(a)) to 5.7 (h = 850 nm and d = 210 nm, Figure 2.9(c)) by decreasing the flow of precursors.

In summary, the effects of various growth parameters are studied to achieve controllable growth of GaAs nanowires on silicon. It is shown that the growth yield close to 100 % can be achieved from various nanohole opening sizes, and the aspect ratio of as-grown nanowires can be controlled by adjusting the temperature and flow rates. These results provide a way toward efficient and functional GaAs nanowire-based devices on silicon platforms.

2.2.2 InAs nanowires on silicon

InAs is a direct-bandgap material with very high electron mobility, which is attractive for electronic devices as well as optoelectronic devices. However, the lattice mismatch between InAs and silicon is huge (> 10%), which makes it very challenging to monolithically integrate high-quality InAs thin films on silicon. Because of this limitation, there have been studies on growing InAs nanowires on silicon[43, 44], and demonstrating InAs nanowire-based electronic[45] and optoelectronic devices on silicon[46].

The growth of InAs nanowires on silicon by VS SAE is demonstrated in this chapter. The sample preparation processes are identical with the processes explained in Chapter 2.2.1, including e-beam resist patterning, dry etching, and sample cleaning. A low-pressure (60 Torr) vertical MOCVD reactor (Emcore D-125) is used for the growth of nanowires, and hydrogen is used as a carrier gas. The D-125 reactor has larger volume than D-75 reactor which is used to grow GaAs nanowires (Chapter 2.2.1). Trimethylindium (TMIn) and TBAs are used as precursors. The samples are de-oxidized by BOE solution for 30 seconds before loading the sample into the reactor, and baked at 860 °C in the reactor for 10 min under hydrogen ambient to remove native oxide.

First, the effect of surface treatment by arsenic is studied to optimize the vertical growth yield of nanowires. Only the surface treatment condition is varied, while nanowire growth condition is kept the same. The molar flow rates of TMIn and TBAs are 1.01×10^{-5} mol/min and 9.79×10^{-5} mol/min, respectively, and the nanowires are grown for 2.5 minutes. It has been reported that As treatment at 400 °C greatly improves the vertical growth yield by terminating the surface by As and forming (111)B-like surfaces [43, 44]. According to these reports, the reactor temperature is ramped down to 400 °C after high temperature baking, and the surface is treated with As for 5 minutes, followed by nanowire growth at 595 °C. However, as shown in Figure

2.10(a), the vertical growth yield is very low, and many vacancies, angled nanowires, and polycrystalline structures are observed. The growth yield is improved by increasing the temperature of As treatment to 595 °C (Figure 2.10(b)), but the growth yield degraded when TBAs flow rate for the surface treatment is increased (Figure 2.10(c)). On the contrary, the highest growth yield is achieved by removing the As treatment and turning on TMIn and TBAs simultaneously, as shown in Figure 2.10(d). These results suggest that As treatment does not help the nucleation of InAs inside nanoholes, which contradicts to other reports. It could be due to the formation of As trimer which prevents the adsorption of indium adatoms, although further study is needed to verify this speculation.

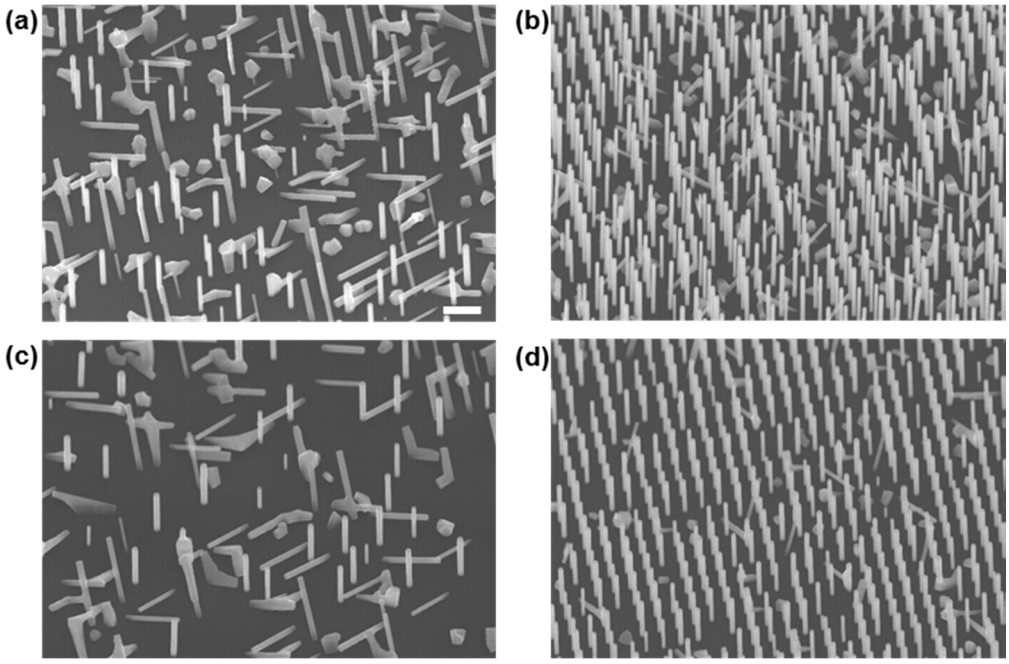

Figure 2.10 30° tilted SEM images of InAs nanowires grown on Si at 595 °C under various As treatment conditions. The nanohole diameter is 50 nm. 5 minutes of As treatment by flowing TBAs of 9.79×10^{-5} mol/min at (a) 400 °C and (b) 595 °C. (c) As treatment at 595 °C for 5 minutes by flowing 4.89×10^{-4} mol/min. (d) No As treatment. Scale bar, 1 μm.

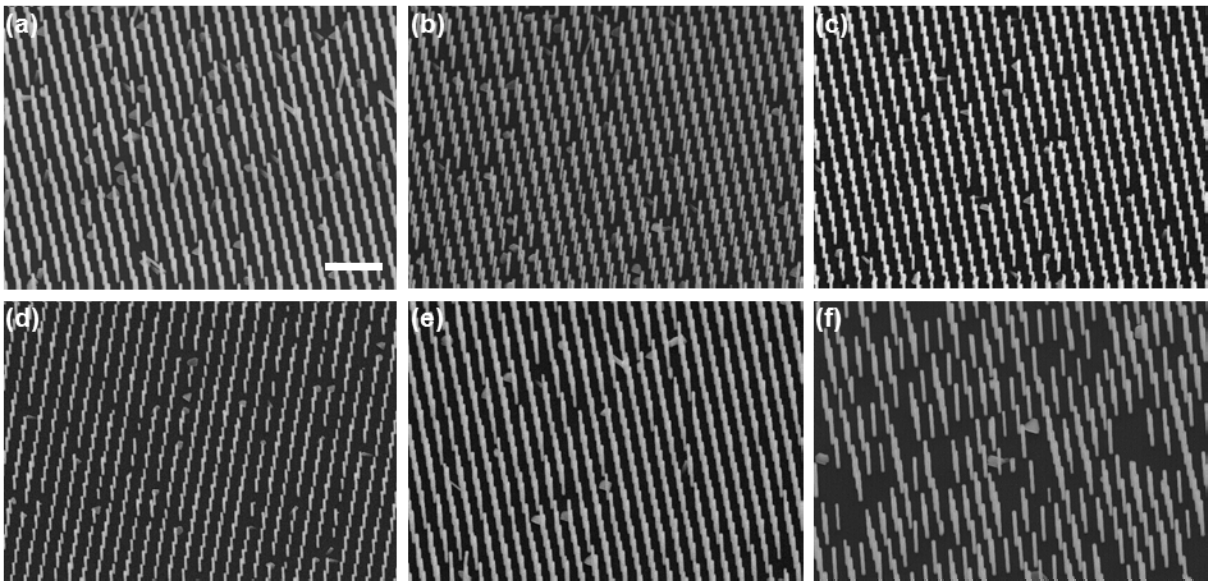

Figure 2.11 30° tilted SEM images of InAs nanowires grown on Si at 610 °C under various TMIn flow rate. The nanohole diameter is 50 nm and TBAs flow is 9.79×10^{-5} mol/min for all growths. TMIn flow is linearly decreased from (a) to (f), where the flow rates are (a) 1.08×10^{-5} mol/min, (b) 9.45×10^{-6} mol/min, (c) 8.10×10^{-6} mol/min, (d) 6.75×10^{-6} mol/min, (e) 5.40×10^{-6} mol/min, and (f) 4.05×10^{-6} mol/min . Scale bar, 2 μm.

Next, the effect of material flow rate on the growth yield is studied. Since As treatment was not effective, TMIn and TBAs are turned on simultaneously for nanowire growth after high temperature baking. The growth temperature is 610 °C for all growths and TBAs flow rate is fixed to 9.79×10^{-5} mol/min. The TMIn flow is gradually decreased from 1.07×10^{-5} mol/min to 4.05×10^{-6} mol/min as shown in Figure 2.11(a-f), whereas the growth duration is gradually increased 2.5 min to 7 min to compensate the decrease of material flow. When the TMIn flow is high, significant portion of nanowires grows along angled <111> direction (Figure 2.11(a-b)). When the TMIn flow is low, the nucleation yield drops and vacancies are observed. Overall, vertical growth yield higher than 90 % is achieved at intermediate flow rates, as shown in Figure 2.11(b-e).

Figure 2.12 30° tilted SEM images of InAs nanowires grown on Si at various temperatures. TMIn and TBAs flow rates are 5.40×10^{-6} mol/min and 9.79×10^{-5} mol/min for all growths. The growth temperatures are (a) 595 °C, (b) 610 °C, and (c) 620 °C. Scale bar, 2 μm.

When the growth temperature is increased from 610 °C to 620 °C, the portion of vacancies significantly increases and nanowires become shorter, as depicted in Figure 2.12(c). On the other hand, the growth yield at 595 °C is similar with the growth at 610 °C, while the nanowire height is increased at low temperature. These results can be attributed to the evaporation of indium adatoms, which is faster at higher temperature and thus leads to the decrease of the effective precursor flow rate.

The optical properties of InAs nanowires are characterized by Fourier-transform infrared (FTIR) spectroscopy. InAs nanowire arrays are optically pumped using a 660 nm solid-state laser, and the emission is measured using a commercial InSb photodetector. The emission from nanowire arrays is measured as a function of temperature, from 77 K to room temperature. To prevent CO_2 and H_2O absorption, the measurement is performed in a nitrogen-purged box. As shown in Figure 2.13, InAs nanowires show strong emission up to 300 K without any *in-situ* or *ex-situ* surface passivation, indicating good material quality of InAs nanowires. Linewidth broadening and redshift of emission spectrum are observed by increasing the temperature, as shown in Figure 2.13(b), due to the temperature dependence of bandgap and thermal motion of carriers. It is

interesting to note that the emission from nanowires is centered around 2.5 μm, while the bandgap of bulk InAs is 398 meV at 77 K, which closely matches with the emission peak of InAs substrates at 3.05 μm (Figure 2.13(a)). This is attributed to the crystal structure of InAs, where bulk InAs exhibits zinc-blende crystals while InAs nanowires typically grows as wurtzite crystal which has larger bandgap than zinc-blende InAs[47].

In summary, the growth of InAs nanowires and their material properties are studied here. It has been shown that the surface treatment, growth temperature and precursor flow are all very important in achieving high vertical growth yield, and optical characteristics of as-grown nanowires suggest that these nanowires have wurtzite crystal structures.

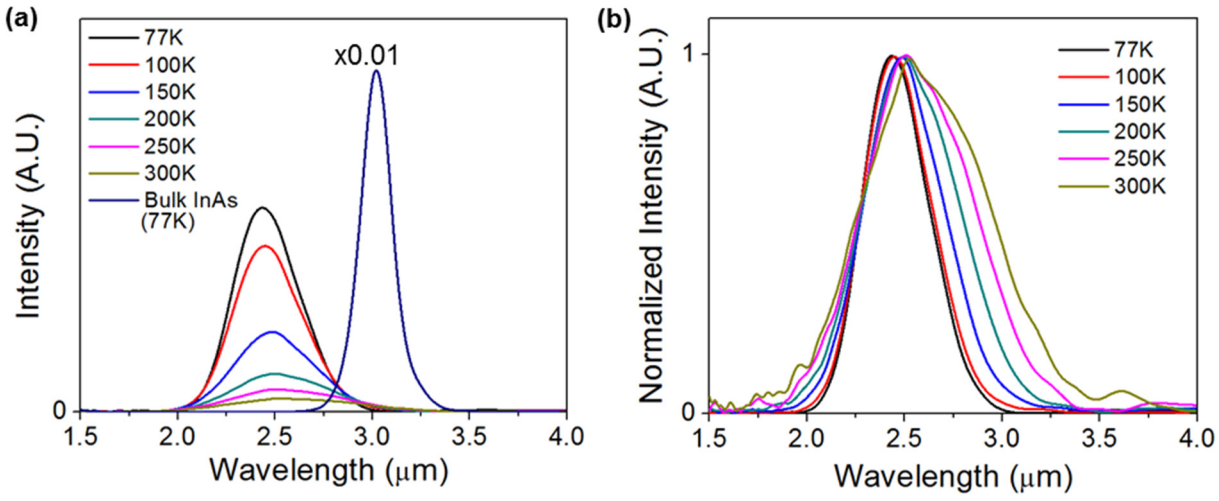

Figure 2.13 Temperature-dependent photoluminescence of InAs nanowires plotted in (a) relative and (b) normalized scales.

2.2.3 InGaAs nanowires on silicon

The growths of two binary compound semiconductor nanowires, GaAs and InAs nanowires, are demonstrated in Chapter 2.2.1 and 2.2.2. InGaAs, which is a ternary of these materials, is an especially attractive material for photonic and optoelectronic devices, since the bandgap and lattice constant can be widely tuned by controlling the material composition. Furthermore, the bandgap of InGaAs covers entire telecommunication bands, which makes the InGaAs-based material platform compatible with fiber optics and communications.

In this chapter, the growth of InGaAs nanowires on silicon-on-insulator by VS SAE is demonstrated. The sample preparation processes are identical with the processes explained in Chapter 2.2.1, except that SOI substrates are used here instead of silicon. The de-oxidation and high-temperature baking processes are also identical as previous growths. Two precursors, TEGa and TMGa, are both tested to grow InGaAs nanowires by MOCVD, in two different reactors.

First, TMGa, TMIn and TBAs are used as precursors for InGaAs nanowire growths. A hydrogen-flow Emcore D-125 reactor is used for MOCVD growth when TMGa is used. The SEM images in Figure 2.14 show the growth results of InGaAs nanowires when the growth temperature is 670 °C and In/(In+Ga) flux is 25 %, assuming that TMIn and TMGa are fully decomposed in the reactor. The growth from small nanoholes resulted in a better nanowire growth yield, roughly 95 % for 40 nm nanoholes. On the other hand, the growth yield is lower in larger nanoholes, which implies that the nanohole opening size is important in the nucleation of nanowires. To tune the material composition of InGaAs nanowires, In/(In+Ga) flux is varied from 25 % to 48 %, while the total group III flow and TBAs flow were kept constant. As shown in Figure 2.15, the nanowire growth yield is higher than 90 % regardless of the In/(In+Ga) flux when the nanowire diameter is small.

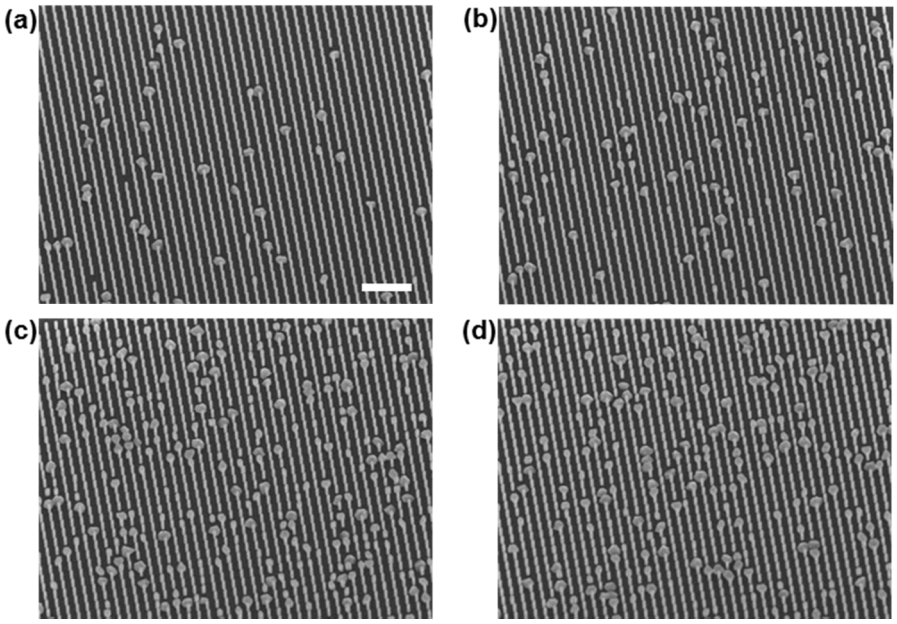

Figure 2.14 30° tilted SEM images of InGaAs nanowires grown on SOI at 670 °C. The TMGa, TMIn and TBAs flow rates are 5.53×10^{-6} mol/min, 1.83×10^{-6} mol/min, and 9.79×10^{-5} mol/min, respectively. Nanohole diameters are (a) 40 nm, (b) 50 nm, (c) 90 nm, and (d) 130 nm. Scale bar, 5 μm.

The optical properties of the InGaAs nanowires grown on the SOI layer under various In/(In+Ga) flux is investigated by FTIR spectroscopy. The nanowire arrays are optically pumped using a 660 nm diode laser with 900 μW pump power, which corresponds to the pump power density of approximately 4.6 kW/cm^2. To prevent CO_2 and H_2O absorption, the measurement is performed in a nitrogen-purged box. Figure 2.16(a) shows the normalized PL spectra of four InGaAs nanowire arrays grown under different In/(In+Ga) flux ranging from 25 % to 48 %. It is found that the peak emission wavelengths vary from 1,175 nm (25 % Indium flux) to 1,755 nm (48 % Indium flux), indicating a wide range of compositional tunability covering telecommunication wavelengths. For more detailed analysis, solid-phase material compositions in the nanowires are calculated from the PL spectra. We applied the Varshni formula and used the

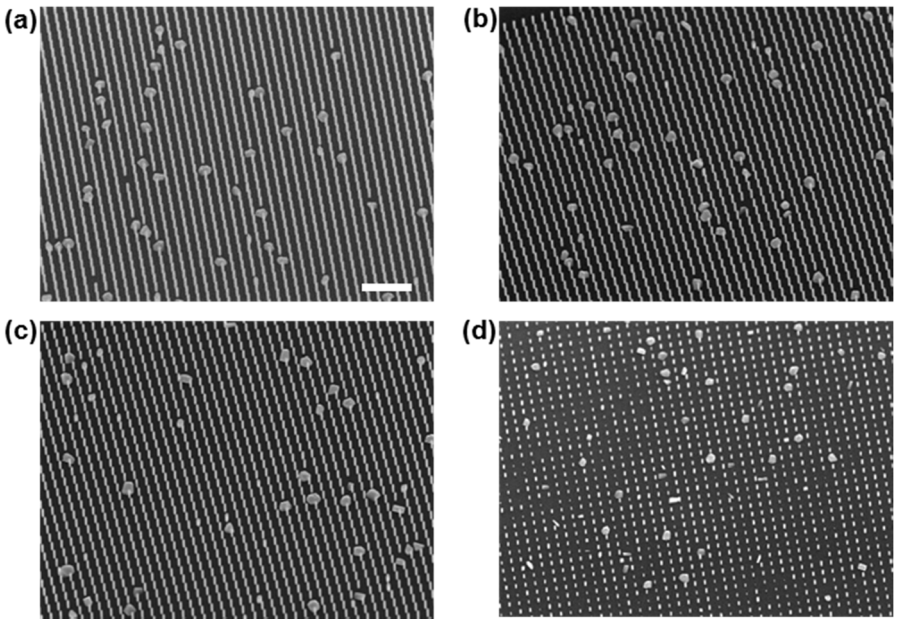

Figure 2.15 30° tilted SEM images of InGaAs nanowires with various material compositions grown on SOI at 670 °C. Nanohole diameters are 40 nm. Gas phase In/(In+Ga) composition is (a) 25 %, (b) 38 %, (c) 43 %, and (d) 48 %. Scale bar, 5 μm.

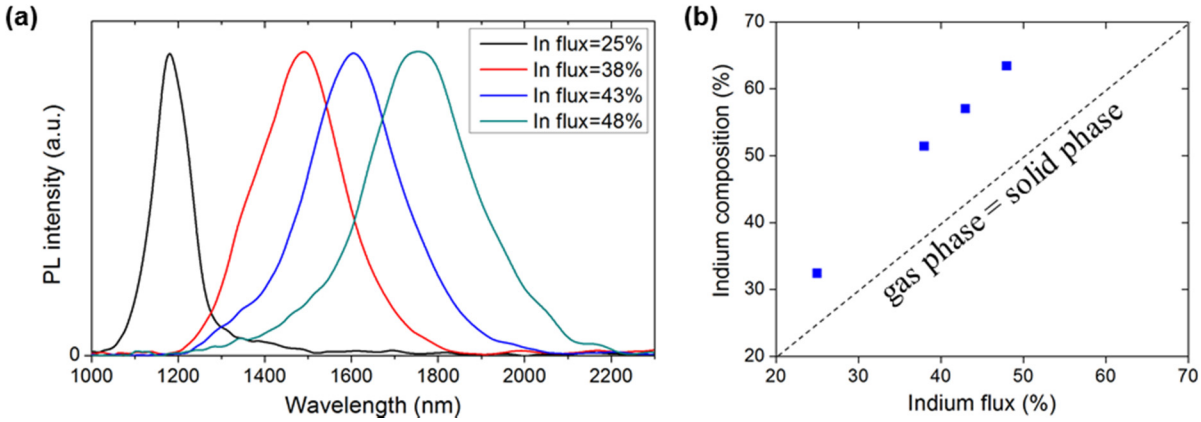

Figure 2.16 (a) Normalized photoluminescence spectra of InGaAs nanowire arrays grown by different In/(In+Ga) flux measured at 77 K. (b) In/(In+Ga) composition of InGaAs nanowire as a function of In/(In+Ga) flux.

bowing parameter of −0.475 eV[48] to derive the Indium composition. Assuming that the bandgap is $k_BT/2$ below the peak emission energy and the strain in the nanowire is fully relaxed, the solid-phase In/(In+Ga) compositions are varied from 32 % ($In_{0.32}Ga_{0.68}As$) to 64 % ($In_{0.64}Ga_{0.36}As$) by changing the Indium flux from 25 % to 48 % as shown in Figure 2.16(b). k_B and T denote the Boltzmann constant and the temperature, respectively. In other words, we have successfully demonstrated the InGaAs nanowires with intermediate In and Ga compositions covering telecommunication wavelengths.

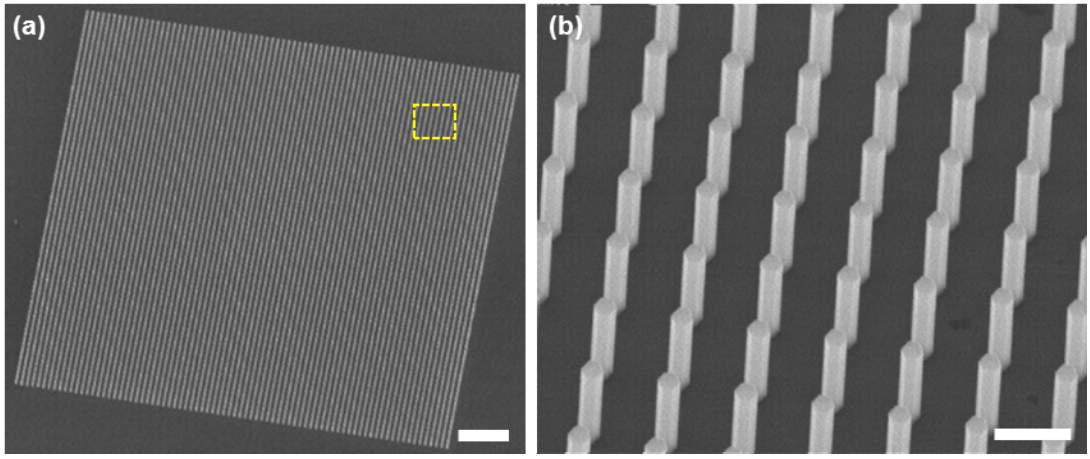

Figure 2.17 (a) 30° tilted SEM images of InGaAs nanowires grown on a GaAs substrate. Scale bar, 5 μm. (b) Close-up image of dashed box in (a). Scale bar, 500 nm.

Next, TEGa is used for InGaAs nanowire growths, instead of TMGa source. TMIn, TBAs, and tertiarybutylphosphine (TBP) are used with TEGa to growth InGaAs nanowires and In(Ga)P shells. An Emcore D-75 reactor is used for MOCVD growth. Notably, the optimum growth condition for InGaAs nanowires turns out to be significantly different from the case of using TMGa source. Also, the growth on silicon or SOI substrates has shown completely different tendency from the growth on GaAs substrates. As an example, Figure 2.17 shows SEM images of InGaAs

nanowires grown on a GaAs substrate with 60 nm nanoholes. The nanowires are grown at 680 °C for 17 minutes, by flowing TEGa = 8.08×10^{-7} mol/min, TMIn = 3.41×10^{-7} mol/min, and TBAs = 2.86×10^{-5} mol/min, which corresponds to In/(In+Ga) flux of 30 %. TBAs is flown before initiating the nanowire growth to prevent the desorption arsenic from GaAs substrates. The nanowire growth yield is close to 100 % and the dimension of nanowires are uniform.

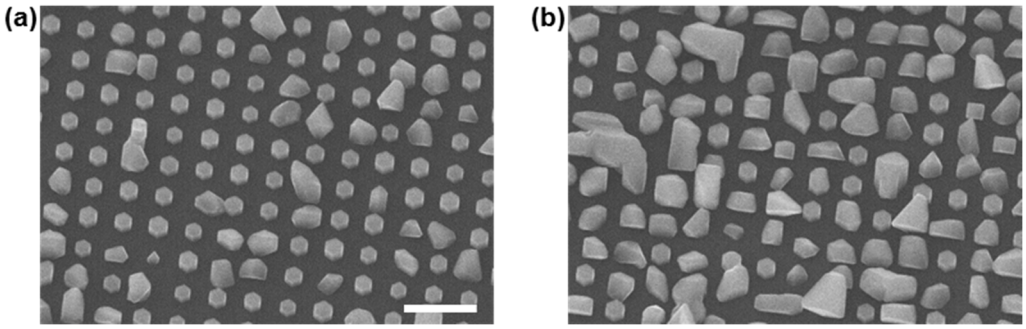

Figure 2.18 30° tilted SEM images of InGaAs nanowires grown on an SOI substrate. Nanohole diameters are (a) 50 nm and (b) 70 nm. Scale bar, 1 μm.

On the other hand, the growth yield of InGaAs nanowires significantly degrades when grown on an SOI substrate, as shown in Figure 2.18. The molar flow rates of precursors are the same with the growth condition on GaAs substrates (Figure 2.17), while high-temperature baking is added and As surface treatment is removed since the substrate is Si. The nanowire growth yield is low and nanowires are very short, regardless of nanohole sizes. These results imply that the nucleation of InGaAs on silicon is not as effective as the nucleation on GaAs. Unlike the case of InGaAs nanowires, the growth yield of GaAs nanowires on silicon can reach almost 100 %, as demonstrated in Chapter 2.2.1. Therefore, it can be inferred that starting the nanowire growth from GaAs (seeding), and then switching to InGaAs (elongation) could achieve high vertical growth yield of InGaAs nanowires on silicon platforms.

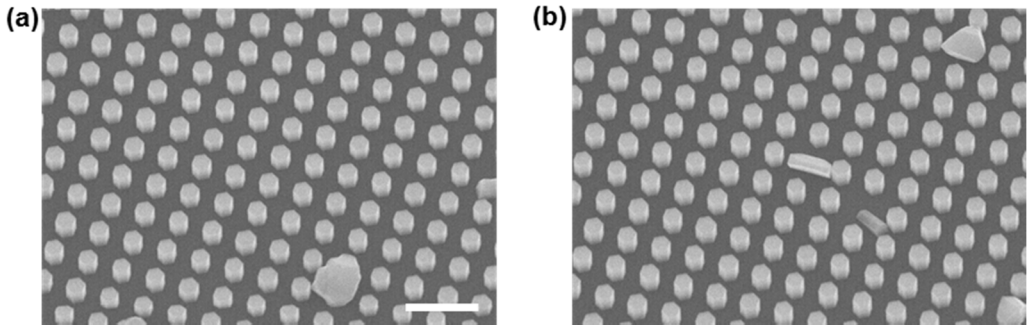

Figure 2.19 30° tilted SEM images of InGaAs nanowires grown on an SOI substrate by inserting GaAs seeding. Nanohole diameters are (a) 50 nm and (b) 70 nm. Scale bar, 1 μm.

To verify this, GaAs seeding is studied to grow InGaAs nanowires with high growth yield. Figure 2.19 shows the InGaAs nanowires grown under the same condition as the case in Figure 2.18, except that GaAs seeding step is added before starting the InGaAs growth. For GaAs seeding, TEGa of 8.78×10^{-7} mol/min and TBAs of 2.83×10^{-5} mol/min are flown for 3 minutes, followed by InGaAs growth without interval. The nanowire growth yield dramatically improves by introducing GaAs seeding, for both 50 nm and 70 nm nanoholes. However, nanowires grow as fat pillars under this growth condition, which is not desirable in applications requiring tall nanowires or axial heterostructures. As it is well-known that V/III flow rate ratio affects the vertical and radial growth rates of nanowire differently[49], the V/III ratio is varied to alter the aspect ratio of nanowires. The V/III ratio is increased from 32 to 69 by keeping the TEGa flow constant and increasing the TBAs flow, and the vertical to radial growth rate is increased at higher V/III ratio, as shown in Figure 2.20. These results show that InGaAs nanowires with high vertical growth yield and high aspect ratio can be grown on silicon platforms.

Next, the composition of InGaAs is varied to cover telecommunication wavelengths, while keeping the aspect ratio of nanowires high. We have found that the optimum growth temperature

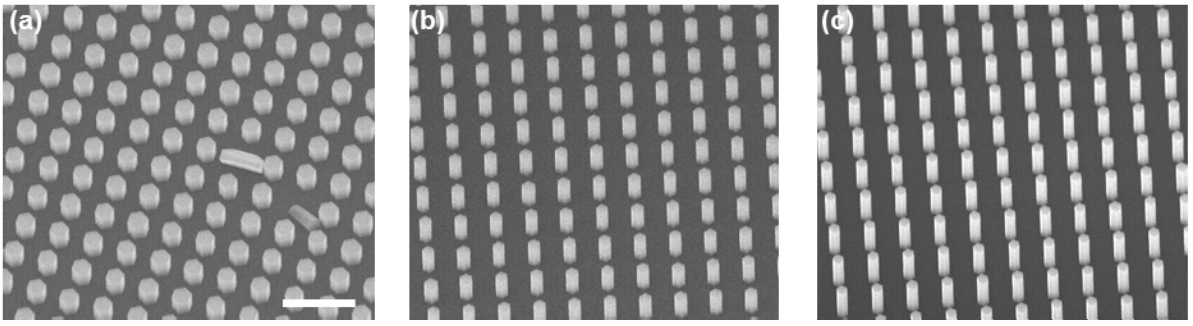

Figure 2.20 30° tilted SEM images of InGaAs nanowires grown on an SOI substrate under various V/III flow rate ratio. The nanohole diameter is 70 nm and the V/III ratio is (a) 32, (b) 49, and (c) 69. Scale bar, 1 μm.

of InGaAs nanowires is lower if indium portion is increased, which agrees with other reports[50]. On the other hand, the GaAs seeding condition is optimized at 680 °C in our study. To benefit from the GaAs seeding, therefore, two-temperature growth of nanowires is studied to achieve InGaAs nanowires with both high indium composition and high yield. First, a thin GaAs seed layer is grown in nanoholes at 680 ˚C. Next, the temperature is ramped down and InGaAs nanowires are grown on top of the GaAs seeding layer, to achieve high indium composition in nanowires. For even higher indium portion, the temperature is further decreased. To total group III flow rate and TBAs flow rate are kept constant, while the ratio between TEGa and TMIn is adjusted to change the gas phase composition. Figure 2.21(a-d) shows the growth results under various InGaAs growth conditions while using the same seeding condition at 680 ˚C. The growth temperature is ramped down from 680 ˚C to 655 ˚C when the gas phase indium composition (TMIn/(TMIn+TEGa)) is increased from 30 % to 40 % (Figure 2.21(b)). Next, InGaAs nanowires with gas phase indium composition of 45 % is grown at two different temperatures, 655 ˚C and 635 ˚C (Figure 2.21(c-d)). After the nanowire growth, InGaAs nanowires are capped by thin In(Ga)P shells to improve luminescence efficiency. The shells are grown at 600 ˚C for 35 seconds

and the lattice constant of InGaP shells are closely lattice-matched with the InGaAs core. The molar flow rates for InGaP shells are TEGa = 8.83×10^{-8} mol/min, TMIn = 2.60×10^{-7} mol/min, TBP = 1.67×10^{-5} mol/min in Figure 2.21(a) and TEGa = 6.91×10^{-8} mol/min, TMIn = 4.63×10^{-7} mol/min, TBP = 1.67×10^{-5} mol/min in Figure 2.21(b). For the nanowires in Figure 2.21(c) and (d), InP shells are grown by flowing TMIn = 4.04×10^{-7} mol/min and TBP = 6.09×10^{-5} mol/min.

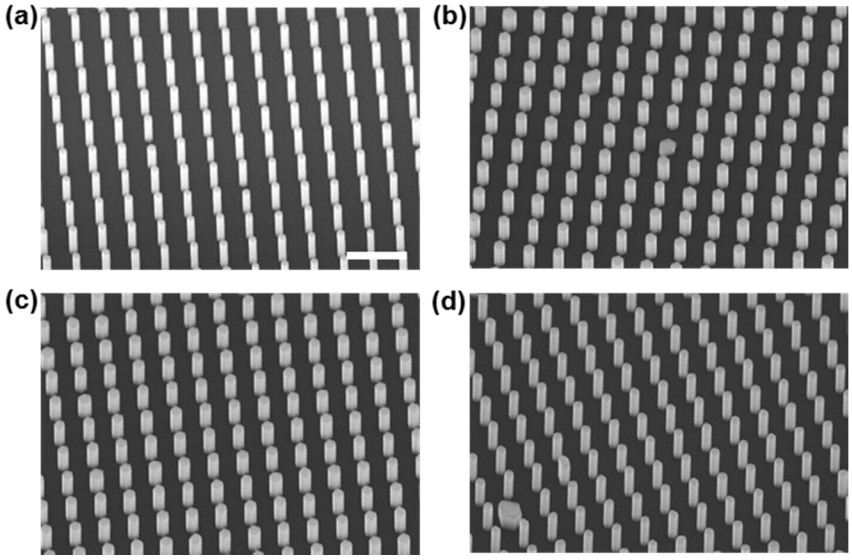

Figure 2.21 30° tilted SEM images of InGaAs nanowires grown on an SOI substrate under various material compositions. Gas phase indium compositions and growth temperatures are (a) 30 % at 680 °C, (b) 40 % at 665 °C, (c) 45 % at 655 °C, and (d) 45 % at 635 °C. Scale bar, 1 μm.

The photoluminescence (PL) spectra of nanowires are measured at room temperature using a spectrometer (SP-2500i, Princeton Instruments) and an InGaAs focal plane array detector (2D-OMA, Princeton Instruments) to deduce the material composition of nanowires. A pulsed laser with 660 nm wavelength (SuperK EXTREME EXW-12, NKT Photonics) is focused vertically onto the nanowires using a 50× objective lens (NA = 0.42) for excitation, and the emission from

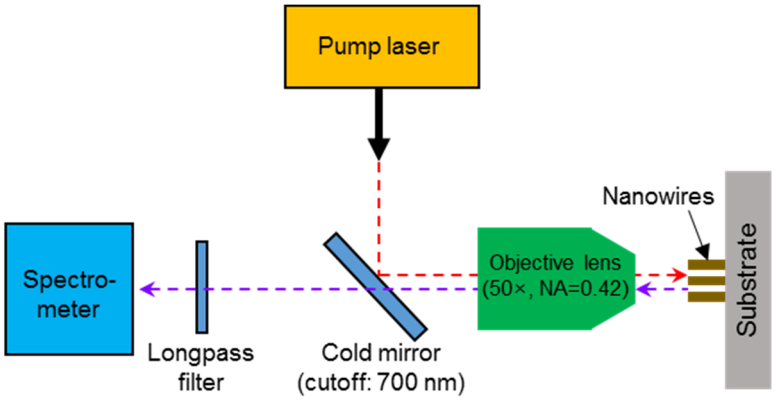

Figure 2.22 Schematic of the setup for photoluminescence measurements (drawing not to scale). The same objective lens is used to focus the pump laser onto nanowires and to collect the emission from nanowires.

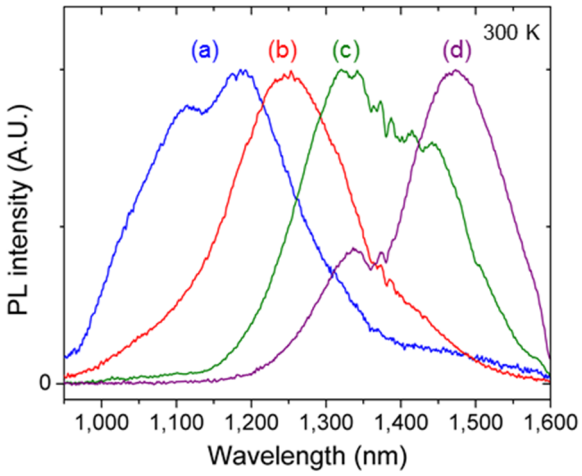

Figure 2.23 Normalized PL spectra of InGaAs nanowire arrays shown in Figure 2.21.

nanowires are collected by the same lens and resolved by the spectrometer, as depicted in Figure 2.22. The emission peak positions are observed around 1,150 nm, 1,240 nm, 1,370 nm, and 1,470 nm for the samples grown under different conditions, which correspond to approximate solid phase indium composition of 0.26, 0.33, 0.42, and 0.48, respectively. Atmospheric absorption around

1,150 nm and 1,400 nm distorts the shape of the PL spectra in Figure 2.23. To further elucidate the emission characteristics of InGaAs nanowires, temperature-dependent PL measurement is performed from $In_{0.42}GaAs$ nanowires. Nanowires are pumped by a continuous-wave 632 nm He-Ne laser with an average power of 12 μW. Thermal broadening of spectra is observed from temperature-dependent PL (Figure 2.24(a)), and the full-width at half-maximum (FWHM) of linewidths is around 70 meV broader than theory regardless of the temperature (inset in Figure 2.24(b)), which is attributed to compositional non-uniformity and wurtzite/zinc-blende polytypism.

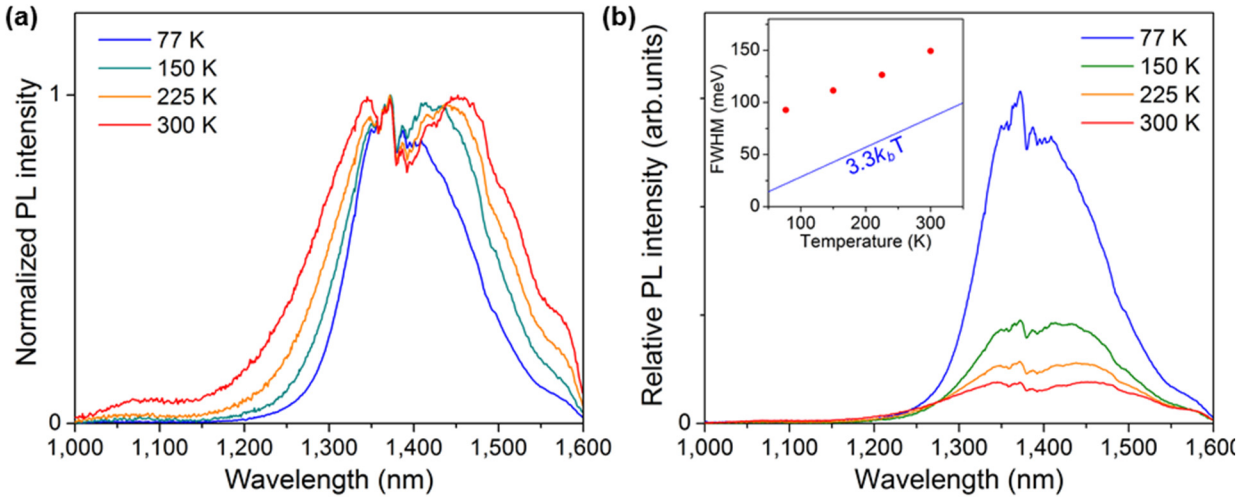

Figure 2.24 PL spectra of an InGaAs nanowire array plotted in (a) normalized and (b) relative scales. Inset: FWHM of nanowires (red dots) compared with theoretical temperature-dependent linewidths of band-to-band transition (blue line).

In summary, InGaAs nanowires with high vertical growth yield are successfully grown on silicon by MOCVD, using both TMGa and TEGa precursors. The composition of indium in InGaAs nanowires is widely tunable covering telecommunication wavelengths, with indium portion in the range of 32−64 % when TMGa is used and 26−48 % when TEGa used. Effective *in-*

situ passivation of InGaAs nanowires by InGaP shell is also developed, which leads to strong room-temperature luminescence.

2.3 Nanowire integration on 3D structured silicon platforms

Although the growth of III-V nanowires on silicon has been demonstrated in previous chapters and also by other research groups, practical integration of nanowire-based devices with silicon photonic chips is still challenging. In order to utilize nanowires for full optical links, it is essential that nanowire-based active components are integrated on 3D structured SOI substrates with other components, such as waveguides and gratings. This concept is schematically illustrated in Figure 2.25. The nanowire arrays grown on planar substrates, which is the most straightforward structure as shown in Figure 2.25(a), can be used not only as passive photonic crystal devices[51], but also as photonic crystal lasers[52], which will be discussed in detail in Chapter 3. Nanowires on gratings, which are shown in Figure 2.25(b), can greatly improve the Q factor of photonic crystal cavities in standard-thickness SOI photonic platforms, which will be discussed in Chapter 4. Lastly, a single nanowire standing on an SOI rib waveguide (Figure 2.25(c)) can be used either

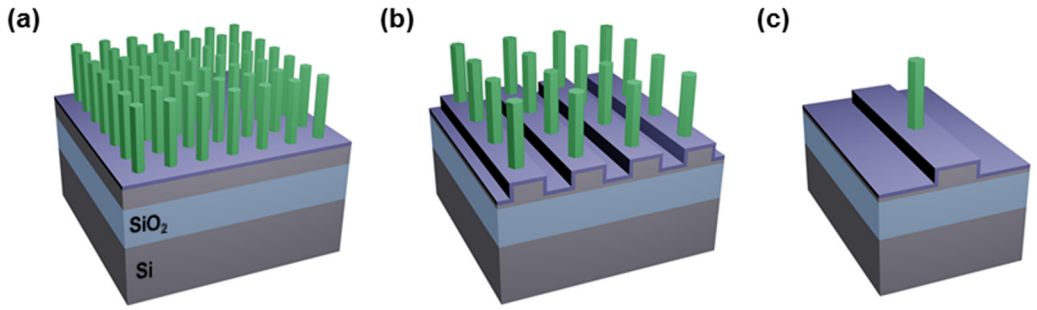

Figure 2.25 Schematic illustrations of InGaAs nanowires on SOI platform. (a) Nanowire arrays on planar SOI, (b) nanowire arrays on a grating structure, and (c) a single nanowire on a waveguide structure.

as (1) a compact light source where the emitted light is directly coupled into the underlying waveguide, and/or (2) a photodetector having a sub-micron size and ultra-low capacitance for energy-efficient on-chip links, which can substitute current Ge-based photodetectors having the size of ~10 μm (length) × 2 μm (width) × 0.25 μm (height)[53]. The fabrication, epitaxy and characterization of nanowires on 3D structured SOI platforms are introduced in this chapter.

To demonstrate the proposed nanowire-based SOI platform, a lightly p-doped (Boron, 10 Ω.cm) SOI (111) wafer with an SOI layer thickness of 2 μm, a buried oxide (BOx) layer thickness of 2 μm, and a Si substrate thickness of 675 μm is used for the nanowire growth. First, the SOI layer thickness is reduced from 2 μm to 220 nm. We have adopted thermal oxidation process to reduce the thickness of the SOI layer, because other thinning processes such as wet chemical etching and dry etching typically degrade the surface roughness of the SOI layer. Following the wet oxidation carried out at 1050 ˚C, the as-grown thermal oxide is removed using a 6:1 buffered oxide etch (BOE) solution (Figure 2.26(b-c)). Next, 3D structures including waveguides, gratings, and alignment markers are patterned on the thinned SOI layer by e-beam lithography and dry etching processes. E-beam resist, ZEP520A diluted with ZEP-A by the ratio of 2:1, is spin-coated on the thinned SOI wafer, followed by e-beam writing and developing using ZED-N50, as shown in Figure 2.26(d). Then, dry etching is carried out using the e-beam resist as an etch-mask. The SOI layer is etched using an ICP etcher (Oxford 80Plus) by flowing 10 sccm of SF_6, 25 sccm of CHF_3, and 2 sccm of O_2 under the RF power of 200 W and the chamber pressure of 30 mTorr. The depth of the trench is controlled to be 180 nm. The etch-mask is removed after the dry etching, as shown in Figure 2.26(e), by N-Methyl-2-pyrrolidone (NMP) rinsing and piranha cleaning. Then, for a nanowire growth mask, a 20 nm-thick Si_3N_4 film is deposited using low-pressure chemical vapor deposition (LPCVD), followed by spin-coating e-beam resist (ZEP520A diluted with ZEP-

A by the ratio of 1:2) on the wafer. The dilution ratio is different from the e-beam resist employed for the 3D structure patterning, because the nanohole size is on the order of tens of nanometers, requiring thinner e-beam resist for fine resolution. Next, e-beam writing is carried out to pattern nanoholes, employing the alignment markers patterned on the substrate to precisely align the position of the nanoholes on the 3D structures. The alignment error was less than 20 nm in our system. After developing the e-beam resist using ZED N-50, dry etching is carried out to expose nanoholes on the Si_3N_4 mask. The Si_3N_4 mask is patterned using an ICP etcher (Oxford 80Plus) by flowing 98 sccm of CHF_3 and 2 sccm of O_2 under the RF power of 50 W and the chamber pressure of 35 mTorr. Finally, the 6-inch wafer is diced into square-shaped samples and the resist is stripped by wet chemical etching.

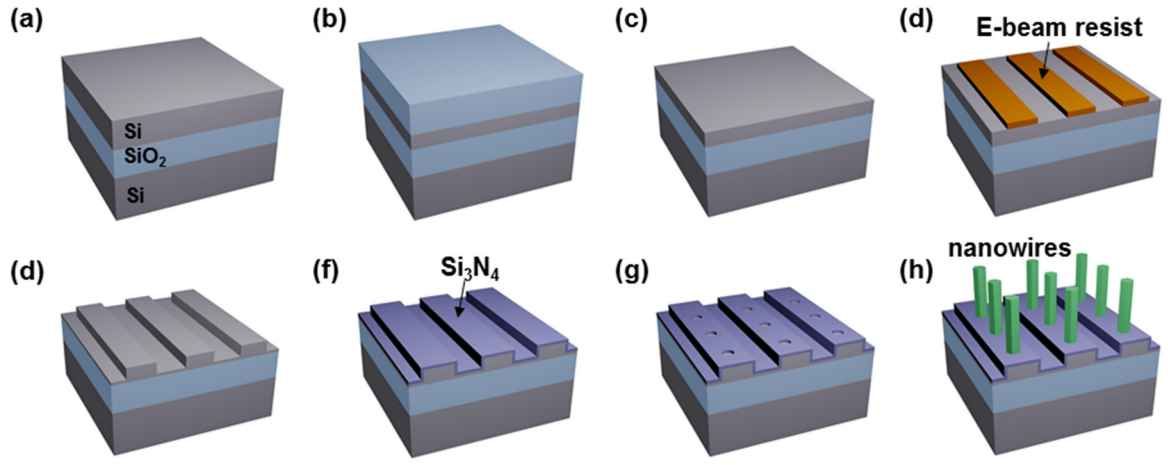

Figure 2.26 Fabrication process for InGaAs nanowires on SOI platform.

The SEM images in Figure 2.27 show the fabricated 3D structured SOI platforms with nanoholes. Nanoholes are patterned on 1D and 2D gratings with fine alignment, which provides a platform for nanowires on 3D structured SOI. Since the growth of binary III-V materials is

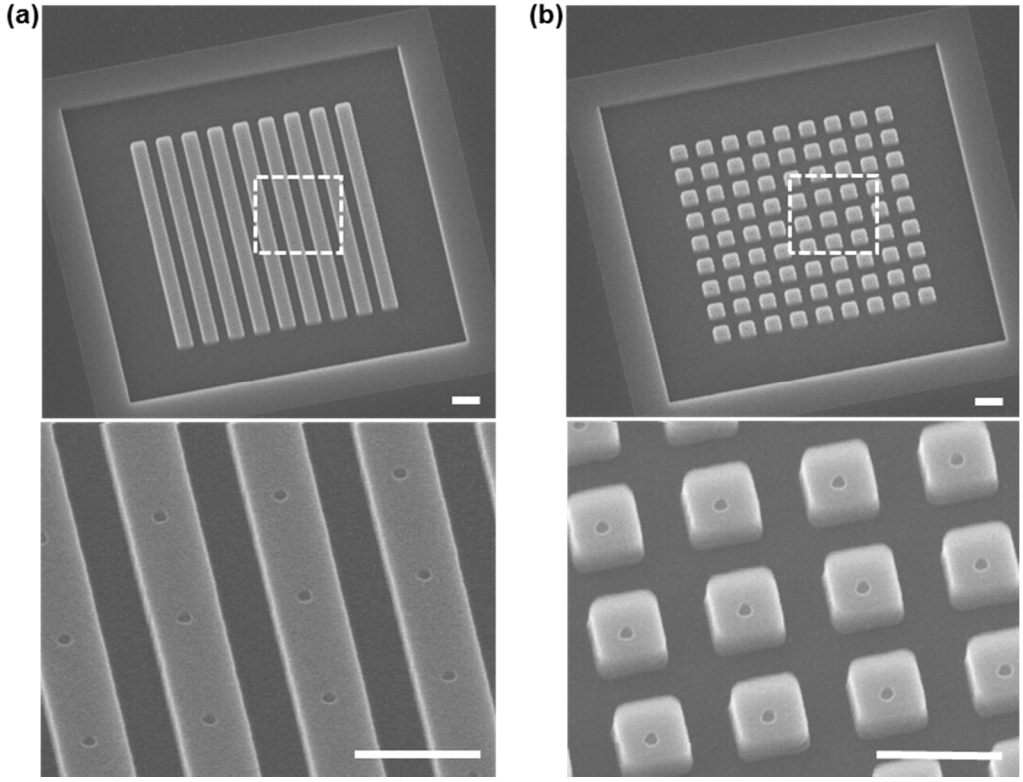

Figure 2.27 30° tilted SEM images of fabricated 3D structured SOI. Nanoholes patterned on (a) 1D gratings and (b) 2D gratings. (Lower) Close-up images of dashed area. Scale bar, 500 nm.

typically more straightforward than ternary III-V materials, growths of InAs nanowires and GaAs nanowires on the patterned SOI are studied first. Figure 2.28(a) shows InAs nanowires grown on 1D gratings, wherein the growth condition of InAs nanowires is identical with the growth shown in Figure 2.11(e) of Chapter 2.2.2. 100 % nanowire growth yield is achieved on 1D gratings, proving that it is possible to grow nanowires with high yield on pre-patterned SOI platforms. Similarly, the growth of GaAs nanowires with 100 % yield is realized on 2D gratings (Figure 2.28(b)), wherein the growth condition is identical with the growth shown in Figure 2.2(c) of Chapter 2.2.1. These results suggest that the growth condition used for nanowire epitaxy on planar substrates can still be applied to grow nanowires on 3D structured substrates.

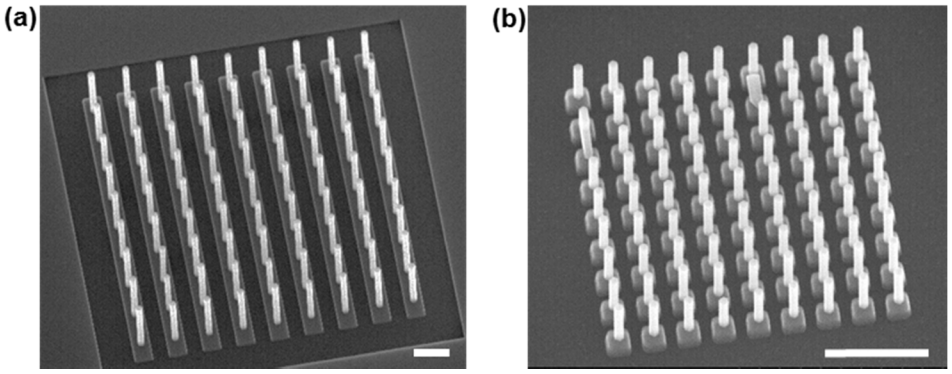

Figure 2.28 30° tilted SEM images of nanowires grown on 3D structured SOI. (a) InAs nanowires and (b) GaAs nanowires. Scale bars, 1 μm.

Next, InGaAs nanowires are grown on the SOI platform, following the growth condition demonstrated in Chapter 2.2.3. Figure 2.29 shows the SEM images of InGaAs nanowires grown under the gas phase indium composition of 43 %. All images are taken from different areas of the same sample, and the diameter of the nanoholes on the mask was 40 nm. The pitch of the nanowire arrays on the planar surface is 1000 nm (Figure 2.29(a)) and 500 nm (Figure 2.29(b)), where the total array size is both 50×50 μm^2. In Figure 2.29(c), the SOI grating has a period of 600 nm, a duty cycle of 50 %, and a total size of 5 × 5 μm^2. The SOI waveguide in Figure 2.29(d) has the width of 440 nm, where a single nanowire is standing on the waveguide center. These arrangements correspond to the schematics in Figure 2.25. This explicitly confirms that it is possible to monolithically integrate InGaAs nanowires on the proposed platform. Given that the position-controlled nanowire growth is achieved regardless of the array size and the substrate structures, such versatility makes the proposed platform very powerful in such a way that various photonics and optoelectronics components can be simultaneously integrated.

Interestingly, the size and the aspect ratio of the nanowires are all similar except for the

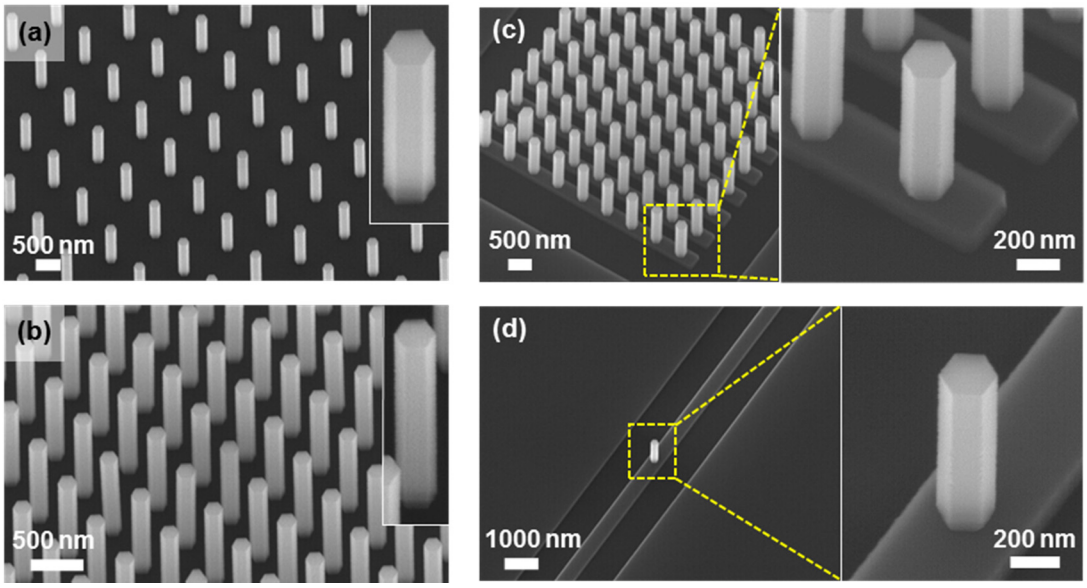

Figure 2.29 SEM images of InGaAs nanowires on an SOI platform. Nanowire arrays on planar areas with (a) 1000 nm pitch and (b) 500 nm pitch. Insets in (a) and (b) show magnified images of nanowires in each array. (c) Nanowire array on a grating structure. (d) Single nanowire on an SOI waveguide structure. All images are tilted 30° from the normal view.

case when nanowires are densely packed in a large array (Figure 2.29(b)). In the cases when the nanowires are sparsely spaced in a large array (Figure 2.29(a)), densely spaced in a small array (Figure 2.29(c)), and when there is only a single nanowire (Figure 2.29(d)), the morphology of the nanowires are all similar, having the diameter of 210 nm and the height of 1100 nm within 6% error. On the other hand, the nanowires densely spaced in a large array (Figure 2.29(b)) show the diameter of 170 nm and the height of 1300 nm, meaning that the nanowires are thinner and taller. Meanwhile, the effect of the substrate trenches on the nanowire morphology is not observed. This can be explained by considering the mechanism of the VS SAE nanowire growth. In the catalyst-free nanowire growth, there are three sources of adatoms contributing to the vertical nanowire growth; (1) adatoms directly incorporating on the top facet of a nanowire, (2) adatoms adsorbed

on the nanowire side facets diffusing to the nanowire tip, and (3) adatoms on the mask surface area diffusing to nearby nanowires; where the contribution from the side facet adsorption dominates the other two sources[28, 54, 55]. Because the amount of adatoms adsorbed on the side facets is identical in the nanowires having the same diameter [54], the dimensions of the nanowires grown from the same size of the nanoholes should also be similar, as evidenced in Figure 2.29(a,c,d). This also clarifies why the trenches around the nanowires do not visibly affect the nanowire growth. Assuming that the trenches do not affect the carrier gas flow on the surface, these trenches act just as additional paths for the adatoms on the mask surface to diffuse. In the same manner, the sidewalls of the trenches can be regarded as additional mask areas. Therefore, the presence of trenches can be interpreted as an increase of the effective mask area per nanowire. Although the effect of trenches on the nanowire morphology is not observed due to the minor contribution of the mask surface diffusion on the growth, we predict that nanowires will grow larger in height and diameter if surrounding trenches are deep enough. To conclude, the effects coming from different array sizes and from the structures on the surfaces are not substantial enough to be reflected on the size of the nanowires.

The remaining question is why the nanowires in a dense and large array (Figure 2.29(b)) grow thinner and taller than the others. We attribute this to increased V/III flow rate ratio around the dense nanowire arrays. The diffusion coefficient of group-III adatoms on the nanowire side facets increases under high As pressure[26], and this leads the III-As nanowires to grow taller and thinner to a certain extent as the V/III flow rate ratio increases[44]. As group-III materials tend to be depleted much faster than arsenic during the competitive absorption process by dense nanowires[56], the local V/III flow rate ratio is the largest around the dense and large array (Figure 2.29(b)), leading to the thinnest and the tallest nanowires. From this observation, we suspect that

the axial growth and lateral overgrowth could be effectively and individually engineered by using proper nanohole arrangements and compensation patterns, which can augment the proposed platform by giving additional flexibility.

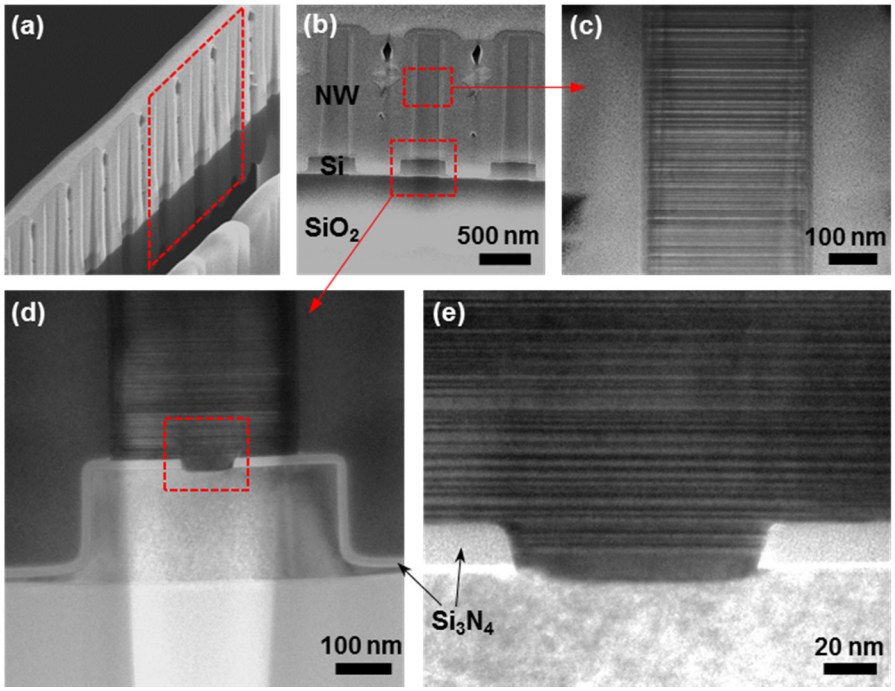

Figure 2.30 (a) Cross-sectional SEM images of an InGaAs nanowire array on a grating structure viewed at an angle. (b) Magnified SEM image of the dashed box in (a) viewed at a horizontal direction. (c) Cross-sectional TEM image of a middle part of a nanowire. (d) TEM image of bottom part of a nanowire. (e) Magnified TEM image of the dashed box in (d).

To investigate the material quality of the InGaAs nanowires on the SOI platform, we performed cross-sectional SEM and transmission electron microscopy (TEM) measurements of the $In_{0.32}GaAs$ nanowires on the SOI grating structure where the diameter of nanoholes for the nanowire growth was 90 nm. The sample is sliced by focused ion beam (FIB) etching for TEM measurements, as shown in Figure 2.30(a). The cross-sectional SEM images in Figure 2.30(a) and

Figure 2.30(b) clearly show the 3D structured SOI layer on top of the buried oxide layer, and also the InGaAs nanowires vertically grown on top of the SOI grating structure with fine alignment. Stacking faults are observed along the nanowire (Figure 2.30(c,d)), which is also reported for InGaAs nanowires grown on Si by VS SAE[18, 47]. Although stacking faults are undesirable crystal defects degrading electrical and optical properties, we believe that the stacking faults can be eliminated by precisely controlling the growth temperature and the V/III flow rate ratio[47]. It is also worth mentioning that there is no threading dislocation observed in Figure 2.30(e) despite the lattice mismatch as large as 6.6 % between InGaAs and Si. In contrast, although a compliant SOI substrate instead of a Si substrate is known to improve the quality of the epitaxial layer grown on top by releasing the strain[57], III-V films grown on SOI substrates still exhibit high density of threading dislocations[58]. This strongly supports our claim that the proposed nanowire-based platform is a promising alternative for the next-generation on-chip photonic and optoelectronic applications.

Lastly, the validity of the proposed platform is substantiated by experimentally showing that InGaAs nanowires can be used as light sources directly coupling into SOI waveguides. A single nanowire standing on an SOI waveguide (Figure 2.31(a)) is optically pumped using a 633 nm He-Ne laser with 1200 μW pump power, which is equivalent to the pump power density of 6.1 kW/cm^2, and the emission spectra are measured on the waveguide edge as well as on top of the nanowire to investigate the coupling characteristics. The emission spectra were measured using an InGaAs focal plane array detector with a 50× objective lens oriented normal to the substrate. The nanowire is positioned on the center of the SOI rib waveguide, where the waveguide has a rib height of 220 nm, a rib width of 440 nm, and a slab height of 40 nm. The length of the waveguide between the nanowire and the waveguide edge is 500 μm, and a grating coupler is patterned at the

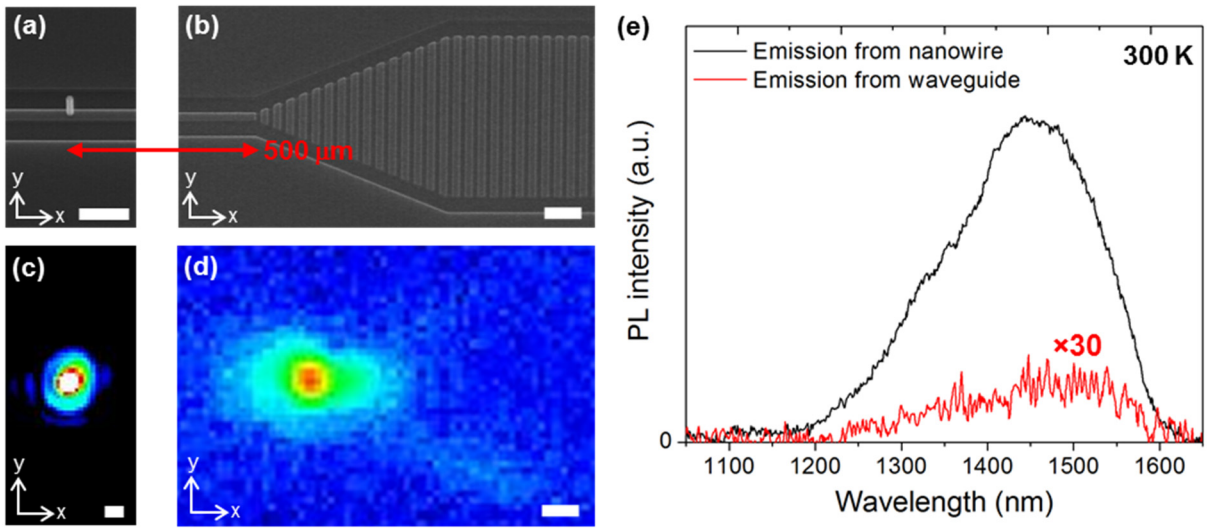

Figure 2.31 SEM images of (a) a single InGaAs nanowire on an SOI waveguide and (b) a waveguide edge. The length of the waveguide is 500 m. Spectrally integrated images measured on (c) the nanowire region and (d) the waveguide edge by optically pumping the nanowire. (e) Photoluminescence spectra measured on the nanowire region and the waveguide edge at room temperature. The emission from the waveguide edge is magnified 30 times for visibility. All scale-bars in (a-d) represent 2 m.

waveguide edge to couple out the light and measure its spectra on the normal direction (Figure 2.31(b)). All measurements were performed at room temperature without nitrogen purging. The spectrally integrated images in Figure 2.31(c) and Figure 2.31(d) represent the spatial emission intensities measured on top of the nanowire and on top of the gratings, respectively. This result explicitly shows that nanowires on SOI waveguides can be employed as active components, such as ultracompact light sources and photodetectors. The nominal efficiency calculated from the spectra in Figure 2.31(e) is 0.57 %, which is derived by dividing the integrated emission intensity measured on the waveguide edge by that on the nanowire. Thus, this efficiency takes into account (1) the coupling-in efficiency, which is the portion of the emitted light coupling into the SOI

waveguide, (2) the propagation loss of the SOI waveguide, and (3) the coupling-out efficiency on the waveguide edge. On the other hand, optical simulations have predicted that the coupling efficiency of a single nanowire emitter with an underlying SOI waveguide will be around 1.0 %. Thus, the measured efficiency reasonably matches with the theoretical efficiency, considering that the sidewall roughness of the SOI waveguide, the coupling-out efficiency on the waveguide edge, and the collection efficiency of the objective lens on top of the nanowire and the waveguide edge are not taken into account in the simulation. We note that although the intensity of the light coupling out of the waveguide is much weaker than the emission measured from the nanowire itself due to the low coupling efficiency, the efficiency can be greatly improved by introducing cavity structures[59].

In conclusion, we have shown that threading dislocation-free InGaAs nanowires can be epitaxially grown on 3D structured SOI layers as well as planar SOI layers with a position controllability. These features allow a high degree of freedom in designing nanowire-based devices such as rod-type photonic crystals. We have also proposed a novel nanowire-based SOI platform for energy-efficient on-chip optical links by demonstrating a single nanowire acting as a light source where the emitted light directly couples into an SOI waveguide. The proposed nanowire-based SOI platform provides the opportunity for the next-generation on-chip optical communication systems.

3. Nanowire photonic crystal lasers

3.1 Overview

Semiconductor nanowires are regarded as an enabling platform to implement ultracompact lasers, which is mainly due to their high material quality and geometry. In specific, their atomically flat end facets and sidewalls naturally provide good optical feedback from end facets and total internal reflection from sidewalls, resulting in Fabry-Perot cavities in single nanowires, whereas high material quality provides enough material gain for lasing. By exploiting these notable features, nanowire lasers operating in ultraviolet, visible, and near-infrared wavelengths have been reported using both III-V and II-VI material systems[34, 60-62]. However, such single-nanowire lasers typically attain optical confinement by transferring the nanowires onto low-index substrates, while achieving lasing from free-standing nanowires on silicon platforms is challenging due to the small index contrast between nanowires and silicon.

Compared with Fabry-Perot cavities, photonic crystal cavities typically provide higher quality factor and tighter mode confinement in sub-wavelength scales. Air-hole type photonic crystals, which are formed by drilling air holes in membranes, have been extensively investigated to realize photonic crystal lasers[63-66]. Although very high Q factor can be achieved from strong out-of-plane confinement by total internal reflection[67], further technological improvements are required to integrate these types of photonic crystal lasers on silicon platforms in large volume. As an alternative approach, rod-type photonic crystal structures are also proposed, employing either top-down or bottom-up approaches. However, achieving vertical confinement is challenging in these structures because a large refractive index difference between the pillars (or rods) and

underlying substrates is required for out-of-plane confinement. Several methods have been reported to satisfy this requirement and demonstrate lasing, such as top-down etched microrod array photonic crystals with multiple quantum wells bonded on a low-index substrate[68], bottom-up nanowire photonic crystals with III-V heterostructures detached from the growth substrate[52], and selectively wet-etched rod photonic crystals with multiple quantum wells on the growth substrate[69].

In this chapter, nanowire array-based photonic crystal cavities on SOI substrates are proposed and lasing from these cavities is demonstrated at room temperature. Two distinctive designs, one-dimensional (1D) 'nanobeam' photonic crystals and 2D photonic crystals, are proposed and demonstrated by selective-area epitaxy of InGaAs nanowires. It is shown that *In-situ* surface passivation of nanowires and the use of SOI layers with adequate thicknesses are essential to achieve high material gain and cavity *Q* factor for low-threshold lasing.

3.2 One-dimensional photonic crystal lasers on SOI

3.2.1 Design

Here, we show a 1D photonic crystal cavity, which is also known as a nanobeam cavity, composed of bottom-up nanowires on SOI substrates. The nanobeam cavity can achieve a high *Q* factor comparable with the 2D counterpart[70, 71], while requiring a much smaller footprint and number of nanowires. The schematic illustration of the 1D nanowire array cavity is shown in Figure 3.1. The nanowire array forms a 1D nanobeam cavity, which employs a photonic bandgap (PBG) in one dimension (*x*-axis) and total internal reflection (TIR) in the other dimensions (*y*- and *z*-axis) to achieve optical confinement. It is already well demonstrated that the artificial defect of

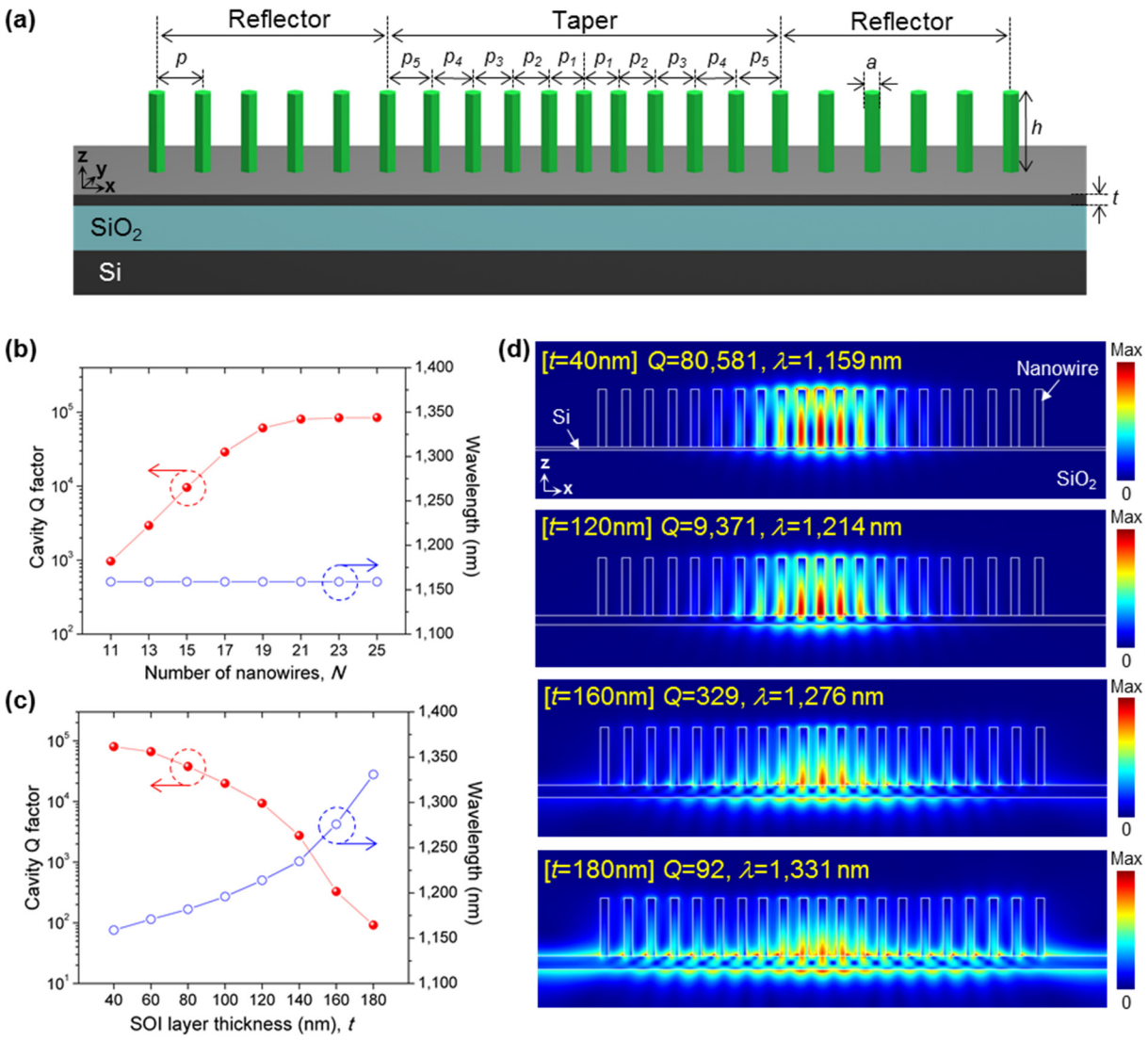

Figure 3.1 (a) Schematic of the nanowire array cavity. (b) Dependence of the number of total nanowires (N) on the cavity Q. (c) Dependence of the SOI layer thickness (t) on the cavity Q, and (d) electric field intensity profiles showing worse confinement at larger t.

the nanobeam cavities can be formed in various ways, such as modulating air-hole diameters, wrist widths, and periods[71-73]. Here we choose to form the artificial defect by modulating the period of the nanowires while keeping the dimension of all nanowires constituting the cavity equal. The period of nanowires in the taper section is modulated gradually to minimize the radiation loss[71],

and the offset of the graded taper is fixed to 10 nm ($p = p_1+50 = p_2+40 = p_3+30 = p_4+20 = p_5+10$) due to the resolution of the e-beam writing setup we used. The effect of the number of total nanowires (N) on the cavity Q is shown in Figure 3.1(b). 3D FDTD simulations (FDTD Solutions, Lumerical) are conducted to calculate Q factors. The cavity Q is 970 without reflector nanowire array ($N = 11$), which increases as the number of nanowires constituting the reflector increases. Because the cavity Q saturates around 80,000 for $N \geq 21$, we have chosen $N = 21$ for our design. The SOI layer thickness (t) of 40 nm, the nanowire diameter (a) of 140 nm, the nanowire height (h) of 800 nm, and the period (p) of 350 nm is used for the simulations.

The out-of-plane confinement along the y- and z-axis is another requisite to achieve high cavity Q. Although the nanowire/air interface along the y-axis satisfies the TIR condition due to high index contrasts, the confinement along the z-axis is degraded by the underlying silicon, because the refractive index of silicon is larger than the effective refractive index of the nanobeam cavity and the TIR condition is not satisfied. Therefore, adopting a thin SOI layer is advantageous since this could minimize the leakage through silicon. The effect of the SOI layer thickness (t) on the cavity Q is shown in Figure 3.1(c). The cavity Q rapidly decreases by increasing t, and the cavity Q becomes less than 1,000 when $t > 140$ nm. A confined mode is not observed anymore at $t > 180$ nm. As shown in the electric field profile in Figure 3.1(d), the overlap of the field with silicon increases and the resonant wavelength becomes longer as t gets thicker. It is also clearly shown in the electric field profile at $t = 160$ nm and $t = 180$ nm that the field is leaking out of the cavity through the SOI layer. In our design, a thin SOI layer of $t = 40$ nm is employed for the nanowire cavity. The proposed structure shows a calculated Q factor of ~81,000, a confinement factor of $\Gamma = 0.64$, and mode volume of $V_{eff} = 0.81\ (\lambda/n)^3$. It should be highlighted that the calculated Q factor is more than 2 orders of magnitude higher than previously reported single-

nanowire lasers, which rely on optical feedback from nanowire end and side facets[20, 74]. Such a high Q factor, high confinement factor, and small mode volume can lead to low lasing threshold[75] and fast direct modulation speeds[76].

3.2.2 Fabrication and lasing measurements

The sample preparation and nanowire growth conditions are described in detail in Chapter 2.2. TEGa, TBAs, TMIn, and TBP are used as precursors for InGaAs nanowire growth and InGaP passivation. Figure 3.2 shows the SEM image of a nanowire array cavity on a 40 nm-thick SOI substrate, where the gas phase composition of indium in InGaAs nanowires and InGaP shell is 29 % and 88 %, respectively. The lasing action is measured at room temperature by optically pumping the nanowire array using a supercontinuum laser (SuperK EXTREME EXW-12, NKT Photonics) with a wavelength of 660 nm, a pulse duration of 30 ps, and a repetition rate of 1.95 MHz. The pump source is applied from the direction normal to the SOI substrate, which is the same as the setup in Figure 2.22. Photoluminescence (PL) spectra in Figure 3.3(a) show that the cavity peak around 1,100 nm is much weaker than the broad spontaneous emission when the pump power is low. As the pump power is increased, the spontaneous emission broadens and blue-shifts due to

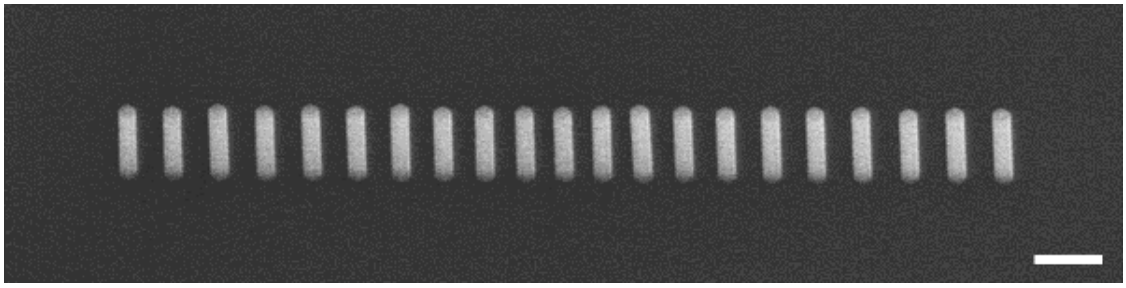

Figure 3.2 30˚-tilted SEM images of an InGaAs/InGaP core/shell nanowire array laser. Scale bar, 500 nm.

the band filling effect, and the cavity peak rapidly increases and finally dominates the spontaneous peak. The integrated intensities of these emission peaks are plotted as a function of input pump power (light-out versus light-in (L-L) curve) in Figure 3.3(b), to further investigate lasing characteristics. The cavity peak intensities show an S-shaped response in the logarithmic scale, whereas the spontaneous emission is clamped above the lasing threshold, which are clear indicators of lasing action. The threshold pump fluence is estimated to 16 μJ/cm^2. The emission patterns reveal an interference fringe pattern above the threshold (Figure 3.3(c)), indicating coherent radiation.

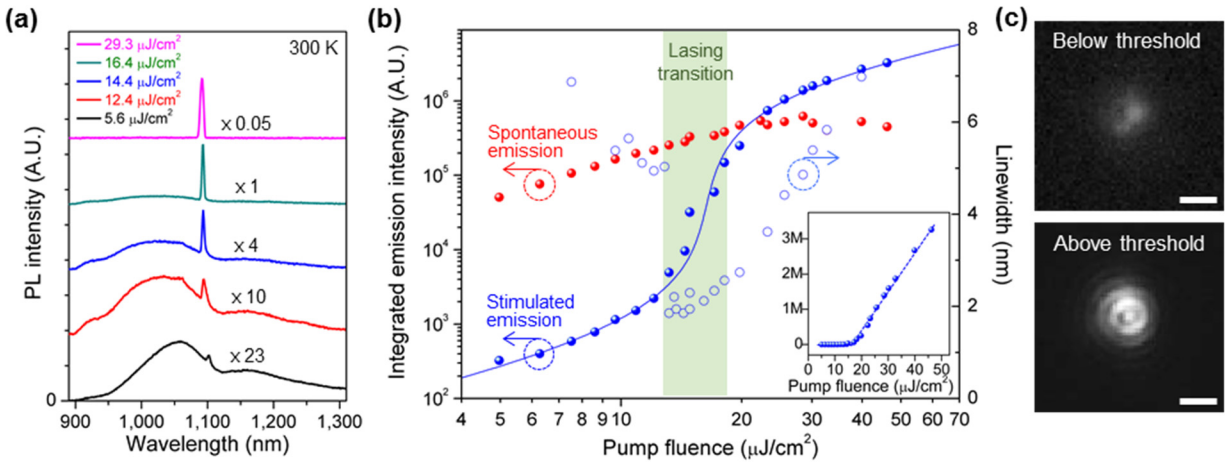

Figure 3.3 (a) Photoluminescence spectra of a nanowire array laser with increasing pump power, showing the transition from spontaneous emission to lasing. (b) integrated emission intensities of the stimulated emission (filled blue circle) and spontaneous emission (filled red circle), and cavity peak linewidth (open circle). Inset: light-light curve of the lasing peak shown in a linear scale. (c) Emission patterns measured by a commercial 2D focal plane array detector. Interference patterns are observed above the lasing threshold. Scale bars, 5 μm.

3.2.3 Rate equation analysis

The L-L curve is further analyzed by a rate equation model to estimate the spontaneous emission factor (β) and Q factor of the nanowire array laser on a thin SOI layer. We used modified rate equations based to investigate the lasing behavior under optical pumping conditions[20, 77]. Carrier density (N) in the active nanowires (11 nanowires in the tapered area) and photon density (S) in the cavity mode are described as follows:

$$\frac{dN}{dt} = \frac{\eta P}{\hbar\omega_p V} - AN - \frac{N}{\tau_{sp}} - CN^3 - v_g GS \quad (1)$$

$$\frac{dS}{dt} = \left[\Gamma v_g G - \frac{1}{\tau_p}\right] S + \Gamma\beta\frac{N}{\tau_{sp}} \quad (2)$$

where the material gain (G) is given by a logarithmic model, $G(N) = g_0 \ln\frac{(N+N_s)}{(N_{tr}+N_s)}$. P and V are the optical pump power and volume of the active nanowires, respectively. N_{tr}, N_s, and g_0 are obtained by fitting the peak gain calculated by modelling based on the measured photoluminescence spectrum as shown in Figure 3.4. All parameters used are listed in Table 3.1. We assume η = 0.01, which is the fraction of the pump light absorbed by the active nanowires, considering our optical characterization setup. Figure 3.5 shows the plot of L-L curves calculated from the rate equations. It should be noted that the Q factor is also a fitting parameter in this analysis, because calculating the Q factor from the cavity linewidth is difficult due to (1) the abrupt change of the linewidth around the transparency carrier density[20] and (2) the broadening of the linewidth under pulsed operation[62]. The best fitting values for β and Q factor are 0.0065 and 1,150, respectively. These β and Q factors are derived by pumping the center of the nanobeam photonic crystal cavity, with a pump spot size of 1.8 μm. This indicates that the pump area overlaps with approximately seven nanowires in the center. As shown in the electric field profile in Figure

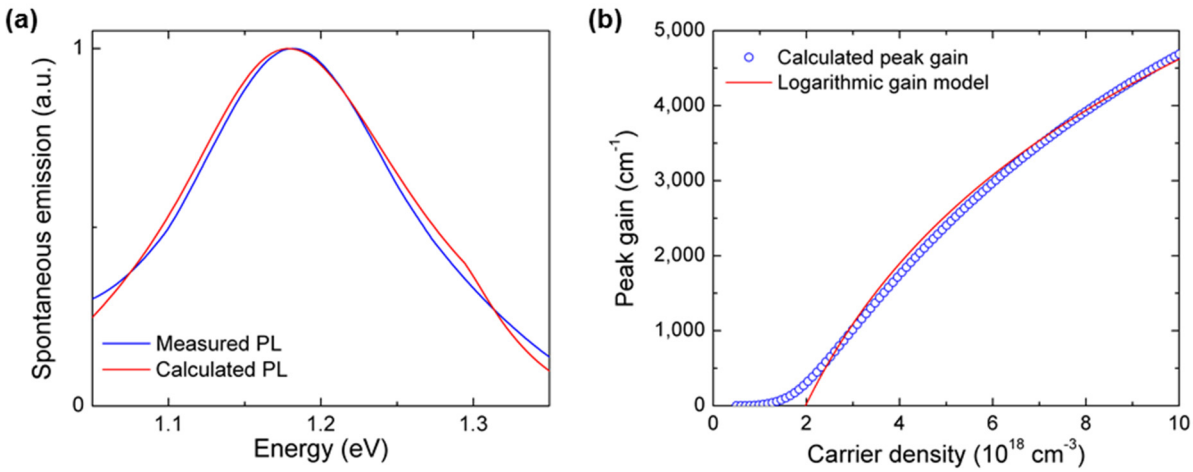

Figure 3.4 (a) The PL spectrum of nanowires and the calculated spectrum ($In_{0.2}GaAs$ with the relaxation energy of 0.15 eV) showing the fit. (b) Calculated peak gain and logarithmic material gain model as a function of carrier density.

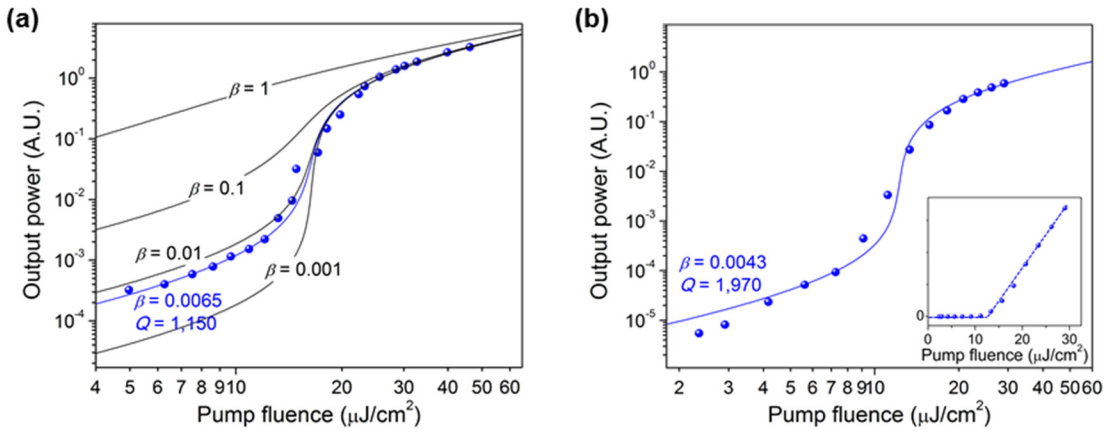

Figure 3.5 (a) Rate equation modellings for various spontaneous emission factors (β). The L-L curve calculated with β = 0.0065 and Q = 1,150 fits the best with experimental data. (b) Double-logarithmic L-L curve measured by homogeneously pumping entire nanowires. β = 0.0043 and Q = 1,970 fits the best with experimental data. Inset: Experimental L-L curve shown in a linear scale.

3.1(d), almost the entire field of the lasing mode is confined in these seven nanowires in the center when t = 40 nm. Therefore, the confinement factor Γ will be almost identical with the case of pumping the entire nanowires. On the other hand, the cavity Q factor will be affected by the pump area, because nanowires outside the pumping area are absorptive at the lasing wavelength which is beyond their bandgap energy. If nanowires in reflector sections are pumped together with nanowires in the center, the material loss of reflector sections will decrease by pumping, which will lead to an increase of the cavity Q factor and a decrease of lasing threshold. This speculation is verified by measuring the L-L curve by pumping the entire nanowire arrays. A cylindrical lens (f = 50 cm) is inserted into the pump beam path to form an elliptical pump beam shape on the sample. The beam spot size is measured to be 10.5 μm (major axis, x-direction) and 1.8 μm (minor axis, y-direction), which covers the entire array (6.7 × 0.14 μm^2).

Table 3.1: Parameters used in the rate equations

Fraction of the pump light absorbed by the active nanowires (η)	0.01
Nonradiative recombination coefficient (A)	1.43×10^{8} s^{-1}
Auger recombination (C)	3.5×10^{-30} cm^{6} s^{-1}
Spontaneous emission lifetime (τ_{sp})	4 ns
Group index (n_g)	4
Gain coefficient (g_0)	3250 cm^{-1}
Transparency current density (N_{tr})	1.98×10^{18}
Third linearity parameter (N_s)	5.71×10^{17}
Confinement factor (Γ)	0.637
Frequency of pump laser ($\omega_p=2\pi c/\lambda$)	2.854×10^{15}

Figure 3.5(b) shows the L-L curve measured by pumping the same nanowire array with a cylindrical lens but keeping other conditions identical. Rate equation fitting reveals that the Q factor is increased from 1,150 to 1,970, while β is decreased from 0.0065 to 0.0043. The threshold pump fluence is decreased from 16 μJ/cm^2 to 12 μJ/cm^2 by pumping the entire array (inset in Figure 3.5(b)), as the Q factor is increased. We attribute the decrease of β to a reduction of the portion of emitted photons coupled into the lasing mode, as the spontaneous emission from nanowires in reflector sections does not contribute to lasing.

The Q factors derived from rate equation fittings are 1,150 and 1,970 for different pumping conditions, which are more than an order of magnitude smaller than the Q factor derived from FDTD simulations. This is primarily stemming from the fabrication imperfections in nanowire cavities. When non-uniformity in the nanowire dimension is considered in simulations (standard deviation of 5 nm in nanowire diameters and 20 nm in nanowire heights), the Q factor is calculated to be 1,045, which is similar with the measured Q factors. This suggests that a more robust cavity design or improved growth conditions are required to realize high-Q bottom-up nanowire array cavities.

3.3 Two-dimensional photonic crystal lasers on SOI

3.3.1 Design

1D photonic crystal lasers demonstrated in the previous chapter employ an artificial defect in photonic crystals, and the cavity mode frequency is within the bandgap determined by reflectors. Here, 2D photonic crystal lasers without an artificial defect are shown, which operate at photonic band-edge.

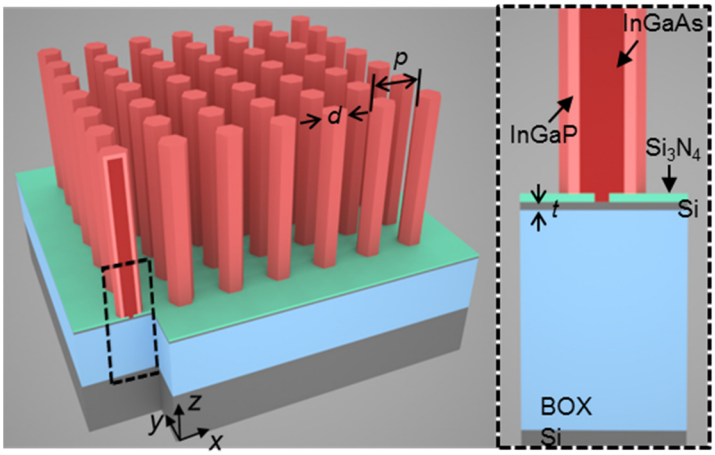

Figure 3.6 Schematic illustrations of the 7 × 7 nanopillar PhC laser with InGaAs/InGaP core-shell structures on an SOI substrate with an SOI layer thickness of *t*. *d* and *p* indicate the diameter and the pitch of nanopillars, respectively.

Figure 3.6 shows schematic illustrations of the nanowire 2D photonic crystal laser, which is comprised of a 7 × 7 nanowire array on an SOI substrate. InGaAs/InGaP core-shell structure is employed to reduce non-radiative surface recombination. The corresponding photonic band structure of the first TM mode in a three-dimensional nanowire array with 350 nm pitch, 130 nm diameter and 800 nm height is calculated using a finite-difference time-domain (FDTD) method, which is shown in Figure 3.7(a). We focused on the first TM mode near the band-edge (M-point, blue circle) below the light line. The electric field intensity profiles ($|E|^2$) of the first M-point band-edge mode are shown in Figure 3.7(b), clearly exhibiting tightly confined field in the 7 × 7 nanowire array. In simulations, the refractive indices of InGaAs/InGaP nanowires and Si are assumed to be 3.4 and 3.55, respectively. Cavity *Q* factors and resonant wavelengths are obtained as a function of an SOI layer thickness (*t*) using FDTD method, as shown in Figure 3.8(a). The *Q* factor increases as *t* is decreased from 100 nm to 40 nm, while the *Q* factor does not increase

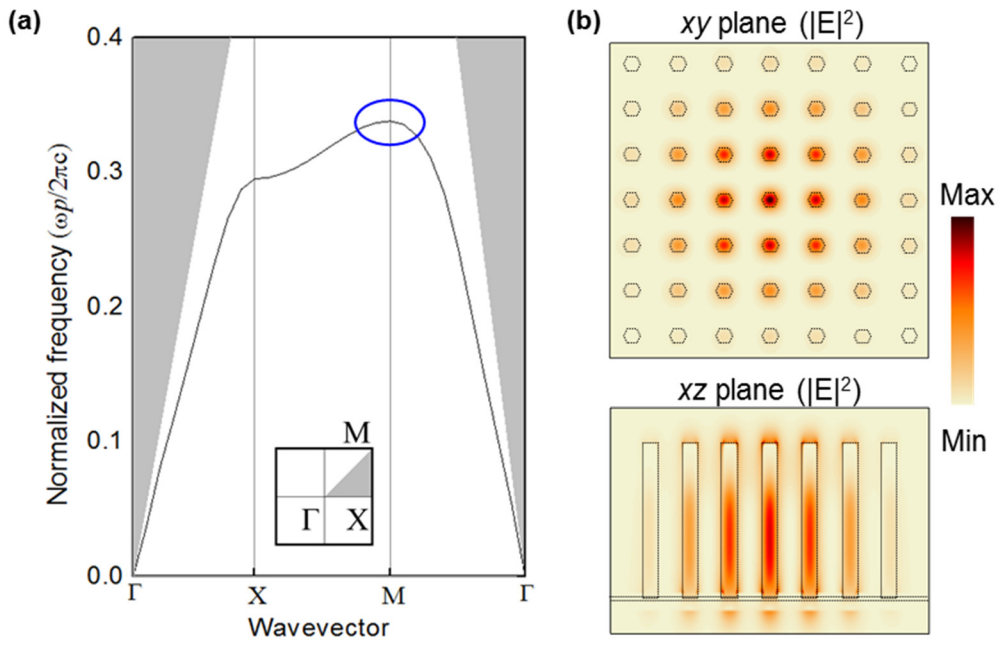

Figure 3.7 (a) TM mode photonic band structure of the square lattice nanopillar array. The grey area denotes the region above the light line in air. (b) $|E|^2$ field profiles of the first band-edge mode (blue circle in (a)) calculated by the FDTD method.

anymore when t becomes smaller than 40 nm. The effect of nanowire array size ($N \times N$) is also studied (Figure 3.8(b)), from which we can observe that the Q factor increases as the number of nanowires increases due to enhanced lateral confinement. We adopt 7 × 7 nanowire array on a 40-nm-thick SOI layer, which has an ultracompact cavity volume of 2,300 × 2,300 × 800 nm^3 and the Q factor of 2,042.

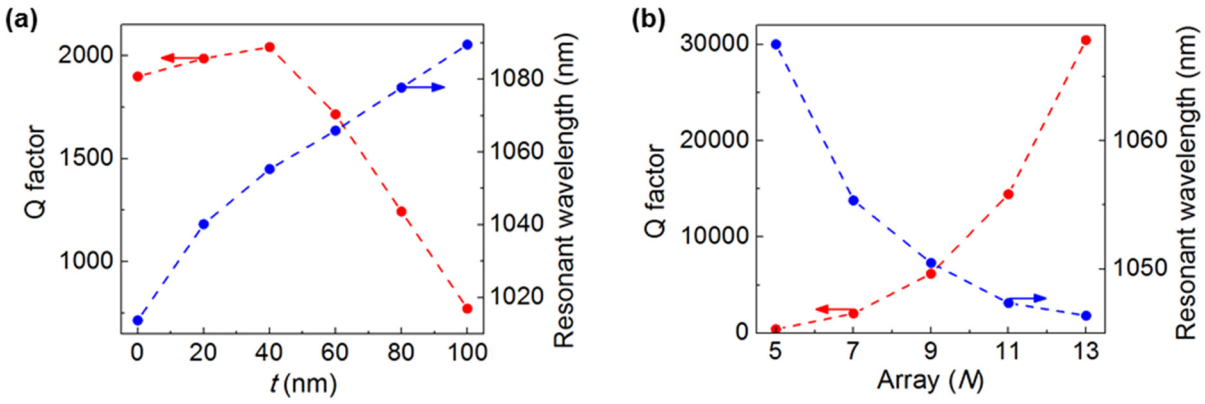

Figure 3.8 (a) Calculated Q factors and resonant wavelengths as a function of t in 7 × 7 nanopillar arrays and (b) a function of an array size at t = 40 nm.

3.3.2 Fabrication and characterization

The sample preparation and nanowire epitaxy conditions are identical with the conditions in Chapter 2.2.3. A 30° tilted and magnified SEM images of as-grown InGaAs/InGaP core-shell nanowire photonic crystals are displayed in Figure 3.9(a). The nanowire in the magnified SEM image exhibits a smooth surface morphology with a diameter (d) of 130 nm and a height of 800 nm. The top-view SEM image in Figure 3.9(b) shows that the nanowires with uniform diameters are vertically grown on the SOI layer.

The fabricated 2D photonic crystal cavities are characterized by optical pumping using a pulsed supercontinuum laser, with the setup introduced in Chapter 3.2. As shown in Figure 3.10(a), broad spontaneous emissions are seen at low pump powers, while the band-edge cavity mode becomes dominant at a wavelength of 1057 nm by increasing the pump power, where the cavity resonant wavelength agrees well with the theoretical calculation using the FDTD method. It is observed that the cavity mode intensity is more than one order of magnitude larger than the

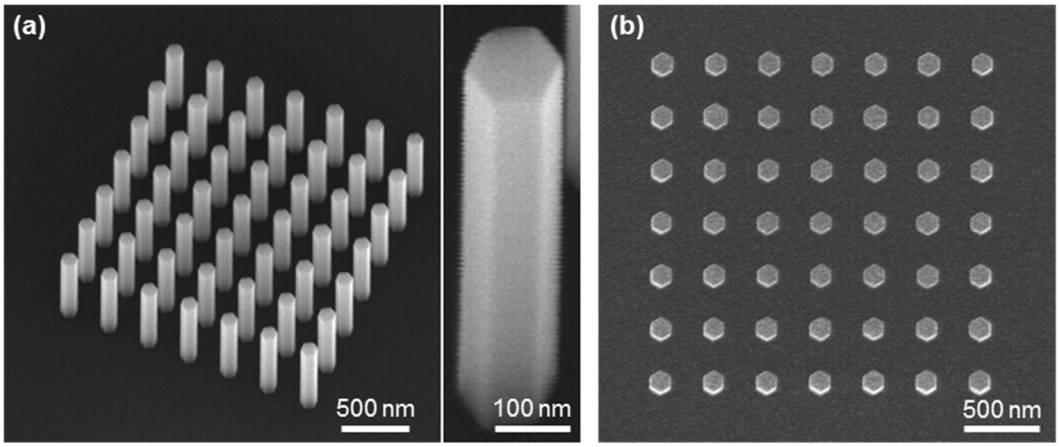

Figure 3.9 (a) 30° tilted and enlarged SEM images of as-grown InGaAs/InGaP core-shell nanowires with d = 130 nm, p = 350 nm, and a height of 800 nm. (b) Top-view SEM image showing uniformly grown nanopillar array.

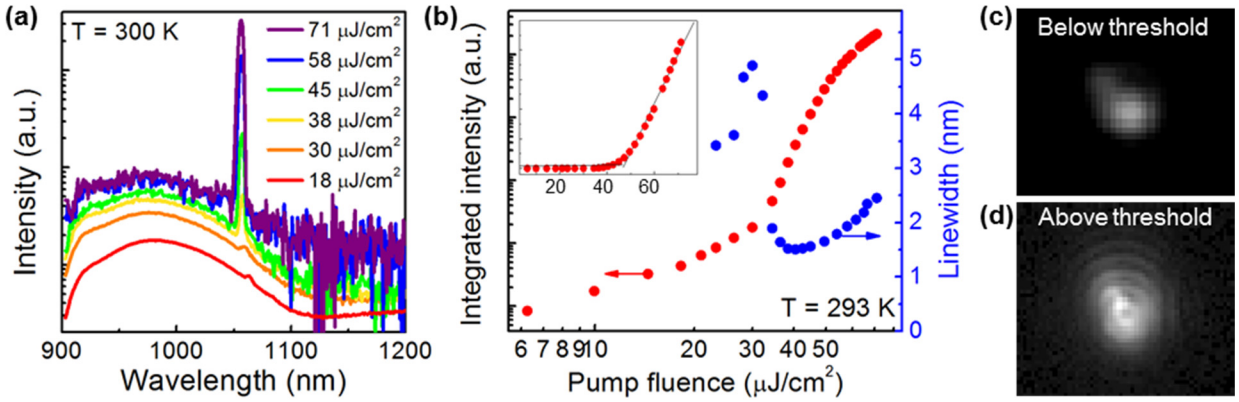

Figure 3.10 (a) Room-temperature emission spectra at various pump powers. The laser peak at a wavelength of 1057 nm steeply increases above threshold. (b) L–L curve of the nanowire array band-edge laser with a threshold of ~45 μJ/cm^2 (filled red circles) and corresponding spectral linewidth (filled blue circles). Integrated intensities are obtained by Gaussian fitting of the spectra. Inset: L–L curve on a linear scale. Optical images of the laser emission below threshold (c) and above threshold (d). Interference fringe patterns are captured above threshold.

spontaneous emission for the pump fluences above 58 μJ/cm^2. We note that single-mode lasing at room temperature is observed from both 1D and 2D photonic crystal cavities which are formed by bottom-up nanowires on 40 nm-thick SOI substrates. These features are crucial for optical sensing and communication applications. Figure 3.10(b) shows the integrated intensity of the cavity mode as a function of a pump power (L-L curve) on a log-log scale, plotted together with the spectral linewidth. The measured integrated intensities manifest lasing action such as an S-shaped behavior and a sudden decrease of the linewidth around the threshold. The lasing threshold is estimated to be ~45 μJ/cm^2 from these characteristics, which is also substantiated from the position of the kink between two linear regions in the inset of Figure 3.10(b). The optical images of the nanowire 2D photonic crystal lasers show that interference fringe patterns are observed above threshold (Figure 3.10(d)), while such interference fringes are not captured below threshold (Figure 3.10(c)). We obtained a donut-shaped lasing emission from the nanowire array laser, where the laser emission was azimuthally polarized, as shown in Figure 3.11.

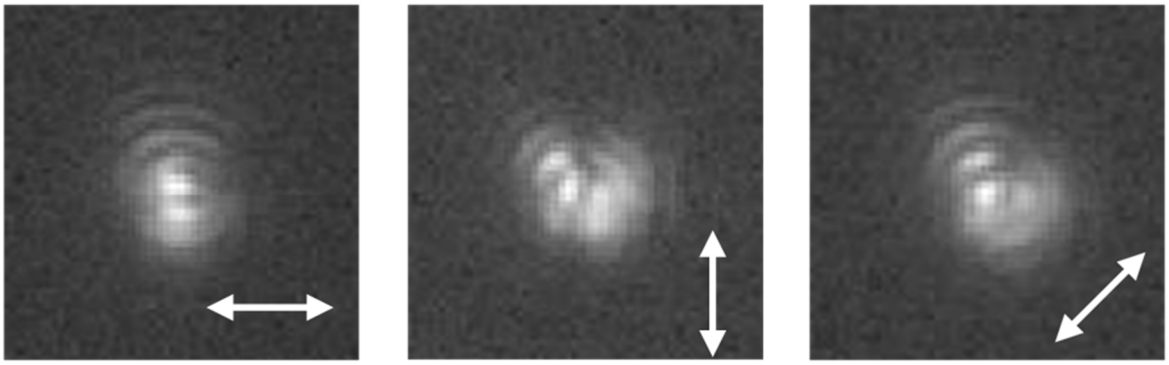

Figure 3.11 Measured angle-resolved lasing mode images as a function of the polarization angle. Left: horizontal polarization. Center: vertical polarization. Right: 45˚ tilted polarization. The lasing mode images clearly show the angle-dependence because the laser emission is azimuthally polarized.

It should be stressed that the nanowire photonic crystal lasers show diameter dependency in their lasing wavelengths, which suggests a potential application to nanowire photonic crystal sensors with direct real-time detection of molecules. As shown in Figure 3.12, the diameter variation of only 13 nm results in the lasing wavelength shift of 93 nm at the fixed pitch of 350 nm, revealing a strong dependence of lasing wavelengths on the nanowire diameter. By changing the pitch to 400 nm and increasing the indium composition in InGaAs nanowires, we also demonstrated the nanowire photonic crystal laser on a silicon platform operating at 1300 nm, which will be useful in silicon photonics as an on-chip laser. Additionally, the measured lasing wavelengths agree well with the calculated resonant wavelengths of the first M-point band-edge modes. It is worth mentioning that the diameter of nanowires can be lithographically controlled by changing the diameter of nanoholes. Since epitaxy conditions such as the growth temperature, V/III flow rate ratio and total flow rates also affect the aspect ratio (height/diameter) and the total

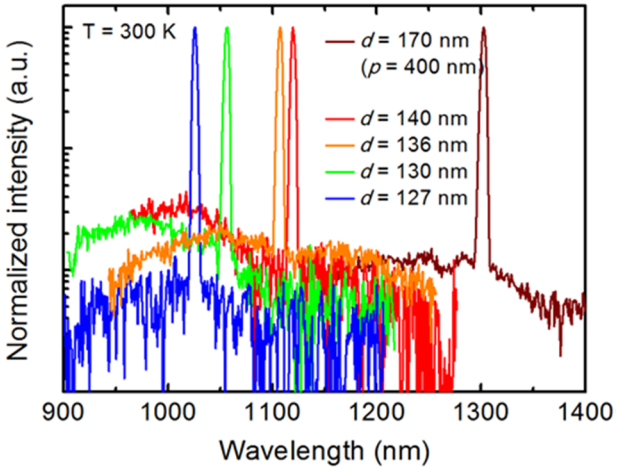

Figure 3.12 Diameter-dependent emission spectra of 2D photonic crystal lasers measured at room-temperature plotted in a log scale. Lasing up to a telecommunication wavelength of 1300 nm (d = 170 nm and p = 400 nm) is obtained.

volume of nanowires[28, 56], the diameter and height of nanowires can be individually controlled by combining these lithographic and epitaxial approaches. This suggests that the proposed bottom-up photonic crystal lasers exhibit a high degree of freedom in tuning the lasing wavelengths.

In summary, we have demonstrated ultracompact nanowire-based photonic crystal lasers operating at room temperature under optical pumping. Diameter dependence of the lasing characteristics indicates a new approach to integrated nanosensors on a silicon platform, which can potentially enable cost-effective lab-on-a-chip biosensing. In addition, as two-dimensional band-edge lasers are attractive and suitable for nonlinear optics, laser-based surgery, and military applications because of their high output power[78, 79], our demonstration provides an approach to scale down high-power lasers on the silicon platform.

4. Nanowire lasers on silicon photonic platforms

4.1 Overview

In the previous chapter, bottom-up photonic crystal lasers on SOI substrates are demonstrated by employing selective-area epitaxy of III-V nanowires. Room-temperature lasing is achieved from both 1D and 2D photonic crystal cavities, which provides a way toward ultracompact on-chip light sources.

However, it should be noted that these nanowire array lasers are grown on a thin SOI layer with a thickness of 40 nm, so that the leakage of optical fields through silicon can be minimized and high Q factor can be achieved. This plagues the compatibility of proposed nanolasers with photonic integrated circuits and silicon photonic platforms, since thicker SOI layers (220 nm) are employed in standard silicon photonic industries[3]. Also, the lasers need to be integrated with other components, such as waveguides, modulators, and detectors, for chip-scale optical communications and data transfer.

Another requirement is operating the laser at telecommunication wavelengths, such as 1,310 nm or 1,550 nm. To the best of our knowledge, there are no reports of monolithic nanowire lasers on silicon operating in the telecom-wavelength range. This may be attributed to difficulties in growing high-quality nanowires with proper bandgaps on silicon[50], as well as non-radiative Auger recombination which increases as the bandgap is decreased[61, 80]. Furthermore, the confinement factor and end-facet reflectivity decrease at longer wavelengths in sub-wavelength scale nanowire cavities, implying that the nanowire diameter and length must increase to support longer wavelength lasing[15]. Operation wavelengths of vertical free-standing nanowire lasers on

silicon have thus been limited to shorter wavelengths (<1,286 nm)[20, 74, 81], and nanowire lasers operating at 1,310 nm or above have been achieved only at cryogenic temperatures by heterogeneous integration methods, such as transferring nanowires onto external cavities[82] and dispersing microwires (wire diameter ~ 1 μm, wire length ~ 30 μm) on low-index substrates[83]. Controlling or selecting the lasing mode of nanowire lasers is another challenge, while this is a crucial requirement for practical applications.

In this chapter, we demonstrate room-temperature operation of nanowire array photonic crystal lasers which are directly integrated on standard-thickness (220 nm) SOI platforms. The nanowire lasers are integrated with SOI waveguides, where coupling of lasing emission to these waveguides is demonstrated and characterized. Finally, we show that the lasing wavelength of nanowire array lasers on SOI platforms can be lithographically tuned up to telecommunication wavelengths, which suggests that the proposed device could be a stepping stone for nanolasers compatible with silicon photonic platforms.

4.2 Waveguide-coupled nanowire lasers

4.2.1 Design

The optical confinement of 1D nanowire array photonic crystals on SOI substrates degrades if the SOI layer becomes thicker, which is shown in Figure 3.1(c) and (d). The same principle is applied in the case of 2D photonic crystals, as evidenced in Figure 3.8(a), and in both 1D and 2D photonic crystals, a confined mode is not observed when the SOI layer thickness is 220 nm. Since SOI wafers with a silicon layer thickness of 220 nm have become the standard for silicon photonic foundries around the world[3], the capability to integrate light sources on 220 nm-thick

SOI substrates with other passive and active components is thus crucial to ensure compatibility with silicon photonic platforms.

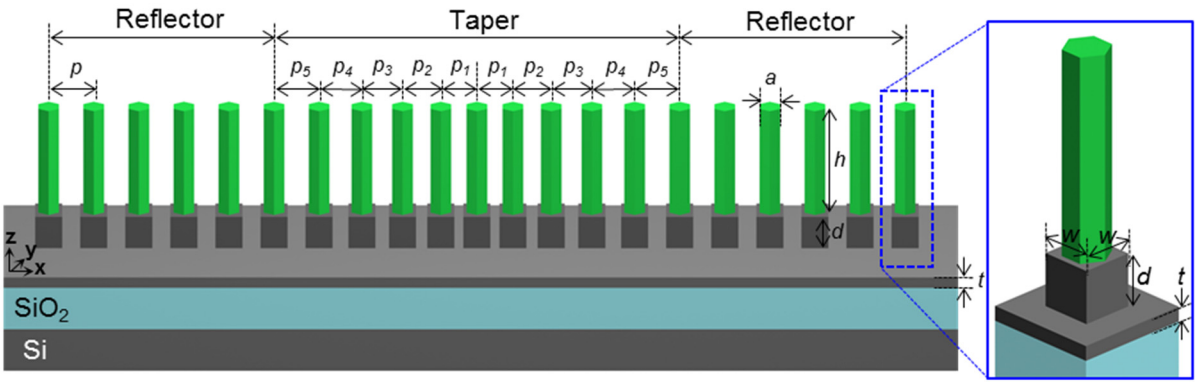

Figure 4.1 Schematic of the nanowire array cavity on SOI mesas.

We propose a new architecture to achieve high-Q nanowire cavities on 220 nm-thick SOI substrates, which is realized by integrating nanowires on SOI mesas. The schematic illustration of the structure is depicted in Figure 4.1. The key idea enabling high Q cavities on standard-thickness SOI is creating silicon trenches around the nanowires to minimize the loss through silicon, which could be realized by adopting the process introduced in Chapter 2.3. In this design, each nanowire is positioned on the center of rectangular mesas, where each mesa with a width of w is pre-patterned by e-beam lithography and dry etched before nanowire epitaxy. This architecture is analogous to the nanobeam design on thin SOI, if we regard the mesa as a part of the nanobeam cavity providing the in-plane optical feedback. We can infer from the simulation results in Chapter 3.2 that the cavity Q will be enhanced by decreasing the thickness of the etched SOI layer (t). Given that the SOI layer thickness is fixed to 220 nm for the compatibility with silicon photonics platforms, increasing the depth of the etched trench d (which is the height of mesas) will increase the Q factor since t is decreased in this case. This speculation is verified by FDTD simulations, as

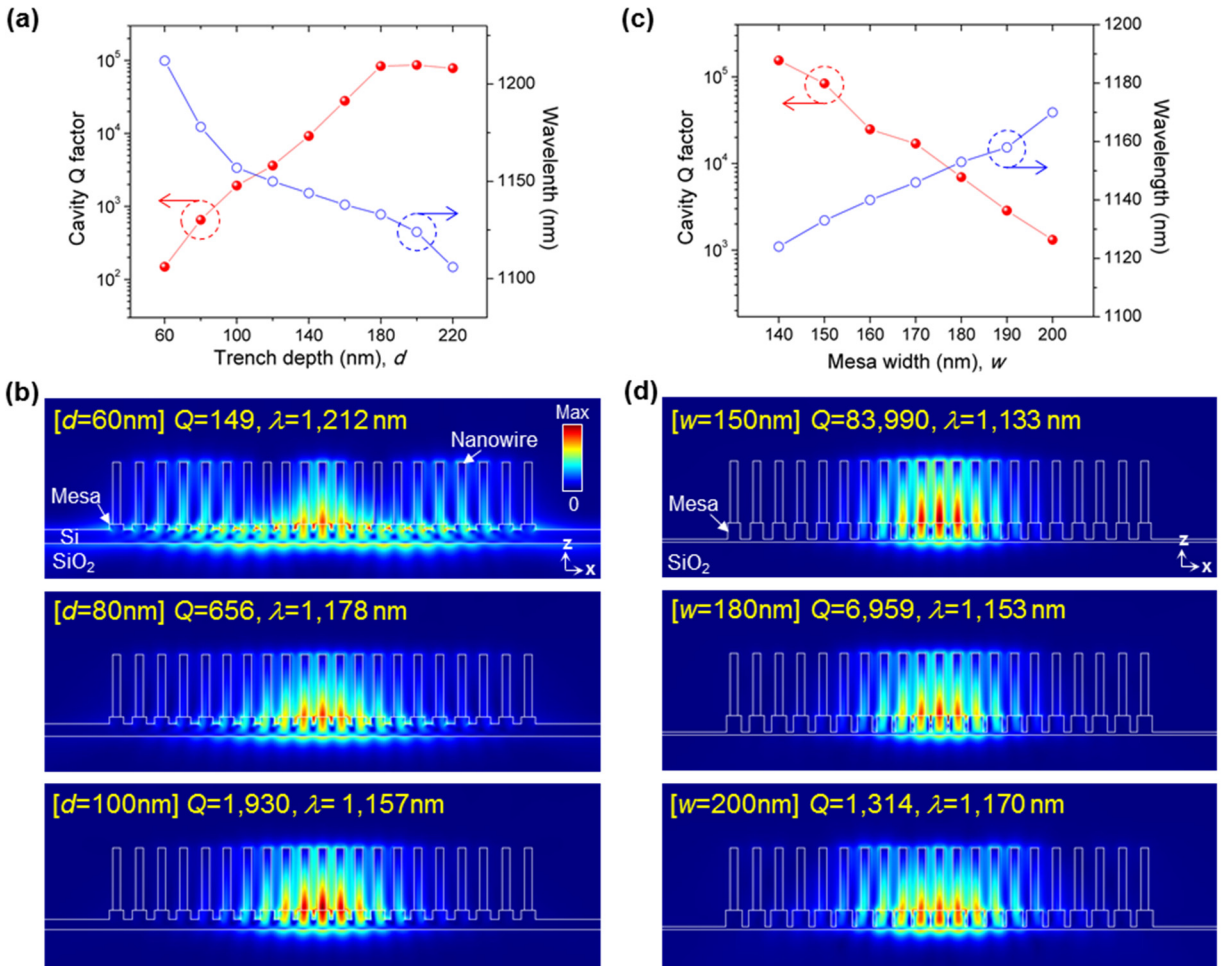

Figure 4.2 (a) Dependence of the trench depth (*d*) on the cavity Q, and (b)electric field intensity profiles showing worse confinement at smaller *d*. (c) Dependence of the mesa width (*w*) on the cavity *Q*, and (d) related electric field intensity profiles.

shown in Figure 4.2(a). Confined modes are observed when $d \geq 60$ nm, and the cavity *Q* increases by making the trench deeper. The parameters $a = 140$ nm, $h = 800$ nm, $p = 300$ nm, and $w = 150$ nm are chosen for the simulation. As shown in the electric field profiles in Figure 4.2(b), the field leaks through the silicon when *d* is small (*t* is large), which is very similar with the case of the nanowire array cavity on thick SOI planes (Figure 3.1(d)). Similarly, the overlap of the field with silicon increases by enlarging the size of mesas, which degrades the cavity *Q* (Figure 4.2(c) and

4.2(d)). It should also be noted that changing the mesa width (w) shifts the cavity peak wavelength, as shown in Figure 4.2(d), in addition to the nanowire diameter (a) and pitch (p). This provides an additional degree of freedom and flexibility in controlling the lasing wavelengths, and suggests the possibility of the proposed platform for wavelength division multiplexing (WDM).

We adopt w = 150 nm for our devices, because the width of mesas needs to be larger than the diameter of nanowires for epitaxy. The mesa height of d = 180 nm (t = 40 nm) is employed, so that the mesas can be patterned simultaneously with SOI rib waveguides without any additional process. The proposed nanowire cavity on SOI mesas exhibits a cavity Q ~ 83,000 and confinement factor Γ ~ 0.51 at the peak wavelength of 1,133 nm.

4.2.2 Fabrication and material characterization

The nanowires are directly integrated on pre-patterned SOI by employing the fabrication and growth processes demonstrated in Chapter 2.3. Nanoholes are patterned on the center of SOI mesas, as shown in Figure 4.3(a), using thes processes. Nanowire growth is initiated by GaAs seeding on exposed silicon (Figure 4.3(b)), which is followed by InGaAs nanowire growth and InGaP passivation using TEGa, TMIn, TBAs, and TBP precursors. Detailed growth conditions can be found in Chapter 2.3. SOI waveguides are patterned along with mesas during the fabrication steps, so that the nanowire array lasers can be coupled with the waveguides, which is a crucial requirement for on-chip optical communications. Figure 4.4(a) shows a schematic of the nanowire array laser attached to an SOI rib waveguide with the width of 440 nm and the slab height of 40 nm. As shown in the SEM images in Figure 4.4(b), the fabricated nanowire array is attached to an SOI waveguide, and an output grating coupler is attached at the end of the waveguide to verify the coupling of nanowire array lasers by measuring the light emission from the couplers.

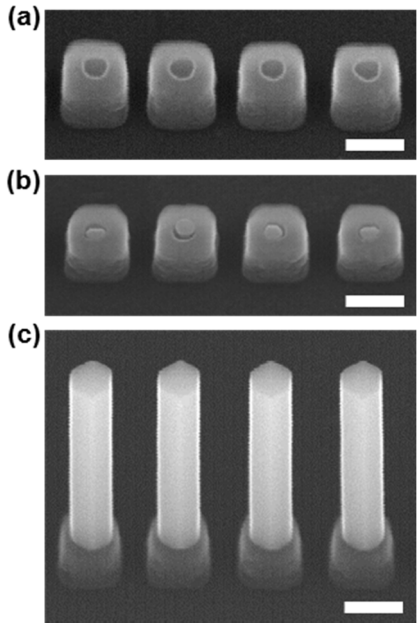

Figure 4.3 (a) SOI mesas with nanoholes. (b) GaAs seeding in nanoholes, followed by (c) InGaAs nanowire growth. Scale bar, 500 nm.

The material properties of as-grown nanowires are assessed by transmission electron microscopy (TEM), energy dispersive x-ray spectroscopy (EDX), and photoluminescence measurements. The nanowires on SOI mesas are sliced by focused ion beam (FIB) etching for characterization, wherein Platinum is used as a glue for the sample preparation. The nanowires on SOI mesas are free of threading dislocations as shown in the cross-sectional TEM image in Figure 4.5(a), although a high density of stacking defects is observed. The stacking disorders are commonly observed from InGaAs nanowires grown by selective-area epitaxy technique[47]. Next, line-scan measurements of EDX along the axial and radial direction are conducted to characterize the material content and compositional uniformity of core/shell nanowires. The spatial resolution of EDX measurement is estimated to be 18 nm, and accelerating voltage of 300 kV is used.

The line-scan data along the radial direction in Figure 4.5(b) show that only In counts

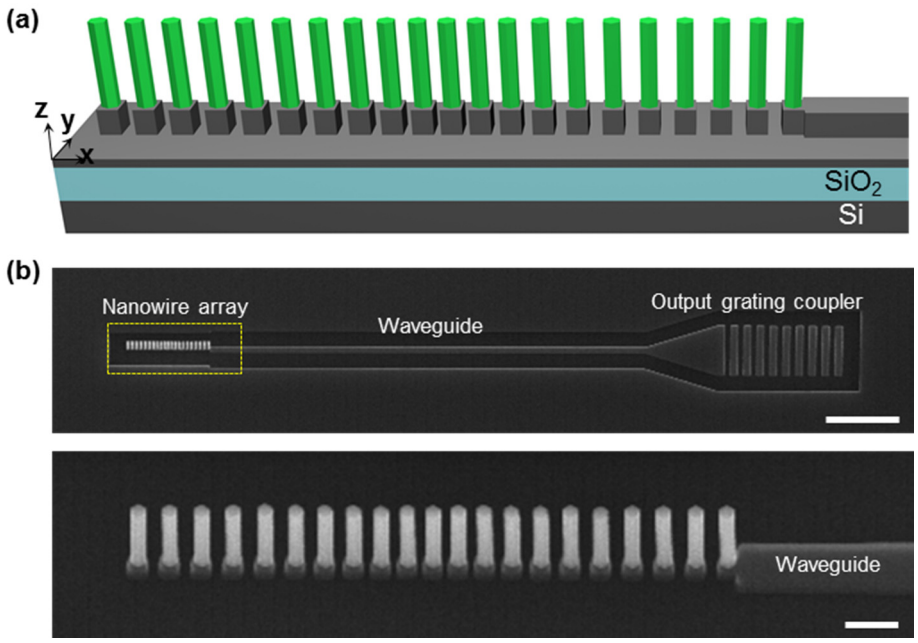

Figure 4.4 (a) Schematic of a nanowire array laser attached to a waveguide. (b) 30˚-tilted SEM images of a nanowire array cavity integrated with a waveguide and an output coupler (upper), and a close-up image of the nanowire array in the dashed box (lower). Scale bars, 5 mm (upper) and 500 nm (lower).

increases while Ga and As counts decrease around the edge of the nanowire. Corresponding In and As compositions in Figure 4.5(c) show that an InGaP shell with approximately 75 % In composition is grown around the InGaAs core with approximately 20 % In composition. Transition of the group-V material from arsenic to phosphorous in the shell is deduced from As composition because the energy of x-ray photons from phosphorous overlaps with the energy from platinum, which makes the P counts unreliable. The $In_{0.75}GaP$ shell is closely lattice-matched with the $In_{0.2}GaAs$ core (mismatch ~ 0.5 %). The axial line-scan data across the entire nanowire (Figure 4.5(d)) also confirms that the indium composition of InGaAs core is around 20 % except around the interface with the substrate. A close-up line-scan measurement around the interface is conducted to further investigate the composition of the nanowires, as shown in Figure 4.5(e). A

gradual increase of indium composition above the GaAs seeding is observed around the bottom 80 nm part of the nanowire, which is attributed to the In segregation during the growth[28]. The fluctuation and segregation of indium portion in nanowires will lead to a broadening of gain spectra, and this will increase the threshold pump power.

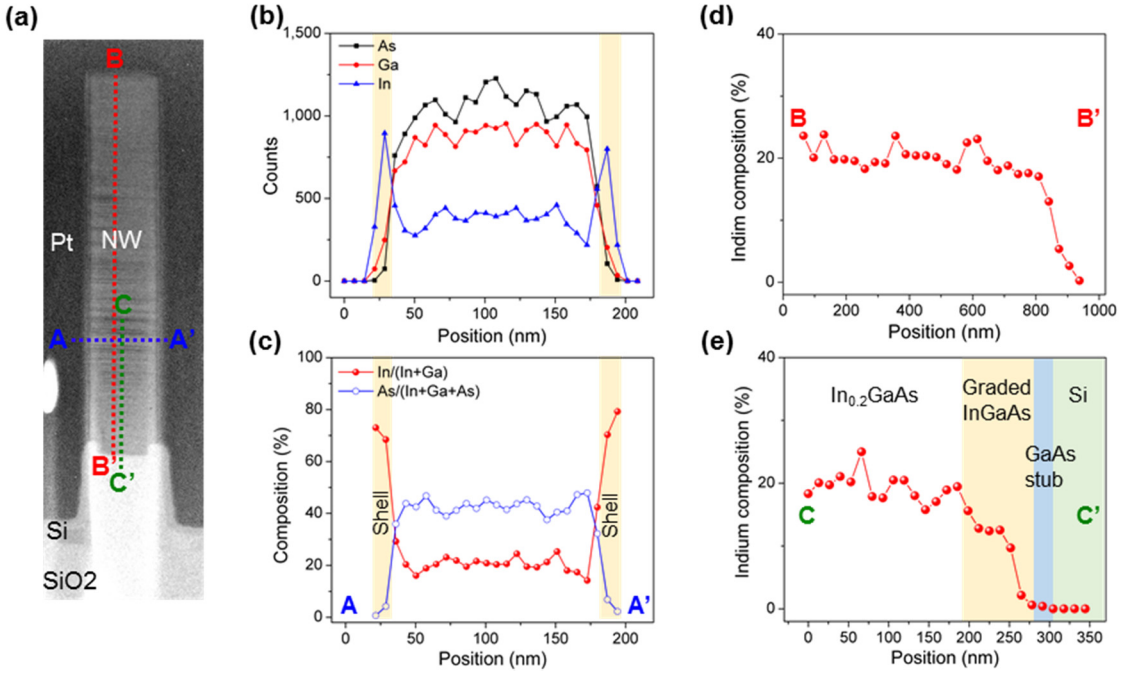

Figure 4.5 (a) TEM image of the nanowire cross-section. (b) Photon counts along the radial direction (A-A'), and (c) In and As compositions calculated from the photon counts. (d) In/(In+Ga) composition along the axial direction (B-B') and (e) (C-C').

The effect of *in-situ* passivated InGaP shells is also confirmed from PL and time-resolved PL (TRPL) measurements. First, the PL from InGaAs/InGaP core/shell nanowires are compared with InGaAs nanowires without the shell. The InGaAs nanowire sample is grown under the same growth condition, only excluding the shell growth step. Both samples are pumped by a continuous 632 nm He-Ne laser with a pump power of 30 μW. A 50× objective lens is used to pump nanowires

and collect the emission, and a large array (50 × 50 μm) of nanowires with 500 nm pitch is measured to exclude the influence of beam alignment on the PL intensity. As shown in Figure 4.6(a), the PL intensity from InGaAs/InGaP core/shell nanowires is around sixfold larger compared with nanowires without passivation.

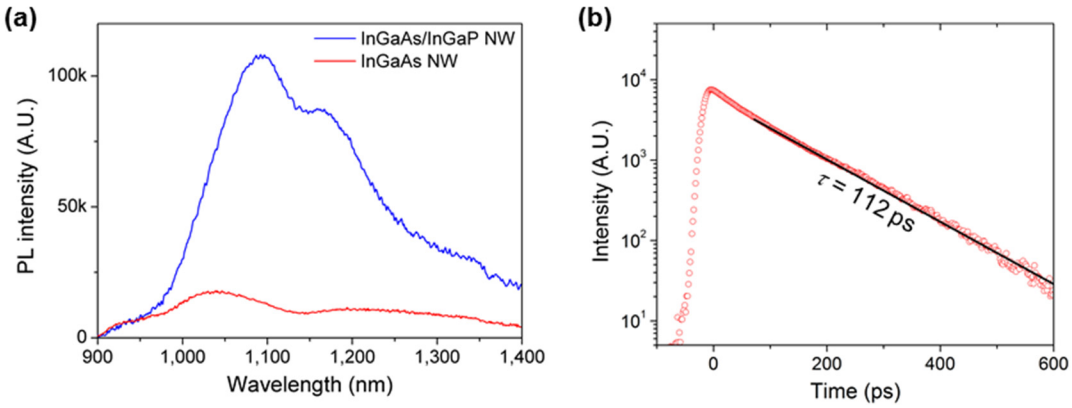

Figure 4.6 (a) PL spectra of InGaAs nanowires with and without InGaP surface passivation measured at room temperature. (b) Time-resolved photoluminescence measurement of InGaAs/InGaP core/shell nanowires.

TRPL measurements are conducted at room temperature by pumping nanowires using a Ti-Sapphire laser with a wavelength of 790 nm, pulse duration of 300 fs, and repetition rate of 75.6 MHz as an excitation source. The emission from nanowires are measured using a streak camera (Hamamatsu C5680) with a resolution of 3 ps. The room-temperature minority carrier lifetime of InGaAs/InGaP core/shell nanowires is estimated to be 112 ps (Figure 4.6(b)), while that of InGaAs nanowires without shell is measured to be 20 ps. Although emission intensities and minority carrier lifetimes are significantly increased (both by a factor of more than five) by surface passivation, the measured lifetime is still as low as 112 ps. It has been demonstrated that InGaAs nanowires grown on GaAs substrates can exhibit room-temperature lifetime of up to 1 ns by in-

situ surface passivation[84], which implies that the quality of surface passivation can be further improved by optimizing growth conditions.

4.2.3 Characterization of lasing and waveguide coupling

Lasing from the nanowire array in Figure 4.4(b) is characterized by optically pumping the array with a supercontinuum laser operating at 660 nm. The pumping scheme is identical with the setup introduced in Chapter 3. The PL spectra measured from the cavity show multiple cavity peaks below lasing threshold, whereas the fundamental mode at the shortest wavelength reaches lasing and dominates other peaks above threshold (Figure 4.7(a)). The lasing peak is slightly blue-shifted above lasing threshold due to the refractive index change caused by band filling[85]. Other peaks originate from low-Q modes, with the electric field exhibiting multiple antinodes along the x-axis and penetrating into the periodic nanowire reflectors on both sides of the defect area (Figure 4.7(b)). The threshold pump fluence is estimated to be $\sim$100 $\mu J/cm^2$ from the sharp kink observed from the linear L-L curve in Figure 4.7(a), which is higher than the laser grown on 40 nm-thick planar SOI substrates. We attribute this to lower Γ and degraded Q factor because the Q factor of cavities on mesas is influenced by mesas fabrication and alignment imperfections, in addition to the degradation from the non-uniformity of nanowire geometries that the cavities on both planar SOI and pre-patterned SOI experience.

Direct coupling of nanowire array lasers with SOI waveguides is confirmed by measuring the light emission from output grating couplers, which substantiates the compatibility of proposed lasers with silicon photonic platforms. Interference fringe patterns are observed above lasing threshold from both the nanowire array cavity and the output grating coupler (Figure 4.8(a)), indicating that coherent light is coupled and transmitted through the waveguide. It is interesting to

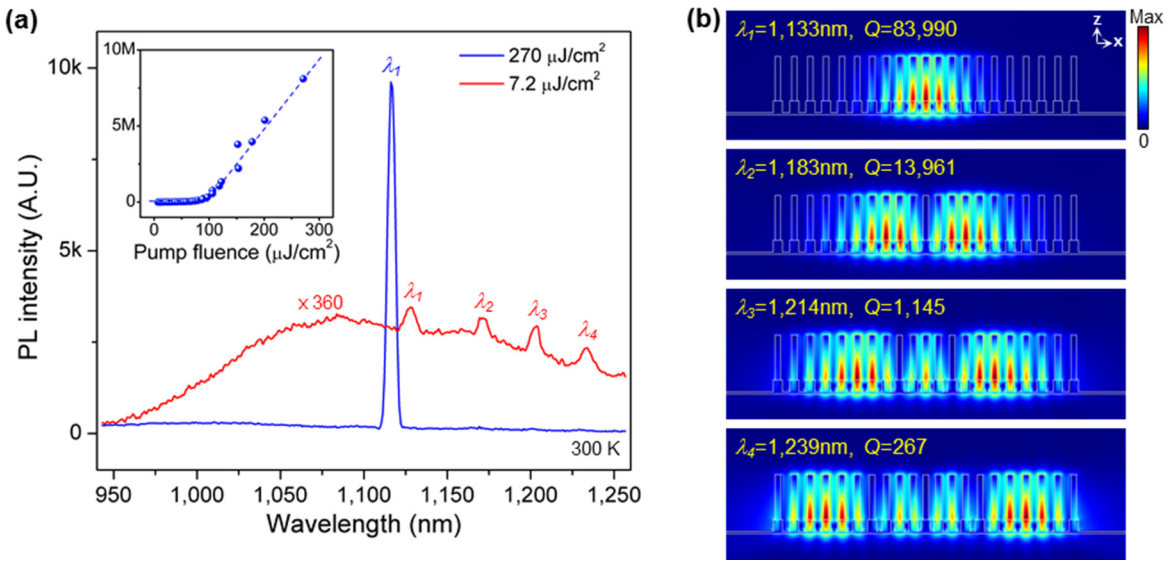

Figure 4.7 (a) Photoluminescence spectra of the laser below (red) and above (blue) the threshold. Inset: light-light curve of the lasing peak in a linear scale, indicating the lasing threshold around 100 μJ/cm^2. (b) Electric field profiles (|E|) of observed cavity modes.

note that all cavity modes are efficiently coupled with the waveguide as shown in Figure 4.8(b), while the coupling of spontaneous emission is negligible. Such coupling characteristics and efficiencies are further studied by FDTD simulations including SOI waveguides in the simulation structure. The electric field profiles from FDTD simulations show that the field of the fundamental mode (λ_1) is strongly confined in the center of the cavity with the coupling efficiency (η_{couple}) of 4.2 % (Figure 4.9(a)). The Q factor of the fundamental mode (~81,000) is slightly decreased due to the additional loss through the waveguide, compared with the Q factor of the cavity simulated without the waveguide (~83,000). The simulated electric field profiles of the second, third and fourth modes exhibit two, three and four antinodes in the cavity, and the peak wavelengths from these modes closely match with the measured data. As the in-plane confinement is weaker in the higher modes, the field couples more efficiently with the waveguides, leading to much higher

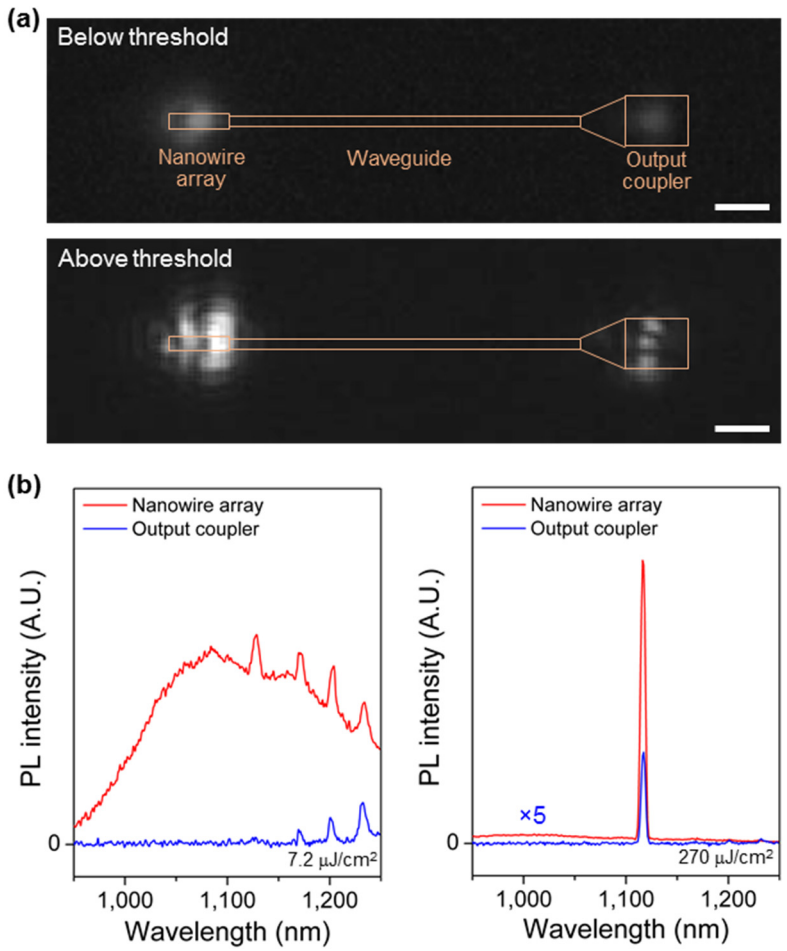

Figure 4.8 (a) Emission patterns of a nanowire array laser coupled with an SOI waveguide, exhibiting interference patterns above the lasing threshold. Scale bars, 5 μm. (b) Photoluminescence spectra measured on top of a nanowire array (red line) and on top of an output coupler (blue line) below the lasing threshold (left) and above the lasing threshold (right), indicating that the cavity peaks are effectively coupled to the waveguide.

coupling efficiency than the fundamental mode. This agrees well with the PL spectra measured from the output coupler in Figure 4.8(b). Pump position-dependent PL measurements are also conducted to further verify that the four cavity peaks observed from the PL originate from the modes described in Figure 4.9(a). As shown in Figure 4.9(b), the pump positions are shifted from

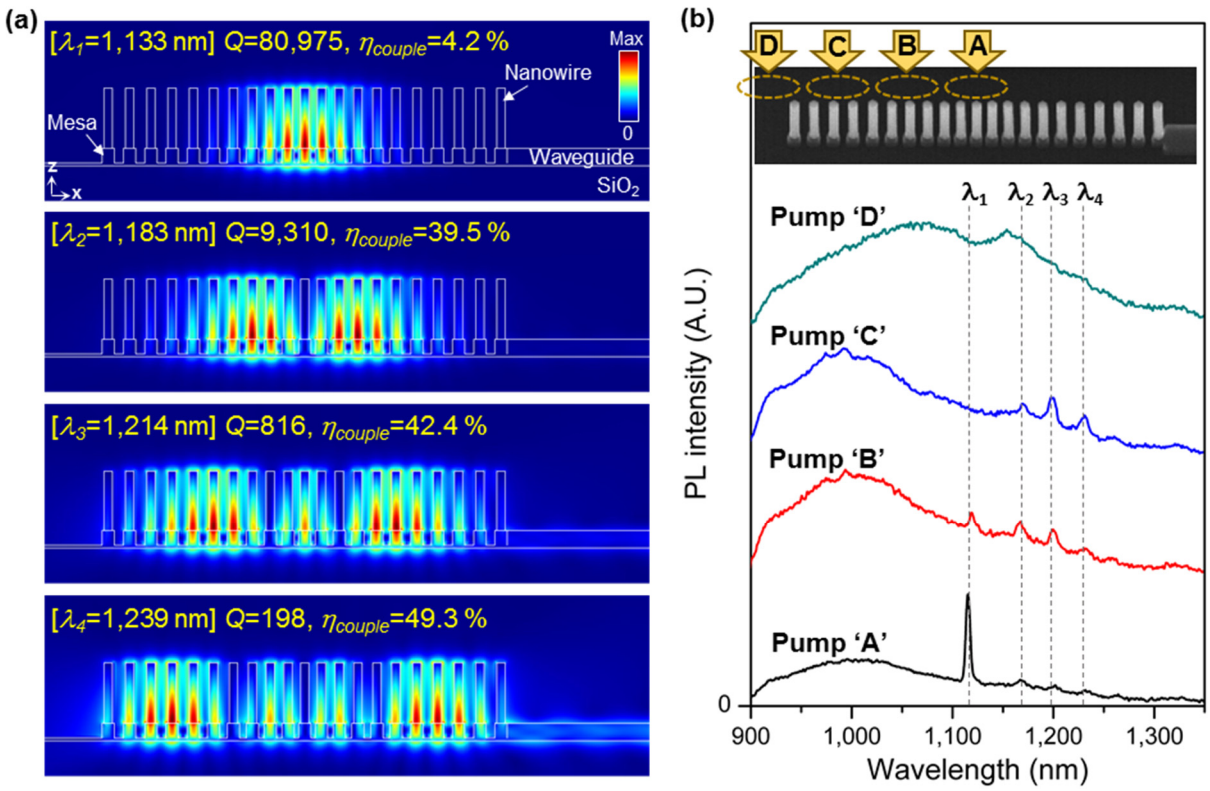

Figure 4.9 (a) Coupled mode profiles of fundamental cavity mode and higher modes. (b) PL spectra measured at different pump positions and fixed pump fluence (88 μJ/cm^2), showing changes in relative intensities between the cavity peaks.

the center (A) to the edge (D) of the cavity, maintaining the pump fluence of 88 μJ/cm^2 with an approximate pump spot size of 1.8 μm. The relative intensity of the peaks from the second and third modes are increased when the pump position is moved from 'A' to 'B', and so do the third and fourth modes when the pump position is moved from 'C' to 'D'. This is owing to the increase of the overlap between the pump area and the high-field region, which can be interpreted as the increase of the confinement factor of respective modes. Cavity peaks are not observed at the pump position 'D', because the emitted light from the nanowire at the edge is not confined but radiates freely into air. These results prove that the lasing operation occurs from the fundamental cavity

mode with a single antinode in the center, while the other peaks are stemming from low-Q modes with multiple antinodes.

The fundamental mode exhibits a waveguide coupling efficiency of only 4.2 %, and improving the coupling efficiency will lead to higher energy efficiency for optical communications. This can be accomplished by engineering the cavity design, for example by forming asymmetric reflectors on each side of the nanobeam cavity. If the number of nanowires constituting one side of the reflector is smaller than the other side, the shorter reflector section becomes more lossy and larger portion of the field leaks through the shorter section than the other side. Thus, the coupling efficiency can be increased by removing some of the nanowires constituting the reflector between the taper and the waveguide, while the cavity Q will decrease due to the larger loss. Figure 4.10(a) shows the effect of an asymmetric cavity on the coupling efficiency and cavity Q. The Q factor is the highest and the coupling efficiency is the lowest (4.2

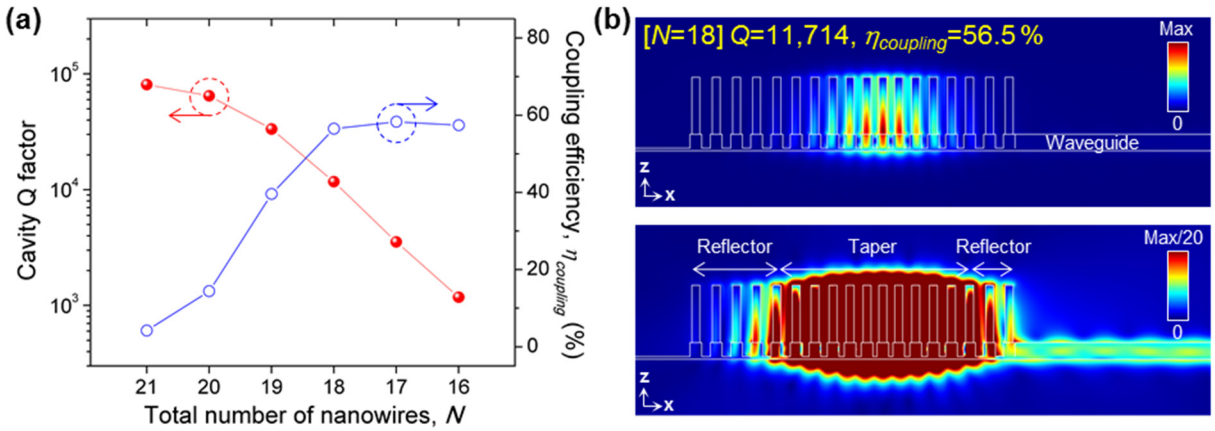

Figure 4.10 (a) Dependence of the number of nanowires constituting the cavity (N) on the coupling efficiency and cavity Q. (b) Electric field intensity profiles of waveguide-coupled cavity mode when N=18 (upper), and the same field profiles rescaled to show that the energy is dominantly dissipated through the waveguide (lower).

%) in the original cavity design with 21 nanowires ($N = 21$). The coupling efficiency increases to > 50 % by sacrificing the cavity Q when the number of nanowires constituting the reflector is decreased. Nanowire-based lasers with both high coupling efficiency and reasonably high Q factor can be achieved from the asymmetric cavity design (i.e. $\eta_{couple} = 56.5\%$ and $Q \sim 12{,}000$ at $N = 18$), as shown in Figure 4.10(b). This is in stark contrast to previously reported single nanowire-type lasers employing Fabry−Perot or helical cavity modes, which are difficult to achieve high Q factor and efficient waveguide coupling at the same time[86, 87].

In summary, we have demonstrated InGaAs/InGaP core/shell nanowire array lasers on a 220 nm-thick SOI platform operating at room temperature. The nanowire lasers are efficiently coupled with conventional SOI waveguides, which represent a new platform for ultracompact and energy-efficient optical links and unambiguously point the way toward practical and functional nanowire lasers.

4.3 Telecom-wavelength nanowire lasers

4.3.1 Design

In the previous chapter, nanowire array lasers on a standard-thickness SOI platform are demonstrated, which operate at room temperature and are coupled to waveguides. These results show possibilities for the proposed lasers to work as functional nanolasers on silicon. For silicon photonic integrated circuits and on-chip communication applications, however, the nanolasers need to operate in telecommunication wavelengths, such as 1,310 nm or 1,550 nm.

The waveguide-coupled nanobeam lasers, which is introduced in Chapter 4.2, operate at 1,100 nm (Figure 4.7(a)). In this chapter, we demonstrate telecom-wavelength nanowire lasers on

a silicon-on-insulator (SOI) platform operating in a single mode at room temperature. Since nanowire arrays form photonic crystal cavities, the cavity mode wavelength can be shifted by modifying the design of photonic crystals. Also, the gain spectra of InGaAs nanowires can be tuned by changing the material composition of InGaAs. Therefore, the lasing wavelengths can be shifted to longer wavelengths by changing the cavity design and increasing the indium composition in nanowires.

The schematic in Figure 4.11 shows the design of a 1D nanowire photonic crystal cavity with the cavity mode wavelength at 1,310 nm, which is a technologically important wavelength. The structure is similar with the nanobeam design on a 220 nm-thick SOI layer with trenches, which is demonstrated in Chapter 4.2. The diameter (d), height (h), and period (p) of nanowires are set to d = 180 nm, h = 700 nm, and p = 350 nm and the trench depth (t) is set to t = 180 nm in 3D FDTD simulations, which supports a fundamental cavity mode at 1,310 nm when the refractive index of InGaAs is assumed to be 3.62 without optical loss[88]. As shown in Figure 4.12, the cavity Q factor is low (Q ~ 1,080) if the 11 nanowires in the tapered section are not surrounded by

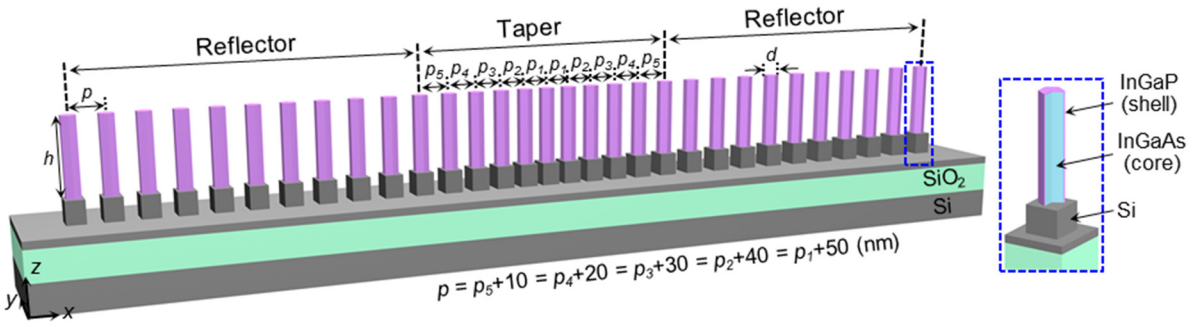

Figure 4.11 Schematic illustration of a nanowire array cavity with a fundamental cavity mode wavelength at 1,310 nm. The dimensions are p = 350 nm, d = 180 nm, and h = 700 nm.

periodic nanowires. The Q factor abruptly increases as the number of nanowires in reflector sections (N) is increased, reaching $Q > 10^5$ when $N \geq 12$.

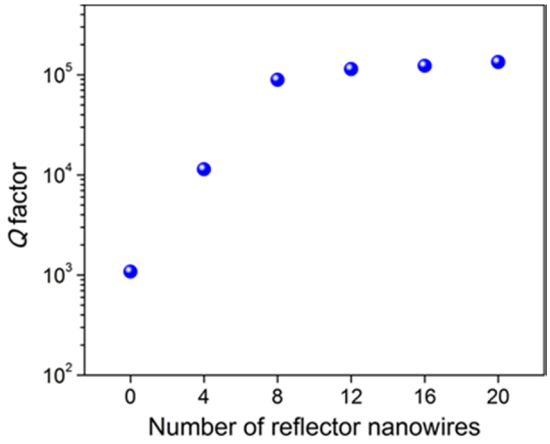

Figure 4.12 Cavity Q factor as a function of the number of nanowires constituting reflector sections when the trench depth is 180 nm.

Here, we have chosen a nanowire array nanobeam design with a total of 31 nanowires (11 nanowires in the tapered section, 10 periodic nanowires on each side of the tapered section) on a 220 nm-thick SOI substrate. The total number of nanowires is increased from 21 nanowires, which was the case of waveguide-coupled in Chapter 4.2, to 31 nanowires for high cavity Q factor. It should be noted that increased number of reflector nanowires will decrease the waveguide coupling efficiency, and thus the tradeoff between the Q factor and the coupling efficiency needs to be considered when designing waveguide-coupled nanowire array lasers.

Figure 4.13 shows electric field profiles (E_z) of the fundamental TM-mode at 1,310 nm. The field is tightly confined in the nanowires in the tapered section, corresponding to a confinement factor of $\Gamma = 0.548$ and cavity Q factor of 134,000, where such a high confinement factor and cavity Q factor can lead to low-threshold lasing and fast modulation speeds. the mode

volume of the cavity is calculated to be a sub-wavelength scale ($V = 0.37(\lambda/n)^3$), which is consistent with top-down fabricated nanobeam cavities with similar dimensions[89, 90]. Such an extremely small mode volume and high Q factor imply that the proposed design could potentially be utilized in the field of cavity quantum electrodynamics (cavity QED), for example by embedding a single quantum dot in nanowires. It should also be noted that the resonance wavelength of nanobeam cavities can be controlled by changing the lattice constant and the fill factor of photonic crystals, which correspond to the period (p) and diameter (d) in our design, and this will be studied further in the later section of this chapter.

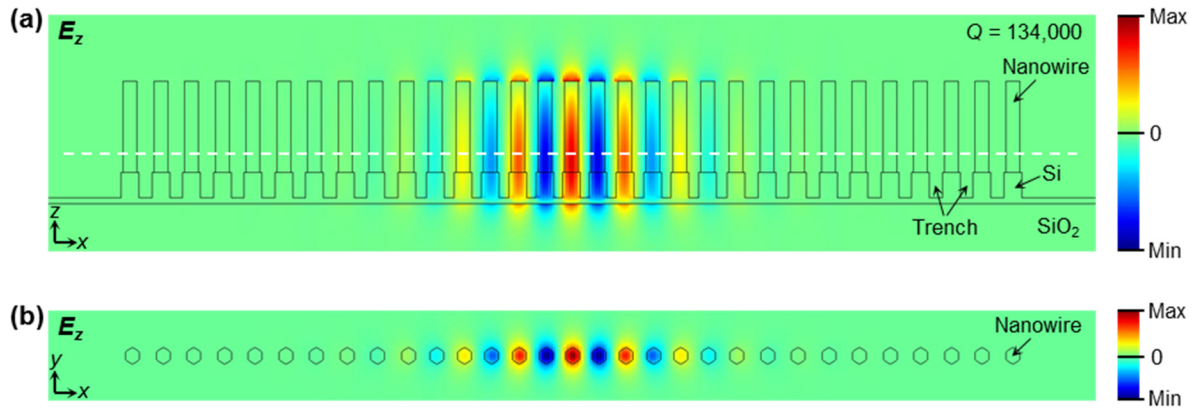

Figure 4.13 (a) Electric field profiles (E_z) of a fundamental TM-mode in xz-plane, and (b) a horizontal cross-section along the white dashed line in (a), both showing that the field is tightly confined in nanowires. A cavity Q of 134,000 and a resonant wavelength of 1,310 nm is obtained when p = 350 nm, d = 180 nm, and h = 700 nm.

4.3.2 Fabrication and lasing measurements

The fabrication of SOI platforms with mesas follows the process introduced in Chapter 2.3 and Chapter 4.2. Selective-area epitaxy of InGaAs/InGaP core/shell nanowires is conducted by MOCVD using TEGa, TMIn, TBAs, and TBP precursors. We have grown several samples with various cavity dimensions and material compositions in InGaAs nanowires to demonstrate lasing at wide wavelength ranges, and the composition of InGaP shell is adjusted according to the InGaAs material composition for close lattice-matching. The growth conditions are explained in detail in Chapter 2.2.3.

Nanowire arrays integrated on an SOI platform are depicted in the SEM images in Figure 4.14. Vertically grown InGaAs/InGaP core/shell nanowires exhibit smooth sidewalls and high uniformity in both the height and diameter between nanowires. Nanowire side facets are aligned

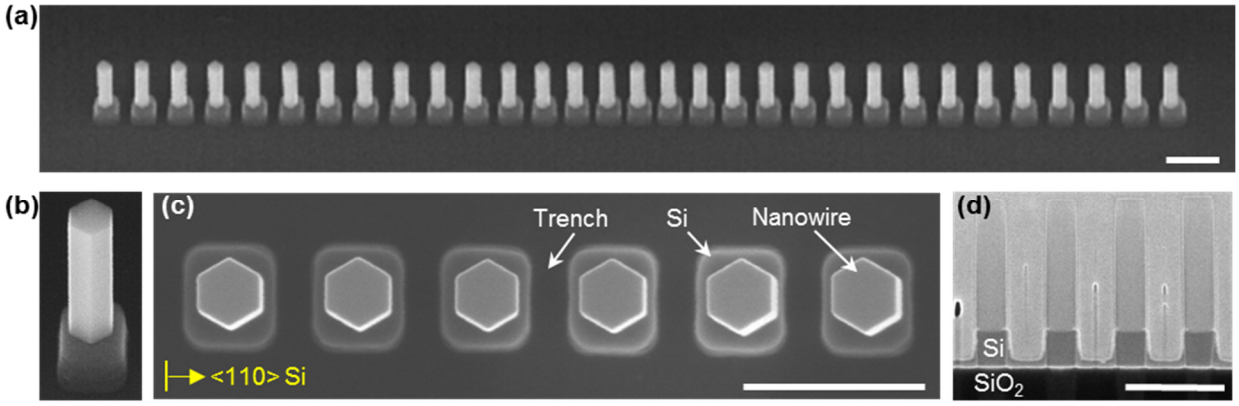

Figure 4.14 (a) 35° tilted SEM images of a nanowire array cavity, and (b) a close-up view, showing high uniformity and smooth sidewalls. (c) Top-view SEM image showing the nanowires aligned to a <110> direction of the silicon layer. (d) Cross-sectional SEM image of nanowires on a patterned SOI substrate measured by slicing the sample by focused ion beam (FIB) etching. Scale bars, 500 nm

perpendicular to the photonic lattice to achieve structural symmetry and high Q factor, as shown in Figure 4.14(c), which is realized by patterning nanohole arrays along the <110> direction of the silicon layer.

The μPL spectra of nanowires are measured at room temperature, with the setup introduced in previous chapters. A pulsed supercontinuum laser with 660 nm wavelength, 30 ps pulse width, and 78 MHz repetition rate is used for optical pumping. The indium portion of $In_xGa_{1-x}As$ nanowires is deduced from PL spectra of nanowire arrays grown on planar areas without silicon trenches, which is shown in Figure 2.23. μPL spectra of nanowire array cavities with different indium composition (x), lattice period (p), and diameter (d) are also measured by aligning the pump beam to the center of the cavities. As the pump spot size is 2 μm, the pumping area covers only the tapered section of the cavity. Lasing at longer wavelength is observed from the nanowire arrays with higher x and larger p and d, where the lasing peak positions at 1,120 nm, 1,230 nm, 1,320 nm, and 1,440 nm overlap well with the spontaneous emission spectra in Figure 4.15(a). The L-L plot, which represents an integrated cavity peak intensity as a function of the input pump power, is shown in Figure 4.15(b) for these four nanowire array lasers. Threshold pump powers of these lasers are estimated to be around 80−110 μJ/cm^2, which are deduced from the position of the kinks in the linear fitting. It is interesting to note that the slope efficiency (differential quantum efficiency) shows a tendency to decrease if the laser operates at a longer wavelength, except the laser emitting at 1,230nm which shows a higher slope efficiency than the laser emitting at 1,120 nm. This tendency can be understood considering an exponential increase of Auger recombination coefficient for InGaAs with larger x[91], which drastically increases non-radiative recombination at high-level carrier injection and decreases the internal quantum efficiency which is proportional to the slope efficiency[77]. We speculate that the reversed tendency between 1,120 nm and 1,230

nm lasers is stemming from the radiative efficiency of $In_{0.33}Ga_{0.67}As$ nanowires being higher than $In_{0.26}Ga_{0.74}As$ nanowires, as shown in Figure 4.16, which could be due to the material quality or core/shell interface quality. It should be highlighted that this is the first demonstration of monolithic nanowire lasers on a silicon platform operating at telecom-wavelengths. Room-temperature lasing in these vertical free-standing nanowire arrays reveals the validity of our approach in attaining a high cavity Q and confinement factor by forming bottom-up nanowire photonic crystals and achieving sufficient gain from InGaP-passivated InGaAs nanowires.

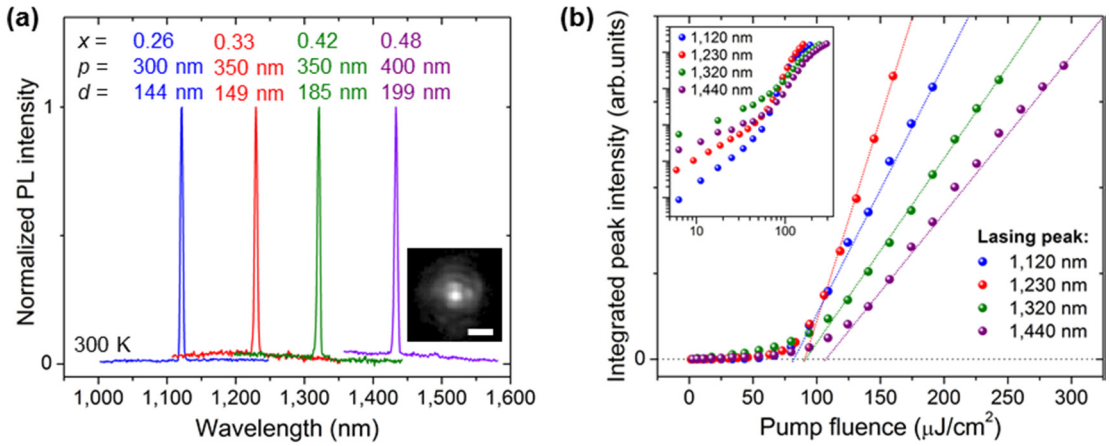

Figure 4.15 (a) Lasing spectra of nanowire array cavities on each sample. Inset: emission pattern above lasing threshold showing an interference fringe pattern. Scale bar, 5 μm. (c) L-L curves of nanobeam lasers in b. Lasing thresholds are estimated to be around 80−110 μJ/cm^2 from the linear fitting. Inset: L-L curves plotted in double-logarithmic scale.

Lasing characteristics of the laser operating at 1,320 nm, which exhibits a lasing threshold of 95 μJ/cm^2 (Figure 4.15(b)), are further analyzed to demonstrate typical behaviors of optically pumped nanowire array lasers operating in the telecom-wavelength regime. Log-scale PL spectra in Figure 4.17(a) show relative emission intensities from the nanobeam laser when the input pump

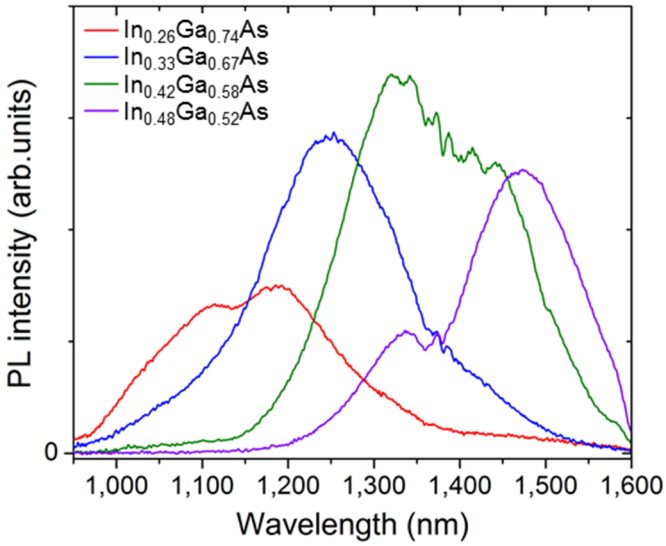

Figure 4.16 Relative PL intensities of InGaAs nanowire arrays with different material compositions, which are measured at a low pump fluence of 2.8 μJ/cm^2.

power is varied. A small cavity peak is observed above a broad spontaneous emission spectrum when the pump power is low. As the pump power is increased, the spontaneous peak blue-shifts due to a band-filling effect and the cavity peak also slightly blue-shifts due to a carrier-induced change of the refractive index[85]. The cavity peak intensity rapidly grows as the pump power is increased, while spontaneous emission is clamped above the lasing threshold, resulting in a side-mode suppression ratio (SMSR) of 13 dB at 2.55 times the threshold power. This is in contrast to the spontaneous emission from nanowire arrays on a planar area of a 220 nm-thick SOI substrate, which is not clamped by increasing the pump power (Figure 4.17(b)). The cavity peak linewidth shows a sudden decrease around the lasing threshold, as depicted in Figure 4.17(c), which is another indication of lasing action. The linewidth above the threshold is relatively high at around 2 meV, which is attributed to a pumping by ultrashort pulses that leads to a significant linewidth broadening by refractive index fluctuation[12, 34]. A double-logarithmic plot of the L-L curve in

Figure 4.17(c) shows an S-shape response, which indicates the transition to lasing from amplified spontaneous emission (ASE).

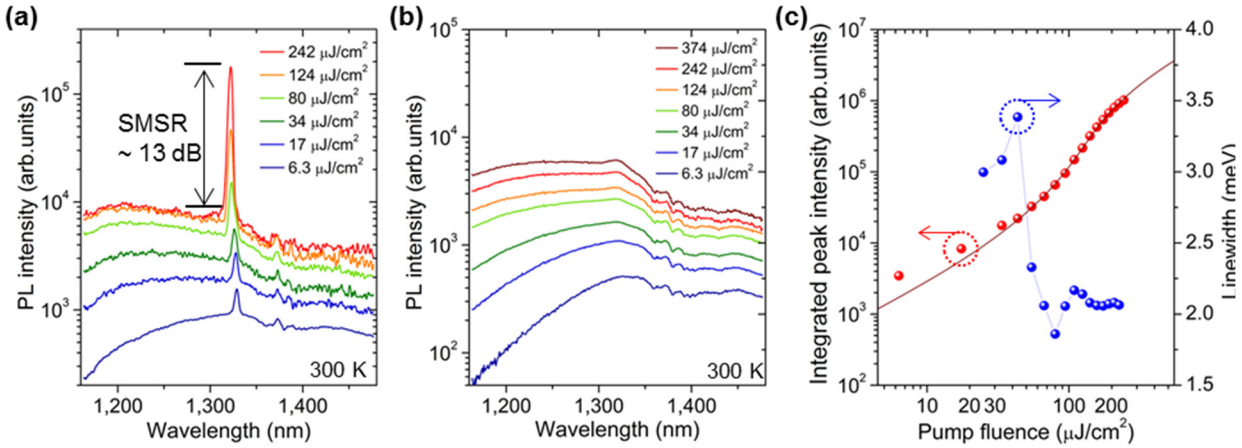

Figure 4.17 (a) Pump power-dependent PL spectra of the $In_{0.42}Ga_{0.58}As$ nanowire array laser, plotted in a log-scale. Spontaneous emission is clamped above the threshold, and SMSR of 13 dB is achieved at the pump fluence of 242 μJ/cm^2. (b) PL spectra of a nanowire array that does not form a cavity, showing that the spontaneous emission is not clamped by increasing the pump power. (c) Double-logarithmic L-L curve of the nanowire array laser showing an S-shape response and a sudden decrease of linewidth around lasing threshold.

4.3.3 Rate equation analysis

A standard rate equation analysis is employed to extract the Q factor and the spontaneous emission factor β of the nanobeam laser operating at 1,320 nm. The governing rate equations are eq. (1) and (2) in Chapter 3.2, while the parameters in the equations need to be modified since the dimension of the cavity and the material properties of InGaAs have changed. The new parameters used are shown in Table 4.1. The spontaneous emission and material gain spectra of the nanowires

Table 4.1: Parameters used in the rate equations	
Fraction of the pump light absorbed by the active nanowires (η)	0.01
SRH non-radiative recombination coefficient (A)[8]	1.43×10^{8} s^{-1}
Auger recombination coefficient (C)[10]	3×10^{-29} cm^{6} s^{-1}
Radiative carrier lifetime (τ_{sp})[8]	4 ns
Group index (n_g)	4
Gain coefficient (g_0)	3,050 cm^{-1}
Transparency carrier density (N_{tr})	1.14×10^{18} cm^{-3}
Third linearity parameter (N_s)	9.95×10^{17} cm^{-3}
Confinement factor (Γ)	0.548
Frequency of pump laser ($\omega_p=2\pi c/\lambda$)	2.854×10^{15} Hz

are calculated from Fermi's golden rule. A, τ_{sp}, and C are the Shockley-Read-Hall (SRH) non-radiative recombination coefficient[20], radiative carrier lifetime[20], and Auger recombination coefficient[91], respectively. L-L curves are calculated from the rate equations by varying β and $\bar{F}$, as shown in Figure 4.18. From the fitting, the nanobeam laser operating at 1,320 nm is estimated to exhibit β and Q of 0.16 and 495, respectively. Such a large β can only be accomplished from cavities with ultra-small mode volume and/or high cavity Q factor[77]. This result suggests that the proposed bottom-up nanobeam lasers have high potential for energy-efficient light sources with extremely low threshold. However, the fitted Q factor of 495 is significantly smaller that the Q factor of ~134,000 derived from FDTD simulations. As this is more than two orders of magnitude difference, additional FDTD simulations are conducted to verify the origin of this huge discrepancy. First, the effect of non-uniformities in nanowire dimensions is considered in

simulations. The diameter of nanowires exhibits a standard deviation of $\sigma \sim 5$ nm, and also $\sigma \sim 20$ nm for the nanowire height. If these dimensional non-uniformities of nanowires are included in the simulation, then the Q factor drops from 134,000 to 2,490. Next, the pumping conditions in our measurement setup are considered in simulations. The pump spot size is approximately 2 μm, which means that only the nanowires in the tapered section are optically pumped. Also, the electric field profile in Figure 4.13 shows that the cavity mode is tightly confined in the tapered section. This implies that the nanowires in reflector sections are absorptive, because all nanowires in the tapered section and the reflector sections are composed of the same materials and population inversion will occur only in the tapered area. If we consider an absorption coefficient of 104 cm^{-1} for the nanowires in reflector sections (which is the value of InGaAs around the band-edge[92, 93]), then the Q factor further drops from 2,490 to 730, which is comparable to the measured Q factor. These FDTD calculations suggest that the uniformity of nanowire dimensions needs to be improved to achieve higher cavity Q, which will lead to low-threshold lasing.

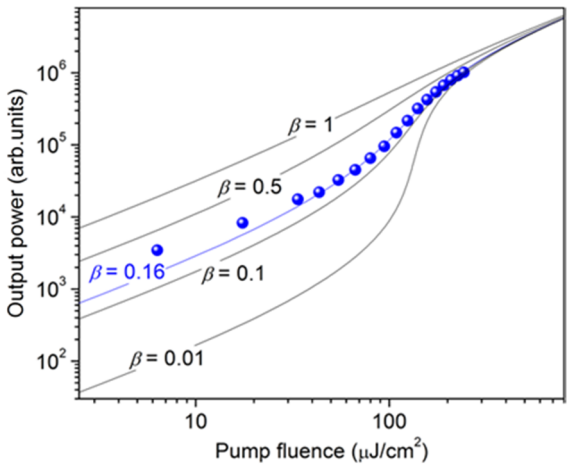

Figure 4.18 L-L curve plotted together with various β. The best fitting is achieved at β = 0.16 and Q = 495.

We also would like to note that several assumptions are made in determining the parameters used in rate equations. First, η and V, which are employed to determine the generation rate of carriers in the gain medium as a function of pump power, are subject to error because (a) the diffusion of (photo)carriers between nanowires and the underlying silicon layer and (b) the generation of carriers by absorption of the silicon layer are both neglected. Second, the SRH recombination coefficient A is largely dependent on the quality of core/shell interfaces due to an extremely high surface-to-volume ratio of nanowires, and thus careful studies are required to properly estimate A. Third, although τ_{sp} is assumed to be fixed to 4 ns in this rate equation fitting, actual radiative lifetime varies as the carrier density changes and is also modified when coupled to a cavity. The rate equation modeling could become more accurate if these effects are taken into account.

4.3.4 Tuning of lasing wavelengths

One of the biggest advantages of our approach is that the lasing wavelength is determined from nanobeam cavity dimensions, which can be controlled by lithography. Laser arrays with various operation wavelengths can, therefore, be integrated on a single chip by lithographically varying the pitch and diameter of nanowires, which provides a path for an ultracompact light source in wavelength-division multiplexing (WDM) systems. Figure 4.19(a) shows lasing spectra of seven $In_{0.33}Ga_{0.67}As$ nanowire array lasers, which are grown on two SOI pieces under identical epitaxy conditions. The measured lasing wavelengths range from 1,187 nm to 1,256 nm, which reveals wide tunability of the operation wavelengths of laser arrays on a chip. The validity and accuracy of tuning the lasing wavelength by lithography are also demonstrated by comparing the

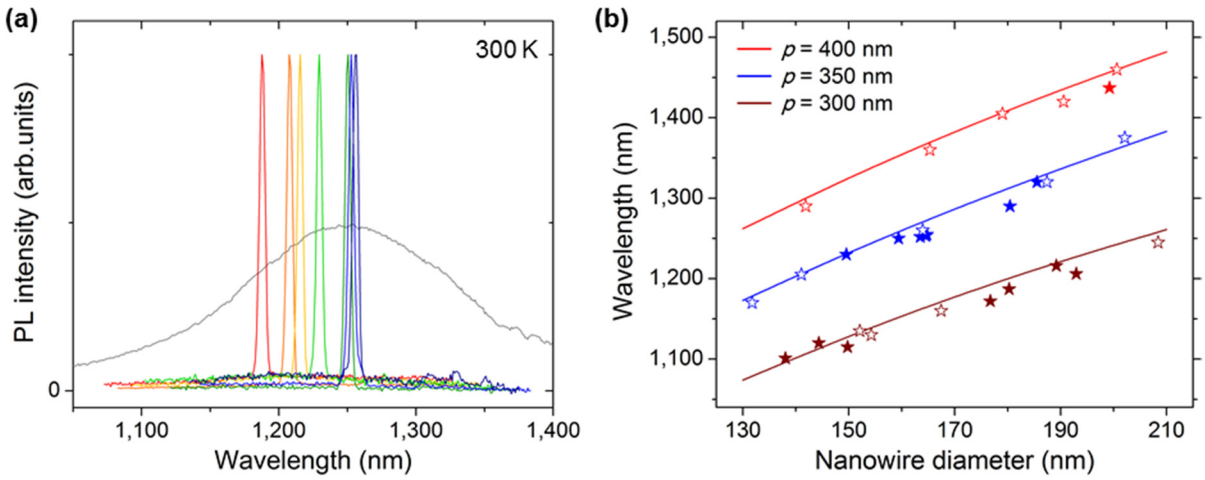

Figure 4.19 (a) Lasing spectra of seven $In_{0.33}Ga_{0.67}As$ nanobeam laser arrays grown on two samples. A spontaneous emission spectrum (grey line) is also shown for a reference. (b) Measured lasing wavelengths of nanobeam lasers (filled stars) plotted together with FDTD simulations (lines). Nanobeam cavities which have not reached lasing (open starts) are also shown for comparison.

measured wavelengths with FDTD simulations, as shown in Figure 4.19(b). The lasing wavelengths of entire nanowire array lasers with different indium compositions (x = 0.26, 0.33, 0.42, and 0.48) (filled stars) are plotted together with nanowire array cavities which have not reached lasing due to the mismatch between the indium composition and the cavity mode wavelength (open stars). An example of such cases is shown in Figure 4.20. As there is a slight non-uniformity between diameters of the nanowires constituting nanowire array cavities (typical standard deviation ~ 5 nm), an average value of nanowire diameters in the tapered section is used as the measured diameter in Figure 4.19(b). The measured peak wavelengths show a clear dependence on the period and diameter, and exhibit a good agreement with FDTD results (lines) within ±20 nm error, substantiating the feasibility of wavelength control without the need of external cavities. We speculate several reasons for the error, such as nanowire diameter fluctuation,

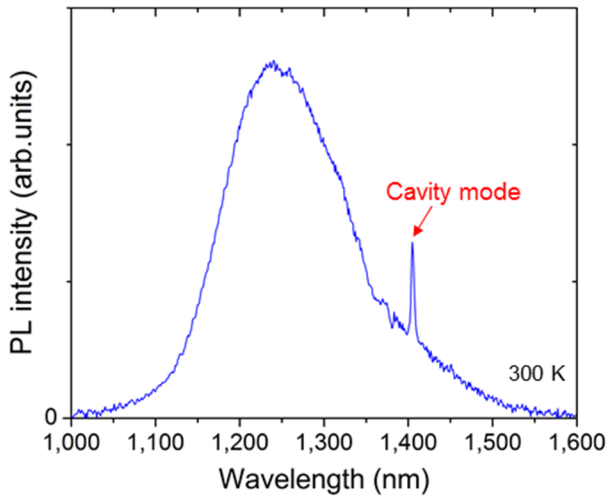

Figure 4.20 PL spectra of an $In_{0.33}Ga_{0.67}As$ nanowire array cavity with the period (p) of 400 nm. This nanobeam cavity has not shown lasing action, because of the mismatch between the indium composition and the position of cavity mode wavelength.

fabrication errors in silicon trench patterns, possible difference between the actual refractive index of nanowires and the index employed for FDTD simulations (n = 3.62), and a non-negligible effect of the nanowire height on a cavity mode wavelength since the height of nanowires does not match exactly with simulations (h = 700 nm). As shown in Figure 4.21(a), the cavity mode wavelength becomes longer when the nanowire height is increased. This is attributed to an increase of effective refractive index of the nanobeam cavity, because the field is confined well inside the high-index materials (nanowires and silicon) when nanowires are tall, while the portion of the electric field smearing out to the top (air, n = 1.0) and bottom (SiO2, n ~ 1.45) side increases when nanowires are short, as clearly shown in Figure 4.21(b).

In conclusion, we have demonstrated monolithic nanowire array lasers on an SOI platform operating in the wavelength range of 1,100 nm – 1,440 nm. Room-temperature lasing from these lasers is achieved by optical pumping, which reveals that nanobeam cavities composed of

InGaAs/InGaP core/shell nanowires exhibit high crystal quality and superior cavity properties. Lithographic control of nanobeam cavity dimensions has facilitated monolithic integration of laser arrays on a single chip with various wavelengths, suggesting a path towards an ultracompact light source in WDM systems.

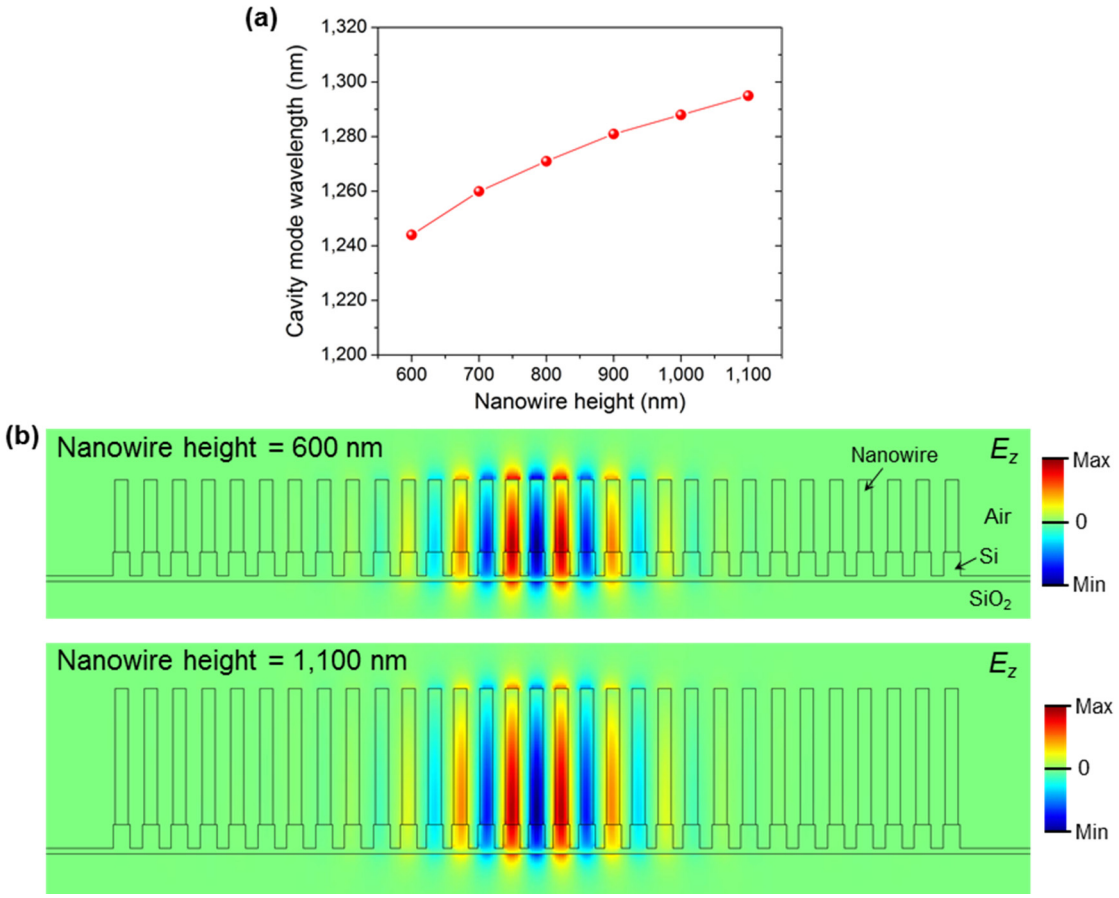

Figure 4.21 (a) FDTD simulations of cavity mode wavelengths of nanobeam cavities as a function of nanowire height. The period and diameter of nanowires are set to 350 nm and 160 nm, respectively. (b) Electric field profiles (E_z) when the nanowire height is 600 nm, and 1,100 nm.

5. Conclusions and outlook

The primary goal of this work was to demonstrate nanolasers on silicon, which could have significant impact on diverse application fields, including bio- and chemical sensing, medical applications, military applications, nonlinear optics, quantum optics, and communications. Among these various possibilities, the design and development of nanolasers in this research was mainly focused on the application to optical communications and photonic integrated circuits.

For this, we have first demonstrated the growth of III-V nanowires on silicon, by selective-area epitaxy using MOCVD. The nanowire approach overcomes the material quality degradation due to the lattice mismatch, leading to high-quality nanowires on silicon platforms. Also, SAE technique which is employed in this work can enable precise control of nanowire positions on the substrate, and thus enables forming well-ordered vertical nanowire arrays on substrates. Nearly 100 % vertical growth yields of GaAs, InAs, and InGaAs nanowires are achieved on silicon, SOI, and pre-patterned SOI substrates, which is crucial for forming bottom-up nanowire-based high-Q cavities.

Next, we have shown two different types of photonic crystal cavity designs, which are 1D photonic crystal cavities with artificial defects and 2D photonic crystal cavities without defects. In both designs, cavities are formed by bottom-up InGaAs/InGaP core/shell nanowires on thin SOI substrates, and room-temperature lasing is achieved from both designs. However, one of the limitations in these devices is that the SOI layer thickness needs to be thin for optical confinement, and therefore it is difficult to integrate these nanolasers with other photonic components.

To overcome this issue and achieve nanowire array lasers on standard thickness (220 nm)

SOI platforms with waveguides, a nanobeam cavity design on SOI mesas is proposed and experimentally demonstrated. Combining the bottom-up nanowire cavity designs with the epitaxy technique developed to integrate nanowires on pre-patterned silicon platforms was the key enabling idea to realize nanowire lasers on SOI and coupling these lasers to SOI waveguides. We also have demonstrated that the lasing wavelengths of nanobeam lasers are lithographically controllable and can be extended up to 1,440 nm, which covers telecommunication wavelengths and still operates at room temperature.

All these results exemplify a path toward ultracompact lasers on silicon photonic platforms for on-chip communications and photonic integrated circuits. However, further improvements are still necessary to employ the proposed nanolasers for real-world applications. The most important requirement would probably be achieving electrical operation of the nanowire array lasers. Although room-temperature operation and telecom-wavelength lasing shown in this work are an important breakthrough to achieve functional nanolasers on silicon platforms, these lasers are operated by optically pumping the nanowire arrays using external laser. This significantly limits the use of proposed lasers in many applications. For optical communications, especially, electrical operation of lasers is a crucial requirement to convert electrical data to optical data. Although electrical injection of nanowire lasers is not demonstrated in this work, this would be an important future work of this research. A preliminary design to realize electrical injection is introduced in Appendix A.

Another criticism which could be raised on the proposed nanowire lasers is that the SOI wafer used here is <111> orientation. Indeed, the demonstration of nanowire lasers on 220 nm-thick SOI substrates does not mean that these lasers are compatible with standard silicon photonic platforms. For the lasers to be truly compatible with silicon photonic foundries, there is no doubt

that the lasers need to be integrated on 220 nm-thick SOI (001) platforms. One possible solution could be adopting SOI (001) platforms and growing nanowires along 'angled' <111> direction of (001) planes. This approach is discussed in detail in Appendix B. Another possible solution would be growing vertical nanowires on SOI (001). Although nanowires typically tend to grow along <111> direction, there have been reports on growing vertical III-V nanowires on (001) substrates by template-based growth[94] or by controlling the growth conditions[95].

In conclusion, I firmly believe that the nanowire array photonic crystal lasers on silicon platforms, which are presented in this dissertation, could be a stepping stone for practical ultracompact lasers. Among various potential applications, the application to optical links and photonic integrated circuits will have significant impact in terms of speed, energy consumption, and functionalities. The proposed nanowire-based approach could also be employed for other optoelectronic and electronic devices, such as nanoscale photodetectors and transistors.

Appendix A. Electrical injection of nanowire lasers

Although optically pumped nanowire lasers have been widely studied, including the work in this dissertation, it is still extremely challenging to electrically operate nanowire lasers. There have been reports on electrically injected lasers based on AlGaN nanowires[96], CdS nanowires[97], and ZnO nanowires[98], but electrically injected III-V nanowire lasers have not been reported yet. The previously reported electrically injected nanowire lasers typically operate at cryogenic temperatures and function at visible or ultraviolet wavelengths, and electrical injection of III-V nanowire lasers at near-infrared wavelengths will be a tremendous breakthrough.

As demonstrated in Chapter 3 and 4, selective-area epitaxy of ordered nanowires enables forming high-Q cavities on SOI platforms. Therefore, we speculate that the same approach could be employed to design and demonstrated electrically injected III-V nanowire lasers. One of the requirements for electrical injection in our design is maintaining high Q factor with the presence of metals. Two metal contact pads are required for current injection in lasers, while typical metals are highly absorptive at near-infrared regime. Therefore, the Q factor is significantly degraded when metal is introduced in cavities. Another requirement is forming p-i-n heterostructures which could realize efficient current injection and achieve high carrier density in the gain medium.

The schematic illustration of proposed electrical injected lasers is depicted in Figure A.1. The nanowire heterostructure is composed of axial p-GaAs and i-InGaAs segments, which is grown on n-type SOI. This p-i-n heterostructure form type-I band alignment around InGaAs and ensures efficient carrier confinement in the InGaAs segment. The surface of nanowires will be passivated *in-situ* or *ex-situ*. Metal contact pads for n-Si can be deposited on Si outside the cavity area, and top metal contact pads (Au) will be deposited on top of p-GaAs segment of the nanowire.

The spacer to deposit top metal is composed of two polymers with different refractive indices, benzocyclobutene (BCB, n=1.54) and CYTOP^{TM} (Type CTL-809M, n=1.34) wherein the low-index CYTOP is a cladding layer, which helps minimizing the overlap of electric field with the top metal. It should be noted that other types of dielectric, such as silicon dioxide, silicon nitride, or aluminum oxide can be used instead of polymers.

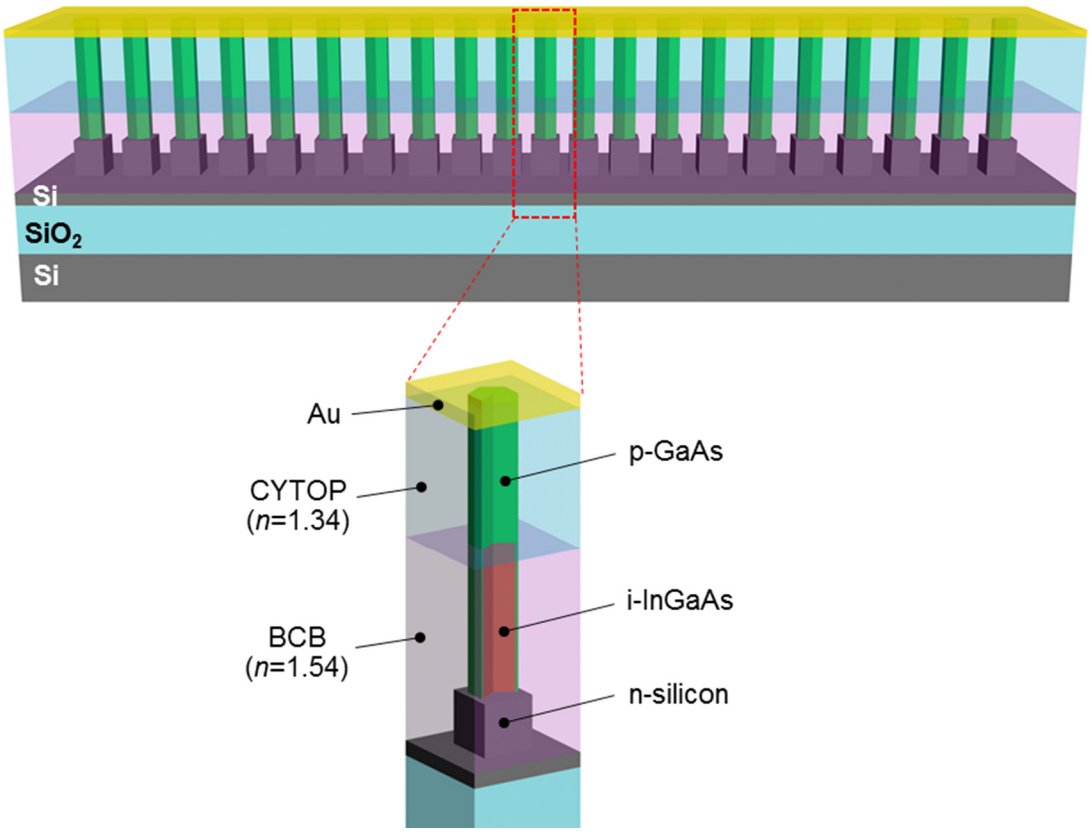

Figure A.1 Schematic of electrically injected nanowire array lasers.

The effect of low-index cladding layer is studied by FDTD simulations. When the nanowire height is 1,600 nm (i-InGaAs of 800 nm and p-GaAs of 800 nm) and there is no cladding, the field is strongly overlapping with Au on the top and thus the Q factor is only 220, as shown in Figure A.2(a). On the other hand, the introduction of CYTOP suppress the field to the lower side and the

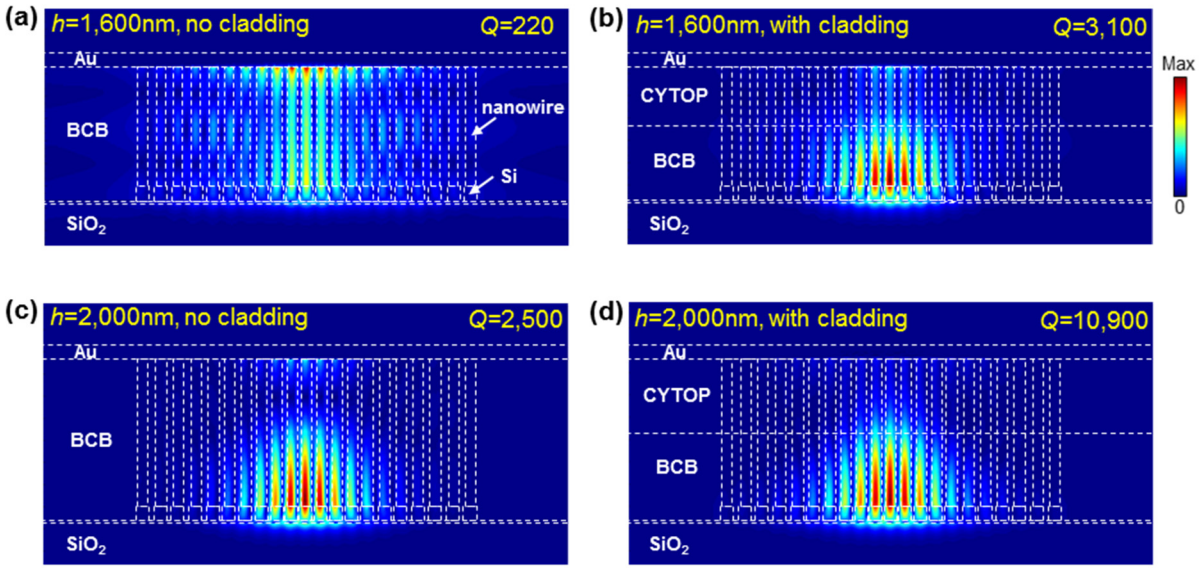

Figure A.2 Electric field profiles ($|E|$) of nanowire array cavities with and without a cladding layer when the nanowire height is (a,b) 1,600 nm, and (c,d) 2,000 nm.

Q factor increases to 3,100 (Figure A.2(b)). The Q factor can be further enhanced by employing taller nanowires, which helps reducing the overlap of electric fields with Au. When the nanowire height is increased to 2,000 nm (i-InGaAs of 1,000 nm and p-GaAs of 1,000 nm), the Q factor increases to 2,500 and 10,900 without and with the cladding, respectively. These results suggest that high-Q cavities with electrical injection configuration can be achieved by employing a cladding layer and tall nanowires. However, it should be noted that nanowires could bend if they are too tall, which will degrade the Q factor. Also, the carrier confinement will become less efficient if the i-InGaAs segment gets taller. Such a tradeoff need to be considered to satisfy both optical and electrical confinement of nanowire-based cavities and realize electrically pumped lasing.

Appendix B. Nanowire lasers on SOI (001) platform

The nanowire lasers demonstrated in this dissertation were formed on SOI (111) platforms, since nanowires grow along <111> direction. However, the lasers need to be integrated on SOI (001) platforms for compatibility with silicon photonic platforms and foundries. Figure B.1 shows a design of nanowire array nanobeam lasers integrated on SOI (001) with a SOI layer thickness of 220 nm. The key idea here is to form (111) planes by wet etching, and then growing nanowires along the angled <111> direction. 1D photonic crystal cavities can be formed on SOI (001) platforms by this approach. If nanowires are directly grown on SOI (001) substrates without revealing (111) planes by wet etching, on the other hand, then nanowires will randomly grow along any of the three angled <111> direction, and therefore photonic crystal cavities cannot be formed.

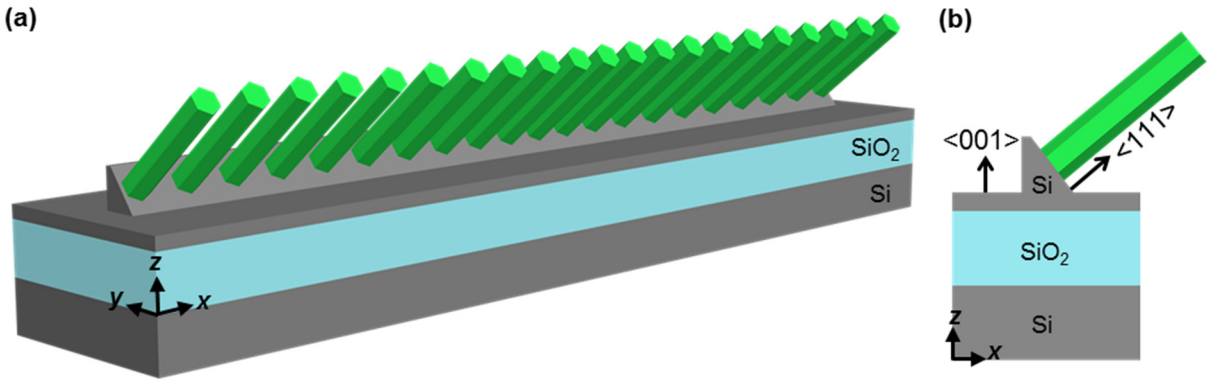

Figure B.1 (a) Schematic of nanowire array lasers on an SOI (001) platform. (b) Cross-sectional view along *xz*-plane.

Detailed fabrication processes are shown in Figure B.2. Dry etching is first performed (Figure B.2(b)), wherein waveguides can also be simultaneously fabricated. Next, an etch-mask (*e.g.* SiO_2 or Si_3N_4) is patterned on the platform and the substrate is etched by anisotropic wet

etchant like KOH (Figure B.2(c-d)). After removing the etch-mask, a growth mask is deposited and nanoholes are patterned, (Figure B.2(e-g)), and finally, nanowires are grown from the exposed (111) surfaces by MOCVD.

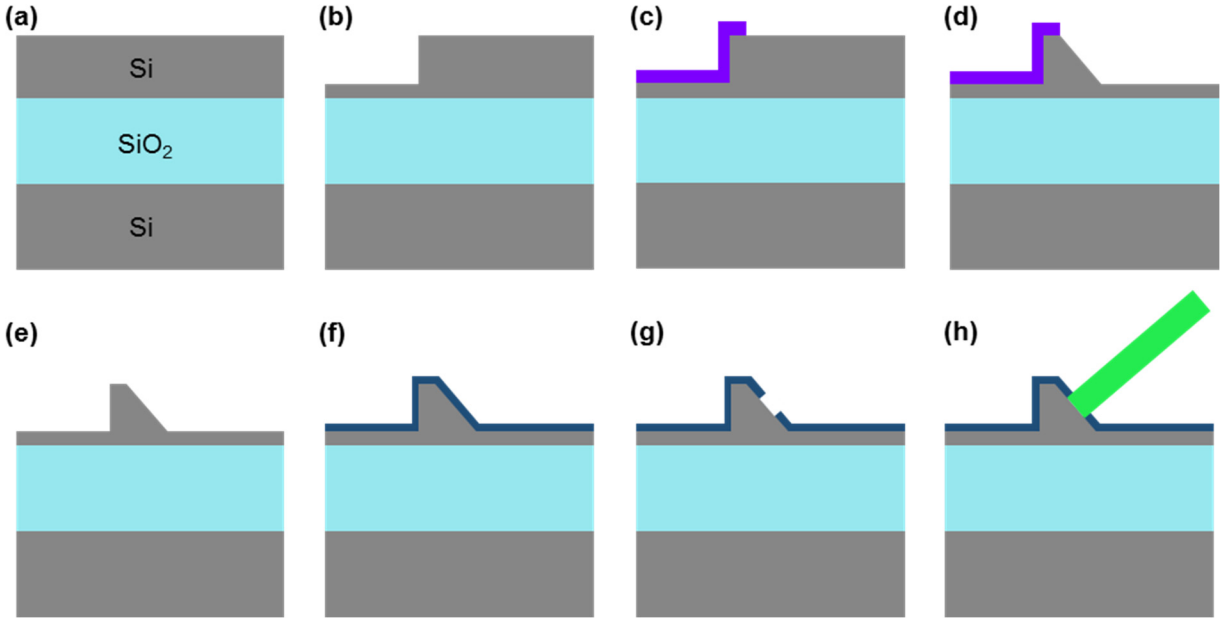

Figure B.2 Fabrication processes. (a) 220 nm-thick SOI (001). (b) Dry etching. (c) Mask patterning for wet etching. (d) Anisotropic wet etching by KOH. (e) Mask removal. (f) Growth mask deposition. (g) Nanohole patterning. (h) Nanowire growth.

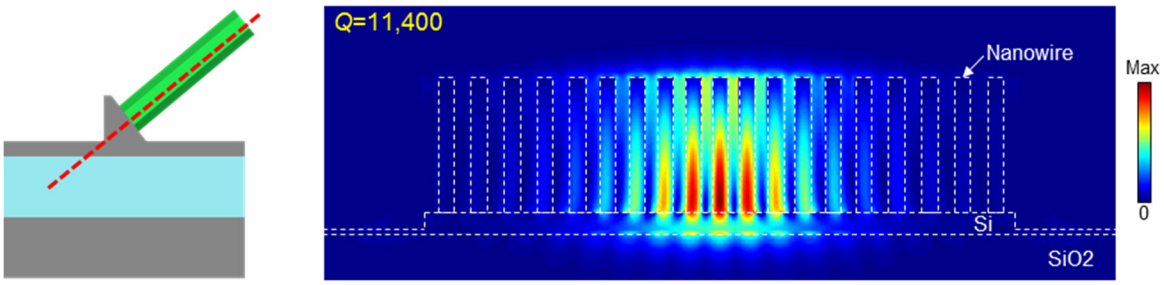

Figure B.3 Electric field profiles (|*E*|) of the fundamental cavity mode plotted along the dashed line.

The electric field profile is shown in Figure B.3. Although nanowires are grown along angled direction and so the nanobeam cavity is not symmetric, the electric field is still tightly confined in nanowires and a Q factor of 11,400 is achieved from FDTD simulations. Here, the SOI layer thickness is 220 nm and the slab thickness is 40 nm, which are the same as the nanobeam configuration shown in Chapter 4. The only difference is that the sidewalls of mesas are slanted and nanowires are tilted from the surface normal. These results suggest that the proposed design could be an enabling technique to integrated ultracompact bottom-up photonic crystal lasers on standard SOI photonic platforms.

References

[1] D. Reinsel, J. Gantz, and J. Rydning, "Data age 2025," *An International Data Corporation (IDC) White Paper,* 2017.

[2] T. Tekin, N. Pleros, R. Pitwon, and A. Hakansson, *Optical interconnects for data centers*: Woodhead Publishing, 2016.

[3] D.-X. Xu, J. H. Schmid, G. T. Reed, G. Z. Mashanovich, D. J. Thomson, M. Nedeljkovic*, et al.*, "Silicon photonic integration platform—Have we found the sweet spot?," *IEEE Journal of Selected Topics in Quantum Electronics,* vol. 20, pp. 189-205, 2014.

[4] M. J. Heck, H.-W. Chen, A. W. Fang, B. R. Koch, D. Liang, H. Park*, et al.*, "Hybrid silicon photonics for optical interconnects," *IEEE Journal of Selected Topics in Quantum Electronics,* vol. 17, pp. 333-346, 2011.

[5] "International Technology Roadmap for Semiconductors 2.0: 2015 Edition."

[6] A. W. Fang, H. Park, O. Cohen, R. Jones, M. J. Paniccia, and J. E. Bowers, "Electrically pumped hybrid AlGaInAs-silicon evanescent laser," *Optics express,* vol. 14, pp. 9203-9210, 2006.

[7] H. Park, A. W. Fang, S. Kodama, and J. E. Bowers, "Hybrid silicon evanescent laser fabricated with a silicon waveguide and III-V offset quantum wells," *Optics Express,* vol. 13, pp. 9460-9464, 2005.

[8] H. Wada and T. Kamijoh, "Room-temperature CW operation of InGaAsP lasers on Si fabricated by wafer bonding," *IEEE Photonics Technology Letters,* vol. 8, pp. 173-175, 1996.

[9] R. E. Camacho-Aguilera, Y. Cai, N. Patel, J. T. Bessette, M. Romagnoli, L. C. Kimerling, *et al.*, "An electrically pumped germanium laser," *Optics express,* vol. 20, pp. 11316-11320, 2012.

[10] J. Liu, L. C. Kimerling, and J. Michel, "Monolithic Ge-on-Si lasers for large-scale electronic–photonic integration," *Semiconductor Science and Technology,* vol. 27, p. 094006, 2012.

[11] M. Razeghi, R. Blondeau, M. Defour, F. Omnes, P. Maurel, and F. Brillouet, "First room-temperature cw operation of a GaInAsP/InP light-emitting diode on a silicon substrate," *Applied physics letters,* vol. 53, pp. 854-855, 1988.

[12] Z. Wang, B. Tian, M. Pantouvaki, W. Guo, P. Absil, J. Van Campenhout, *et al.*, "Room-temperature InP distributed feedback laser array directly grown on silicon," *Nature Photonics,* vol. 9, p. 837, 2015.

[13] T. Mårtensson, C. P. T. Svensson, B. A. Wacaser, M. W. Larsson, W. Seifert, K. Deppert, *et al.*, "Epitaxial III− V nanowires on silicon," *Nano Letters,* vol. 4, pp. 1987-1990, 2004.

[14] T. Bryllert, L.-E. Wernersson, L. Froberg, and L. Samuelson, "Vertical high-mobility wrap-gated InAs nanowire transistor," *IEEE Electron Device Letters,* vol. 27, pp. 323-325, 2006.

[15] S. W. Eaton, A. Fu, A. B. Wong, C.-Z. Ning, and P. Yang, "Semiconductor nanowire lasers," *Nature Reviews Materials,* vol. 1, p. 16028, 2016.

[16] P. Yang, R. Yan, and M. Fardy, "Semiconductor nanowire: what's next?," *Nano letters,* vol. 10, pp. 1529-1536, 2010.

[17] X. Wang, J. Zhou, J. Song, J. Liu, N. Xu, and Z. L. Wang, "Piezoelectric field effect transistor and nanoforce sensor based on a single ZnO nanowire," *Nano letters,* vol. 6, pp. 2768-2772, 2006.

[18] K. Tomioka, M. Yoshimura, and T. Fukui, "A III–V nanowire channel on silicon for high-performance vertical transistors," *Nature,* vol. 488, p. 189, 2012.

[19] K. Tomioka, J. Motohisa, S. Hara, K. Hiruma, and T. Fukui, "GaAs/AlGaAs core multishell nanowire-based light-emitting diodes on Si," *Nano letters,* vol. 10, pp. 1639-1644, 2010.

[20] R. Chen, T.-T. D. Tran, K. W. Ng, W. S. Ko, L. C. Chuang, F. G. Sedgwick*, et al.*, "Nanolasers grown on silicon," *Nature Photonics,* vol. 5, pp. 170-175, 2011.

[21] J. V. Holm, H. I. Jørgensen, P. Krogstrup, J. Nygård, H. Liu, and M. Aagesen, "Surface-passivated GaAsP single-nanowire solar cells exceeding 10% efficiency grown on silicon," *Nature communications,* vol. 4, p. 1498, 2013.

[22] S. Xie, H. Kim, W.-J. Lee, A. C. Farrell, J. P. David, and D. L. Huffaker, "InAs/InAsP Core/Shell Nanowire Photodiode on a Si Substrate."

[23] D. E. Perea, J. E. Allen, S. J. May, B. W. Wessels, D. N. Seidman, and L. J. Lauhon, "Three-dimensional nanoscale composition mapping of semiconductor nanowires," *Nano letters,* vol. 6, pp. 181-185, 2006.

[24] Y. Wang, V. Schmidt, S. Senz, and U. Gösele, "Epitaxial growth of silicon nanowires using an aluminium catalyst," *Nature nanotechnology,* vol. 1, p. 186, 2006.

[25] S. Plissard, G. Larrieu, X. Wallart, and P. Caroff, "High yield of self-catalyzed GaAs nanowire arrays grown on silicon via gallium droplet positioning," *Nanotechnology,* vol. 22, p. 275602, 2011.

[26] J. Shapiro, A. Lin, D. Huffaker, and C. Ratsch, "Potential energy surface of In and Ga adatoms above the (111) A and (110) surfaces of a GaAs nanopillar," *Physical Review B,* vol. 84, p. 085322, 2011.

[27] J. Noborisaka, J. Motohisa, and T. Fukui, "Catalyst-free growth of GaAs nanowires by selective-area metalorganic vapor-phase epitaxy," *Applied Physics Letters,* vol. 86, p. 213102, 2005.

[28] J. Shapiro, A. Lin, P. Wong, A. Scofield, C. Tu, P. Senanayake*, et al.*, "InGaAs heterostructure formation in catalyst-free GaAs nanopillars by selective-area metal-organic vapor phase epitaxy," *Applied Physics Letters,* vol. 97, p. 243102, 2010.

[29] M. Moewe, L. C. Chuang, S. Crankshaw, C. Chase, and C. Chang-Hasnain, "Atomically sharp catalyst-free wurtzite Ga As⁄ Al Ga As nanoneedles grown on silicon," *Applied Physics Letters,* vol. 93, p. 023116, 2008.

[30] A. C. Scofield, J. N. Shapiro, A. Lin, A. D. Williams, P.-S. Wong, B. L. Liang*, et al.*, "Bottom-up photonic crystal cavities formed by patterned III–V nanopillars," *Nano letters,* vol. 11, pp. 2242-2246, 2011.

[31] P. Senanayake, C.-H. Hung, J. Shapiro, A. Scofield, A. Lin, B. S. Williams*, et al.*, "3D nanopillar optical antenna photodetectors," *Optics express,* vol. 20, pp. 25489-25496, 2012.

[32] A. C. Scofield, A. Lin, M. Haddad, and D. L. Huffaker, "Axial Diffusion Barriers in Near-Infrared Nanopillar LEDs," *Nano letters,* vol. 14, pp. 6037-6041, 2014.

[33] G. Mariani, A. C. Scofield, C.-H. Hung, and D. L. Huffaker, "GaAs nanopillar-array solar cells employing in situ surface passivation," *Nature communications,* vol. 4, p. 1497, 2013.

[34] J. Tatebayashi, S. Kako, J. Ho, Y. Ota, S. Iwamoto, and Y. Arakawa, "Room-temperature lasing in a single nanowire with quantum dots," *Nature Photonics,* vol. 9, p. 501, 2015.

[35] A. C. Farrell, P. Senanayake, X. Meng, N. Y. Hsieh, and D. L. Huffaker, "Diode characteristics approaching bulk limits in GaAs nanowire array photodetectors," *Nano letters,* vol. 17, pp. 2420-2425, 2017.

[36] L. C. Chuang, F. G. Sedgwick, R. Chen, W. S. Ko, M. Moewe, K. W. Ng*, et al.*, "GaAs-based nanoneedle light emitting diode and avalanche photodiode monolithically integrated on a silicon substrate," *Nano letters,* vol. 11, pp. 385-390, 2010.

[37] Y. Kohashi, T. Sato, K. Ikejiri, K. Tomioka, S. Hara, and J. Motohisa, "Influence of growth temperature on growth of InGaAs nanowires in selective-area metal–organic vapor-phase epitaxy," *Journal of Crystal Growth,* vol. 338, pp. 47-51, 2012.

[38] J. Motohisa, J. Noborisaka, J. Takeda, M. Inari, and T. Fukui, "Catalyst-free selective-area MOVPE of semiconductor nanowires on (111) B oriented substrates," *Journal of crystal growth,* vol. 272, pp. 180-185, 2004.

[39] W. Hobson, S. Pearton, D. Kozuch, and M. Stavola, "Comparison of gallium and arsenic precursors for GaAs carbon doping by organometallic vapor phase epitaxy using CCl4," *Applied Physics Letters,* vol. 60, pp. 3259-3261, 1992.

[40] C. Caneau, R. Bhat, C. Chang, K. Kash, and M. Koza, "Selective organometallic vapor phase epitaxy of Ga and In compounds: a comparison of TMIn and TEGa versus TMIn and TMGa," *Journal of crystal growth,* vol. 132, pp. 364-370, 1993.

[41] W. Hobson, T. Harris, C. Abernathy, and S. Pearton, "High quality Al x Ga1− x As grown by organometallic vapor phase epitaxy using trimethylamine alane as the aluminum precursor," *Applied physics letters,* vol. 58, pp. 77-79, 1991.

[42] T. Sato, J. Motohisa, J. Noborisaka, S. Hara, and T. Fukui, "Growth of InGaAs nanowires by selective-area metalorganic vapor phase epitaxy," *Journal of Crystal Growth,* vol. 310, pp. 2359-2364, 2008.

[43] K. Tomioka, J. Motohisa, S. Hara, and T. Fukui, "Control of InAs nanowire growth directions on Si," *Nano letters,* vol. 8, pp. 3475-3480, 2008.

[44] M. T. Björk, H. Schmid, C. M. Breslin, L. Gignac, and H. Riel, "InAs nanowire growth on oxide-masked< 111> silicon," *Journal of crystal growth,* vol. 344, pp. 31-37, 2012.

[45] M. Björk, H. Schmid, C. Bessire, K. Moselund, H. Ghoneim, S. Karg*, et al.*, "Si–InAs heterojunction Esaki tunnel diodes with high current densities," *Applied Physics Letters,* vol. 97, p. 163501, 2010.

[46] W. Wei, X.-Y. Bao, C. Soci, Y. Ding, Z.-L. Wang, and D. Wang, "Direct heteroepitaxy of vertical InAs nanowires on Si substrates for broad band photovoltaics and photodetection," *Nano letters,* vol. 9, pp. 2926-2934, 2009.

[47] G. Koblmüller and G. Abstreiter, "Growth and properties of InGaAs nanowires on silicon," *physica status solidi (RRL)-Rapid Research Letters,* vol. 8, pp. 11-30, 2014.

[48] H. Seki and A. Koukitu, "Solid composition of alloy semiconductors grown by MOVPE, MBE, VPE hand ALE," *Journal of crystal growth,* vol. 98, pp. 118-126, 1989.

[49] K. Tomioka, K. Ikejiri, T. Tanaka, J. Motohisa, S. Hara, K. Hiruma*, et al.*, "Selective-area growth of III-V nanowires and their applications," *Journal of Materials Research,* vol. 26, pp. 2127-2141, 2011.

[50] J. Treu, M. Speckbacher, K. Saller, S. Morkötter, M. Döblinger, X. Xu*, et al.*, "Widely tunable alloy composition and crystal structure in catalyst-free InGaAs nanowire arrays grown by selective area molecular beam epitaxy," *Applied Physics Letters,* vol. 108, p. 053110, 2016.

[51] M. Tokushima, H. Yamada, and Y. Arakawa, "1.5-μ m-wavelength light guiding in waveguides in square-lattice-of-rod photonic crystal slab," *Applied physics letters,* vol. 84, pp. 4298-4300, 2004.

[52] A. C. Scofield, S.-H. Kim, J. N. Shapiro, A. Lin, B. Liang, A. Scherer*, et al.*, "Bottom-up photonic crystal lasers," *Nano letters,* vol. 11, pp. 5387-5390, 2011.

[53] S. Tanaka, T. Akiyama, S. Sekiguchi, and K. Morito, "Silicon photonics optical transmitter technology for Tb/s-class I/O co-packaged with CPU," *FUJUTSI Sci. Technol. J,* vol. 50, pp. 123-131, 2014.

[54] K. Ikejiri, T. Sato, H. Yoshida, K. Hiruma, J. Motohisa, S. Hara*, et al.*, "Growth characteristics of GaAs nanowires obtained by selective area metal–organic vapour-phase epitaxy," *Nanotechnology,* vol. 19, p. 265604, 2008.

[55] L. Xu and Q. Huang, "Growth process modeling of iii–v nanowire synthesis via selective area metal–organic chemical vapor deposition," *IEEE Transactions on Nanotechnology,* vol. 13, pp. 1093-1101, 2014.

[56] A. C. Farrell, W.-J. Lee, P. Senanayake, M. A. Haddad, S. V. Prikhodko, and D. L. Huffaker, "High-Quality InAsSb Nanowires Grown by Catalyst-Free Selective-Area Metal–Organic Chemical Vapor Deposition," *Nano letters,* vol. 15, pp. 6614-6619, 2015.

[57] J. Cao, D. Pavlidis, Y. Park, J. Singh, and A. Eisenbach, "Improved quality GaN by growth on compliant silicon-on-insulator substrates using metalorganic chemical vapor deposition," *Journal of applied physics,* vol. 83, pp. 3829-3834, 1998.

[58] N. Karam, V. Haven, S. Vernon, F. Namavar, N. El-Masry, N. Haegel*, et al.*, "Growth and Characterization of InP/GaAs on SOI by MOCVD," *MRS Online Proceedings Library Archive,* vol. 198, 1990.

[59] M.-K. Kim, A. M. Lakhani, and M. C. Wu, "Efficient waveguide-coupling of metal-clad nanolaser cavities," *Optics express,* vol. 19, pp. 23504-23512, 2011.

[60] R. Agarwal, C. J. Barrelet, and C. M. Lieber, "Lasing in single cadmium sulfide nanowire optical cavities," *Nano letters,* vol. 5, pp. 917-920, 2005.

[61] D. Saxena, S. Mokkapati, P. Parkinson, N. Jiang, Q. Gao, H. H. Tan*, et al.*, "Optically pumped room-temperature GaAs nanowire lasers," *Nature Photonics,* vol. 7, pp. 963-968, 2013.

[62] M. H. Huang, S. Mao, H. Feick, H. Yan, Y. Wu, H. Kind*, et al.*, "Room-temperature ultraviolet nanowire nanolasers," *science,* vol. 292, pp. 1897-1899, 2001.

[63] N. V. Triviño, R. Butte, J.-F. Carlin, and N. Grandjean, "Continuous wave blue lasing in III-nitride nanobeam cavity on silicon," *Nano letters,* vol. 15, pp. 1259-1263, 2015.

[64] H.-G. Park, S.-H. Kim, S.-H. Kwon, Y.-G. Ju, J.-K. Yang, J.-H. Baek*, et al.*, "Electrically driven single-cell photonic crystal laser," *Science,* vol. 305, pp. 1444-1447, 2004.

[65] K. Takeda, T. Sato, A. Shinya, K. Nozaki, W. Kobayashi, H. Taniyama*, et al.*, "Few-fJ/bit data transmissions using directly modulated lambda-scale embedded active region photonic-crystal lasers," *Nature Photonics,* vol. 7, p. 569, 2013.

[66] M. Nomura, S. Iwamoto, K. Watanabe, N. Kumagai, Y. Nakata, S. Ishida*, et al.*, "Room temperature continuous-wave lasing in photonic crystal nanocavity," *Optics Express,* vol. 14, pp. 6308-6315, 2006.

[67] M. Lončar, D. Nedeljković, T. P. Pearsall, J. Vučković, A. Scherer, S. Kuchinsky*, et al.*, "Experimental and theoretical confirmation of Bloch-mode light propagation in planar photonic crystal waveguides," *Applied physics letters,* vol. 80, pp. 1689-1691, 2002.

[68] L. Ferrier, O. El Daif, X. Letartre, P. R. Romeo, C. Seassal, R. Mazurczyk*, et al.*, "Surface emitting microlaser based on 2D photonic crystal rod lattices," *Optics Express,* vol. 17, pp. 9780-9788, 2009.

[69] J.-H. Choi, Y.-S. No, M.-S. Hwang, S.-Y. Kwon, K.-Y. Jeong, S.-H. Kwon*, et al.*, "Low-threshold photonic-band-edge laser using iron-nail-shaped rod array," *Applied Physics Letters,* vol. 104, p. 091120, 2014.

[70] W. S. Fegadolli, S.-H. Kim, P. A. Postigo, and A. Scherer, "Hybrid single quantum well InP/Si nanobeam lasers for silicon photonics," *Optics letters,* vol. 38, pp. 4656-4658, 2013.

[71] M. Notomi, E. Kuramochi, and H. Taniyama, "Ultrahigh-Q nanocavity with 1D photonic gap," *Optics Express,* vol. 16, pp. 11095-11102, 2008.

[72] K.-Y. Jeong, Y.-S. No, Y. Hwang, K. S. Kim, M.-K. Seo, H.-G. Park*, et al.*, "Electrically driven nanobeam laser," *Nature communications,* vol. 4, p. 2822, 2013.

[73] B.-H. Ahn, J.-H. Kang, M.-K. Kim, J.-H. Song, B. Min, K.-S. Kim*, et al.*, "One-dimensional parabolic-beam photonic crystal laser," *Optics Express,* vol. 18, pp. 5654-5660, 2010.

[74] B. Mayer, L. Janker, B. Loitsch, J. Treu, T. Kostenbader, S. Lichtmannecker*, et al.*, "Monolithically integrated high-β nanowire lasers on silicon," *Nano letters,* vol. 16, pp. 152-156, 2015.

[75] J. T. Robinson, C. Manolatou, L. Chen, and M. Lipson, "Ultrasmall mode volumes in dielectric optical microcavities," *Physical review letters,* vol. 95, p. 143901, 2005.

[76] H. Altug, D. Englund, and J. Vučković, "Ultrafast photonic crystal nanocavity laser," *Nature Physics,* vol. 2, pp. 484-488, 2006.

[77] L. A. Coldren, S. W. Corzine, and M. L. Mashanovitch, *Diode lasers and photonic integrated circuits*: John Wiley & Sons, 2012.

[78] S. Kim, S. Ahn, J. Lee, H. Jeon, P. Regreny, C. Seassal*, et al.*, "Milliwatt-level fiber-coupled laser power from photonic crystal band-edge laser," *Optics Express,* vol. 19, pp. 2105-2110, 2011.

[79] K. Hirose, Y. Liang, Y. Kurosaka, A. Watanabe, T. Sugiyama, and S. Noda, "Watt-class high-power, high-beam-quality photonic-crystal lasers," *Nature photonics,* vol. 8, p. 406, 2014.

[80] B. Mayer, D. Rudolph, G. Abstreiter, G. Bracher, G. Koblmüller, J. J. Finley*, et al.*, "Lasing from individual GaAs-AlGaAs core-shell nanowires up to room temperature," *Nature communications,* vol. 4, p. 2931, 2013.

[81] F. Lu, I. Bhattacharya, H. Sun, T.-T. D. Tran, K. W. Ng, G. N. Malheiros-Silveira*, et al.*, "Nanopillar quantum well lasers directly grown on silicon and emitting at silicon-transparent wavelengths," *Optica,* vol. 4, pp. 717-723, 2017.

[82] A. Yokoo, M. Takiguchi, M. D. Birowosuto, K. Tateno, G. Zhang, E. Kuramochi*, et al.*, "Subwavelength nanowire lasers on a silicon photonic crystal operating at telecom wavelengths," *ACS Photonics,* vol. 4, pp. 355-362, 2017.

[83] A. Chin, S. Vaddiraju, A. Maslov, C. Ning, M. Sunkara, and M. Meyyappan, "Near-infrared semiconductor subwavelength-wire lasers," *Applied Physics Letters,* vol. 88, p. 163115, 2006.

[84] K. Komolibus, A. C. Scofield, K. Gradkowski, T. J. Ochalski, H. Kim, D. L. Huffaker*, et al.*, "Improved room-temperature luminescence of core-shell InGaAs/GaAs nanopillars via lattice-matched passivation," *Applied Physics Letters,* vol. 108, p. 061104, 2016.

[85] B. R. Bennett, R. A. Soref, and J. A. Del Alamo, "Carrier-induced change in refractive index of InP, GaAs and InGaAsP," *IEEE Journal of Quantum Electronics,* vol. 26, pp. 113-122, 1990.

[86] T. Stettner, T. Kostenbader, D. Ruhstorfer, J. Bissinger, H. Riedl, M. Kaniber*, et al.*, "Direct Coupling of Coherent Emission from Site-Selectively Grown III–V Nanowire Lasers into Proximal Silicon Waveguides," *ACS Photonics,* vol. 4, pp. 2537-2543, 2017.

[87] G. N. Malheiros-Silveira, F. Lu, I. Bhattacharya, T.-T. D. Tran, H. Sun, and C. J. Chang-Hasnain, "III–V Compound Semiconductor Nanopillars Monolithically Integrated to Silicon Photonics," *ACS Photonics,* vol. 4, pp. 1021-1025, 2017.

[88] H. Dinges, H. Burkhard, R. Lösch, H. Nickel, and W. Schlapp, "Refractive indices of InAlAs and InGaAs/InP from 250 to 1900 nm determined by spectroscopic ellipsometry," *Applied surface science,* vol. 54, pp. 477-481, 1992.

[89] P. B. Deotare, M. W. McCutcheon, I. W. Frank, M. Khan, and M. Lončar, "High quality factor photonic crystal nanobeam cavities," *Applied Physics Letters,* vol. 94, p. 121106, 2009.

[90] Y. Zhang, M. Khan, Y. Huang, J. Ryou, P. Deotare, R. Dupuis*, et al.*, "Photonic crystal nanobeam lasers," *Applied Physics Letters,* vol. 97, p. 051104, 2010.

[91] T. Gfroerer, L. Priestley, M. Fairley, and M. Wanlass, "Temperature dependence of nonradiative recombination in low-band gap In x Ga 1− x As/InAs y P 1− y double heterostructures grown on InP substrates," *Journal of applied physics,* vol. 94, pp. 1738-1743, 2003.

[92] E. Zielinski, H. Schweizer, K. Streubel, H. Eisele, and G. Weimann, "Excitonic transitions and exciton damping processes in InGaAs/InP," *Journal of applied physics,* vol. 59, pp. 2196-2204, 1986.

[93] M. Alam, M. Rahman, M. Islam, A. Bhuiyan, and M. Yamada, "Refractive index, absorption coefficient, and photoelastic constant: Key parameters of InGaAs material relevant to InGaAs-based device performance," in *Indium Phosphide & Related Materials, 2007. IPRM'07. IEEE 19th International Conference on*, 2007, pp. 343-346.

[94] M. Borg, H. Schmid, K. E. Moselund, G. Signorello, L. Gignac, J. Bruley*, et al.*, "Vertical III–V nanowire device integration on Si (100)," *Nano letters,* vol. 14, pp. 1914-1920, 2014.

[95] J. Wang, S. b. R. Plissard, M. A. Verheijen, L.-F. Feiner, A. Cavalli, and E. P. Bakkers, "Reversible switching of InP nanowire growth direction by catalyst engineering," *Nano letters,* vol. 13, pp. 3802-3806, 2013.

[96] K. Li, X. Liu, Q. Wang, S. Zhao, and Z. Mi, "Ultralow-threshold electrically injected AlGaN nanowire ultraviolet lasers on Si operating at low temperature," *Nature nanotechnology,* vol. 10, p. 140, 2015.

[97] X. Duan, Y. Huang, R. Agarwal, and C. M. Lieber, "Single-nanowire electrically driven lasers," *Nature,* vol. 421, pp. 241-245, 2003.

[98] S. Chu, G. Wang, W. Zhou, Y. Lin, L. Chernyak, J. Zhao*, et al.*, "Electrically pumped waveguide lasing from ZnO nanowires," *Nature nanotechnology,* vol. 6, p. 506, 2011.