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FEM-Based Capacitor Structure Optimization Studies for Large-Scale High Energy Density Electrostatic Energy Storage Device

A thesis submitted in partial satisfaction

of the requirements for the degree Master of Science

in Materials Science and Engineering

by

Harshit Ranjan

2023

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2023

ABSTRACT OF THE THESIS

FEM-Based Capacitor Structure Optimization Studies for Large-Scale High Energy Density Electrostatic Energy Storage Device

by

Harshit Ranjan

Master of Science in Materials Science and Engineering University of California, Los Angeles, 2023 Professor Subramanian Srikanteswara Iyer, Chair

The growing demand for clean and sustainable energy sources necessitates effective energy storage solutions. In response to this challenge, this thesis proposes a decentralized approach to energy storage by leveraging high-density rolled polymer-based capacitors. The aim is to address the intermittent nature of renewable energy generation and develop a storage system that is not only affordable and sustainable but also easily deployable. In their typical form, capacitors do not exhibit high energy capacity. Therefore, this research emphasizes the importance of optimizing surface area, implementing high voltage storage capabilities (up to 10 kV), and utilizing a polymeric material with a high dielectric constant. By focusing on these factors, the research aims to overcome the limitations of conventional capacitors and develop a storage system with significantly increased energy density, enabling more efficient energy storage for clean and

sustainable sources. The study also explores the potential benefits of introducing trenches into the capacitor structure, with the objective of enhancing capacitance and energy density by increasing the surface area. The validation of these enhancements is carried out using simulation techniques, ensuring a comprehensive evaluation of the proposed approach. It is important to note that while trenches hold promise for increasing capacitance, the thesis acknowledges the need to carefully consider the potential drawbacks: the introduction of trenches can lead to increased electric field concentration, which may result in dielectric breakdown and compromise the overall performance and reliability of the capacitor. Therefore, the primary objective of this thesis is to identify the optimal capacitor configuration that maximizes capacitance enhancement while maintaining the capacitor's integrity.

The thesis of Harshit Ranjan is approved.

Jamie Marian

Qibing Pei

Subramanian Srikanteswara Iyer, Committee Chair

University of California, Los Angeles

2023

Dedicated to my family

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CHAPTER 1: INTRODUCTION

1.1 Motivation

The modern world is heavily reliant on energy, and the increasing demand [1] for clean and sustainable sources of energy has made energy storage an important topic of research. Renewable energy sources are widely regarded as a more sustainable alternative to traditional fossil fuels. They have many advantages, such as producing lower emissions, being sustainable over the long term, and becoming more cost-effective as technology improves. However, there are also some disadvantages to consider. One such major challenge stems from the "intermittent" nature of renewable energy generation, depicted in Figure 1-2. Unlike traditional power sources, solar and wind energy production can fluctuate, posing difficulties in maintaining a consistent energy supply. This intermittency can be visualized through the "duck curve," a graph depicting the net load on the grid over time (Figure 1-1). During peak demand periods in the morning and evening, the net load on the grid reaches its highest point. Conversely, during midday, when energy demand is lowest, solar cells generate surplus electricity, leading to a "belly" in the curve. Without effective storage solutions, this excess energy goes to waste, limiting the accessibility and reliability of renewable energy. Addressing these challenges requires innovative energy storage solutions that can effectively stabilize energy demand fluctuations and maximize the utilization of renewable energy resources.

Existing energy storage methods for renewables have limitations, high costs, or environmental impacts (Figure 1-2). For instance, Li-ion batteries, renowned for their high-density energy storage, are not sustainable for long-term usage and have significant environmental consequences. Supercapacitors offer fast charge and discharge times but may lack the same energy storage capacity as Li-ion batteries. Pumped hydro storage, another method, involves converting gravitational energy to electrical energy but suffers from inefficiencies. This is partly because energy from these sources needs to be transduced into other forms, resulting in efficiency losses.

To summarize, existing energy storage approaches tend to be impractical due to their associated environmental impact, among other issues, including lack of scalability, especially in areas far from large grids - this may signal a bigger problem if sustainable technology ever becomes mainstream. Hence, there is a pressing need for innovative energy storage solutions to address these challenges and maximize the accessibility and efficiency of renewable energy. In this thesis, we propose a new decentralized approach to storing electrical energy from renewable sources, which involves storing large amounts of energy electrostatically at high voltages on rolled polymer-based capacitors.



Figure 1-1: Solar Power Duck Curve [2]



Figure 1-2: Challenges in Implementing Renewable Energy Sources (Reproduced from [3])

1.2 Research Objectives and Scope

Our research focuses on developing a more sustainable, cheap, and easily deployable storage system for renewable sources. By utilizing polymer components and roll-to-roll processing techniques, we aim to create a large-scale capacitor energy storage device with a competitive cost point per kWh of energy, integrated into a rollable flexible hybrid electronics (FHE) package that enhances practicality and enables power management electronics embedding, Figure 1-3.

Our approach involves employing a multivariate optimization strategy, which includes modifying the surface area, utilizing high voltage storage (~10 kV) via transformer and convertors, and incorporating a high dielectric constant polymer material to achieve high energy density. To increase the surface area, we implement a technique of rolling the interleaved capacitors. We prioritize flexibility and thinness in the dielectric material selection, ensuring compatibility with the rolling process.; thus, a flexible polymer like PVDF is an ideal candidate for this approach.

While rolling an interleaved capacitor is a well-established method to increase capacitance, we explore the introduction of trenches in the rolled structure as a means to further enhance capacitance and energy density. However, it is important to note that introducing trenches can also elevate electric fields, potentially leading to dielectric breakdown of the material. Hence, the focus of this thesis is to validate, via simulation, the effectiveness of the proposed structural modifications and determine if they provide superior performance. By analyzing the simulation results, we will assess the impact of these structural changes on capacitance, energy density, and electric field. This investigation will provide valuable insights into the potential benefits and limitations of trench-based configurations compared to traditional parallel plate setups.



Figure 1-3: Schematic Illustration of Our Approach for High Energy Density Capacitor-Based Energy Storage System

CHAPTER 2: BACKGROUND

2.1 Capacitor Fundamentals and Performance Metrics

A capacitor is a passive electronic component that stores electrical energy as charge in an electric field between two conductive plates/electrodes. The stored energy can be released quickly, making capacitors ideal for applications requiring high power output. However, capacitors have a relatively low energy storage capacity compared to other energy storage devices.

Traditional capacitors consist of two conductive electrodes separated by an insulating layer known as a dielectric. When a voltage is applied, charge accumulates on the surfaces of the electrodes, creating an electric field that allows the capacitor to store energy. The amount of charge a capacitor can hold is proportional to the applied voltage and the capacitance of the device. Capacitance is defined as the ratio of the charge stored on each electrode to the applied voltage and is measured in farads (F). Capacitance can be calculated using the equation:

$$=\frac{\mathbf{Q}}{\mathbf{V}}$$

(2.1.1)

where C is capacitance, Q is charge, and V is voltage. The voltage can further be defined as the integral of the electric field (E) with respect to spacing (d) between the plates. When a dielectric with permittivity ε and thickness d is introduced between the two parallel plates with surface area A, the capacitance can be defined as:

С

$$V = -\int_0^d E \, dx = \iint_0^d \frac{\rho}{\epsilon} \, dx = \int_0^d \frac{Q}{\epsilon} \, dx = \frac{Qd}{\epsilon A} \Rightarrow \mathbf{C} = \frac{\epsilon A}{d}$$
(2.1.1)

As seen in the equation and Figure 2-1, the capacitance of a capacitor depends on the physical characteristics of the device, such as the surface area of the plates, the distance between the

electrodes, and the properties of the dielectric material. To increase capacitance, one can use a dielectric material with a high permittivity or dielectric constant, or reduce the distance between the electrodes, or use an electrode material with a high surface area, which will be explained in detail in the next section.

The performance of a capacitor-based energy storage device is characterized by two primary values: specific capacitance and energy density. Energy density, also known as specific energy, is the amount of energy stored per unit mass, but in our case, since the device would be stored in one place, we are not interested in energy per unit mass; instead, it is energy per unit volume. The energy stored in a capacitor is given by the equation $\mathbf{E} = 0.5^{\circ} \mathbf{C}^{\circ} \mathbf{V}^{2}$, where E is energy and C and V are capacitance and voltage, respectively.

Conventional capacitors have the advantage of fast charging and discharging capabilities but are limited in their energy storage capacity compared to batteries and fuel cells. However, there are several ways to enhance the energy storage capabilities of capacitors, as detailed in the following section.



Figure 2-1: Schematic of an Electrostatic Capacitor

2.2 Enhancing Energy Density of a Capacitor

The energy density of a capacitor is influenced by capacitance and voltage. Increasing voltage is a crucial factor in enhancing energy density, as the relationship between energy and voltage is quadratic. Our approach focuses on storing charge at significantly high voltages (~10 kV), leading to a substantial increase in energy density. Higher voltage levels enable a larger amount of charge to be stored within the same physical dimensions. However, safety considerations and proper insulation are essential to prevent electrical breakdown and maintain capacitor integrity.

In addition to voltage, capacitance can be increased to enhance energy density. One approach is exploring advanced materials with higher dielectric constants (Eqn. 2.1.2). Dielectric materials, located between the capacitor's electrodes, store electrical energy. By utilizing materials with higher dielectric constants, more energy can be stored per unit volume, thus boosting energy density. Optimizing the capacitor's design and structure is another avenue for improving energy density. Increasing the effective surface area of the electrodes within a given volume allows for more energy storage (Eqn. 2.1.2). By combining these approaches, we aim to develop capacitors with higher energy density, paving the way for more efficient energy storage solutions.

2.2.1 Dielectric Material Selection – PVDF (Polyvinylidene Fluoride)

In our pursuit of a cost-effective and scalable capacitor-based energy storage system, the selection of dielectric materials plays a pivotal role. Among various options, polymeric materials have emerged as a superior choice over ceramics due to their advantageous properties and practical benefits. In particular, polymers offer compelling advantages in terms of cost, roll-to-roll processing compatibility, and easy handling, making them an ideal candidate for our approach.

Among the various polymeric dielectric materials, Polyvinylidene Fluoride (PVDF) stands out as a particularly promising candidate, as shown in Table 2-1 [4] – [15]. PVDF possesses a high dielectric constant of 10.2 [11], making it an excellent choice for storing large amounts of electrical energy within a given volume. Furthermore, PVDF exhibits a higher breakdown strength of 720 V/μ m [9], indicating its ability to withstand higher electric fields without experiencing a dielectric breakdown. By strategically selecting PVDF as the dielectric material, we can leverage its desirable properties to maximize energy density in our capacitor design and simultaneously achieve cost-effectiveness and simplify the processing involved.

Table 2-1: DC breakdown Strength and Dielectric Constant of Flexible Substrates for High-Voltage Capacitor

Electrical Properties	DC Breakdown Strength (V/µm)	Dielectric Constant
PVDF (Polyvinylidene Fluoride)	590 ^[4] , 720-770 ^[9]	10.2 ^[11] 8.4 (60Hz) ^[12] 7.7 (1kHz) ^[12] 6.4 (1MHz) ^[12]
HDPE (High-Density Polyethylene)	600 ^[8]	2.30-2.35 (1MHz) ^[13]
LDPE (Low-Density Polyethylene)	650 ^[5]	2.25-2.35 (1MHz) ^[13]
PC (Polycarbonate)	528 ^[5] , 720 ^[9]	2.8 (1MHz) ^[14]
PET (Polyethylene Terephthalate)	570 ^[4] , 420-460 ^[7] (660-750) ^[7]	3.25 (1kHz) ^[14] 3 (1 MHz) ^[14] 2.8 (1 GHz) ^[14]
PI (Polyimide)	470 ^[9] , 600-650 ^[10]	3.6 (100 Hz) ^[9] 3.4 (1kHz) ^[15] 3.3 (1MHz) ^[15] 3.2 (1GHz) ^[15]
PP (Polypropylene)	640 ^[4] , 730 ^[9] , 500-800 ^[10]	2.2-2.6 (1MHz) ^[14]
PS (polystyrene)	600 ^[5] , 450 ^[9]	2.4-2.7 (1MHz) ^[14]
PTFE (polytetrafluoroethylene)	$\begin{array}{c} 600\text{-}700^{[4]},\\ 400\text{-}800^{[10]} \end{array}$	2.1 (1kHz & 1MHz) ^[13]
SU-8	440 ^[4] , 400 ^[6]	3.28 (1GHz) ^[6]

2.2.2 Surface Area Enhancement Techniques

To further enhance the energy density of capacitors, maximizing the effective area of the plates or electrodes is a crucial consideration. There are two approaches that can be employed to achieve this:

1. Rolled Interleaved Capacitors: Rolling the interleaved capacitors is a well-established method for increasing capacitance [16]. When a parallel plate capacitor is rolled up, the outer faces of the plates come into contact, forming a second capacitor in parallel with the inner plates. This effectively utilizes previously unused plate surfaces, resulting in a higher overall capacitance, shown in Figure 2-2. The rolling process not only increases the charge storage capacity but also helps reduce parasitic capacitance, which is the unwanted capacitance between the conductive plates and the surrounding environment. By isolating the conductive plates from the environment, the rolled capacitor achieves improved efficiency and performance.



Figure 2-2: Capacitance Enhancement Through Rolling Interleaved Capacitor

2. Introduction of Trenches: This approach offers the potential to further increase capacitance [17], as depicted in the accompanying Figure 2-3, showcasing the enhanced capacitance resulting from the presence of trenches. A key question arises: can the introduction of trenches yield a higher capacitance beyond the gains achieved through rolling? While trenches have the potential to enhance capacitance, it is crucial to consider the impact of increased electric field concentration, which may lead to dielectric breakdown. Therefore, the objective of this thesis, as discussed earlier, is to validate the benefits of introducing trenches and identify the optimal configuration that maximizes capacitance enhancement without compromising the overall performance and reliability of the capacitor.



Figure 2-3: Capacitance Enhancement Through Introduction of Trenches

This segues into our research methodology, where we employ simulation techniques to validate the effectiveness of introducing trenches in enhancing capacitance. Through the use of advanced simulation tools, such as ANSYS Maxwell, we will accurately model the capacitor's geometry and apply the appropriate equations to simulate its behavior. Our simulation process will involve systematically varying the parameters related to the trenches, such as their number, depth, radius, spacing, and arrangement, while keeping other factors, like dielectric thickness, constant. By analyzing the simulation results, we will quantitatively assess the impact of these trench configurations on the capacitance enhancement. The simulation enables us to explore a wide range of design possibilities quickly and cost-effectively, providing valuable insights into the optimal trench configuration for maximizing capacitance without compromising the capacitor's integrity. Additionally, simulation allows us to evaluate the electric field distribution within the capacitor, helping us identify if such a modification is beneficial or not.

2.3 Introduction to Finite Element Modeling and ANSYS Maxwell

Before we dive deep into the simulation process flow, it is crucial to establish a solid understanding of the underlying modeling concept. Finite element modeling, a widely employed numerical technique in engineering and science, forms the basis of our simulation methodology. It is a powerful approach that enables the solution of complex problems by breaking them down into smaller, more manageable elements. This technique involves discretizing the problem domain into finite elements, which can be simple shapes like triangles or tetrahedrons. By applying the principles of mathematical analysis, such as finite element analysis (FEA), to these elements, we can obtain numerical solutions that approximate the behavior of the real system.

In our case, ANSYS Maxwell serves as the software tool of choice for implementing finite element modeling. It is a high-performance software package specifically designed for electromagnetic field analysis. It leverages the power of finite element analysis to solve a wide range of electromagnetic problems, encompassing phenomena such as magnetic fields, electric fields, and electromagnetic radiation. Through Maxwell, we can define the geometry, material properties, and boundary conditions of our model. The software then divides the model into finite elements and applies Maxwell's equations, which describe the fundamental principles of electromagnetism, to obtain a numerical solution. This process allows us to simulate and analyze the electric fields with a high degree of accuracy and reliability, which is a crucial parameter in our case. The appropriate set of equations [18] and their terms are used based on the solver ("Electrostatic" solution type needed for our studies) selected.

$$\nabla \times \boldsymbol{H} = \boldsymbol{J} + \frac{\partial \mathbf{D}}{\partial t}$$
(2.1.1)

 $\nabla \cdot \boldsymbol{B} = 0$

(3.1.2)

$$\nabla \times \boldsymbol{E} = -\frac{\partial \boldsymbol{B}}{\partial t}$$
(3.1.3)

$$\nabla \cdot \boldsymbol{D} = \rho \tag{3.1.4}$$

By comprehending the foundational concept of finite element modeling and its application within ANSYS Maxwell, we establish a solid groundwork for delving into the subsequent stages of our simulation process flow.

CHAPTER 3: RESEARCH METHODOLOGY - SIMULATION

3.1 ANSYS Maxwell – Simulation Process Flow

For the capacitor design and simulation, ANSYS Maxwell was used. Figure 3-1 shows the process flow involved in an ANSYS Maxwell environment, which consists of three key components: Pre-Processing, Solver, and Post-Processing. Each component plays a crucial role in accurately simulating and analyzing the behavior of the designed capacitor structure (unit cell):



Figure 3-1: Simulation Process Flow in ANSYS Maxwell

 Pre-Processing: This initial phase involves creating the basic geometry of the unit cell structure. The geometry creation includes defining the dimensions and shape of the capacitor, as well as any additional features such as trenches or other modifications. The mesh properties are also set up, determining the level of detail and accuracy required for the simulation. Additionally, design variables are parameterized to allow for easy modifications and adaptation to different scenarios. The solution setup is controlled during pre-processing, where parameters such as refinement per pass and convergence criteria are adjusted to ensure accurate results.

- 2. Solver: For our analysis, an "electrostatic" solver is used as the current is very small in our energy storage system. The solver component of ANSYS Maxwell applies the Maxwell equations to the 3D geometry defined in the pre-processing phase. These equations describe the behavior of electromagnetic fields within the structure. By solving these equations numerically, the solver calculates the electric field distribution, charge distribution, and other relevant output parameters. The solver component is responsible for accurately simulating the behavior of the unit cell structure under different voltage and geometry conditions.
- 3. Post-Processing: Once the solver completes the simulation, the post-processing phase begins. The output obtained from the solver, such as the capacitance of the structure, is received and analyzed. This data is used to generate plots and graphs to visualize the behavior of the capacitor and its performance characteristics. Additionally, post-processing allows for the generation of field overlays, which display the electric field distribution within the structure. These overlays provide valuable insights into the behavior of the electric field and help identify areas of potential breakdown or high electric field concentration.

By following this simulation process flow in ANSYS Maxwell, we can effectively analyze the capacitance and performance of the unit cell capacitor structure. This enables us to validate the effectiveness of the proposed modifications and gain valuable insights into the energy density enhancement achieved through the introduction of trenches and other design optimizations.

3.2 Simulation Model Validation via Analytical Calculations

To ensure the accuracy and reliability of our proposed energy storage model based on a trenched capacitor configuration, thorough model validation is essential. This validation process involves comparing the analytical calculations of capacitance for a simplified test model with the model's predicted results. The test model, depicted in Figure 3-2, is deliberately designed with rectangular trenches instead of cylindrical ones to facilitate easy analytical calculations. The test model consists of top and bottom plates measuring 40 x 40 μ m, with rectangular trenches of 60 μ m depth embedded within a 100 μ m thick dielectric material, PVDF. By conducting this validation, we can assess the performance of the model, verify its effectiveness in accurately calculating capacitance, and address any potential issues that may arise.



Figure 3-2: Schematic of Simplified Test Model

To determine the capacitance value, we consider the dimensions and dielectric properties (PVDF's dielectric constant = 10.2) of the unit cell, employing the parallel-plate capacitor formula (Eqn. 2.1.2). In our calculations, we make several assumptions and divide the entire structure into smaller parallel plates denoted as C_1 , C_2 , C_3 , and C_4 . Calculating C_2 is somewhat complex due to internal fringing effects. To address this, we assume an effective fringing length of 40 μ m. Since all the capacitances are in parallel, we sum them to obtain the total capacitance, as shown below.

Analytical Calculations:

$$C_{1} = \frac{A_{1}\varepsilon_{0}\varepsilon}{d} = \frac{(10 * 40) * 8.85 * 10^{-18} * 10.2}{40} = 9.03 \times 10^{-16} \text{ F}$$

$$C_{2} = \frac{A_{2}\varepsilon_{0}\varepsilon}{d} = \frac{(40 * 40) * 8.85 * 10^{-18} * 10.2}{20} = 7.22 \times 10^{-15} \text{ F}$$

$$C_{3} = \frac{A_{3}\varepsilon_{0}\varepsilon}{d} = \frac{(20 * 40) * 8.85 * 10^{-18} * 10.2}{100} = 7.22 \times 10^{-16} \text{ F}$$

$$C_{T} = 2C_{1} + C_{2} + C_{3} = 9.80 \times 10^{-15} \text{ F}$$

Simulation $C_{sim} = 9.88 \times 10^{-15} F$

Upon comparing the calculated capacitance (9.80 x 10^{-15} F) with the model's predicted capacitance (9.88 x 10^{-15} F), we find a close agreement between the two values. The minor discrepancy observed can be attributed to the assumption made for the effective depth of fringing effects. If we consider a fringing length greater than 40 μ m, the calculated capacitance value would perfectly align with the simulated value, showing that the simulation model works perfectly. In summary, the thorough model validation process confirms the performance and accuracy of our simulation model setup.

3.3 Capacitor Models and Associated Design Parameters

In order to maintain consistency and comparability among the different capacitor models, a set of design variables was defined. These design variables are integral to the construction and characterization of the models. Additionally, the thickness of the dielectric was standardized at 100 µm. The design variables used across the models are as follows:

- Unit Cell Length and Breadth (a): The dimensions of the unit cell, representing the fundamental repeating structure, are denoted by "a." Both the length and breadth of the unit cell are equal.
- 2. Trench Depth (td): The depth of the trenches within the dielectric is denoted by "td." This parameter determines the extent to which the trenches penetrate into the dielectric.
- Trench Radius (r): For models featuring cylindrical trenches, the radius of the trenches is denoted by "r."
- 4. Trench Width (tw): In the case of models incorporating rectangular trenches, the width of the trenches is denoted by "tw." This parameter specifies the dimension of the rectangular trenches along the length of the unit cell.
- 5. Ring radius (Rr): Specifies the radius of the rings, denoted by "Rr," that form the corrugations on the trench surfaces.

Below is a table illustrating the schematics of the unit cell for each capacitor configuration, along with their associated design parameters:



Table 3-1: Capacitor Designs and Associated Design Parameters





Now that we have defined and illustrated all the capacitor configurations, the next chapter will delve into the results obtained from each of these configurations. The following chapter will provide a comprehensive analysis, comparison, and evaluation of the performance of each capacitor model based on various parameters such as specific capacitance, energy density, and electric field distribution.

CHAPTER 4: RESULTS AND DISCUSSION

4.1 Model Optimization – Models 1, 2, and 3

Models 1 (Extended Trench), 2 (Corner Quarter Top Trench), and 3 (Corrugated Trench) were optimized by manipulating key design parameters such as trench depth and unit cell length/breadth parameter "a". The dielectric properties of the PVDF material were obtained from literature, i.e., a dielectric constant of 10.2 [11] and a conductivity of 0.66 x 10^{-12} S/m [19], respectively. The film thickness was fixed at 100 µm, and the trench radius "r" at 10 µm. Initially, the optimization process focused on Model 1, where the pitch "a" was varied from 30 to 200 µm and the trench depth "td" from 20 to 45 µm. Subsequently, the maximum electric field, specific capacitance, and energy density were evaluated and illustrated in Figure 4-1.

Generally, an increase in pitch leads to a decrease in the maximum electric field, specific capacitance, and energy density. This optimization process also served as a means to verify that the simulated models aligned with this expected behavior. To ensure the maximum electric field of the structure remained below the PVDF's DC breakdown strength of 720 V/µm [9], a careful selection of pitch and depth ranges was performed. The electric field values were required to remain below the designated threshold, with an added safety margin of 300 V/µm. The "Acceptable" Emax values in Figure 4-1 (a) represent the region where the chosen pitch and depth combinations met the safety criteria. From this acceptable region, the best-case scenario was selected for the model, presenting an optimal combination of electric field and energy density. The results of the optimization process, including the best-case pitch and depth value, along with the corresponding electric field and energy density, are tabulated in the accompanying table.



Figure 4-1: Effect of Pitch and Trench Depth on (a) Maximum Electric Field, (b) Specific Capacitance, and (c) Energy Density in Model 1

A similar optimization process was conducted for Model 2 (Corner Quarter Top Trench) with a specific focus on lower trench depth (td) values ranging from 20 to 35 μ m. This narrower range was chosen to ensure that the maximum electric field (E_{max}) remained within the designated safety margin, similar to the optimization approach followed for Model 1. Subsequently, the best-case configuration was selected based on the desired energy density.

Moving on to Model 3, it can be regarded as an extension of Model 2, where corrugations were introduced to the trenches. The underlying idea was to increase the surface area, thereby enhancing the capacitance while keeping the trench depth unchanged [20]. The aim was to maintain the same electric field as that of Model 2. Consequently, considering this similarity in behavior, the best-case configuration determined for Model 2 can be naturally utilized for Model 3 as well. These optimized configurations for Models 2 and 3 are presented in Table 4-1, where the chosen parameters are tabulated.

Capacitor Configuration	Optimized Case (Unit Cell Parameters)
Model 1 ((Extended Trench)	$a=30~\mu m,tw=10~\mu m,td=25~\mu m$
Model 2 (Corner Quarter Top Trench)	$a=30~\mu\text{m},r=10~\mu\text{m},td=25~\mu\text{m}$
Model 3 (Corrugated Trench)	$a = 30 \ \mu m, r = 10 \ \mu m, td = 25 \ \mu m$

Table 4-1: Optimized Configurations for Models 1, 2, and 3

4.2 Comparison of Models 1, 2, and 3 with Parallel Plate Design

Table 4-2 provides a performance comparison of Models 1, 2, 3, and the Parallel Plate configuration in terms of maximum electric field (E_{max}) and specific capacitance (Specific C). The maximum electric field represents the highest electric field value achieved in each model, measured in volts per meter (V/m). The specific capacitance denotes the capacitance per unit area, expressed in farads per square micrometer (F/ μ m²).

 Table 4-2: Performance Comparison of Optimized Models 1, 2, 3, and Parallel Plate Configuration in Terms of Electric Field (E_{max}) and Specific Capacitance (Specific C)



Despite the initial appearance of higher capacitance in each trenched structure compared to the parallel plate configuration, a closer examination reveals that all the models ultimately perform poorly when considering the impact of electric field effects:

1. Model 1 vs. Parallel Plate:

Model 1 Maximum Electric Field (E_{max}): 3.0 x 10⁸ V/m

Equivalent Parallel Plate (PP) thickness at the same E_{max} : 33.3 μm

Parallel Plate Specific Capacitance for 33.3 μ m depth: 2.71 x 10⁻¹⁸ F/ μ m²

Model 1 Specific Cap. (1.65 x 10^{-18} F/ μ m²) < PP Specific Cap. (2.71 x 10^{-18} F/ μ m²)

2. Model 2 vs. Parallel Plate:

Model 2 Maximum Electric Field (E_{max}): 3.62 x 10⁸ V/m

Equivalent Parallel Plate (PP) thickness at the same E_{max} : 27.7 μm

Parallel Plate Specific Capacitance for 27.7 μ m depth: 2.36 x 10⁻¹⁸ F/ μ m²

Model 2 Specific Cap. (1.57 x 10^{-18} F/ μ m²) < PP Specific Cap. (3.26 x 10^{-18} F/ μ m²)

3. Model 3 vs. Parallel Plate:

Model 3 Maximum Electric Field (Emax): 3.70 x 10⁸ V/m

Equivalent Parallel Plate (PP) thickness at the same E_{max} : 27 μm

Parallel Plate Specific Capacitance for 27 μ m depth: 2.36 x 10⁻¹⁸ F/ μ m²

Model 3 Specific Cap. (1.58 x 10^{-18} F/ μ m²) < PP Specific Cap. (3.34 x 10^{-18} F/ μ m²)

From the above comparison, it is evident that the Parallel Plate Configuration outperforms all the models in terms of specific capacitance. These findings emphasize the trade-off between electric field and specific capacitance in the design of energy storage systems. While the trench-based models may offer advantages such as increased surface area and enhanced capacitance, also exhibit

higher electric fields between the trenches, thus, ultimately performing worse than a traditional parallel plate design.

4.3 Comparison of Model 4 with Parallel Plate Design

Due to the underwhelming capacitance values of the trenched design, we tried an entirely new approach, Model 4: the Square Bipolar Electrode Array, to achieve better results. This design features square electrodes with opposite polarity positioned adjacent to each other and on opposite sides in a 400 x 400 μ m unit cell, with a separation distance of 100 μ m as exceeding it would result in a reduction of capacitance, contrary to our intended goal. The fundamental idea underlying this design is to foster parallel plate interactions both horizontally (C₁) and vertically (C₂). Additionally, two such designs are stacked to simulate internal fringing effects, which is anticipated to significantly contribute to enhancing the overall capacitance. The expected outcome of these design elements working in tandem is an increased capacitance, visually depicted in Figure 4-2.



+10 kV Electrode
 Grounded Electrode

Figure 4-2: Schematic Representation of the Square Bipolar Electrode Array Design, Illustrating the Parallel Plate Interactions and Stacking

To validate the performance of this design, a comparison was made against an equivalent interleaved parallel plate capacitor with a plate area of 400 x 400 μ m. This parallel plate capacitance was calculated using the capacitor formula and tabulated in the accompanying table. Since we assumed an equivalent plate area, a direct comparison of capacitance values can be made instead of using specific capacitance.

 Model
 Parallel Plate
 Model 4

 E_{max}
 1.0 x 10⁸ V/m
 8.32 x 10⁹ V/m

 Capacitance
 2.89 x 10⁻¹³ F
 1.45 x 10⁻¹³ F

Table 4-3: Performance Comparison of the Square Bipolar Electrode Array Design with the Parallel Plate

As indicated in Table 4-3, the electrode design exhibits relatively lower performance. One possible reason for this outcome could be the reduced electrode area in comparison to a parallel plate configuration, resulting in a lower capacitance value. Furthermore, another contributing factor to the electrode design's suboptimal performance is the presence of sharp corners on the electrodes. These sharp corners can lead to a concentration of the electric field, resulting in higher electric field values. This higher electric field can negatively impact the overall performance and efficiency of the design, as seen earlier. Therefore, even the electrode design does not perform better than the parallel plate design.

4.4 Comparison of Model 5 with Parallel Plate Design

The last design we tried is Model 5, i.e., the Deep Trench Model. This design draws inspiration from the concept of Deep Trench Capacitors (DTC) employed in semiconductor devices. DTCs are recognized for their ability to augment the capacitive area while retaining the

component's existing footprint, aligning closely with our objectives. Conventionally, DTCs are fabricated through an intricate process involving multiple lithographic and etching steps, which can be costly due to the number of masks used. However, our approach (Figure 4-3) introduces an alternative method: employing a planar capacitor with trenches stamped using a mold, as depicted in the accompanying figure. This approach offers a potentially more efficient and cost-effective means of achieving the desired outcome.



Figure 4-3: Schematic Illustration of an Inexpensive Approach to Formation of Deep Trenches Via Molding

The Deep Trench Model offers a significant advantage over the previous trench designs. Since the trenches are embedded into the substrate and not the dielectric, the dielectric thickness remains the same (100 μ m); as a result, concerns regarding electric field concentration are mitigated in this case. In stark contrast to previous trenched designs, where trench depth was constrained by the dielectric thickness, the deep trench model offers the unprecedented ability to customize trench depth —restricted only by fabrication constraints and rolling of capacitors, due to which we will fix the trench depth to 3 times the radius, i.e., 750 μ m.

The simulated model consisted of 50 μ m metal plates with a 100 μ m dielectric layer sandwiched between them. The radius was fixed at 250 μ m with the unit cell length 'a' as 750 μ m or (3r). Table 4-4 shows the electric field comparison between the Parallel Plate and Model 5, revealing a minor difference. However, it is important to consider that this disparity could also be attributed to the meshing size utilized in the simulations.



Table 4-4: Electric Field Comparison of Parallel Plate and Model 5

When examining the surface area metrics, we observe the following values:

- Actual Area (AA): $3.23 \times 10^6 \,\mu\text{m}^2$
- Projected Area (PA): $5.63 \times 10^5 \mu m^2$

Calculating the Capacitive Area Increase as AA/PA, we find a ratio of 5.74. This highlights the substantial increase in capacitance achieved by the Deep Trench Model, reinforcing its better performance over the parallel plate design.

CHAPTER 5: CONCLUSION AND PERSPECTIVE

Capacitor Configuration	Specific Capacitance (F/µm ²)
Parallel Plate	0.9 x 10 ⁻¹⁸
Model 1 ((Extended Trench)	1.65 x 10 ⁻¹⁸
Model 2 (Corner Quarter Top Trench)	1.57 x 10 ⁻¹⁸
Model 3 (Corrugated Trench)	1.58 x 10 ⁻¹⁸
Model 4 (Square Bipolar Electrode Array)	0.45 x 10 ⁻¹⁸
Model 5 (Deep Trench Model)	$1.80 \ge 10^{-18}$

Table 5-1: Specific Capacitance Values for Different Capacitor Structures

In this thesis, we investigated and compared multiple capacitor models, including Model 1 (Extended Trench), Model 2 (Corner Quarter Top Trench), Model 3 (Corrugated Trench), Model 4 (Square Bipolar Electrode Array), and Model 5 (Deep Trench Model), against the traditional Parallel Plate configuration. The objective was to assess the impact of structural modifications (such as trenches) on increasing the capacitive surface area and ultimately improving energy density.

Through optimization, the best configuration for each model was determined and subsequently evaluated against the parallel plate design in terms of specific capacitance and electric field. While initially showing higher capacitance values compared to the parallel plate, a closer examination revealed that the specific capacitance of all the trenched models was actually lower if we account for the increased electric field. This trade-off between electric field and specific capacitance highlighted the limitations of the trenched designs when considering their overall performance. However, the Deep Trench Model stood out by demonstrating improved performance. It managed to increase the capacitive area by 5.7 times that of the parallel plate while maintaining a lower electric field, suggesting that it could serve as a promising capacitor design for achieving enhanced capacitance in energy storage systems.

Overall, this thesis offers valuable insights into the design considerations for capacitor models, showcasing the immense potential of the Deep Trench Model as a practical solution. By enhancing energy density, this model positions high-density capacitors as promising candidates for sustainable and cost-effective energy storage systems.

REFERENCES

[1] "Renewables 2019: Market analysis and forecast from 2019 to 2024," IEA (International Energy Agency), https://www.iea.org/reports/renewables- 2019 (Accessed Feb 2023).

 [2] S Poulter, "The Duck Curve and How Energy Storage Can Beat It", Pacific Green Group, https://www.pacificgreen.com/articles/duck-curve-and-how-energy-storage-can-beat-it/ (Accessed April 2023).

[3] A Robb, "Balancing a Renewable Grid: What are the options", Power Grid International, https://www.power-grid.com/executive-insight/balancing-a-renewable-grid-what-are-the-options-2/ (Accessed April 2023).

[4] G. Shimoga and S.-Y. Kim, "High-k Polymer Nanocomposite Materials for Technological Applications," *Appl. Sci.*, vol. 10, 4249, 2020.

[5] M. Ieda, "Dielectric Breakdown Process of Polymers," *IEEE Transactions on Electrical Insulation*, vol. EI-15, pp. 209-224, 1980.

[6] M.-T. Hong, S. J. Moon, J. M. Lee and B. S. Bae, E.-J. Yun, M. Harnois, E. Jacques, and T. M.-Brahim, "The Effect of Bake Temperature on SU-8 Gate Insulator of IGZO Thin Film Transistor," *Journal of the Korean Physical Society*, Vol. 73, pp. 297~301, 2018.

[7] S. J. Laihonen, U. Gafvert, T. Schiitte, U. W. Gedde, "Influence of Electrode Area on Dielectric Breakdown Strength of Thin Poly (Ethene Terephthalate) Films," *Proceedings of 2004 Annual Report Conference on Electrical Insulation and Dielectric Phenomena*, pp. 563-567, 2004.

[8] M. M. Ueki and M. Zanin, "Influence of Titanium Dioxide and Carbon Black on the High-Density Polyethylene," *Proceedings of 1997 IEEE Annual Report - Conference on Electrical Insulation and Dielectric Phenomena, Minneapolis*, pp. 173-176, 1997.

[9] T. R. Jaw and P. J. Cygan, "Dielectric Breakdown of Polyvinylidene Fluoride and Its Comparisons with Other Polymers," Journal of Applied Physics, vol. 73, pp. 5147-5151, 1993.

[10] D. Q. Tan, "Differentiation of Roughness and Surface Defect Impact on Dielectric Strength of Polymeric Thin Films," *IET Nanodielectrics (Short Communication)*, vol. 3, pp. 28-31, 2020.

[11] Q. G. Chi, L. Gao, X. Wang, Y. Chen, J. F. Dong, Y. Cui, and Q. Q. Lei, "Effects of Magnetic Field Treatment on Dielectric Properties of CCTO@Ni/PVDF Composite with Low Concentration of Ceramic Fillers," *AIP Advances*, vol. 5, 117103, 2015.

[12] "PVDF Resin Property Table," in Japanese, KDA Corporation, https://www.kda1969.com/materials/pla_mate_pvdf2.htm (accessed Feb. 2023).

[13] D. E. Gray, B.H. Billings, "Properties of Dielectrics," in *American Institute of Physics Handbook, 3rd ed., New York: McGraw-Hill*, pp. 5-132, 1972.

[14] "Dielectric Constant of Selected Polymers," hbcp.chemnetbase.com, https://hbcp.chemnetbase.com/faces/documents/13 04/13 04 0001.xhtml (Accessed Sept. 2022).

[15] S. Chisca, I. Sava, V. -E. Musteata and M. Bruma, "Dielectric and Conduction Properties of Polyimide Films," *CAS 2011 Proceedings (2011 International Semiconductor Conference), Sinaia, Romania*, pp. 253-256, 2011.

[16] S K Foong and C H Lim, "On the Capacitance of a Rolled Capacitor," *Phys. Educ.*, pp. 37-429, 2002.

[17] C. Gonzalez and J. P. McVittie, "A Study of Trenched Capacitor Structures," in *IEEE Electron Device Letters*, vol. 6, no. 5, pp. 215-218, 1985.

[18] "ANSYS Maxwell Getting Started," ANSYS Inc, 2020, https://courses.ansys.com/wpcontent/uploads/2021/07/MAXW GS 2020R2 EN LE01.pdf (Accessed Feb 2023).

[19] P. Dhatarwal and R. J. Sengwa, "Polymer Compositional Ratio-Dependent Morphology, Crystallinity, Dielectric Dispersion, Structural Dynamics, and Electrical Conductivity of PVDF/PEO blend films, "*Macromol. Res.*, vol. 27, pp. 1009-1023, 2019. [20] F Toshiharu, H Mark, H Steven, M William, "Increased Capacitance Trench Capacitor (US
 Patent No. US-6620675-B2)," U.S. Patent and Trademark Office, https://app.dimensions.ai/details/patent/US-6620675-B2 (Accessed Feb 2023).