UNIVERSITY OF CALIFORNIA, SAN DIEGO

Design Considerations of Graphene FETs for RF Applications

A dissertation submitted in partial satisfaction of

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in

Electrical Engineering (Nanoscale Devices and Systems)

by

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2016

The dissertation of Kangmu Min Lee is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Dedication

This dissertation is dedicated to my family.

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Chapter 2 or portion thereof has been published in MRS Proceedings (2010 MRS Spring Meeting), May 2010, K. Lee, L. Wang, P. Asbeck and J. Moon, and in International Semiconductor Device Research Symposium (ISDRS), Dec. 2011, K. M. Lee, A. Ohoka, P.M. Asbeck. The dissertation author was the primary investigator and author of both papers.

Chapter 3, in full, is a reprint of the material as it appeared in *Solid State Electronics* 2014, K. Lee, J.S. Moon, T. Oh, S. Kim, P. Asbeck and P. M. Asbeck. The dissertation author was the primary investigator and author of this paper.

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Journal Publications

- P. M. Asbeck, **K. Lee** and J. Min, "Projected Performance of Heterostructure Tunneling FETs in Low Power Microwave and mm-Wave Applications," in IEEE Journal of the Electron Devices Society, vol. 3, no. 3, pp. 122-134, May 2015

- **K. Lee**, P. Asbeck, "Numerical study of inhomogeneity effects on Hall measurements of graphene films," Solid-State Electronics, Volume 106, April 2015, Pages 34-43, ISSN 0038-1101

- **K. Lee,** J.S. Moon, T. Oh, S. Kim, P. Asbeck, "Analysis of heat dissipation of epitaxial graphene devices on SiC," Solid-State Electronics, Volume 101, November 2014, Pages 44-49, ISSN 0038-1101

- S. Gu, H. Katayose, K. Nomoto, T. Nakamura, A. Ohoka, **K. Lee**, W. Lu and P. M. Asbeck, "High transconductance ion-implanted GaN MISFETs using atomic layer deposited high-k dielectrics," physica status solidi (c), Vol. 10, Issue 5, pages 820–823, May 2013

- J. S. Moon, H. -C. Seo, M. Antcliffe, D. Le, C. McGuire, A. Schmitz, L. O. Nyakiti, D. K. Gaskill, P. M. Campbell, **K.-M. Lee**, and P. Asbek, "Graphene FETs for Zero-Bias

Linear Resistive FET Mixers," IEEE Electron Device Letters, Vol. 34, No. 3, March 2013

- J.S. Moon, H.-C.Seo, M. Antcliffe, S. Lin, C. McGuire, C. D. Le, L.O. Nyakiti, D.K. Gaskill, P, M. Campbell, **K. -M. Lee**, P.Asbeck, "Graphene FET-Based Zero-Bias RF to Millimeter-Wave Detection," IEEE Electron Device Letters, Oct. 2012

- J.S. Moon, M. Antcliffe, H.C. Seo, D. Curtis, S. Lin, A. Schmitz, L. Milosavljevic, A. A. Kiselev, R. S. Ross, D. K. Gaskill, P. M. Campbell, R.C. Fitch, **K.-M. Lee**, P. Asbeck, "Ultra-low resistance ohmic contacts in graphene field effect transistor," Applied Physics Letters, May 2012

- J.S. Moon , M. Antcliffe, H.C. Seo, S.C. Lin, A. Schmitz, L. Milosavljevic, K. McCalla, D. Wong, D.K. Gaskill, P.M. Campbell, **K.-M. Lee**, P. Asbeck, "Graphene review: An emerging RF technology", Silicon Monolithic Integrated Circuits in RF Systems (SiRF), 2012 IEEE 12th Topical Meeting on, On page(s): 199 - 202

- J.S. Moon , M. Antcliffe, H.C. Seo, S.C. Lin, A. Schmitz, L. Milosavljevic, K. McCalla, D. Wong, D.K. Gaskill, P.M. Campbell, **K.-M. Lee**, P. Asbeck, "Graphene transistors for RF applications: Opportunities and challenges," in Int. Semiconductor Device Research Symposium (ISDRS), Dec. 2011

- J.S. Moon, D. Curtis, D. Zehnder, S. Kim, D. K. Gaskill, G.G. Jernigan, R.L. Myers-Ward, C.R. Eddy, P.M. Campbell, **K.M. Lee**, P. Asbeck, "Low-Phase-Noise Graphene FETs in Ambipolar RF Applications," IEEE Electron Device Letters, March 2011

- W Chen, W. V. Chen, **K Lee**, SS Lau and T. F. Kuech, "High Quality InP Layers Transferred by Cleavage Plane Assisted Ion-Cutting," Electrochem. Solid-State Lett.2010 volume 13, issue 8, H268-H270, May 2010

Conference Proceedings

- **K. Lee** and P. Asbeck, "Analysis of Heat Dissipation of Epitaxial Graphene Devices on SiC," in International Semiconductor Device Research Symposium (ISDRS), 2013

- J. S. Moon et al., "Graphene review: An emerging RF technology," Silicon Monolithic Integrated Circuits in RF Systems (SiRF), 2012 IEEE 12th Topical Meeting on, Santa Clara, CA, 2012, pp. 199-202.

- **K. M. Lee**, A. Ohoka, P.M. Asbeck, "Charge transfer region at the edge of metal

contacts on graphene and its impact on contact resistance measurement," in International Semiconductor Device Research Symposium (ISDRS), Dec. 2011, Nominated: Best Student Paper

- **K. Lee**, L. Wang, P. Asbeck and J. Moon, "Analysis of Resistance Asymmetry Due to p-n Junctions in Graphene FETs," in MRS Proceedings (2010 MRS Spring Meeting) / Vol.1259 / 2010

- P. Asbeck, **K. Lee** and J. Moon, "Graphene: Status and prospects as a microwave material," in IEEE 12th Annual Wireless and Microwave Technology Conference (WAMICON), April 2011

ABSTRACT OF THE DISSERTATION

Design Considerations of Graphene FETs for RF Applications

by

Kangmu Min Lee

Doctor of Philosophy in Electrical Engineering (Nanoscale Devices and Systems)

University of California, San Diego, 2016

Professor Peter Asbeck, Chair

This dissertation discusses various physical aspects of graphene electronic devices, particularly FETs, of importance for high frequency (RF, microwave and mm-wave) applications. Device physics of graphene junctions and contact junctions are considered. Inhomogeneity effects, heat dissipation and graphene FET compact modeling including unique nonlinearity mechanisms are discussed.

The first part of the dissertation discusses device physics of graphene. The importance of its unique band structure, high carrier mobilities, and maximum current handling are highlighted for RF applications. Graphene junctions are discussed in detail, including p-n junctions and graphene-to-metal junctions. It is shown that graphene p-n

junctions provide additional resistance at the transition region within representative FETs due to depletion of carriers, which results in asymmetric ambipolar Id-Vg curves. It is also shown that a charge transfer region is formed at metal-graphene edges, which produces errors in the customary contact resistance measurement and analysis. Both junction effects are controlled by carrier density of the film, fringe electric field, and bias conditions.

Inhomogeneous graphene films are modeled in detail to describe the formation of electron-hole puddles, and their impact on Hall mobility measurements. Inhomogeneity is more significant with larger amplitude of random charge fluctuation and the size of puddles. It is shown that measured Hall mobility can be degraded by more than 8 % due to inhomogeneity, compared with ideally uniform films with the same average carrier density.

Thermal properties of graphene FETs must also be understood in relation to their performance and reliability. Heat dissipation of graphene devices has been analyzed with 3-D thermal simulations. The significance of interface thermal resistance, device design for quick heat release, and contact metal use for lateral heat spreading is described. Simulation and experimental results showed that pulses as short as 200 ns can still heat up graphene devices due to their small heat capacity.

Finally, graphene device models are developed in two forms: a SPICE-like compact model for straightforward usage in circuit simulators, and a more abstract analytic model for investigation of the impact of device parameters on circuit performance. Both device models are used to explore the performance of graphene-

based FETs in zero bias r.f. power detector and resistive linear mixer applications. Parasitic elements such as parasitic capacitances, gate and series resistances are included for realistic circuit simulation, and the role of these components on the circuit performance is investigated. Graphene-based zero-biased power detectors showed sensitivity comparable to those using CMOS and InP HEMT-based technologies. Simulated noise equivalent power (NEP) was estimated to be as low as 10 pW/Hz0.5 for a passive r.f. power detector, thanks to the suppression of flicker noise. The mixer also exhibited linearity comparable to state-of-the-art, with input third-order intercept point (IIP3) estimated at about 22 dBm. Simulation results describe the experimental results well. The impact of different device design parameters are investigated by simulation in order to optimize performance.

Chapter 1

Introduction

Since the first experimental realization of graphene by Geim and Novoselov [1], the research activities on graphene have grown explosively over the last decade [2, 3]. Numerous researchers explored this novel material which has unique electrical [4, 5], photonic [6, 7], mechanical [8] characteristics. Graphene showed the highest room temperature mobility [4, 9, 10], for both holes and electrons. It is transparent, flexible, and has very high strength. Among many possible applications, r.f. applications could have a significant benefit from utilization of graphene [11].

Traditionally, better performance of FETs has been achieved by scaling down the gate length. In order to maintain the electrostatic channel control and to suppress short

channel effect, the vertical dimensions of the gate dielectric and channel should be scaled down as well [12]. The vertical scaling down has been a major challenge because it generates problems such as the degradation of mobility due to surface scattering, deterioration of electrostatic control over the channel, and gate leakages through the thin oxide layers. However, graphene is already an extremely scaled down channel layer – one atom thick. One can control the characteristics of graphene FET channel via electrical field modulation, forming both n- and p-channel and changing the polarity. Graphene also showed excellent room temperature mobility for both electrons and holes. Graphene FET already demonstrated high cutoff frequencies [13-17], thanks to its large carrier velocity and ability to stand high current flow. The large optical phonon energy of graphene also helps to reduce the scattering and maintain the high mobility of carriers [18-20]. The planar structure of the material enables to have compatible process with various technologies including CMOS. More over, graphene is transparent and flexible, which would be possible to serve as a platform of flexible electronic devices.

In this chapter, a brief overview is provided to review advantages of graphene for high frequency FETs, material preparation methods, and opportunities and challenges towards graphene based high speed microwave transistors. The objective of this thesis is then described, and the research results are summarized. The chapter ends with a brief description of the remaining chapters.

1.1. Graphene Structure and Electrical Properties

Graphene is a single atom thick sheet of carbon atoms hexagonally arranged to honeycomb structure (Figure 1.1). Physically it is equivalent to single layer detached from graphite single crystal. Interlayer bonding force is relatively weaker than intralayer bond, therefore it is possible to peel off graphene layers from the bulk graphite. Often the exfoliation results more than a single layer, which is known as bilayer, trilayer, and multi-layer graphene.

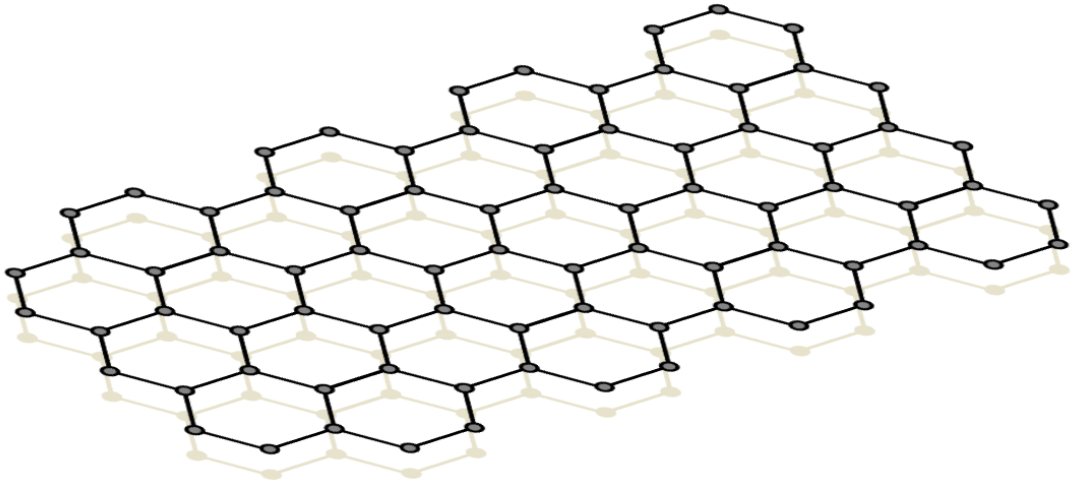


Figure 1.1. Atomic structure of graphene. Carbon atoms arranged two dimensionally in honeycomb structure

Within the layer, carbon atoms are tightly bonded with sp2 bonding, and additional electrons are forming orbital perpendicular to the plane which contributes to form conduction and valence bands [21]. Graphene has a unique E-k relation: $E=\hbar \cdot v_D \cdot k$, where v_D is the Dirac velocity $8 \cdot 10^7$ cm/s. As displayed in Figure 1.2, graphene energy

band forms a mirrored cone structure with zero bandgap. E_c and E_v meeting at the charge neutrality point, also known as the Dirac point. Fermi energy will reside at the Dirac point when the graphene is at intrinsic condition. Thermally activated finite minimum charge density is in the order of ~$1 \cdot 10^{11}$ cm^{-2} at room temperature. According to the linear E-k relation, the density of states of band reduces near at the Dirac point, and quickly increases as the Fermi energy pushed away from E_{Dirac}.

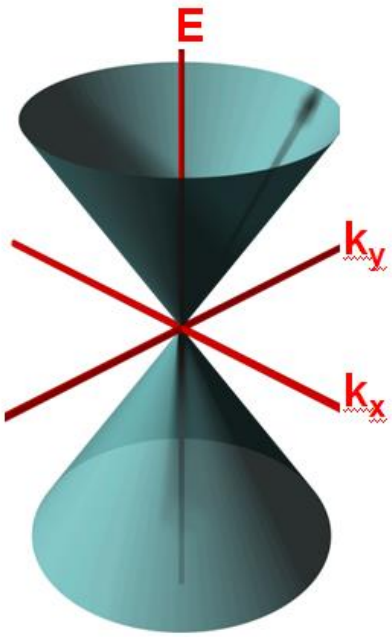


Figure 1.2. E-k dispersion relation of graphene forms a cone shape near Dirac point

Graphene's unique linear E-k dispersion also allows very high speed for both electrons and holes. Dirac velocity v_D is the maximum, however average velocity of carriers with field will be reduced in the presence of scattering induced by defects [22],

fixed charges [23, 24], acoustic [18] and optical phonons [18, 19]. Mobility of graphene carrier is affected by carrier density as well, where the intrinsic, minimum carrier density state will result maximum mobility [25]. The optical phonon energy of graphene is very high (180 meV) [20], because of graphenes light mass and strong bonds. Large optical phonon energy suppresses optical phonon scattering and enhances the carrier mobility. However, optical phonon scattering from gate dielectric limits the mobility of graphene channel of FETs. Therefore, highest mobility was measured from suspended graphene structures where graphene is standing alone without any interface with dielectric or substrate.

1.2. Material Preperation of Graphene

The first seperation of graphene layer was demonstrated by peeling off flakes from graphite crystal using Scotch tape [1]. Exfoliated flakes are mechanically transferred on to 300 nm-thick SiO_2 layer on Si substrate which is widely used, because the graphene flake is visible on this particular substrate, displayed in figure 1.3 (a) [1]. It is possible to distinguish the number of layers of the graphene flake with optical microscope. Since the method doesn't require high cost equipment, most of graphene devices were fabricated on exfoliated graphene flakes at the beginning of graphene research boom. Highest mobility of carriers of graphene was measured on suspended device of exfoliated graphene flake which is a single crystal and has an excelent uniformity of thickness withing short distance (~μm). However, despite its high quality, the exfoliated graphene has a critical weakness; lack of scalability.

Chemical vapor deposition (CVD) emerged as a popular method of graphene growth since the size of graphene film is only limited by the size of metal foil, which serves as a film growth surface. Carbon film is deposited on copper [26] or nickel [27] films, and C atoms arranges in honeycomb structure with grain boundaries. The size of graphene grain is affected by the size of the grain of metal foils, growth temperature. CVD film of graphene can be transferred to various substrates by wet-transfer [28], dry-transfer [29]. Large area of graphene (continuous roll of 10 inches width film) fabrication and transfer was demonstrated using thermal detach adhesion [30]. Since the CVD graphene often need to be transferred to target substrate, non-negligible probability of contamination exists during the process. Several electronic devices have been reported that used CVD graphene as channel material, however, large area graphene films showed it is more suitable for transparent, flexible electrode material when it is used as multi-layer graphene.

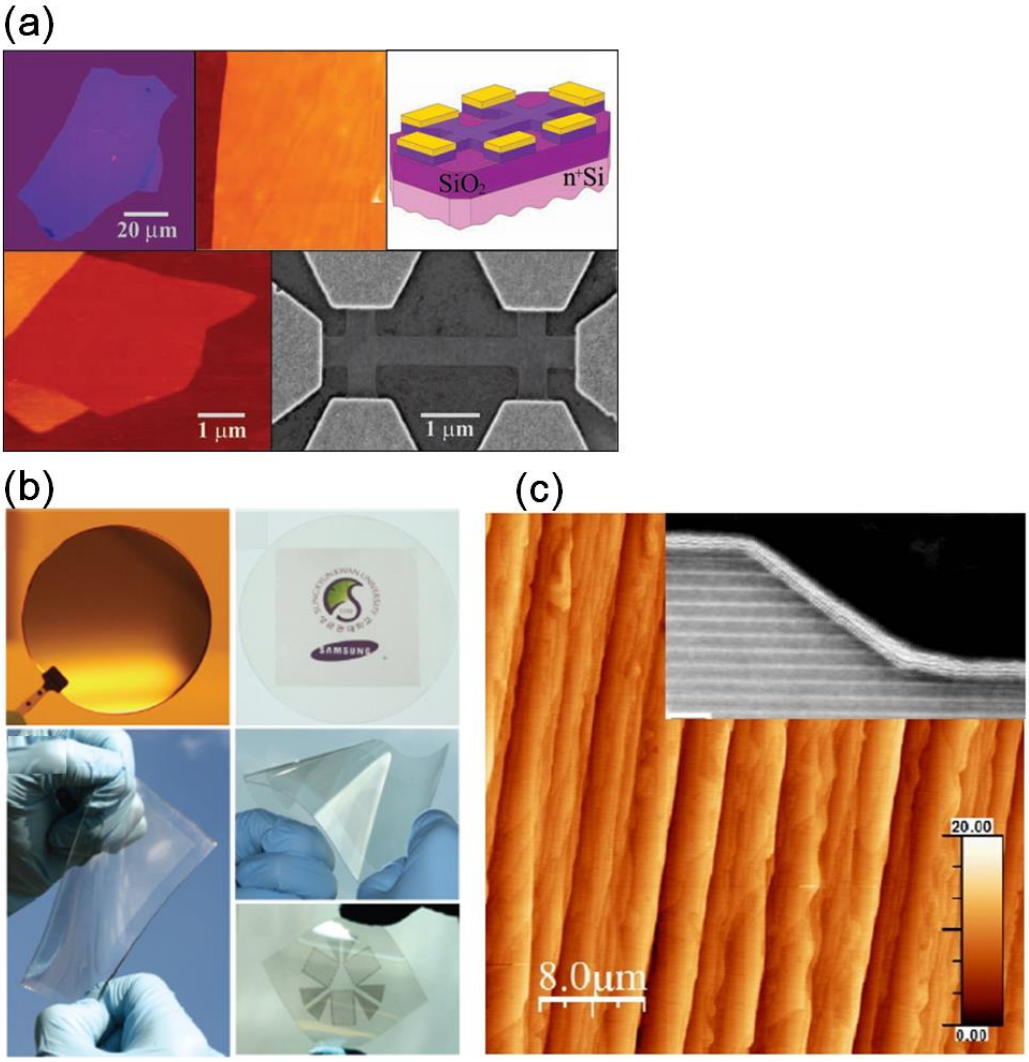


Figure 1.3. (a) Hall bar fabrication with exfoliated graphene [1] (b) CVD graphene transfer on flexible substrate [28] (c) AFM image of epitaxial graphene shows terraces of SiC surface (inset) TEM image of graphene coverage over SiC terrace [31]

Epitaxial graphene has been an attractive candidate for high speed graphene transistor applications, because of its excellent film quality and no need of transfer to other substrate. The film is grown on SiC substrate by sublimation of Si atoms of the top surface by annealing at >1000^{o}C under vacuum or Ar environment [31, 32]. Carbon atoms remain at the surface and rearrange to form a graphene film. C-terminated faces

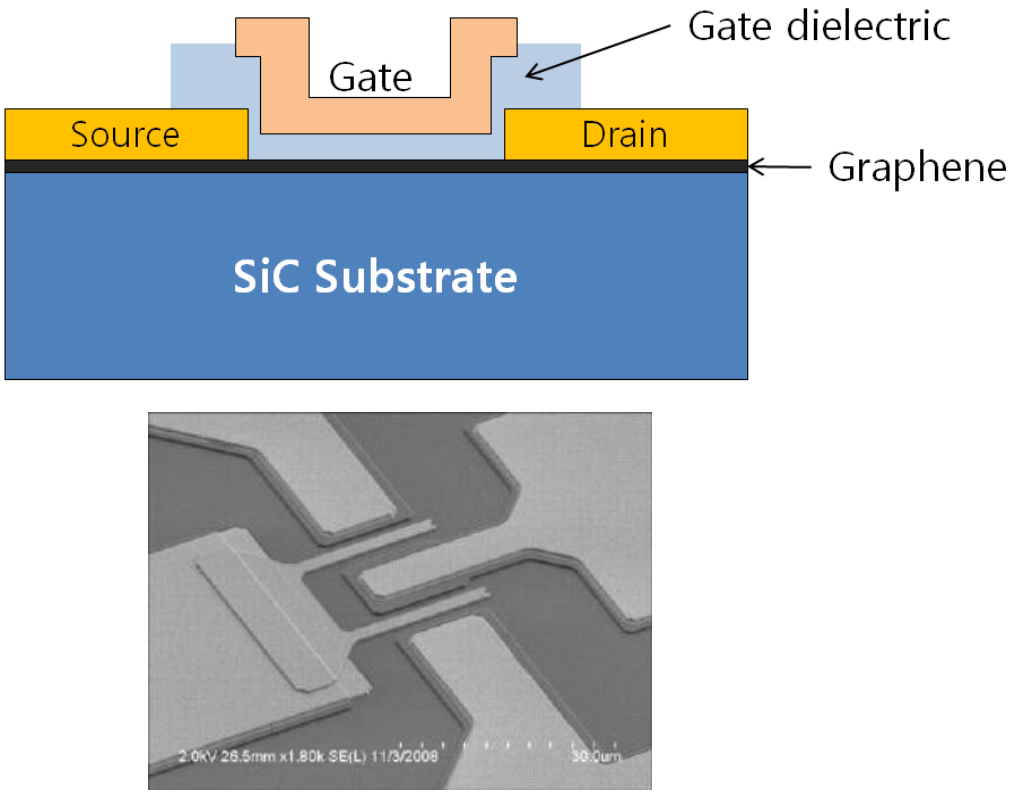
tend to form a multi layer graphene, while it is easier to control the number of carbon sheet layers from single to few layers on Si-terminated SiC surface. Epitaxial graphene shows n-type doped characteristics due to background doping effect from the substrate and interface [32]. Figure 1.3 (c) shows TEM image of epitaxial graphene over the terrace of SiC substrate, where graphene has an excellent coverage over steps and terraces of SiC surface.

The film quality of graphene is typically measured by means of atomic force mictroscopy (AFM) and Raman spectroscopy. AFM measurement shows grain sizes up to micron scale [33, 34] and steps of epitaxial graphene due to the topography of SiC substrate [31]. Raman spectroscopy can distinguish the number of layers [35, 36] by investigating the height and width ‘g peak’, which is a signal according to graphene. Quality of graphene film can be estimated by ‘d peak’ which typically shows the defects of the film. After years of intensive R&D efforts, the quality and reproducibility of large area graphene film has been improved significantly. The degree of control of material characteristics over wafer scale is comparable to conventional semiconductor materials [37-39]

1.3. Graphene Field Effect Transistors (GFET)

A representative top-gated graphene FET structure on semi-insulating SiC substrate is shown in Figure 1.4 (a) [11]. The graphene FET channel area is defined by O_2 plasma etch. Source and drain electrodes, gate dielectric, and gate metal stack processes follows. Figure 1.4 (b) shows a SEM image of fabricated r.f. GFET on SiC substrate. Ohmic contacts showed resistance as low as 0.2 Ω·mm [40]. devices are also similar

structure, except using the substrate of SiO_2 on bulk Si [13, 41]. When the Si substrate is low resistivity substrate, it can act as a global bottom gate. In fact, many of initial device fabrication have used global back gate to control the transferred graphene flake devices without top gate.



Figuer 1.4. (a) Representative structure of epitaxial graphene FET (b) SEM image of 2-finger GFET [11]

Various types of gate dielectrics have been utilized for graphene surface, which have been a challenging task due to lack of dangling bonds on the surface of graphene [42]. Prototype transferred graphene used thick oxide as a gate dielectric. Building an embedded gate structure under high-k material then transferring graphene film on top was

another way to avoid this problem [43]. Spontaneous oxidization of few nanometer of Al film or graphene surface functionalization by grafting diazonium salt [44] are a few example of providing an initial seed layer for subsequent ALD deposition for conventional device process steps.

Doping the graphene film is also a difficult challenge. There have been several methods reported such as replacing carbon atoms with nitrogen atoms [45], add organic layer to provide charge transfer [46]. However, it is still difficult to obtain high quality graphene (without degrading mobility) after these doping methods. Transferred graphene FETs can use the global back gate to provide desired charge density level of the region between gate and source/drain. Ungated gap region is series resistance along the channel of the FET, which degrades the performance [14, 15]. Epitaxial graphene is known to have n-type film which has ~10^{12} cm^{-2} of charge density [11, 31], relatively relieves the need of additional doping, however, it would be desired to have self aligned structure best performance.

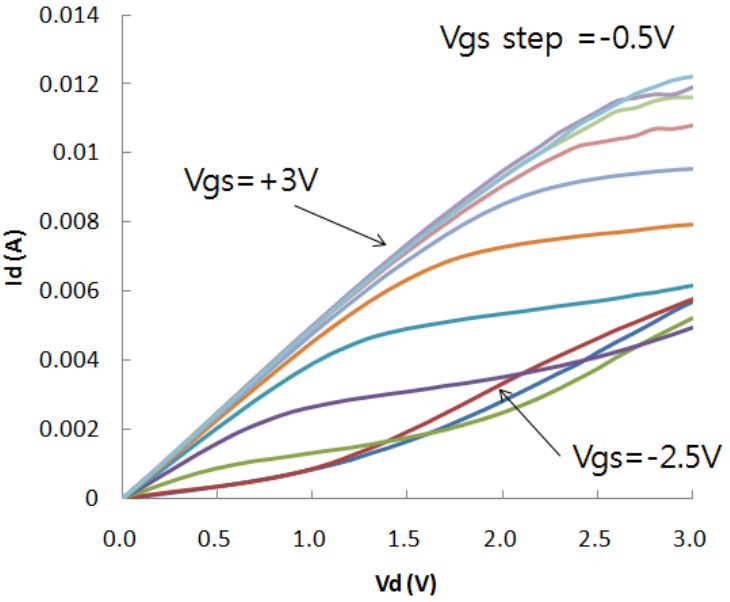


Figure 1.5. Id-Vd curves of GFET with different Vgs

A long channel graphene FET I_d-V_d characteristics are displayed in figure 1.5. Current level is modulated with gate bias, however, current flows even when $V_g < V_{th}$ (or V_{Dirac}). It is due to graphene's zero bandgap nature which makes the pinch off difficult, especially under large V_{ds}. When V_{ds} increases the current shows a saturation behavior, then increases again because hole channel is introduced near drain instead of pinch-off region of conventional FETs. A model with the Gradual Channel Approximation describes the I-V characteristics.

$$I = \mu \frac{W}{L} C_{eff} \left[\frac{1}{2}(V_g - V_t)^2 + \frac{1}{2}(V_d - V_g + V_t)^2 \right]$$

where I is drain current when μ is effective mobility, W and L are width and length of the channel, respectively. C_{eff} is effective gate capacitance, V_d is drain bias, V_g is gate bias, and V_t is threshold voltage also known as Dirac point. Figure 1.6 displays I_d-V_g characteristic of graphene FET is a V-shaped ambipolar curve, with minimum current conduction point at $V_g=V_{Dirac}$. Where $V_g>V_{Dirac}$, the channel is filled with electrons (electron branch), while it becomes hole channel when $V_g<V_{Dirac}$ (hole branch). Near at Dirac point, it also offers unique features such as quadratic variation of current with gate voltage.

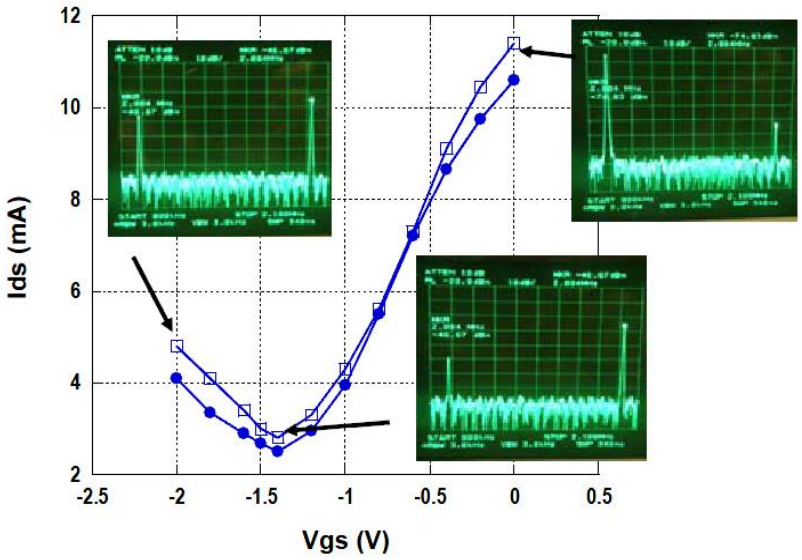


Figure 1.6. Graphene FET's Id-Vgs curve shows ambipolar, v-shape curve with minimum current at Vgs=VDirac. Mixer output spectra is also shown, which benefitted from quadratic current increase of GFET [47]

Graphene also could handle a very high on current, up to values of >3mA/um, limited by dielectric strength [17], thermal breakdown [48]. Excellent confinement barriers surrounding graphene channel also affects the efficient current flow, which is

much improved compared with conventional FETs. The number of carriers can increase if the gate dielectric is thinner and also hold large electric field. Better thermal design can increase the I_{max} by lower the junction temperature from Joule self heating.

Graphene offers new opportunities for a high frequency FETs because of its high carrier mobility, planar structure with excellent scaling properties, limited scattering and a simple modulation of electron and hole channels.

1.4. Research Summary

Motivated by unconventional experimental results and mismatches between test data and theory on epitaxial graphene devices, several simulation and modeling approaches have been employed to illuminate the details of several building-blockcomponents required to build graphene-based device systems. A starting point for the research is the set of graphene material properties such as uniformity of the charge density, and junctions of graphene-contact metal, and between p- and n-type graphene. Joule-self heating is heavily involved in current saturation and breakdown of GFETs, therefore the thermal behavior of graphene device is investigated with 3-D thermal simulations. After reviewing the characteristics of elements of GFETs, device models are introduced in two forms: a SPICE-like compact model; and an abstract analytic model. Circuit simulations with these device models are demonstrated for GFET based power detector and resistive mixer applications. Key results of this dissertation are summarized here:

- Techniques to perform a classical approach with physically based TCAD simulator for electrostatics of graphene p-n junction. Numerical estimation of spatial resistivity based on carrier distribution and carrier density dependent mobility of electrons and holes, which matches the experimental results and provides a simple understanding of origin of asymmetrical I_d-V_g curves.

- Modeling of lateral charge spread from the metal contact by employing a two-dimensional Poisson solver, to find out relations of charge density and metal work function which causes unintentional lateral doping and errors on contact resistance measurements.

- Modeling techniques of inhomogeneous graphene film which describes the physical consequences of randomly distributed charges, so-called electron hole puddles, on Hall measurements, Dirac point estimation, and overall device-to-device uniformity on wafer scale.

- Application of a three-dimensional thermal simulation to investigate the junction temperature of graphene devices. Investigated the heat dissipation behavior with focus on device dimensions, structure, and interface thermal resistances. Comparison with experimental results shows the saturation behavior of I-V of graphene device is partially due to Joule self-heating.

- Establishment of a SPICE based compact model to describe the ambipolar conduction of GFETs to explore circuit applications in straightforward manner. The model shows a good fit with experimental results with only a few device parameter adjustments.

- Development of an abstract analytic model of GFET with Taylor expansion to investigate the impact of device parameters on circuit performance, such as nonlinearity.

- Demonstration of GFET circuit simulation utilizing compact and abstract models, for description of power detector and mixer applications. Investigation on impact of device parameters on circuit performances for optimization.

1. 5. Thesis overview

This thesis presents an analysis of various aspects of graphene behaviors and device physics, of importance for applications of graphene in high frequency electronics. Electrical characteristics at graphene p-n junctions and metal-graphene contact edges, graphene film uniformity and its impact on mobility measurements, Joule self-heating and heat dissipation are described and analyzed. The thesis also covers compact device modeling of graphene FETs for circuit simulations and discusses implications for r.f. applications

In Chapter 2 the local resistance of graphene devices around p-n junctions and graphene-metal edges are described. p-n junction resistance causes additional series

resistance and asymmetry of V-shaped ambipolar Id-Vg current between hole and electron current. Metal edges can form several types of junctions and impacts the accuracy of TLM measurement for contact resistance. These experimentally observed effects are analyzed with two dimensional devices simulations and Poisson solver. Classical approach shows characteristics of graphene p-n junctions and its impact on ambipolar current asymmetry. Effective graphene doping from metal and charge transfer region will be discussed, focusing on contact resistance measurement.

Chapter 3 introduces a two-dimensional inhomogeneous graphene model for calculation of electric charges and fields with or without magnetic fields. In the model, dopants are distributed randomly to emulate the so-called electron-hole puddle. Various device parameters such as puddle size, charge density deviation and channel sizes are investigated to provide potentials and limits of uniformity for practical graphene devices.

Chapter 4 presents analysis on thermal behavior of graphene resistors on silicon carbide substrates, using three dimensional heat simulations. Several device parameters such as interface thermal resistance, channel width, and contact spacing are investigated for vertical and lateral heat spread characteristics. For comparison, pulsed I-V measurement is employed with various pulse lengths and environment temperature. Effective thermal resistance of the system and Joule heating during a short pulse will be discussed.

Chapter 5 explores the potential performance of radio frequency (r.f.) graphene FETs (GFET). A compact model is developed with SPICE models and also an analytic model was used for analyze the relation of device parameters with circuit performances.

Zero biased power detector and resistive linear mixers are investigated and optimized with circuit simulations including parasitic componenets.

Chapter 6 summarizes the thesis and briefly mentions future works.

1.6. References

[1] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva and A. A. Firsov, “Electric field effect in atomically thin carbon films,” Science, vol. 306, Oct. 2004, no. 5696, pp. 666-669, doi: 10.1126/science.1102896

[2] F. Schwierz, "Graphene transistors," Nature Nanotech., vol. 5, May 2010, pp. 487–496, doi:10.1038/nnano.2010.89

[3] A. K. Geim, "Graphene: status and prospects," Science, vol. 324, June 2009, pp. 1530-1534, doi: 10.1126/science.1158877\

[4] S. V. Morozov, K. S. Novoselov, M. I. atsnelson, F. Schedin, D. C. Elias, J. A. Jaszczak, and A. K. Geim, "Giant Intrinsic Carrier Mobilities in Graphene and Its Bilayer," Phys. Rev. Lett., vol. 100, Jan. 2008, pp. 160602, doi: 10.1103/PhysRevLett.100.016602

[5] K. S. Novoselov, A. K. Geim, S. Morozov, D. Jiang, M. Katsnelson, I. Grigorieva, S. Dubonos, and A. Firsov, "Two-Dimensional Gas of Massless Dirac Fermions in Graphene," Nature, vol. 438, Nov. 2005, pp. 197-200, doi: 10.1038/nature04233

[6] H. Wang, Q. Wang, K.-G. Zhou, and H.-L. Zhang, "Graphene in Light: Design, Synthesis and Applications of Photo-active Graphene and Graphene-Like Materials." Small 9, no. 8, 2013, pp. 1266-1283

[7] S. Seo, M. Min, S.M. Lee, and H. Lee, “Photo-switchable molecular monolayer anchored between highly transparent and flexible graphene electrodes,” Nature communications, 4, 2013, p.1920

[8] C. Lee, X. Wei, J. W. Kysar, J. Hone, “Measurement of the Elastic Properties and Intrinsic Strength of Monolayer Graphene ,” Science 18 Jul. 2008, Vol. 321, Issue 5887, pp. 385-388, DOI: 10.1126/science.1157996

[9] K. I. Bolotin, K.J. Sikes, Z. Jiang, M. Klima, G. Fudenberg, J. Hone, P. Kim and H.L. Stormer, "Ultrahigh electron mobility in suspended graphene," Solid State Comm. vol. 146, June 2008, pp. 351-355, doi:10.1016/j.ssc.2008.02.024

[10] Y. Zhang, Y.-W. Tan, H. L. Stormer & P. Kim, "Experimental observation of the quantum Hall effect and Berry's phase in graphene," Nature, vol. 438, Nov. 2005, pp. 201-204, doi:10.1038/nature04235

[11] J. S. Moon, D. Curtis, M. Hu, D. Wong, C. McGuire, P.M. Campbell, G. Jernigan, J.L. Tedesco, B. VanMil, R. Myers-Ward and C. Eddy Jr, "Epitaxial-Graphene RF Field-Effect Transistors on Si-Face 6H-SiC Substrates," IEEE Elec. Dev. Lett., vol. 30, pp. 650-652, doi: 10.1109/LED.2009.2020699

[12] D. J. Frank, Y. Taur, and H. -S. P. Wong, "Generalized Scale Length for Two-Dimensional Effects in MOSFET's," IEEE Elec. Dev. Lett., vol. 19, Oct. 1998, pp. 385-387, doi: 10.1109/55.720194

[13] Max C. Lemme, Tim J. Echtermeyer, Matthias Baus, and Heinrich Kurz, "A Graphene Field-Effect Device," IEEE ELEC. DEV. LETT., VOL. 28, APRIL 2007, pp. 282-284, doi: 10.1109/LED.2007.891668

[14] D. B. Farmera, Y.-M. Lin and Ph. Avouris, "Graphene field-effect transistors with self-aligned gates," Appl. Phys. Lett. vol. 97, July 2010, pp. 013103/1-013103/3, doi:10.1063/1.3459972

[15] L. Liao, Y.C. Lin, M. Bao, R. Cheng, J. Bai, Y. Liu, Y. Qu, K.L. Wang, Y. Huang, and X. Duan, "High-speed graphene transistors with a self-aligned nanowire gate," Nature, vol. 467, Sep. 2010, pp. 305–308, doi: 10.1038/nature09405

[16] J. S. Moon, D. Curtis, S. Bui, T. Marshall, D. Wheeler, I. Valles, S. Kim, E. Wang, X. Weng and M. Fanton, "Top-Gated Graphene Field-Effect Transistors Using Graphene on Si (111) Wafers," IEEE Elec. Dev. Lett., vol. 31, Nov. 2010, pp. 1193-1195, doi: 10.1109/LED.2010.2065792

[17] Y.M. Lin, C. Dimitrakopoulos, K.A. Jenkins, D.B. Farmer, H.Y. Chiu, A. Grill, and P. Avouris, "100-GHz transistors from wafer-scale epitaxial graphene," Science, 327(5966), 2010, pp.662-662

[18] R. S. Shishir and D. K. Ferry, "Intrinsic mobility in graphene," J. Phys.: Condens. Matter vol. 21, June 2009, pp. 232204/1-232204/4, doi: 10.1088/0953-8984/21/23/232204

[19] J. Yan, Y. Zhang, P. Kim and A. Pinczuk, "Electric Field Effect Tuning of Electron-Phonon Coupling in Graphene," Phys. Rev. Lett. vol. 98, Apr. 2007, pp. 166802/1-166802/4, doi: 10.1103/PhysRevLett.98.166802

[20] A. Konar, T. Fang and D. Jena, "Effect of high-k gate dielectrics on charge transport in graphene-based field effect transistors," Phys. Rev. B, vol. 82, Sep. 2010, pp. 115452/1-115452/7, doi: 10.1103/PhysRevB.82.115452

[21] A. K. Geim and K. S. Novoselov, "The rise of graphene," Nature Mat.erials, vol. 6, Mar. 2007, pp. 183-191, doi: 10.1038/nmat1849

[22] G. M. Rutter, J. N. Crain, N. P. Guisinger, T. Li, P. N. First, and J. A. Stroscio, "Scattering and Interference in Epitaxial Graphene," Science. vol. 317, July 2007, pp. 219-222, doi: 10.1126/science.1142882

[23] M.I. Katsnelson and A.K. Geim, "Electron scattering on microscopic corrugations in graphene," Phil. Trans. R. Soc. A, vol. 366, Jan. 2008, pp.195-204, doi: 10.1098/rsta.2007.2157

[24] C. Jang, S. Adam, J.-H. Chen, E. D. Williams, S. Das Sarma, and M. S. Fuhrer, "Tuning the Effective Fine Structure Constant in Graphene: Opposing Effects of Dielectric Screening on Short-and Long-Range Potential Scattering," Phys. Rev. Lett. vol.101, Oct. 2008, pp.146805/1-146805/4, doi: 10.1103/PhysRevLett.101.146805

[25] Y. Zhang, Y.-W. Tan, H. L. Stormer and P. Kim, "Experimental observation of the quantum Hall effect and Berry's phase in graphene," Nature, vol. 438, Nov. 2005, pp. 201-204, doi:10.1038/nature04235

[26] X. Li, W.Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, and S.K. Banerjee., "Large-Area Synthesis of High-Quality and Uniform Graphene Films on Copper Foils," Science, vol. 324, June 2009, pp. 1312-1314, doi: 10.1126/science.1171245

[27] A. Reina, X. Jia, J. Ho, D. Nezich, H. Son, V. Bulovic, M. S. Dresselhaus and J. Kong, "Large Area, Few-Layer Graphene Films on Arbitrary Substrates by Chemical Vapor Deposition," Nano Lett., vol. 9, Dec. 2008, pp. 30–35, doi: 10.1021/nl801827v

[28] Y. Lee, S. Bae, H. Jang, S. Jang, S. E. Zhu, S. H. Sim, Y.I. Song, B. H. Hong, J. H. Ahn, "Wafer-scale synthesis and transfer of graphene films," Nano letters, 10(2), Jan 2010, pp. 490-493

[29] J. D. Caldwell, T.J. Anderson, J.C. Culbertson, G.G. Jernigan, K.D. Hobart, F.J. Kub, M.J. Tadjer, J.L. Tedesco, J.K. Hite, M.A. Mastro, and R.L. Myers-Ward, "Technique for the Dry Transfer of Epitaxial Graphene onto Arbitrary Substrates," ACS Nano, Jan. 2010, 4 (2), pp 1108–1114, DOI: 10.1021/nn901585p

[30] S. Bae, H. Kim, Y. Lee, X. Xu, J.S. Park, Y. Zheng, J. Balakrishnan, T. Lei, H.R. Kim, Y.I. Song, and Y.J. Kim, "Roll-to-roll production of 30-inch graphene films for transparent electrodes," Nature nanotechnology, Aug. 2010, *5*(8), pp.574-578

[31] D.K. Gaskill, G. Jernigan, P. Campbell, J.L. Tedesco, J. Culbertson, B. VanMil, R.L. Myers-Ward, C. Eddy, J. Moon, D. Curtis, and M. Hu, "Epitaxial Graphene Growth on SiC Wafers," ECS Trans., vol. 19, May 2009, pp. 117-124, doi: 10.1149/1.3119535

[32] C. Berger, Z. Song, T. Li, X. Li, A.Y. Ogbazghi, R. Feng, Z. Dai, A.N. Marchenkov, E.H. Conrad, P.N. First, and W.A. De Heer, "Ultrathin Epitaxial Graphite: 2D Electron Gas Properties and a Route toward Graphene-based Nanoelectronics," J. Phys. Chem. B, vol. 108, Dec. 2004, pp. 19912-19916, doi: 10.1021/jp040650f

[33] P. Y. Huang, C.S. Ruiz-Vargas, A.M. van der Zande, W.S. Whitney, M.P. Levendorf, J.W. Kevek, S. Garg, J.S. Alden, C.J. Hustedt, Y. Zhu, and J. Park, "Grains and grain boundaries in single-layer graphene atomic patchwork quilts," Nature 469, Jan. 2011, pp. 389–392, doi:10.1038/nature09718

[34] P. Nemes-Incze, K.J. Yoo, L. Tapasztó, G. Dobrik, J. Lábár, Z.E. Horváth, C. Hwang, and L.P. Biró, "Revealing the grain structure of graphene grown by chemical vapor deposition," Appl. Phy. Lett., Jul. 2011 1;99(2):023104

[35] A. C. Ferrari, J.C. Meyer, V. Scardaci, C. Casiraghi, M. Lazzeri, F. Mauri, S. Piscanec, D. Jiang, K.S. Novoselov, S. Roth, and A.K. Geim, "Raman Spectrum of Graphene and Graphene Layers," Phys. Rev. Lett., vol. 97, Oct. 2006, pp.187401/1-187401/4, doi: 10.1103/PhysRevLett.97.187401

[36] A. Gupta, G. Chen, P. Joshi, S. Tadigadapa and P. C. Eklund, "Raman scattering from high-frequency phonons in supported n-graphene layer films," Nano Lett., vol. 6, Nov. 2006, pp. 2667-2673, doi: 10.1021/nl061420a

[37] J. S. Moon, D. Curtis, M. Hu, D. Wong, P. M. Campbell, G. Jernigan, J. Tedesco, B. VanMil, R. Myers-Ward, C. Eddy, D. K. Gaskill, J. Robinson, M. Fanton, P. Asbeck, "Development toward Wafer-Scale Graphene RF Electronics," ECS Trans., vol. 19, May 2009, pp. 35-40, doi: 10.1149/1.3119525

[38] Y.-M. Lin, C. Dimitrakopoulos, K.A. Jenkins, D.B. Farmer, H.Y. Chiu, A. Grill, and P. Avouris, "100-GHz Transistors from Wafer-Scale Epitaxial Graphene," Science, vol. 327, Feb. 2010, p. 662, doi: 10.1126/science.1184289

[39] K. Kim, "From the future Si technology perspective: Challenges and opportunities," IEEE Intl. Elec. Dev. Meeting (IEDM 2010), Dec. 2010, pp. 1.1.1 - 1.1.9, doi: 10.1109/IEDM.2010.5703274

[40] J.S. Moon, M. Antcliffe, H.C. Seo, D. Curtis, S. Lin, A. Schmitz, I. Milosavljevic, A.A. Kiselev, R.S. Ross, D.K. Gaskill, and P.M/ Campbell, "Ultra-low resistance ohmic contacts in graphene field effect transistors," Appl. Phys. Lett. 100(20), 2012, p.203512

[41] I. Meric, M. Y. Han, A. F. Young, B. Ozyilmaz, P. Kim, and K. L. Shepard, "Current saturation in zero-bandgap, top-gated graphene field-effect transistors," Nat. Nanotechnol., vol. 3, Nov. 2008, pp. 654–659, doi: 10.1038/nnano.2008.268

[42] X. Wang, S. M. Tabakman and H. Dai, "Atomic Layer Deposition of Metal Oxides on Pristine and Functionalized Graphene," J. Am. Chem. Soc., vol. 130, June 2008, pp. 8152–8153, doi: 10.1021/ja8023059

[43] J. Lee, H. J. Chung, J. Lee, J. Shin, J., Heo, H. Yang, S.H. Lee, S. Seo, J. Shin, U.I. Chung, and I. Yoo, "RF performance of pre-patterned locally-embedded-back-gate graphene device," IEEE International Electron Devices Meeting (IEDM), Dec. 2010, pp. 23-5

[44] Y. Q. Wu, D.B. Farmer, A. Valdes-Garcia, W.J. Zhu, K.A. Jenkins, C. Dimitrakopoulos, P. Avouris, and Y.M. Lin, "Record high RF performance for epitaxial graphene transistors," IEEE International Electron Devices Meeting (IEDM), Dec. 2011, pp. 23-8

[45] X. Wang, X. Li, L. Zhang, Y. Yoon, P.K. Weber, H. Wang, J. Guo, and H. Dai, "N-Doping of Graphene Through Electrothermal Reactions with Ammonia," Science, vol. 324, May 2009, pp. 768-771, doi: DOI: 10.1126/science.1170335

[46] Y. Gao, H.L. Yip, K.S. Chen, K.M. O'Malley, O. Acton, Y. Sun, G. Ting, H. Chen, and A.K.Y.Jen, "Surface doping of conjugated polymers by graphene oxide and its application for organic electronic devices," Advanced Materials, 23(16), 2011, pp.1903-1908

[47] J. S. Moon, D. Curtis, D. Zehnder, S. Kim, D.K. Gaskill, G.G. Jernigan, R.L. Myers-Ward, C.R. Eddy Jr, P.M. Campbell, K.M. Lee, and P. Asbeck, "Low Phase Noise

Graphene FETs in Ambipolar RF Applications," IEEE Elec. Dev. Lett., 32, no. 3, 2012, pp. 270-272.

[48] A.D. Liao, J.Z. Wu, X. Wang, K. Tahy, D. Jena, H. Dai, and E. Pop, “Thermally limited current carrying ability of graphene nanoribbons,” Physical review letters, 106(25), 2011, p.256801

Chapter 2

Physics of Junctions of Graphene Devices

In this chapter, the device physics of graphene junctions will be investigated. In the first part of the chapter (Section 2.1~2.4), the resistance of graphene p-n junctions is analyzed following a classical approach. A two dimensional device simulator was employed to determine the electric field and channel conductivity variations across p-n junctions formed in graphene FET structures. Simulation results will verify the origin of asymmetry of I_d-V_g curves of graphene FET measurements.

In the second part of the chapter (section 2.5~2.9), effective doping from a metal on graphene by its work function difference and graphene's small density of states will be discussed, focusing on a charge transfer region (CTR) near the contact edge. We will

investigate various factors which can affect the CTR length, and the impacts of CTR on conventional contact resistance measurement method.

2.1. Drain Current Asymmetry in Transfer Characteristics of Graphene FETs

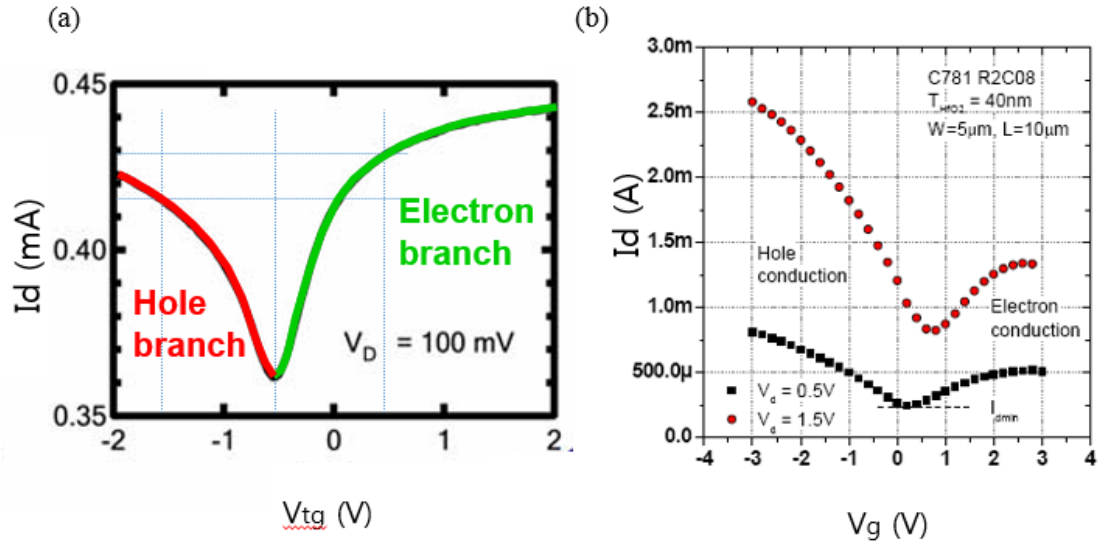


Figure 2.1. Asymmetry in the drain current transfer characteristics reported in literatures. (a) Graphene FET with n-type channel (effectively doped) [1]. V_{Dirac} is below 0V and electron branch shows higher current level than hole branch. (b) I_d-V_g of p-doped graphene channel FET [2]

For graphene FETs, asymmetry in the drain current transfer characteristics has been observed with respect to the gate bias as shown in Figure 2.1. It is important to understand this asymmetry to properly model and design future carbon based electronics. It has been proposed that the asymmetry is due to additional resistances from p-n transition regions along the channel under specific bias conditions, particularly between contact regions and the channel, arising due to the ambipolar nature of graphene conduction [3, 4]. Calculations of the additional resistance have already been reported,

with particular attention to circumstances where p-n transition lengths are small [5, 6]. Here we provide a simple analysis of the resistance of graphene FETs with p-n junctions under conditions where transition lengths are long compared with energy and momentum relaxation lengths, as is found in many experimental FETs.

2.2. Theory and Simulations: Graphene FET and p-n Junction

We employ a two dimensional device simulator to determine the electric field and channel conductivity variations in the vicinity of the FET gate, assuming rapid electron/hole equilibration. The physically-based device simulator Atlas of Silvaco with parameters modified to describe single layer graphene was used to obtain electrostatic carrier distributions under various bias conditions. The idealized structure considered in the model is particularly appropriate to single layer graphene (as opposed to bilayer graphene) since the absence of a bandgap is conducive to rapid electron-hole equilibration. As described in Figure 2.2, the device studied was a graphene FET on a SiO_2 substrate; a global back gate was placed beneath the back oxide, and 0.3 μm gate/drain and gate/source gaps were used. The thickness of the top gate oxide (T_{ox}) was 10 nm. A long channel device with small drain bias condition (V_{ds}= 10 mV) was used to minimize the lateral electric field effect.

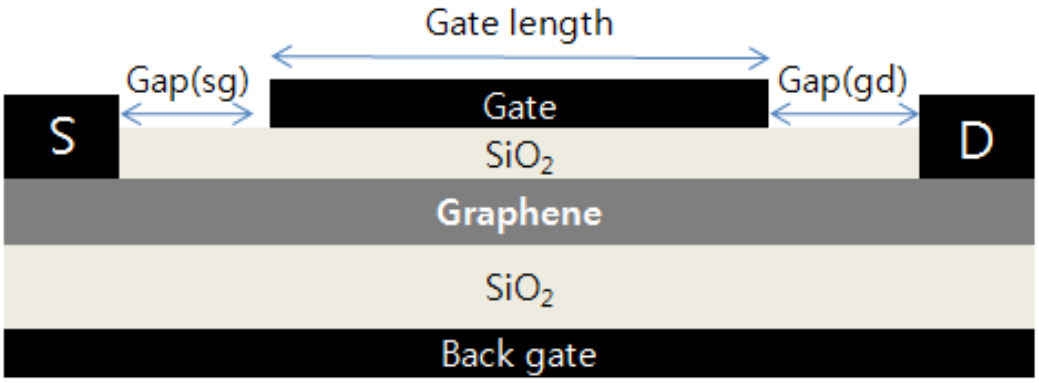


Figure 2.2. (a) Schematic of the simulated device structure. The gate length is 1.5μm, and the length of each gap is 0.3um. T_{ox} is 10nm.

The carrier density in the gap regions was controlled by the back gate bias (V_{bg}), while the channel region under the top gate was modulated by top and back gate simultaneously. Under positive V_{bg}, the graphene layer becomes n-type in the gap regions. Proper top gate bias (V_{tg}) may be applied to make channel region intrinsic, p-type or n-type. Therefore, various configurations along the channel such as npn or nnn structures may be created. Schematic description of graphene bands and Fermi energies of each configuration are displayed in Figure 2. 3. When the channel is modulated to n-type, p-type or intrinsic are by top gate bias, Fermi energy level is aligned in the conduction band, valence band and the Dirac point of graphene bands. Simulation results of lateral carrier distribution of nin, nnn, and npn structures are showed in Figure 2. 4 with assumed n-type contact for source and drain.

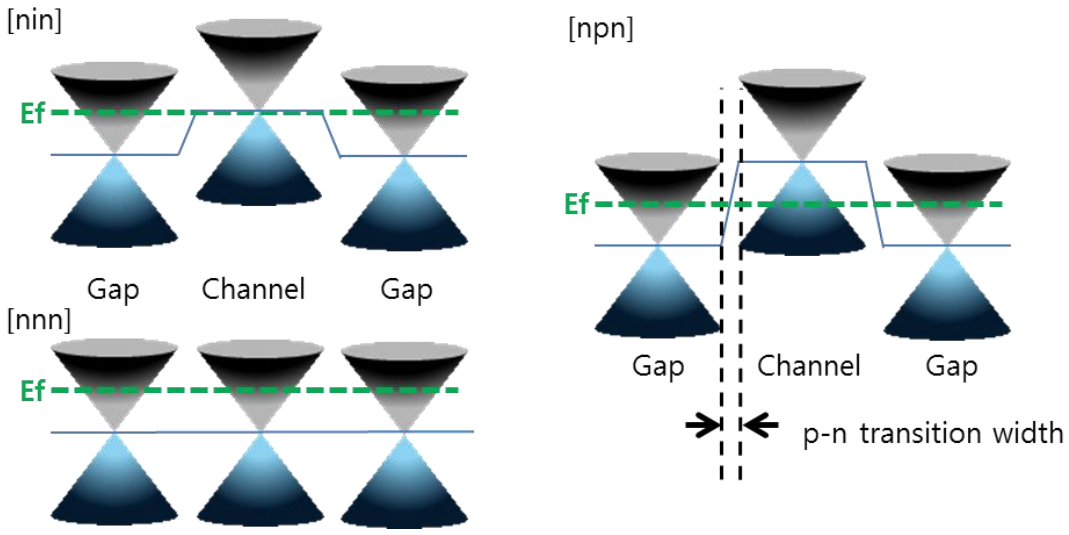


Figure 2.3. Schematic band alignments versus Fermi energy for intrinsic, n-type and p-type channel graphene FET.

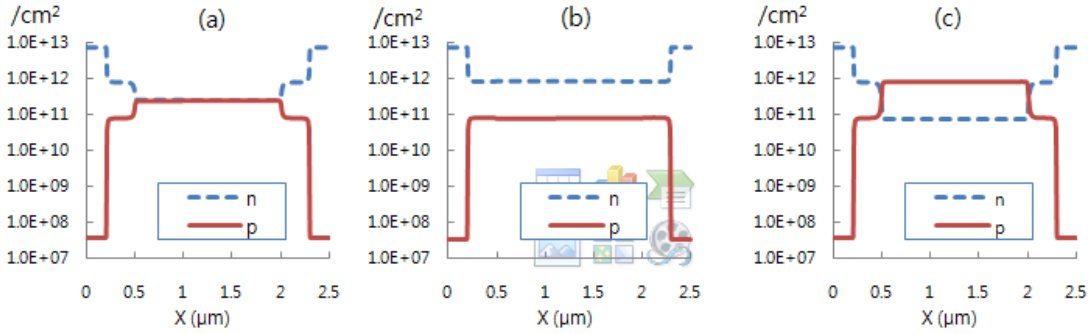


Figure 2.4. Simulated carrier distribution of graphene FETs. (a) nin structure (b) nnn structure (c) npn structure. Contacts are assumed to be n-type.

The resistivity vs position is calculated based on the simulated total number of carriers (n+p) following $\rho = 1 / [q \mu (n+p)]$. Mobility is assumed to be the same for electrons and holes, and is assumed to depend on carrier concentration N_s, $\mu=\mu_0 (N_0/N_s)^{1/2}$ where N_0 is the carrier concentration (n+p) under intrinsic conditions and μ_0 is the peak mobility. The calculated resistance values were not highly sensitive to the N_s dependence chosen for the mobility. Resistivity at the position of the p-n junction reaches its peak

value of $\rho_{max} = 1 / (q\ \mu_0\ N_0)$. We assumed peak mobility of 4500 $cm^2/Vsec$ in the simulation. In practical FETs, mobility will be affected by the quality of the graphene channel, and the p-n junction resistance will correspondingly change in nearly inverse fashion.

2.3. Analysis of Graphene p-n Junction and Additional Resistance

2.3.1. Additional Resistance at p-n Junction

Figure 2.5 plots ρ calculated from total number of carriers versus channel position at different gate voltage conditions. The total resistance is the integrated area under this resistivity curve. When V_{tg} reaches V_{Dirac} (charge neutral point, or Dirac point), the channel region becomes intrinsic and the drain current reaches a minimum. When we have npn structure with V_{tg}-$V_{Dirac} < 0$, and in Figure 2.5 (c), the resistivity peaks up at the p-n transition. No such resistivity peak appears for the nnn case.

The additional resistance of a p-n junction (ΔR) is calculated by integrating the difference of the nnn resistivity and npn resistivity vs. channel position. Figure 2.6 shows overlapped resistivity curves for n-p-n and n-n-n structures; ΔR can be visualized by the integrated area difference. The simulations show that added resistances that in the range of 50-500 Ωμm per p-n junction are obtained. The magnitude of the extra resistance is approximately equal for both directions of current flow.

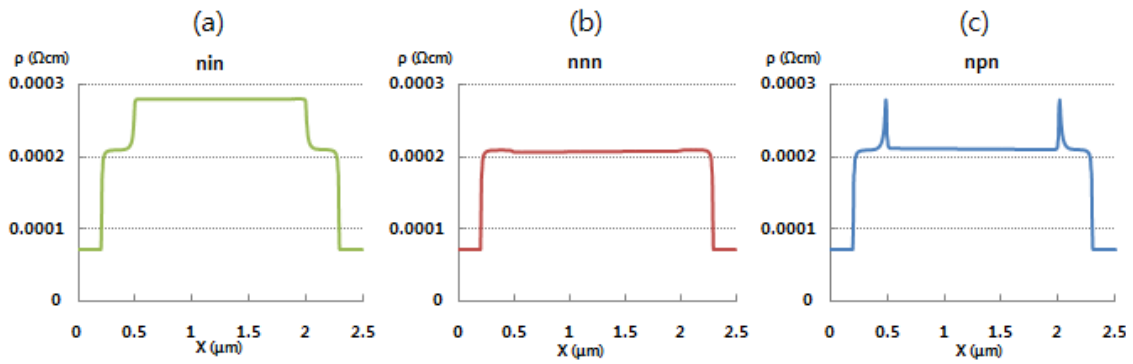


Figure 2.5. ρ versus channel position. (a) nin structure ($V_{tg}=V_{Dirac}$), the channel is intrinsic and shows high resistivity (b) nnn structure ($V_{tg}>V_{Dirac}$), the channel is n-type (c) npn structure ($V_{tg}<V_{Dirac}$). Resistivity peak is at the p-n junction.

2.3.2. p-n Resistance Control Factors

The integrated resistance value is impacted by the resistivity peak height and peak width. The peak height can be defined as ρ_{max} - ρ_{ch} where ρ_{ch} is the resistivity of the channel. The resistivity reaches a maximum value (ρ_{max}) at the threshold condition, where the electron and hole densities reach their intrinsic levels. The resistivity of both n and p channels decreases when $|V_{tg}-V_{Dirac}|$ increases, therefore the difference ρ_{max} - ρ_{ch} increases as well. Figure 2.6 (b) shows the peak height at the junction is smaller when p-n transition is from weak p-type (p-) channel to n-type in the gap region, and larger with transition of strong p-type (p+) channel to n-type.

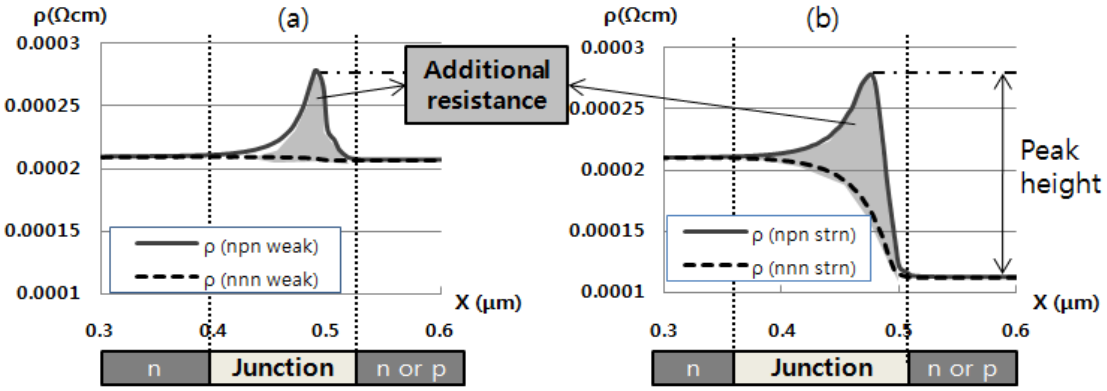


Figure 2.6. The additional resistance from the resistivity curve. (a) Additional resistance of p-n junction is the integrated area between resistivity of nnn and npn. (b) Increased peak height and integrated area when larger V_{tg} applied to the top gate.

As carrier concentration in the channel increases, the peak of resistivity changes position slightly and moves into the gap region - Figure 2.7. With larger $|V_{tg}-V_{Dirac}|$, the p-n transition region width is reduced in channel region, but widened out to the gap region. We find that the fringe electric field from the top gate is responsible for the width of the peak. Simulation results for 20nm oxide thickness (T_{ox}), show that the width of the transition region (110nm) increases by 28 % relative to the value for 10nm (86nm).

The additional p-n resistance shows saturation behavior near 500 Ωμm when $|V_{tg}-V_{Dirac}|$ further increases. With larger gate bias the peak height is increased, however the slope of the resistivity curve became more vertical at the gate edge. The integrated area increment due to Vg change is very small at large $|V_{tg}-V_{Dirac}|$, therefore the p-n resistance saturates.

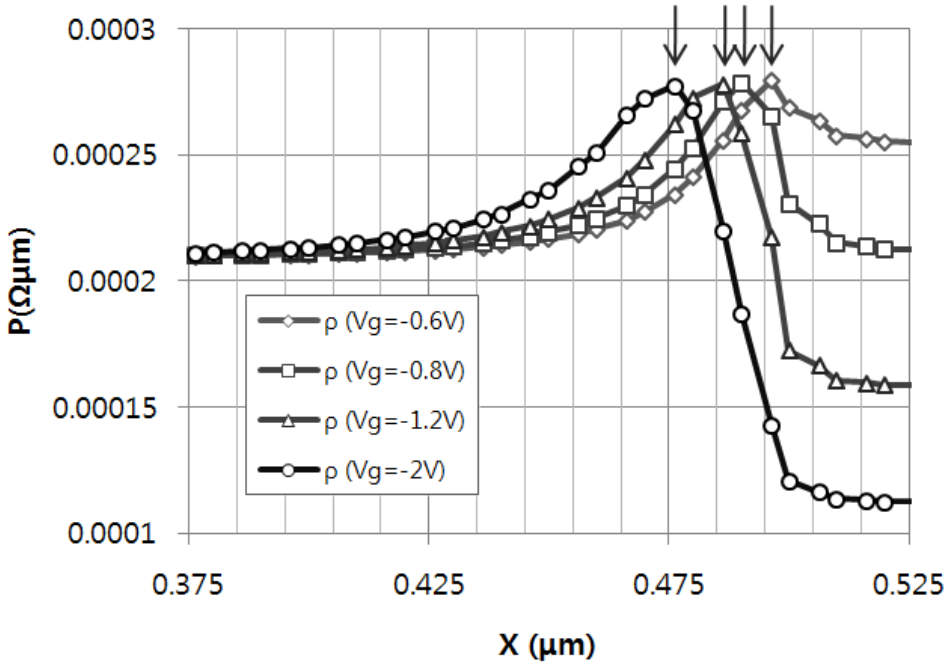


Figure 2.7. The maximum resistivity peak shifts with V_{tg} change. Larger V_{tg} pushes the position of the peak far from the gate edge

2.3.3. Extracting p-n Resistance from Experimental Data

We have extracted the additional p-n resistance ΔR from experimental results for comparison with the analysis. Figure 2.8 (a) shows reported measurements of drain current vs gate voltage for a FET fabricated with exfoliated graphene [3]. The effective resistance V_d/I_d contains components associated with channel resistance, contact and gap resistances and (for appropriate bias) the p-n junction resistances on both sides of the channel. We plot V_d/I_d vs. $1/|V_{tg}-V_{Dirac}|$ for the two branches (with V_{tg} above and below the Dirac point), as shown in figure 2.8 (b). It is expected that the channel resistances extrapolate to zero for $1/|V_{tg}-V_{Dirac}|=0$, and the contact gap resistances should be similar for the two branches. Thus the difference in y-intercepts for the two curves corresponds to twice the p-n junction resistance. Therefore, the p-n resistance for 1 μm width is ΔR =

[Y_{int}(npn) - Y_{int}(nnn)] * W/2, where Y_{int}(npn) and Y_{int}(nnn) are y-intercepts of the corresponding curves, and W is the width of the FET. Values of ΔR of order 450 Ωμm were extracted from FET results reported in [3] (based on graphene liftoff techniques). We have also extracted experimental values from FETs fabricated with epitaxial graphene produced by sublimation on SiC substrates. These FETs typically have V_{Dirac} values that are below zero, which is believed to be associated with n-type doping of the graphene from the SiC sublimation process. Unless the FET gate is self-aligned with the contacts, there is an n-type gap between contacts and the channel region, and p-n junctions are formed for V_{tg} values below V_{Dirac}. Our measurement of epitaxial graphene FETs fabricated on SiC substrates [7] gives resistance of 620 Ωum. Both results are in reasonable agreement with the simulations.

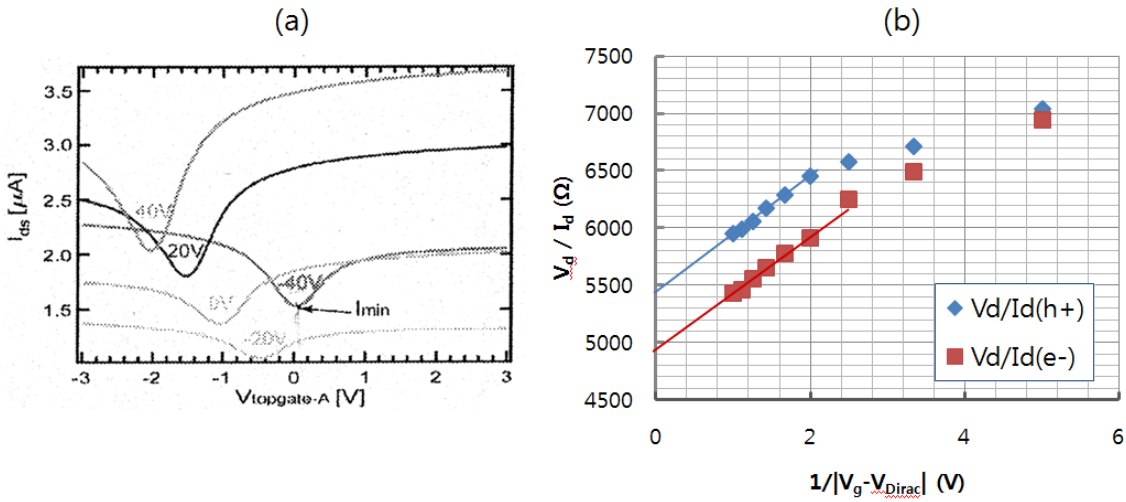


Figure 2.8. (a) A measured example of drain current transfer characteristics [3]. (b) Extracting ΔR from V_d/I_d vs. $1/|V_{tg}-V_{Dirac}|$ plot.

2.3.4. Analytical model for the p-n junction

To further characterize the added resistance we developed an analytical model for the p-n junction, given in the following:

$$E_d = E_{do} - F_c x \qquad (2.1)$$

$$n + p = A + B(E_f - E_d)^2 \qquad (2.2)$$

$$J = q(n+p)\mu \, dE_f/dx \qquad (2.3)$$

The spatial variation of the Dirac energy E_d of the graphene was assumed follow to equation (2.1) where E_{do} is a reference energy at the position of the p-n junction (x=0), and F_c is a constant electric field assumed to be established by the external structure (such as a gate fringing field). The carrier density of single layer graphene varies spatially according to the position of a quasi- fermi level E_f (assumed to be equal for electrons and holes) relative to E_d, following the approximate formula of equation (2.2). Here A = 1.6e11 cm^{-2} and B=6.5e13 $cm^{-2}eV^{-2}$ were chosen to represent single layer graphene at room temperature. The net current flow J associated with drift and diffusion is expressed in equation (2.3). Equations (2.1-2.3) were solved numerically using Matlab, for various assumptions of μ vs n, p. A representative profile of E_f vs x is shown in Figure 2.9. The E_f vs x profiles show an overall change across the junction that can be associated with the p-n junction voltage drop. Figure 2.10 shows the computed p-n junction resistance varies with current density for a range of different values of junction electric field (computed for peak carrier mobility=10,000 $cm^2/Vsec$).

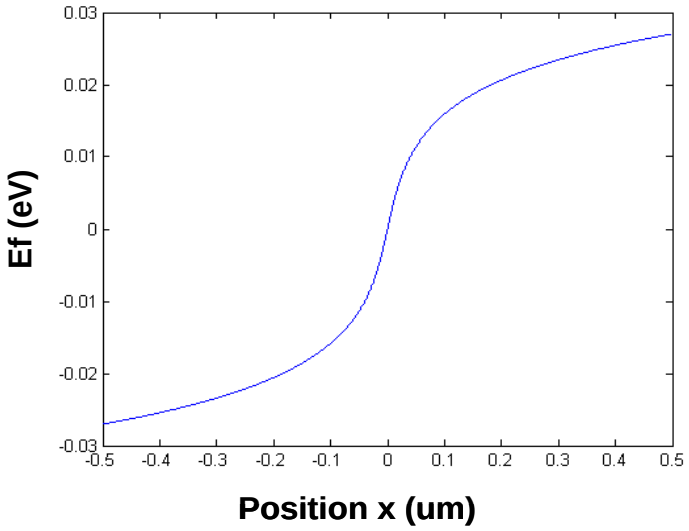


Figure 2.9. Calculated spatial variation of carrier quasi-fermi level across the p-n junction.

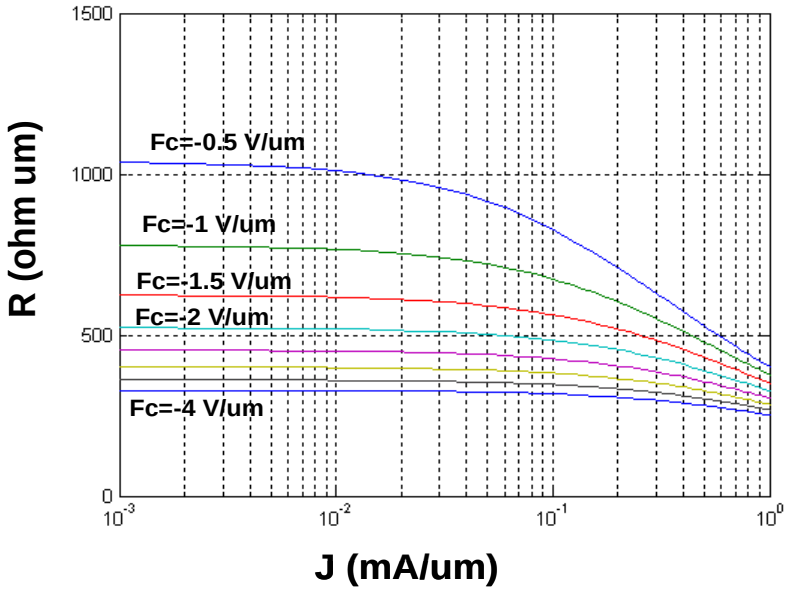


Figure 2.10. p-n junction resistance calculated from analytical model vs junction current, for different values of electric field F_c.

2.4. Summary: Graphene p-n Junction

An analysis of the additional resistance of p-n transition regions in graphene FETs based on a classical approach was presented. We obtained carrier distributions and calculated resistivity from a two dimensional device simulator. The npn structure showed a resistivity peak at the junction which is not shown in a comparably doped nnn structure. The p-n resistance is estimated by integrating the resistivity difference between n-n and n-p junction. The gate bias controls resistivity peak height and width, which determine the resistance. We compared our simulation results with extracted p-n resistance from measurement data, and showed that the results were of comparable magnitude.

2.5. Challenges to improve contact resistance of graphene-metal interface

As graphene devices are increasingly developed, the metal-graphene contact has acquired an important role. It is because recently reported contact resistances are not good enough to maintain the intrinsic advantages of graphene in scaled devices. There have been several approaches to overcome this problem. Extensive cleaning has been performed often [8], and sacrificial layer has used to keep the interface clean [9]. PSU group reported a partial damaged graphene by mild O_2 etching to increase the chance of conduction between graphene and metal [10]. One of possible way would be utilizing a work function difference between graphene and metals to result an effective doping effect.

2.6. Doping on graphene by metal contact and the Charge Transfer Region

2.6.1. Effective Doping on Graphene by Workfunction Difference of Contact

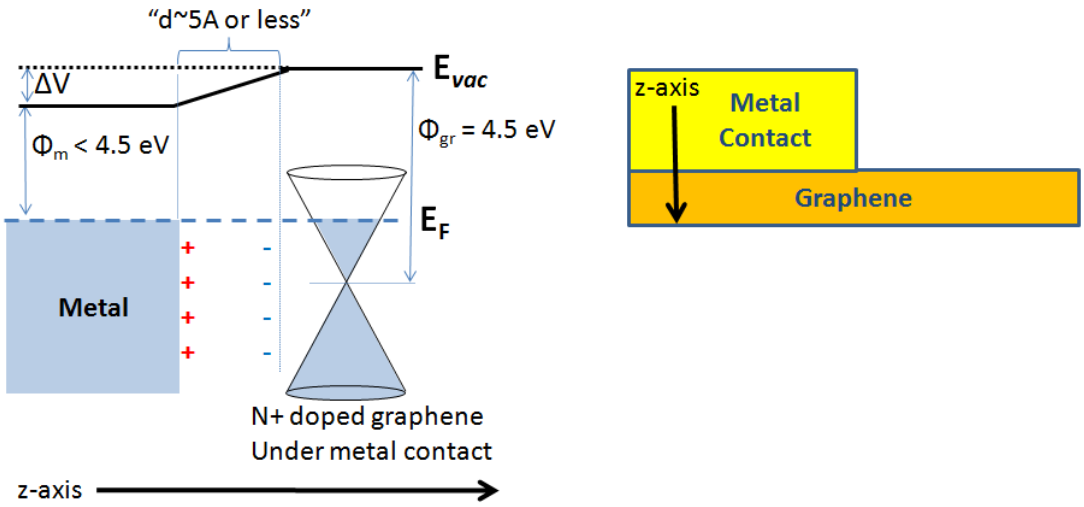


Figure 2.11. Charge transfer occurs between graphene and metal contact as a result of work function difference and small density of states of graphene.

It is known that a metal on graphene can provide a strong doping effect associated with its work function difference and graphene's small density of states [10, 11]. In Figure 2.11, the charge transfer of vertically layered graphene and metal is described for n-type doping. When there is a difference between Fermi energy of graphene and the work function of metal, charges are transferred to have a balanced, flat Fermi energy of graphene aligned with the top of occupied electron level of metal. Since the density of state of metal is extremely large compared with that of graphene, energy shift of metal is negligible and only graphene band is shifted from an equilibrium state (un-affected by metal contact). Charge transfer between graphene and metal can effectively dope the graphene film, however, it can also deplete or change the polarity of graphene which depends on the combination of metal work function and the initial doping level of

graphene. For example, Ni contact tends to apply a p-type doping to graphene, therefore if Ni meets epitaxial graphene on SiC substrate (known to be n-type), it is possible to have a depleted region at the metal contact, or even p-doped graphene contact.

2.6.2. Lateral Charge Transfer Region Formation

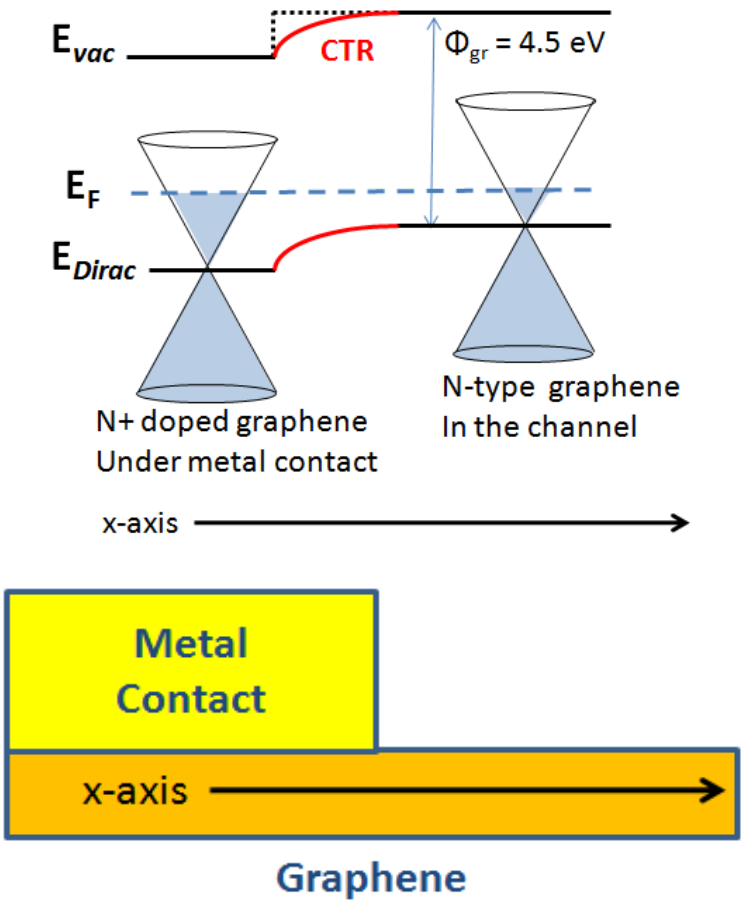


Figure 2.12. Lateral Charge transfer region formation at high-doped graphene and low-doped graphene junction. Potential and carrier density gradually change to equilibrium states.

When the carrier densities of the graphene channel and the metal-covered graphene are different, a charge transfer region (CTR) near the contact edge is formed [12, 13], in which the potential and carrier density gradually change to their equilibrium state. In particular, Figure 2.12 displays a CTR formed betweenn n+ doped contact region and n-type channel. In following sections, we investigate various factors which can affect the CTR length, and the impacts of CTR on contact resistance measurement.

2.7. Two-Dimensional Simulation of CTR

2.7.1. Theory and Simulation Method

Graphene "doping" by the contact metal and the charge transfer region are simulated with a custom-written 2-D Poisson solver. We have studied epitaxial graphene on SiC substrate, which is n-type due to the doping effect from the substrate, with a sheet carrier density N_s in the range of $2 \cdot 10^{12} \sim 1 \cdot 10^{13}$ cm^{-2} [7]. In the simulation, the density of states and carrier density calculations are modified to account for single layer graphene. Mobility and sheet resistance of graphene was applied as μ=1,137 cm^2/Vs and R_{sh}=2,805 Ω/□ respectively, following the measurement result reported in [7]. Zero bias was applied as a boundary condition ($V_s=V_g=V_b=0$), with E_f=0 eV everywhere. The simulated structure (Figure. 2 (a)) has elongated metal region and channel length to minimize edge or boundary effects. The device structure can have top gate metal as well, howerver it is removed in figure ss intentionally to investigate the impact of source (or drain) metal contact on CTR.

When the work function (Φ_G) of graphene (energy difference between vacuum level and the Dirac point) is taken to be 4.5 eV [8], the work function difference

($\Delta\Phi=\Phi_G-\Phi_M$) with a Titanium contact will be ~0.15 eV for an ideal contact, and ~0.34 eV for the chemisorbed case [14], which correspond with additional electron doping of ~$2\bullet10^{12}$ cm^{-2} and ~$8\bullet10^{12}$ cm^{-2}, respectively. It should be noted the effective 'doping' is from balancing the metal work function level and Fermi energy of graphene, which is related to the initial doping state. In case of $N_s=2\bullet10^{12}$ cm^{-2} and $\Delta\Phi=0.15eV$, the amount of additional doping will be small because graphene under the contact metal already has certain amount of doping and $\Delta\Phi$ is not large enough to add significant doping to graphene.

(a)

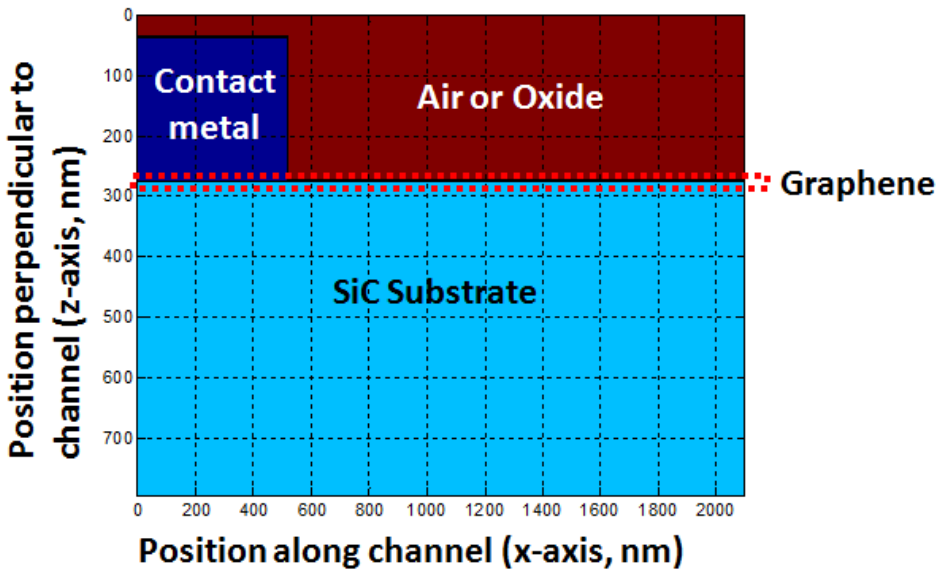


Figure 2.13. (a) Metal-graphene structure simulated by 2-D Poisson solver.

(b)

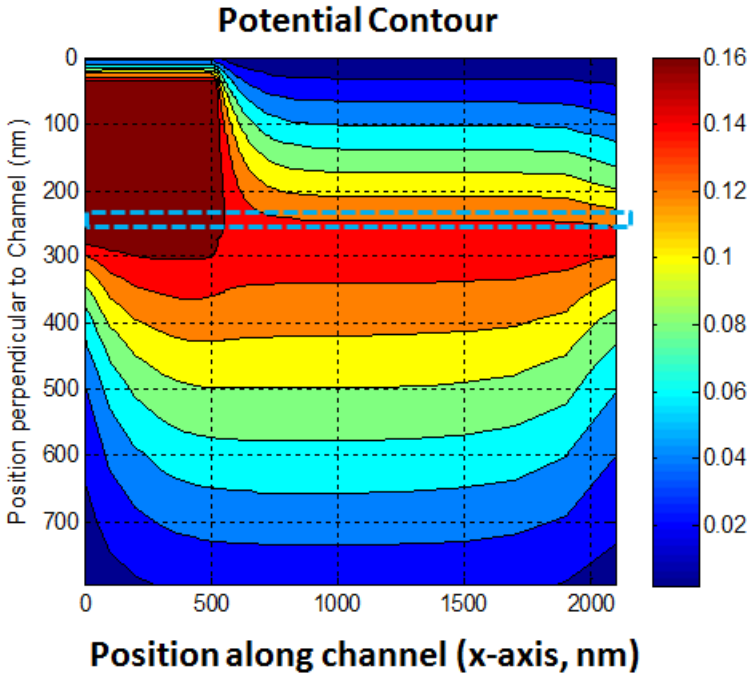


Figure 2.13. (continued) (b) Representative potential distribution. Graphene area is indicated by blue dashed box.

Gradual change of carrier density is shown in Figure 2.14, which indicates about 7 nm and 50 nm of CTR, depending on work function of contact. Since there is no clear cut of exact length of gradual charge transfer, here we define CTR length as the point where $N_s=1.05 \bullet N_{so}$ (5% larger than equilibrium charge density of graphene), where N_{so} is equilibrium sheet charge density in the middle of channel. When the difference in charge density is larger, more distance is needed to reach the equilibrium density. Therefore, more work function difference $\Delta\Phi$ extends CTR length.

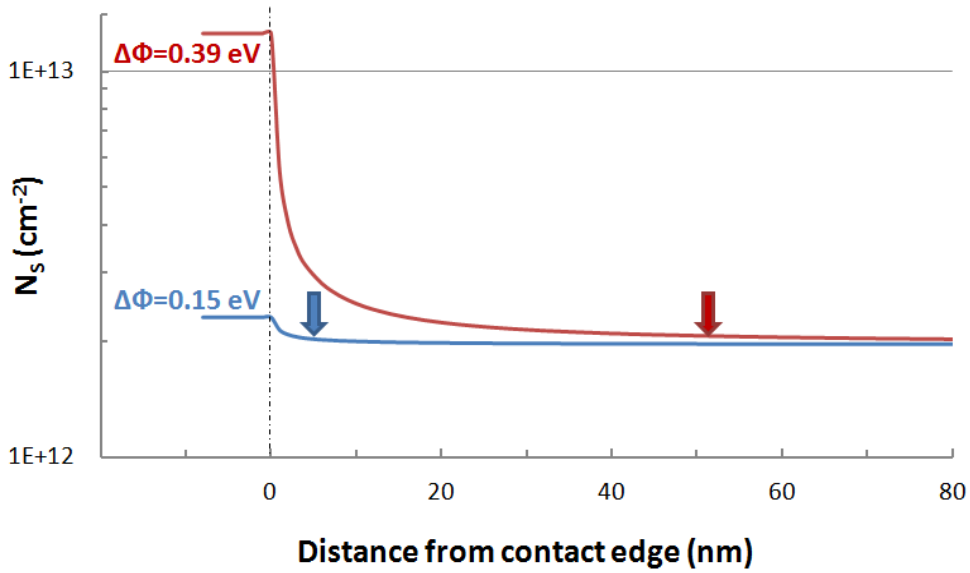


Figure 2.14. Representative graphene sheet charge density vs distance near the metal contact for unbiased, $N_S=2\bullet10^{12}$ cm^{-2}, and $\Delta\Phi=0.34$ eV. Arrows are indicating the end point of CTR with emphasis on the impact on sheet resistance.

2.7.2. Device Parameters Influencing CTR Lengths

Charge transfer region is formed laterally between graphene channel and metal-doped graphene. As the doping of graphene under the metal contact is defined by initial graphene doping and metal-graphene work function difference, charge transfer length is also heavily affected by same factors. In figure 2.15 (a), CTR length versus work function difference and initial graphene charge density is described. CTR extends as $\Delta\Phi$ ($=\Phi_G-\Phi_M$) increases for weak n-type graphene film ($N_{so}=1\bullet10^{12}$ cm^{-2}) and n-type doping metal case (metal work function is less than 4.5 eV). Thickness of metal contact (T_{metal}) is 20 nm, and relative dielectric constant (ε_{ox}) of top oxide is 3.9. 0.15 eV of Fermi energy shift is equivalent to $2\bullet10^{12}$ cm^{-2} electro static doping, therefore there will be a negligible additional doping to graphene and CTR length is almost 0 nm. When we fix the metal work function and varies the initial graphene doping (N_{SO}), simulated CTR length

extends more than 250 nm for $\Delta\Phi$=0.39 eV and N_{SO} ~$2\bullet10^{11}$ cm^{-2} which is about room temperature intrinsic charge density (Figure 2.15 (b)).

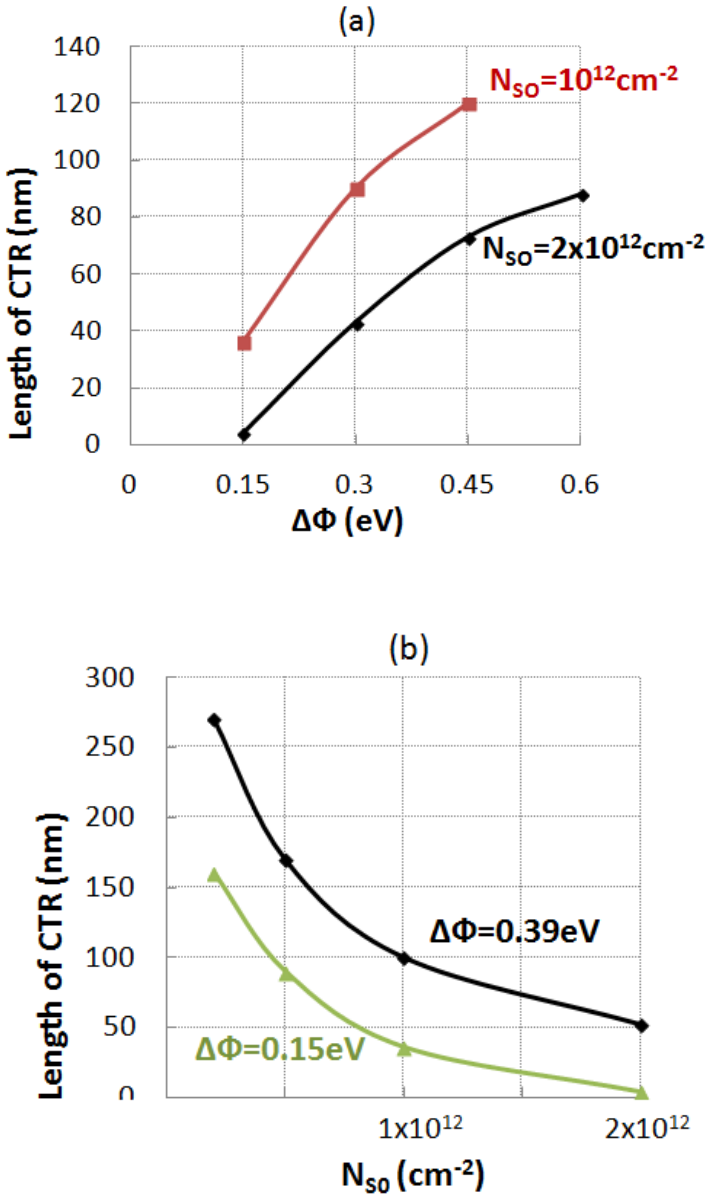


Figure 2.15. (a) Computed dependence of CTR length on Metal-graphene workfunction difference $\Delta\Phi=\Phi_G-\Phi_M$ (T_{metal}=20 nm, ε_{ox}=3.9). (b) CTR length dependency on sheet charge density of graphene (T_{metal}=20 nm, ε_{ox}=3.9)

Although $\Delta\Phi$, N_{so} shows dominant impact on CTR length, fringing electric field effect cannot be ignored. Like the schematic in figure 2.16, electric field from the metal sidewall will affect the potential and charge distribution of vicinity. Fringing field from metal is controlled by metal thickness and top oxide dielectric constant.

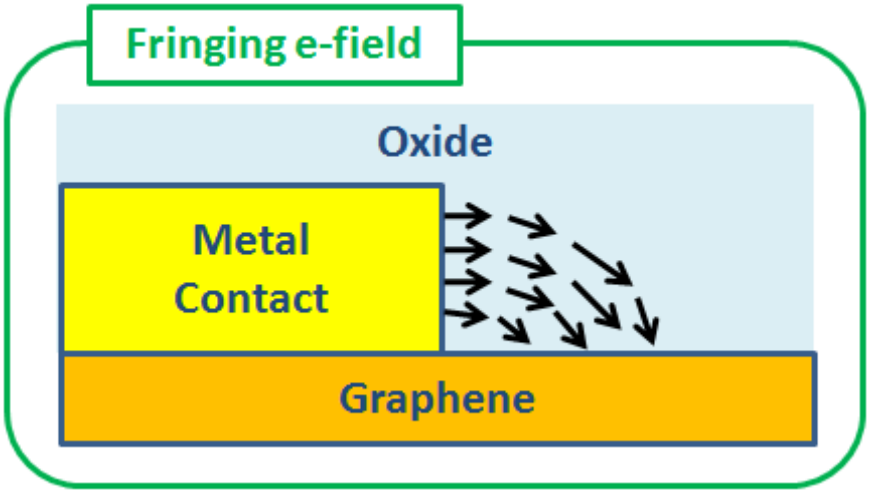


Figure 2.16. Influence of fringing electric field on graphene electrostatics and charge transfer region

Figure 2.17 (a) shows the CTR length (L_{CTR}) change with the height (thickness) of metal contact, when $\Delta\Phi$=0.34eV, $N_{SO}=2\bullet10^{12}$ cm^{-2} and ε_{ox} is 3.9. L_{CTR} increases with thicker metal (more e-field from sidewall), and eventually shows a saturation behavior over 100 nm of metal height. Fringing e-field from sidewall of higher than 100 nm contributes lesser due to the increased distance from the graphene surface. Fringing field effect is more effective through dielectric with higher permittivity; figure 2.17 (b) displays that CTR length increases about 50% when top dielectric changes from SiO_2 (ε=3.9) to Al_2O_3 (ε=9) when $\Delta\Phi$=0.15 eV, T_{metal}=20 nm, $N_{SO}=2\bullet10^{12}$ cm^{-2}.

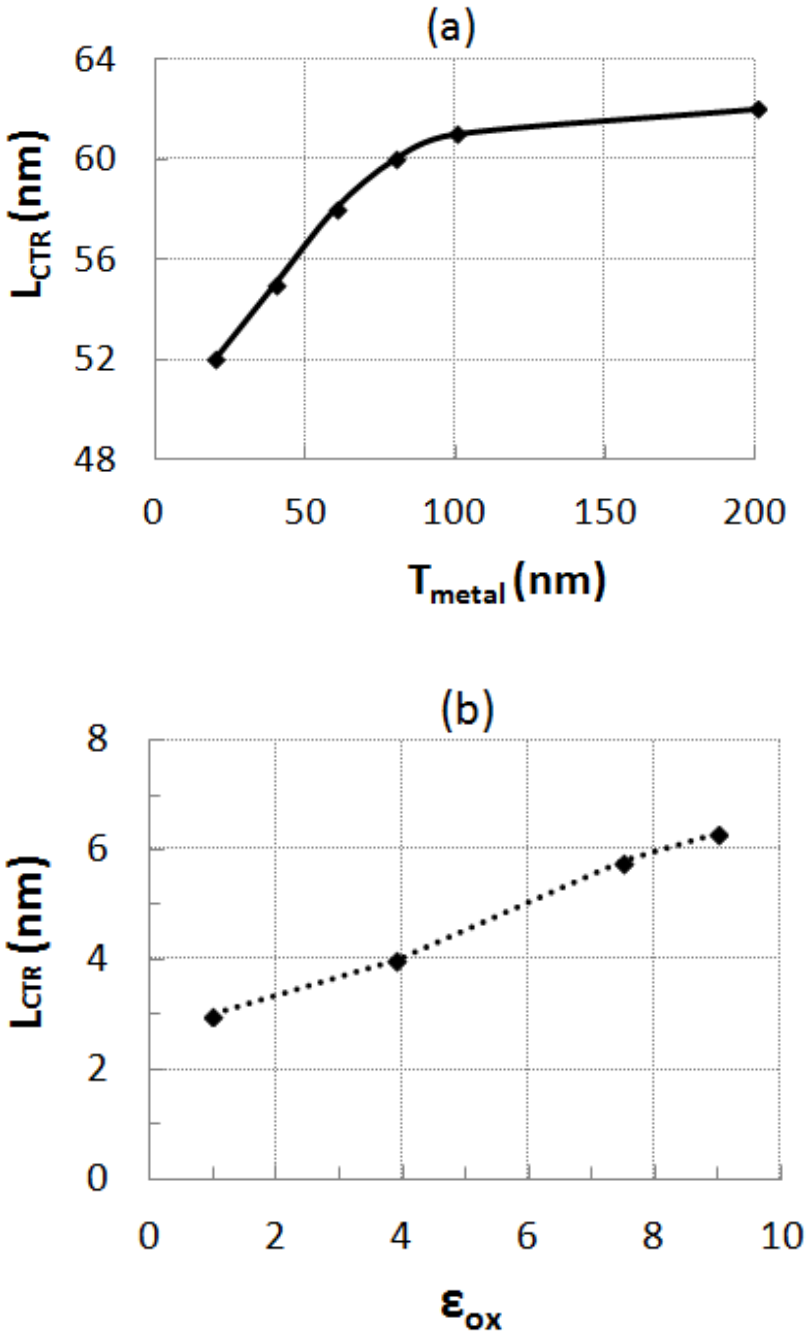


Figure 2.17. (a) Computed dependence of CTR length on metal thickness ($\Delta\Phi$=0.34eV, N_{SO}=2•10^{12} cm^{-2}). (b) CTR length vs. top oxide dielectric constant ($\Delta\Phi$=0.15eV, T_{metal}=20nm, N_{SO}=2•10^{12} cm^{-2})

2.8. Impact of CTR on Device Characteristics

2.8.1. Contact Resistance Measurement: Transfer Length Method

Transfer length method (TLM) is a common way to estimate the contact resistance of metal on semiconductor [15]. Typical TLM sample requires a bar-shaped semiconductor film on insulating substrate, with multiple metal contacts of same size. Spacing of metal contact should vary. One can use probes to measure the total resistance between two neighbor metal contact sets. Total resistance measured ($R_{measured}$) between two contacts will be $\rho_{sh}\bullet(L/W) + 2\bullet R_c$, where ρ_{sh} is sheet resistance of semiconductor, L is length between contacts, W is width of semiconductor and R_c is contact resistance (Ω μm). Figure 2.18 shows schematic of TLM measurement and example of measured result. Total resistance vs. contact spacing curve will have a slope of ρ_{sh} /W, and one can extract the contact resistance from y-intercept which is $2\bullet R_c$ in the L=0 limit.

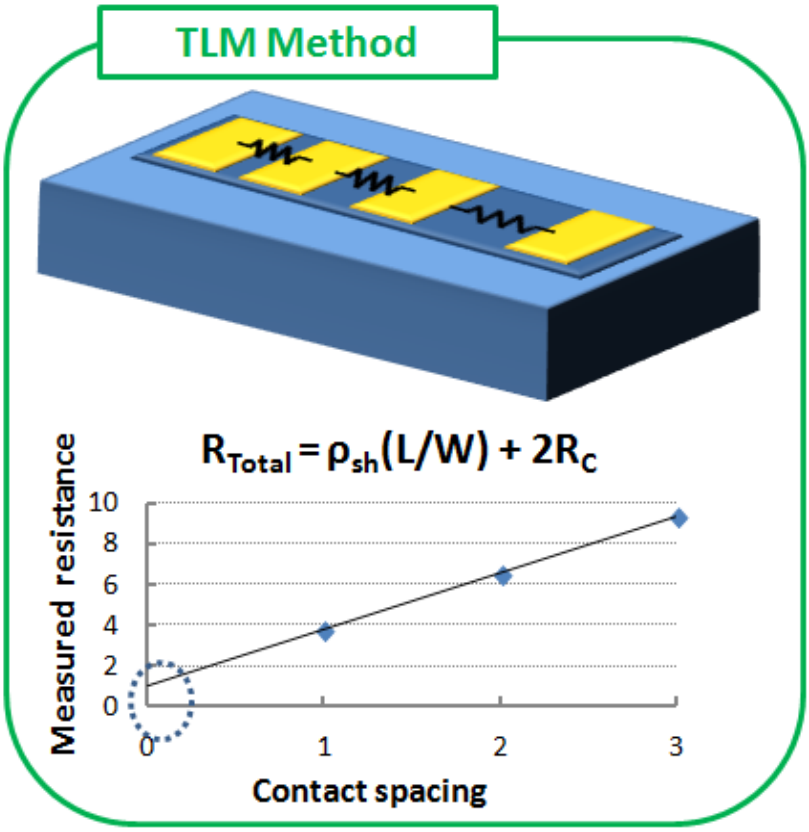


Figure 2.18. Schematic of TLM method and typical measured result of total resistance vs. contact spacing curve. Contact resistance R_c will be half of the y-intercept value.

When there is substantial amount of additional doping added to graphene contact region, a low resistance CTR is formed at the contact edge (Figure 2.19). High doped region would help to lower the contact resistance, however CTR will make it difficult to estimate the exact contact resistance. Since the sheet resistance is changing between the contacts, conventional TLM method with assumption of constant ρ_{sh} will have errors in the measurement and analysis. n+ doping region and CTR can reduce the total resistance of n-type graphene channel. In this case, it causes an underestimation of contact resistance (R_c) in the transfer length method (TLM) measurement.

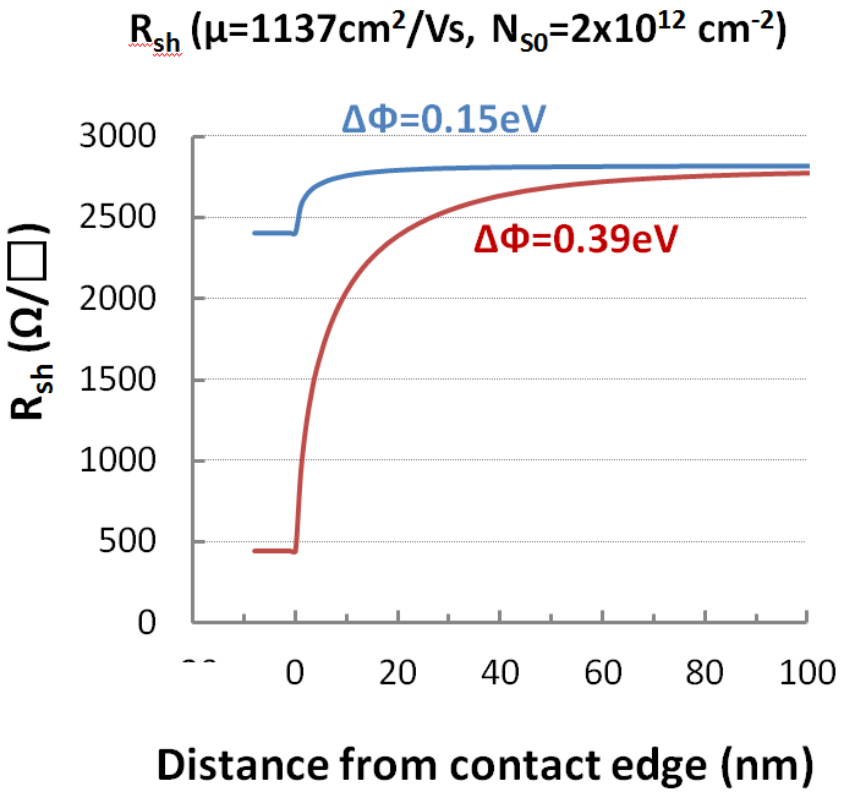


Figure 2.19. Representative graphene sheet resistance vs distance near the metal contact for unbiased, N_s=2e12cm^{-2}, and ΔΦ=0.15, 0.34eV.

Considering the parameters of the TLM measurement, only known variables are L and W. However, without knowing the R_c or effective ρ_{sh} with CTR, we can simulate [R_{Total}-2•R_c]. For a uniform ρ_{sh} along the channel between contacts (no CTR), extrapolated y-intercept will meet the origin. When there is a low resistance CTR, y-intercept of [R_{Total}-2•R_c] will go below zero and this causes the Rc underestimation of TLM measurement (Figure 2.20)

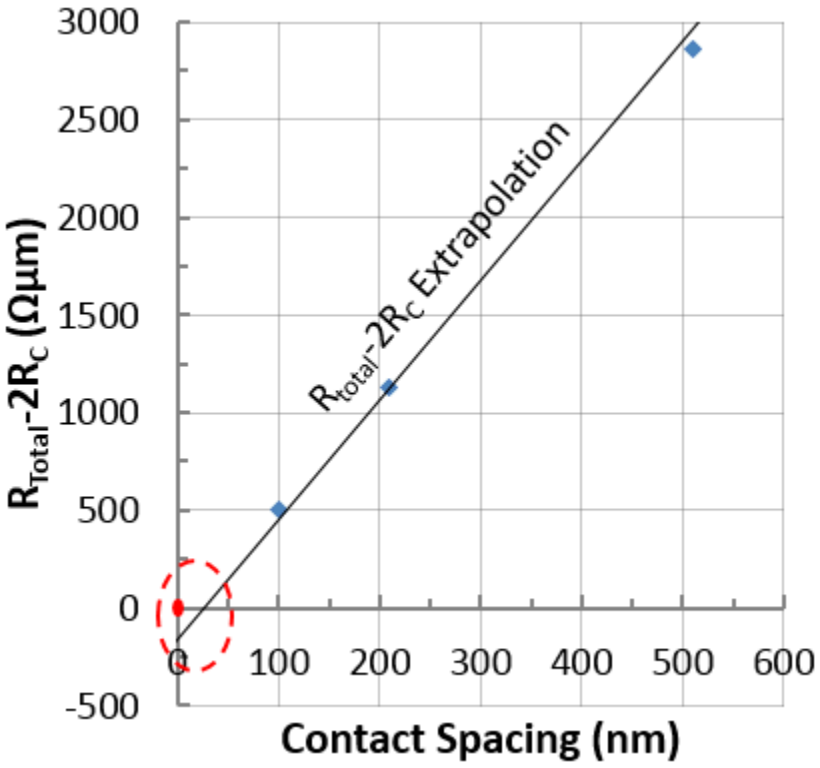
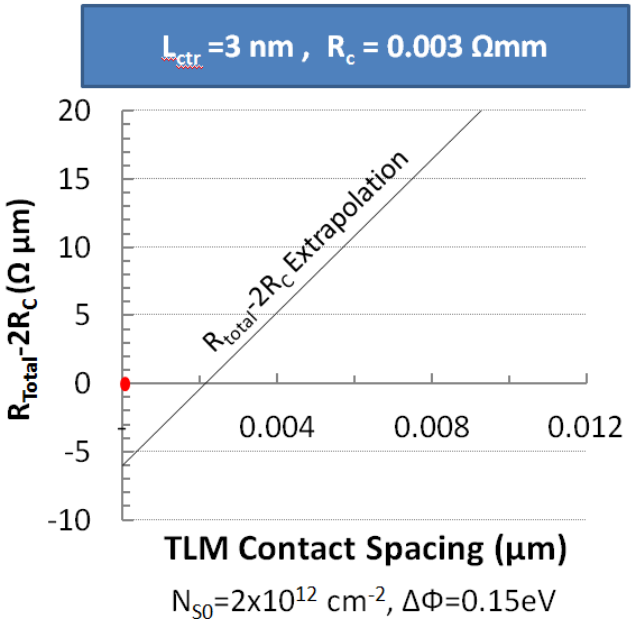


Figure 2.20. Simulated dependence of measured resistance [R_{Total}-2•R_c] vs. TLM contact spacing, showing negative intercept

When effective doping from the metal-graphene charge transfer is comparable to initial graphene doping (equilibrium charge density of graphene channel area), then resistivity of CTR and mid-channel will be similar ($\rho_{CTR}=\rho_{channel}$). This is essentialy same with uniform channel material between metal contacts. Figure 2.21 (a) shows a case of contact metal of $\Delta\Phi$=0.15eV on $N_{S0}=2\bullet10^{12}$ cm^{-2} which results a short charge transfer region and insignificant ~3Ωμm of contact resistance measurement error. When the CTR is larger and low resistivity region is extended, it can have more influence on TLM measurement. In case of figure 2.21 (b), $\Delta\Phi$=0.3eV on $N_{S0}=2\bullet10^{12}$ cm^{-2} graphene film forms 90 nm of CTR and ~84 Ωμm of underestimation of contact resistance is expected.

(a)



(b)

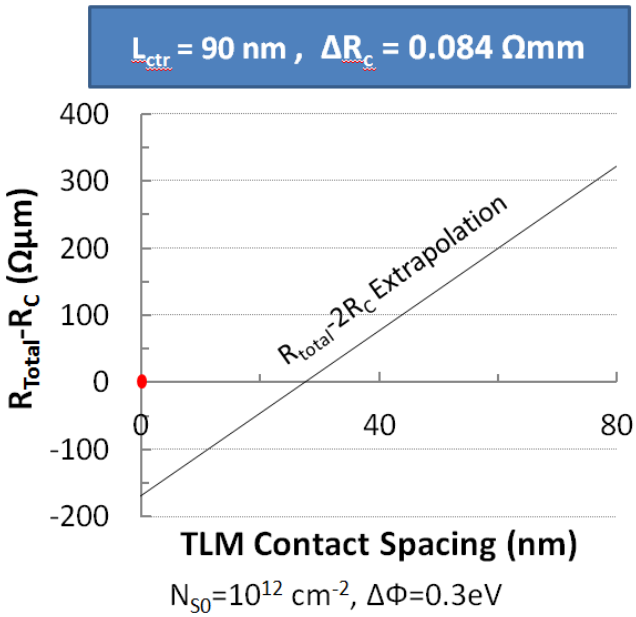


Figure 2.21 Simulated TLM measurement in terms of [R_{Total}-2•R_c] vs. TLM contact spacing, for cases of (a) ΔΦ=0.15eV on N_{S0}=2•10^{12} cm^{-2}, (b) ΔΦ=0.3eV on N_{S0}=2•10^{12} cm^{-2}

2.8.2. Formation of p-n Junction due to Metal-Graphene Effective Doping Effect

On the other hand, p-type graphene with n-type contact will form an additional p-n junction at the contact edge (Figure x-a). As discussed in Chapter 2-xx, it will provide a p-n junction resistance up to 500 Ωμm [16] and effective R_c will increase. In sheet charge density vs. position along the channel (Figure x-b), depletion of carriers at the p-n transition is shown for this case. Carrier depletion due to p-n junction is relevant to the peak of of local resistivity of grapheme-contact edge area (Figure x-c).

(a)

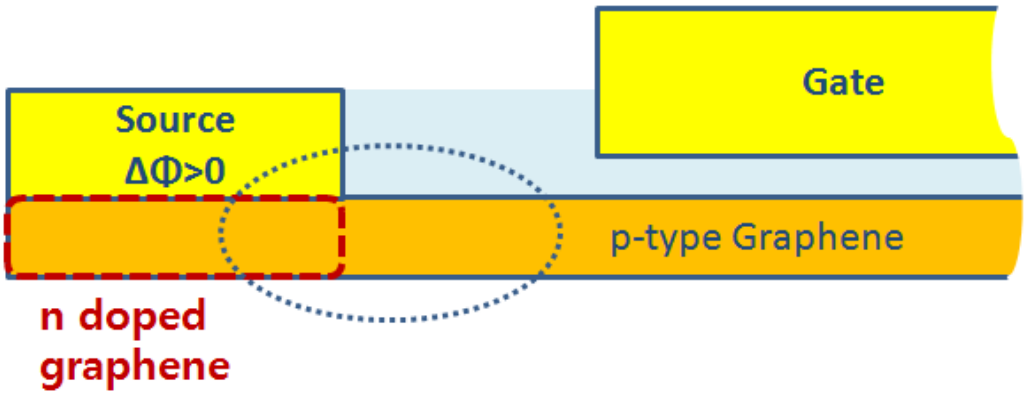
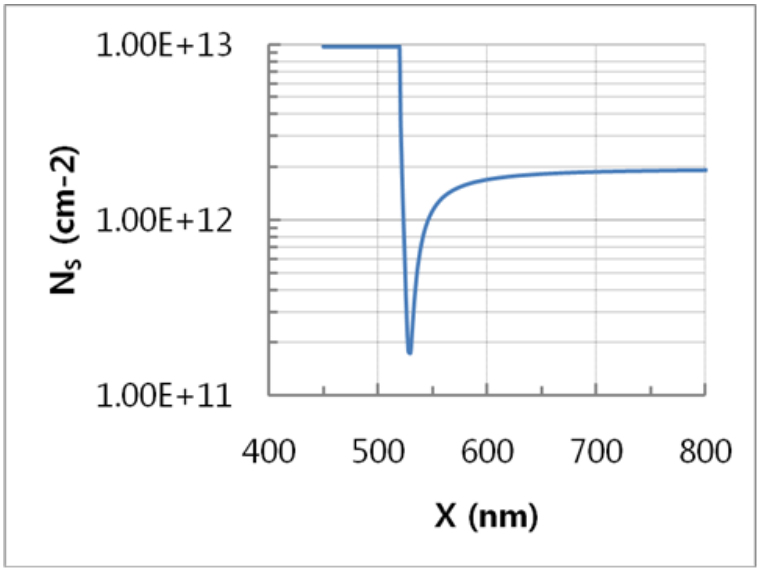


Figure 2.22. (a) A schematic device structure of n-type doping on p-type graphene film.

(b)



(c)

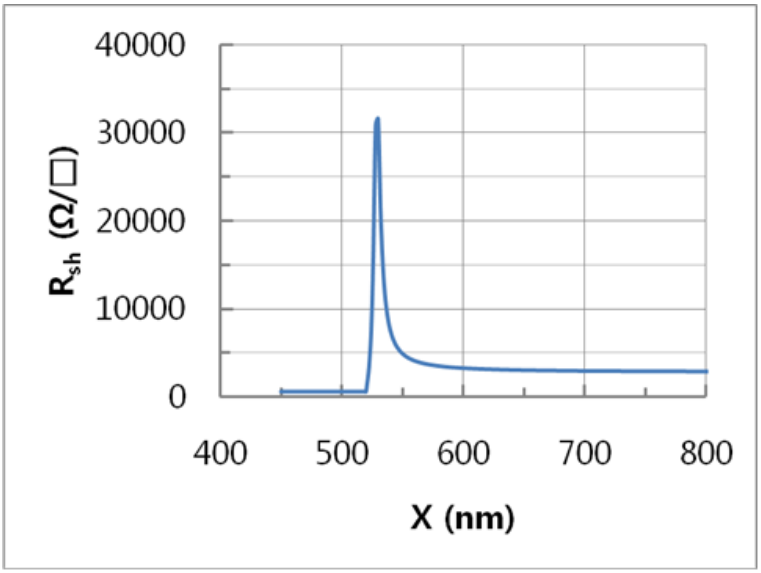


Figure 2.22. (continued) (b) Simulated sheet charge density profile for case of n-type contact and p-type channel. (c) p-n junction shows carrier depletion which causes higher resistivity.

2.8.3. CTR of Highly Scaled Devices and I_{on}/I_{off} Ratio

The effect of CTR on the channel of graphene FETs will be stronger in highly scaled graphene devices where the source to drain length is comparable to the length of CTR. As we have discussed in previous chapters, impact of CTR is emphasized when carrier density of channel is small. CTR is also a regional effect near at the contact edge, however, it has finite length (order of several tens of nanometers) under influence. Regarding these facts, CTR could be a serious concern for off-state in highly scaled devices. Figure 23 shows a schematic of self-aligned graphene FET with channel length of 100 nm and R_{sh} of various situations. Assuming an equilibrium state with small V_d, channel resistance and I_{on}/I_{off} ratio can be estimated by resistivity along the channel. CTR length is reduced and it has a little effect for 'on' state, because the Ns is high (discussed in chapter 2.7.2). However, when the FET is biased to ‘off’ state, carrier density of channel is reduced to intrinsic level, and CTR length and effect increases. In sheet resistance plot in figure 23, resistance of the channel for ‘off’ state is reduced to ~25% due to charge transfer from source and drain contact. Consequently, the I_{on}/I_{off} is degraded in the same order with Roff level. This would be only valid estimation for a small V_d, and difference between ideal case and CTR affected case will be smaller for large V_d. However, it is obvious that short channel self-aligned GFET will loose certain amount of channel control due to the CTR effects.

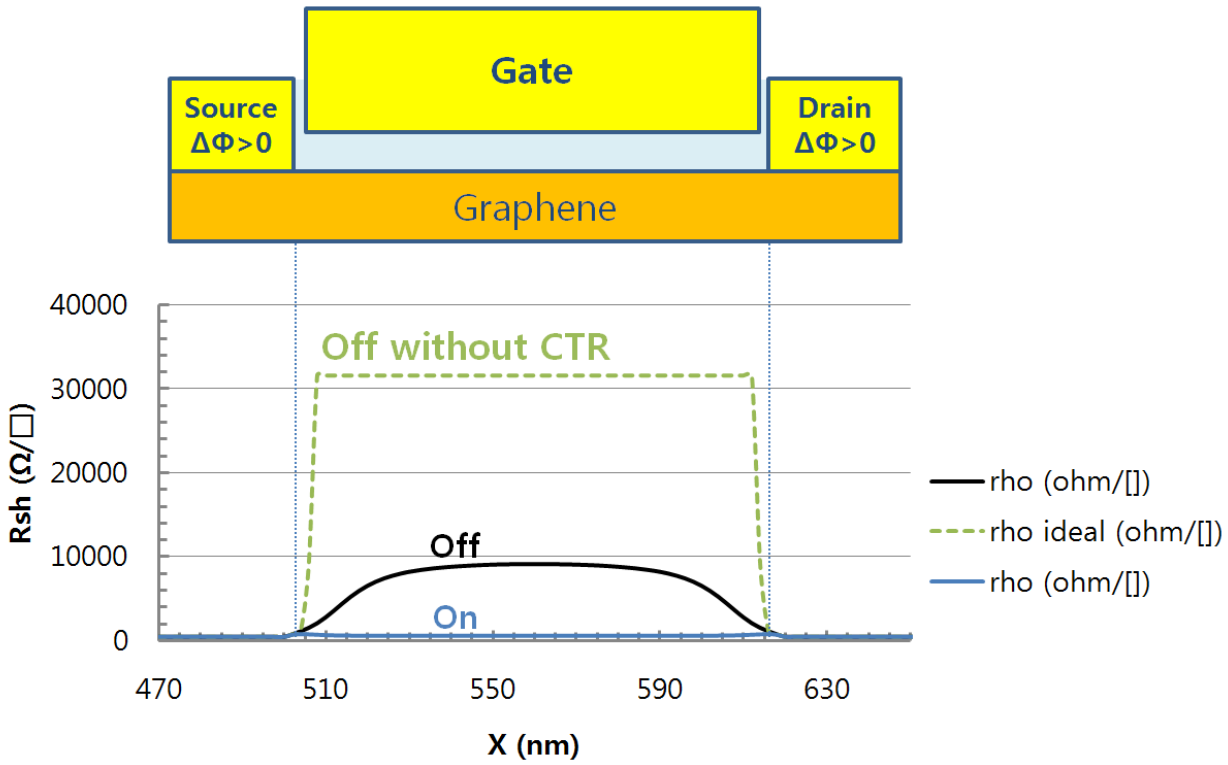


Figure 2.23. A schematic of self-aligned graphene FET with channel length of 100 nm and R_{sh} of on, off, off without CTR cases.

2.9. Summary: Charge Transfer Region of at Graphene-Metal Contact

Charge transfer region at the graphene-metal contact edge was investigated with 2-D Poisson solver. Effective doping was applied due to graphene-metal workfunction difference and small density of states of graphene. CTR between doped contact region and equilibrium state channel is controlled by metal workfunction, charge density of graphene film, metal thickness and top oxide dielectric constant. CTR can induce errors in the contact resistance measurement by TLM method and degrade I_{on}/I_{off} ratio of scaled GFETs.

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2.10. References

[1] Lin YM, Jenkins KA, Valdes-Garcia A, Small JP, Farmer DB, Avouris P. Operation of graphene transistors at gigahertz frequencies. Nano letters. 2008 Dec 19;9 (1):422-6.

[2] Kedzierski J, Hsu PL, Healey P, Wyatt PW, Keast CL, Sprinkle M, Berger C, De Heer WA. Epitaxial graphene transistors on SiC substrates. Electron Devices, IEEE Transactions on. 2008 Aug;55 (8):2078-85.

[3] Z. Chen and J. Appenzeller, "Gate modulation of graphene contacts - on the scaling of graphene FETs," *2009 Symposium on VLSI Technology*, Honolulu, HI, 2009, pp. 128-129.

[4] B. Huard, J. A. Sulpizio, N. Stander, K. Todd, B. Yang, and D. Goldhaber-Gordon, "Transport Measurements Across a Tunable Potential Barrier in Graphene," Phys. Rev. Lett. **98**, (2007) 236803

[5] L. M. Zhang and M. M. Fogler, "Nonlinear Screening and Ballistic Transport in a Graphene p−n Junction," Phys. Rev. Lett. 100, (2008) 116804

[6] T. Low, S. Hong, J. Appenzeller, S. Datta, and M. S. Lundstrom, "Conductance asymmetry of graphene p-n junction," IEEE Trans. Electron. Devices, vol. 56, no. 6, pp. 1292–1299, Jun. 2009

[7] J. S. Moon, D. Curtis, M. Hu, D. Wong, C. McGuire, P.M. Campbell, G. Jernigan, J.L. Tedesco, B. VanMil, R. Myers-Ward, and C. Eddy Jr, "Epitaxial-Graphene RF Field-Effect Transistors on Si-Face 6H-SiC Substrates," in IEEE Electron Device Letters, vol. 30, no. 6, pp. 650-652, June 2009

[8] W. Li, Y. Liang, D. Yu, L. Peng, K.P. Pernstich, T. Shen, A.H. Walker, G. Cheng, C.A. Hacker, C.A., Richter, and Q. Li, "Ultraviolet/ozone treatment to reduce metal-graphene contact resistance." Applied Physics Letters 102.18 (2013): 183110.

[9] A. Hsu, H. Wang, K. K. Kim, J. Kong and T. Palacios, "Impact of Graphene Interface Quality on Contact Resistance and RF Device Performance," in IEEE Electron Device Letters, vol. 32, no. 8, pp. 1008-1010, Aug. 2011.

[10] J. A. Robinson, M. LaBella, M. Zhu, M. Hollander, R. Kasarda, Z. Hughes, K. Trumbull, R. Cavalero, and D. Snyder, "Contacting graphene," Applied Physics Letters 98.5 (2011): 053103.

[11] G. Giovannetti, P.A. Khomyakov, G. Brocks, V.V. Karpan, J. Van den Brink, and P.J. Kelly, "Doping Graphene with Metal Contacts", Phys. Rev. Lett. vol. 101, 026803, July 2008.

[12] T. Mueller, F. Xia, M. Freitag, J. Tsang, and P. Avouris, "Role of contacts in graphene transistors: A scanning photocurrent study", Phys. Rev. B 79, 245430, June 2009.

[13] K. Nagashio, T. Nishimura, K. Kita, K. and A. Toriumi, "Metal/graphene contact as a performance Killer of ultra-high mobility graphene analysis of intrinsic mobility and contact resistance", Proc. IEDM. 2009. 5424297, Baltimore, Maryland, Dec. 2009

[14] P. A. Khomyakov, G. Giovannetti, P.C. Rusu, G.V. Brocks, J. Van den Brink, and P.J. Kelly, "First-principles study of the interaction and charge transfer between graphene and metals", Phys. Rev. B 79, 195425, Feb. 2009.

[15] Schroder, Dieter K. "Semiconductor material and device characterization." John Wiley & Sons, 2006.

[16] K Lee, L. Wang, P. Asbeck, J. Moon, "Analysis of Resistance Asymmetry Due to p-n Junctions in Graphene FETs", Mater. Res. Soc. Symp. Proc. Vol. 1259, S08-04, Apr. 2009.

Chapter 3

Numerical Study of Inhomogeneity Effects on Hall Measurements of Graphene Films

In this chapter, we discuss a two-dimensional model calculation of inhomogeneous graphene films which incorporates a random distribution of dopants (leading to electron and hole puddles) for analysis of Hall measurements. The model predicts significant effects of inhomogeneity on the Hall coefficient, which can lead to an understimate of carrier mobility. We investigate the effect of parameters including size of puddles, local charge density deviation, and device sizes. The inhomogeneity of epitaxial graphene generated by steps and terraces of SiC substrates is also discussed. The

simulation results quantify possible statistical errors in Hall mobility measurements, Dirac point estimation and non-uniformity of scaled devices over wafers.

3. 1. Introduction

In recent years, graphene has been highlighted as a candidate for next generation r.f. devices due to its outstanding intrinsic properties including very high electron and hole mobilities, and high carrier saturation velocities [1, 2]. To characterize graphene as a potential channel material for FETs, Hall measurements are often carried out to determine carrier mobility, as is common for other semiconducting materials. However, analysis of graphene Hall measurements should be performed with care, considering the possible simultaneous participation of both electrons and holes when the Fermi energy of graphene lies near the Dirac point. The need for ambipolar analysis of Hall measurement of graphene and other narrow band gap materials has been previously discussed [3]. Incorrect use of the simplified equation assuming a single dominant carrier leads to an over-estimate of the number of carriers and artificially reduces the calculated mobility of the film particularly near the Dirac point. In this paper, we highlight an additional concern for Hall analysis. Relatively slight amounts of inhomogeneity in the films can lead to participation of both electrons and holes in distinct regions of the device (rather than at the same location, as occurs under ambipolar conditions). In materials with large bandgaps, inhomogeneous doping with both donor-like and acceptor-like impurities generally leads to insulating materials, as well as the presence of considerable electric fields associated with depletion regions in the material. In graphene, because of rapid equilibration of electrons and holes, very low built-in potentials, and ready possibility of

tunneling between conduction and valence bands, the behavior is qualitatively different; films continue to conduct well, although their conductivity is degraded, and we show here that their mobility is significantly altered from simple expectations based on uniform material. The uniformity of devices fabricated in wafer scale are often limited by inhomogeneities [4, 5]. Although the quality of graphene films and process technologies have improved steadily, it is still very challenging to prepare uniform, defect free large areas of graphene [5, 6]. Even for the case of uniform graphene, in gated structures there are generally interface states and bulk oxide traps associated with the dielectrics, that cause localized variations in potential [7, 8]. One of the well-known phenomena is the appearance of electron-hole puddles when the graphene channel is biased near to Dirac point (V_{Dirac}). It is reported that one of the limits of graphene FETs like low I_{on}/I_{off} ratio becomes worse due to the puddles, [9, 10] and origin of puddles and its nature has been studied [7, 10-12]. However, only limited studies have been done of large area inhomogeneity of graphene and its impact on device characteristics such as carrier mobility measurement. Local inhomogeneity should be also considered to analyze the Hall measurement of graphene films. In this chapter, we will conduct numerical simulations of Hall measurement with randomly generated doping layers which describe the inhomogeneous graphene film.

3. 2. Sample Structure

The schematic geometry for Hall measurements in ambipolar materials such as graphene is presented in Figure 3.1. A longitudinal (x-directed) electric current density J_x is imposed in the rectangular sample, and a normal (z-directed) magnetic field B_z is

applied. Electrons and holes are deflected in the y- direction as shown in the diagram, until a y-directed electric field E_y is built up to counter their net lateral flow.

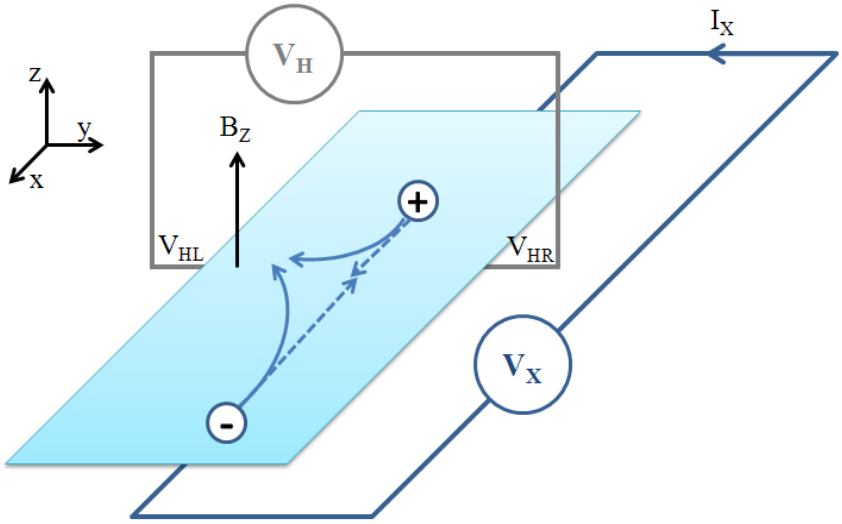


Figure 3.1. Schematic diagram of Hall measurement. Motions of both holes and electrons are indicated.

For experiments analyzed below, there is furthermore a gate contact overlaying the graphene, separated from it by a dielectric (such as SiO_2). The application of a gate voltage can alter the average number of carriers across the sample. The voltage V_x is assumed to be small enough that the carrier density induced by the gate is uniform across the sample.

3. 3. Ambipolar Hall Equations

The Hall coefficient resulting from the measurement is defined as,

$$R_H = \frac{E_y}{J_x \cdot B} \qquad (3.1)$$

For uniform material containing both electrons and holes, it is readily shown

$$R_H = \frac{\mu_p^{\,2} \cdot p - \mu_n^{\,2} \cdot n}{e\left(\mu_p + \mu_n\right)^2} \qquad (3.2)$$

Here E_y is induced electric field and J_x is longitudinal electric current density, B is magnetic field and *e* is the fundamental charge. n and p are electron and hole densities, while μ_n and μ_p are mobility of electron and hole, respectively.

Under common-place unipolar conditions, one has

$$R_H = -\frac{1}{e \cdot n} \qquad (3.3)$$

for n-type material and similarly for p material, $R_H = \frac{1}{e \cdot p}$. One can reduce (1) with both holes and electrons simultaneously conducting, assuming $\mu_n = \mu_p$.

$$R_H = \frac{(p-n)}{e \cdot (p+n)^2} \qquad (3.4)$$

The value of R_H from equation (4) is plotted in Figure 3-2 vs N_c, the carrier density in the material (=n+p under ambipolar conditions), which can be varied by application of the gate voltage. Here n and p are assumed to be in thermal equilibrium, and charge neutrality applies. The electron density of graphene can be expressed as,

$$n = \int_0^\infty \rho_{Gr}(E) \cdot f(E)\, dE \qquad (3.5)$$

$$\rho_{Gr}(E) = \frac{2}{\pi(\hbar \cdot v_F)^2} \cdot |E| \qquad (3.6)$$

$$f(E) = \frac{1}{1+e^{\frac{E-E_F}{kT}}} \qquad (3.7)$$

where ρ_{Gr} is density of states of graphene 2D sheet and f(E) is the Fermi-Dirac distribution function, ħ is the reduced Planck constant, v_F is Fermi velocity of electrons and holes of graphene ($1.06 \cdot 10^8$ cm/s), k is the Boltzmann constant and T is the absolute temperature. One can rewrite the equation for electron density associated with the Fermi energy (Dirac point as a reference energy).

$$n(E_F) = \frac{2}{\pi \cdot (\hbar \cdot v_F)^2} \cdot \int_0^\infty \frac{E}{1+e^{\frac{E-E_F}{kT}}}\, dE \qquad (3.8)$$

A similar equation applies for holes. Equation (3.4) and Figure 3.2 illustrate that if n~p under intrinsic conditions and $\mu_n \sim \mu_p$, then R_H vanishes, so that the estimated value

of carrier density becomes unrealistically high. If we denote the measured Hall mobility and carrier density based on single carrier assumption as $\mu_{measured}$ and $N_{measured}$, then we can calculate the true value of carrier density N_{true}, by using the proper Hall measurement equation. Figure 3.3 shows the relationship between $N_{measured}$ and N_{true} calculated from equations (3.3-3.8).

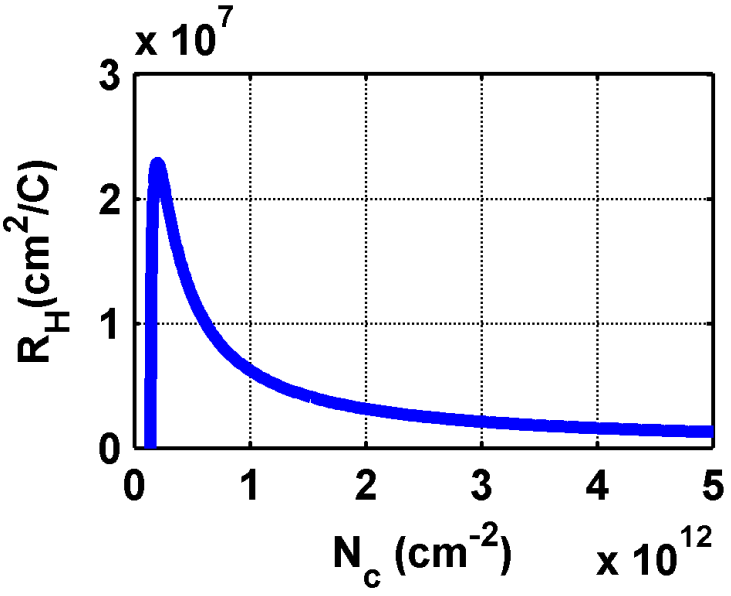


Figure 3.2. R_H vs N_c using ambipolar formula. R_H vanishes near Dirac point where n~p.

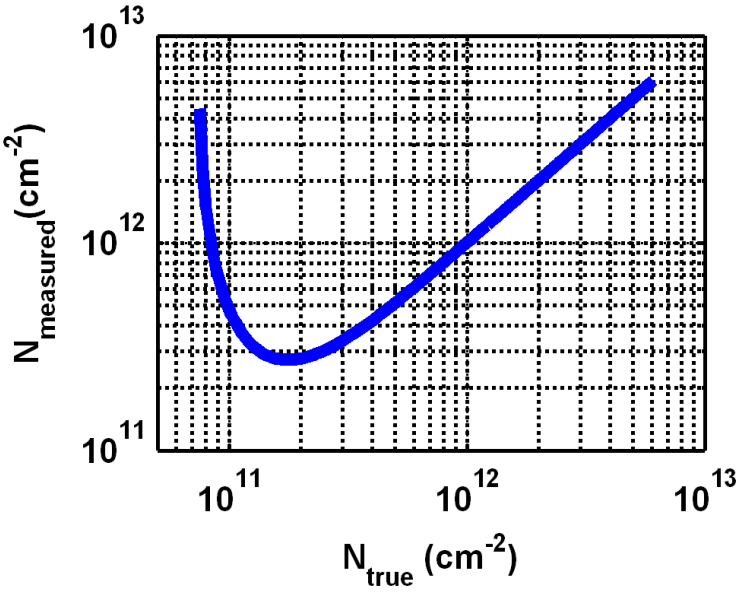


Figure 3.3. Relation between the extracted carrier density from single carrier Hall measurement ($N_{measured}$) of graphene and carrier density from ambipolar Hall equation (N_{true}). Single carrier Hall equation overestimates the number of carriers near the Dirac point.

3. 4. Nonuniformity Model

Interface and bulk oxide states in the substrate or dielectrics can cause nonuniformity to the graphene film [7, 8]. If the material under study is nonuniform, then potentially in different regions of the device one can satisfy n>>p or p>>n, but the across the sample there is significant participation of both types of carriers. For this configuration, we have made numerical estimates of the resulting Hall measurements. A representative simulated structure is a rectangular graphene Hall bar of dimensions 3μm x 10μm. A uniform mesh was defined with ~3,000 grid points (resulting from a tradeoff of speed of simulation and accuracy). A uniform charge distribution of N_{x0} (cm^{-2}) was included in the graphene, in order to represent effective doping from substrate, interface states or applied gate bias. Typical epitaxial graphene samples show negative V_{th} (or

V_{Dirac}), which means it is effectively doped to be n-type [13, 14], while transferred graphene often shows p-type nature [15-19]. Carrier type and density for both graphene types can be modulated by gate bias. To represent the nonuniformity, there is an effective doping fluctuation along the surface of the sample. With an average doping of N_{x0}, the local doping concentration $N_x(x,y)$ can be expressed as $N_{x0}+\Delta N_x(x,y)$ where $\Delta N_x(x,y)$ is local zero mean fluctuation of doping at point (x, y) on the Hall bar sample. In this study, we assumed effective doping density (N_x) has a Gaussian distribution with standard deviation N_{fluct}. There is a variation and standard deviation of Fermi potential $\Delta\varphi$ corresponding with N_{fluct}. In fact, the local fluctuations of n and p could be alternatively defined in terms of Fermi potential fluctuations instead of effective doping variations. It should be noted, however, that the relationship between $\Delta\varphi$ and N_{fluct} is dependent on carrier density. For a fixed value of $\Delta\varphi$, N_{fluct} increases as φ moves away from Dirac point, as discussed below.

In the calculations, random distributions of $N_x(x, y)$ with Gaussian distributions with standard deviation N_{fluct} were initially assigned independently to the different grid points. To account for the correlated spatial distributions of the fluctuations, we filtered the initially assigned values, by using filters defined in patch-like regions of average 1 μm length (which covers about 100 grid points). The filter size can be adjusted to correspond to different sizes of inhomogeneous doping patches. Figure 3.4 (a) shows representative values of the randomly generated matrix of local dopants showing sharp peaks and abrupt changes as initially assigned. After spatial filtering using a hanning window filter, the matrix has gradual variation in local doping concentration (Figure 3.4

(b)). The final shape of the distribution is controlled by the shape of random matrix and the size of filter.

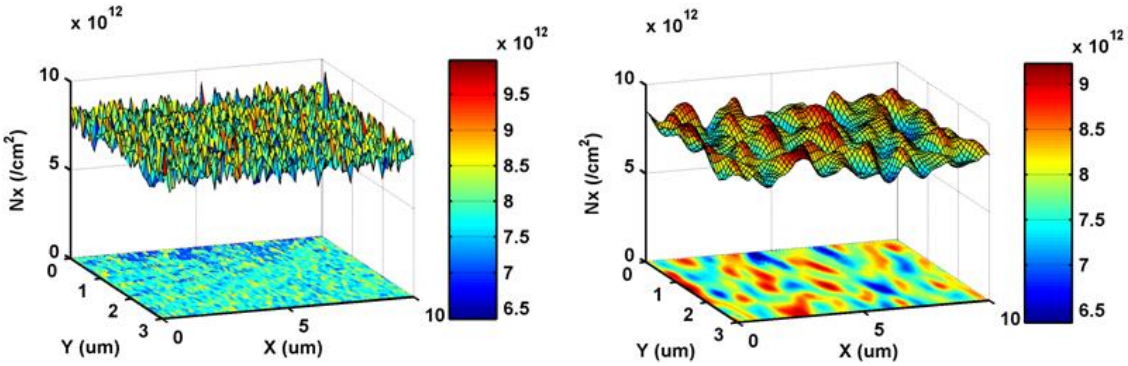


Figure 3.4. The generation and smoothing of inhomogeneous doping profile. (a) Randomly generated matrix of effective doping for 2-dimensional numerical simulation. The average effective doping density (N_x) is $8 \cdot 10^{12}$ cm^{-2} with standard deviation (N_{fluct}) of $5 \cdot 10^{11} cm^{-2}$. Three dimensionally visualized effective doping density (N_x) for z-axis, over the device area. 2-D projected contour is also presented on x-y plane. (b) The random matrix is smoothed after the 'hanning window' filter is applied. Filter size is 1μm x 1μm.

3.5. Simulation of local n(x,y) and p(x,y) distributions

With the given inhomogeneous doping distribution, electron and hole density n(x,y) and p(x,y) were calculated for each grid point using the charge neutrality equation, and relationships (3.4-3.7). In the calculations, we did not consider lateral charge re-arrangement by diffusion due to the local imbalance of charge distribution and screening effects. The approximation we used assumes the spatial doping fluctuation is filtered sufficiently to have smooth change between each mesh points. Variations in “doping” were equivalent to variations in electrostatic potential. In order to satisfy the space charge neutrality, we expect n-p= N_x relations with n(E_F, T) and p(E_F, T) which vary with Fermi energy and temperature. Figure 3.5 shows the relationship between the variation Δφ in

local electrostatic potential and the standard deviation of "effective doping" N_{fluct} defined above. Our choices of inhomogeneous parameter N_{fluct} is reasonably matched with the interface state densities [8, 15, 20]. Corresponding potential fluctuation $\Delta\varphi$ is also within the same order of the reported potential fluctuation [7, 10].

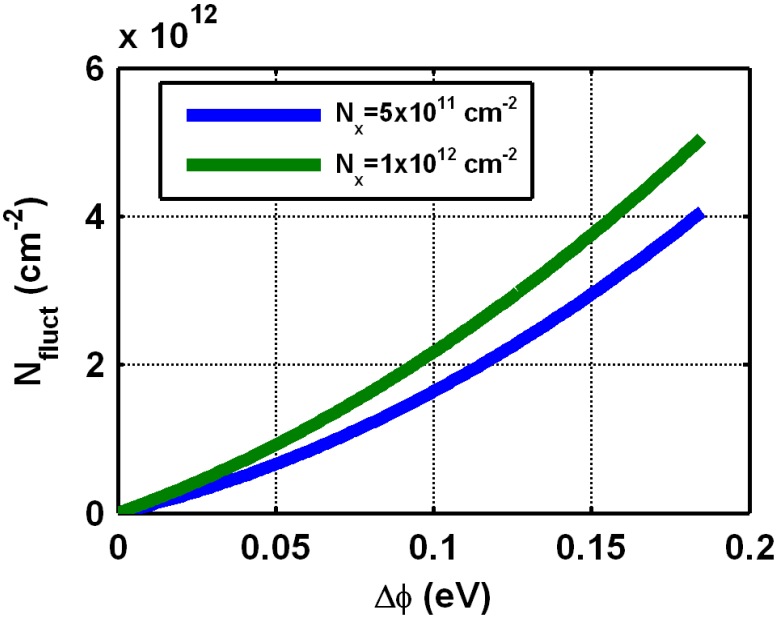


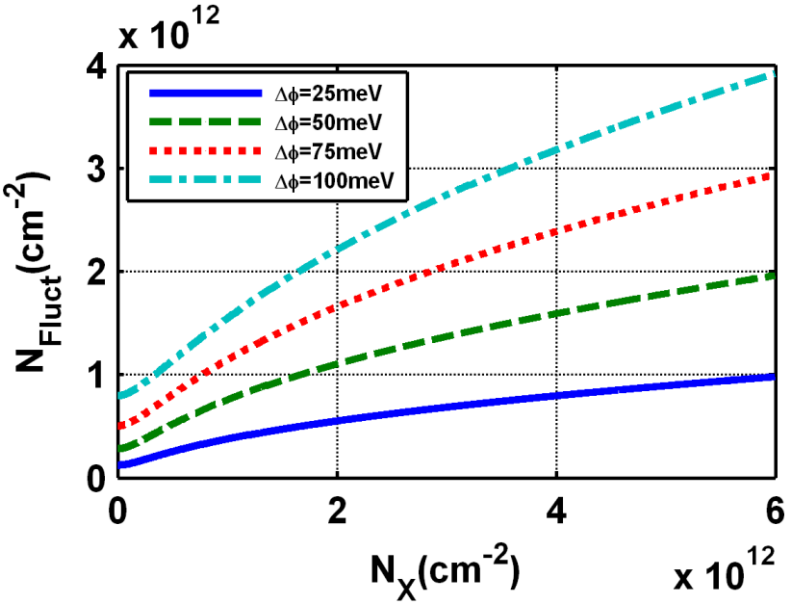
Figure 3.5. Variation in local electrostatic potential ($\Delta\varphi$) vs. local effective doping fluctuation (ΔN_{fluct}) from average doping level N_x of $5\cdot10^{11}$ and $5\cdot10^{12}$ cm^{-2}.

Gated Hall measurement has been done often in order to monitor the relation between the mobility and carrier density [3]. Within our formulation, the average effective doping density N_x (and correspondingly the Fermi energy level) are controlled by the gate bias V_g. The fluctuation in effective doping density ΔN_x remains constant as V_g changes. Alternately, as described above, the local inhomogeneity can be defined in terms of Fermi energy fluctutations. The amplitude of N_{fluct} associated with a fixed potential deviation $\Delta\varphi$ depends on the bias condition, due to the change of the density of

states at the Fermi level. Figure 3.6 describes the relation between N_x and N_{fluct} when $\Delta\varphi$ is kept constant as N_x varies. When V_g is near V_{Dirac} (when carrier density reaches its intrinsic value), the density of states is reduced therefore ΔN_x decreases for constant $\Delta\varphi$. In contrast, ΔN_x becomes larger for a given $\Delta\varphi$ for higher carrier density ($|V_g-V_{Dirac}| >> 0$) due to the increased density of states at the Fermi level. Likewise, for a fixed doping fluctuation, $\Delta\varphi$ will increase as φ approaches V_{Dirac} (Figure 3.6 (b)). The inhomogeneous doping ($N_x+\Delta N_x$) effect on Fermi energy will more obvious near the Dirac point, where the local Fermi energy level will typically vary from below to above V_{Dirac}. In this condition, the fluctuation of the effective doping can locally change the majority carrier type, which results the well known electron hole puddles.

The effect of doping fluctuations on Hall coefficient is smaller when $|V_g-V_{Dirac}|$ increases, because it represents a smaller fraction of the total carrier density. For this condition, although N_{fluct} increases as V_g deviates from the Dirac point for a constant $\Delta\varphi$, the total number of electrons (holes) became orders of magnitude larger than the intrinsic carrier density and the change of the amplitude of ΔN_x is now proportionally less significant.

(a)



(b)

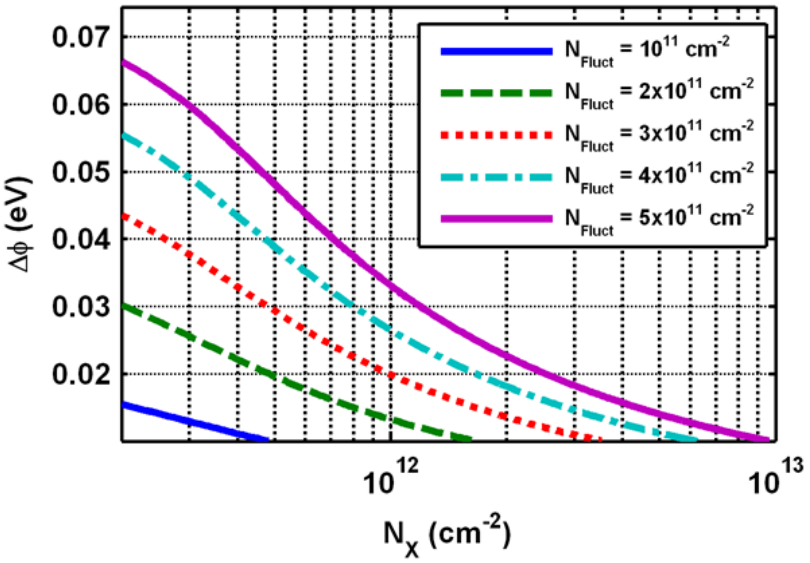


Figure 3.6. (a) Standard deviation of carrier density (N_{fluct}) vs. average doping density (N_x) of graphene film, when the standard deviation of potential fluctuation ($\Delta\varphi$) is fixed as 25, 50, 75 and 100 meV. For example, $N_{fluct} \sim 5 \cdot 10^{11}$ cm^{-2} is about 75 meV of fluctuation at Dirac point, but it is matched with 25meV of fluctuation when $N_x = 2 \cdot 10^{12}$ cm^{-2}. (b) Standard deviation of potential fluctuation ($\Delta\varphi$) vs. average doping density (N_x).

3. 6. Two dimensional current distribution calculation

Using the simulated 2-D spatial charge distribution of the sample we calculated corresponding current and potential distributions during graphene Hall measurements. The ambipolar current of holes and electrons was numerically calculated using Matlab. The calculation was based on electric current density equation under an applied vertical magnetic field:

$$\bar{J}_n = -n \cdot \mu \cdot \bar{F} \qquad (3.9)$$

$$\bar{J}_p = -p \cdot \mu \cdot \bar{F} \qquad (3.10)$$

$$\bar{F} = e \cdot (\bar{E} + \bar{v} \cdot \bar{B}) \qquad (3.11)$$

where n and p are electron and hole concentrations, J_n and J_p are the respective current densities, E is the gradient of the local Fermi potential, μ is assumed constant mobility, B is the applied magnetic field, and v_n and v_p are the average velocities for electrons and holes.

$$v_{nx} = -\mu \cdot (E_x + \mu \cdot B \cdot E_y) \qquad (3.12)$$

$$v_{px} = -\mu \cdot (E_x - \mu \cdot B \cdot E_y) \qquad (3.13)$$

It was assumed that the electron and hole populations were at every point in equilibrium among themselves and with each other (which corresponds to the assumption of rapid generation and recombination), and that there was no added contribution to resistance associated with junctions between n and p type material. Applied current is

also small (~0.5 mA/mm) in order to maintain the equilibrium state and avoid the consideration of extra electron-hole generation due to high field. Our model assumed that hole current and electron current meet the continuity equation for electric current flow,

$$\frac{\partial J_{nx}}{\partial x} + \frac{\partial J_{ny}}{\partial y} + \frac{\partial J_{px}}{\partial x} + \frac{\partial J_{py}}{\partial y} = 0 \qquad (3.14)$$

Boundary conditions included voltage V=0 at one edge of the sample, and the other end had a constant applied voltage V_x; boundary conditions of zero total current flow (including both electrons and holes) applied on the other edges of the sample. The current flows along the x-axis of the sample. By solving equations (3.9-3.14) with the boundary conditions, we can obtain the potential and electric field for every grid point. Spatially-varying charge imbalance, as needed to provide the spatially varying electric field, was not enforced, since the lateral electric fields were small. For simplicity, we took mobility to be constant over the entire region (and equal for electrons and holes). Hall coefficients were estimated by determining the difference in potential between test points located on opposite sides along the y-direction of the structure, averaging results computed with both positive and negative magnetic fields.

With the simulation framework defined above, we were able to investigate the dependence of Hall coefficient and apparent mobility on the standard deviation of charge distribution, spatial variation of charge distribution, repeatability of measurements as well as magnetic field effects.

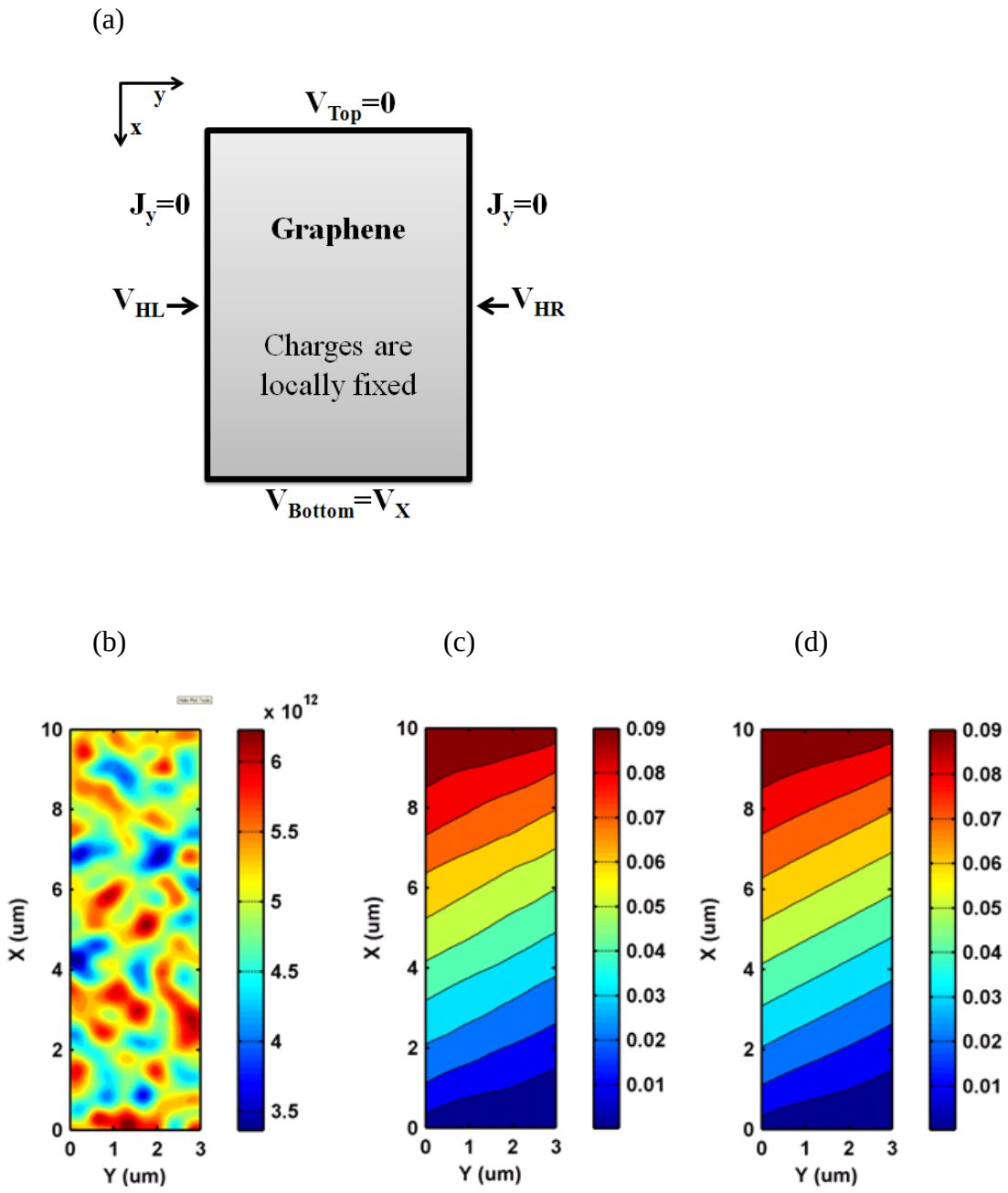


Figure 3.7. (a) Simulated device structure with boundary conditions. (b) Randomly generated inhomogeneous charge density distribution. Red and blue area represents the local fluctuation of effective doping, which can be appeared as electron hole puddles near the Dirac point. (c) Electrical potential contour of non-uniform graphene Hall measurement sample. The potential distribution is distorted due to the inhomogeneous charge distribution of the film. (d) Electrical potential contour of uniform graphene Hall measurement sample. The potential contour at the middle area is straight line.

3. 7. Potential and charge distribution

Charges in the film under constant longitudinal current flow and vertical magnetic field will push electron and hole flow to side wall and set up potential difference between each side of Hall bar. The Hall voltage V_H is measured by the potential difference between two measurement points V_{HR} and V_{HL}. A constant Hall voltage is expected at measurement points along the x-axis when the material, magnetic field, and current are uniform. Figure 7 (b) and (c) illustrate the local electron concentration and the computed potential profile for a representative selection of "doping" variation, respectively. Figure 7 (d) shows a typical potential distribution of Hall bar under measurement, for a homogeneous film for comparison. Potential distribution in the middle of the inhomogeneous graphene sample is distorted due to non-uniform doping effect of the film. While the magnetic field is kept constant, the local current path is also affected by the sample's local resistivity which is directly related to the carrier density.

3. 8. Simulation of Hall mobility

Hall mobility can be calculated from the simulated Hall coefficient,

$$\mu_H = |R_H| \cdot \sigma \qquad (3.15)$$

$$\sigma = \frac{I_x}{V_x} \cdot \frac{W}{L} \qquad (3.16)$$

σ is the simulated conductivity of the film, I_x is the simulated electrical current along the Hall bar; applied voltage (V_x) along the Hall bar, width (W) and length (L) of the sample are input parameters to the simulation. As described in Figure 3.2 and

equation (3.3), Hall coefficient R_H goes to zero near the Dirac point which leads to an unphysical mobility 'drop' at the Dirac point in the measurement [3, 21], and in our simulation for uniform graphene case ($\mu_{apparent}$ in Figure 3.8). We found that conductivity also decreased in our simulation near V_{Dirac}, however, by smaller orders of magnitude than the R_H reduction. In our simulations, we could assume either constant or carrier density dependent mobility (μ_{input}) and compare its value with the simulated Hall mobility ($\mu_{apparent}$) obtained using equation (3.15) and (3.16). The conductivity of the semiconductor can be defined as $\sigma=e\ (\mu_n \cdot n + \mu_p \cdot p)$. Therefore an overestimated carrier density from erroneous R_H will artificially degrade the extracted mobility value when it is near the intrinsic condition. From the N_{true} and $N_{measured}$ relation, one can observe the relationship between the measured (or simulated, in this case) $\mu_{apparent}$ and μ_{true}. This is plotted in Figure 3.8 for the case of carrier density dependent mobility, $\mu(N_x) = \mu_0 \cdot \sqrt{\frac{n_i}{N_x}}$ [22], where μ_0 is intrinsic (maximum) mobility and n_i is intrinsic (minimum) carrier density.

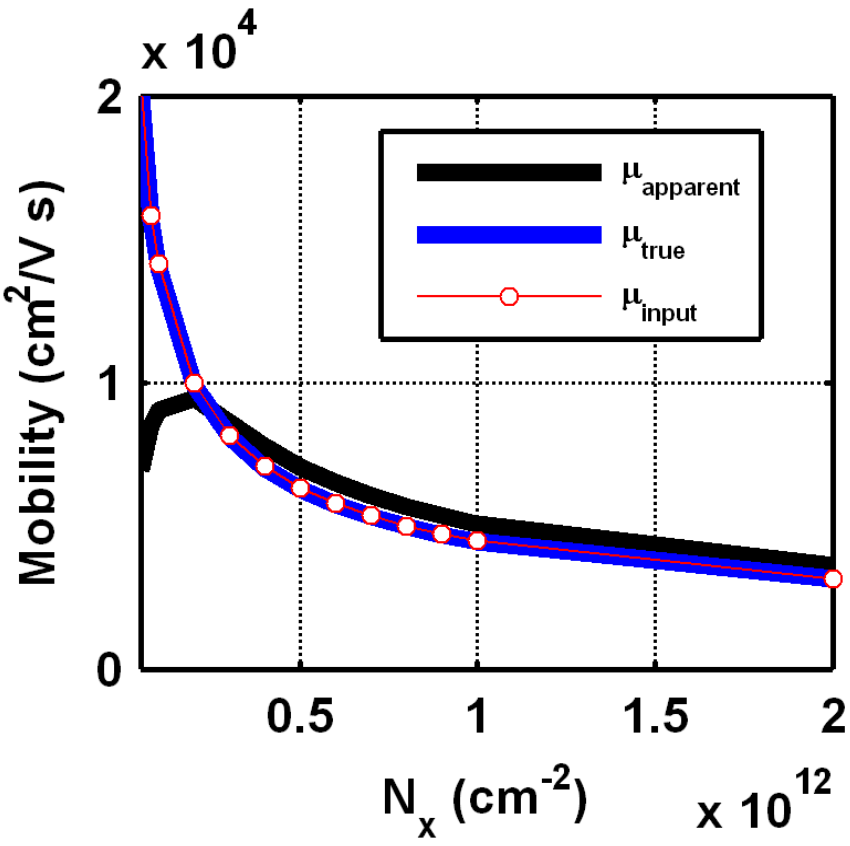


Figure 3.8. Comparison of simulated Hall mobility ($\mu_{apparent}$) vs. input mobility value in the simulation (μ_{input}) and corrected mobility value (μ_{true}). Simulated Hall sample is uniform film without any local inhomogeneity (N_{fluct}=0).

3. 9. Assesment of Hall Measurement of inhomogeneous graphene

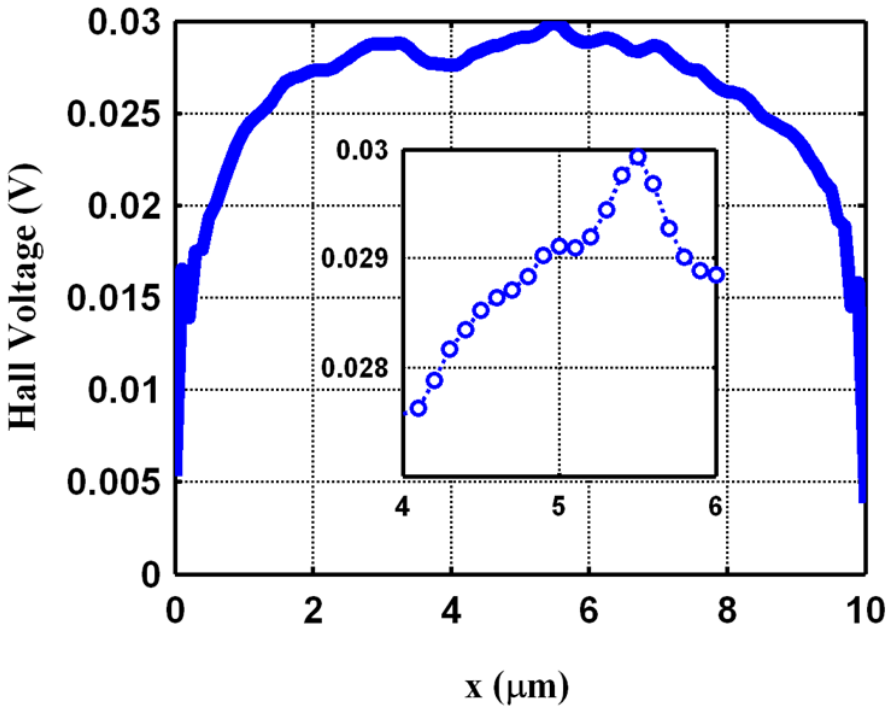


Figure 3.9. Simulated Hall voltage along the x-axis (longitudinal current flowing direction) when $N_x=3\cdot10^{12}$ cm^{-2} and $N_{fluct}=5\cdot10^{11}$ cm^{-2}. Inset: Zoom-in image of Hall voltage for mid area of the Hall bar.

Figure 3.9 is an example of simulated Hall voltage at each point along the x-axis for one instance of the ensemble of inhomogeneous graphene Hall bars simulated. The Hall voltage is shorted out near the current-injecting electrodes at top and bottom since these are assumed to be equipotentials [23, 24], therefore it is normal to locate 'branches' for Hall measurement at the middle of the Hall bar or well away from the current contacts. In the middle area of Hall bar, the spatial distribution of the Hall voltage with typical grid spacing of 100 nm shows fluctuations related to the local doping density. When $N_x=3\cdot10^{12}$ cm^{-2} and $N_{fluct}=5\cdot10^{11}$ cm^{-2} (equivalent to ~20 meV fluctuation of potential),

the fluctuation of R_H, Hall mobility shows up to 8% of fluctuation range. The result implies that the actual measurement point or in other words, the location of the branch of Hall bar would have impact on the measured Hall voltage of each specific device on a given wafer when the graphene film is inhomogeneous. The effect of local fluctuation might be averaged out in a macro scale Hall measurement or in a film level non-contact measurement method. In this study, typical grid spacing is 100 nm and it will capture the local variations, which might be neglected in large area film measurements.

Figure 3.10 represents the gated Hall simulation of inhomogeneous graphene films with various standard deviations of the doping fluctuation (N_{fluct}), ranging from 0 (uniform doping) to $5 \cdot 10^{11}$ cm^{-2} when N_x varies up to $5 \cdot 10^{12}$ cm^{-2}. Figure 3.10 (a) shows the geometry for measurement of the simulated Hall voltage V_H (in the dashed line) along with a representative doping spatial distribution. Figure 3.10 (b) shows the impact of N_{fluct} variation on Hall coefficient R_H. The V_H is highly affected by the local inhomogeneity around the measurement points [25]. As N_x was changed (by variation of the gate voltage), we maintained the shape of the inhomogeneous distribution while changing the amplitude of the effective doping fluctuation on the same distribution matrix. The peak of the measured Hall coefficient is highest for the homogeneous film, and it decreases with increasing amplitude of the doping fluctuations. The $R_{H\_measured}$ of the inhomogeneous cases deviates significantly from that of the uniformly doped graphene film of same electron and hole mobility and the same N_x. Simulation parameters such as mobility and applied bias are constant, therefore the reduction of the peak height is purely a result of the increasing amplitude of N_{fluct}. The significant changes in the curves suggest that it should be possible to use the experimental Hall coefficient

curve to estimate the inhomogeneity of graphene films when the ideal N_x, mobility, electric and magnetic field conditions are known.

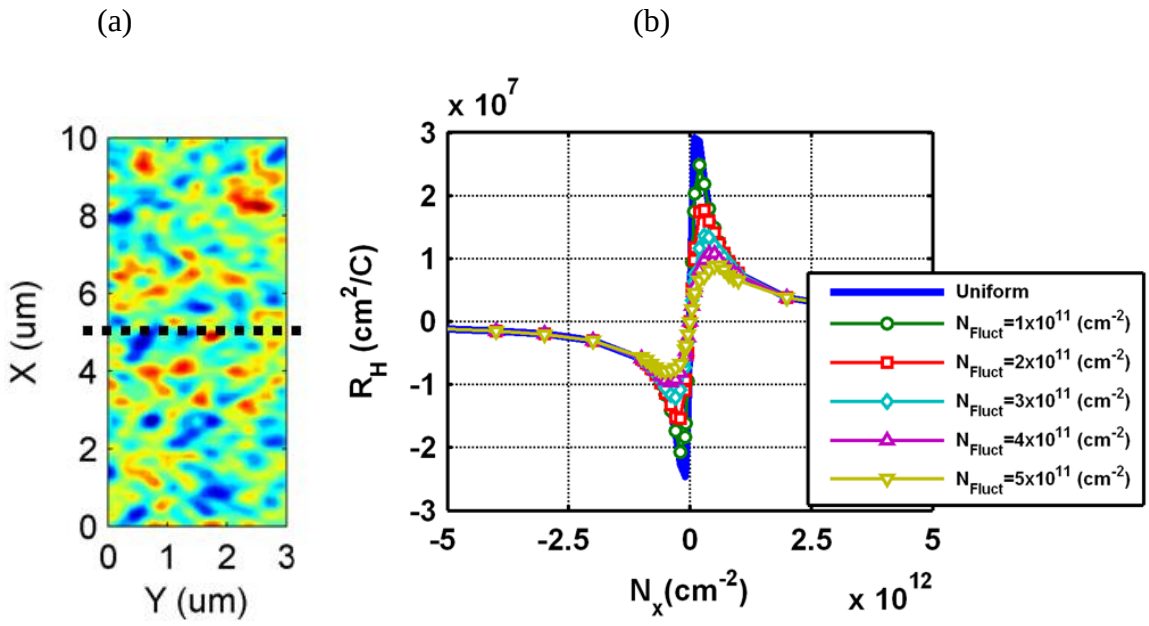
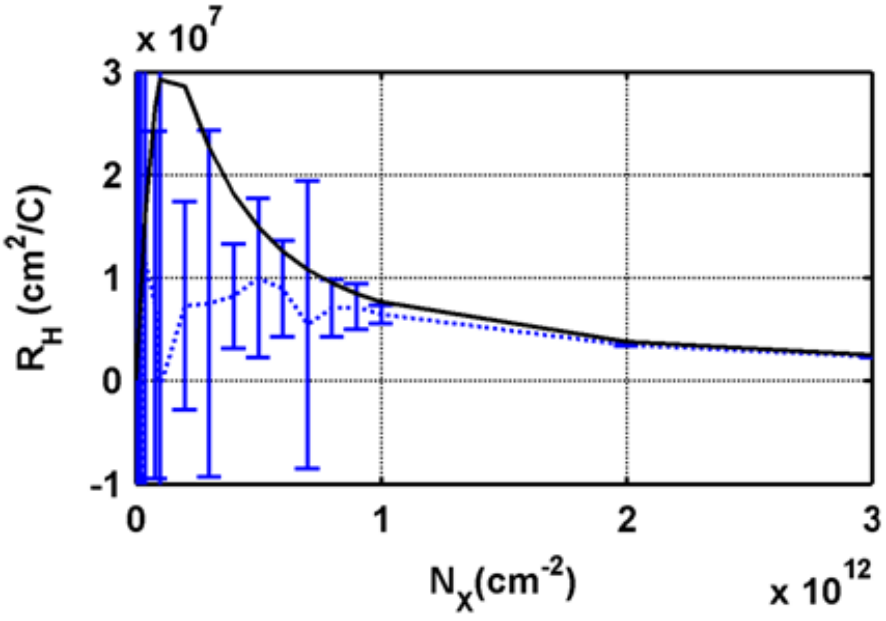


Figure 3.10. Inhomogeneous graphene Hall measurement simulation. (a) Effective doping distribution of inhomogeneous graphene. Dashed line indicates the location of Hall voltage measurement point. (b) Hall coefficient vs. gate voltage. The peak value of apparent Hall coefficient decreases when the amplitude of local doping fluctuation increases.

(a)



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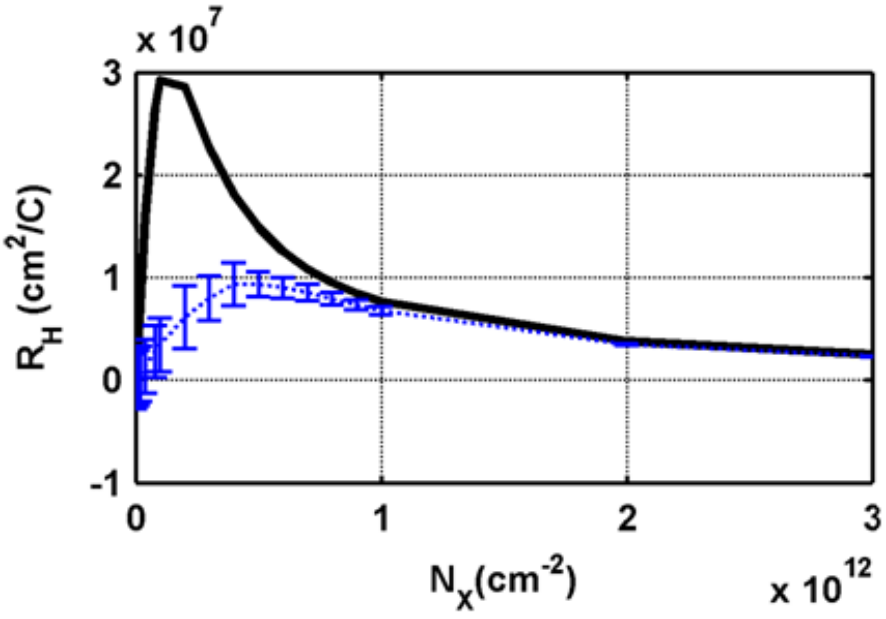
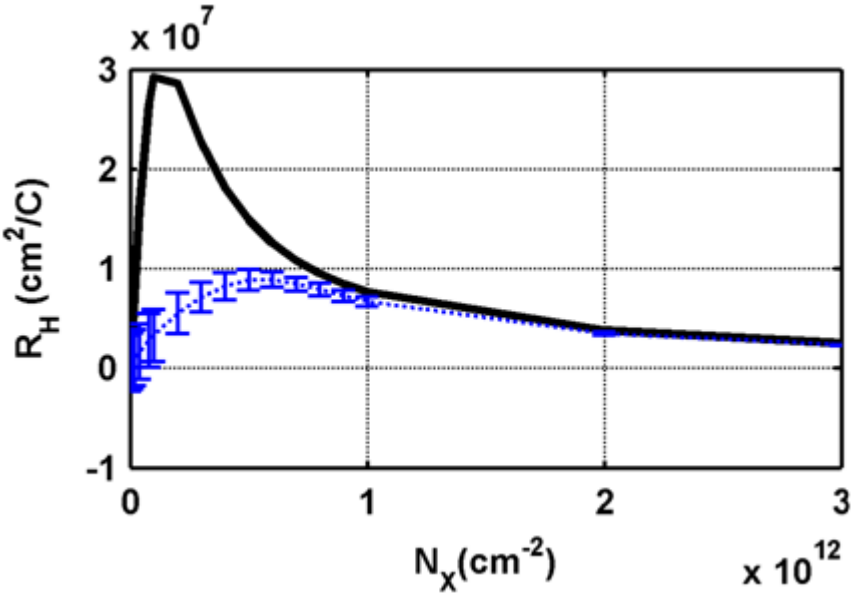


Figure 3.11. Hall coefficient vs N_x. Solid line (black) indicates the uniform graphene sample case. (a) Hall coefficient vs N_x when the size of filter size is 200 nm. (b) Hall coefficient vs N_x when the size of filter is 500 nm.

(c)



(d)

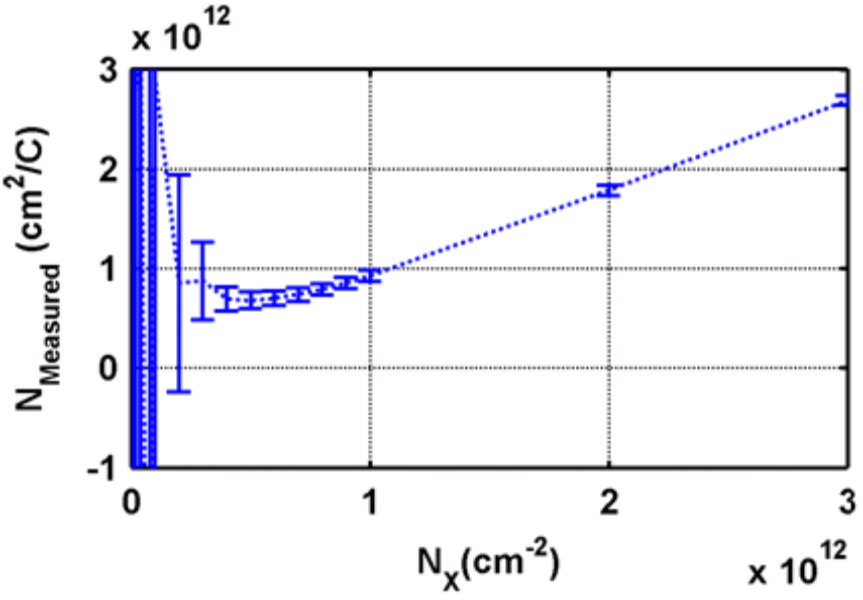


Figure 3.11. (continued) (c) Hall coefficient vs N_x when the size of filter is 1μm. All three cases show more fluctuation at lower career density condition. (d) $N_{measured}$ (Simulated measurement of carrier density assuming a single carrier Hall equation) vs. N_x. Error bars are from multiple runs of inhomogeneous graphene simulation while average doping density is set to the homogeneous case. Top and bottom of error bar are showing the standard deviation of repeated simulation results.

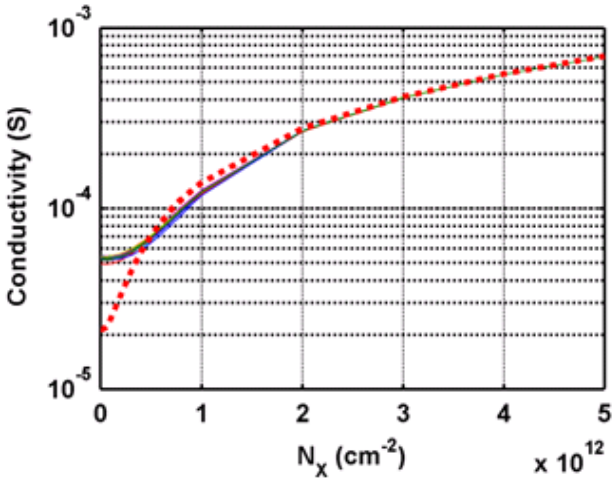
Figure 3.11 (a) ~ (c) shows collected data sets of R_H from repeated simulations, each with a different random distribution having the same value of N_{fluct}. Various filter sizes such as $0.2x0.2\mu m^2$, $0.5x0.5\mu m^2$, $1x1\mu m^2$ were applied to study the effect of the size of puddles or local doping clusters. While the filter size does not exactly define the size of the puddles, the average size of doping patches follows the filter size. The simulation was repeated 32 times, each time with a regenerated random distribution array keeping N_{fluct} of $5 \cdot 10^{11}$ cm^{-2} and filter size fixed, then the Hall voltage V_H was measured at the mid-point of the device. The dashed line is the average Hall coefficient, and the error bars indicate the standard deviation from multiple runs of simulation with different configurations of the random matrix. At a given level of inhomogeneity, simulation results show possible error margins of measurement among different samples with identical shape. The deviations from the average values arise due to the specific shapes of local doping density variation. The simulated Hall coefficient fluctuates considerably near the Dirac point (low carrier density), where inhomogeneity has more impact; the amplitude of the fluctuation reduces as the carrier density increases. Simulated $N_{measured}$ vs. N_x is shown in Figure 3.11 (d). Values of $N_{measured}$ have un-controlled fluctuations when the Dirac point is approached. The filter size of 500nm x 500nm was applied for (d). Error bars became dramatically longer when the carrier density is lower, where the effect of inhomogeneity appears more obviously. Figure 3.11 (e) displays the comparison between apparent Hall mobility ($\mu_{apparent}$) with deviation between each simulation, overlaid by corrected average mobility (μ_{true}) curve by proper carrier density which is also averaged and calculated from data of Figure 3.11 (d). The corrected mobility curve

follows the trend of μ_{true} in Figure 8, only distorted by huge inhomogeneous effect on N_{true} calculation near the Dirac point.

3.10. Minimum conductivity and Dirac point shift

As a result of inhomogeneity, the conductivity that is measured in a representative Hall (or similar "bar" structure) will vary. Simulated results for the variation of conductivity are shown in Figure 3.12. It is noteworthy that the graphene inhomogeneity will also produce variations in the measured Dirac voltage V_{Dirac} obtained from conductivity measurements (generally defined as the gate voltage for which the conductivity is minimum). When the average doping density over the device is constant, V_{Dirac} shifts due to the shape of the local doping fluctuations and low resistivity paths established by local imbalance of carrier densities. As a result, conductance versus N_x curve from simulation of multiple devices (Figure 3.12 (a)) shows variation of minimum conduction point (Dirac point) and minimum conductivity value as well. Since the inhomogeneous effect has more impact when the carrier density is low, it provides problems especially for turning off the devices. Local 'off' condition will vary within the device when the film is inhomogeneous, therefore it shows higher current level at the Dirac point than the uniform film device (dashed line). Figure 3.12 (b) shows the zoom-in conductivity curves in log scale, near the Dirac point. Several arrows indicate some of the shifts of minimum conductivity point for several different inhomogeneous samples. The simulated fluctuation of minimum conductivity point vs. N_x corresponds up to ~30 meV of potential fluctuation at the minimal conduction regime near the Dirac point for the particular setup in Figure 3.12.

(a)



(b)

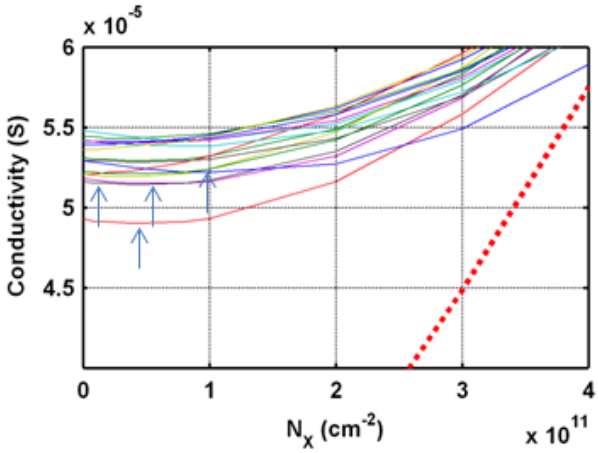


Figure 3.12. (a) Conductivity curves from multiple simulations of inhomogeneous doping distribution. The set of simulated inhomogeneous graphene conductivities show a higher minimum value near Dirac point (where N_x approaches 0) than ideal, uniform graphene (dashed line). (b) Zoomed-in conductivity near Dirac point; the Dirac point is shifted and the minimum conductivity also varies.

(a) (b)

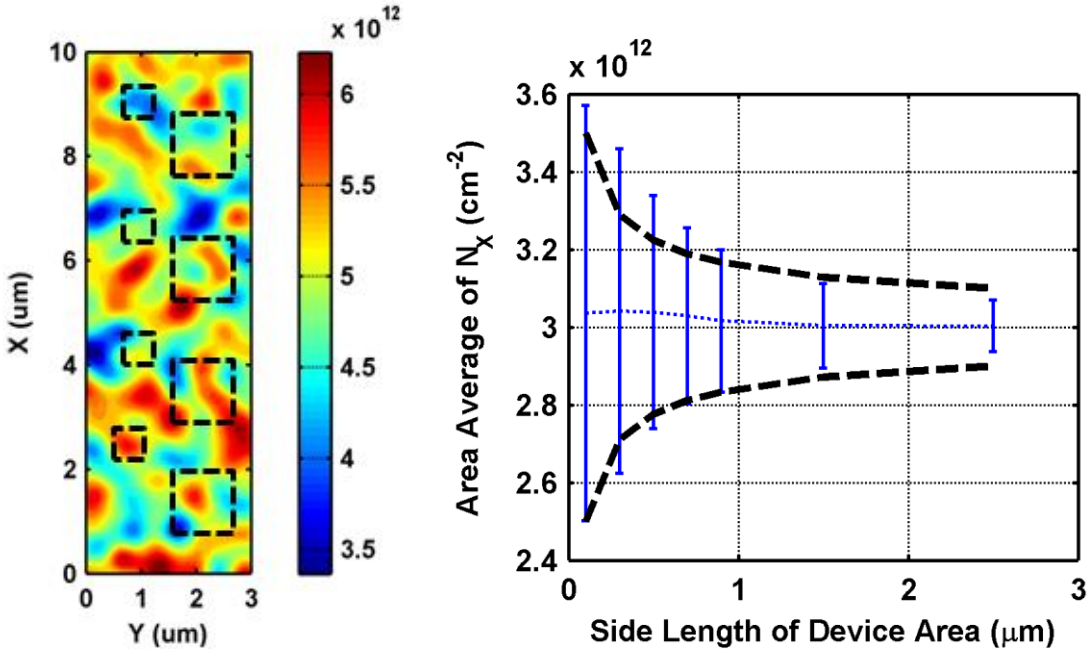


Figure 3.13. (a) Device area defined on inhomogeneous graphene. Larger boxes include spatial distribution, however, smaller ones often dominated by single type of effective doping N_x. (b) Distribution of average N_x (blue dot) and standard deviation (error bars) vs. device size, for 100 devices. Black dash line indicates statistical change of deviation which is inversely with device dimension.

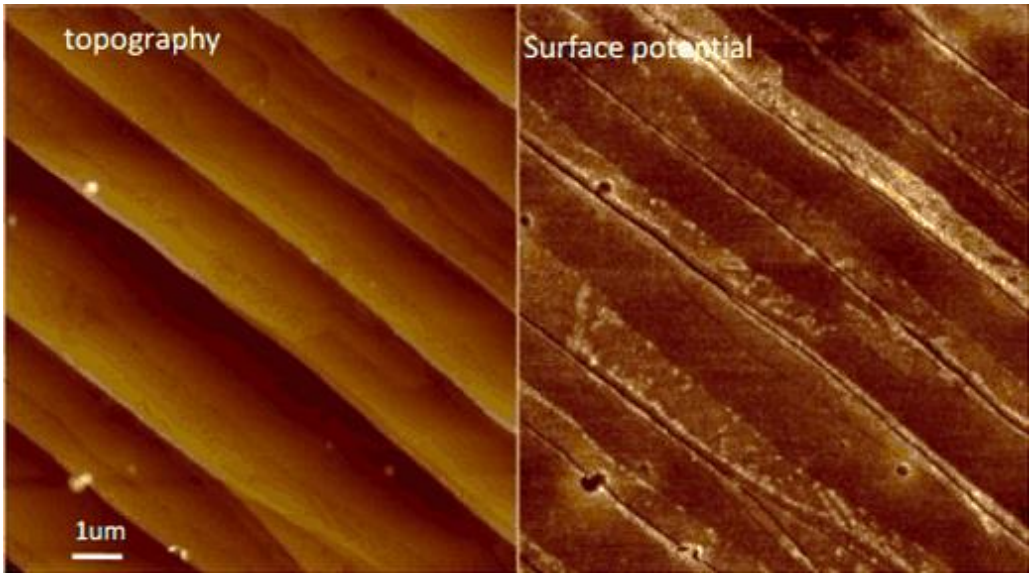
Dirac point shifts are likely to be less significant for larger devices because local inhomogeneities can be averaged over the active area of the devices. Variations among devices will increase when the dimensions are comparable to the size of puddles, where the regional doping density can dictate the characteristics of each individual device. In order to show the effect of device scaling on device-to-device uniformity with inhomogeneous graphene, we assumed the Dirac point (V_{Dirac}) of each scaled device is defined by the average doping density of the device's active area. Figure 3.13 (a) shows an example of defining the 'device area' of 1um x 1μm or 500nm x 500 nm on

inhomogeneous graphene with average $N_x=3\cdot10^{12}$ cm^{-2} and $N_{fluct}=5\cdot10^{11}$ cm^{-2}. Larger boxes usually cover an area that includes different doping types and densities, therefore the overall N_x value will be averaged over the whole area of the device. However, smaller boxes are often dominated by a single carrier type, which will cause more variation from one device to another. The simulation is repeated for 100 devices for each size of device from side length of 100nm to 2.5μm, with different spatial distributions of N_x. Figure 3.13 (b) shows the relation of device size and fluctuation of average N_x of each device. The dotted line is the average N_x and error bar shows the standard deviation of 100 devices for each size. Since the background inhomogeneous graphene has an average N_x of $3\cdot10^{12}$ cm^{-2}, the average of all devices should correspond to this value. However, when the size of the device is scaled down, local inhomogeneity begins to control the device characteristics of device and more fluctuations occur. Maintaining device uniformity over a wafer can be expected to be more difficult when each device becomes smaller. The results show that the standard deviation varies according to d^{-1}, where d is the device (linear) dimension, as expected for the standard deviation of the sum of independent identically distributed variables (black dash line in Figure 13 (b)).

3. 11. Epitaxial Graphene on SiC Substrates

Epitaxial graphene is grown on SiC substrates, in a process where Si atoms sublime and the remaining carbon atoms rearrange themselves to form a graphene film [26]. A high degree of uniformity of film characteristics, including the number of graphene layers produced, has been demonstrated over the substrates. A common-place perturbation to the graphene homogeneity occurs, however, when there is atomic scale

'terrace edge'. Terraces on the SiC are produced as a result of a slight off-cut from the c-axis for the substrates. It is likely to have double or multi-layer graphene at the terrace edges and in their vicinity, while single layer coverage is dominant in the flat basal plane areas between steps [5]. Measurements of conductivity dependence on current orientation relative to that of the terrace edges in epitaxial graphene was reported by Yakes et al. [27]. Figure 3.14 (a) shows an AFM topograph of Si-face epitaxial graphene and the surface potential (b) over the same area. There is a slight variation of the potential at the terrace edges which can also be emulated in our simulations by modifying the carrier density. We simplified the change of layer number near the steps by modeling strips of two types of films with different carrier densities at assumed step positions. Global inhomogeneity (N_{fluct}) is omitted here to get a clearer understanding of the effect of edges only. Since the typical steps are aligned in a certain direction on the substrate, we modeled straight lines boundaries between regions and made several simulations for different angular arrangements.



(a) (b)

Figure 3.14. (a) Atomic force microscope image of topography of steps on epitaxial graphene on SiC. (b) Surface potential of epitaxial graphene on SiC substrate.

As shown in Figure 3.15 (a) ~ (d), various orientations of the strips in the simulation produce an impact on the measured Hall voltage. For these structures, the assumed strip characteristics are carrier density of $3 \cdot 10^{12}$ cm^{-2} for blue region (representing the single layer area) and $6 \cdot 10^{12}$ cm^{-2} for brown strips (bi- or multi layer at the terrace edges). Due to increased density of states, bilayer graphene shows increased carrier density at the same potential [3]. The coverage ratio of the bilayer region depends on the process conditions and the preparation of the SiC substrate [5, 6]. The ratio we assumed in the simulation roughly follows our AFM measurements and also estimates from reported images [6].

When the simulated Hall voltage was measured “across” the terrace lines (0 degree case), the result was different from the result which was measured along the edges

(90 degree case) and intermediate angles (45 degree case). The 0 degree case result (a) is similar to the uniform case, because there is no difference among the points involved in the Hall voltage measurement along the channel. Figure 3.15 (b) corresponds to a measurement along the edges. The result depends on the voltage measurement point, following a roughly periodic variation with position. The Hall voltage depends on measurement position in a more complicated manner when there are angles intermediate between 0 and 90 degrees, as in (c). The $R_{H\_measured}$ result depends on the ratio of basal plane and terrace widths that are intersected by the line between the Hall voltage measuring points.

(a)

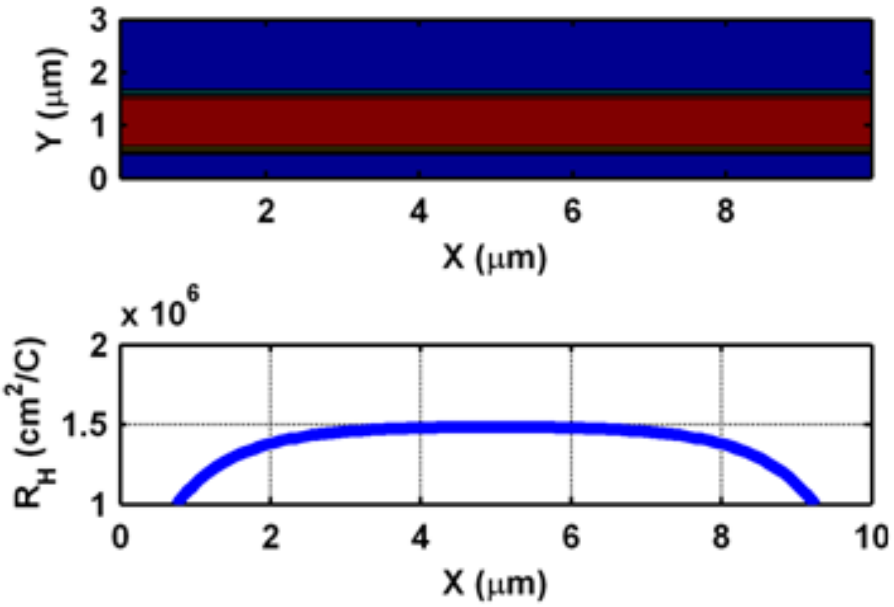
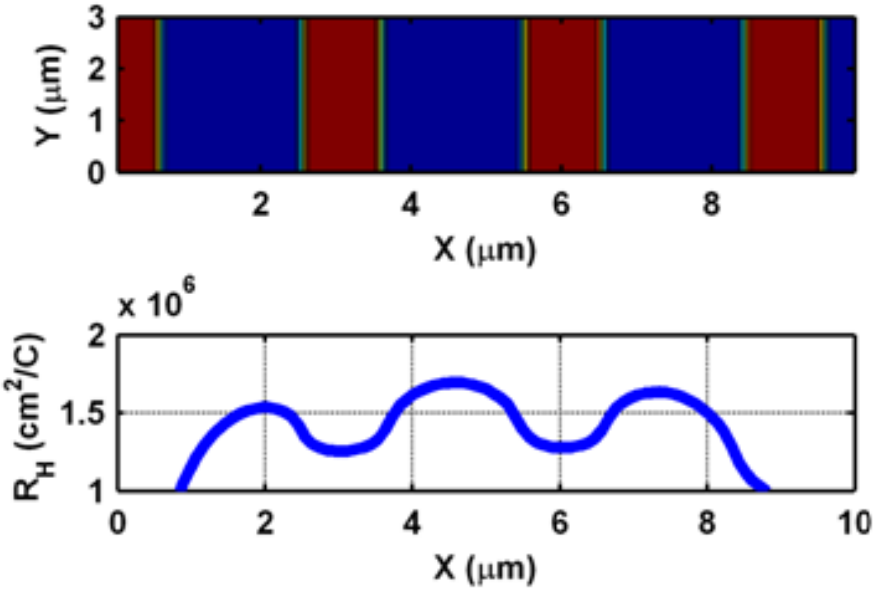


Figure 3.15. Various orientations of terraces and associated graphene regions of edge area (Red) in the simulation and their impact on the Hall coefficient. (a) 0 degree orientation. Hall voltage is measured across the edge area.

(b)



(c)

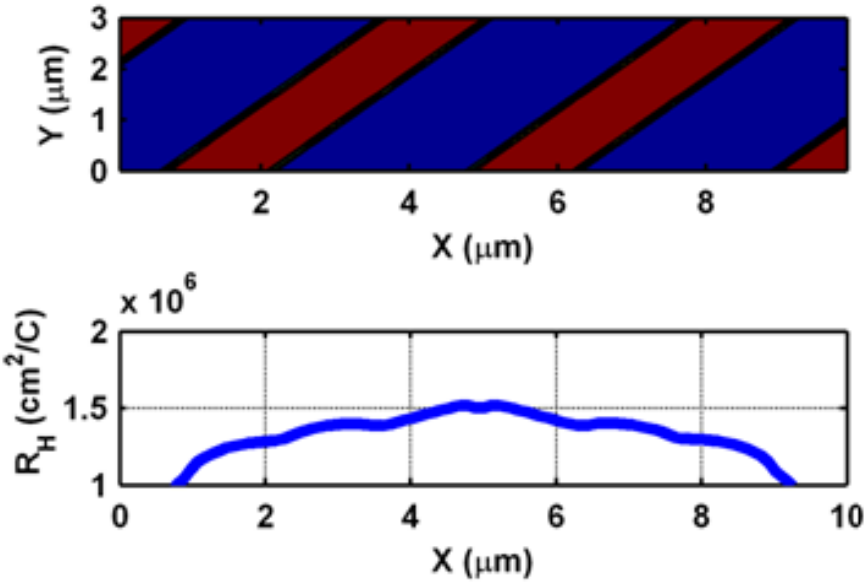


Figure 3.15. (continued) (b) 90 degree orientation where Hall voltages are measured on pure basal plan or edge area.. (c) 45 degree orientation. R_H is affected by the characteristics of the measurement location and the ratio of edge vs. basal plane lies between V_H measurement points.

3. 12. Conclusion

Two dimensional numerical simulation of inhomogeneous graphene has been performed to investigate the impact of inhomogeneity on Hall measurements. Our results show significant variations of the measurement results due to local fluctuation of charge density (or electric potential), and the placement of the Hall contacts. According to our model, the size of local inhomogeneous region and the amplitude of the fluctuations control the amount of deviation of Hall mobility from the value of uniform film case. Especially for epitaxial graphene on SiC wafers, step edges can be a source of inhomogeneity depending on the angle of the device orientation on the wafer. Although these effects are largely suppressed in measurements of large area devices, it is expected they will be significant sources of variation in the characteristics of scaled graphene devices.

Chapter 3, in full, is a reprint of the material as it appeared in *Solid State Electronics* 2014, K. Lee, J.S. Moon, T. Oh, S. Kim, P. Asbeck and P. M. Asbeck. The dissertation author was the primary investigator and author of this paper.

3.13. References

[1] Moon, J.S., Curtis, D., Bui, S., Hu, M., Gaskill, D.K., Tedesco, J.L., Asbeck, P., Jernigan, G.G., VanMil, B.L., Myers-Ward, R.L. and Eddy Jr, C.R., "Top-Gated Epitaxial Graphene FETs on Si-Face SiC Wafers With a Peak Transconductance of 600 mS/mm." Electron Device Letters, IEEE. 2010;31:260-2.

[2] Bolotin, K.I., Sikes, K.J., Jiang, Z., Klima, M., Fudenberg, G., Hone, J., Kim, P. and Stormer, H.L. "Ultrahigh electron mobility in suspended graphene." Solid State Communications. 2008;146:351-5.

[3] Zhu W, Perebeinos V, Freitag M, Avouris P. "Carrier scattering, mobilities, and electrostatic potential in monolayer, bilayer, and trilayer graphene." Physical Review B. 2009;80.

[4] Kedzierski, J., Hsu, P.L., Healey, P., Wyatt, P.W., Keast, C.L., Sprinkle, M., Berger, C. and De Heer, W.A., "Epitaxial Graphene Transistors on SiC Substrates." Electron Devices, IEEE Transactions on. 2008;55:2078-85.

[5] Nyakiti LO, Wheeler VD, Garces NY, Myers-Ward RL, Eddy CR, Gaskill DK. "Enabling graphene-based technologies: Toward wafer-scale production of epitaxial graphene." MRS Bulletin. 2012;37:1149-57.

[6] Emtsev, K.V., Bostwick, A., Horn, K., Jobst, J., Kellogg, G.L., Ley, L., McChesney, J.L., Ohta, T., Reshanov, S.A., Röhrl, J. and Rotenberg, E., "Towards wafer-size graphene layers by atmospheric pressure graphitization of silicon carbide." Nature materials. 2009;8:203-7.

[7] Zhang Y, Brar VW, Girit C, Zettl A, Crommie MF. "Origin of spatial charge inhomogeneity in graphene." Nature Physics. 2009;5:722-6.

[8] Zebrev GI, Melnik EV, Batmanova DK. "Using capacitance methods for interface trap level density extraction in graphene field-effect devices." Microelectronics (MIEL), 2012 28th International Conference on2012. p. 335-8.

[9] Li Q, Hwang E, Sarma SD. "Disorder-induced temperature-dependent transport in graphene: Puddles, impurities, activation, and diffusion." Physical Review B. 2011;84:115442.

[10] Martin, J., Akerman, N., Ulbricht, G., Lohmann, T., Smet, J.V., Von Klitzing, K. and Yacoby, A. "Observation of electron–hole puddles in graphene using a scanning single-electron transistor." Nature Physics. 2008;4:144-8.

[11] Rossi E, Adam S, Das Sarma S. "Effective medium theory for disordered two-dimensional graphene." Physical Review B. 2009;79.

[12] Adam S, Jung S, Klimov NN, Zhitenev NB, Stroscio JA, Stiles MD. "Mechanism for puddle formation in graphene." Physical Review B. 2011;84.

[13] Kopylov S, Tzalenchuk A, Kubatkin S, Fal'ko VI. "Charge transfer between epitaxial graphene and silicon carbide." Applied Physics Letters. 2010;97:112109.

[14] Wu, Y., Jenkins, K.A., Valdes-Garcia, A., Farmer, D.B., Zhu, Y., Bol, A.A., Dimitrakopoulos, C., Zhu, W., Xia, F., Avouris, P. and Lin, Y.M., "State-of-the-art graphene high-frequency electronics." Nano letters. 2012;12:3062-7.

[15] Chen Z, Appenzeller J. "Mobility extraction and quantum capacitance impact in high performance graphene field-effect transistor devices." Electron Devices Meeting, 2008 IEDM 2008 IEEE International: IEEE; 2008. p. 1-4.

[16] Lin Y-M, Chiu H-Y, Jenkins KA, Farmer DB, Avouris P, Valdes-Garcia A. "Dual-gate graphene FETs with of 50 GHz." Electron Device Letters, IEEE. 2010;31:68-70.

[17] Kedzierski, J., Pei-Lan Hsu, J., Reina, A., Jing Kong, A., Healey, P., Wyatt, P. and Keast, C., "Graphene-on-insulator transistors made using C on Ni chemical-vapor deposition." Institute of Electrical and Electronics Engineers; 2009.

[18] Sharma BK, Ahn J-H. "Graphene based field effect transistors: Efforts made towards flexible electronics." Solid-State Electronics. 2013;89:177-88.

[19] Al-Amin C, Karabiyik M, Vabbina PK, Sinha R, Pala N. "Field controlled RF Graphene FETs with improved high frequency performance." Solid-State Electronics. 2014;95:36-41.

[20] Tan, Y.W., Zhang, Y., Bolotin, K., Zhao, Y., Adam, S., Hwang, E.H., Sarma, S.D., Stormer, H.L. and Kim, P. "Measurement of scattering rate and minimum conductivity in graphene." Physical Review Letters. 2007;99:246803.

[21] Ponomarenko, L.A., Yang, R., Mohiuddin, T.M., Katsnelson, M.I., Novoselov, K.S., Morozov, S.V., Zhukov, A.A., Schedin, F., Hill, E.W. and Geim, A.K., "Effect of a High-κ Environment on Charge Carrier Mobility in Graphene." Physical Review Letters. 2009;102.

[22] Giesbers A, Procházka P, Flipse C. "Surface phonon scattering in epitaxial graphene on 6 H-SiC." Physical Review B. 2013;87:195405.

[23] Volger J. "Note on the Hall potential across an inhomogeneous conductor." Physical Review. 1950;79:1023.

[24] Rendell R, Girvin S., "Hall voltage dependence on inversion-layer geometry in the quantum Hall-effect regime." Physical Review B. 1981;23:6610.

[25] Ohgaki, T., Ohashi, N., Sugimura, S., Ryoken, H., Sakaguchi, I., Adachi, Y. and Haneda, H., "Positive Hall coefficients obtained from contact misplacement on evident n-type ZnO films and crystals." Journal of Materials Research. 2008;23:2293-5.

[26] Gaskill, D.K., Jernigan, G., Campbell, P., Tedesco, J.L., Culbertson, J., VanMil, B., Myers-Ward, R.L., Eddy, C., Moon, J., Curtis, D. and Hu, M., "Epitaxial graphene growth on SiC wafers." ECS Transactions. 2009;19:117-24.

[27] Yakes, M.K., Gunlycke, D., Tedesco, J.L., Campbell, P.M., Myers-Ward, R.L., Eddy Jr, C.R., Gaskill, D.K., Sheehan, P.E. and Laracuente, A.R., "Conductance anisotropy in epitaxial graphene sheets generated by substrate interactions." Nano letters. 2010;10:1559-62.

Chapter 4

Analysis of Heat Dissipation of Epitaxial Graphene Devices on SiC

A three-dimensional thermal simulation for analysis of heat dissipation of graphene resistors on silicon carbide substrates is presented. We investigate the effect of parameters such as graphene-substrate interface thermal resistance, device size and source-to-drain contact spacing, to quantify lateral as well as vertical heat spreading. Pulsed I-V measurements were performed at different temperatures and pulse widths to extract device thermal resistance for comparison with simulation results. Due to small heat capacitance of the device, self-heating occurs even at the shortest pulse time of 200

ns. The effective thermal resistance of epitaxial graphene resistors on SiC was estimated as $8 \cdot 10^{-5}$ K $cm^2 W^{-1}$, by comparison between measurement and simulation results.

4.1. Introduction

Graphene has been the topic of extensive research because of its superb electrical [1], mechanical [2], optical [3] and thermal [4, 5] characteristics. In the r.f. and microwave area, extremely high electron and hole mobility [6, 7] have made graphene an attractive candidate for the channel material of high speed devices. Various demonstrations of graphene rf transistors have proven graphene's potential for high frequency applications, based on outstanding carrier mobility, high saturation velocity and high carrier density [8, 9]. However, in order to enhance the performance of many high speed devices, intense electric fields along with high current densities are needed in the channel, and consequently Joule heating occurs. [10] Although graphene has extremely good thermal conductivity [4], the overall heat dissipation of graphene devices is controlled by the thermal resistance of the system, which depends on the device structure, interface resistance, substrate material, etc. Understanding the heat spreading of graphene devices is important because self-heating effects can limit the effective carrier mobility of the graphene [11, 12], maximum current carrying capability [13], and overall device reliability. [14]

In this chapter, we conducted a three dimensional (3-D) thermal simulation to investigate the heat dissipation characteristics of representative device structures for r.f. applications. In order to compare our simulations with experimental results, pulsed

current vs. voltage characteristics of graphene resistors were also measured under various temperatures and bias conditions.

4.2. Simulation Method

A physically-based device simulator (Sentaurus TCAD of Synopsys) was used for the 3-D simulation. We typically assumed a uniform heat source over the graphene resistor's 'channel' area. The baseline structure is a non-gated epitaxial graphene device [8] which has “source-drain” spacing L_{SD} of 500 nm, graphene channel width of 6 μm. A 300 K heat sink is located at the bottom of the SiC substrate, which is reduced to 50 μm in the simulation for efficient calculation. The insensitivity to SiC thickness is validated by comparing simulation for thicknesses up to 150 μm, which show less than 1% difference of T_{Max} from that of the 50 μm case used. A large volume outside of the device region was included to allow for 3D heat spreading. A quarter of the device was simulated for to decrease simulation time, thanks to the reflective boundary conditions. Figure 4.1 shows a representative 3-D simulation structure (a quarter of the device) with zoom-in image of channel area with mesh grid (inset).

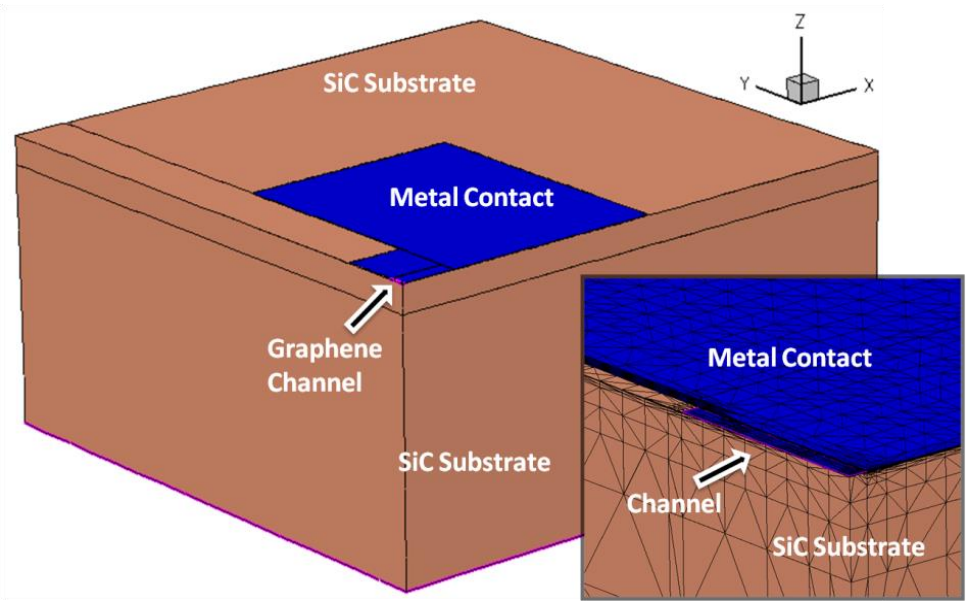


Figure 4.1. Simulated device structure; a quarter of graphene resistor on SiC substrate. (inset) Zoom-in image of the device with mesh grid.

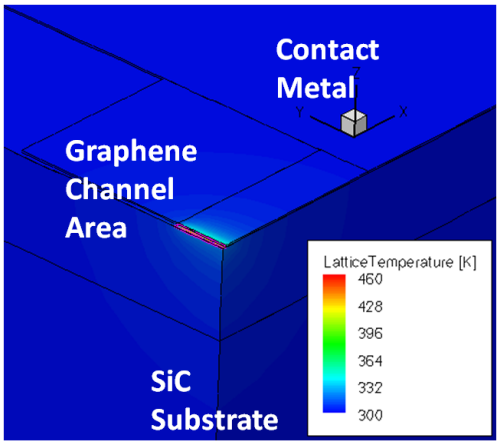
Reported parameters were used for thermal conductivity κ_{th} of graphene (50 $Wcm^{-1}K^{-1}$ [4]), SiC (4.9 $Wcm^{-1}K^{-1}$ [15]), as well as for interface thermal resistance at the graphene-substrate interface ($8.8 \cdot 10^{-9}$ $K \cdot m^2W^{-1}$ [16]), and at the graphene-metal interface ($1.92 \cdot 10^{-9}$ $K \cdot m^2W^{-1}$ [17]). The interface thermal resistance is also known as Kapitza resistance, which is thought to originate from differences of electronic and vibrational properties of attached materials [18]. Heat transfer is hindered at the interface by the differences of phonon frequencies and vibrational characteristics between the two materials. The bulk thermal conductivity of 6H-SiC has been measured to be in the range 2.9~4.9 $Wcm^{-1}K^{-1}$ [15, 19, 20]; uncertainties in this value will affect the simulation by less than 10% of maximum temperature differences. For graphene, also, thermal conductivity values are also reported over a wide range according to various circumstances, such as graphene supported by SiO_2 and suspended graphene devices

(50~5500 $Wm^{-1}K^{-1}$ [4, 5, 21, 22]). It is also reported to have reduced thermal conductivity in the case of devices in ballistic regime [23]. In epitaxial graphene films, it is likely that the mean free path of phonon will decrease due to the substrate scattering [24, 25], therefore it may not reach the ballistic limit until the device is scaled down to less than 100 nm. In this study, we assumed the graphene thermal conductivity value to be 50 $Wcm^{-1}K^{-1}$ with for graphene layer of 0.35 nm thickness.

4.3. Simulation Results

Figure 4.2 (a) displays the lattice temperature distribution for uniform DC power dissipation over the channel area. A zoom-in image (b) and a cut-area picture (c) indicate better cooling near the metal contact and the edge of the graphene. Because of the lateral heat spreading into metal contacts and edges of the device, the maximum "junction" temperature (T_{Max}) can be found at the middle of the device channel, when the heating is occurring uniformly over the channel area.

(a)



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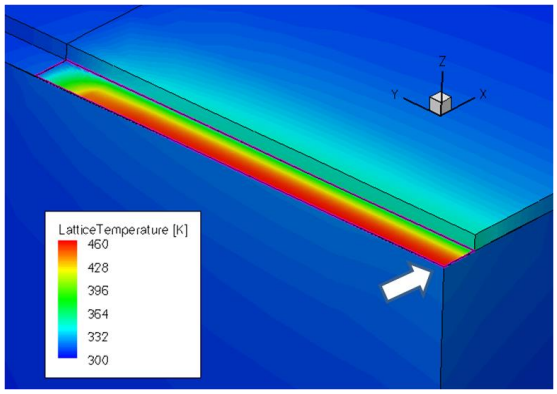


Figure 4.2. (a) 3-D simulated lattice temperature of graphene resistor. A quarter of the device is shown here. (b) Zoom-in figure of (a) which shows cooling effect from the metal contact and side edge of the channel. Hottest point is indicated by white arrow.

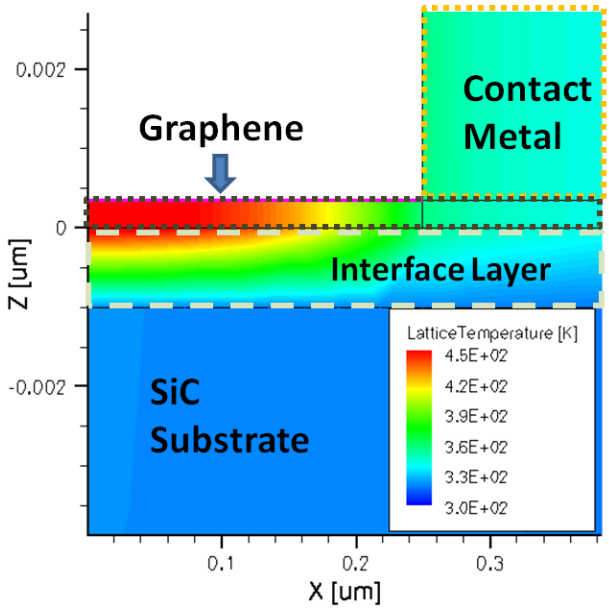
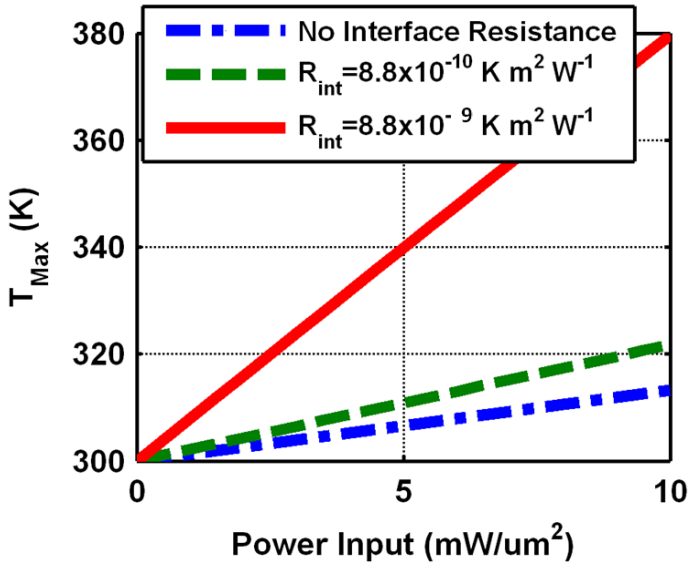


Figure 4.2. (continued) (c) Vertical cut-area temperature profile at the middle of the channel.

4.3.1. Substrate and Interface Thermal Resistances

Overall thermal resistance of the device is highly impacted by the bulk thermal conductivity of the substrate [16], because the heat spreads through the substrate to reach the bottom heat sink. In our simulation, the heat sink is only located at the bottom of substrate, which is also valid in most real devices. Cooling by air convection from the top surface is not considered in this study.

(a)



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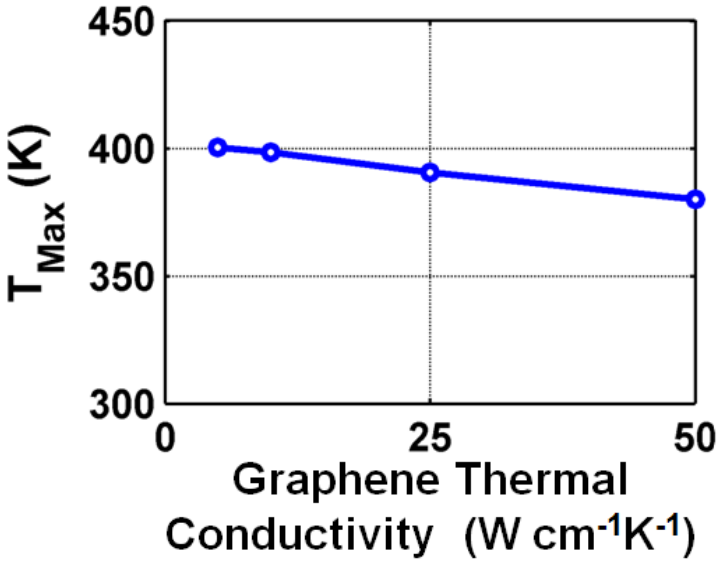


Figure 4.3. (a) Simulated junction temperature (T_{Max}) with graphene-substrate interface resistance variation. Assumed graphene thermal conductivity is 50 $Wcm^{-1}K^{-1}$ (b) Simulated junction temperature with various graphene thermal conductivities assumed. 10mW/μm^2 of input power was applied for R_{int}=8.8·10 $^{-9}$ K m^{2}W^{-1} case.

When the substrate material is fixed, the graphene-substrate interface thermal resistance (R_{int}) becomes an important factor. The relation of input power density (P_{in}) to T_{Max} is shown in Figure 4.3 (a) for several R_{int} values. T_{Max} is 380 K (80 K temperature rise) for P_{in} of $1 \cdot 10^{6}$ W/cm^2, when $R_{int}=8.8 \cdot 10^{-9}$ K m^{2}W^{-1} [16] (corresponding to the assumption that graphene layer and SiC substrate interface thermal resistance has approximately the same value as for the graphene-SiO_2 interface). Even if R_{int} is smaller than expected thermal resistance of hydrogen passivated interface, it shows significant effect on temperature rise compared with assuming no interface resistance. R_{int} of $8.8 \cdot 10^{-9}$ K m^{2}W^{-1} is an example of non-zero, however, order of magnitude smaller interface resistance than SiO_2 case. In the following, $R_{int}=8.8 \cdot 10^{-9}$ K m^{2}W^{-1} is assumed. The impact of the thermal conductivity of the graphene film is shown in Figure 4.3 (b), where the temperature rise is shown for the case of $R_{int}=8.8 \cdot 10^{-9}$ K m^{2}W^{-1} at 10 mW/um^2 input power. The graphene thermal conductivity is observed to have only a minor effect on overall temperature rise.

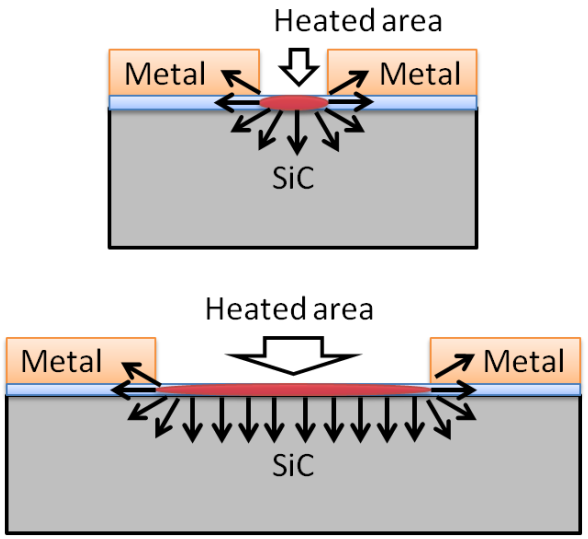
4.3.2. Lateral Heat Spreading

The effect of lateral heat spreading and 3-D heat spreading can be seen in figure 4.4. Figure 4.4 (a) shows the 2-D structure of simulated devices with various channel lengths and uniform power input over the whole channel (for example, when the sheet resistance of graphene channel is uniform and same amount of current is applied across the channel length). T_{Max} vs. uniform power input density of P_{in} over the channel is described in figure 4.4 (b). As channel length increases while the power density is fixed, heat spreading from the middle of the channel becomes more difficult because lateral

spreading is suppressed and vertical heat spreading is also limited to 1D, rather than 3D, heat spreading. Since the power density is uniform, the total amount of power is also larger for long channel cases.

Most of the heat arriving at the metal contact conducts laterally through thick metal films, eventually spreads into the substrate. In order to determine the paths of heat spreading, one can integrate the heat flux of each interface. According to the simulation, the majority of the heat spreads vertically into the substrate while only a small amount of heat is relieved laterally by source and drain contacts, even for short channel lengths. The lateral heat diffusion component along the graphene layer is ~14% out of total power input for L_{SD}=100 nm and only ~1% for L_{SD}=500 nm. This ratio will be decided by contact distance, thermal conductivity of bulk substrate and interface, for instance, lateral heat spreading will be more helpful when the substrate's thermal conductivity is low, such as SiO_2.

(a)



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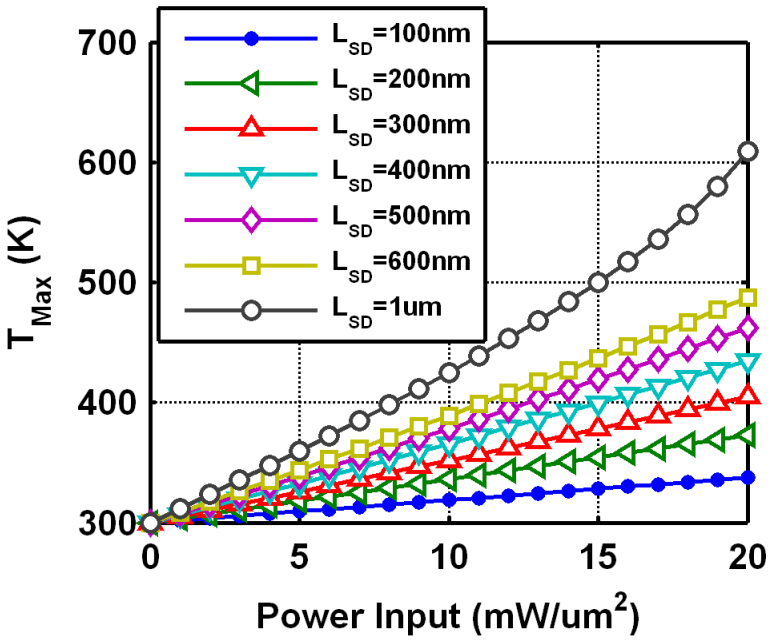
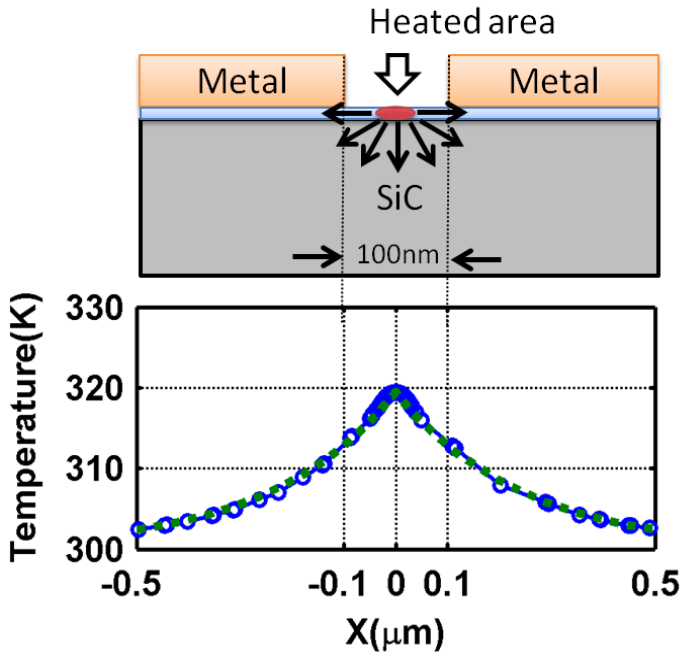


Figure 4.4. (a) Schematic of channel length varying thermal simulation with uniform power input over channel area (cut along x-z plane of 3-D simulation). Arrows indicate heat dissipation paths. (b) Simulated T_{Max} for various L_{SD}. Power input density is uniform for all cases

(a)



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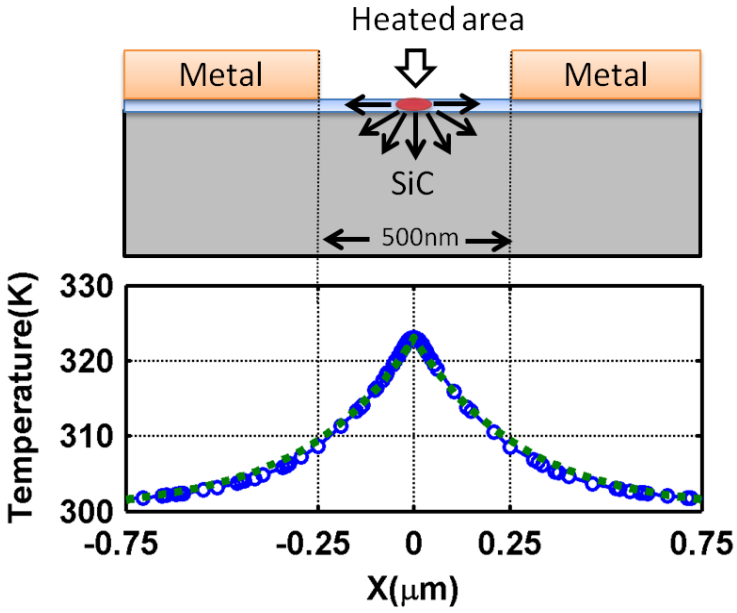
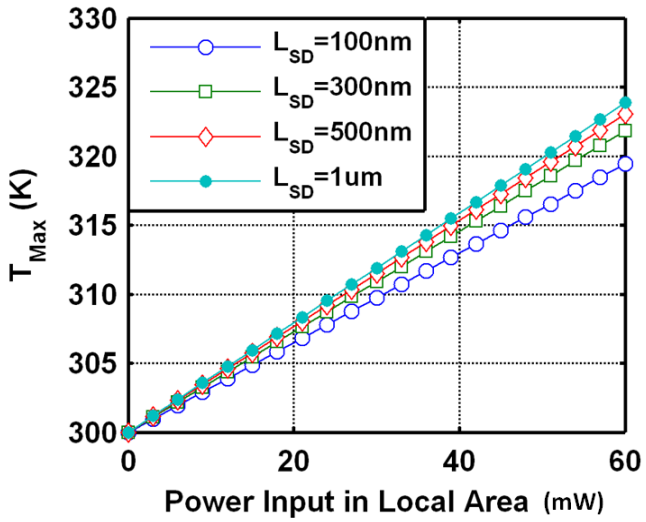


Figure 4.5. (a, b) Schematic of channel length varying thermal simulation with local heating (cut along x-z plane of 3-D simulation). Arrows are indicating heat dissipation paths. Lateral temperature profile (circles) and fitting curve (dashed line) is also shown.

(c)



(d)

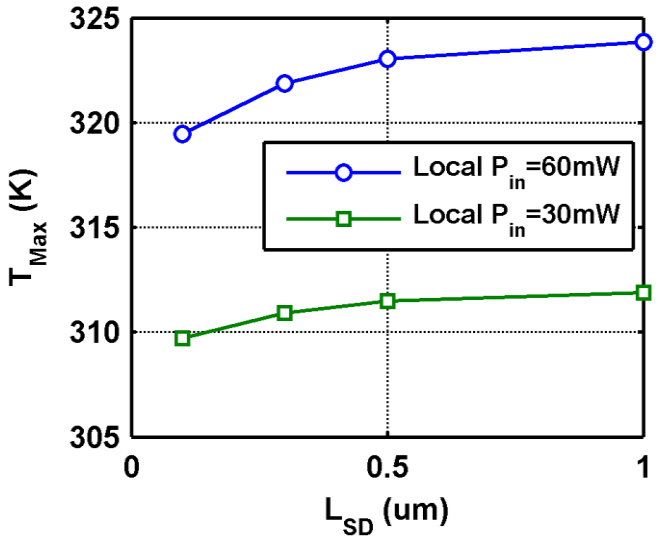


Figure 4.5. (continued) (c) Simulated T_{Max} vs. P_{in} for various L_{SD}, when local heating is applied to a 50nm width strip in the middle of the channel. (d) Simulated T_{Max} vs. L_{SD}

A localized heating area simulation can show the impact of contact spacing on lateral heat spreading. The simulation schematic is described in figure 4.5 (a) and (b), where we applied 50 nm length and 6μm width of limited local heat source at the middle

of the channel length of 100 nm and 500 nm, respectively. This allows the same total power input for devices with different contact spacing. Even though the absolute temperature rise in figure 4.5 (c) and (d) is smaller than in figure 4.4 (b) due to limited heating area and 3-D heat spreading, short channel devices have more benefit (~15% lower T_{Max}) from the lateral heat spreading into metal contacts. The limited relief to the hotspot in the middle of the channel is reduced with longer L_{SD}. Lattice temperature profile is also described in Figure 4.5 (a) and (b), which can be fitted by $T(x) = T_0 + T_{Max} \cdot e^{-|x|/L_c}$, where $T(x)$ is temperature vs. location, T_0=300 K, T_{Max} is maximum junction temperature at the middle of the channel, and L_c is characteristic length of exponential decay, which is 0.24 and 0.28 μm for 100 nm and 500 nm devices, respectively. An approximate value for L_c can be obtained in straight forward manner by $L_c=[\kappa_{lateral} \cdot R_{verical}]^{1/2}$ where $\kappa_{lateral}$ describes the lateral thermal conductivity of the graphene (or graphene plus overlying metal in the region under the contacts), and $R_{verical}$ describes the vertical thermal resistance area product (typically dominated by the interface thermal conductivity).

4.4. Device Fabrication and Measurement Method

An epitaxial graphene sample on Silicon Carbide (SiC) substrate was used for I-V test pattern fabrication. The graphene film was formed by sublimation of Si atoms from the surface of 6H-SiC substrate [26], and had carrier density of ~$8.5 \cdot 10^{12}$ cm^{-2} and Hall mobility of ~1,016 $cm^2V^{-1}s^{-1}$ [27]. A Ti-Pt-Au metal stack was used for ohmic contacts, then graphene is patterned by e-beam lithography followed by oxygen plasma

etching. Process details are the same as described elsewhere [8, 26], except there is no gate dielectric and top gate. The open channel devices which were used in this study have same configuration of source and drain contacts as RF transistors which were also fabricated on the same mask set. Most of measurements are done with 6 μm width, 0.5 μm length (source to drain spacing) devices.

Pulsed current vs voltage was measured for two-terminal non-gated epitaxial graphene devices over the temperature range of 225K~375K. The pulse measurement was conducted by a dynamic I-V analyzer (DiVA 265A) from Accent, and the sample was probed inside of a temperature controlled chamber. Before each measurement, we stabilized the sample for about 20 minutes after each temperature change to ensure the whole device reaches the desired temperature. The shortest pulse time we applied was 200 ns with 1 ms of pulse to pulse separation time.

4.5. Analysis on Pulsed I-V Measurement Results

Figure 4.6 shows the pulsed I-V measurement results at various temperatures. Since phonon scattering will increase at higher temperatures, electron and hole mobility of graphene film will be decreased [7, 28]. On the other hand, elevation of temperature results more electron-hole pair generation which contributes to lower the overall resistance of the graphene resistor. The temperature dependence of current is expected to be a combined effect of mobility and carrier generation with increasing temperature. The measured results emphasize the dominance of mobility degradation by rising temperature. The temperature dependence of pulsed current I_D was found to follow $I_D(T+\Delta T) = I_D(T)\cdot(1-\alpha\cdot \Delta T)$, and the extracted α is 0.002 /K for V_D of 2.3V.

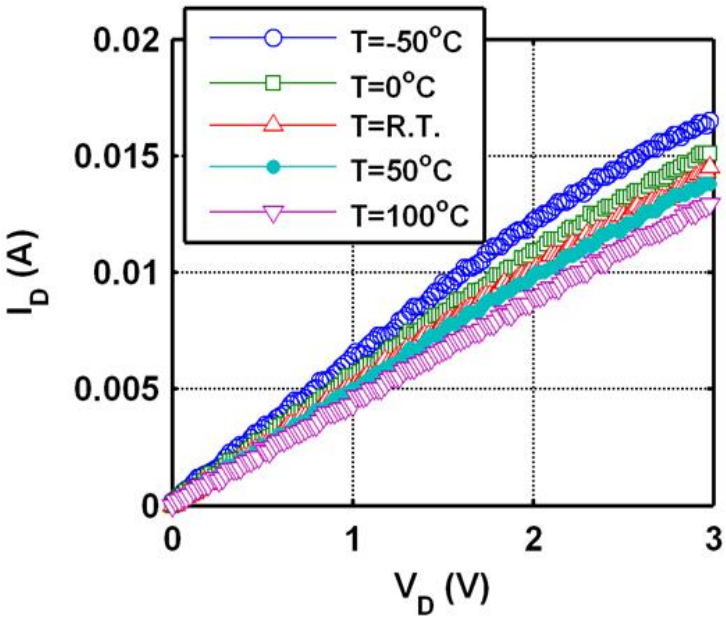
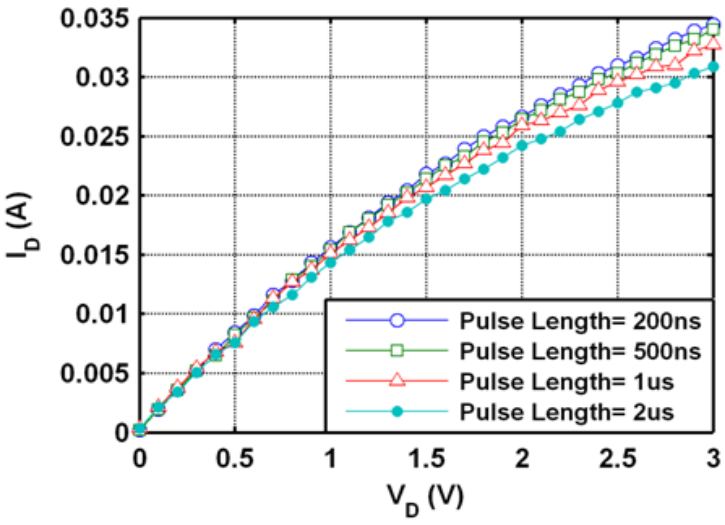


Figure 4.6. Measured pulsed I-V at various temperatures, with pulse length of 200 ns.

Figure 4.7 (a) displays pulsed I-V curves at room temperature with varying pulse time from 200 ns to 2 μs. Shorter pulse time gives higher current as a result of lower Joule self-heating. Self-heating is not eliminated completely, however, since 200 ns was the shortest pulse length we could apply, while reported time constants are in 30~300 ns range [12]. Simulations show that the heating transient departs dramatically from exponential behavior, and contains a wide range of time constants. In figure 4.7 (b), although the slope of I_D vs. pulse time decreases as pulse duration reduces, it is likely there is considerably more room to suppress Joule heating and increase the current level at even shorter pulse time. Therefore, the absolute T_{Max} value vs. P_{in} is hard to estimate from the measurement because of possible self heating from 200 ns pulse, even the self-heating is smaller than longer pulses or DC bias. The estimation of the

temperature difference ($T_{2\mu s}$-T_{200ns}) produced by self-heating of 200 ns and 2 μs pulses is 61ºC when V_D=2.3V.

(a)



(b)

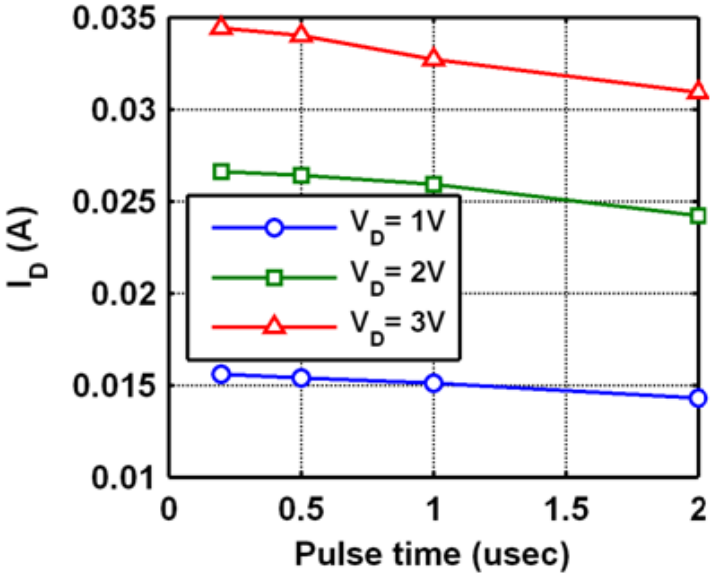


Figure 4.7. (a) Measured pulsed I-V characteristics with variable pulse durations. (b) I_D vs. pulse duration for various V_D values.

In actual measurements, the pulse shape in time domain cannot be an 'ideal' square wave (with zero pulse rise time). There is a finite rise time of the pulse about 20 ns which can affect the heating profile. Because the heat capacitance of the graphene layer is very small, self heating will occur immediately after power is applied. Effective heat capacitance of the device will be affected by substrate, capping layer [12], and structure of device. As we plotted in Figure 4.8, we emulated the power input pulse in the transient simulation with 20 ns ramp-up time. This simulation showed very rapid heating; temperature increment follows power rise without any delay until it reaches the peak of the pulse. After the pulse reaches its desired power level and holds, then temperature increases slowly (exponent time constant is applicable) with constant power level during the pulse duration. In this case, the simulations indicate there is self-heating in graphene devices even with pulse durations used in the measurement.

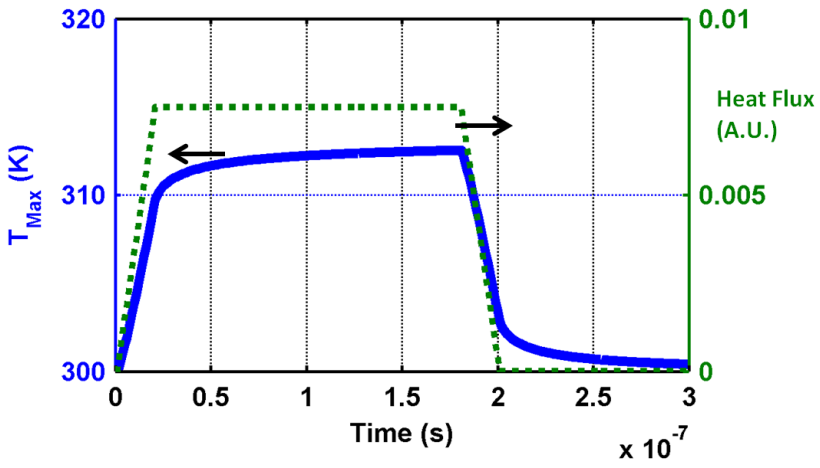


Figure 4.8. Transient simulation with 20 ns pulse rise time.

The measured currents for pulses of duration 2μs can be used together with the data of Figure 4.6 to estimate the thermal resistance of devices. If the entire nonlinearity of the I_D-V_D curve is assumed to be the result of heating, ΔT due to 2μs pulse can be estimated to be 158K for P_{in}= 20 mW/μm^2. The corresponding effective thermal resistance of the device R_{th} is $8 \cdot 10^{-5}$ K cm^{2}W^{-1}, in substantial agreement with the simulation results of figure 4.4 (b). This agreement tends to support the choices of R_{int} and of graphene lateral thermal conductivity used in the calculation. It is worthwhile noting that due to the superior thermal conductivity of SiC substrates, R_{th} of epitaxial graphene device is dramatically better than for suspended graphene device ~$1 \cdot 10^{-2}$ K cm^{2}W^{-1} (data from [29]). The effective thermal resistance is on the same order as (although better than) what can be estimated for Si devices on Si wafers of the same dimensions (~$1.5 \cdot 10^{-4}$ K cm^{2}W^{-1}, simulated without interface thermal resistance).

4.6. Conclusions

Joule self-heating of graphene rf devices is inevitable due to their small time constants and the need for driving high currents in the channel. This is minimized for grapheme on SiC due to high thermal conductivity of the substrate. A high quality graphene-substrate interface with high thermal conductivity substrate is important for lower thermal resistances. Shorter channel length is also favorable to utilize lateral heat spreading.

Chapter 4 in full, is a reprint of the material as it appeared in *Solid State Electronics* 2014, K. Lee and P. M. Asbeck. The dissertation author was the primary investigator and author of this paper.

4.7. References

[1] Novoselov, K.S.A., Geim, A.K., Morozov, S., Jiang, D., Katsnelson, M., Grigorieva, I., Dubonos, S. and Firsov, A., "Two-dimensional gas of massless Dirac fermions in graphene." Nature 438.7065 (2005): 197-200

[2] Lee, C., Wei, X., Kysar, J.W. and Hone, J., "Measurement of the elastic properties and intrinsic strength of monolayer graphene." Science, 321.5887 (2008): 385-388

[3] Wang, F., Zhang, Y., Tian, C., Girit, C., Zettl, A., Crommie, M. and Shen, Y.R., "Gate-variable optical transitions in graphene." Science, 320.5873 (2008): 206-209

[4] Balandin, A.A., Ghosh, S., Bao, W., Calizo, I., Teweldebrhan, D., Miao, F. and Lau, C.N., "Superior thermal conductivity of single-layer graphene." Nano letters, 8.3 (2008): 902-907

[5] Pop, E., Varshney, V. and Roy, A.K., "Thermal properties of graphene: Fundamentals and applications." MRS Bulletin, 37, (2012): 1273–1281

[6] Novoselov, K.S., Jiang, Z., Zhang, Y., Morozov, S.V., Stormer, H.L., Zeitler, U., Maan, J.C., Boebinger, G.S., Kim, P. and Geim, "Room-temperature quantum Hall effect in graphene." Science, 315.5817 (2007): 1379-1379

[7] Bolotin, K.I., Sikes, K.J., Jiang, Z., Klima, M., Fudenberg, G., Hone, J., Kim, P. and Stormer, H.L., "Ultrahigh electron mobility in suspended graphene." Solid State Communications, 146.9 (2008): 351-355

[8] Moon, J.S., Curtis, D., Hu, M., Wong, D., McGuire, C., Campbell, P.M., Jernigan, G., Tedesco, J.L., VanMil, B., Myers-Ward, R. and Eddy Jr, C., "Epitaxial-graphene RF field-effect transistors on Si-face 6H-SiC substrates." Electron Device Letters, IEEE 30.6 (2009): 650-652

[9] Lin, Y.M., Dimitrakopoulos, C., Jenkins, K.A., Farmer, D.B., Chiu, H.Y., Grill, A. and Avouris, P., "100-GHz transistors from wafer-scale epitaxial graphene." Science, 327.5966 (2010): 662-662

[10] Conway, A.M., Asbeck, P.M., Moon, J.S. and Micovic, M., "Accurate thermal analysis of GaN HFETs." Solid-State Electronics, 52.5 (2008): 637-643

[11] E. H. Hwang and S. Das Sarma. "Acoustic phonon scattering limited carrier mobility in two-dimensional extrinsic graphene." Physical Review B, 77.11 (2008): 115449

[12] S. Islam, et al. "Role of Joule Heating on Current Saturation and Transient Behavior of Graphene Transistors." IEEE Electron Device Letters, 34, (2013): 166-168

[13] Liao, A.D., Wu, J.Z., Wang, X., Tahy, K., Jena, D., Dai, H. and Pop, E., "Thermally limited current carrying ability of graphene nanoribbons." Physical Review Letters, 106.25 (2011): 256801.

[14] Semenov, O., Vassighi, A. and Sachdev, M., "Impact of self-heating effect on long-term reliability and performance degradation in CMOS circuits."Device and Materials Reliability, IEEE Transactions on, 6.1 (2006): 17-27

[15] Levinshtein, M.E., Rumyantsev, S.L. and Shur, M.S., "Properties of Advanced Semiconductor Materials: GaN, AIN, InN, BN, SiC, SiGe." Wiley.com (2001)

[16] Li, X., Kong, B.D., Zavada, J.M. and Kim, K.W., "Strong substrate effects of Joule heating in graphene electronics." Applied Physics Letters, 99.23 (2011): 233114-233114

[17] Koh, Y.K., Bae, M.H., Cahill, D.G. and Pop, E., "Heat conduction across monolayer and few-layer graphenes." Nano Letters, 10.11 (2010): 4363-4368

[18] E. T. Swartz and R. O. Pohl, "Thermal boundary resistance." Reviews of Modern Physics, 61.3 (1989): 605

[19] Burgemeister, E.A., Von Muench, W. and Pettenpaul, E., "Thermal conductivity and electrical properties of 6H silicon carbide." Journal of Applied Physics, 50.9 (1979): 5790-5794

[20] Joshi, R.P., Neudeck, P.G. and Fazi, C., "Analysis of the temperature dependent thermal conductivity of silicon carbide for high temperature applications." Journal of Applied Physics, 88.1 (2000): 265-269

[21] Cai, W., Moore, A.L., Zhu, Y., Li, X., Chen, S., Shi, L. and Ruoff, R.S., "Thermal transport in suspended and supported monolayer graphene grown by chemical vapor deposition." Nano Letters, 10.5 (2010): 1645-1651

[22] Sadeghi, M.M., Pettes, M.T. and Shi, L., "Thermal transport in graphene." Solid State Communications, 152.15 (2012): 1321-1330.

[23] Bae, M.H., Li, Z., Aksamija, Z., Martin, P.N., Xiong, F., Ong, Z.Y., Knezevic, I. and Pop, E., "Ballistic to diffusive crossover of heat flow in graphene ribbons." Nature Communications, 4 (2013): 1734

[24] Freitag, M., Steiner, M., Martin, Y., Perebeinos, V., Chen, Z., Tsang, J.C. and Avouris, P., "Energy dissipation in graphene field-effect transistors." Nano Letters, 9.5 (2009): 1883-1888

[25] Weingart, S., Bock, C., Kunze, U., Speck, F., Seyller, T. and Ley, L., "Low-temperature ballistic transport in nanoscale epitaxial graphene cross junctions." Applied Physics Letters, 95.26 (2009): 262101-262101

[26] VanMil, B.L., Myers-Ward, R.L., Tedesco, J.L., Eddy, C.R., Jernigan, G.G., Culbertson, J.C., Campbell, P.M., McCrate, J.M., Kitt, S.A. and Gaskill, D.K., "Graphene formation on SiC substrates." Materials Science Forum. Vol. 615. 2009

[27] Moon, J.S., Seo, H.C., Antcliffe, M., Lin, S., McGuire, C., Le, D., Nyakiti, L.O., Gaskill, D.K., Campbell, P.M., Lee, K.M. and Asbeck, P., "Graphene FET-based zero-bias RF to millimeter-wave detection." IEEE Electron Device Letters, 33, 10, (2012): 1357–1359

[28] E. H. Hwang and S. Das Sarma. "Acoustic phonon scattering limited carrier mobility in two-dimensional extrinsic graphene." Physical Review B, 77.11 (2008): 115449

[29] Dorgan, V.E., Behnam, A., Conley, H.J., Bolotin, K.I. and Pop, E., "High-field electrical and thermal transport in suspended graphene." Nano Letters, 13. 10, (2013): 4581–4586

Chapter 5

R.F. Circuit Applications of Graphene FETs: Zero-Biased R.F. Power Detector and Resistive Mixer

In this chapter, we investigate the potential performance of graphene FETs (GFET) for r.f. applications. In order to understand the device parameters' relation to the circuit performances, a compact model of GFETs was developed for circuit simulations (Chapter 5.2.1). Analytic expressions of an abstracted model have also been used to understand the impacts in device parameters on performance in circuit applications (Chapter 5.2.2). R.f. circuit simulations are done with these device models in sections 5.3, 5.4, and 5.5, where r.f. to millimeter-wave power detector and linear resistive mixer

based on GFETs were investigated. This work has contributed to publications [1] and [2], where the experimental measurements are well supported by simulation results in this chapter.

5.1. Introduction

Based on high carrier mobility and saturation current, graphene channel devices have emerged as strong candidates for active devices in r.f. circuit applications. Although GFETs lack high I_{on}/I_{off} ratio, which is essential for logic applications, the characteristics of graphene shows significant potential for high speed r.f. devices. GFETs showed high f_T on both epitaxial graphene [3, 4] and transferred CVD graphene [5, 6], and also, have been proven to have potential compatibility with current planar CMOS technologies [6]. Moreover, graphene-based devices have potential to be used as a platform of electronics on flexible or non-planar substrates [7, 8], due to their atomically thin film nature.

Figure 5.1 displays a schematic of a GFET made with epitaxial graphene on SiC (a), its SEM image (b), and representative I_d-V_d (c) and I_d-V_g (d) characteristics [9]. The experimental graphene film was grown by Naval Research Laboratories, and devices were fabricated and tested in HRL laboratories. The epitaxial graphene layers were grown on Si-face 6H-SiC substrates via Si sublimation. The film shows n-type nature with the sheet electron density of ~8.5 x 10^{12} cm^{-2} at room temperature. Electron mobility was measured as ~1,016 cm^2/Vs. For the FET fabrication, graphene channel was defined by O_2 plasma etching. Ti/Pt/Au metal stacks were used for source and drain contact, fabricated by lift-off process. TLM measurement showed < 0.1 Ω·mm of contact

resistance. The metal gates were processed on top of HfO_2 gate dielectric which was deposited by atomic layer deposition (ALD).

Fabricated GFETs are used for experimental test for r.f. power detector and resistive mixer, with connections described in section 5.3.1 and 5.5.1. GFET modeling and fitting are based on measured characteristics of the device.

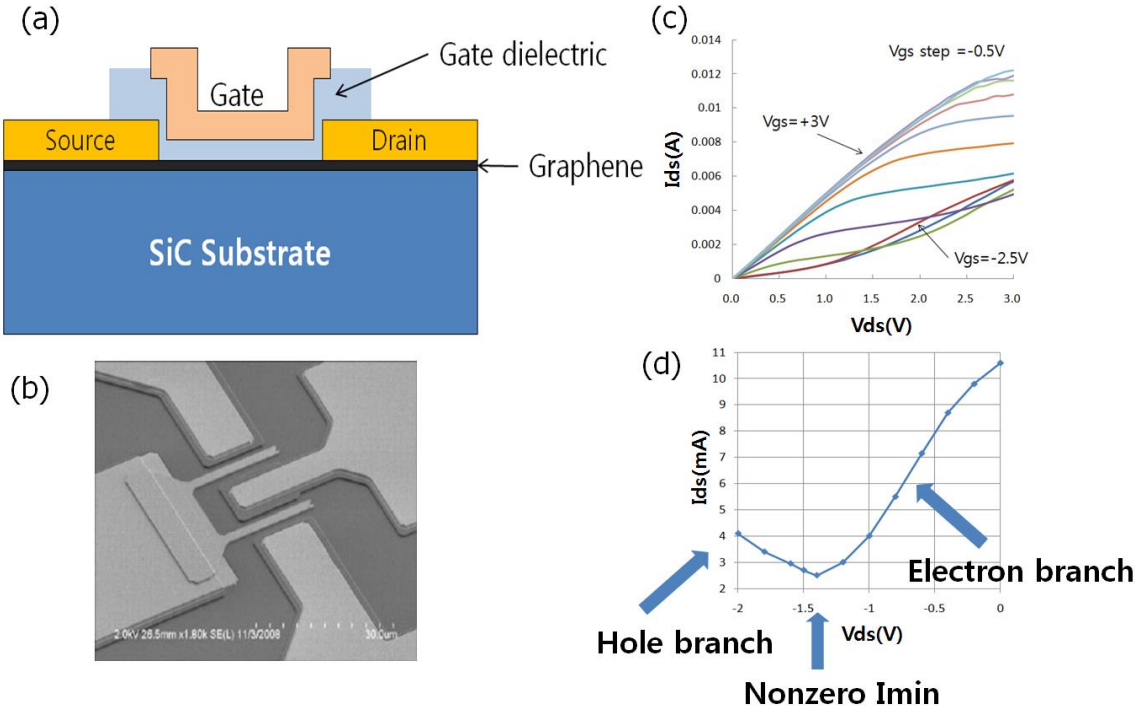


Figure 5.1 (a) Schematic of graphene FET structure based on epitaxial graphene on SiC substrate (vertical cut) (b) SEM image of r.f. Graphene FET with two gate fingers (c) Representative I_d-V_d curve of graphene FET. Width is 6 μm, channel length is 3 μm. (d) Representative Id-Vg curve of GFET. Electron and hole conduction branches are shown on each side of the Dirac point.

Because of the zero bandgap nature of graphene, it is difficult to turn off the graphene FET. The characteristics show a minimum conduction point (Dirac point) with

V-shaped ambipolar I_d-V_g curve which can be utilized for frequency doubler applications [9, 10]. The I_d-V_d curve shows a saturation behavior as in conventional MOSFETs, however, the current increases again at higher V_{ds} due to the hole injection from the drain side rather than having a depleted channel near the drain region of conventional FET. GFET has linear I_d-V_d relation at small bias condition, which makes it useful for a linear resistive mixer. It is favorable to use a highly linear resistance region for mixing because it generates very low intermodulation than mixers with nonlinear devices [11]. High carrier mobility and large I_{max} also supports graphene as an excellent candidate for high frequency mixer applications.

5.2. Graphene FET models for circuit simulation

5.2.1. Compact model: Back to back connected FETs (BBCF)

In order to establish a simple methodology to use SPICE modeling to represent graphene FETs, a compact model consisting of back-to-back connected n-type and p-type FETs was developed. A top-gated, n-type epitaxial graphene FET on SiC substrate is assumed. Figure 5.2 (a) shows the configuration of back-to-back connected FETs for describing the ambipolar behavior of I_d-V_g curves of graphene FETs. While the sources are grounded and a single V_d is applied for both FETs, the gate bias controls the channel current of nFET and pFET simultaneously. nFET will turn on with $V_g > V_{th\_nFET}$ and pFET will be mostly turned off for this condition. pFET is turned on with V_g less than V_{th_pFET} while nFET is off at the same bias condition. nFET will depict the electron branch of the typical ambipolar I_d-V_g curve of GFET, and pFET current corresponds to the hole branch. Figure 5.2 (c) is the fitted I_d-V_g curve of the BBCF to the measurement

result [9], figure 5.2 (b). Table 5.1 summarizes device paramters used for nFET and pFET for SPICE model. Additional p-n junction resistance of 400 Ω•μm was added for pFET (hole branch) as discussed in Chapter 2.

Table 5.1. Device parameters for GFET compact model based on BSIM3 model

	NMOS	PMOS
T_{ox}	15 nm	15 nm
μ_0	5000 cm / V s	5000 cm / V s
V_{th0}	-1.7 V	-1.5 V
v_{sat}	4e5 cm/s	4e5 cm/s
L_g	3 μm	3 μm
W_g	6 μm	6 μm
R_c	450 Ω•μm	450 Ω•μm
R_{pn}		400 Ω•μm

The FET model is utilizing BSIM3 model, which is also included in circuit simulator packages for easy use. The equation for the drain current without parasitic drain/source resistance is given below [ ]:

$$I_{ds0} = \mu_{eff} C_{ox} \frac{W}{L} \frac{V_{gsteff}\left(1 - A_{bulk}\frac{V_{dseff}}{2(V_{gsteff} + 2V_{tm})}\right)V_{dseff}}{1 + \frac{V_{dseff}}{E_{sat}L}}$$

where μ_{eff} is effective mobility, C_{ox} is gate capacitance, W and L are channel width and length, respectively. V_{gsteff} is the effective (V_{gs}-V_{th}) voltage, V_{dseff} is effective drain source voltage with consideration of velocity saturation (V_{dsat} parameter included), V_{tm} is temperature voltage, defined as (kBT)/q. A_{bulk} is bulk charge effect coefficient, and E_{sat} is velocity saturation electric field. For full models and details, please refer to "BSIM3 Manual" [12].

In order to utilize BSIM3 models for graphene FET simulations, high mobility values are used for both NMOS and PMOS. C_{ox} value can deviate from geometric capacitance due to smaller density of states of graphene (than Si), especially near the Dirac point. Threshold voltage (V_{th}) for both FETs are important fitting parameters to fit the minimum conduction current level and bias condition.

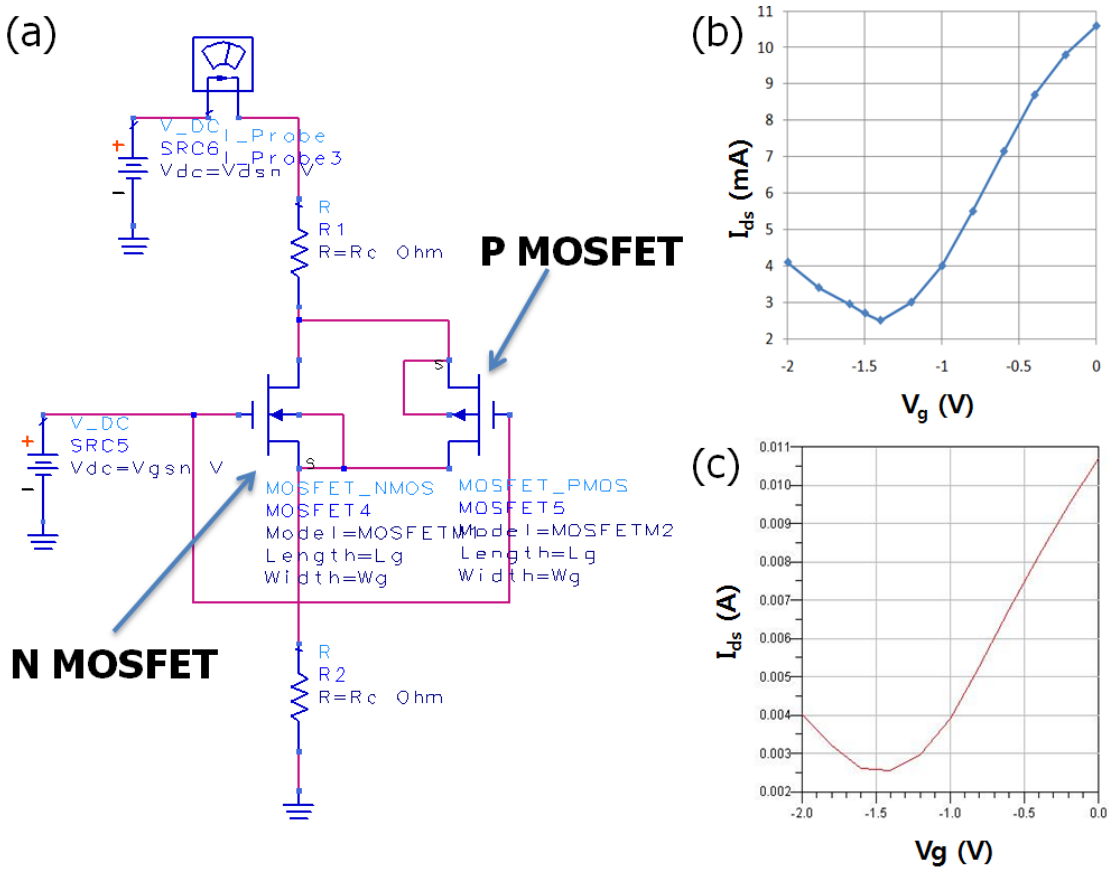


Figure 5.2. (a) Compact model of GFET for circuit level simulations as appeared in ADS simulation. N MOSFET and P MOSFET are connected back-to-back to describe the ambipolar behavior of GFET. (b) I_d-V_g measurement result of GFET [9] (c) Fitted I_d-V_g curve with GFET compact model

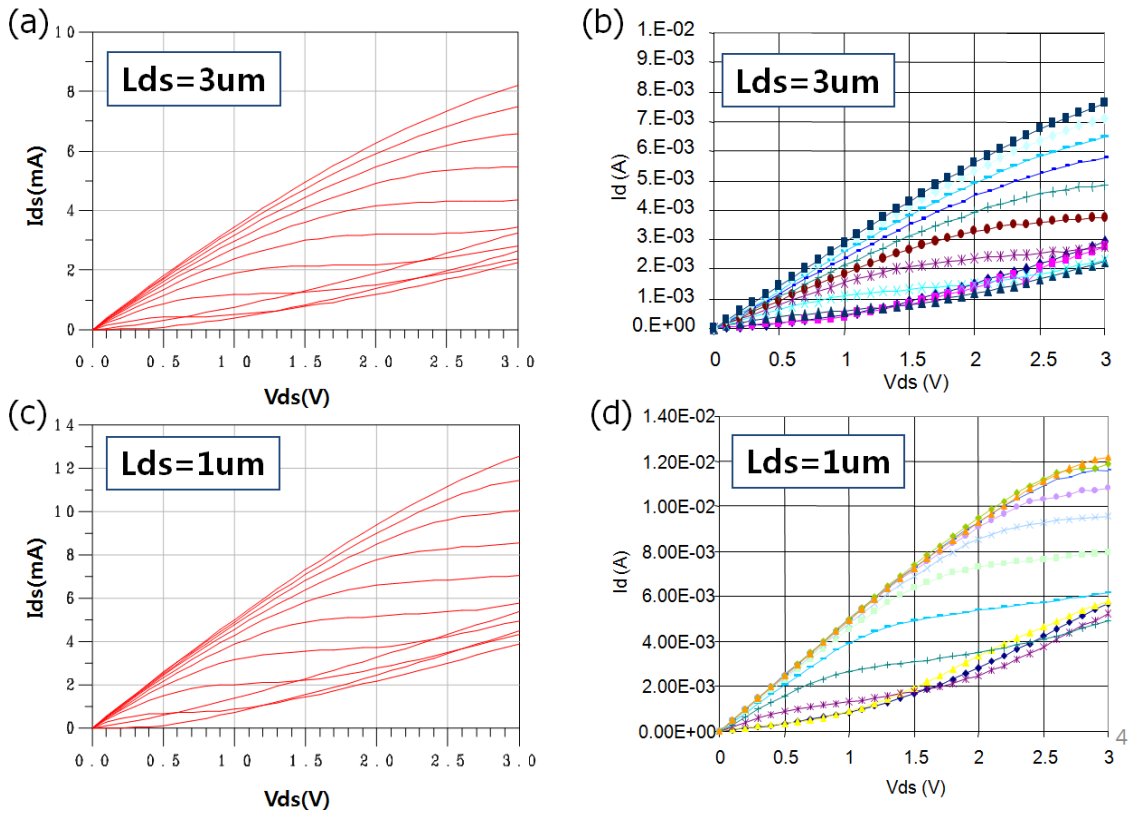


Figure 5.3. (a) Simulated I_d-V_d curves for GFET with L_{ds}= 3 µm (b) I_d-V_d measurement result of GFET with L_{sd}= 3 µm (c) Simulated I_d-V_d curves for GFET with L_{ds}= 1 µm (b) I_d-V_d measurement result of GFET with L_{sd}= 1 µm. Measurement results: courtesy of HRL Laboratories.

In figure 5.3, simulated results of I_d-V_d are compared with measurement data (measured in HRL Laboratories) for GFETs of channel length of 1 µm and 3 µm. Device parameters were tuned to have a good fitting of I_d-V_g curves (figure 5.2). The model was then found todescribe the characteristics of I_d-V_d curves reasonably well, such as saturation and p-channel turn-on behavior at higher drain bias, without additional parameter adjustment. Between two devices of different channel lengths, L_{sd} is the only modified parameter in the simulation, which also showed reasonable results. The BBCF

model provides with a simple but physical description of characteristics of graphene FETs.

5.2.2. Abstract model

The compact model described in the previous section is easy to use with simulation tools based on SPICE models. However, an analytic expression of the FET model would be useful to investigate the impact of device parameters on circuit performance in a more abstract, behavioral fashion. We extracted an abstract model, which represents GFET I_d as a function of V_g and V_d, using Taylor series to represent measurement results over a narrow current range around a particular bias point, as follows:

$$I_d = V_{ds} (a_0 + a_1 V_{gs} + ½ a_2 V_{gs}^2)$$

a_1 and a_2 are nonlinearity coeffecients which are extracted from first and second derivatives of the drain current of GFET with respect to V_g. Figure 5.4 (a) shows a circuit diagram using the abstracted model as a “black box” device with a_0 ~ a_2 parameters, where we can easily test the impact of a_0, a_1 and a_2 coefficients on the performance of basic nonlinear circuits. Figure 5.4 (b) shows the s-parameter simulation result of GFET abstracted model, which is very similar to the measured result (Figure 5.4 (c)). Capacitances were included in the model to correspond with the measured frequency responses.

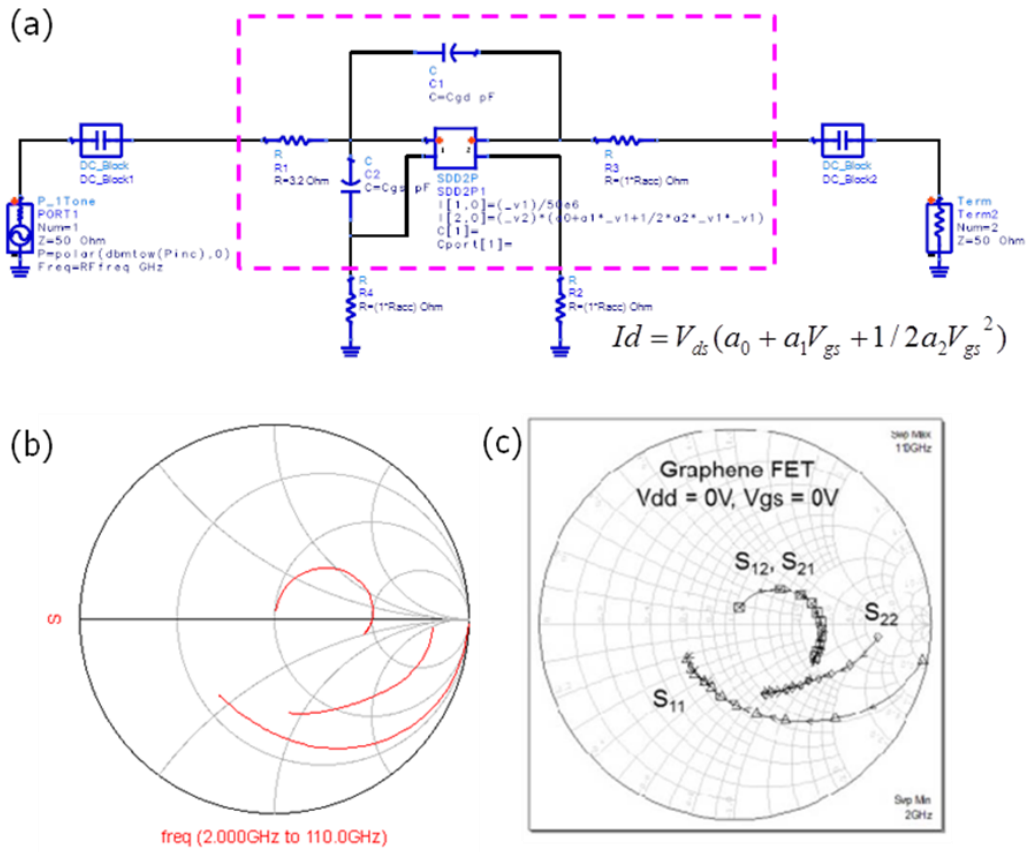


Figure 5.4 (a) Circuit diagram using abstracted model with parasitic elements as a 2-terminal box device, which uses V_g and V_d as input and calculated I_d from the abstracted model for output. (b) s-parameter simulation result using the abstracted model of GFET (c) measurement s-parameter of GFET [1].

GFET device is 6 μm wide, 2 gate fingers (effective width is 12 μm). Additional device paramters used in the simulation are, L_{sd} = 1 μm, L_{gate} = 0.5 μm, W = 12 μm, R_g = 3.2 Ohm, E_g = 0.001 eV, μ_0 = 4,500 cm^2/V s, V_{th_n}= -10.36 V, V_{th_p} = -3.1 V, R_s, R_d=160 Ohm. R_s and R_d are calculated from mobility, expected carrier density of non-gated area, physical gap distance between gate edge and source/drain edges and contact resistance. T_{ox} (or EOT) was used as a fitting parameter due to the difference from BSIM model and the actual measured effective C_{ox} value from GFET. Such a difference could be caused

by difference of density of states from graphene to Si, interface trap densities, and border traps in high-k dielectrics. Therefore, we used a generic value of thick T_{ox} to fit the R-V_g curve, then external C_{gs} = 3.3 pF/mm and C_{gd} = 3.6 pF/mm were added to have similar s-parameter simulation results with the measured data.

5.3. Graphene FET-Based RF to millimeter-wave detector

Direct r.f. power detection is common for power monitoring and control in mobile communications. For higher frequencies, detection of power of signals in the range 100-800 GHz range is of interest for passive thermal imaging applications such as imagers in limited visibility environments [13], security applications [13, 14], and general temperature sensors. In such applications radiation at hundreds of GHz is collected and rectified by the detector circuit for each pixel to produce a dc voltage output.

Various devices such as diodes [15], bipolar transistors [16] and FETs [17] have been used for r.f. power detectors. Highly integrated CMOS based power detector with square-law operation have also been demonstrated [18]. Although each technology showed promising results, the limits of the detector was also shown such as narrow bandwidth, power consumption and limited sensitivity due to flicker noise. A good linearity with wide dynamic range and low noise characteristics are required for wideband, high sensitivity detectors.

With zero bias current detection circuits, 1/f noise can be minimized because there is no DC current flow during the operation [1]. The Johnson (white) noise still remains, which is proportional to the junction or channel resistance. This contribution needs to be controlled by proper layer design or gate bias control to lower the resistances.

Noise equivalent power (NEP) is one of key metrics for detector, determined by equivalent input noise divided by reponsivity. Responsivity is defined by the ratio of input power to output voltage (V_{out}) delivered by the detector. The responsivity is approximately independent of input power for square law detectors.

In this section, we report ADS circuit simulation based on device models described in previously in section 5.2, to analyze the impact of device parameters such as nonlinearity coefficients, parasitic components, load resistance on the performance of r.f. power detectors. Simulated results provide a guideline for the optimization of device and circuit design of GFET based power detectors.

5.3.1. Detector operation and simulation setup

The schematic of the GFET based power detector circuit [1] is displayed in Figure 5.5, featuring the 'back-to-back connected FETs' compact model for the ADS circuit simulation. All parasitic components such as C_{gd}, C_{gs}, R_g, gate capacitance, and series resistances R_s and R_d are included in the full model.

DC gate bias can be applied to get the proper offset for optimized operating condition. The r.f. power input is also connected to the gate. The input signal is coupled to the drain via C_{dg} together with an additional capacitor connected in parallel. The r.f. signal is rectified by gate-drain coupling of the device, giving a DC output (V_{out}) measured from the R_{load} at the drain. In this zero-biased diode-connected FET structure for the detector, the r.f. input signal to the gate modulates not only the channel, but also the drain at the same time. The input AC voltage of $V_{g.AC}$ is coupled with the drain node,

and finally $V_{g.AC}=V_{d.AC}$. Effective modulation will be the product of these two components.

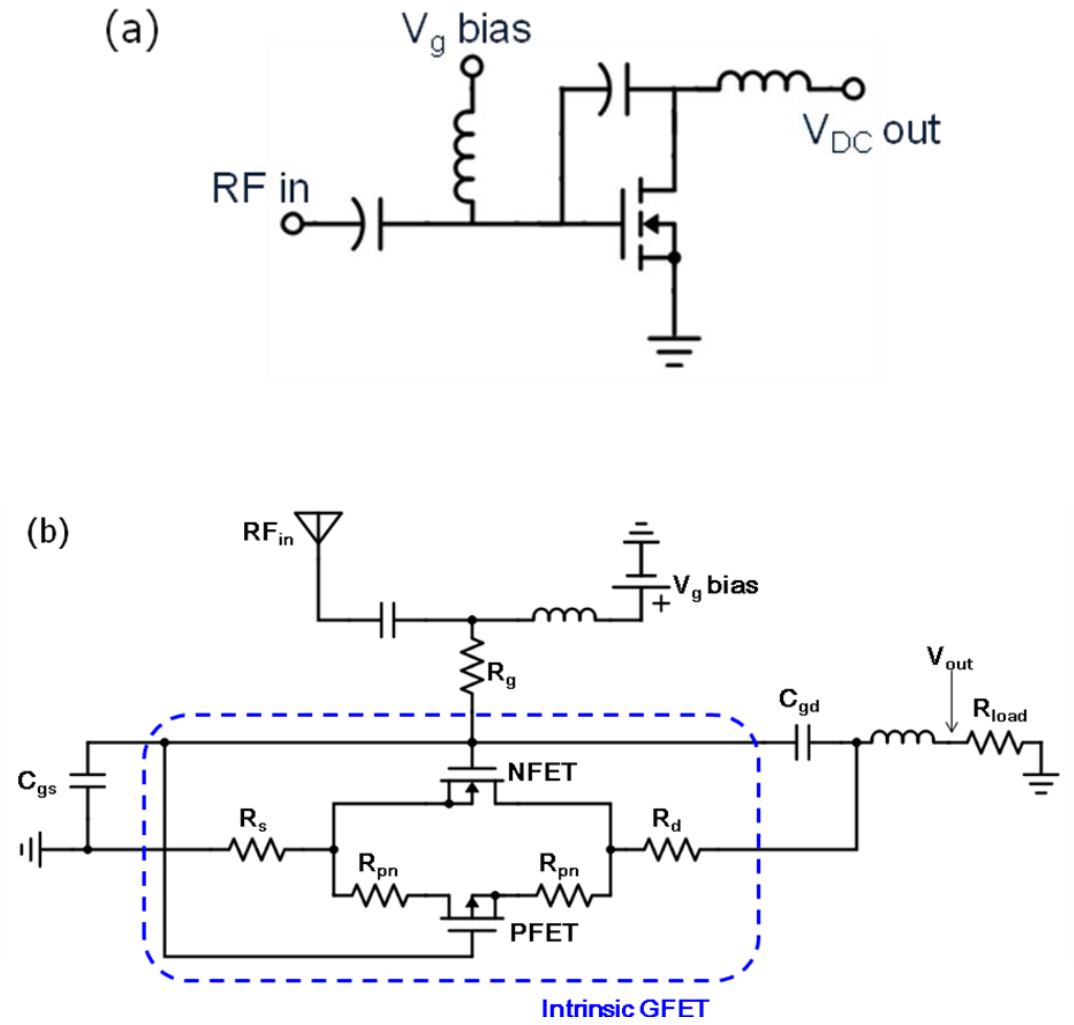


Figure 5.5. (a) Schematic of power detector system (b) A circuit diagram of the power detector with full model of GFET including parasitic elements

This design of detector circuit features no dc power dissipation due to zero drain bias operation. Moreover, noise sources are limited to thermal noise because shot noise and flicker noise is suppressed with no DC current. In various circuit applications, circuit

doesn't require matching network, so it can be broadband as well as being compact. For highly scaled array applications, each detector can be connected directly to an antenna. For the highest responsivity performance, input impedance matching can be used, at the cost of limited bandwidth and circuit area.

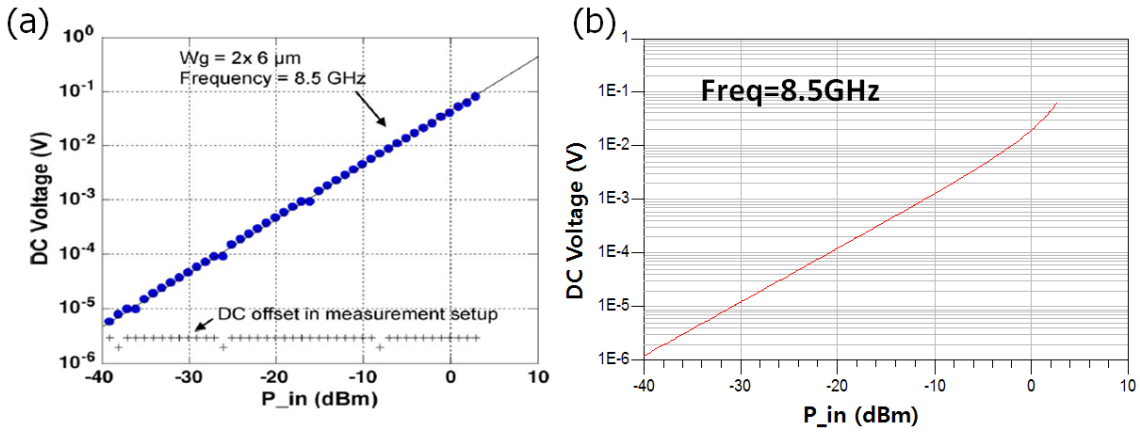


Figure 5.6. Input power (P_{in}) vs. output voltage (V_{out}) plot of GFET power detector (a) measurement result [1] (b) simulated result

Graphene FET device described in section 5.1 has been used for detector demonstration, set as Figure 5.5 (a), with RF_load termination of 50 Ω. Open structure DC measurement shows the output voltage of ~10 μV, which is used as the background DC offset for a calibration of detection voltage (Figure 5. 6 (a)). s-parameters are measured with HP85109 XF network analyzer to calculate the RF power delivered to the graphene FETs and the DC output voltage responsivity.

Baseline simulation was done with input frequency of 8.5 GHz and power level of -40 ~ 0 dBm, following the measurement condition in [1]. Both gate and drain bias were set to 0 V, however the gate bias can be controlled to set the FET at the optimized

condition. Intrinsic and extrinsic device parameters and parasitic components were fitted to have a good agreement with the measurement result. Figure 5.6 is a representative (a) measurement and (b) simulation result of power input (P_{in}) versus rectified output voltage (V_{out}). Device parameters affecting the performance of the detector will be discussed in the following section.

5.3.2. Intrinsic device parameters related to the sensitivity of detector

In order to understand the impacts of device parameters on the detector performance, the abstract model (Section 5.2.2.) was used with analytic expressions. First we investigated the device parameters with varying bias conditions, then the optimization of responsivity was performed based on external parameters such as pad capacitance and series resistance of the FET. All baseline circuit simulations were done with frequency of 8.5 GHz and -40 to 0 dbm of r.f. input power under zero DC bias condition.

Figure 5.7 (a) shows simulated curve the change of SD resistance vs. gate bias, fitted to the measurement result. Parasitic elements of $C_{pad} = 0.6$ pF, $R_s + R_d = 40\ \Omega$ were used. When V_g is near V_{Dirac}, both resistance and g_m increases. When the gate bias is applied to have a higher transconductance condition, the detector shows improved Vout as shown in figure 5.7 (b). In other words, responsivity (defined as output voltage over input power) increases when the device is operating at higher non-linearity regime. We would like to note that noise consideration is also an important factor to find the optimum operation condition. Because increased channel resistance at small $|V_g\text{-}V_{Dirac}|$ causes more thermal noise, which will make the noise equivalent power larger and limit the sensitivity of the detector.

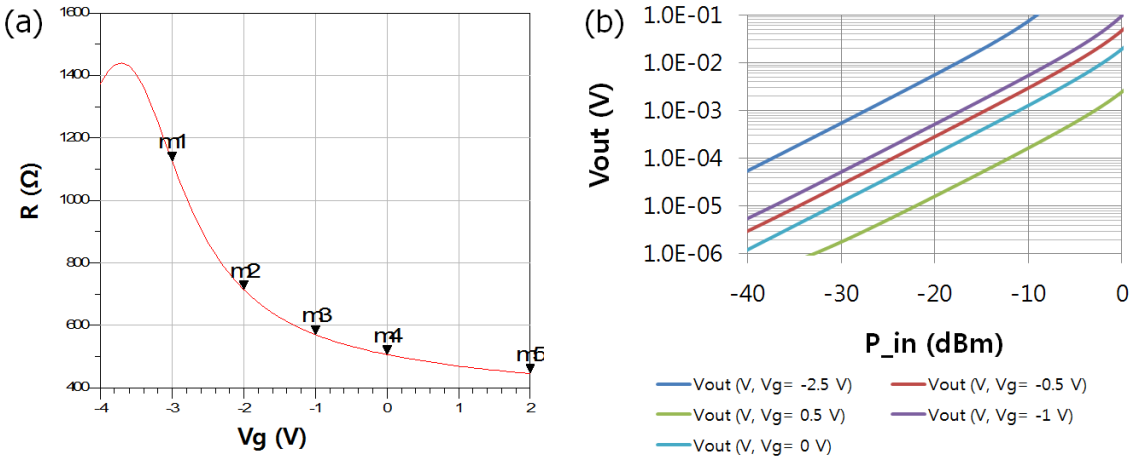


Figure 5.7. (a) R vs V_g plot of GFET. (b) V_{out} vs. P_{in} plot with V_g variation.

From the abstract model, we can investigate which non-linear coefficient is important for sensitivity of the detector. We simulated the detector operation with swept values of a_1 and a_2 coefficients of following analytic expression of drain current as a function of V_g and V_d. a_0, a_1, and a_2 coefficients are only valid for a small range, so they need to be adjusted for different bias conditions.

$$I_d = V_{ds} (a_0 + a_1 V_{gs} + \tfrac{1}{2} a_2 V_{gs}^2)$$

a_0 corresponds to a linear resistance component while a_1 represents the non-linearity of the FET detector. Figure 5.8 (a) shows the increment of V_{out} of the detector when a_1 coefficient increases. V_{out} is a sensitive function of a_1 value. a_1 is affected by non-linearity and junction resistance R_j, both are functions of V_g and V_d, which can be

optimized to maximize the responsivity of the detector. a_2 variation shows it has more impact when P_{in} is larger, however it shows a weaker dependency than a_1.

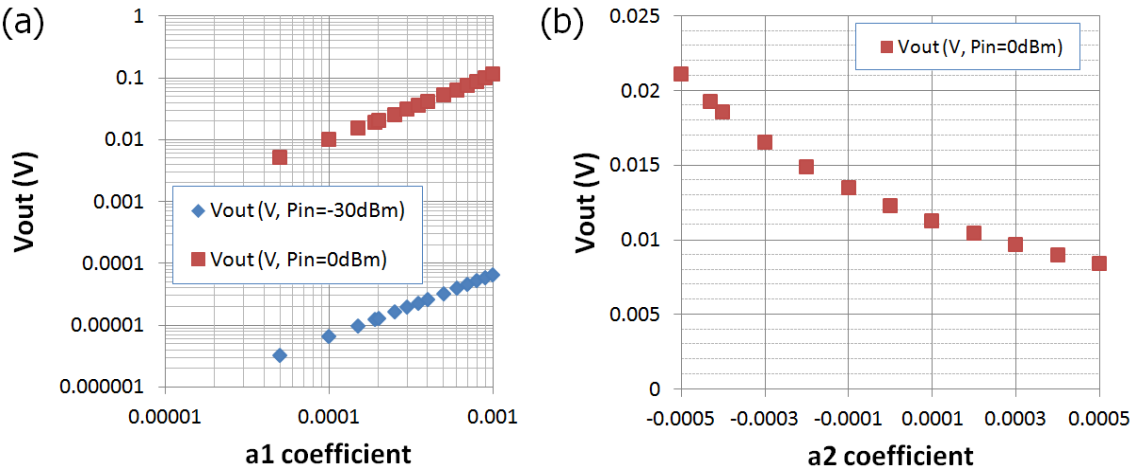


Figure 5.8. (a) Output voltage variation with a_1 coefficient at P_{in}=0 and -30 dBm. (b) Output voltage variation with a_2 coefficient

5.4. Optimization of GFET based r.f. power detector

5.4.1. Power Incident and Noise Considerations

In previous discussions, we calculated the V_{out} of the detector in terms of the actual input power delivered to the detector FET from a source (such as antenna) with 50 Ω source impedance R_s. This delivered power (P_{in}) could be calculated by subtracting the reflected power from the total incident power. However, in order to build a practical system, it would be helpful to estimate the realistic characteristics of device with consideration of extrinsic components of the detector system, such as parasitic capacitance, input impedance, and noise with consideration of as-is incident power input (P_{inc}) from the source (also known as available power of the source). Figure 5.9 displays

the schematic of power detector appeared in ADS simulator, including parasitic elements and noise sources such as Flicker noise and thermal noise.

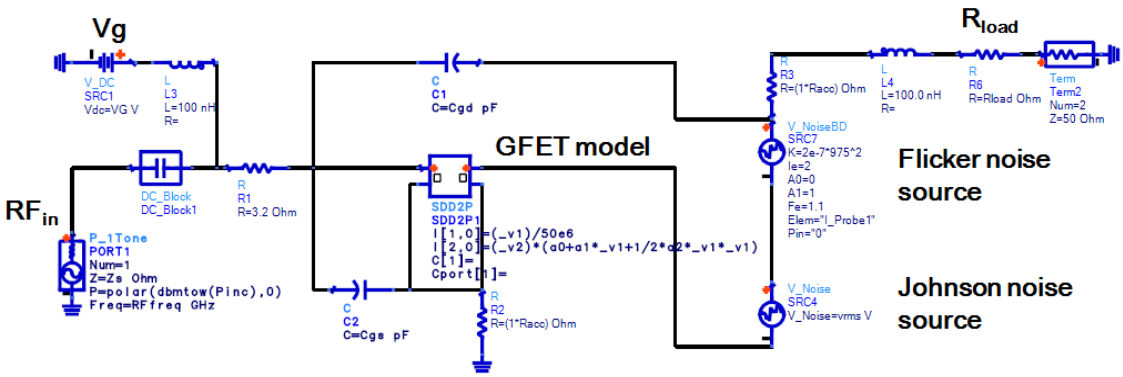


Figure 5.9. Schematic of power detector with noise source

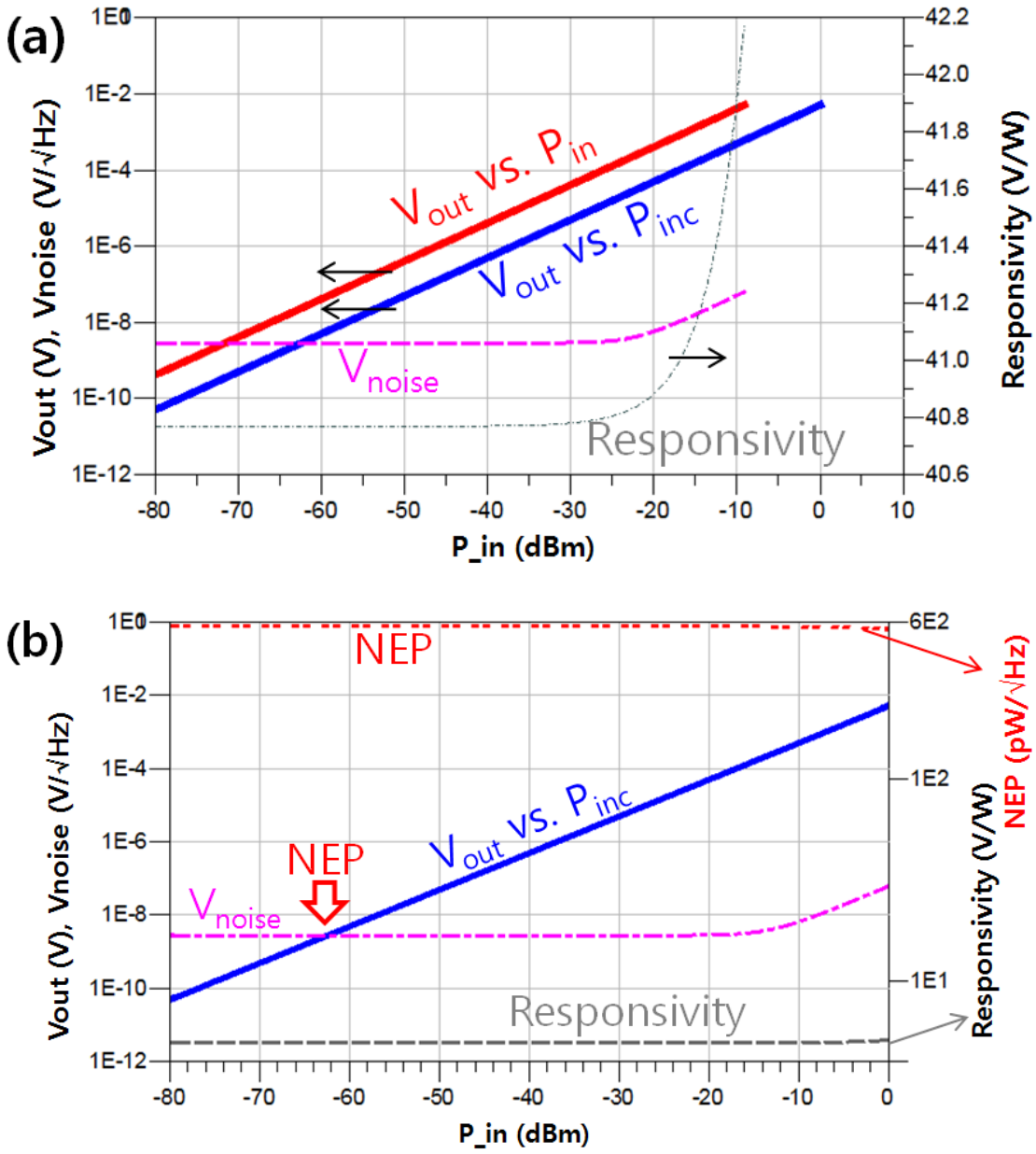


Figure 5.10. (a) Representative V_{out} vs. P_{in} plot with comparison of incident power (P_{inc}) versus delivered power (P_{in}). (b) Simulated V_{out} vs. incident power (P_{inc}) of unbiased graphene FET based power detector. Noise voltage (pink dot-dash line), responsivity (~40 V/W, gray dash), and noise equivalent power (NEP, red dot-dot) were also plotted.

In figure 5.10 (a), comparison of output voltage (V_{out}) between using incident power (P_{inc}) and delivered power (P_{in}) shows obvious reduction of sensitivity for using Pinc as a power input rather than P_{in}. The simulation is done with Z_{in} = 50 Ω, and s-parameters are calculated for each input power to extract the reflection coefficient Γ and r.f. power delivered to the GFET. It is possible to improve the responsivity with a matching network on the input to reduce the power loss by reflection, however, it could also result a narrower bandwidth of the detector response.

Figure 5.10 (b) shows V_{out} vs. Pinc plot with ~40 V/W responsivity and 550 pW/√Hz of noise equivalent power (NEP) for 8.5 GHz of r.f input frequency at $V_g = V_d$ = 0V. One can calculate NEP by the noise level divided by output voltage responsivity. It can be estimated as the input power level corresponds to intersection of V_{out} and V_{noise} from plots in Figure 5.9 (indicated by arrow). The abstract model of GFET device was fitted to R_j-V_g curve of figure 5.7 (a) [1], assuming W = 12 μm. The r.f. circuit simulation was performed with parasitic components extracted from the measurement – C_{gs} = 3.3 pF/mm, C_{gd} = 3.6 pF/mm, gate resistance (R_g) of 3.2 Ω, and access resistance ($R_s + R_d$) of 40 Ω.

Noise voltage is also displayed in the same plots, which show flat level versus input power of ~4 nV/√Hz until the P_{in} or P_{inc} reaches -25 dBm. Since the detector has no DC current due to zero drain bias operation, 1/f noise was suppressed at low Pin while only the thermal noise (or Johnson noise) contributes to noise voltage as discussed previously. However, when input power increases, V_{out} can build up large enough to induce the DC drain current from the device, which will generate the 1/f noise. This is the reason for the increasing noise voltage at higher input power.

Channel resistance of 497 Ω (at V_g = 0V) is the major factor of the thermal noise, however each parasitic components such as gate resistance and series resistances are also included in the total noise calculation. Both flicker noise and thermal noise are added as a serial voltage noise source at the channel of the simulation, using following expressions.

Flicker noise:

$$< v^2 >= \frac{K_f \times {I_{dc}}^{A_f}}{f^{F_{fe}}}$$

,

where K_f=2x10^{-7} Hz $^{a-1}$ ·R_j^2, I_{dc} is measured DC current at the drain in amperes, A_f=1.1, f is simulation frequency, F_{fe}=1.1. For the zero-biased power detector, 1/f noise is negligible until the input power is large enough (~ -10 dBm) to build a DC output voltage which draws drain current. At the low power input operation range, thermal noise is the dominant noise source of the detector system.

Thermal noise:

$$< v^2 >= 4 \times k \times T \times R_j$$

, where *k* is the Boltzmann constant, T is temperature, R_j is channel resistance.

5.4.2. Optimum Size of the Device: Effective Channel Width

In order to have better sensitivity by applying proper gate bias, Vg is adjusted to -2.5 V to increase transconductance for following simulation results. Responsivity increased with bias changes as described in figure 5.7 (a). a_0, a_1, a_2 coefficients are also adjusted for each gate biases. Although the new bias condition will result higher channel

resistance, the benefit from operating at higher g_m outweighs the higher noise from increased channel resistance.

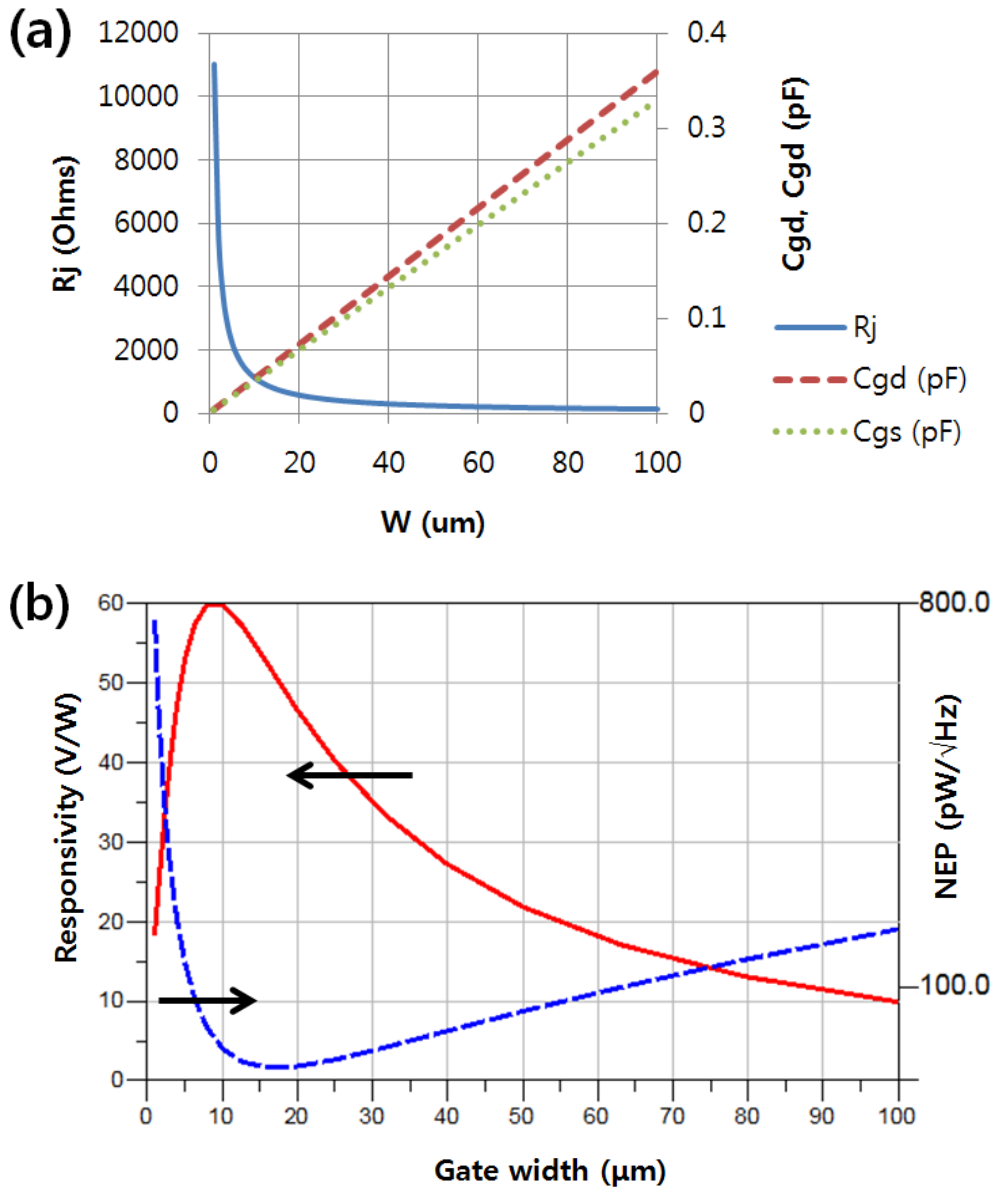


Figure 5.11. (a) Channel resistance (R_j) and parasitic capacitance (C_{gs}, C_{gd}) versus effective device width at Vg=-2.5V. (b) Responsivity and NEP vs. device channel width. Larger width will increase the Cpara, while lowering the channel resistance.

The size of the device is represented by the effective width of the device. By varying the width while maintaining other dimensions, there is a clear trade-off between the channel resistance and parasitic capacitance, which is indicated in figure 5.10 (a). Lower resistance in larger devices will suppress the thermal noise and make the Noise equivalent power (NEP) smaller, however, increasing capacitance will degrade the responsivity of the detector. In figure 5.11 (b), Simulation result shows the width of 15 ~ 17 μm will be optimal width for this device for detector. Size of the device should be optimized with consideration of input power range, frequency, bias condition and other extrinsic components.

5.4.3. Extrinsic Parameters: Z_s, C_{pad} and R_{load}

Source impedence (Z_s) is another extrinsic parameter that affects the performance of the detector. Figure 5.12 shows the change of responsivity and NEP according to the source impedance at a given frequency 8.5 GHz. The result shows optimum input impedance is 250 ~ 300 Ω for 8.5 GHz. About 300 ohm of impedance could be obtained from the setup of antenna. Increased (from 50 Ω) impedance would be beneficial for enhancing the sensitivity, however, it will degrade the frequency response and make the detector bandwidth narrower.

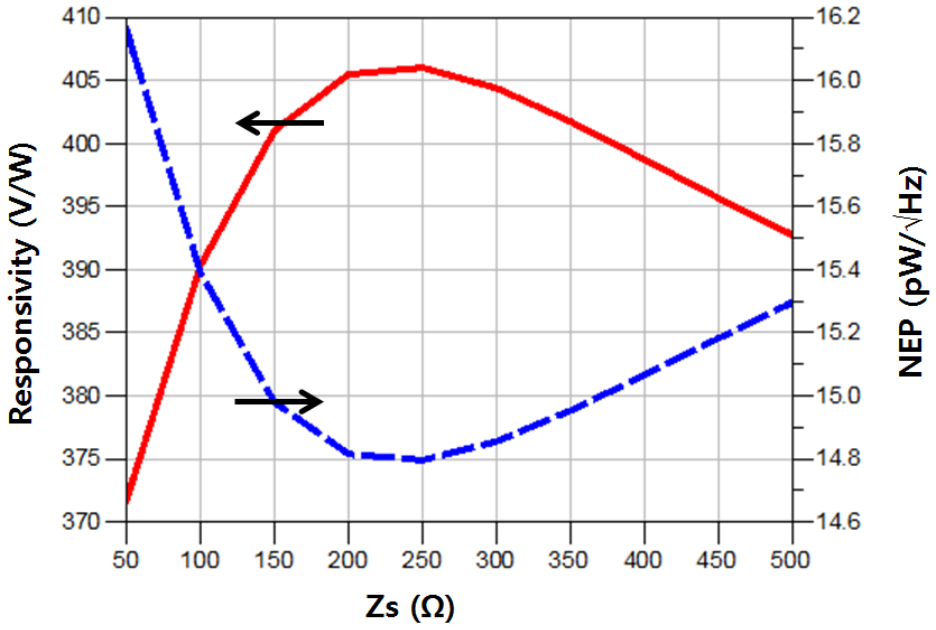


Figure 5.12. Responsivity and NEP versus input impendance (Z_s).

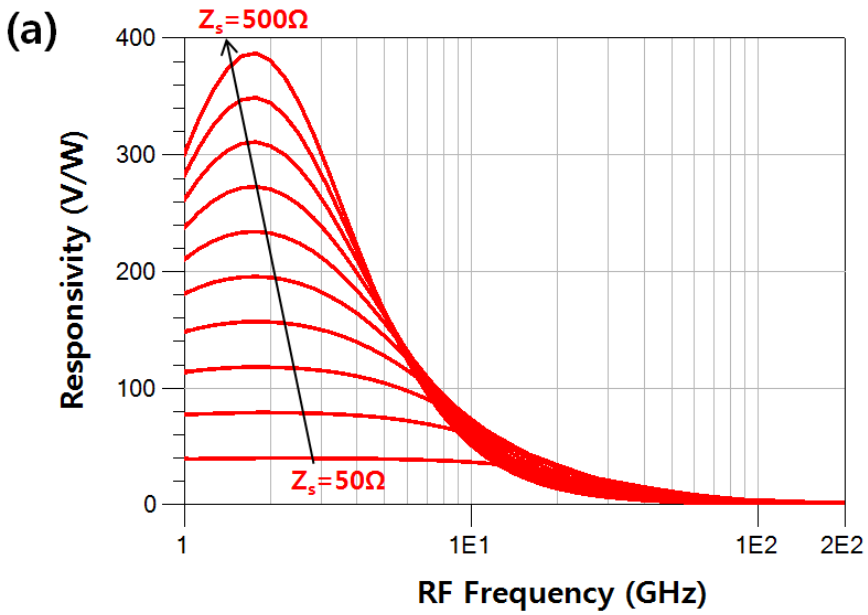


Figure 5.13 (a) Frequency response of responsivity of power detector when Z_s is varying from 50 to 500 Ω.

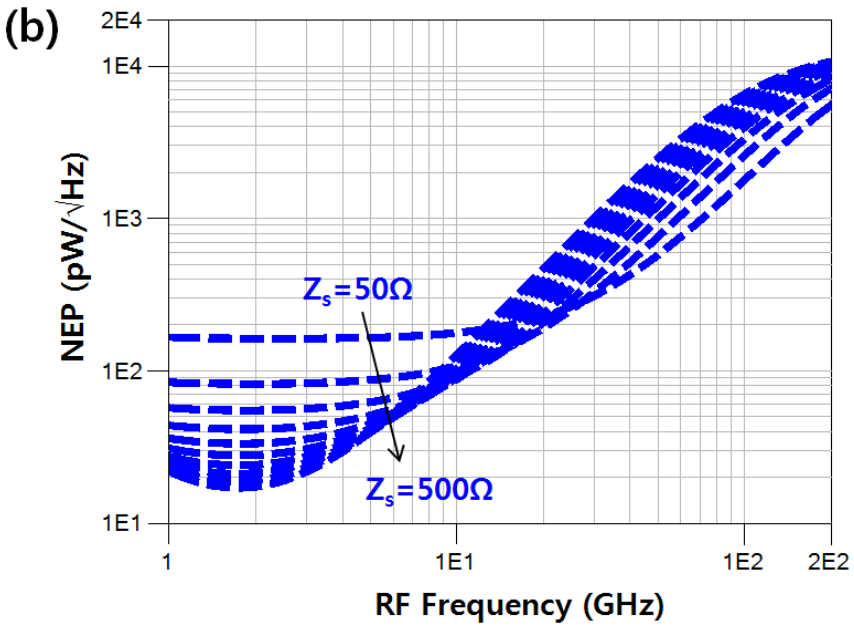


Figure 5.13 (continued) (b) NEP vs. r.f. frequency when Z_s is varying

In figure 5.13, the simulated frequency response is shown for Z_s = 50 ~ 500 Ω, over the input r.f. frequency range of 1 ~ 200 GHz. Figure 5.13 (b) and (c) are frequency response plots of responsivity and noise equivalent power (NEP), respectively. At lower frequency range at 1 ~ 4 GHz, responsivity is maximized at Z_s = 500 Ω. However, the responsivity drops rapidly as the input r.f. frequency increases. On the other side, lower input impedence such as 50 Ω shows lower responsivity than DC voltage than higher Z_s cases at lower frequencies, but has better frequency response with a very flat level of sensitivity, which represents the characteristics of an excellent wide bandwidth detector. Z_s = 50 Ω case eventually shows better or comparable responsivity and NEP at 30 GHz or higher frequency.

The output voltage is measured at the load resistance at the output drain side node. Increased load resistance can enhance the responsivity and decrease the NEP to a

limited extent. Figure 5.14 displays the impact of R_{load} on responsivity and NEP when input r.f. frequency is 8.5 GHz. Larger resistance is favorable to have a high sensitivity power detector. With higher R_{load}, the response to time-varying input powers will be slower, however, for a given output capacitance.

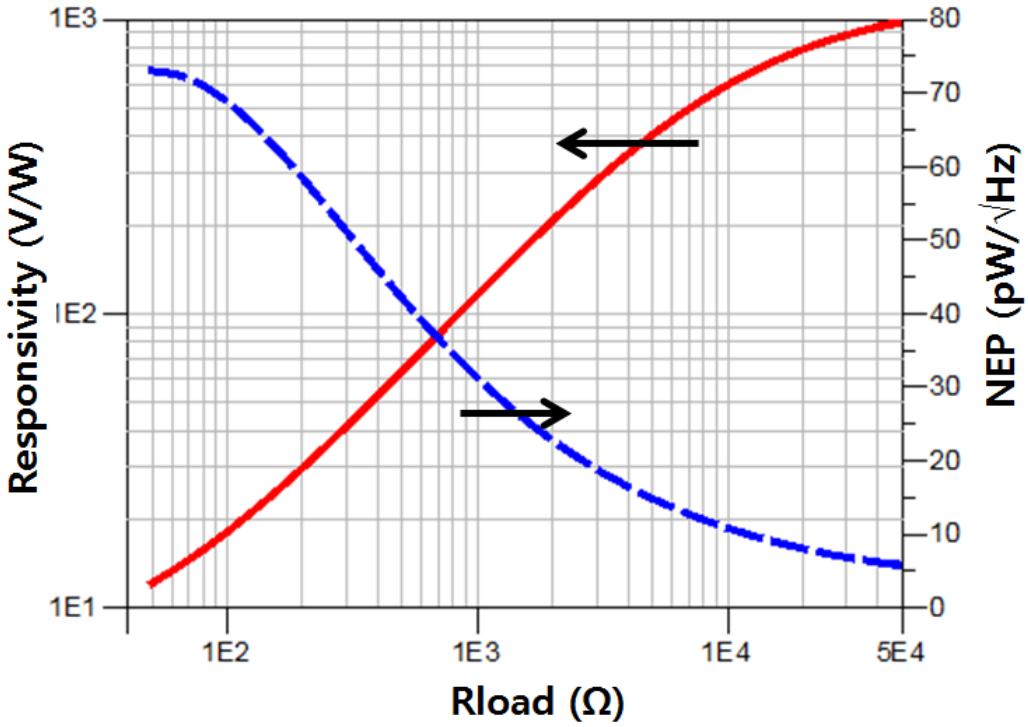


Figure 5.14. Responsivity and NEP for various R_{load} at 8.5 GHz.

5.5. Zero-Bias Linear Resistive Mixers

Other than power detectors, various graphene FET applications using graphene's unique ambipolar behaviors have been explored, such as frequency doublers and mixers [9, 10]. It is also reported the mixer performances regarding linearity can improve with an

alternate scheme of using GFET for mixer. A demonstration of zero-bias linear resistive GFET mixers shows GFETs with excellent mixer linearity [2].

In this section, simulated performance of GFET based linear resistive mixer will be discussed in order to support the experimental results, and to validate the versatility of GFET device models for circuit simulations. Both back-to-back connected GFET model and abstract analytic device model for GFET were used for fitting the the experimental device measurement data for mixers.

5.5.1. GFET resistive mixer operation

The dynamic range and linearity of mixers are important for r.f. communication systems [2]. R.f. up- or down-conversion linear mixers passive resistive FET mixers have been preferred due to low intermodulation results [11]. Figure 5.14 describes the schematic of GFET based linear resistive FET mixer. This shows a completely passive resistive FET mixer with gate-pumped configuration. No DC drain bias was applied, therefore the DC power consumption is eliminated.

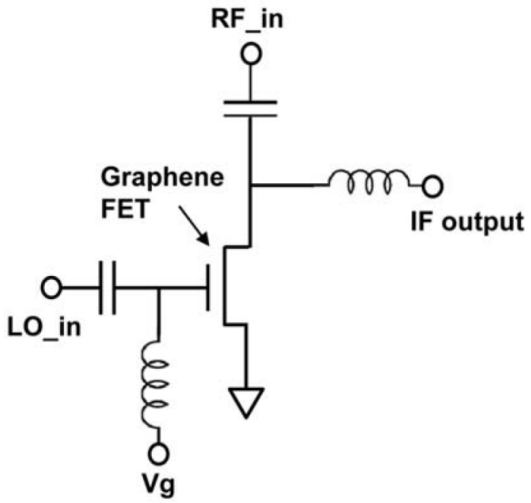


Figure 5.15. Schematic of resistive FET mixer, where the LO signal is applied to the gate (gate-pumped). The IF output signal is measured at the drain. [2]

The mixer operates with local oscillator (LO) signal applied to the gate while DC gate bias controls the channel property to desired resistance level. When r.f. signal is feeded to the drain, LO signal to the gate will control the channel resistance modulation and provides linear r.f. mixer performance. Intermediate frequency (IF) signal is measured at the output at drain. The input third-order intercept point (IIP3) displays the nonlinearity of the mixer, which can be read off from the input or output power axis of intercept point of extended straight lines of first and third-order output vs. input curves.

5.5.2. Linear region of GFET near zero bias

For zero-biased linear resistive FET mixer, linear drain current vs. bias near at near zero drain bias is a region of intersest. Figure 5.16 displays I_{ds}-V_{ds} curve of GFET, focusing on linear region near zero bias. Operation near zero V_{ds} provides linear response

of channel resistance and suppresses intermodulation, which results an excellent mixer linearity. [2, 11]

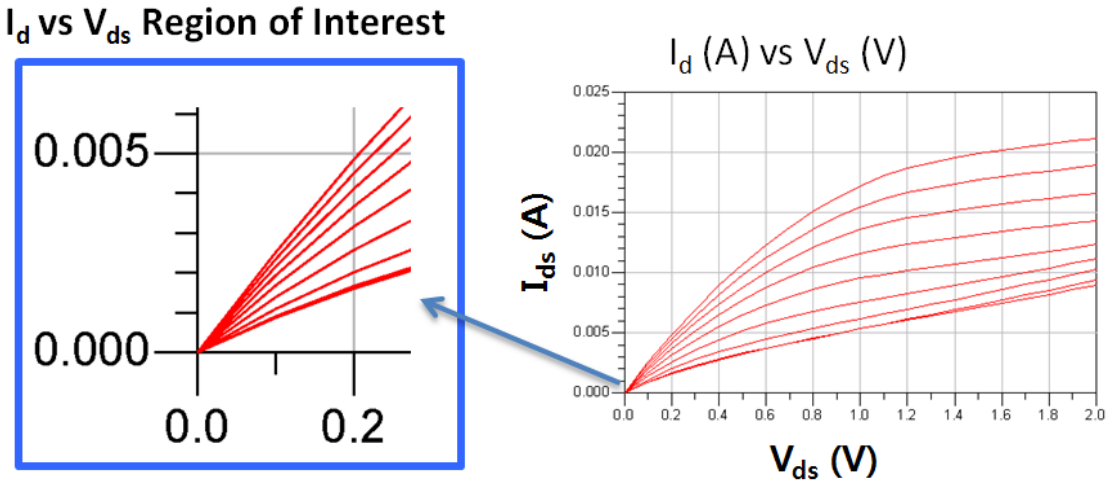


Figure 5.16. Simulated I_{ds}-V_{ds} curves of GFET with varying gate bias. (inset) zoom-in: region of interest near V_{ds} = 0 V.

5.5.3. Mixer Simulation and impact of device parameters

Figure 5.17 displays the schematic of GFET based resistive mixer in the ADS simulation with parasitic elements such as series resistances, which used the BTBC GFET model fitted to the measurement result (Figure 5. 18, R-V_g). The simulated and measured device is 2-finger graphene FET with width of 2x12 μm, gate length of 0.25 μm.

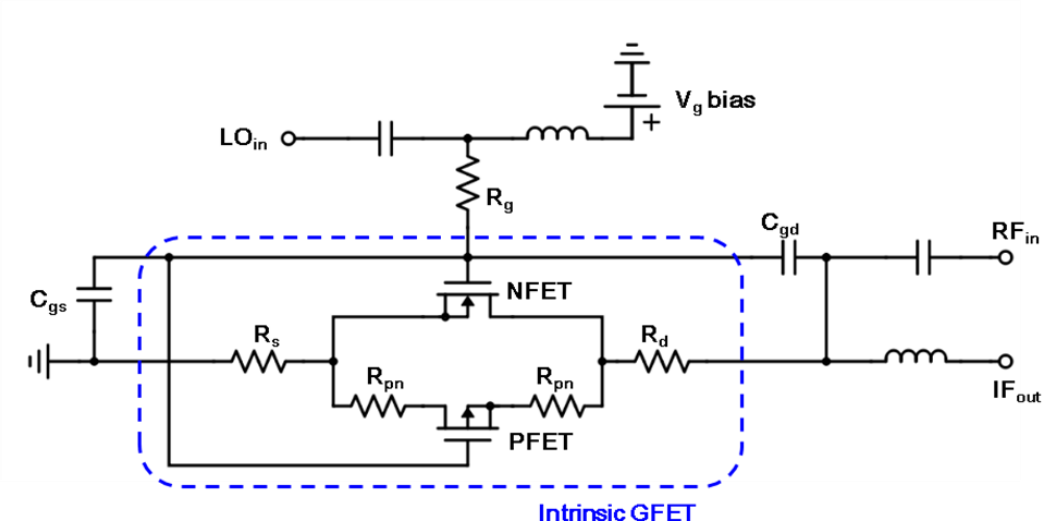


Figure 5.17. Schematic of resistive GFET mixer with bact-to-back-connected FET device model

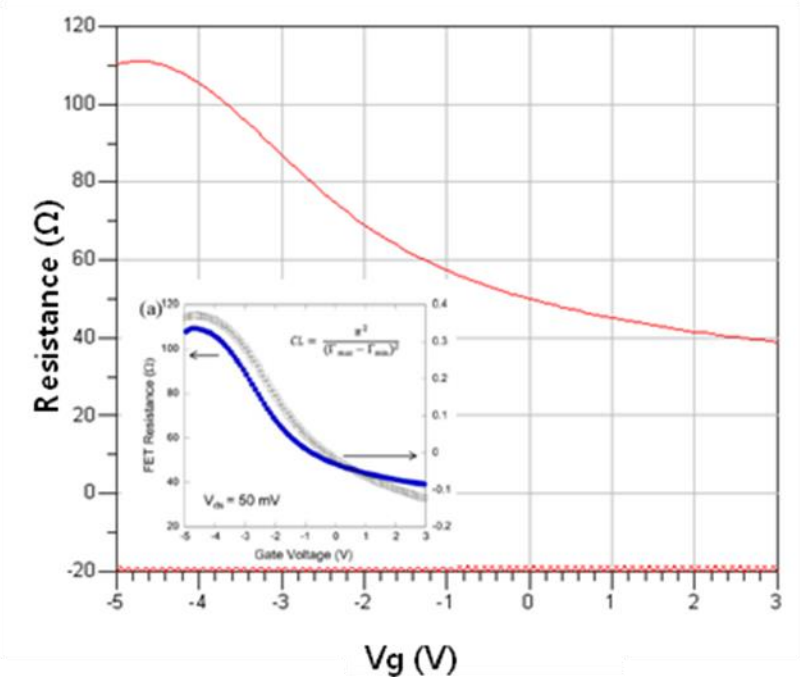


Figure 5.18. Simulated GFET resistance as a function of gate voltage. (inset) Measured GFET resistance vs. Vg and reflection coefficient [2].

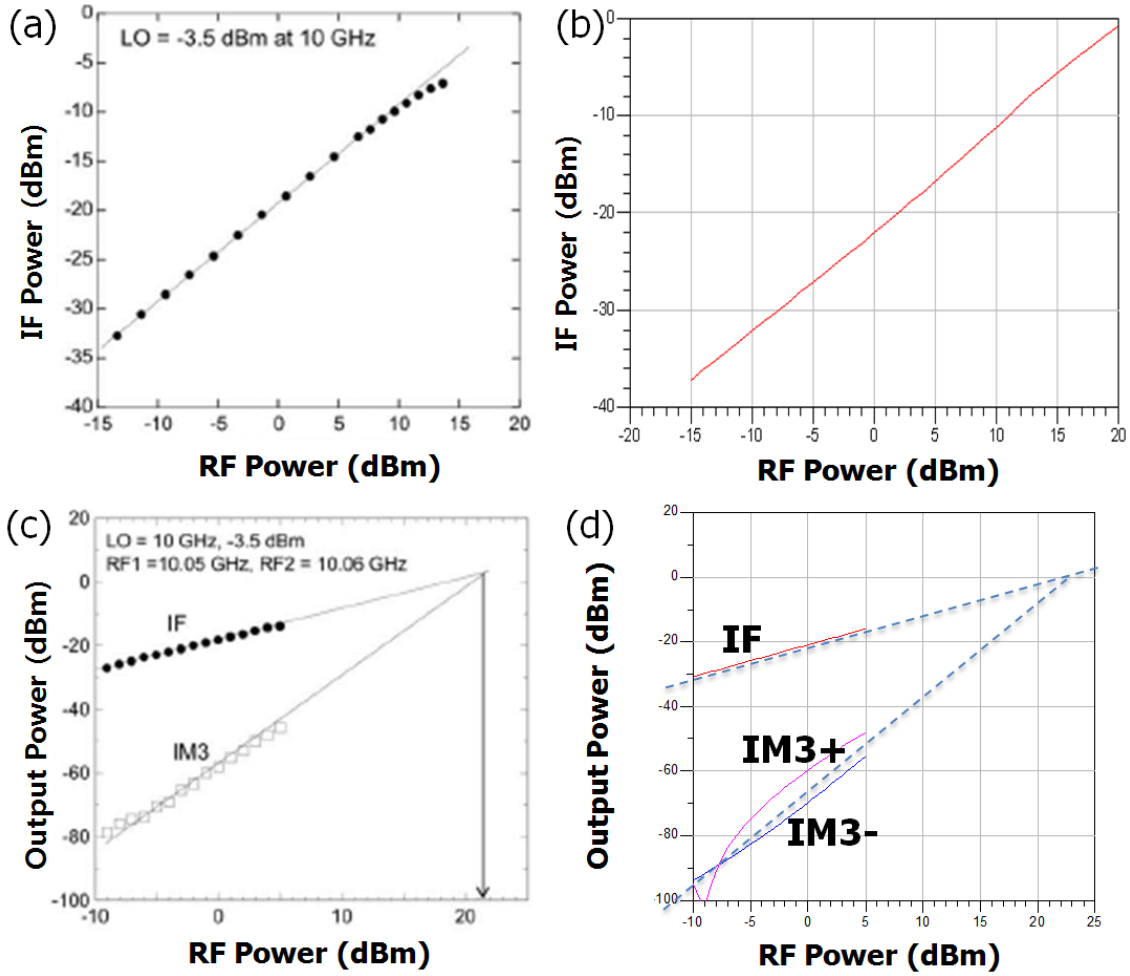


Figure 5.19. (a) Measured IF power versus r.f. input power of GFET at 10 GHz [ ] (b) Simulated IF power vs. r.f. input power at 10 GHz (c) Measured two-tone test result of a GFET at 10 GHz (d) Simulated two-tone test of GFET at 10 GHz. The gate width was 2*12μm, gate length was 0.25 μm.

Figure 5.19 (a) and (b) shows IF power versus r.f. power of a graphene FET with gate length of 0.25 μm, measured and simulated with LO power -3.5 dBm and 10 GHz of r.f. frequency. In the measurement, 1 dB compression occurs at r.f. power of 12 dBm. Simulation result with BTBC FET model shows a good agreement with the measurement result. IF and IM3 of two-tone measurement and simulation is displayed in Figure 5.19 (c) and (d), respectively. IIP3 is estimated about 22 dBm for both measurement and

simulation by extrapolation of IF and IM3 based on 10 and 30 dB/dec slopes. Ambipolar graphene mixer showed IIP3 of 13.8 dBm at V_{ds} = 1V at 10 MHz [10].

Abstract model replaced the BTBC FET model for investigation of impact of nonlinearity coefficients. Figure 5.20 (a) shows the schematic of the linear mixer as used in the ADS simulation. R.f. power is set to 1 dBm, frequency is 10 GHz and LO power is -3.5 dBm. Baseline device parameters are a_0 = 0.033445, a_1 = 0.0550792, a_2 = -0.01903, b = 0. a_1 and a_2 variation sweep shows that the rectification hinges on a1 coefficient, however it is not strongly dependent on a_2 coefficient (Figure 5. 20 (b) and (c)).

$$Id = (V_{ds} - b V_{ds}^{\ 3})(a_0 + a_1 V_{gs} + 1/2 a_2 V_{gs}^{\ 2})$$

An additional third order term is added with coefficient b, in order to show the impact third harmonic component on the linearity of mixer. In Figure 5. 20 (d), as non-zero coefficient b is used and third order term of V_d contributes to the modulation, IM3 increases faster which results a lower linearity and IIP3. b coefficient influences compression point as well.

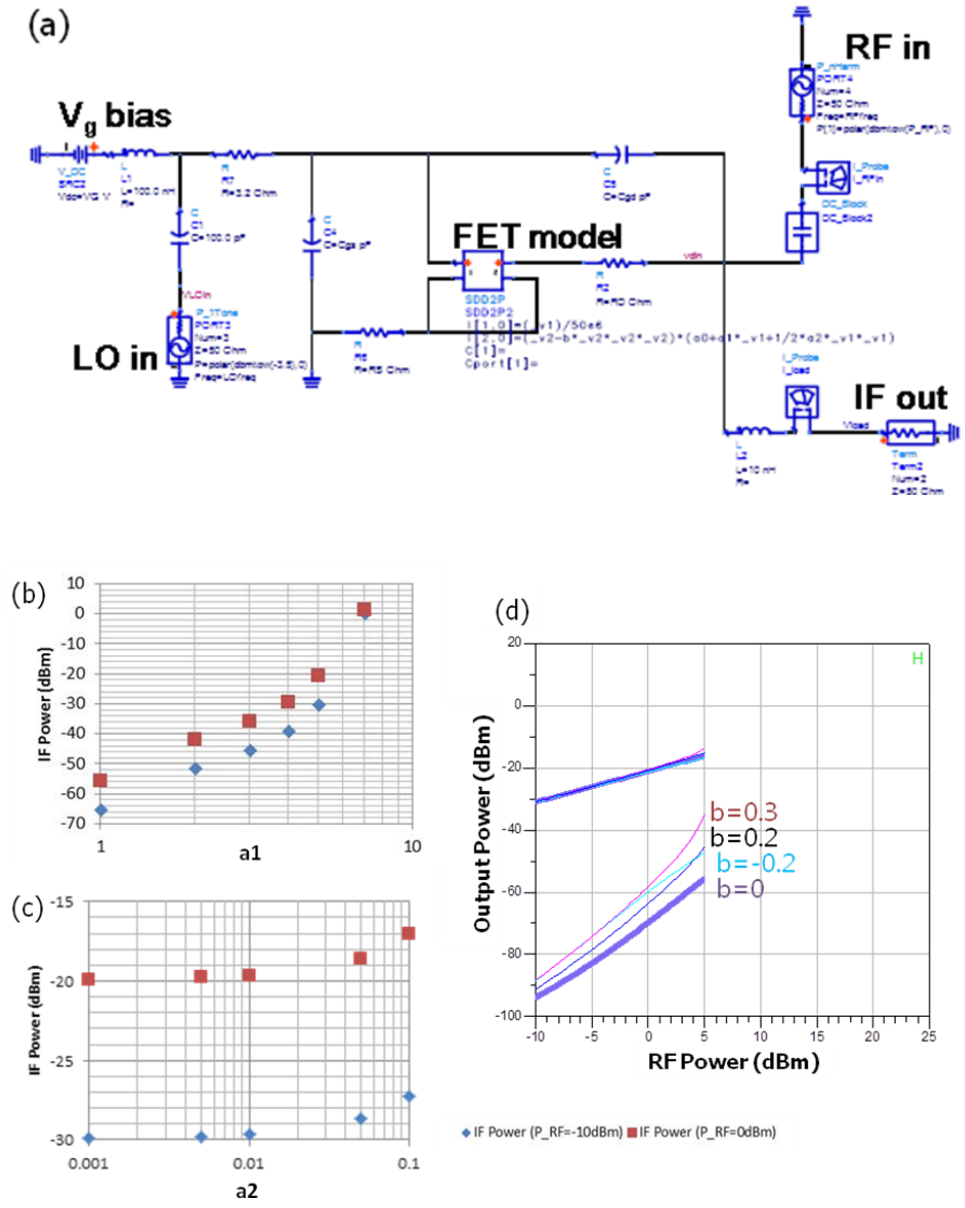


Figure 5.20. (a) A schematic of the linear mixer as used in the ADS simulation. (b) IF power respect to a_1 parameter variation (c) IF power versus a_2 parameter (d) Output power vs. r.f. power when b parameter varies.

5.6. Conclusion

Graphene FET models, power detector and resistive mixer applications are investigated with simulations in detail. Back-to-back-connected FET model describes ambipolar current flows in GFET and easy to use in circuit simulations with proper parameter setup. Abstract analytic model provides in depth information of device parameter for circuit performance, such as non-linearity coefficients to estimate responsivity of detectors and linearity of mixers. Circuit simulations using both device models showed a good agreement with experimental results. Various extrinsic and parasitic components were included to simulate more realistic r.f. power detector and mixer systems, then the impacts of each components were discussed.

Optimized width for low channel resistance and low parasitic capacitance is required, and input impedance is important to choose high responsivity at lower frequency or a wide frequency response of detector. GFET based resistive mixer showed excellent linearity at low LO power without DC bias applied, offers the potential high quality linear mixers.

5.7. References

[1] Moon, J.S., Seo, H.C., Antcliffe, M., Lin, S., McGuire, C., Le, D., Nyakiti, L.O., Gaskill, D.K., Campbell, P.M., Lee, K.M. and Asbeck, P., "Graphene FET-Based Zero-Bias RF to Millimeter-Wave Detection," in IEEE Electron Device Letters, vol. 33, no. 10, pp. 1357-1359, Oct. 2012.

[2] Moon, J.S., Seo, H.C., Antcliffe, M., Le, D., McGuire, C., Schmitz, A., Nyakiti, L.O., Gaskill, D.K., Campbell, P.M., Lee, K.M. and Asbeck, P., "Graphene FETs for Zero-Bias Linear Resistive FET Mixers," in IEEE Electron Device Letters, vol. 34, no. 3, pp. 465-467, March 2013.

[3] Moon, J.S., Curtis, D., Hu, M., Wong, D., McGuire, C., Campbell, P.M., Jernigan, G., Tedesco, J., VanMil, B., Myers-Ward, R. and Eddy, C., "Epitaxial graphene RF field-effect transistors," 2009 Device Research Conference, University Park, PA, 2009, pp. 195-196.

[4] Wu, Y.Q., Lin, Y.M., Jenkins, K.A., Ott, J.A., Dimitrakopoulos, C., Farmer, D.B., Xia, F., Grill, A., Antoniadis, D.A. and Avouris, P., "RF performance of short channel graphene field-effect transistor," Electron Devices Meeting (IEDM), 2010 IEEE International, San Francisco, CA, 2010, pp. 9.6.1-9.6.3.

[5] Liu, Q.B., Yu, C., Li, J., He, Z.Z., Song, X.B., Lu, W.L. and Feng, Z.H., "Epitaxial graphene FETs on sapphire substrate," Electron Devices and Solid-State Circuits (EDSSC), 2014 IEEE International Conference on, Chengdu, 2014, pp. 1-2.

[6] Han, S.J., Valdes-Garcia, A., Bol, A.A., Franklin, A.D., Farmer, D., Kratschmer, E., Jenkins, K.A. and Haensch, W., "Graphene technology with inverted-T gate and RF passives on 200 mm platform," Electron Devices Meeting (IEDM), 2011 IEEE International, Washington, DC, 2011, pp. 2.2.1-2.2.4.

[7] Lee, J., Parrish, K.N., Chowdhury, S.F., Ha, T.J., Hao, Y., Tao, L., Dodabalapur, A., Ruoff, R.S. and Akinwande, D., "State-of-the-art graphene transistors on hexagonal boron nitride, high-k, and polymeric films for GHz flexible analog nanoelectronics," Electron Devices Meeting (IEDM), 2012 IEEE International, San Francisco, CA, 2012, pp. 14.6.1-14.6.4.

[8] M. N. Yogeesh, S. Park and D. Akinwande, "Graphene based GHz flexible nanoelectronics and radio receiver systems (Invited)," 2015 IEEE International Symposium on Circuits and Systems (ISCAS), Lisbon, 2015, pp. 2916-2919.

[9] Moon, J.S., Curtis, D., Zehnder, D., Kim, S., Gaskill, D.K., Jernigan, G.G., Myers-Ward, R.L., Eddy Jr, C.R., Campbell, P.M., Lee, K.M. and Asbeck, P., "Low-Phase-Noise Graphene FETs in Ambipolar RF Applications," in IEEE Electron Device Letters, vol. 32, no. 3, pp. 270-272, March 2011.

[10] H. Wang, A. Hsu, Ki Kang Kim, Jing Kong and T. Palacios, "Gigahertz ambipolar frequency multiplier based on CVD graphene," Electron Devices Meeting (IEDM), 2010 IEEE International, San Francisco, CA, 2010, pp. 23.6.1-23.6.4.

[11] S. A. Maas, "A GaAs MESFET Mixer with Very Low Intermodulation," in IEEE Transactions on Microwave Theory and Techniques, vol. 35, no. 4, pp. 425-429, Apr 1987.

[12] C. Yuhua, and C. Hu. “MOSFET modeling & BSIM3 user’s guide,” Springer Science & Business Media, 1999.

[13] R. Appleby and R. N. Anderton, "Millimeter-Wave and Submillimeter-Wave Imaging for Security and Surveillance," in Proceedings of the IEEE, vol. 95, no. 8, pp. 1683-1690, Aug. 2007.

[14] Michael C. Kemp, “Millimetre wave and terahertz technology for the detection of concealed threats: a review,” Proc. SPIE 6402, Optics and Photonics for Counterterrorism and Crime Fighting II, 64020D (September 28, 2006); doi:10.1117/12.692612.

[15] P. Fay, J. N. Schulman, S. Thomas, D. H. Chow, Y. K. Boegeman and K. S. Holabird, "High-performance antimonide-based heterostructure backward diodes for millimeter-wave detection," in IEEE Electron Device Letters, vol. 23, no. 10, pp. 585-587, Oct. 2002.

[16] Tiebout, M., Wohlmuth, H.D., Knapp, H., Salerno, R., Druml, M., Rest, M., Kaeferboeck, J., Wuertele, J., Ahmed, S.S., Schiessl, A. and Juenemann, R., "Low Power Wideband Receiver and Transmitter Chipset for mm-Wave Imaging in SiGe Bipolar Technology," in IEEE Journal of Solid-State Circuits, vol. 47, no. 5, pp. 1175-1184, May 2012.

[17] S. I. Ivanov, A. P. Lavrov and Y. A. Matveev, "A square-law microwave transistor detector for wideband radiometers," Control and Communications (SIBCON), 2015 International Siberian Conference on, Omsk, 2015, pp. 1-4.

[18] Y. Zhou and M. Y. W. Chia, "A Low-Power Ultra-Wideband CMOS True RMS Power Detector," in IEEE Transactions on Microwave Theory and Techniques, vol. 56, no. 5, pp. 1052-1058, May 2008.

Chapter 6

Conclusion

6.1. Thesis Summary

This dissertation presents various physical aspects of graphene FETs of importance in r.f. applications. Basic building blocks of graphene electronics such as p-n junction and graphene-metal junction are described, as well as the impact of film quality in terms of uniformity. Joule self heating and heat dissipation of graphene device is also studied. Finally, two examples of graphene based r.f. circuit applications are presented with device models, for investigating the relation between graphene's device parameters and the circuit performance.

In the first part, a brief history and background was reviewed, followed by a summary of structure and electrical properties of graphene and film manufacturing

methods. Electrical characteristics of graphene have been emphasized, such as high electron and hole mobilities due to its unique band structure, large maximum current, and ambipolar nature of graphene FETs.

Chapter 2 starts with the discussion of the device physics of graphene p-n junctions with a two dimensional device simulation with adjusted parameters for graphene devices. The estimation of spatial resistivity in vicinity of graphene p-n junction is based on carrier density and local variation of carrier mobilities. Id-Vg curves of GFETs nominally should have a symmetric ambipolar curve due to same density and mobility of carriers on electron and hole branch with same |Vg-VDirac|. However, the observed hole branch current is lower than electron branch's current when ungated graphene film and contacts are n-type. In this thesis, it is shown that because the channel of electron branch has n-n-n type area along the channel while carriers of hole branch should flow through n-p-n regions, where two p-n junction exists. The simulation results show the p-n junction adds additional resistance generated by carrier depletion at the p-n transition region with comparable magnitude with experimental results. The amplitude and width of p-n junction resistivity peak is controlled by carrier density, gate bias and fringe electric field.

Metal-graphene interface and junctons are also of important for device performance, and as graphene devices are developed and improved, the impact of contact resistance on the performance becomes more significant factor. Imbalance between Fermi energy of graphene and the work function of metal at the interface causes charge transfer between layers, which can dope or deplete the graphene film in contact. This effect is emphasized in graphene due to its single atom-thick physical dimension that forces the

whole material affected by the interface, and also its small density of states near conduction or valence band edges. It is shown here that when the doping (or depletion) have large enough difference from the equilibrium charge density of the un-doped graphene in the channel, lateral charge transfer occurs and form a finite charge transfer region (CTR). It can make the contact resistance lower (additional doping) or higher (form a p-n junction), and generate errors on conventional contact resistance measurement such as TLM method. CTR becomes larger when channel equilibrium charge density is low, work function difference is larger, the metal is thicker, where fringe field comes from the side wall of metal.

Chaper 3 describes modeling of inhomogeneous graphene films, based on randomly distributed charges on 2-D graphene film which represents the so-called electron and hole puddles. Graphene film fabrication technology has been improved significantly, however it is still a challenging task to control the charge density uniformly over large area, especially near VDirac where puddle formation has significance. Inhomogeneity not only impacts the result of Hall measurement and causes the underestimation of Hall mobility but also gives errors in the VDirac estimation. Size (area) and strength (amplitude of charge density variation) of puddles contribute to inhomogeneous Hall measurement data and spread Dirac point among devices on inhomogeneous film. Statistical trends on these deviations were studied with repeated simulations with different random dopant matrices.

Thermal properties related to heat dissipation of epitaxial graphene devices are investigated in chapter 4. 3-D heat thermal simulation displayed the importance of lower interface thermal interface, small device dimensions, and the role of metal contacts to

enhance lateral heat spreading for minimizing the impact of Joule self-heating. Even though the graphene has excellent lateral thermal conductivity, majority of heat should dissipate vertically through the substrate, where SiC substrate might have benefit over oxide substrates. Since graphene has a very small heat capacity, it can self-heat even with a short period of pulse such as 200 ns. Both simulation and experiments showed consistant results on this and the extracted thermal resistance of the system is $8 \cdot 10^{-5}$ K cm^2W^{-1}.

The first part of chapter 5 shows SPICE model of graphene FET which consists with back-to-back connected NMOS and PMOS to describe the ambipolar Id-Vg curves. The model fits well with experimental data and can be used for graphene based circuit simulations easily. Analytic expression of abstract model was also developed for further investigation of device parameters such as non-linearity, and its overall impact on the circuit performance.

The rest of chapter 5 discusses the GFET based r.f. power detector and resistive mixer simulation results compared with experiments. Both results show good agreement, which validates the compact model for GFET. For the GFET r.f. power detector, non-linearity of GFET enhances the responsivity while the zero-biased operation suppresses the flicker noise and allows a good sensitivity, which is represented with noise equivalent power (NEP). Optimization of the detector was performed with various device parameters including parasitic elements such as parasitic capacitances, gate resistance, and series resistance at source and drain. High input impedance improves the sensitivity at lower frequency, however, lower impedance input showed better broadband capability. On the other hand, linearity of GFET drain current near Vd=0V helped to make a good

resistive linear mixer performance at low LO power without DC bias, which was comparable to other state-of-the-art passive resistive mixers.

6.2. Future Work

This dissertation has covered various aspects towards building the graphene based r.f. system, from material properties, junction with other materials, thermal behavior and a few examples of circuit applications. The following presents several research objectives that are extensions of the topics discussed in this dissertation.

- More case studies could be doneof errors and oversights in the use of measurement and analysis techniques for conventional semicondcutors when applied to on nano devices such as graphene FETs. Inhomogeneous graphene modeling study was motivated by unexpectedly lower Hall mobility measurement, while CTR investigation started with unphysically low contact resistance data from TLM method. Ambipolar conduction was also prominent in graphene. Due to its extremely scaled dimension and small DOS, it is possible to have additional sources of errors in applying conventional semiconductor measurement methods to graphene devices.

- Expansion of thermal simulation for other devices and material systems: The study in this dissertation showed the importance of interfacial thermal resistance and the limit of graphene's extremely good lateral thermal conductivity. More consideration for optimum device thermal design will be needed. One of several

findings is that it is important to place a low thermal resistance heat spreading layer as near as possible to the hot spot of the device, which can be applied to design of devices with any materials.

- Capacitance modeling: One possible topic which could have been covered in the dissertation is study of capacitance between graphene andadjacent materials. An analytic modeling of capacitance using conformal mapping to describe fringe field and parasitic elements could be done. More over, it would be interesting to apply the method to graphene devices on flexible substrate which can be bent or rolled.

- Exploration of more GFET circuit applications with compact model: Since the simple SPICE compact model showed the capability of straight forward use of device models in the circuit simulations, it would be good to expand the scope of applications and apply similar method to understand and optimize the circuit performances.