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Influence of Gate Separation on IGZO Thin Film Transistor Behavior

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Influence of Gate Separation on IGZO Thin Film Transistor Behavior

A thesis

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of the requirements for the degree Master of Science

in Materials Science and Engineering

by

Zhiyu Zhao

2020

ABSTRACT OF THE THESIS

Influence of Gate Separation on

IGZO Thin Film Transistor Behavior

by

Zhiyu Zhao

Master of Science in Materials Science and Engineering

University of California, Los Angeles, 2020

Professor Yang Yang, Chair

Metal oxide are attracting great interests in the electronics field as a promising active layer candidate for various uses including wearable sensors, flexible display, and LED displays. The current status of manufacturing relies on cleanroom manufacturing, which can be time consuming and costly. Consequently, a repeatable and reliable process to fabricate stable, large scale TFT is needed for manufacturing and consumer's need. Metal oxides have proven their values to be the next generation display for their hi-performance electrical characteristic, abundance, and straight forward fabrication method. In particular, system consists of Indium-Gallium-Zinc-Oxide (IGZO) has demonstrated stability as well as high electrical performance. Science then, TFTs with IGZO systems had prompt extensive research in the solution process field. Since the conventional method are limited by sample size and processing time, solution-processing had opened gateway to more

flexible, even large-scale fabrication with way less steps and processing time. The major drawback of solution processing the its instability, uncertainty, and weaker device performance comparing to those fabricated in the cleanroom environment. In this work, several methods were investigated including direct light patterning and UV and ozone treatment of sample surface to improve device performance. A gallium rich IGZO solution TFT with 2:2:1 molar ratio was made with direct light patterning method and compared to conventionally made IGZO TFT. It is shown that direct light pattering could drastically enhance device stability and performances. Other factors such as cluster size, interface treatment, and etchant composition could greatly affect the outcome as well.

The Thesis of Zhiyu Zhao is approved.

Jaime Marian

Ya-Hong Xie

Yang Yang, Committee Chair

University of California, Los Angeles

2020

TABLE OF CONTENTS

LIST OF FIGURES, EQUATIONS AND TABLES

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Chapter 1

INTRODUCTION

1.1. Motivation

Electronic visual display had attracted great attention for various applications ranging from wearable displays, sensors, large scale display panels and more. From billboards to cellphones, televisions, computers, activity tracers and more, display technology has seeped through our daily lives. Demand for large scale, high resolution, fast response displays with low power consumption has been rising. The next generation display technologies such as organic light-emitting diode (OLED), Quantum dot, and Ferro liquid display (FLD) had drawn massive industrial interests. OLED presents one of the most promising result in large scale display. A branch of OLED, active-matrix organic light-emitting diode (AMOLED), has been used in mobile phones, digital cameras, and is taking the next steps to more cost efficient, higher resolution, and lower power consumption. All those technologies need transistors to serve as switches in the panel to control the current flow to each pixel. Thin film transistors backplanes are imbedded in display panel matrixes, directly affects the image quality, contrast, power consumption and lifetime.

Thin film transistors have dominated the display technology for the past 20 years. TFT is best known for liquid crystal display (LCD), and its potential application in AMOLED. Conventional, silicon was used as the active layers in the backplanes. Albeit the relatively lower carrier mobility and instability, silicon-based semiconductors are cheap to fabricate across large areas and were adequate to function as switches. A new type of TFT was in need to keep up with the fast development of the display industry, and provide high uniformity, better stability, faster response, higher transparency, and low processing temperature. Metal oxides (MOs) are attracting

great interest in electronic for its distinct properties and its abundance in the Earth's crust. MOs are easier to fabricate than silicon, has lower annealing temperature, and has faster response time, making them positive candidates to replace silicon. Indium-Gallium-Zinc Oxide (IGZO) TFT has shown promising results as it had achieved mobility of 10-40 $cm^2/(Vs)$. It could also be processed at comparably low temperature which allows future development of flexible display.

The traditional way to make IGZO TFT is by deposition in a cleanroom environment, which can drive the cost and time drastically. Recently, a brand-new method, solution gel processing has been investigated for its potential to revolutionize the fabrication process. This method allows processing under ambient condition with low annealing temperature, makes it feasible for fabrication on flexible substrate. The drawback of this method is that device fabricated in this way has relatively inconsistent results, lower mobility, and poor stability. Once those weaknesses are improved, IGZO TFT would have great confidence to be a part of the future generation display backplane.

Chapter 2

BACKGROUND AND LITERATURE REVIEW

2.1. History of Thin Film Transistors

The concept of thin film transistors could be dated back to 1925, when J.E Lilienfeld and patented concepts of a material which controls current flow through a transversal electrical field. [1] [2] [3] Lilienfeld had proposed the hypothetical materials and structure shown in Figure 2-1 an active layer of Cu_2S, followed by a layer of insulating Al_2O_3, and a metal gate of aluminum. Since the technology back then were not advanced enough to fabricate the device, Lilienfeld's idea remained as a concept for a long time. In 1935, O. Heil proposed a better constructed model for field emission transistors based on Lilienfeld's model. [3] His proposal was a device which could control the resistance in a semiconducting material with current flow. Unfortunately, deposition technology and vacuum system were still in development, their devices never got proven in the physical world. Their concepts were indeed valuable and inspired generation later for modern TFTs.

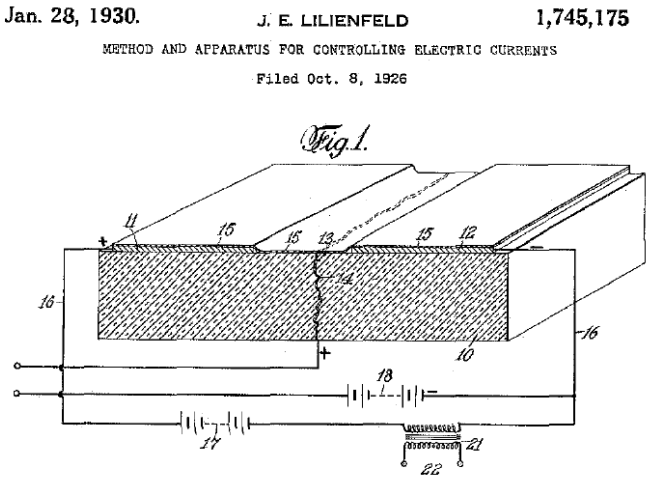


Figure 2-10 Lilienfeld's hypothetical model for thin film transistor. [2] [3]

As vacuum technology and deposition technology advanced, Weimer at RCA Laboratories were able to make the first thin film transistor in 1962. [4] [5] He used vacuum deposition technique to deposit gold source and drain, followed by polycrystalline cadmium sulfide, silicon monoxide insulator on top of an insulating substrate shown in Figure 2-1. This is a classic top gate TFT structure. Weimer and his colleagues continued to work on improving this structure and tested many other materials such as cadmium selenide (CdSe) and tellurium. Those results were all successful and achieved mobility up to 200 $cm^2/(Vs)$. [6] Weimer also published the first analysis of TFT characteristics, including current voltage (I-V) behavior and turn on voltage. Soon after, the first metal oxide, tin oxide, TFT was fabricated using photolithography. His inventions contribute greatly to the first-generation LCD televisions in later years.

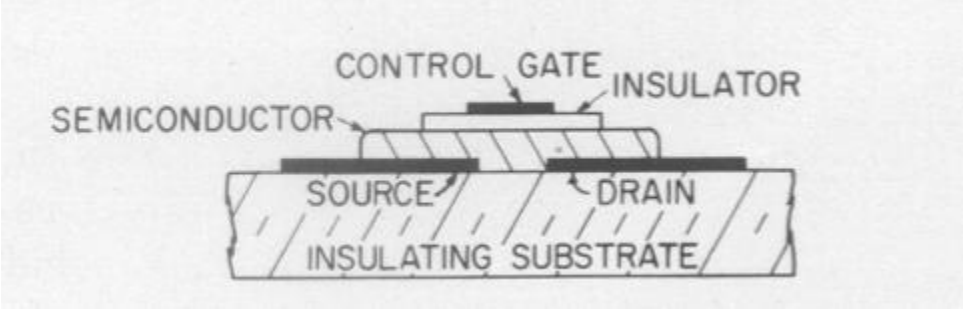


Figure 2-2 Weimer's top gate TFT structure. [5]

In 1973, the first CdSe TFT LCD was created. It had achieved high mobility of 40 $cm^2/(Vs)$. [6] However, it did not become popular due to its small viewing angles, long response time, and relatively small scale. [7] Mass production of LCD was not achieved until hydrogenated amorphous silicon (a-Si:H) was put in use as TFT back panels. In 1979, the first functional a-Si:H was reported by P.G. LeComber. [8] It combined a silicon nitride gate dielectric layer with a-Si:H and aluminum source drain and gate electrodes using glow-discharge deposition technology. The devices maintained good stability under atmospheric conditions. This process used plasma-enhanced chemical vapor deposition (PECVD), was relatively simple and exposed new frontiers

in LCD back panels. Devices made with a-Si:H does not exhibit the best properties. The mobility is about 1 $cm^2/(Vs)$, off current at 10^{-12}, and threshold voltage at about 3V. These characteristics were not exceptional but were enough for pixel switching in a display. Since then, active matrix displays used a-Si:H exclusively for a long period of time. [10] [11]

2.2.1 Metal Oxide TFTs

Since Russel Ohl patented the first silicon detector and p-n junction in 1939, silicon had dominated the semiconductor industry till now. [9] Scientists had engineered this material with doping, adjusting crystallography to achieve different functionalities. The emergency of a-Si:H solve the problems of crystalline silicon: low carrier mobility, high defect density, and low uniformity. It is the most vastly used black plane material albeit its low carrier mobility (~0.5-1.0 $cm^2/(Vs)$). The mobility is indeed too low for high-speed, high current application, such as OLED display. Furthermore, a-Si:H is a photoconductor, which means the TFT would have a large leakage current under exposure to light. While the current market calls for flexible, wearable, transparent, low power consumption, and fast speed display have been rising, a-Si:H is not able to keep up with the demand. To overcome the difficulties posted by a-Si:H, researchers turned to metal oxides (MOs) for solutions. [13]

Metal oxides excellent properties including high optical transparency, high carrier mobility, and good stress tolerance. The first metal oxide TFT was made by N.C. Klasens and W.P.C Koelmans in 1964. [10] [11] They used glass as substrate, deposited SnO_2 on top using evaporation, deposited aluminum for source-drain and grate electrodes, and used anodized Al_2O_3 as gate dielectric. Four years later, G.F. Boesen and J.E Jacobs created a lithium-doped zinc oxide (ZnO) single crystal TFT with evaporated silicon oxide dielectric layer and aluminum as

electrodes. [12] It has small drain current modulation and no drain current saturation, thus did not meet the criteria for functional device. In 1996, M. W. J. Prins detailed a tin oxide channel layer thin film, later that year, indium oxide TFT. [13]

The first large scale industrial feasible amorphous oxide semiconductors were synthesized in 1954. [10] Despite the long history of the discovery of oxide TFTs, it was not until 2003 when H. Hosono brought attention to them by presenting his work on IGZO systems. Transparent ZnO devices with mobility up to 2.5 $cm^2/(Vs)$ was achieved. The annealing temperature for this process was relatively high, around 450-600 °C. Devices with similar characteristics could be achieved at room temperature with radio frequency magnetron sputtering. Many labs and industries saw the potential of metal oxide TFTs and reported more materials suitable for display technology such as indium oxide, (In_2O_3), and different combination of IGZO system. Decent device characters including mobility of 80 $cm^2/(Vs)$, turn on voltage at -0.5Vand on/off ratio of 10^6 was soon achieved later in the year. [14] [15] Since then, metal oxide had become commercialized active matrix displays.

	a-Si:H	Poly-Si	Amorphous Metal Oxides
Stability	Good	Fair	Poor
Annealing Temperature	Relatively High	Relatively High	Relatively Low
Cost of Manufacturing	Low	High	Low
Optical Transparency	Poor	Poor	Good
Degradation with Time	Slow	Slow	Fast
Carrier Mobility	~1 $cm^2/(Vs)$	~50-100 $cm^2/(Vs)$	~10-100 $cm^2/(Vs)$
Uniformity	Good	Poor	Good

Table 2-1 Comparison of Current TFT Materials.

MOs are unique in the semiconductor world for their optical transparency and low fabrication temperature. Many industries have taken advantage of those properties, making materials such as indium tin oxide (ITO) feasible for displays and solar panels. The electronic device market has also investigated their potential for advanced applications such as artificial implants, transparent oxide memory, biosensors, and interactive readable displays. [16] [17] [18] [19] [20] [21] [22] In short, with their superior properties comparing to conventional silicon competitors, MOs has a lot of potential to take more part in the electronic field. [24]

2.2. TFT Characteristic

2.2.1 Overview

The TFT relies on current flow modulation between source and drain electrode through the gate electrodes with different potentials. The gate electrode controls the current flow through the capacitive injection of carriers close to the dielectric vs semiconductor interface, initiating the field effect. As charge carriers accumulates under the gate bias, charge drifts between source and drain. In a AOs TFT, the channel layer lies between source and drain electrode and dielectric layer is imbedded between the semiconductor and the gate electrode. The device can be either top gated or bottom gated, top contact or bottom contact.

2.2.2. Band Structure

Carrier mobility is the most important factor when deciding the quality of the device. The transport of electrons can be described by traditional band theory. Amorphous oxides (AOs) are

wide gap semiconductors, with a conduction band minimum (CNM) and the valence band maximum (VBM), where the dispersions determine the electron and hole effective masses respectively as shown in Figure 2-3. In theory, smaller effective mass leads to larger CBM and VBM hybridization, and finally higher carrier mobilities. In comparison to transport behavior in silicon where sp^3 σ-bonding and anti-bonding states determines the VBM and CBM, AOs has large overlapping s orbitals in crystalline phase and amorphous phase, allowing easier transport of electrons, leading to higher mobility in general. [23] With such high tolerance for lattice distortion without compromising electron mobility, AOs could have electron mobility comparable to single crystals. [25] [26] The energy band gaps also differ greatly between AOs and silicon. MO semiconductors are transparent due to their energy gaps larger than 3eV in the visible spectrum. From a conventional point of view, high conductivity is related to opacity, but in MOs, the low optical absorption due to the large bandgap and the localized O 2p orbitals and metal ns-orbital interaction produce a band structure with high free-electron mobility due to the low effective mass. This property makes n-type MOs semiconductors thrive.

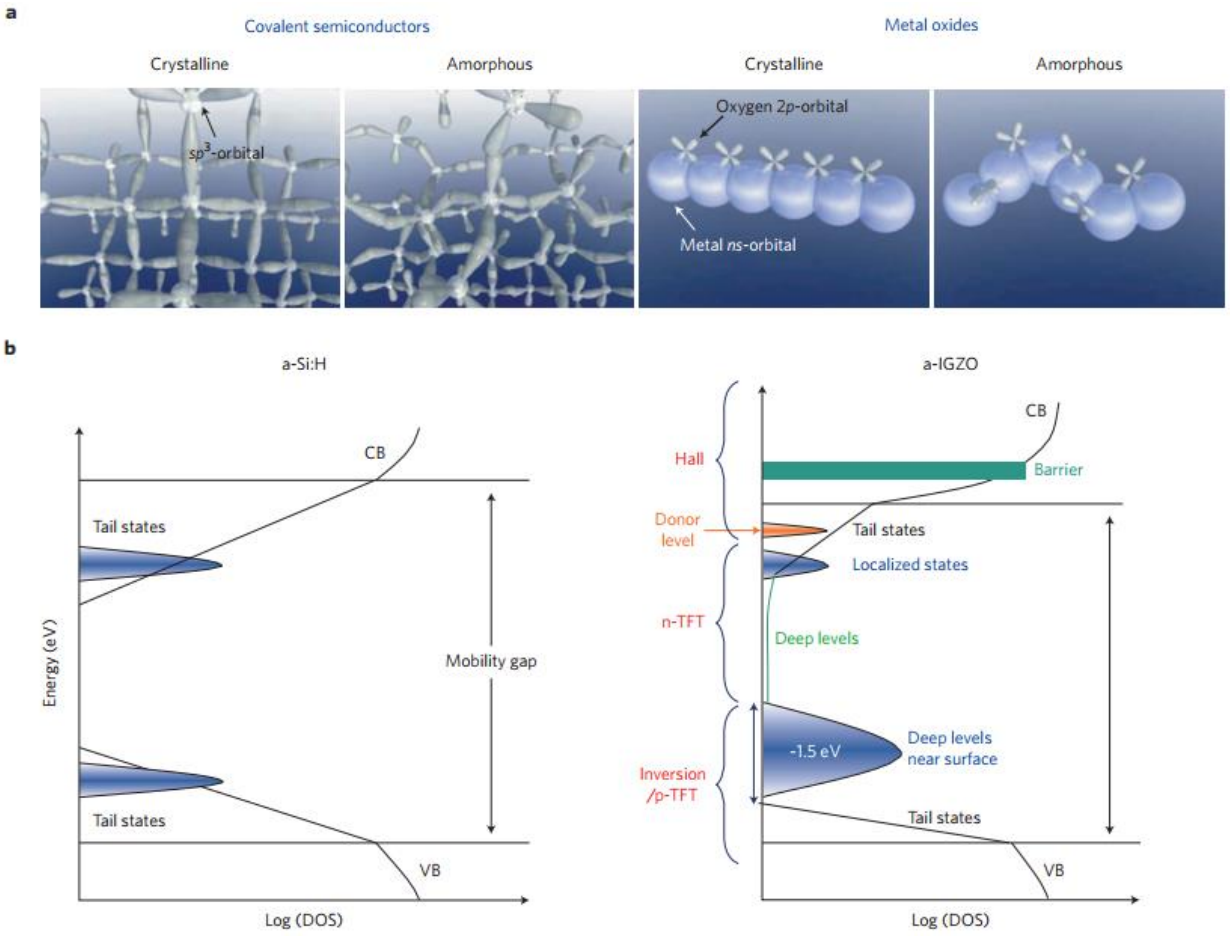


Figure 2-3 Band energy level in a-Si:H and MOs. [25] [27]

2.2.3. Metal Composition Effects

Different metals and metal composition could greatly affect device properties. MOs TFT could come in forms of binary, ternary and quaternary compounds. There are many functional binary systems reported including SnO_2, ZnO, In_2O_3, and Ga_2O_3. They are easy to fabricate, but those structures exhibit poor performances namely high resistivity, poor stability, and low on-off ratio. [27] Binary compounds are prone to crystallize, creating grain boundaries during the process, hinder transport behavior and scatter free carriers and degrade device reliability. Although those binary TFTs might have supreme carrier mobility, the property would degenerate quickly with time. In Figure 2-4 (b), it is shown that each element contributes differently to the overall carrier

concentration. The cut off level at -4.5 eV distinguishes cations and anions (donors and acceptors). Elements around this cutoff level are favorable for electron doping and increase carrier concentration. Electron concentration needs to be reduced to lower lever for successful TFT channel layer whereas an IGZO system has In and Zn that would increase carrier concentration, suppressing element Ga is needed. Ga has SSE value of -3.1 eV, making it a great suppressor for the IGZO system. [28]

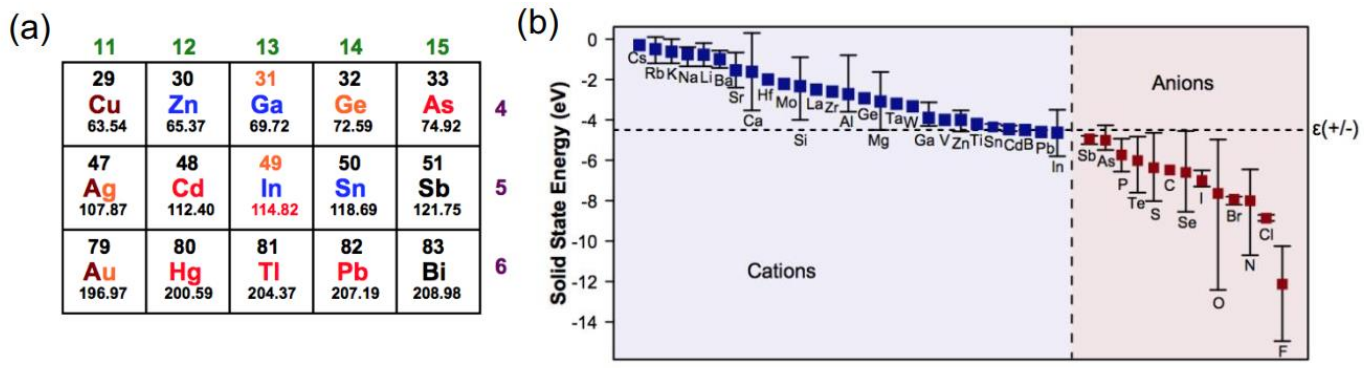


Figure 2-4 (a) Candidate elements for heavy metal cations with $(n-1)d^{10}ns^0$ electronic configuration [28] (b) Solid-state energy values for 40 elements for use in metal oxide semiconductors. [29]

Compound with two or more metal elements tend to stay amorphous. Systems including IGZO, indium zinc oxide (IZO) and zinc gallium oxide (GZO) are more common in amorphous form. Differences in atom size, ionic charges make it energetically more feasible to not crystallize. IGZO is the main interest of this study, crystallinity and hall-effect mobility is shown in Figure 2-5. Unless a system is at extreme concentration with ZnO or In_2O_3, amorphous system can usually be achieved. In IGZO. [32]

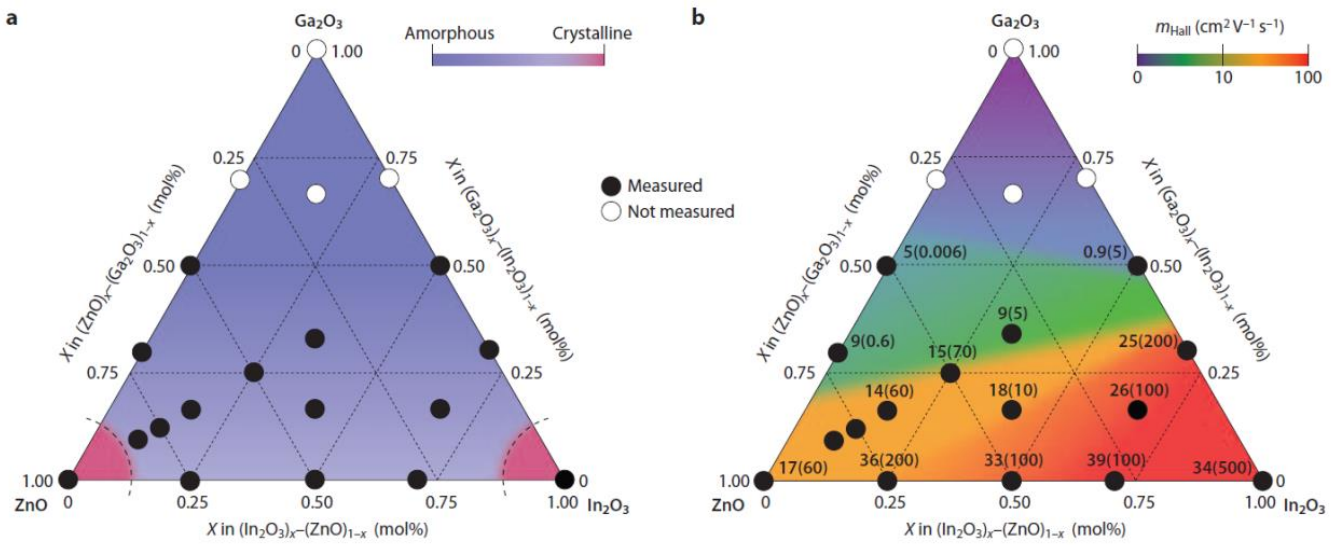


Figure 2-5 Crystallinity of representative metal oxide semiconductor and each hall mobility. [25]

Many studies have shown that performances of multicomponent materials heavily rely on their compositions. Metal composition effect is studied for vapor process as well as solution process. Studies include investigation of the effect of composition on electrical performance, composition effect of surface morphology and more. [30] Successful compositions include In:Ga:Zn ratio with 9:1:2, 2:2:1, 1:1:1, 2:1:2. In solution process, 2:2:1 exhibits the best performance in solution processed devices.

2.2.4. Device Structure and Electrical Characteristics

The four classic TFT configurations as shown in Figure2-6 (b) all has distinct properties and applications. [31] The staggered bottom-gated structure is widely used in LCD backlight for lower light sensitivity for the semiconductor layer. The coplanar top gate structures are usually used for large scale flat film that requires high temperature for processing. Bottom gate devices are good for surface modification. All those structures are suitable for MOs TFTs.

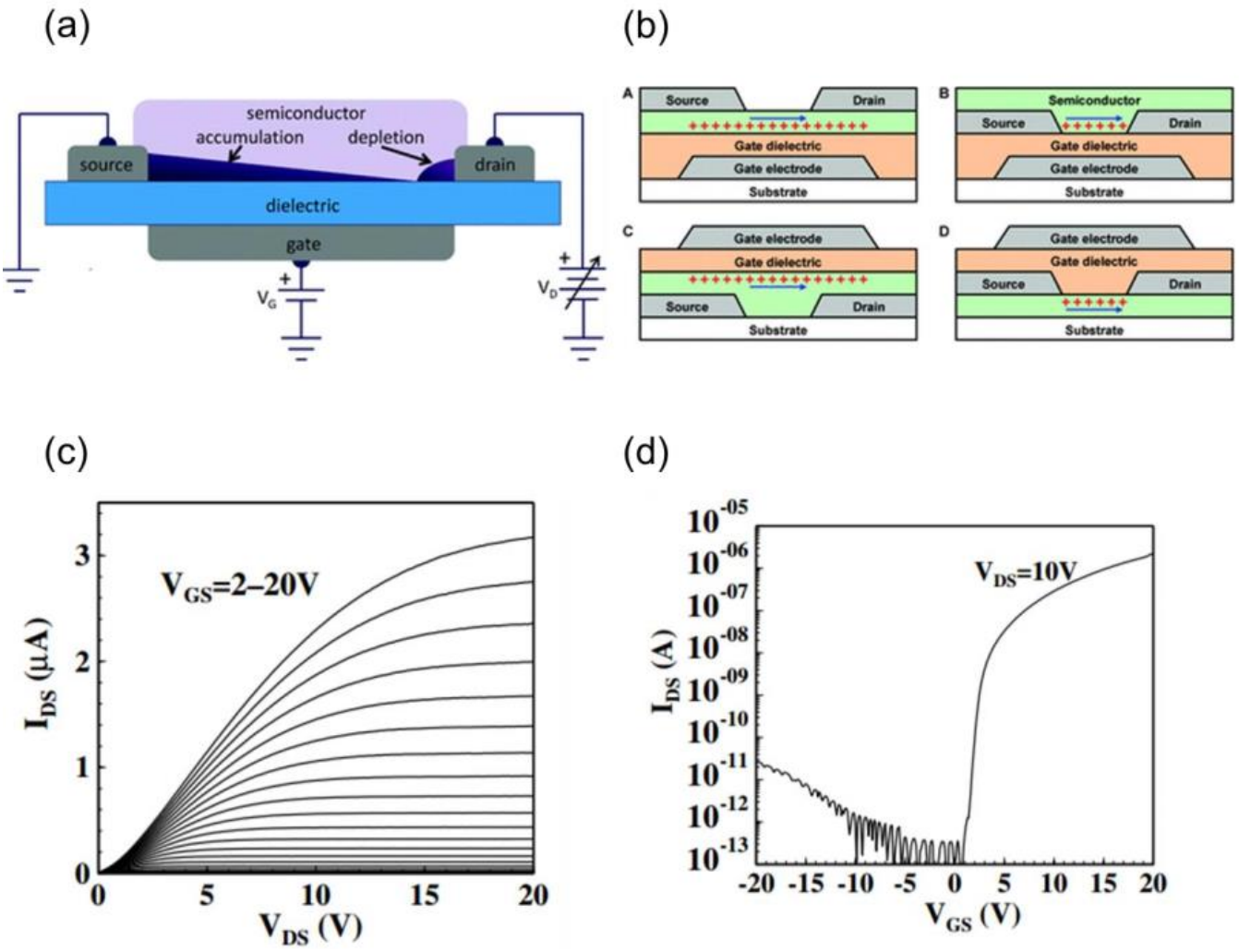


Figure 2-6 (a) Thin-film transistor schematic of device structure operating under VG. (b) Device architecture for A: Bottom-gate staggered TFT, Bottom gate: coplanar TFT, C: Top-gate staggered TFT, D: Top-gate coplanar TFT. (c) Output curve of a-Si:H TFT, (d) Transfer curve of a-Si:H TFT. [31]

MOs TFT has the same I-V behavior as MOSFET which can be described by Equation 2-1 and Equation 2-2, where μ is the field effect mobility ($cm^2/(Vs)$), C is the capacitance per unit area of the insulator (F/cm^2), V_t is the threshold voltage, V_G is the gate voltage, V_D is the drain voltage, and W and L are the channel width and length, respectively. [32] Under the bias applied to V_G, carriers start to accumulate and travel between the channels with increasing V_D. The current and V_D has a linear relation until the channel is saturated with carriers as described by Eq 2-1. Then it comes in to ta saturation region, where the there is no more increase in the current level,

described by Eq 2-2. The I_D vs V_D behavior is called an output curve and described by graph in Figure 2-6 (c). The saturation level can change by altering V_G. They are positively related. With higher V_G, more carriers can be accommodated at the semiconductor-insulator interface. [33] This I_D vs V_D behavior is called an output curve and described by graph in Figure 2-6 (c).

Equation 2-1

$$I_D = \frac{1}{2}(\mu_n C_i)\left(\frac{W}{L}\right)[2(V_G - V_T)V_D - V_D^2] \quad For\ 0 \le V_D \le V_G - V_T$$

Equation 2-2

$$I_D = \frac{1}{2}(\mu_n C_i)\left(\frac{W}{L}\right)(V_G - V_T)^2 \quad For\ V_D \ge V_G - V_T$$

The transfer curve, shown in Figure 2-6 (d) and Figure 2-7. demonstrate the relationship between I_D and V_G. As the voltage bias of V_G increases to a certain level, the device is considered to be in the turn-on mode, where I_D drastically increases, shown in Figure 2-6. (d) around V_G=0V. This voltage where the device turns on is called the turn-on voltage. By analyzing the output and transfer curve, information on device performance including threshold voltage, turn-on voltage, on/off ratio and subthreshold swing could be obtained, the device quality can be thus determined as shown in Figure 2-7. The on/off ratio is the ratio between the maximum drain current and the minimum drain current. The minimum drain current is noise level when the device is off. A good on-off ratio should be in at least 6 orders of magnitude for good amplification ability. [34]

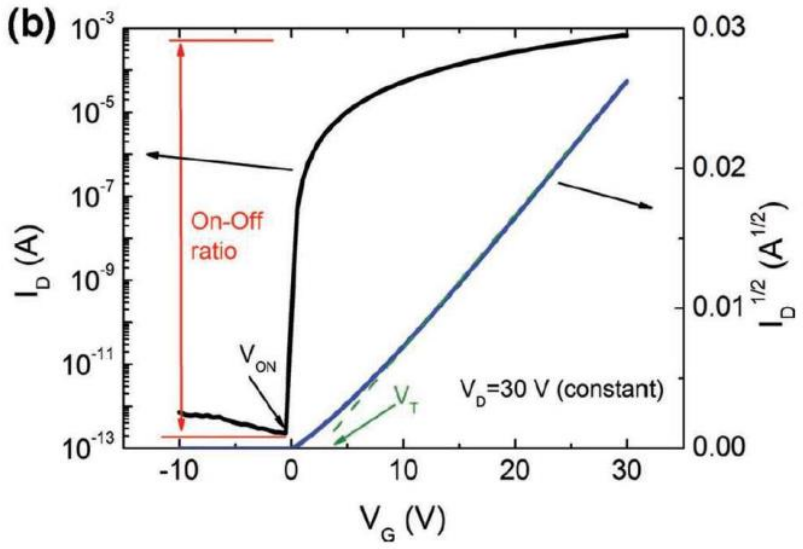


Figure 2-7 Transfer curve with on/off ratio, V_{on}, and V_T. [27]

The subthreshold swing describes an exponential behavior of the current as a function of voltage as shown in equation (6). It measures how efficiently a TFT turns on and off. [34] Low subthreshold is needed for reduced device power consumption and operation voltage. [35]

Equation 2-3

$$SS = \left(\frac{dlog(I_D)}{dV_G}\Big|_{max}\right)^{-1}$$

Carrier mobility μ also defines device quality for it describes the efficiency of charge carrier transport in a material, directly affect the maximum drain current of the device. The intrinsic mobility of a conventional bulk material can be extrapolated by the Hall-effect mobility. TFT is on a way smaller scale comparing to the bulk material, thus affected by scattering from dielectric charges, interface states, and surface roughness. [36] The effective mobility (μ_{eff}), field-effect mobility (μ_{FE}), and saturation mobility (μ_{Sat}) are described with the equations below. They are affluence by transconductance (g_m) and conductance (g_d). Field-effect mobility and effective mobility are calculated at low drain voltage, whereas saturation mobility is calculated at high drain voltage.

Equation 2-4

$$\mu_{eff} = \frac{g_d}{C_i \frac{W}{L}(V_G - V_{TH})}$$

Equation 2-5

$$\mu_{sat} = \frac{(\frac{d\sqrt{I_D}}{dV_G})^2}{(\frac{1}{2})C_i(\frac{W}{L})}$$

Equation 2-6

$$\mu_{FE} = \frac{g_m}{C_i \frac{W}{L} V_D}$$

2.3 Fabrication methods

2.3.1. Vapor Processed Transistors

Vapor processing is a traditional to make transistors. It uses evaporation technology, sputtering, atomic layer deposition and radiofrequency magnetron sputtering. Those technology has high precision and can control the crystallinity of MOs film. Despite the relatively high precision on atomic level, it is still hard to achieve large scale devices with consistent accuracy especially in the case of single crystals. What's more, carrier density in MOs is hard to control using those methods. [37] [38] H. Hosono had proposed epitaxial grown IGZO on single-crystal yttria-stabilized zirconia substrate. [15] In such way, IGZO could stack along the (0001) direction. Those TFTs exhibit decent mobility and on off current and can be fabricated under room temperature by pulse laser deposition. With such intricate system, the amount of time used, and masks used for patterning are lot more comparing to the other methods. Vapor processed transistors are well studied and had matured over the past years, yet its high cost makes it harder to be manufactured in large scale.

2.3.3. Solution process

Solution processing starts with a MO precursor solution. It can then be spin coated, spray coated or printed on a substrate. Spin coated is one of the simplest methods for deposition thin film on a large smooth surface. Precursor is first dropped evenly onto the surface, followed by bring the rotary plate to a certain speed to evenly spread the material on the surface. An annealing process is followed, the substrate is brought up to certain temperature for the metal oxides to form network and sol gel. Spray coating is another inexpensive way to deposit thin film on flexible substrate such as plastics. The film is grown by aerosol spraying precursors solutions spraying on pre-heated substrate. Chemical reaction drives the reagent to form gel when contact. Solution process can be performed in a wide range of temperature and are relatively cheap and simple. The processing time is way less comparing to vapor-phase processing, and it requires less masks us for patterning. [24] As metal salts dissolve in water, aqueous compound forms as shown in Figure 2-8. Water and UV interact, forming OH radicals, later leads to formation of M-OH structures. M-OH and M-OH groups forms M-O-M structures that cannot be etched easily.

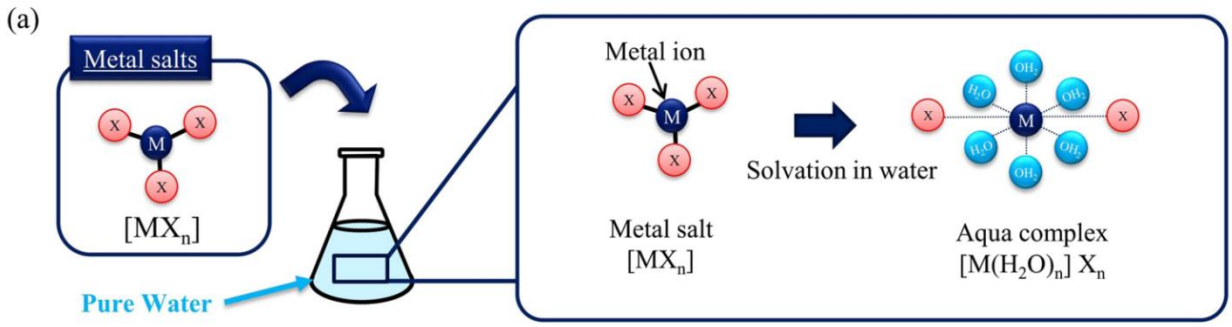


Figure 2-8 Aqua complexes $[M(H_2O)_m]X_n$ formed by solvation with water molecules in the aqueous precursor. [39]

The schematics of both vapor and solution processed patterned devices are shown in Figure 2-8. The vapor process is way more intricate and convoluted than solution process as there are way more steps and masks used for the conventional process method. What is not shown in this graph is that the conventional photolithography process must take place in a cleanroom, which also boosts the time and cost of the fabrication process.

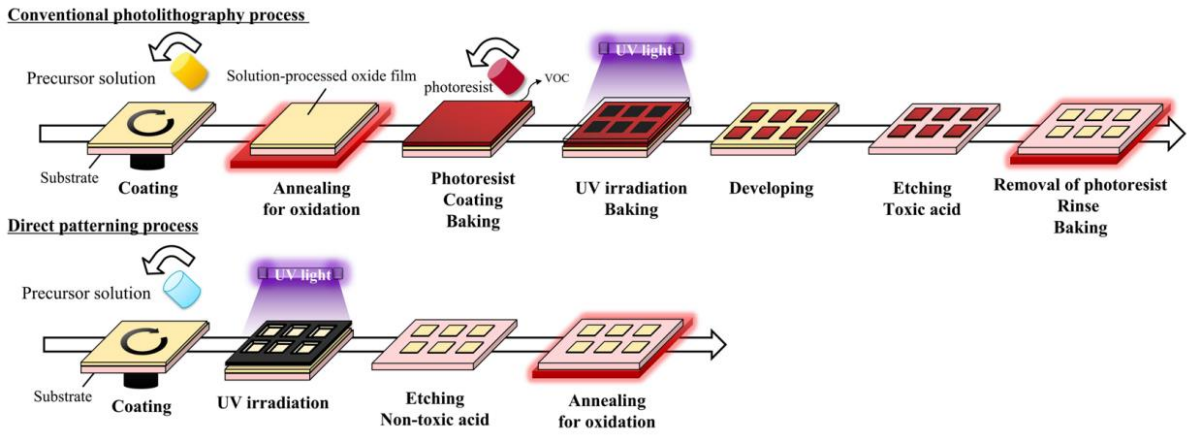


Figure 2-9 Comparison of process flow for metal oxide film fabrication using a conventional photolithography process vs. direct patterning process. [48]

2.4 Research Objective

Currently the most promising cheap and simple way to manufacture MOs TFT devices is via sol-gel process. The biggest issue with this method is the device characteristics is not yet comparable with those fabricated with vapor, in addition to low stability and repeatability. But its potential for large scale application is attractive. To achieve stable, repeatable, and high-performance devices, techniques such as patterning, and pre annealing was applied to this study.

Chapter 3

EXPERIMENTAL PROCEDURE

3.1 Experiment Overview

The experiment is a five steps process using various techniques. First, developing an IGZO so gel layer. This step provides an even layer of amorphous IGZO system on top of the silicon wafer. Second, UV ozone radiation is applied to pattern the so gel. This pre-irradiation annealing process put water into half-annealed condition. The third step is to remove the non-patterned area. Different etchants were applied. Forth, the system is brought to low temperature annealing. Finally, aluminum was deposited on top of IGZO to form channels. A sample group without the direct light patterning step was also made in comparison for device characteristics.

3.2 Experimental Procedure

3.2.1 Substrate, Metal Oxide Solutions, and Etchant Preparation

3.2.1.1 Synthesis of Metal Oxide Solutions:

The 0.1 M IGZO is composed of by indium nitrate hydrate ($In(NO_3))_3 \cdot xH_2O$, Aldrich, 99.999%), gallium nitrate hydrate ($Ga(NO_3))_3 \cdot xH_2O$, Aldrich, 99.999%), and zinc dihydrate ($(Zn(CH_3COO)_2)_3 \cdot 2H_2O$, Aldrich, 99.999%) dissolved in 2-methoxyethanol (2ME, Aldrich, 99%) in a total metal ion molarity of 0.1M, and 2% of acetylacetone (Aldrich, 99999%). The molar ratio of the In, Ga, Zn in solution was 2:2:1. The solution is then brought up to 80 °C on a hot plate for an hour to dissolve completely. After the solution had cool down, it was filtered with 13 mm

syringe filter (Aldrich) to remove dust, and particles. The comparison group is made without the acac additive.

3.2.1.2 Substrate Preparation:

Six-inch highly boron doped silicon wafer (p++ Si) with thermally grown 100 nm SiO_2 (WafterPro. Inc) was chosen to be the substrate for this experiment. The wafer is first cut by diamond tip scriber into 1cm*1.8cm pieces. The substrates were then sonicated in surfactant (Alconox, mixed with water in 1:200 volume ratio), DI water, and isopropyl alcohol sequentially for half an hour each. UV irradiation was applied to the substrates for 15 minutes to further remove possible organic matters on the substrates and improve wettability and uniformity for spin coating.

3.2.1.2 Etchant Preparation:

Acetic acid (Aldrich, 3%) was dissolved in Methanol (Aldrich, 99.999%) in 1:10, 1:20, and 1:40 volume ratio. Yttrium nitrate hexahydrate ($Y(NO_3)_3$, Aldrich, 71.0%) was selected as a potential additive to the previous system with concentration of 0.1 mol/L.

3.2.2 Device Fabrication

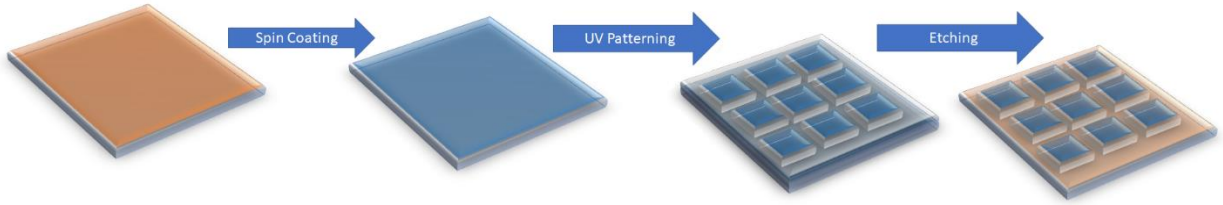


Figure 3-1 Schematic of sol gel processing.

3.2.2.2 So-Gel Formation

80 µl of IGZO solutions were spin coated on to the substrate at 3000 rpm for 30 seconds. It was then baked on a hotplate for 1 minutes at 100 °C. This process was repeated for 3 times, 5 times, and 7 times.

3.2.2.3 UV Radiation

A3 mask with rectangular cut outs with size of 100*130 μm was applied on to the substrate. The substrates are then brought into UV ozone generator (Jelight Company) for 5 minutes, 20 minutes, and 40 minutes for pre-annealing. The light source is generated by high-intensity and low-pressure mercury vapor UV gird lam. The emission peaks were 184.9 nm and 253.7 nm. Automatically generated ozone disassociates at those emission peaks.

3.2.2.4 Etching

The substrates were dipped into the different etchants for 5 minutes or 10 minutes, or till the non-pre annealed part faded completely.

3.2.2.5 Annealing

The substrates were brought to a preheated hot plat at 400 °C in air for 3 hours. A glass shield with opening for circulation was provided to avoid contamination. The substrates experienced rapid cooling to room temperature.

3.2.2.6 Channel Deposition

A shadow mask with channel dimension of 100 μm in width and 1000 μm in length was put on top of the substrates. A layer of 100 nm aluminum was deposited with thermal evaporator below 10^{-5} bar. The SiO_2 layer was scrapped off to expose Si for a bottom-gate, top contact structure.

3.3 Device Characterization

Devices' electrical characteristics were tested by probe station (Agilent 4155C) in ambient condition. Positive bias stress were applied at 0, 100, 200, 500, 1000, 2000, 5000, 10000 seconds. The gate-source voltage was set to 30V and the drain-source voltage was set to 10V. Precursor

solution was tested for dynamic light scattering (DLS) and zeta potential with Zetasizer, Malvern Panalytical, Huckel Approximation. Study on the morphology of the IGZO film through its forming phases was carried out by optical microscopy (Nikon Eclipse LV 150) SEM (FEI Nova Nano230) images was taken with the following parameters: HV=12.0 kV, spot size = 4, working distance at 5mm. Calculation of mobility, hysteresis, V_{on}, transfer curve, on/off ratio and subthreshold swing are done in MATLAB, attached in Appendix A.

Chapter 4

Results and Discussion

4.1 Determinant for successful fabrication

The lengthy fabrication process introduced many variations in the devices fabricated. Several parameters were investigated to see if there was any determining effect on device characteristics. Characteristics that indicates successful device fabrication includes high electron mobility, low subthreshold swing, stability, large on/off ratio, and low leakage current. The device structure in cross sectional view is shown in Figure 4-1.

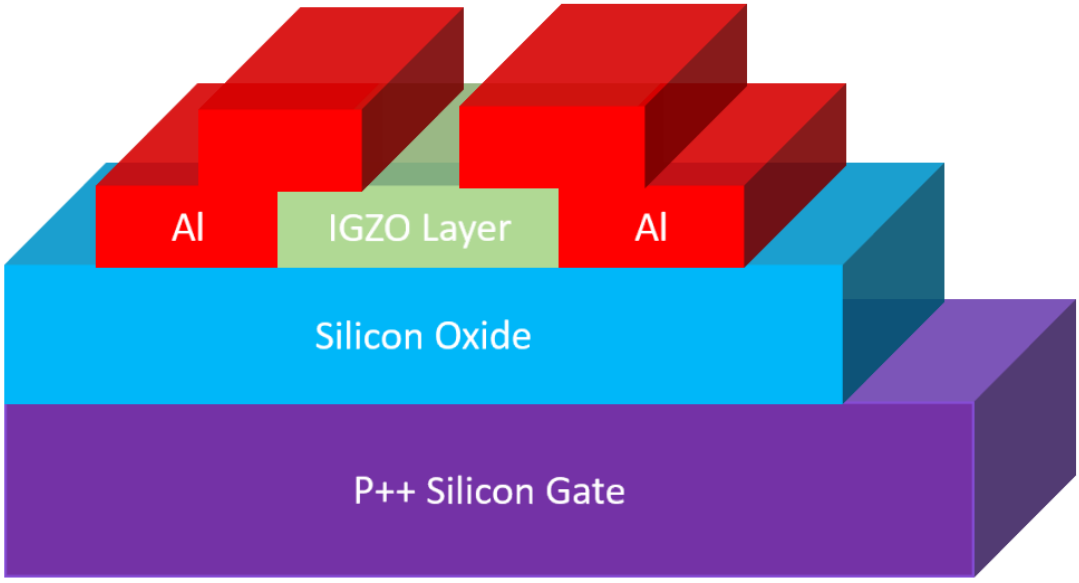


Figure 4-1 Schematics of direct light patterned device cross section.

4.1.1 Impact of direct light patterning

Direct light patterning greatly decreases leakage current in all devices, comparing to devices fabricated without direct light patterning, structure shown in Figure 4-2. Without direct

light patterning, the leakage current can account for 5% of the total current, sometimes even as high as 30% of the total current. There are two different tracks for leakage current to occur in a non-patterned device. Current could leak while pathing between source and drain. The leakage could also occur between the source and drain across the entire layer of IGZO since it is conductive. With direct light patterning, this problem can be eliminated as the channel is small and just enough to tough the electrode, the carrier pathway via the entire layer of IGZO is cut off. Noise can be reduced greatly with this method, and the device could work at a higher efficiency level. Mobility, hysteresis, V_{on}, and off current all have significant improvement from the reduced channel size as shown in Appendix B.

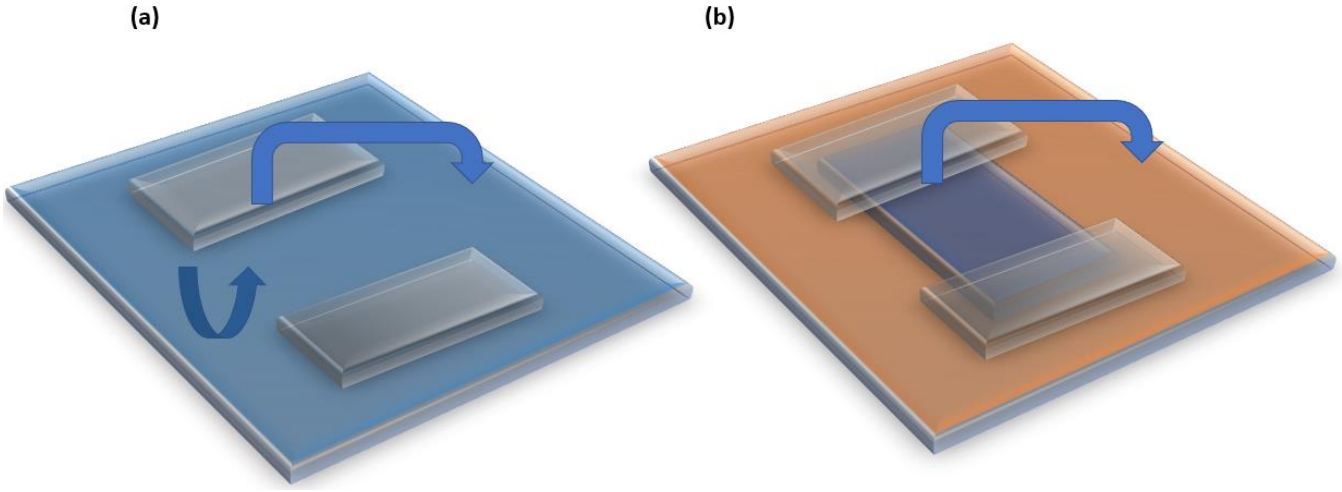


Figure 4-2 (a) Leakage current between channel and through dielectric layer. (b) Leakage current only between channels.

4.1.2 Impact of UV and Ozone Exposure

This study is a collaboration with Dr. Guangwei Xu, and Dr. Zhenxu Wang. Study on the impact of device performance solely on UV and ozone treatment was conducted. Sample with no UV and ozone treatment was compared to sample treated UV and ozone without patterning. It was interesting that sample treated with UV and ozone showed superior device characteristics in all

aspects. Mobility, turn on voltage, subthreshold swing all had seemed to improve with the UV ozone treatment. What's more, the mobility at high gate voltage bias usually drops in the untreated group but did not do so in the UV and ozone treated devices. This phenomenon was further investigated with IGZO system with 1:1:1 ratio and with four probe resistance testing. It is found that the mobility degradation at high bias originates from phonon scattering in the band-like transport regime. At high gate bias, contact resistance dominates at high gate bias as the channel resistance decreases.

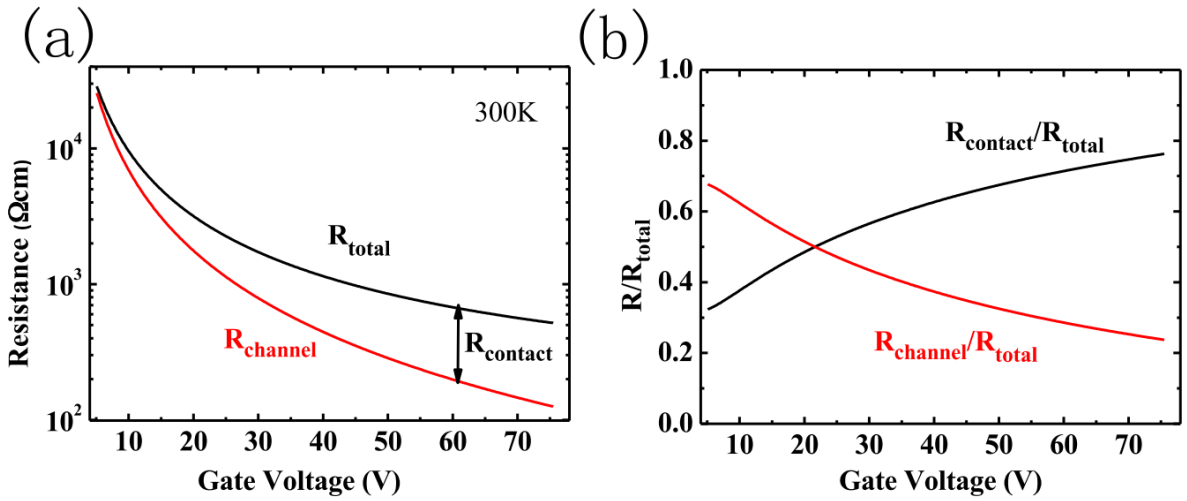


Figure 4-3 Contact resistance extracted by gate four-probe measurement. (a) Total resistance and channel resistance depend on gate voltage, extracted from two-terminal and four-terminal transfer curves at 300K. (b) Ratio of contact resistance in total resistance. [41]

Improvement of post current at high gate voltage is done by utilizing UV-ozone pre-annealing. The assumption is that the UV ozone treatment filled the oxygen vacancies, improving the contact between IGZO and the electrodes, reducing the contact resistance. Hydroxyl group was also introduced by UV treatment, which served as a donor in IGZO, generating free electrons, thus boosting the mobility. During this set of experiment, comparing the effect of UV ozone treatment solely, it is shown that there was a 40% increase of mobility at high gate bias as interfacial defect concentration reduced by the UV ozone treatment.

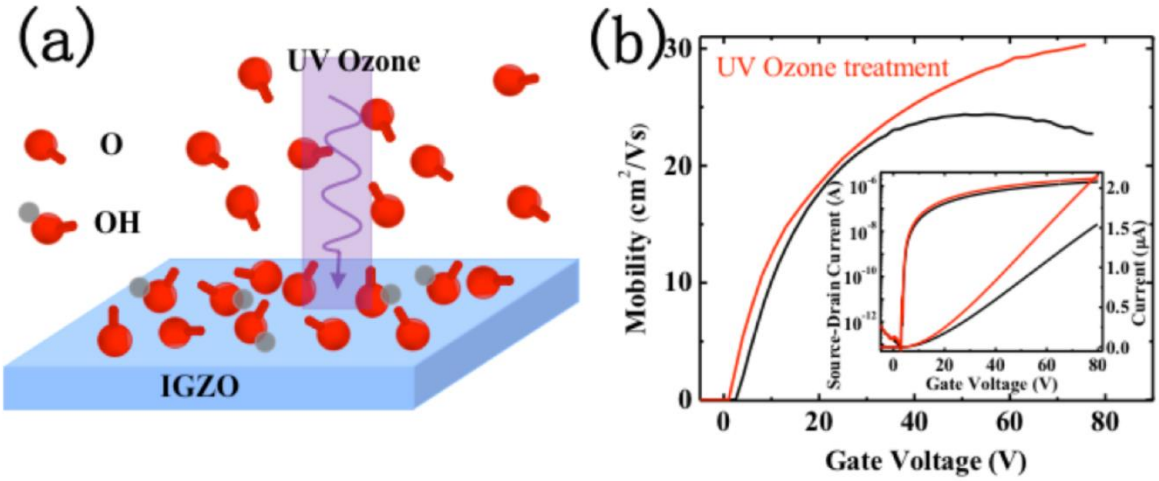


Figure 4-4 UV ozone treatment on a-IGZO film. (a) Schematic shows the surface chemical modified by UV ozone. (b) Mobility of the device with UV ozone treatment and the original device, and the current-voltage curves. [41]

4.1.3 Impact of Sample Roughness

This study is a collaboration with Dr. Zhengxu Wang. Before examining then samples with SEM, it was assumed that samples with better uniformity, i.e. roughness, would have better performance for its homogeneous coverage for electron transport. It was interesting to find that samples with features in the channel region exhibit equal or even better characteristics than smooth ones. To make more comparison group and study this phenomenon, acetic acid was also introduced as an additive to examine the relationship between sample performance and roughness. To examine the actual feature, AFM was used and shown a different story. It is shown that the dielectric layer with no additive have the roughest surface, followed by dielectric layer with AcOH and acac additives, respectively. Acac additives shows the smallest feature with the best device performance as shown in Figure 4-5. Smaller features are more evenly distributed while larger features spread out more. Just by observing the SEM images, it appears that the "rougher" surface has better device performance. By using AFM, it is shown that the density of spikes is way less in the seemly rough ones as in Figure 4-5 (c)-(e). Future step by step analysis shows that the peaks

started out high after soft baking and shrank after high temperature annealing. Larger surface tension was introduced by acac as pinholes formed and expanded at highest rate among all three scenarios.

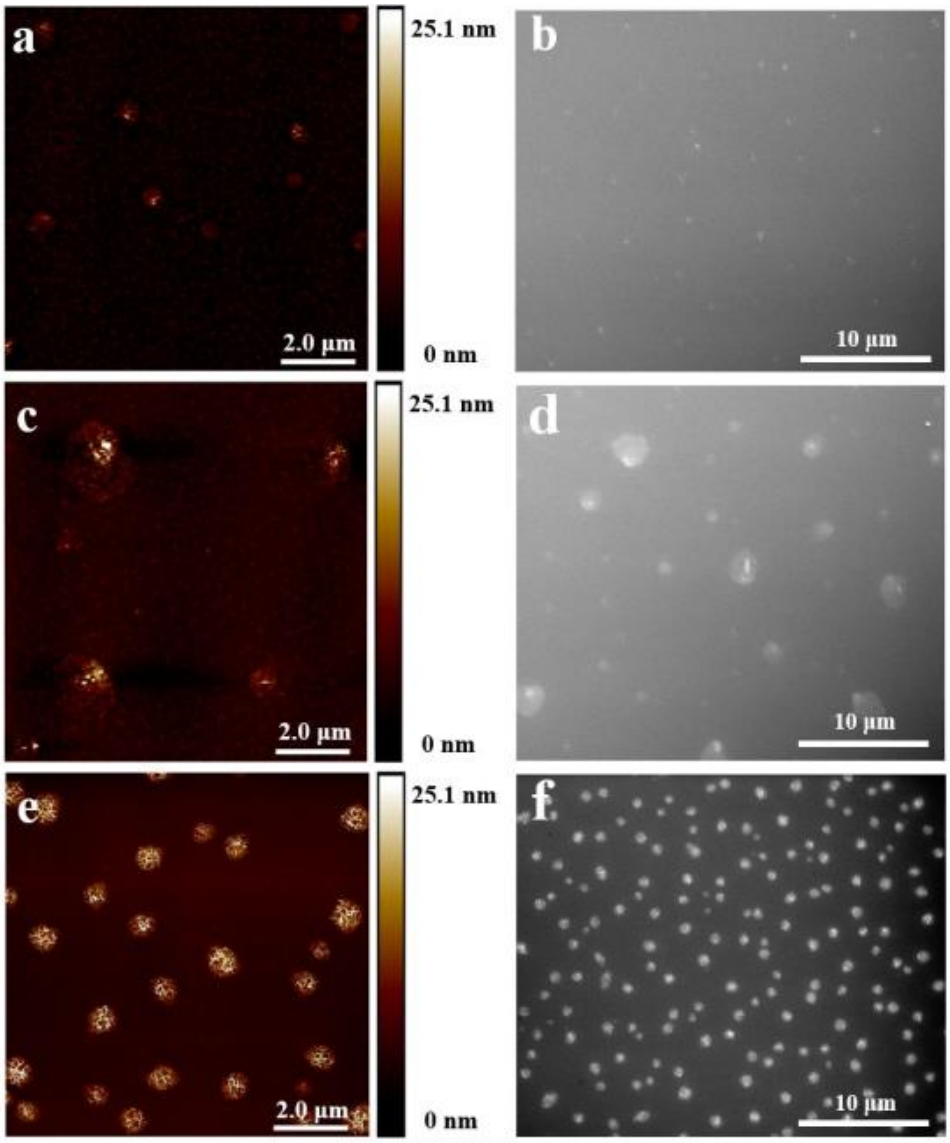


Figure 4-5 (a) AFM image of IGZO film with no additive. (b) SEM image of IGZO film with no additive. (a) AFM image of IGZO film with no AcOH. (a) SEM image of IGZO film with AcOH. (a) AFM image of IGZO film with acac. (a) AFM image of IGZO film with acac. [42]

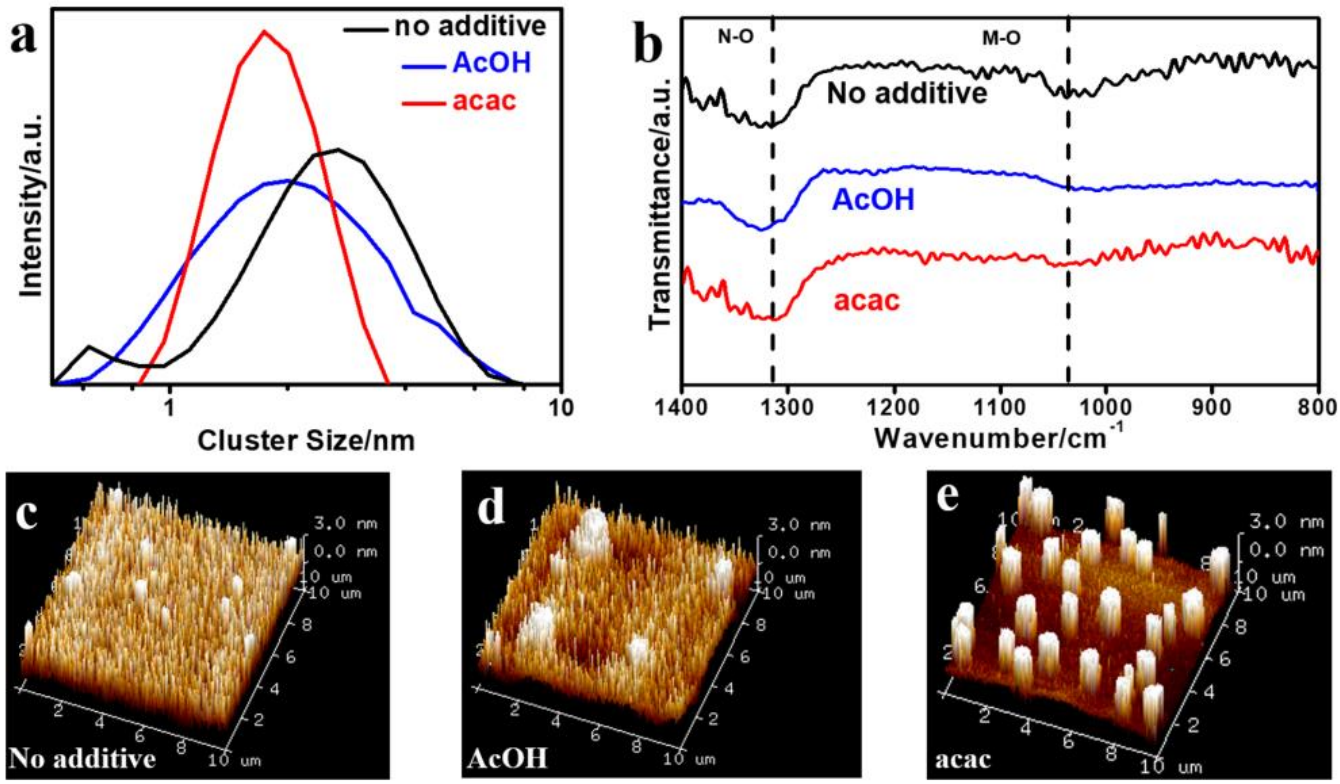


Figure 4-6 (a) Cluster size distribution in the IGZO precursor solution with different additives measured by dynamic light scattering (DLS). (b) Fourier-transform infrared spectroscopy (FTIR) of IGZO wet film fabricated by a spin coating precursor solution without annealing. (c)-(3) 3D AFM images of the device feasible IGZO film with no additive, AcOH as additive, and acac additive. [42]

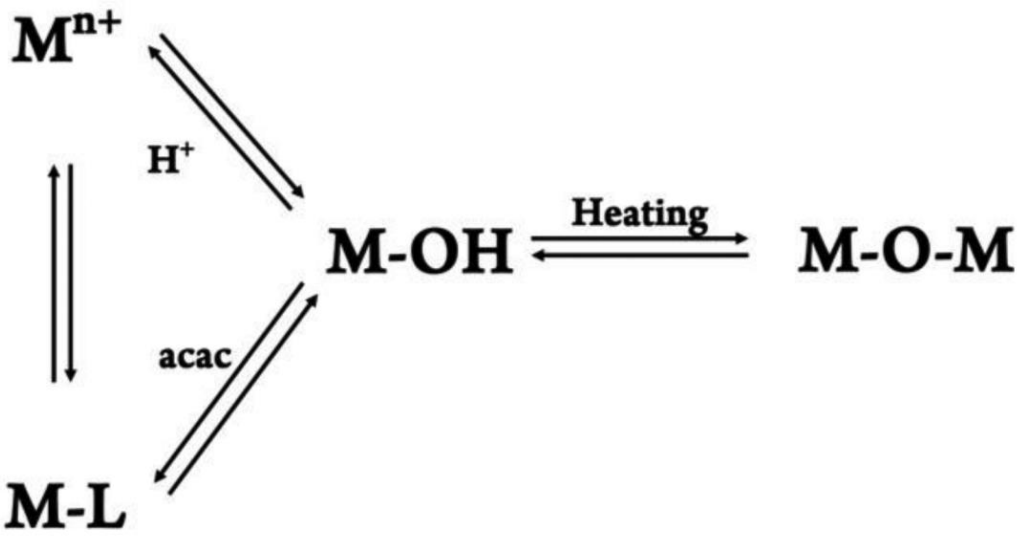


Figure 4-7 Equilibriums in the Metal Oxide Precursor Solution [42]

Metal oxides undergoes hydrolysis as shown in Figure 4-7. Metal cations such as In^{3+}, Ga^{3+}, and Zn^{2+} has empty outer shell electron orbital and small ion radius from d-orbital

contraction, are prone to go through hydrolysis and produce metal-hydroxyl (M-OH) groups. This can happen under trace of H_2O influence. Even though the solution used in this experiment 2-ME, water vapor from the air, impurity, and metal salts are sufficient to start the process. The M-OH structure is then condensed, forming metal-oxygen-metal (M-O-M) clusters in the solution. The left-over M-OH structures could then condense and form more clusters in later condensation process. It is shown in Figure 4.1.3.3 that M-OH groups are mostly located on the outer shell, ready to react.

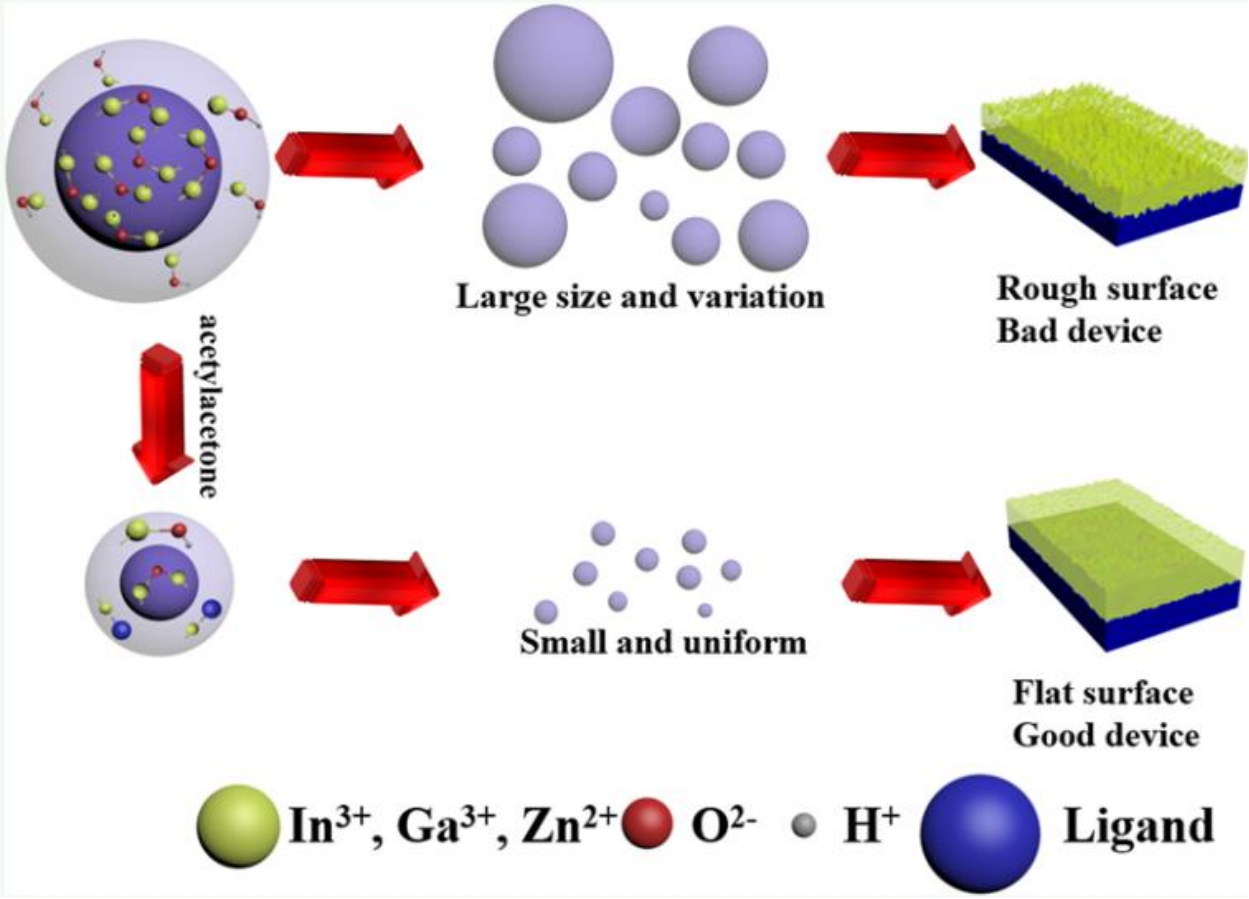


Figure 4-8 Hydrolysis, cluster structure, cluster distribution depending on precursor reactant, and final film morphology, film-substrate of IGZO films. [42]

When different reactants are introduced to the solution, equilibrium of this reaction shifts. When AcOH is introduced, the equilibrium is shifted to the left, fewer M-OH structures form, reducing the cluster size, and it exposes more metal cation at the out most shell, enlarging the

reaction area, and catalyze the formation of clusters. Acac functions as a ligand, shift the equilibrium to form stable metal-ligand (M-L), reducing the formation of M-OH and M-O-M groups as well. As the film goes through annealing, cluster are thought to accumulate and condense. System with acac additive have the smallest and most uniform clusters, forming a relatively flat surface providing good contact.

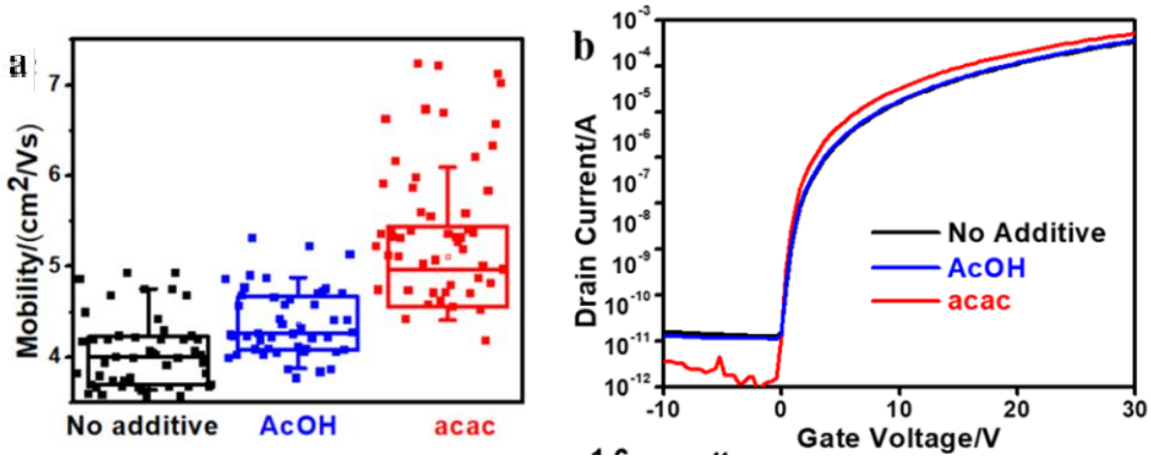


Figure 4-9 (a) Comparison of device mobilities. (b) Comparison of transfer curves. [42]

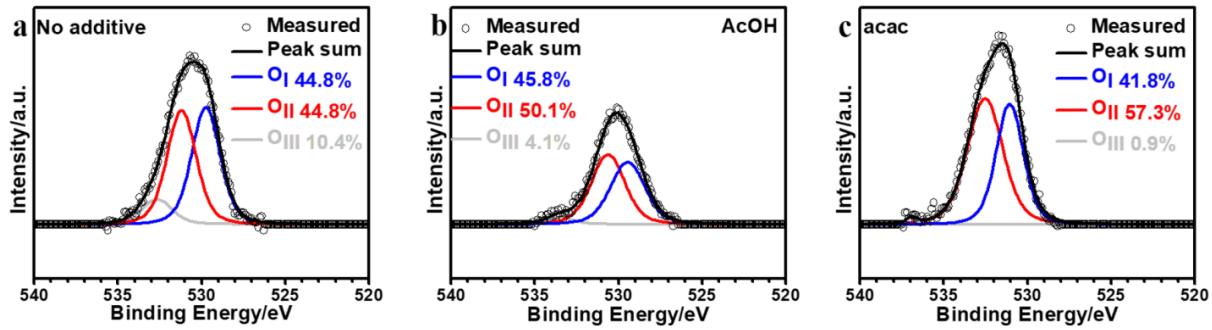


Figure 4-10 XPS analysis of 1s oxygen level in the IGZO film with (a) no additive. (b) AcOH additive. (c) aca additive [42].

The cluster formation in solution before spin coating and annealing was also studied. DLS was performed and shown the distribution of clusters in precursor solutions. Clusters already formed in all the solutions before applied due to the trace water molecule introduced by the environment, metal oxide salt, and process itself. The cluster size is the largest when there is no

additive in the system, where the diameter of clusters was up to 2.7nm in diameter. In AcOH additive solution, the diameter reduced to 2.4nm, and in acac additive solution, the diameter is further reduced to 1.8nm on average. Zeta potential of clusters were measured for determination of stability. The zeta potential was 2.97/mV, 2.4/mV, and 4.11/mV for precursor with no additive, precursor with AcOH additive, and precursor with acac additive, respectively. The stability of those clusters was not high, and ready to react in the later steps of the process. There was sufficient evidence that condensation occurs after soft baking, with more M-O-M structures observed after the film got annealed. The evolution of the growing and shrinking process examined with optical microscope is attached in Appendix C.

To examine the chemical environment of the films, XPS was performed. It is shown that oxygen peaks vary as additives differs. Three types of oxygen peaks emerged, including saturated oxygen at binding energy O_I around 529 eV, oxygen vacancy O_{II} at about 531 eV, and trace oxygen O_{III}. This concludes that with richer oxygen environment, less cluster forms, cluster size decreases. Oxygen vacancies are major source of IGZO carrier, with more oxygen vacancies in the sample, the mobility increases. It is noted that the off current is significantly lower, and the on off ratio of acac system film is lower than the other two. It is noted that the mobility of acac additive system is generally higher but has exceptionally low stability as it spreads from 4.2 cm^2/Vs to 7.3 cm^2/Vs, whereas the nonadditive system and the AcOH system are more repeatable. Further study on In, Ga, Zn atoms environment using XPS was conducted and attached in Appendix D, indicating more oxygen vacancies formed when cluster size is smaller.

4.1.3 Impact of Etchant Composition

In general, etchant with 5% AcOH and 10% ACOH has the best results comparing to other compositions as shown in Appendix B and table 4.1.3.1. No good results were found using any other concentration combination as listed in Appendix B. It is not confirmed why the concentration effects the performance. The assumption is that after soft baking and UV pre-annealing, the stability of the M-O-M bonds are not stable yet (as correlated to the zeta potential). As AcOH was introduced and could interact with the system, modifying the surface structure and provide better contact. Although both groups are better than the non-additive comparison group, the one with 5% AcOH has superior performance. It is assumed that the higher concentration etchant has too high of reaction rate, where it damages the pre-annealed film, etching the M-O-M structures and unreacted M-OH groups, diluting the active layer, worsen the device performance. The sample etched with lower concentration of AcOH faces similar problem. In order to have a clean channel area, slower reaction (lower concentration) would require longer etching time, damaging and diluting concentration of M-OH in the film.

	Process made with 5% AcOH etchant	Process made with 10% AcOH etchant	Comparison group, without patterning
Mobility	5.97±0.40 $cm^2/(Vs)$	4.4784±0.04 $cm^2/(Vs)$	4.05±0.93 $cm^2/(Vs)$
V_{on}	0.32±0.19 V	0.5±0.2 V	-1.72±2.76 V
Hysteresis	0	0	0.56±0.22 V

Table 4-1 Comparison of device performance with different etchants.

Chapter 5

Conclusion

From this experiment, it is shown that direct light patterning can be successfully used to fabricate IGZO TFTs. The patterning drastically decreases the leakage current of the device. The pre-annealing process via UV ozone showed a surprise improvement of overall device performance especially at high voltage due to modification in contact resistance. It is also shown that flatter surface made with additive performs better thank rough surfaces. Lastly, etchant concentration seems to have effect on the device performance. Contact resistance, oxygen vacancies, off current, and surface morphology were found to be the dominating factors behind outstanding devices.

Chapter 6

Future work

The results had shown that direct light patterning is a promising alternative to the traditionally fabricated devices in a cleanroom environment, could still be improved for better device performance. With the help of direct light pattering, UV ozone treatment, and cluster size modification, devices with good performances were achieved. It is still hard to tell which one of those factors contributes more to the overall success of devices. After all, there are so many variables to control for in a solution processed transistor. Different etchant might induce chemical reaction which stabilized the film. Etchant with different acid combination could be used in future work to determine what type of reaction and reaction rate would improve the performance of devices without sacrificing any of the device properties. There is no conclusion on how those stops affect each or if they counteract and suppress one another. Future work can be focused on what is the most performance determining factor, and how to tweak all those factors to achieve even better performing devices.

APPENDIX

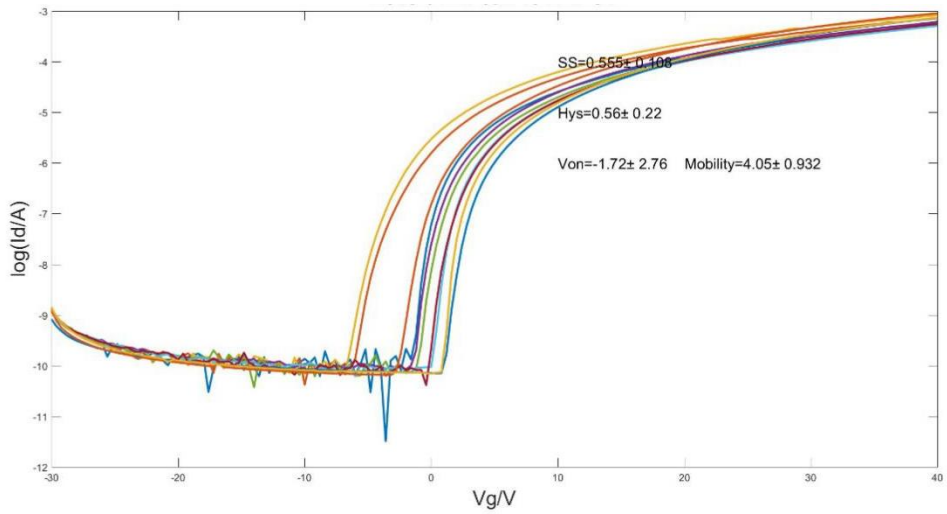
Appendix A-MatLAB Code for Calculation

```
% Vg=0;
% Id=0;
SrcDIR=uigetdir('Choose the source folder!');
cd(SrcDIR);
Data_File=dir('*.csv');
    onOffRatioCollection=zeros(16,1);
    SSCollection=zeros(16,1);
    mobilityCollection=zeros(16,1);
    VonCollection=zeros(16,1);
    counts=size(Data_File);
  for j=1:counts(1)
    [Vg,Id]=readCsv(Data_File(j).name,'B252:B427','E252:E427');
  Idsize=size(Id);
  lgId=zeros(Idsize);
  sqrtId=zeros(Idsize);
  for i=1:Idsize(1)
    lgId(i)=log10(Id(i));
    sqrtId(i)=sqrt(Id(i));
  end
%       [lgId,sqrtId]=prepareId(Id);
    onOffRatioCollection(j)=seekOnOffRatio(Id);
    SSCollection(j)=seekSS(lgId,Vg);
```

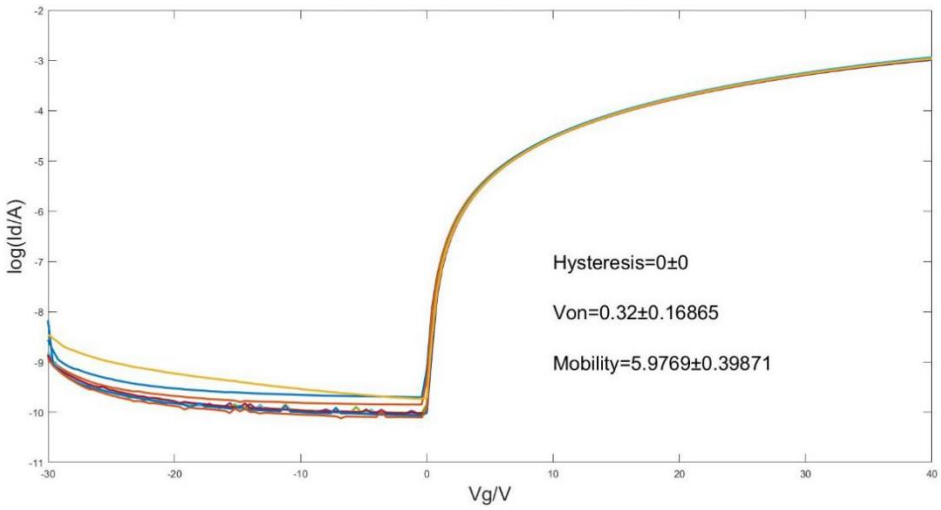
```
        [VonLocation,VonCollection(j)]=seekVon(Id,Vg,lgId);
        [kmax,Vth]=seekVth(Id,Vg,VonLocation,sqrtId);
        mobilityCollection(j)=seekMobility(kmax);
    end
function [Id,Vg]=readCsv(filename,IdRange,VgRange)
```

Appendix B-Comparison of device performance with and without patterning

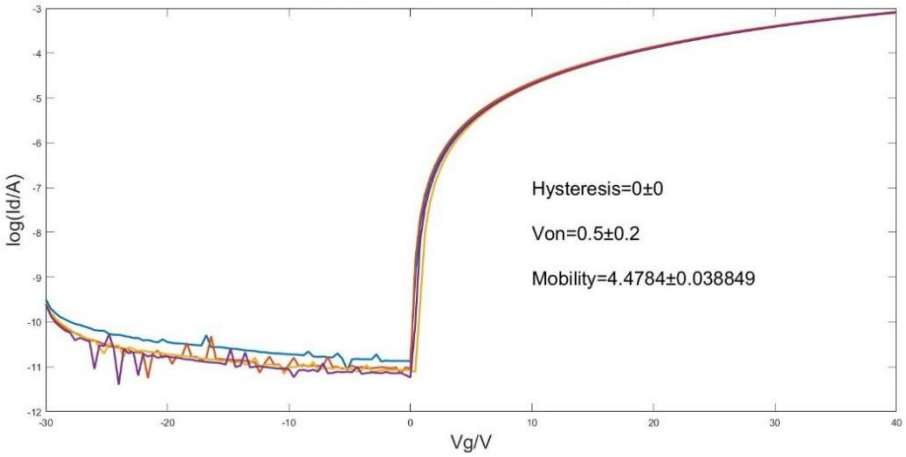
Without patterning



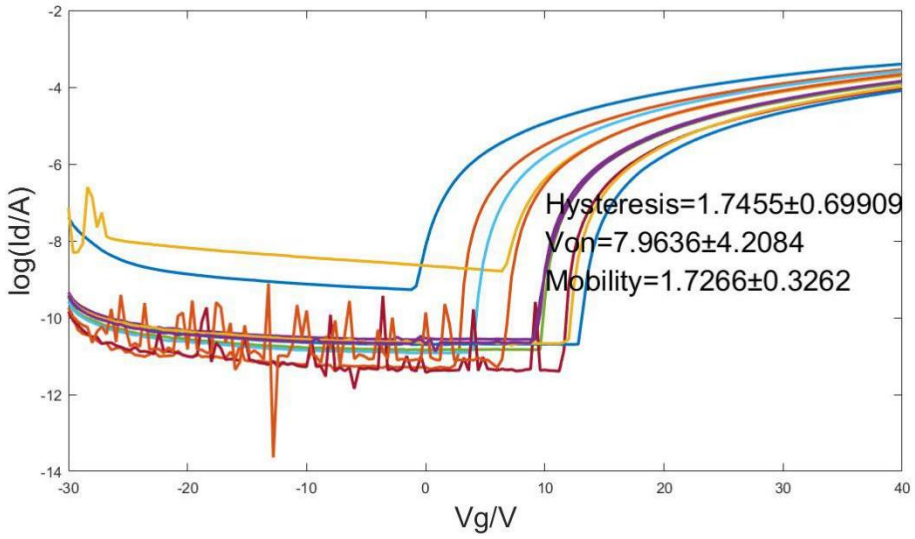
With Patterning, Etchant 5%AcOH



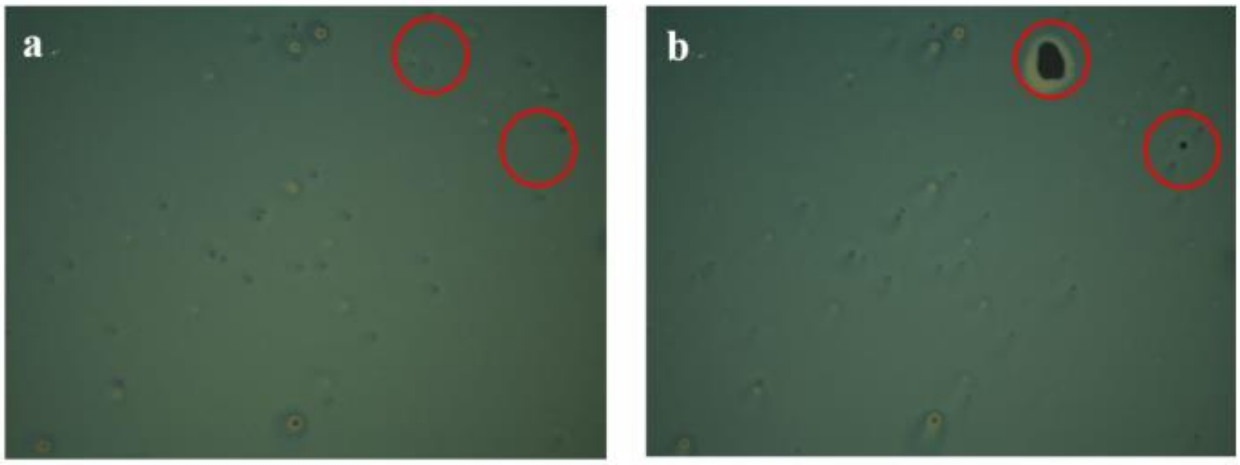
With Patterning, Etchant 10% AcOH



With Patterning, Etchant 2.5% AcOH

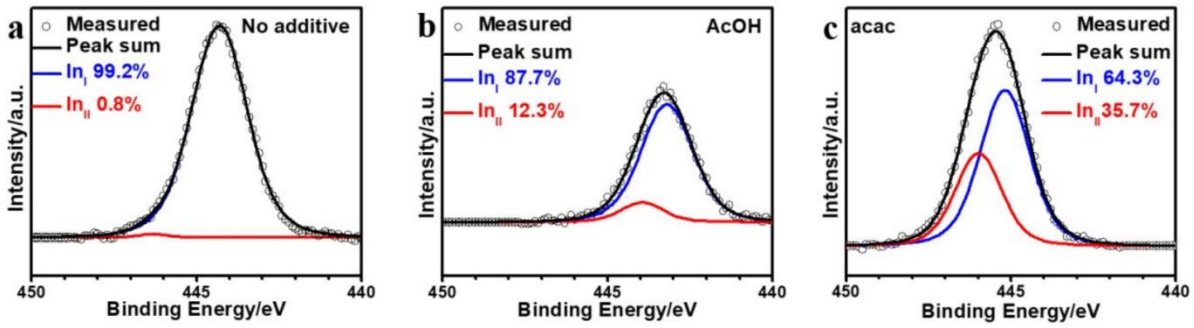


Appendix C-Optical Microscopy on Film evolution before and after spin coating

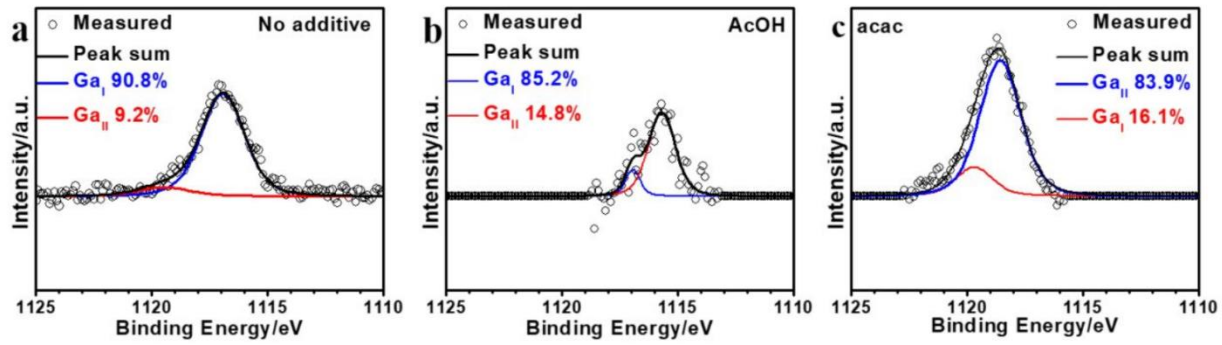


Appendix D-XPS Analysis on In, Ga, Zn environment with different additives

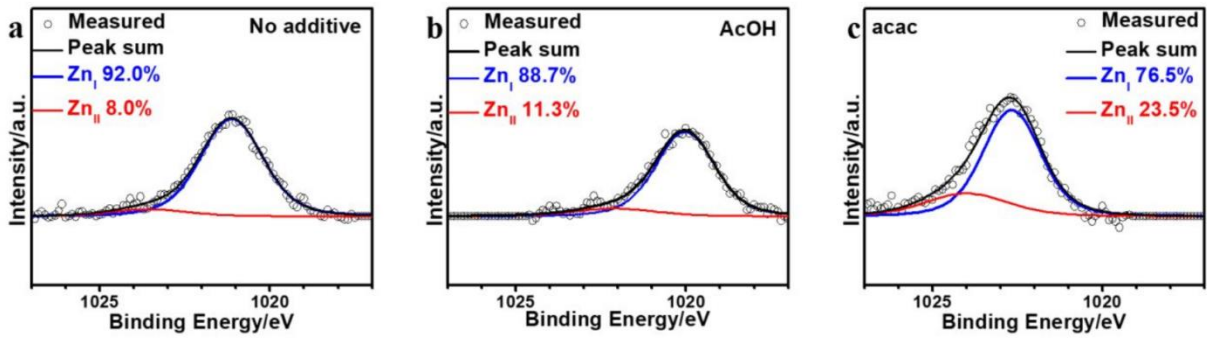
Indium



Gallium



Zinc


a
Measured
Peak sum
Zn$_I$ 92.0%
Zn$_{II}$ 8.0%
No additive
Intensity/a.u.
1025
1020
Binding Energy/eV
b
Measured
Peak sum
Zn$_I$ 88.7%
Zn$_{II}$ 11.3%
AcOH
Intensity/a.u.
1025
1020
Binding Energy/eV
c
acac
Measured
Peak sum
Zn$_I$ 76.5%
Zn$_{II}$ 23.5%
Intensity/a.u.
1025
1020
Binding Energy/eV

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