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High-Performance Wideband Power Amplifiers for 6G and Optical Communications

By

NGUYEN LE KHOI NGUYEN

DISSERTATION

Submitted in partial satisfaction of the requirements for the degree of

DOCTOR OF PHILOSOPHY

in

Electrical and Computer Engineering

in the

OFFICE OF GRADUATE STUDIES

of the

UNIVERSITY OF CALIFORNIA

DAVIS

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2021

High-Performance Wideband Power Amplifiers for 6G and Optical Communications

Abstract

Given how much of our current technology relies on the use of wireless sensors, improving communications technology directly benefits consumer products (smartphones, tablets, mobile devices of all kinds), healthcare (mobile monitoring devices, life-saving implants). Therefore, much higher communication speed, lower latency, and cheaper solutions are highly demanding as the technology is moving to the sixth generation (6G). The frequency band from 70 to 100 GHz and 125 to 160 GHz are currently the main focus band for the next generation of wireless communication.

Different from wireless communication systems, optical communication involves the transfer of information using light rather than radio frequencies (RF). This method of data transportations has many advantages over standard telecommunications methods, such as improved bandwidth, speed, and power. Optical communication devices have applications in data connectivity (such as cloud storage), transportation networks, CATV systems, submarines, and defense technology. Indeed, as communication technology continues to advance, optical networking devices are becoming a much sought-after commodity.

One of the most critical components in wireless communication and optical communication systems is the wideband power amplifiers (PA). Various semiconductor processes have been investigated to support the development of PA for 6G and optical communications systems. By far, Indium Phosphide (InP) and Silicon Germanium (SiGe) process have been proven to be great candidates for the development of the future system thanks to their superior performance in terms of cut-off frequencies. In addition, Indium Phosphide has a significantly higher output power and, therefore, is favorable for high power applications at high frequencies. However, as the operating frequencies emerge into the mm-W region, gain, linearity, and output power degrade rapidly, making the PA highly inefficient and unrealizable.

In this dissertation, several original techniques are proposed and implemented to distributed amplifiers and wideband amplifiers. These techniques are applied to demonstrate high-performance power amplifiers up to 160 GHz, potentially enabling the future realization of 6G and the next generation of optical communications. The original techniques are listed as follows:

1. A new bandpass distributed amplifier (DA) using a wideband gain-boosting technique is introduced. A novel feedback network with a series inductor and a shunt capacitor is employed. The traditional theory has suggested that a series inductor only enhances narrowband gain, and a shunt capacitor decreases upper-frequency capacities. However, the combination of these components can obtain a wideband gain enhancement. The proposed amplifier achieves the record gain boosting over the wide bandwidth ever reported.
2. A wideband linearization technique for distributed amplifiers achieves the highest linearization bandwidth. The technique utilizes an auxiliary transistor that generates distortion components, which are the opposite sign of those generated by the main amplifier. The proposed prototype demonstrates the widest linearization bandwidth.
3. A 160 GHz DA with bandwidth improvement using 3-D interdigital capacitors and a 150 GHz using metal-insulator-metal (MIM) capacitors are designed in an InP process. This work demonstrates for the first time that 3-D interdigital capacitors can be used to improve input matching conditions and bandwidth of a distributed amplifier.
4. A linear wideband differential optical driver amplifier in a SiGe process for the next generation of optical communication systems is demonstrated. This is the first time a triple-stacked hetero junction bipolar transistor (HBT) with an emitter degeneration network is employed for optical drivers.

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PUBLICATIONS

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[1] **N. L. K. Nguyen**, B. T. Nguyen, T. Omonri, D. P. Nguyen, R. Moroney, S. D'Agostino, W. Kennan, and A. Pham, "A Wideband SiGe Power Amplifier Using Modified Triple Stacked-HBT Cell," in *IEEE Microwave and Wireless Components Letters*, vol. 31, no. 1, pp. 52-55, Jan. 2021

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Under Review

[9] **N. L. K. Nguyen**, *et al*., "A 150 GHz, 17.8 dBm and 110 GHz, 24.5 dBm Output Power Distributed Amplifier in InP Process", under review, in *IEEE Transactions on Microwave Theory and Techniques*.

[10] **N. L. K. Nguyen**, *et al*., "A 1 – 220 GHz High Isolation Amplifier in InP Process for 6G Applications", to be submitted, in *IEEE Microwave and Wireless Components Letters*.

[11] **N. L. K. Nguyen**, *et al*., "A DC-75 GHz High Gain InP HBT Distributed Amplifier Using Pseudo Tapered Output Line", to be submitted.

Chapter 1. Introduction of 6G and Optical Communication Applications

1.1 The sixth-generation (6G) and Optical Communications

The need for improved communications is spurred by the increase in mobile traffic as developments in artificial intelligence (AI), and the Internet of Everything (IoE) proliferate. In 2017, global mobile data traffic was at 11.51 exabytes per month. In 2020, it reached 40.77 exabytes per month and is set to be 77.49 exabytes per month by 2022 [1]. Nowadays, the fifth generation (5G) of wireless communication has been introduced to the public with the expectation of greatly improve user experiences. Moreover, 5G communication is unable to accommodate the most leading-edge advances in automation and AI technology.

Given how much of our current technology relies on the use of wireless sensors, improving communications technology directly benefits consumer products (smartphones, tablets, mobile devices of all kinds), healthcare (mobile monitoring devices, life-saving implants), and defense (more powerful radios in ground vehicles, aircraft, and for soldiers). In 2019, the global smartphone market had a value of $714.96 billion USD. Further, the United States is investing heavily in patient monitoring devices (with market size of $4.4 billion USD in 2016, set to reach $6 billion USD by 2023) and defense (current spending is $934 billion USD) [2].

Therefore, much higher communication speed, lower latency, and cheaper solutions are highly demanding as the technology is moving to the sixth generation (6G). The millimeter-wave region is attractive to researchers due to the fact that smaller wavelength such as visible light, which is highly susceptible to the ambient environment, or radiative wavelengths such as X-ray, which are harmful to human and, therefore, infeasible to be used at a wireless communication method [3]. As a result, the frequency band from 70 to 100 GHz and 125 to 160 GHz are the main focus band for the next generation

of wireless communication. In fact, several research groups have demonstrated the feasibility of a wireless communication system at 150 GHz [4].

Different from wireless communication systems, optical communication involves the transfer of information using light rather than radio frequencies (RF). This has many advantages over standard telecommunications methods, such as improved bandwidth, speed, and power. Optical communication devices have applications in data connectivity (such as cloud storage), transportation networks, CATV systems, submarines, and defense technology. Indeed, as communication technology continues to advance, optical networking devices are becoming a much sought-after commodity, commanding $16.9 billion in total market value. Moreover, it is estimated that the United States must invest anywhere from $130-$150 billion in optical fiber communication to keep up with the competition [5].

One of the most critical components in both wireless communication and optical communication systems is the power amplifiers (PA). In a typical transceiver architecture, the PA is the most power-hungry component in the chain. Furthermore, highly advanced systems such as multiple-input-multiple-output (MIMO) require a large number of power amplifiers on the transmitter side. As a result, high-performance PAs over a very wide bandwidth is crucial to the implementation of the systems. Several specifications such as high gain, high linearity, high output power, and high efficiency over a very wide bandwidth are desirable in many applications.

1.2 Distributed Amplifiers

The wideband matching performance of passive matching networks is limited by the Bode-Fano bandwidth limitation and is impractical to achieve a fractional bandwidth near 200% [6]. The Bode-Fano equation does, however, indicate that the bandwidth of an amplifier can be extensively increased if the output capacitance of the amplifier can be reduced. The reduction of the effective input and output capacitance of a gain block is essentially the underlying basis of distributed amplifiers (DAs).

The distributed amplifier, which is also named traveling-wave amplifiers, was originally invented by Ginzton in 1948 [7]. The very first DA was presented in vacuum tube technology in the 1950s, which had the gain of 11dB in a bandwidth of 100Hz-300MHz with a 15W output power [8]. The first monolithic integrated circuit (MMIC) DA was implemented in 1982 by Ayasli in a Gallium Arsenide (GaAs) metal-semiconductor field-effect transistor (MESFET) process [9]. The first MMIC DA was accommodated with a 50Ω input and output system and achieved 9dB gain from 1-13GHz bandwidth. Ever since, the distributed amplifiers have been implemented in various technologies such as complementary metal-oxide-semiconductor (CMOS), Gallium Nitride (GaN), Silicon Germanium (SiGe), and Indium Phosphide (InP), etc. These technologies provide different benefits from bandwidth, power, noise, and production cost.

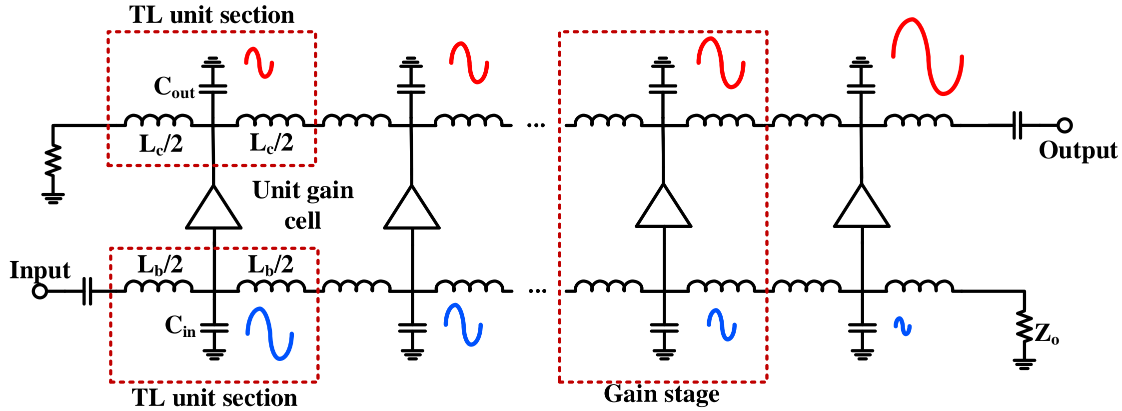

Fig. 1.1 Conceptual presentation of an N-stage DA

Fig 1.1 shows an N-stage conceptual distributed amplifier, where L_b, L_c, C_{in} and C_{out} are the base-line inductor, collector-line inductor, effective input capacitance and effective output capacitance of the gain cell, respectively. The base-line inductors and the effective input capacitance of the gain cell form an input artificial transmission line. The collector-line inductors and the effective output capacitance of the gain cell create an output artificial transmission line. This is the key idea of the distributed amplification. The inductances are chosen in such a way that the characteristic impedance of the lossless input and output artificial transmission lines are equal to Z_0 to achieve a good return loss. The values of L_b and L_c, therefore, can be computed by

$$Z_{0,b} = Z_{0,c} = Z_0 = \sqrt{\frac{L_b}{C_{in}}} = \sqrt{\frac{L_c}{C_{out}}}. \qquad (1.1)$$

Furthermore, the phase synchronization between the input and the output lines should be satisfied to achieve gain flatness over frequency. This relation can be expressed as

$$\tau_b = \tau_c = \sqrt{L_b C_{in}} = \sqrt{(L_c C_{out})} \qquad (1.2)$$

If we assume each of the gain cell contributes an transconductance of g_m, and the load of each gain cell is identical, then the voltage gain of the DA can be derived as

$$A_v = \frac{1}{2} N \cdot g_m \cdot Z_0 \qquad (1.3)$$

where N is the number of stages and Z_0 is the characteristic impedance of the lines. The wave propagates to the input line, gets amplified by the gain cell. The input wave is terminated at the end of the line. At the output, the wave propagates in two directions, namely forward and reverse. The forward direction provides the same phase path for each of the gain cells. Therefore, the signal is added up and propagates to the output. In the reverse direction, the signal is out of phase and is terminated with the characteristic impedance. There is a trade-off between the gain bandwidth of the DA.

1.3 Dissertation Organization

Background motivations, global and the U.S. statistics on communications, concept and basic theory on distributed amplifiers are introduced in Chapter 1.

Chapter 2 presents a novel wideband gain boosting technique for distributed amplifiers. In this chapter, a detailed analysis, design, and characterizations of two DA prototypes in an Indium Phosphide (InP) process are discussed. The proposed technique illustrates the highest gain enhancement over the widest bandwidth from (60 to 145 GHz) ever reported.

Chapter 3 introduces a novel wideband linearization technique for DAs using a feed-forward technique. The chapter covers the analysis, design, and characterization of two prototypes in InP. The proposed technique demonstrates the highest linearization bandwidth (dc to 90 GHz) ever reported.

Chapter 4 focuses on the design and demonstration of high-performance DAs from 1 to 160 GHz in InP. This chapter presents two prototypes with the implementation of double-stacked HBT gain cell and interdigital capacitors for bandwidth enhancement.

Chapter 5 presents the design of a new wideband triple-stacked HBT power amplifier in Silicon Germanium (SiGe). The driver amplifier design is suitable for the next generation of optical communication systems.

Chapter 6 concludes the dissertation with notable remarks.

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Chapter 2. A Wideband Gain Enhancement Technique for Distributed Amplifiers

Wideband, high gain, high output power, and low power consumption are the prominent figures of merit for high data rate communication systems, high-resolution radars, and instrumentation applications [1]. When frequency emerges to the millimeter-wave (mmW) and sub-millimeter-wave regions, maintaining high gain and output power becomes challenging due to increased transmission line losses, unwanted couplings, and parasitic elements [2], [3]. Gain is further degraded when a transistor operates near the transition frequency (f_T) for a given process. Distributed amplifiers (DAs) have been proven to offer ultra-wideband performance but still suffer from gain-bandwidth (GBW) trade-offs [1].

Different techniques have been reported to enhance the DA gain, including cascaded gain stages [3]-[8], cascaded multi- and single-stage [9]-[11], and matrix DAs [12], [13]. However, the results come along with larger chip sizes and higher dc consumption. These techniques also increase the gain in a multiplicative amplification, thereby degrading stability. Cascaded amplifiers also reduce the bandwidth performance depending on the number of cascaded stages and passive losses. Furthermore, mismatches between the stages introduce mid-band ripples and worsen the group delay of the amplifier.

Techniques to enhance the gain-bandwidth product of the DA have also been reported. A widely used technique is to employ peaking inductors at the inter-stage nodes [5], [7], [8], [11], [14]. The gain peaking approach is simple and easy to implement, although the overall gain flatness and stability are sensitive to temperature variations and model accuracy. The coupled drain-line inductors [15], [16], coupled gate-line inductors [15]-[18], and the negative resistance loss compensation have been proposed to extend DA bandwidth [19]-[21]. In addition, several feedback techniques have already been employed in a DA structure to improve performance. The resistive-source-degeneration technique is used in [22]-[24], which provides negative feedback to improve the bandwidth at the expense of the amplifier's gain. A DA with an internal feedback loop introduced in [25] uses an internal path to direct the signal back through the DA for

re-amplification. Another form of feedback is a direct coupling between the input and output line, such as the gate-drain transformer feedback technique [26], [27], or by using capacitive feedback [28]. In [28], a capacitor is connected from the output to the input line to inject power and compensate for the loss from the input line at high frequency. However, direct feedback from output to input could reduce the stability of the circuit. The aforementioned techniques are inherently gain boosting techniques at high frequencies, while the gain at low frequencies remains unchanged.

Besides the conventional low-pass structure, distributed amplifiers can be implemented in a bandpass configuration. The conventional bandpass DA is implemented using bandpass transmission line structures instead of low-pass ones. Several methods have been introduced, such as adding series capacitors on the transmission line [29], or connecting shunt-series LC networks at either or both of the input and output line [28], [30]-[32]. The benefit of using a shunt inductor in a T-section model of a transmission line is to slightly increase the maximum operating frequency. However, the trade-off is the degradation of the lower frequency edge performance, and GBW is significantly reduced. Recently, a bandpass Silicon Germanium (SiGe) distributed amplifier using cascode HBT cells and a supply-scaling technique to achieve high power and efficiency has also been introduced [33].

In this chapter, we present a new bandpass distributed amplifier using an inductive feedback technique to uniformly enhance the gain for the entire passband while maintaining the upper cut-off frequency. The original contributions of our work include:

1) The introduction of a new bandpass topology for DAs that preserves the GBW compared to the conventional low-pass structure.

2) A comprehensive analysis is presented showing how the proposed inductive feedback enhances the DA gain for the entire bandwidth. Notably, the introduction of peaking poles at lower and upper-frequency edges of the bandpass amplifier.

3) The designed DA achieves the highest reported gain boosting over a very wide bandwidth.

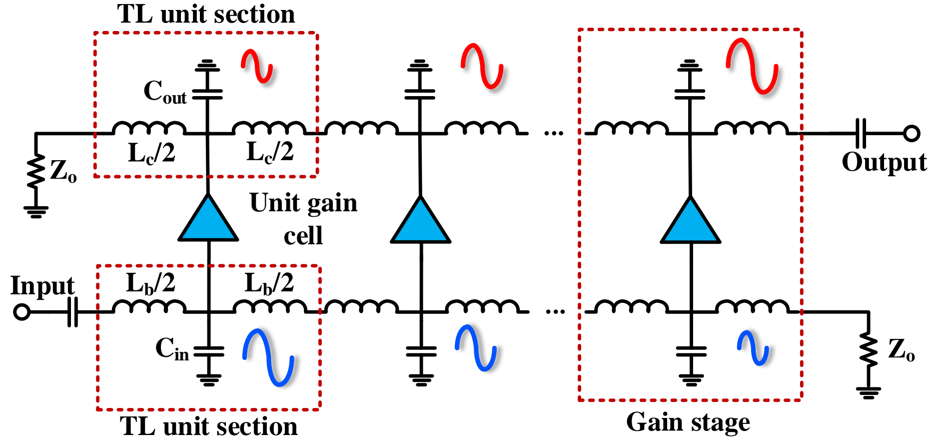


Fig. 2.1. Conceptual presentation of an N-stage low-pass DA.

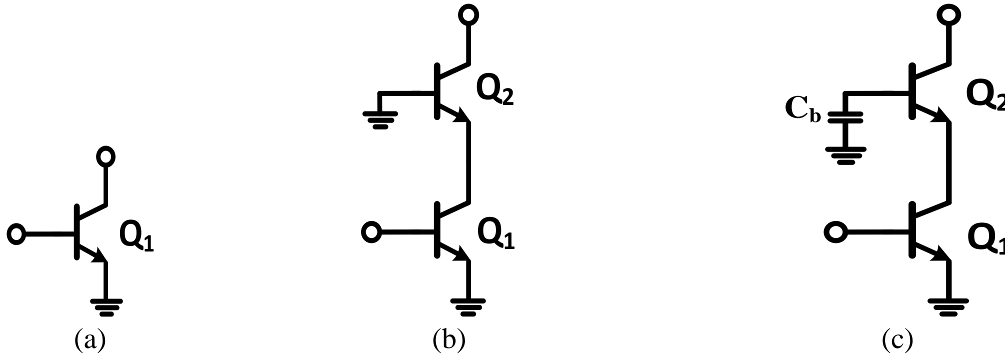


Fig. 2.2. Typical unit gain cells using HBTs: (a) common emitter, (b) cascode topology, (c) stacked-HBTs with a base capacitor C_b.

To validate the proposed technique, a 60 – 145 GHz bandpass DA is designed and fabricated in an Indium Phosphide (InP) Heterojunction Bipolar Transistor (HBT) process. The prototype exhibits a measured average small-signal gain of 10.5 dB, a 3-dB bandwidth from 60 – 145 GHz, and a maximum saturation power (P_{sat}) of 20.9 dBm with the corresponding 1 dB compression power (P_{1dB}) of 18.5 dBm at 75 GHz. The feedback DA has a 4-dB gain improvement spanning from 64 to 142 GHz compared to its counterpart conventional DA.

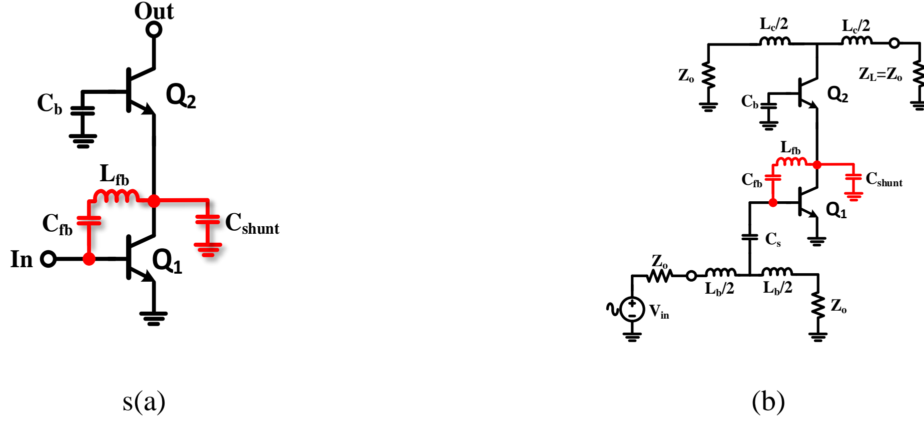
2.1 The Proposed Feedback Gain Cell

Fig. 2.1 shows a conceptual N-stage distributed amplifier, where L_b, L_c, C_{in}, and C_{out} are the base-line inductor, collector-line inductor, and effective input and output capacitances of an ideal gain cell,

respectively. Fig. 2.2 illustrates common implementations of the unit gain cell of Fig. 2.1 using HBT devices, including a common emitter transistor, a cascode structure, and double-stacked HBTs. Compared to a single common emitter device, a cascode and double-stacked HBTs can provide a lower output conductance. This low output conductance of the cascode/stacked structure minimizes the loss of the output artificial transmission line [34]-[36]. The base capacitor C_b in Fig. 2.2(c) provides a finite impedance that allows for a small voltage swing at the base of the transistor Q_2. Hence, the voltage swing between the collector and the emitter of Q_2 is reduced at high frequencies and is below the breakdown voltage [24], [37], [38].

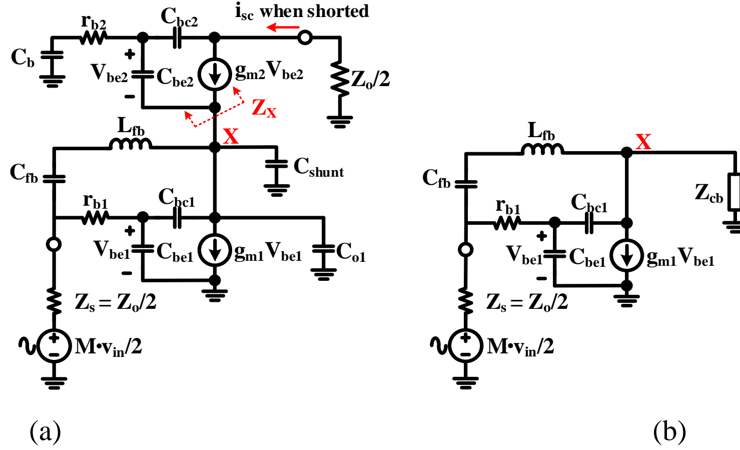
We propose a wideband gain enhancement technique for a DA, which provides a high roll-off bandpass structure by using an inductive feedback network applied to Fig. 2.2(c), as shown in Fig. 2.3(a). The proposed technique introduces a feedback inductor L_{fb} and a shunt capacitor C_{shunt} at the collector of the common emitter transistor in the stacked-HBT gain cell configuration. The feedback inductor L_{fb} introduces gain peaking at the low-frequency edge while the shunt capacitor C_{shunt} boosts up the gain at the high-frequency edge. The feedback capacitance C_{fb} acts as a dc block from the collector to the base of transistor Q_1 to prevent shorting out the HBT.

Fig. 2.3(b) shows a single-stage DA employing the proposed gain cell in Fig. 3(a) in addition to a commonly used series input capacitor C_s to obtain a high bandwidth. In general, the feedback network has an insignificant impact on the overall input capacitance of the gain cell for most of the passband. The input capacitance of the feedback gain cell is then approximately equal to C_{be1}. The coupling capacitor C_s factors the gain of the DA by the capacitive division ratio, M, defined as $M = C_s/(C_s + C_{be1})$ [39]. In order to maximize the bandwidth, the ratio M can be much smaller than one. Although stacked-FETs have been scrutinized and reported [37], [38], [40], a DA using inductive feedback stacked-HBTs has not been examined before. By constructing a Thevenin equivalent at the input, the input voltage source is factored by $M/2$. The output network is simplified into $Z_0/2$. The schematic in Fig. 2.3(b) can be presented by a small-signal circuit in Fig. 4(a). The voltage gain of the single-stage DA can be calculated as



s(a) (b)

Fig. 2.3. (a) The proposed bandpass inductive feedback gain cell, and (b) a single-stage DA using the proposed gain cell.



(a) (b)

Fig. 2.4. (a) Simplified small-signal model of the single-stage DA for gain calculation (dc bias is omitted for simplicity) and (b) simplified the load at node X of the transistor Q1.

$$A_{stage,fb} = |G_{M,eff} \cdot \frac{Z_0}{2}| \tag{2.1}$$

where $G_{M,eff}$ and Z_0 are the effective transconductance and the characteristic impedance of the transmission lines, respectively. The effective transconductance, $G_{M,eff}$, can be derived when the output is shorted and the short-circuit output current, i_{sc}, is calculated, as illustrated in Fig. 2.4(a). The effective transconductance $G_{M,eff}$ is then

$$G_{M,eff} = \frac{i_{sc}}{Mv_{in}/2} = \frac{i_{sc}}{v_X} \cdot \frac{v_X}{Mv_{in}/2} = G_{M2} \cdot A_{v1,fb} \tag{2.2}$$

where G_{M2} is the transconductance of transistor Q_2, and $A_{v1,fb}$ is the gain of the common emitter transistor Q_1 with the feedback network. The transconductance G_{M2} is given by

$$G_{M2} = \frac{g_{m2}C_b + sC_{bc2}(C_{be2} + g_{m2}r_{b2}C_b)}{(C_b + C_{be2}) + sC_{be2}C_b r_{b2}} \tag{2.3}$$

with s as the complex frequency variable in Laplace transform. Assuming that C_{fb} is an ideal dc block ($C_{fb} = \infty\ fF$), the gain $A_{v1,fb}$ can be deduced in (2.4) at the bottom of the page, where Z_x is the impedance looking into the emitter terminal of transistor Q_2, as shown in Fig. 2.4(a). Z_{cb} is the equivalent load seen by common emitter transistor Q_1 at node X. In other words, Z_{cb} is equivalent to Z_x in parallel with C_{o1} and C_{shunt} as shown in Fig. 2.4(b). The impedances Z_x and Z_{cb} are frequency-dependent and given by

$$Z_x \approx \frac{(C_b + C_{be2}) + s \cdot r_{b2}C_b C_{be2}}{(g_{m2} + sC_{be2})(C_b + s \cdot r_{b2}C_b C_{bc2})} \tag{2.5}$$

$$Z_{cb} = Z_x || \frac{1}{s(C_{o1} + C_{shunt})}. \tag{2.6}$$

Although the impedance Z_x and Z_{cb} vary with frequency; they are not a strong function of frequency. The poles and zeroes in (2.5) and (2.6) locate at very high frequencies and, therefore, are non-dominant factors.

From (2.1)-(2.6), the simplified voltage gain of a DA stage employing the proposed feedback topology is given by (2.7), neglecting the higher-order products of the capacitances. Note that the coefficient M is valid for most of the passband. By letting $L_{fb} \to \infty$ and $C_{shunt} \to 0$, the voltage gain of a conventional double-stacked HBT single-stage DA is shown in (2.8). The significant differences between the proposed feedback technique in (2.7) and the conventional structure in (2.8) can be observed as follows:

1. Since $L_{fb}C_{bc1}$ is much smaller than $g_{m1}L_{fb}$, the dominant zero in (2.7) of the proposed feedback DA is now introduced at $-1/(g_{m1}L_{fb})$, which indicates a bandpass structure. Likewise, the zero of the conventional DA is at g_{m1}/C_{bc1} in (2.8). Clearly, inductor L_{fb} neutralizes feedback capacitor C_{bc1} in the proposed design.

2. The lower frequency pole of the conventional DA at $-1/(C_{be1}Z_s)$ in (2.8) moves up and interacts with the feedback inductor L_{fb} forming a dominant conjugate pole pair, which results in gain peaking at the lower bandpass frequency edge.

3. The high-frequency pole at $-1/((C_{bc1}+C_{o1})Z_x)$ in (2.8) is shifted to a lower frequency by C_{shunt}, which also interacts with L_{fb} and the inductive interconnection line between the two transistors. This coupling effect leads to gain improvement at high frequency.

As a result, the proposed feedback technique provides a bandpass characteristic with a gain enhancement for the entire passband. In the following subsections, the bandpass cut-off frequencies are derived and validated. In addition, (2.7) and (2.8) are verified with simulations.

2.2 Bandpass Cut-off Frequencies and Transmission Zero

The lower cut-off frequency of the feedback structure is determined by the peaking frequency between feedback inductor L_{fb} and input capacitance C_{be1} of transistor Q_1, as described in point 2 in the previous subsection. The exact peaking frequency is complicated to quantify because of various coupling

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$$A_{v1,fb} \approx \frac{M\cdot\left(-s^2L_{fb}C_{bc1}+g_{m1}L_{fb}s+1\right)\cdot Z_x}{2\left(s^2C_{be1}L_{fb}Z_s+s\left(L_{fb}+C_{be1}Z_sr_{b1}+C_{be1}Z_sZ_{cb}\right)+Z_s\right)\left(1+s(C_{o1}+C_{bc1}+C_{shunt})Z_x\right)} \tag{2.4}$$

$$A_{stage,fb} \approx \frac{M\cdot[g_{m2}C_b+sC_{bc2}(C_{be2}+g_{m2}r_{b2}C_b)](\boldsymbol{-s^2L_{fb}C_{bc1}+g_{m1}L_{fb}s+1})}{2(g_{m2}+sC_{be2})(C_b+sr_{b2}C_bC_{bc2})\left(\boldsymbol{s^2C_{be1}L_{fb}Z_s+s\left(L_{fb}+C_{be1}Z_sr_{b1}+C_{be1}Z_sZ_{cb}\right)+Z_s}\right)(\boldsymbol{1+s(C_{o1}+C_{bc1}+C_{shunt}}} \cdot\frac{Z_o}{2} \tag{2.7}$$

$$A_{stage,conv} = \frac{M\cdot[g_{m2}C_b+sC_{bc2}(C_{be2}+g_{m2}r_{b2}C_b)](g_{m1}-sC_{bc1})}{2(g_{m2}+sC_{be2})(C_b+sr_{b2}C_bC_{bc2})(1+sC_{be1}Z_s)(1+s(C_{bc1}+C_{o1})Z_x)}\cdot\frac{Z_o}{2} \tag{2.8}$$

factors. However, an elegant expression of the low frequency, f_{low}, at which the peaking occurs, can be derived from the Miller theorem for L_{fb} as

$$f_{low} = \frac{1}{2\pi\sqrt{\frac{L_{fb}}{1+|A_{v1}|}C_{be1}}} \quad (2.9)$$

where A_{v1} is the low-frequency voltage gain from the base to the collector of transistor Q_1 without the feedback inductor. The peaking magnitude depends on the damping term $\left(L_{fb} + C_{be1}Z_s r_{b1} + C_{be1}Z_s Z_{cb}\right)$ in (2.7), as well as the resistive loss of L_{fb}. The upper cut-off frequency, f_{high}, is limited by the process capability. The proposed inductive feedback technique also improves the gain at the high frequency of the passband.

The gain peaking mechanism at the upper band is similar to the peaking inductor technique [5], [7], [8], [11], [18], [24]. If C_{shunt} is too big, the pole described in point 3 above will become dominant, thereby reducing the upper cut-off frequency. The values of C_b and C_{shunt} will determine the impedance looking into the base of the transistor Q_2. Therefore, the two design parameters need to be chosen carefully from (7) and verified by simulations to ensure both gain enhancement and unconditional stability. Furthermore, C_{shunt} shifts the pole in (7) to lower frequency and, at the same time, interacts with the feedback inductor, which might cause degradation in the stability of the feedback DA compared to the conventional DA. A transmission zero can be achieved at the series resonant frequency of C_{fb} and L_{fb}.

Fig. 2.5 shows the normalized gain of single-stage DA from (2.7) and (2.8) with different values of L_{fb} and C_{shunt}, in which α and β are normalized feedback parameters. The parameter α is defined as the ratio of L_{fb} in pH over C_{be1} in fF or $\alpha = L_{fb}/C_{be1}$. The dimensionless parameter β *is* the capacitance ratio, $\beta = C_{shunt}/C_{o1}$. The calculation is based on the extracted small-signal parameters from the InP transistor model. The ideal calculated analytical results do not consider the resistive losses of the DA transmission lines, and losses contributed by the devices, nor losses from the feedback inductor itself.

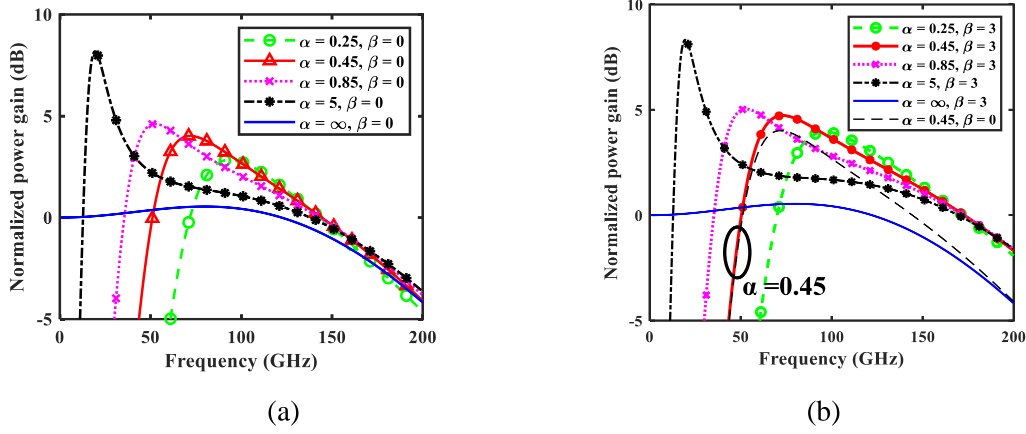
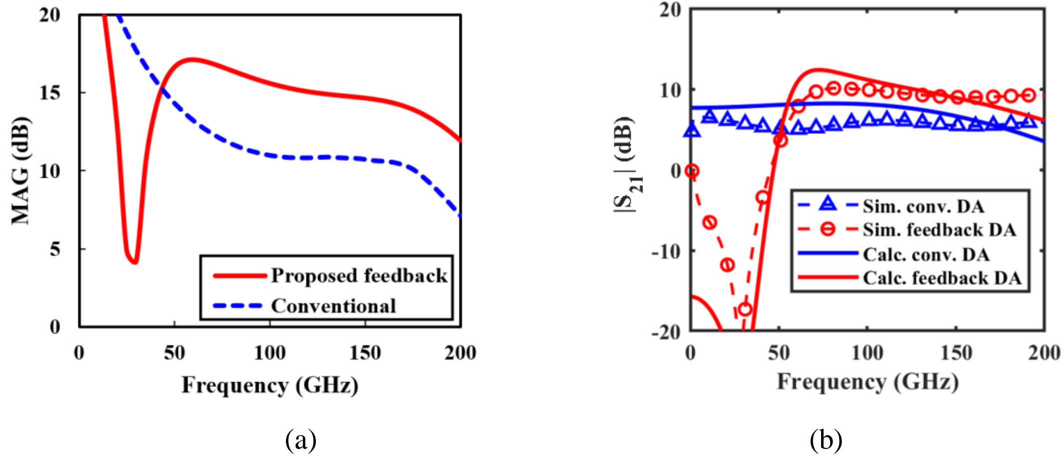


Fig. 2.5. Normalized voltage gain using analytical equation calculations (7), (8): (a) varying α with $\beta = 0, and$ (b) varying α with $\beta = 3$, where $\alpha = L_{fb}/C_{be1}$ and $\beta = C_{shunt}/C_{o1}$.

Fig. 2.5(a) shows the behavior of the gain under the effect of L_{fb} alone, that is $\alpha > 0$ and $\beta = 0$. The conventional low-pass topology can be modeled by $\alpha = \infty$ *and* $\beta = 0$. The smaller the inductance, the lower gain enhancement there would be since the inductor behaves as a low impedance circuit. By adding both the feedback inductor L_{fb} and the shunt capacitor C_{shunt}, the gain of the DA can be improved over the entire passband, as shown in Fig. 2.5(b). An overlay of $\alpha = 0.45$ and $\beta = 0$ is shown in Fig. 2.5(b) to highlight the effect of L_{fb} and C_{shunt} to the DA's gain.

The value of C_{shunt} should be large enough to achieve uniform gain enhancement while maintaining the maximum operating frequency. From Fig. 2.5(a), it demonstrates that high peaking can be achieved with large α or L_{fb}. However, to maintain the gain flatness over the bandwidth, larger α or L_{fb} requires increasing C_{shunt} or β. At the same time, large C_{shunt} or β will decrease the higher cut-off frequency of the DA. Therefore, optimal α and β can be chosen to maximize the bandwidth while simultaneously obtaining gain flatness.



(a) (b)

Fig. 2.6. (a) Simulation of the maximum available gain of a unit gain cell and (b) simulation and analytical solutions (7), (8) of S_{21} of a six-stage DA with and without feedback. The feedback network is L_{fb}= 140 pH, C_{shunt}= 20 fF, and C_{fb} = 0.2 pF.

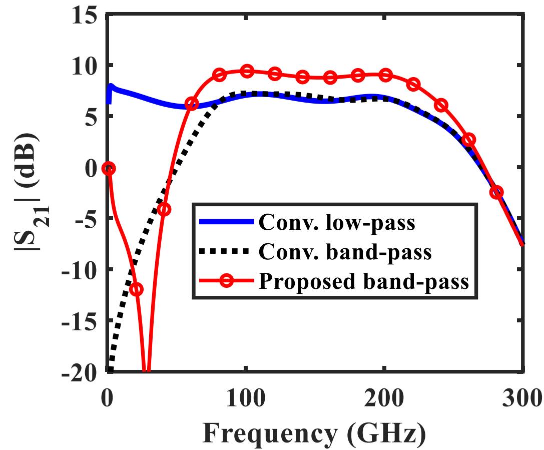
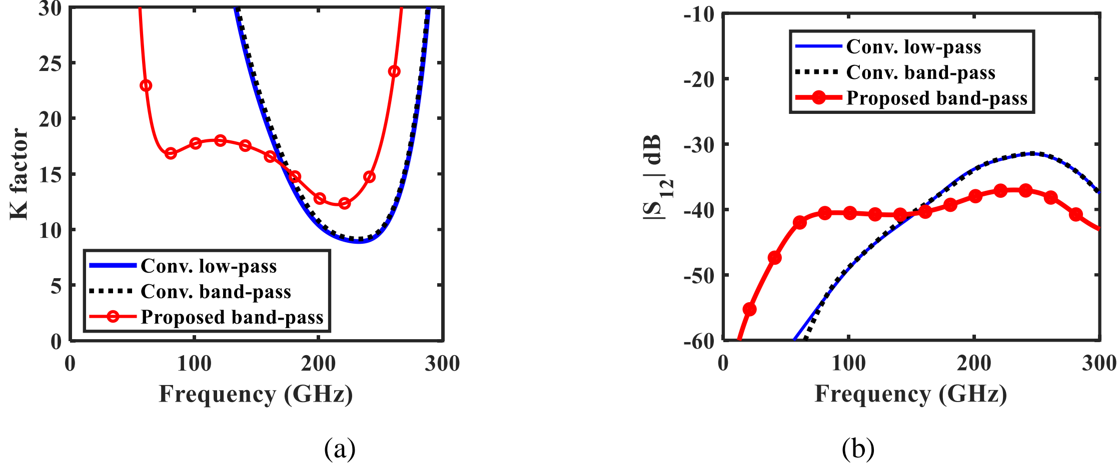


Fig. 2.7. S_{21} simulation of three six-stage DAs in a conventional low-pass, conventional bandpass with shunt inductors at input and output line, and the proposed bandpass structure.

2.3 The DA with the Proposed Feedback Technique

By neglecting all the losses due to the input and output transmission lines, the ideal total voltage gain of an N-stage DA exploiting the proposed technique can be calculated by factoring N into (2.7). Fig. 2.6(a) illustrates the simulated maximum available gain (MAG) of a unit gain cell with and without the feedback network. Uniform gain enhancement of approximately 5 dB can be observed in our design frequency band from 60 to 150 GHz. Fig. 2.6(b) compares the calculated power gain based on (2.7) and (2.8) in a 50 Ω system and the simulated S_{21} using the actual transistor model and lumped components of a six-stage DA ($N = 6$) with and without the proposed feedback technique.

The series input capacitor to the gain stage, C_s, is chosen to be 20 fF. Inductances L_b and L_c provide the characteristic impedance and phase synchronization. The feedback capacitor, C_{fb}, is valued at 0.2 pF. The value of L_{fb} =140 pH is calculated using (9) to peak at 70 GHz as the lower edge of W-band, and the value of C_{shunt} = 20 fF is chosen to achieve a flat gain response without sacrificing the upper cut-off frequency. A good agreement is obtained between the simulation and the analytical solution as described by (2.7) and (2.8) as shown in Fig. 2.6(b). The difference in magnitude is due to the uncaptured losses from multiple stages and devices.

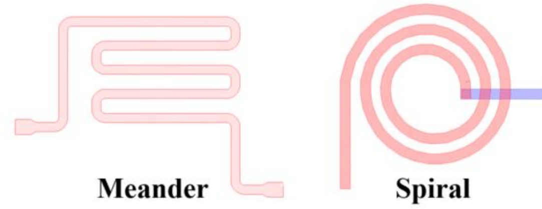


(a) (b)

Fig. 2.8. (a) Stability factor, and (b) reverse isolation S_{12} of the six-stage conventional low-pass, conventional bandpass, and the proposed feedback DA.

Fig. 2.7 shows the S_{21} simulations of the conventional low-pass DA, conventional bandpass DA with shunt inductors at the input and output, and the proposed six-stage DA using the gain cell in Fig. 2.3. The simulations indicate that the feedback DA provides gain improvement for the entire passband. Previously in section 2.1, C_{fb} is assumed to be infinite and acts as a dc block. However, in practice, the value of C_{fb} can determine a transmission zero at the resonant frequency between C_{fb} and L_{fb}, as shown in Fig. 2.7. The presence of a zero will increase the roll-off of S_{21} at the low-frequency edge. In addition, C_{fb} will affect the peaking frequency and magnitude.

Fig. 2.8(a) shows the simulation of the stability factor of the conventional low-pass, conventional bandpass, and the feedback bandpass DAs. The proposed feedback technique introduces a negative feedback path, which is a stabilizer for the DA at high frequency compared to its counterparts. Fig. 2.8(b) presents the simulated reverse isolation S_{12} of the three amplifiers. As predicted, the reverse isolation of the feedback DA shows improvements compared to the conventional designs. The conventional low-pass and bandpass structures share similarities in Fig. 2.8(a) and (b) since the active components are identical, and the input/output transmission line remains the same characteristic impedance.



	Meander line	Spiral coil
Area (μm^2)	3876	2856
SRF (GHz)	180	145

Fig. 2.9. Comparison between a meander line and a spiral inductor for the inductance of 150 pH.

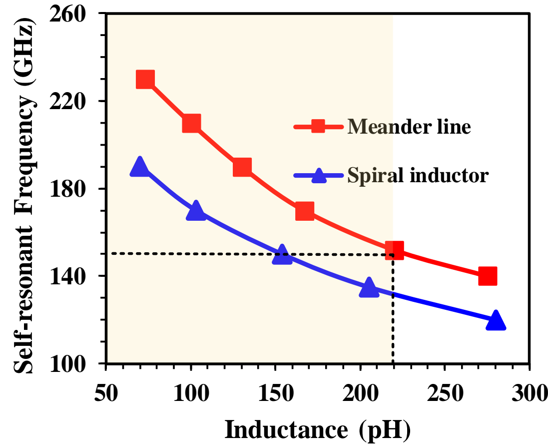


Fig. 2.10. Simulated self-resonant frequency of the meander line and the spiral inductor with respect to the inductance.

2.4 Circuit design and implementation

2.4.1 The Inductive Feedback Network

In this subsection, we present the study and design of the feedback network to maximize the peaking amplitude while preserving the upper cut-off frequency. In particular, the feedback inductor is realized with a meander transmission line for a high self-resonant frequency (SRF) given layout constraints. The shunt capacitor, C_{shunt}, is absorbed into the feedback inductor parasitic, avoiding an additional Metal-Insulator-Metal (MIM) capacitor. The inductors are simulated in an InP process using the Keysight Advanced Design System (ADS) Momentum Electromagnetic (EM) full-wave simulator. Test structures and customized calibration kits are fabricated to compare with the simulated results. The EM simulation

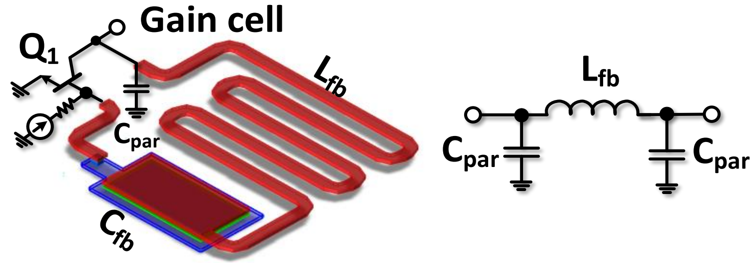
setups, including port excitation configurations, meshing, and convergence conditions, are validated with the measurement of different test structures.

Fig. 2.9 shows the comparison of two typical implementations of an inductor using a meander transmission line and a spiral coil for the same inductance of 150 pH. The most important aspect of the feedback inductor for this extremely wideband application is the self-resonant frequency (SRF). If this frequency falls within the band of interest, the benefits of the feedback network will be eradicated. Fig. 2.10 shows the simulated SRF with respect to the inductance of the meander line inductor and the spiral inductor. The higher self-resonant frequency in a broad range of inductance makes the meander line inductor more suitable for our wideband implementations.

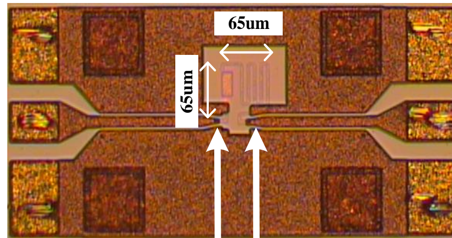
In this application, the passband extends up to 150 GHz; hence, according to Fig. 2.10 in the shaded area, the maximum allowable inductance from the meander line is approximately 220 pH. This range allows some flexibility in designing the feedback inductor. To achieve gain boosting at 70 GHz, the calculated inductance using (2.9) gives a value of 100 pH with $C_{fb} = \infty$ fF. However, due to the size limitation and layout consideration, the feedback capacitor C_{fb} is selected to be 200 fF, which requires the inductance to be adjusted to 140 pH to achieve the same peaking frequency. The transmission zero is predicted by the resonant frequency of L_{fb} and C_{fb} at 30 GHz.

The shunt capacitance, C_{shunt}, is found to be approximately 20 fF to achieve a flat gain while maintaining the required upper frequency. This small capacitance can be absorbed to the feedback inductor's parasitic capacitance C_{par} in the π-model, as shown in Fig. 2.11(a). Fig. 2.11(b) illustrates the fabricated test structure of the feedback inductor-capacitor network with two Ground-Signal-Ground (GSG) probe pads and 50 Ω feed lines for characterization. The calculated and extracted parameters from the measurement at 70 GHz are shown in Fig. 2.11(b). Since the layout of the feedback inductor is compact, the proposed technique is useful to improve the amplifier gain performance.

2.4.2 The Band-pass Gain Enhanced Distributed Amplifier



(a)



Parameters	Calculated	Measurement
L_{fb}	$140pH$	$190pH$
C_{fb}	$200fF$	$272fF$
C_{shunt}	$20fF$	$24fF$

(b)

Fig. 2.11. (a) Feedback network layout and inductor pi-model and (b) inductor-capacitor feedback network test structure and extracted data compared to theoretical calculations.

To verify the concept, two distributed amplifiers are designed and fabricated in an InP HBT process [14], [24], [41], [42]. This process offers a transition frequency f_T of 290 GHz and a maximum frequency f_{max} of 390 GHz. The first prototype is the conventional DA with the coupling ratio optimized to achieve the maximum bandwidth while maintaining good input and output matching conditions. The second prototype is the first prototype with the proposed inductive feedback network added. The complete schematic diagram of the feedback DA is shown in Fig. 2.12. Both DAs employ nine stages to meet the gain requirement. Based on our simulations, adding more stages after the 9th gain cell does not provide gain enhancement due to losses of the artificial transmission lines.

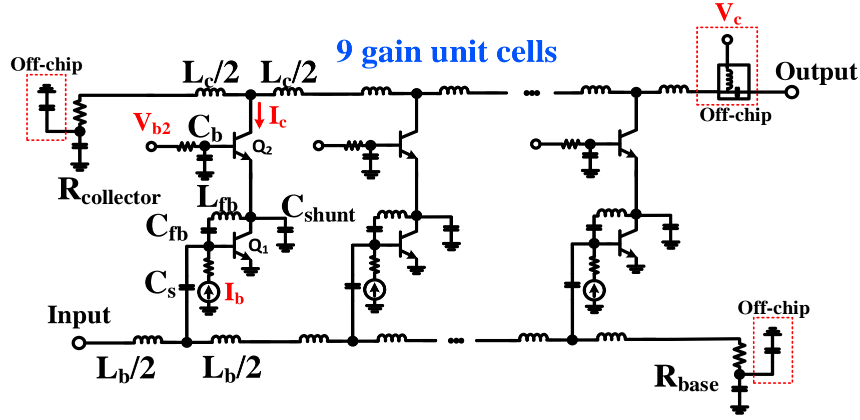
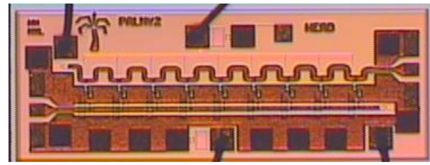
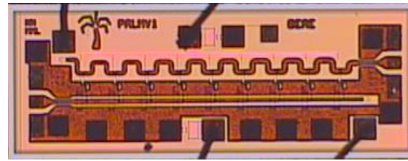


Fig. 2.12. Complete schematic diagram of the nine-stage feedback DA.



(a)



(b)

Fig. 2.13. Chip photograph of (a) proposed inductive feedback bandpass DA and (b) conventional low-pass DA. Both chips have a size of 1.6 mm x 0.6 mm.

Each gain unit cell employs a stacked-HBT configuration in which both the common-emitter transistor and the common-base transistor have 10-μm emitter length. The stacked-HBT structure not only increases the voltage swing but also helps reduce the input parasitic capacitance due to the Miller effect [37] and the output conductance of the gain cell to minimize the loss of the output line [34]-[36]. Therefore, the DA can achieve higher output power and gain-bandwidth product as compared to the conventional single common emitter transistor topology. Fig. 2.13 presents the chip photos of the fabricated prototypes. Both amplifiers have a chip size of 1.6×0.6 mm^2, including all pads. The bases of the two transistors are

Table 2.1. Design Parameters of The Proposed Feedback DA

Design parameters		Feedback DA
Gain unit cell	**Topology**	Feedback stacked-HBT
	C_b	128 fF
Emitter length	L_e	10 µm (both Q_1 and Q_2)
Bias conditions	I_b	250 µA
	V_c	4 V
	V_{b2}	1.8 V
	I_c	12.3 mA
Input series capacitor	C_s	20 fF
Inductances	L_b	38 pH
	L_c	77 pH
Terminations	R_{base}	65 Ω
	$R_{collector}$	55 Ω
Feedback network	L_{fb}	190 pH
	C_{fb}	272 fF
	C_{shunt}	24 fF

biased through a 1 kΩ resistor. The circuit operates at 4 V collector supply, V_c, and 12.3 mA collector current, I_c, each cell at the small signal condition. The common emitter device, Q_1, is biased in class A with a base current of I_b= 250 µA per gain cell.

The feedback network is carefully designed, as described in the previous subsection. The interconnection length between the two devices is minimized to reduce any peaking effects other than those from our proposed network. Collector inductors, L_c, are realized using microstrip lines. The base inductors, L_b, are implemented using a coplanar waveguide structure to reduce losses and create a better grounding for the devices. All the passive components are fully simulated using the Keysight ADS Momentum.

In our proposed design, the input and output planar transmission lines are tapered to improve output power and efficiency. In particular, the width of the output microstrip line is 10 µm at the first stage and gradually increases to 17 µm at the output port. The input coplanar waveguide width decreases from 15 µm at the input port to 8 µm toward the termination. Thanks to a low-loss dielectric substrate offered by InP processes [43], [44], the simulated conductor loss of the proposed output microstrip line is about 0.15 dB/mm at 110 GHz. Not only the low output conductance provided by the InP HBT device [45] and the feedback stacked-HBT configuration, but the low conductor loss of the InP microstrip lines also contribute to the low loss per stage of the output artificial transmission lines [36].

Our simulated loss per distributed gain stage of the output transmission line is approximately 0.07 dB/stage at 110 GHz. The low loss per stage of the output line allows for the power from each stage to arrive at the load with minimal attenuations. Furthermore, the tapered output line maximizes the output signal traveling toward the output load, therefore, increases the output power. Compared to an identical DA with a uniform output microstrip line, the simulated output power using the proposed tapered line increases by 17 %.

Based on the output line loss per stage and the tapered line discussed above [36], the total output power can be estimated by superposing the power arrives at the load contributed by each stage after subtracting the loss on the signal path. The calculated output power for the proposed DA is approximately 98.8 mW at 110 GHz. With a dissipated power of 442 mW, the power added efficiency is in the order of 17.8 %. Overall, the low output conductance HBT device, the stacked-HBT configuration with the feedback network, the low-loss microstrip line, and the tapered output transmission lines help the proposed DA achieving high power and efficiency while maintaining good input and output matching conditions.

In our proposed design, the values of the two termination resistors are determined as 55 Ω and 65 Ω for the collector line and the base line, respectively. The termination networks, which include the resistors $R_{collector}$ and R_{base} in series with a small capacitor, are designed on-chip to achieve good input and output return losses, as well as a flat gain response over a wide frequency range up to 180 GHz. Each network is bond-wired to a 700 pF off-chip shunt bypass capacitor to eliminate any low-frequency signals. The collector of the DA is biased through an external bias-tee. Both input and output are connected to 100 µm pitch GSG probe pads. The design parameters of the feedback DA are listed in Table 2.1. The conventional DA has an identical set of parameters with the feedback network in Fig. 2.11(a) removed for comparison.

2.5 Measurement results

2.5.1 Small-signal Measurements

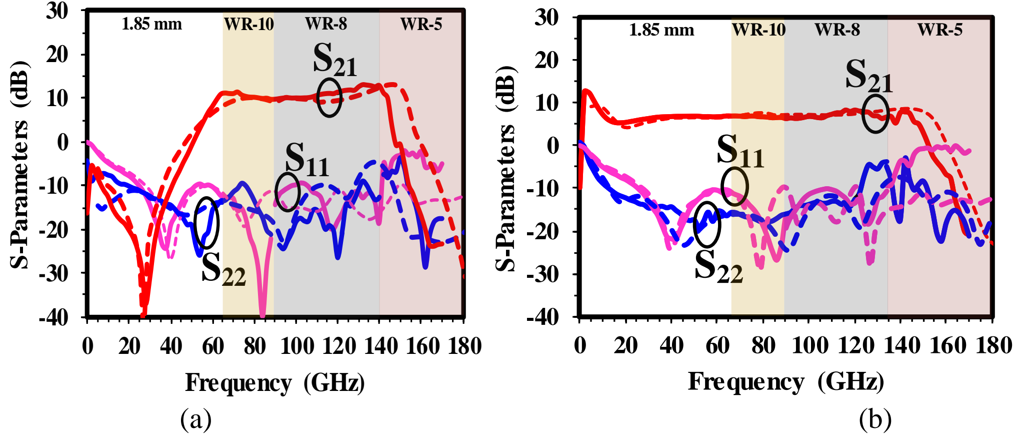


Fig. 2.14. Measured (solid) and simulated (dashed) S-parameters of (a) the proposed feedback DA and (b) the conventional low-pass DA.

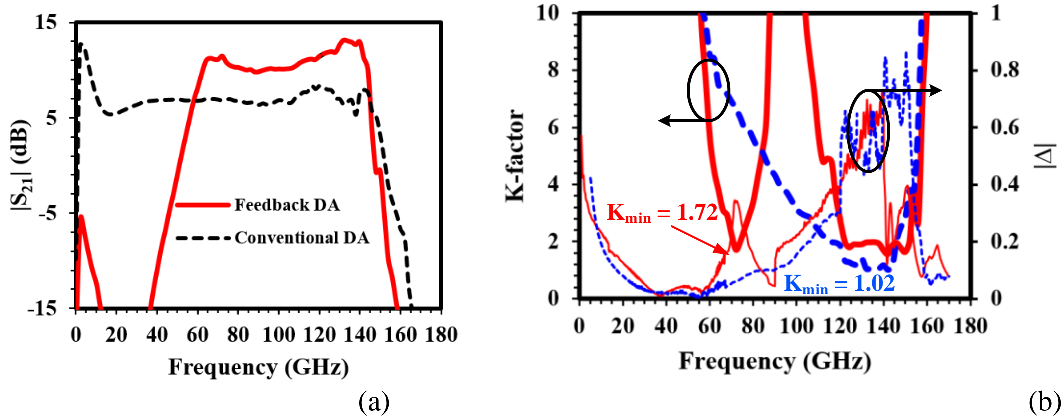


Fig. 2.15. Comparison between feedback DA and conventional DA for (a) measured gain, S_{21}, and (b) measured stability factors k and $|\Delta|$. The solid red line is the proposed feedback DA, and the dashed blue line is the conventional DA.

Fig. 2.14(a) and 2.14(b) present the frequency response of the proposed feedback and the conventional DA, respectively. The dashed and solid lines are simulated and measured results, respectively. The small-signal measurements are conducted in different frequency bands: 0 – 67 GHz (1.85 mm coaxial cable), 67 – 90 GHz (WR-10 waveguide), 90 – 140 GHz (WR-8 waveguide), and 140 – 170 GHz (WR-5

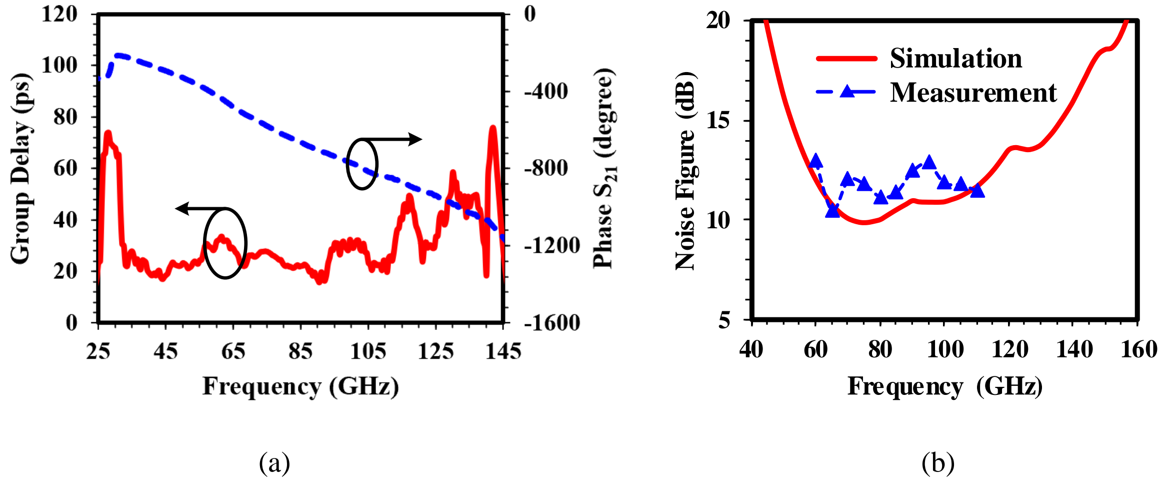


Fig. 2.16. (a) Measured group delay (ps) and relative phase (degree) of S_{21}, and (b) noise figure of the feedback DA.

waveguide) using the PNA-X network analyzer and appropriate frequency extenders. The gain discontinuities are less than 0.7 dB at 90 GHz and 1 dB at 140 GHz for both DAs.

The proposed gain boosting feedback DA exhibits an average gain of 10.5 dB with a positive gain slope. The 3-dB bandwidth extends from 60 GHz up to 145 GHz, making the gain-bandwidth product of 285 GHz. The DA achieves input and output return loss better than -10 dB up to 110 GHz. The transmission zero appears at 27 GHz. The conventional DA demonstrates a 6.5 dB average gain with a 3-dB bandwidth from 15 to 148 GHz. The input and output return loss maintain below -10 dB up to 120 GHz. The measurements correlate well with the simulated results for both DAs. Due to the large device size and a wide bandwidth close to f_T, our conventional DA has lower gain. Therefore, the feedback network is developed to enhance the gain while still achieving high output power and high-frequency operation.

Fig. 2.15(a) illustrates the measured gain S_{21} of the feedback DA and the conventional low-pass DA. An average gain improvement of 4 dB is achieved in the feedback DA compared to the conventional DA from 64 to 142 GHz. Both distributed amplifiers consume 440 mW. Fig. 2.15(b) exhibits the measured stability factors k and $|\Delta|$ of the DAs up to 180 GHz. Both DAs fulfill the Rollet proviso and exhibit $k > 1$ and $|\Delta| < 1$ at all frequencies. Therefore, both DAs are unconditionally stable. It is noteworthy that the k-

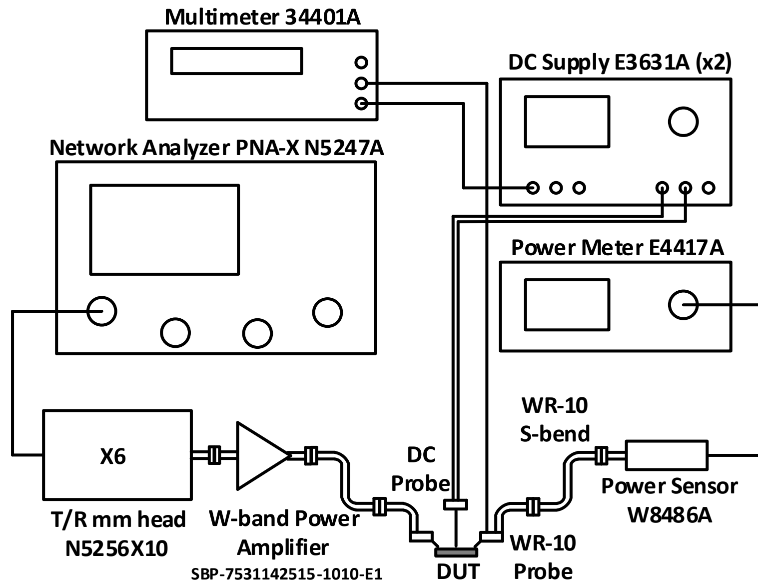


Fig. 2.17. W-band power measurement test setup.

factor of the feedback DA is larger than that of the conventional DA at above 80 GHz. Fig. 2.16(a) depicts the measured group delay in pico-second (ps) and the relative phase of S_{21} (degree) of the feedback DA. The proposed feedback DA achieves a linear phase with respect to frequency up to 145 GHz with a maximum deviation of $\pm$ 20 ps within the passband.

The noise measurement is performed at V-band (60 – 70 GHz) and W-band (75 – 110 GHz) by adapting the direct method [28]. The device under test (DUT) is terminated at the input. The output noise contributed by the DUT is observed using a spectrum analyzer. The noise figure of the feedback DA is then extracted after the overall system loss is calibrated out. Fig. 2.16(b) illustrates the simulated and measured noise figure of the feedback DA. The minimum noise figure achievable is 10.5 dB at 65 GHz.

2.5.2 Large-signal Measurements

Fig. 2.17 illustrates the measurement setup for the W-band power sweep. In this approach, a W-band signal is generated using a PNA-X network analyzer and multiplied by a WR-10 frequency extender from Keysight Technologies. The signal is amplified by a commercially available connectorized waveguide

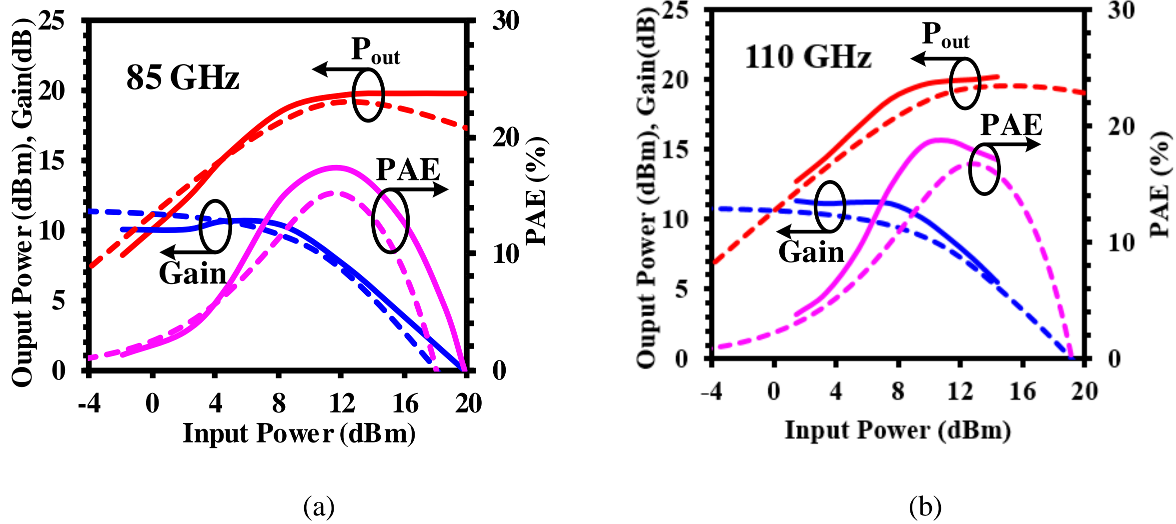


Fig. 2.18. Measured and simulated output power, gain, and PAE of the proposed feedback DA at (a) 85 GHz, and (b) 110 GHz. The solid line and dashed line are measurement and simulation, respectively.

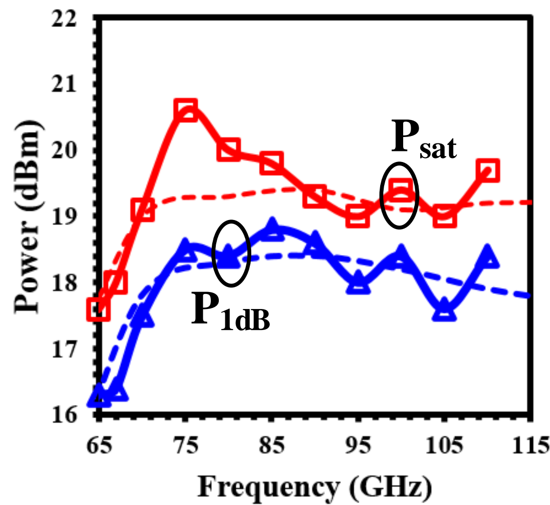


Fig. 2.19. P_{sat} and P_{1dB} over the frequency of the feedback DA. The solid line and dashed lines are measurement and simulation, respectively.

W-band power amplifier from SAGE Millimeter. The input signal to the WR-10 S-bend is calibrated using the WR-10 power sensor Agilent W8486A and the power meter Keysight E4417A EPM-P. The loss of the probe and S-bend combination is then de-embedded using data from the thru-measurement of the back-to-back configuration. The input and output power from the DUT can be obtained. The dc current is recorded

Table 2.2. Comparison to State-of-The-Art Wideband Amplifiers

Reference	Technology	Gain (dB)	BW (GHz)	f_T/f_{max} (GHz)	P_{sat} (dBm)*	PAE (%)	P_{dc} (mW)**	Die size (mm^2)
[46]	InP	20.7	71-95	400/700	21.2@81GHz	40@81GHz	433	0.47
	InP	17.8	96-122	400/700	20.2@110GHz	22.5@110GHz	442	0.38
[47]	InP	10	38-220	375/650	9.2 @77GHz	5@77GHz	105	0.33
[48]	InP	10	40-185	360/400	10 @160GHz	-	96	1.36
[49]	InP	12	31-130	360/400	11.5 @110GHz	8@110GHz	129	0.6
[50]	InP	10	40-105	270/750	12@96GHz	43@93GHz	43	0.73
[3]	SiGe	20	10-170	270/450	13.5 @135GHz	-	560	0.91
[28]	SiGe	14.5	52-142	-/210	1.6 @75GHz	-	103	0.45
[51]	SiGe	8.5	dc-135	230/300	11 @20GHz	-	99	0.36
[33]	SiGe	12	14-105	300/-	17 @50GHz	12.6@50GHz	297	1.51
[40]	SOI	16	1.5-103	290/250	22@15GHz	19.5@15GHz	890	0.33
[52]	SOI	13	10-82	280/270	17.2@50GHz	17.4@50GHz	182	0.8
	SOI	12.6	11-83	280/270	17.5@50GHz	20.2@50GHz	182	0.8
[53]	GaAs	11	dc-110	380/500	11 @75GHz	-	425	1.69
Conventional DA	**InP**	**6.5**	**15-148**	**290/390**	**19.5 @20GHz**	**20.1@20GHz**	**440**	**0.96**
Feedback DA	**InP**	**10.5**	**60-145**	**290/390**	**20.9 @75GHz**	**19.2@110GHz**	**440**	**0.96**

*Maximum reported saturated output power** Small-signal condition

through the high-precision dc supply Agilent 34401A. The large-signal measurement setup is validated by measuring a commercial power amplifier and comparing it with the provided datasheet, which shows consistency across W-band.

Fig. 2.18 presents the large-signal measurement of the proposed feedback DA. The measured and simulated results at 85 GHz, and 110 GHz are shown in Fig. 2.18(a) and (b), respectively. At 85 GHz, the DA attains a saturated power (P_{sat}) of 19.8 dBm, a 1-dB compression output power (P_{1dB}) of 18.8 dBm, and a maximum power added efficiency (*PAE*) of 17.3 %. At 110 GHz, the P_{sat}, P_{1dB}, and maximum *PAE* are 20.2 dBm, 18.6 dBm, and 19.2 %, respectively. The measured results at these frequencies are slightly higher than the simulated ones. This effect might be caused by the conservative modeling of the device.

The input power is driven up to 20 dBm without damaging the device. The output signal of the DA at high input power is observed with the spectrum analyzer. There are no indications of parametric instability.

The measured and simulated 1-dB compression output power, P_{1dB}, and the saturated power, P_{sat}, over the frequencies are provided in Fig. 2.19. The maximum achievable P_{sat} is 20.9 dBm at 75 GHz with the corresponding P_{1dB} of 18.5 dBm. The minimum P_{sat} in W-band is 19 dBm, which is coherent with state-of-the-art InP technologies that can offer at W-band and above [46], [54]. Table 2.2 summarizes the performance of state-of-the-art wideband amplifiers in the same frequency range.

2.6 Conclusion

A wideband gain boosting technique for distributed amplifiers has been introduced and analyzed. The technique employs an inductive feedback network to achieve a wideband gain improvement without sacrificing the gain-bandwidth product. The fabricated InP DA achieves a measured gain of 10.5 dB from 60 to 145 GHz, and the highest P_{sat} of 20.9 dBm at 75 GHz. Compared to the conventional DA, the proposed gain enhanced DA exhibits an average gain improvement of 4 dB over a wide bandwidth from 64 to 142 GHz. More importantly, the gain enhancement is achieved without a trade-off in gain bandwidth, dc power consumption, output power, and chip size. Therefore, the proposed technique is suitable for high gain distributed amplifiers operating close to the transition frequency f_T of the process.

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Chapter 3. A Wideband Highly Linear Distributed Amplifier Using Intermodulation Cancellation Technique for Stacked-HBT Cells

As the demand for high data rate communication systems is increasing rapidly, distributed amplifiers (DAs) are among the critical components to enable such systems, especially for measurement and testing purposes [1]. Typically, the requirements for DAs are high gain and wide bandwidth. However, when the systems become more sophisticated and highly integrated, the amplifiers are also required to have high output power, high linearity, low power consumption, and small chip size. Distributed amplifiers have been presented in various technologies. While Gallium Arsenide (GaAs) and Gallium Nitride (GaN) processes can provide medium to high output power, the gain-bandwidth product (GBW) is limited by their low transition frequencies [2]-[7]. On the other hand, complementary metal-oxide-semiconductor (CMOS) technologies offer wide bandwidth but low output power and poor linearity [8]-[9]. Silicon-on-Insulator (SOI), Silicon Germanium (SiGe), and Indium Phosphide (InP) are among the processes that maintain a good balance between power, bandwidth, and dc consumption [10]-[21].

Different linearization schemes for power amplifiers have been introduced including analog post-distortion [22], pre-distortion [23], active pre-distorter [24], feedforward [25], and harmonic injection [26]-[29]. However, most linearization techniques are inherently narrow-band and only suitable for band-limited amplifiers. Few wideband linearization techniques have been presented to date. [30] presented a CMOS distributed amplifier that uses a distortion cancellation gain unit cell. The technique can achieve up to 5 dB 3rd order intermodulation product (IM3) enhancement, but the bandwidth limits to only 8 GHz. On the other hand, the feedforward linearization concept was extended to linearize a GaAs DA up to 20 GHz [31]. The proposed circuit employed a separated auxiliary amplifier and two phase-shifters, which significantly increases the chip size and limits the bandwidth. Recently, a dc - 65 GHz CMOS DA using active input balun was demonstrated [32]. The amplifier also employs a dual-output two-stage g_m topology to enhance

linearity with 10 dBm output power at 1-dB compression (P_{1dB}) reported. However, the linearity enhancement is only achieved at low frequency.

Derivative superposition (DS), which was first presented in [33], [34], is another innovative linearization technique for amplifiers. The technique employs one or more auxiliary transistors to create an external 3rd order intermodulation (IM3) that has an equal amplitude and out-of-phase with the main IM3. Therefore, in theory, the overall 3rd order intermodulation can be canceled. Later, [35] presented a modified DS method using a power series analysis to improve the IIP3 of a low noise amplifier (LNA) while [36], [37] demonstrated a multi-gated transistor technique (MTGR) that was originally based on the Volterra series analysis of the DS technique. Also, based on the DS technique, [38] combined both MTGR and capacitance compensation to increase the distributed amplifier linearity from 4 to 8.8 GHz. However, the technique requires the process to have both n-type and p-type transistors. Recently, the digitally assisted DS technique has also been presented in [39]. Compared to other conventional linearization methods, the DS technique can provide good IM3 improvement over a wide dynamic range while consuming very little extra dc power [40]. However, the DS method has some bandwidth limitations at high frequency. Also, most DS techniques have only been applied for conventional common-source FET topology or cascode FET cells. In addition, the phase and amplitude characteristics over wide bandwidth have not been fully analyzed in previously published works. Hence, high linearity is only achieved in a limited frequency and power range.

A highly linear dc – 90 GHz InP distributed amplifier with the proposed 3rd order intermodulation cancellation technique has been presented in [41]. In this chapter, a detailed mathematical and numerical analysis, simulations, and further experimental results will be reported. The linearization technique proposes a feed-forward IM3 cancellation applied for stacked-Heterojunction Bipolar Transistor (HBT) cells in a distributed amplifier. In particular, the main arm employs a stacked-HBT cell, and an auxiliary arm employs a common-emitter transistor. With a small auxiliary transistor employed, the overall 3rd order intermodulation distortion product is significantly reduced at the output. The 3rd degree coefficient behavior

of a stacked-HBT cell is different from that of a single device. Secondly, the phase and amplitude characteristics over a wide frequency range are investigated, and solutions such as an emitter degeneration resistor and phase-matching transmission lines are proposed ssto tackle these issues. Finally, linearity responses over temperature, bias variations, and the sensitivity of the linearization scheme are demonstrated.

To verify the concept, two millimeter-wave monolithic integrated circuit (MMIC) amplifiers, namely a conventional stacked-HBT DA and a linearized DA, are designed, fabricated, and compared using experimental results. Finally, large-signal measurement results up to 85 GHz will be presented to verify the theory and simulation. Both the conventional and linearized DA's exhibit a wide bandwidth of 75 GHz and 90 GHz, with a small-signal gain of 14 dB and 10.5 dB, respectively. Most importantly, the linearized DA achieves a measured maximum output power at 1-dB compression P_{1dB}, saturation power (P_{sat}), and 3rd order intercept point (OIP3) of 20.5 dBm, 22 dBm, and 33 dBm, respectively. As compared to the conventional DA, the results show 3.5 dB, 2 dB, and 4.5 dB improvement in P_{1dB}, P_{sat}, and OIP3, respectively. The linearity enhancement is maintained up to 85 GHz with the same die size and very little increase in dc power consumption. To the best of the author's knowledge, the linearized amplifier achieves the highest bandwidth compared to previous amplifiers using DS method techniques. More importantly, while other DS and MTGR methods only focus on improving the IM3 [40], our proposed DA not only improved the IM3, but it also enhances the 1-dB compression point.

3.1 Proposed Linearization Technique

3.1.2 Proposed wideband linearization technique

Unlike most conventional linearization methods in which the linearization is implemented for a common source FET [33], [34], our proposed distributed amplifier employs a stacked-HBT configuration. Compared to the conventional common-emitter amplifier [42], the stacked-HBT topology can achieve a higher output power and better bandwidth [11], [43], [44]. Fig. 3.1(a) presents the stacked-HBT gain unit cell. In the stacked-HBT cell, two transistors Q1, Q2 are placed in a common emitter and common base

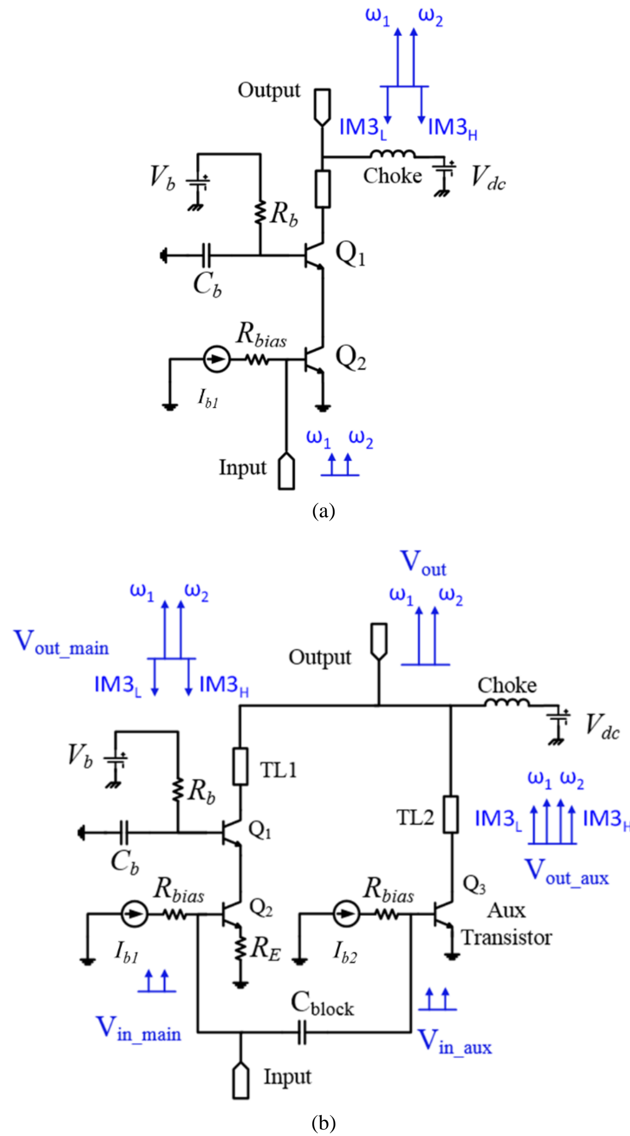


Fig. 3.1. (a) Conventional stacked-HBT gain unit cell, and (b) proposed linearized gain unit cell.

configuration. It is important to note that the resistor-capacitor (Rb – Cb) network at the base of Q1 allows for a certain voltage swing at that node so that the voltage swing will be equally divided between the two transistors [45]-[47]. Therefore, the amplifier can achieve high output power without exceeding the breakdown limit of the process. Moreover, the stacked-HBT structure helps reduce the Miller effect, resulting in a lower input capacitance. Therefore, a distributed amplifier employing stacked-HBT gain unit cells can achieve higher bandwidth.

Fig. 3.1(b) illustrates the proposed linearized gain unit cell. The stacked-HBT cell is still the main signal path. An auxiliary small transistor Q_3 is employed and placed in parallel with the main stacked-HBT cell. The main arm and auxiliary arm are biased separately by two current sources I_{b1} and I_{b2}. Besides the device size of the auxiliary transistor Q_3, the bias conditions are critical to achieving the desired linearity. In addition, the main arm employs emitter degeneration resistor R_E to have more control over the phase and amplitude. Finally, the two transmission lines TL1 and TL2, help align the phase of the signals from the main and auxiliary arms to achieve wideband IM3 cancellation. It is worth noting that the main arm employs a stacked-HBT cell to maximize the fundamental output power and bandwidth. On the other hand, the main purpose of the auxiliary arm is to provide negated 3rd order intermodulation product IM3's. Therefore, only a single common-emitter device is used in the auxiliary arm to minimize the overall power consumption. A single auxiliary transistor also reduces the complexity of biasing circuits, layout, and optimization.

To effectively reduce the 3rd order intermodulation products IM3, both the phase and amplitude of the 3rd degree coefficients need to be engineered correctly since all the coefficients are functions of the bias current, input power level, and frequency. If we consider the main stacked-HBT cell as a single-stage amplifier and the input signal has two frequency tones ($\omega_2 > \omega_1$) with equal amplitude, the output voltage (up to 3rd degree) can be expressed as follows:

$$V_{in}(t) = A[\cos(\omega_1 t) + \cos(\omega_2 t)] \tag{3.1}$$

$$V_{out} = a_1 V_{in} + a_2 V_{in}^2 + a_3 V_{in}^3 \tag{3.2}$$

where a_1, a_2, a_3 are the first three terms of the power series expansion of the output voltage as a function of the input tone. In particular, a_2 has the unit of V^{-1} and a_3 has the unit of V^{-2}. Although these coefficients are different from a_{i1} and a_{i3} demonstrated in Section 2.1, they are related to each other and share similar characteristics. Replacing V_{in} in (3.2) by (3.1), the fundamental output voltage V_{out} at frequency ω_1 can be written as [48]:

$$V_{out}(\omega_1 t) = (a_1 A + \frac{9}{4} a_3 A^3)\cos(\omega_1 \text{t}) \quad (3.3)$$

In class-AB amplifiers, the value of a_3 has an opposite sign with a_1. Therefore, the term ($a_1A + \frac{9}{4} a_3A^3$) is smaller than a_1A, causing the gain compression in the amplifier. In particular, due to the mixing phenomenon, the high side and low side 3rd order intermodulation products ($IM3_H$ and $IM3_L$), which will appear in the vicinity of ω_1 and ω_2, can be written as [39]:

$$IM3_L = \frac{3}{4} a_3 A^3 \cos\left[(2\omega_1 - \omega_2)t\right] \quad (3.4)$$

$$IM3_H = \frac{3}{4} a_3 A^3 \cos\left[(2\omega_2 - \omega_1)t\right] \quad (3.5)$$

In the proposed design, the auxiliary arm is added to create additional IM3 components. Similarly, (b_1, b_2, b_3) are the fundamental, 2nd degree, and 3rd degree coefficients of the auxiliary device. If the input signal is split between the main and auxiliary arms with a splitting factor γ, then:

$$V_{in_{main}}(t) = \gamma A[\cos(\omega_1 t) + \cos(\omega_2 t)] \quad (3.6)$$

$$V_{in_{aux}}(t) = (1-\gamma)A[\cos(\omega_1 t) + \cos(\omega_2 t)] \quad (3.7)$$

The total fundamental signal at ω_1 and the low side IM3 products $IM3_L$ will be expressed in (3.8) and (3.9).

$$V_{out}(\omega_1 t) = [a_1 \gamma A + \frac{9}{4} a_3 \gamma^3 A^3 + b_1(1-\gamma)A + \frac{9}{4} b_3 (1-\gamma)^3 A^3]\cos\omega_1 \text{t} \quad (3.8)$$

$$IM3_L = \frac{3}{4} a_3 \gamma^3 A^3 \cos(2\omega_1 - \omega_2)t + \frac{3}{4} b_3 (1-\gamma)^3 A^3 \cos(2\omega_1 - \omega_2)t \quad (3.9)$$

According to (3.9), to cancel the IM3 product, the coefficient b_3 need to satisfy the condition:

$$b_3 = -a_3 (\frac{\gamma}{1-\gamma})^3 \quad (3.10)$$

in which the minus sign implies that the auxiliary IM3 has a 180° phase different from the main IM3. In practice, the value of γ depends on the input impedance of the main and auxiliary transistors. Therefore, all

the parameters a_3, b_3, and γ in (3.10) are generally frequency-dependent. Compared to the analysis in previous linearization papers [34]-[37], [39], [40], (3.10) provides a simple and efficient method for the initial design of the auxiliary transistor to be then further optimized in CAD tools. If we replace b_3 in (3.8) by (3.10), the fundamental signal at frequency ω_1 will become:

$$V_{out}(\omega_1 t) = [a_1 \gamma A + b_1 (1-\gamma) A] \cos\omega_1 \mathrm{t} \tag{3.11}$$

Identical results can be derived for frequency ω_2 and the high side $IM3_H$; thus are not presented here. With any certain value of a_3 derived from (3.12) (or extracted from CAD tools), we can engineer an auxiliary arm to have the value of b_3 that satisfies (3.10), and the overall IM3 signals will be suppressed. Moreover, the value of b_1 is typically smaller than a_1. Therefore, according to (3.11), the small-signal gain of the linearized amplifier will be smaller than that of the conventional amplifier. The numerical analysis of our proposed linearization method will be discussed in the next section.

3.2 Linearized Gain Unit Cell

While the previous section presents a theoretical analysis of the proposed technique, simulation using the InP process design kit (PDK) has been conducted to take into account all the effects of frequency-dependent parameters. The degeneration resistor and parasitic emitter inductance create a feedback path from the collector current to the base-emitter voltage. At high frequencies, the feedback path makes the contribution of the 2nd order non-linearity to IM3 become noticeable and eventually limits the IM3 improvement of the proposed technique [35]. In our design, the emitter and the degeneration resistor are connected to the common ground through a co-planar plane to minimize the parasitic inductance. Furthermore, the base bias current is optimized to achieve good linearity improvement at both low and high frequencies.

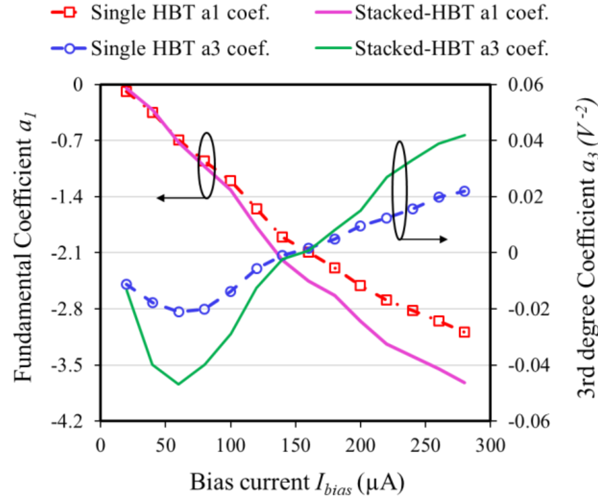


Fig. 3.2. Fundamental and 3rd degree coefficients of the single common-emitter HBT and stacked-HBT gain unit cell

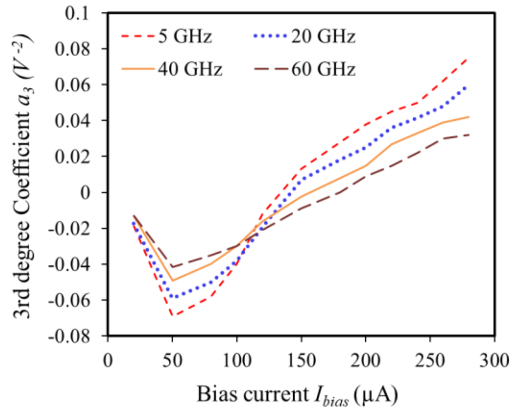


Fig. 3.3. Third degree coefficient a_3 at frequencies: 5, 20, 40, 60 GHz

To extract the coefficient values for our numerical analysis, we simulated both the stacked-HBT and single common-emitter transistor using the components provided in the PDK. The simulation was carried out at different bias currents, temperatures, device peripheries, and frequencies to find the fundamental output V_{out} and 3rd order intermodulation distortion product IM3. Since in general, V_{out}, $IM3_L$, and $IM3_H$ have complex values, a_1 and a_3 are also derived in complex terms. In this section, the presentation of the complex a_1 and a_3 is separated into amplitude and phase. Very little difference between the lower side $IM3_L$ and upper side $IM3_H$ is observed in the simulation.

Fig. 3.2 presents the two coefficients a_1 and a_3 as a function of I_{bias}. The values are extracted from the simulation of a single 10 µm common emitter (CE) HBT device and a stacked-HBT unit cell (both devices in the stack have 10 µm emitter length). It is critical to note that while a_1 is always negative (the negative sign is because of the common-emitter configuration [49]), and its absolute value increases with respect to the bias current, the value of a_3 switches from negative to positive when I_{bias} crosses a certain value (usually around the pinch-off of the HBT device). Moreover, the values of a_1 and a_3 of both single and stacked configurations change in the same manner. However, the stacked-HBT has a higher fundamental gain as well as higher 3rd degree coefficients. Therefore, to linearize a stacked-HBT cell, the auxiliary arm needs to supply a higher IM3 amplitude.

The behavior of the 3rd degree coefficient a_3 is further investigated over different frequencies and different temperatures. Fig. 3.3 shows the simulated coefficient a_3 of the stacked-HBT cell at four different frequencies across the band: 5, 20, 40, and 60 GHz. Although the absolute values of a_3 vary over frequencies, the sign flipping behavior still maintains across the frequency band of interest. More importantly, at the frequencies where a_3 has a higher absolute positive value (e.g., 5 GHz), it also has a higher absolute negative value. This phenomenon helps maintain the linearization over a very wide bandwidth. Fig. 3.4 presents the a_3 coefficient over temperature from -5°C to 95°C. The variation of a_3 over temperature shares a similar trend but is much smaller than the variation over frequency. It is also worth noting that the "switching points" (where a_3 changes from negative to positive) are different at different frequencies and temperatures.

From the above analysis, since the main stacked-HBT cell is biased in class-AB, a_3 will be positive. Therefore, if we bias the auxiliary device below the "switching point," we can have a negative b_3. Hence, the two IM3 signals from the main and auxiliary arms will be 180° phase different. Besides the 180° phase different requirement, to suppress the IM3 products, the amplitudes of a_3 and b_3 also need to satisfy (3.10). The critical parameter that determines the value of b_3 is the emitter length of the auxiliary device.

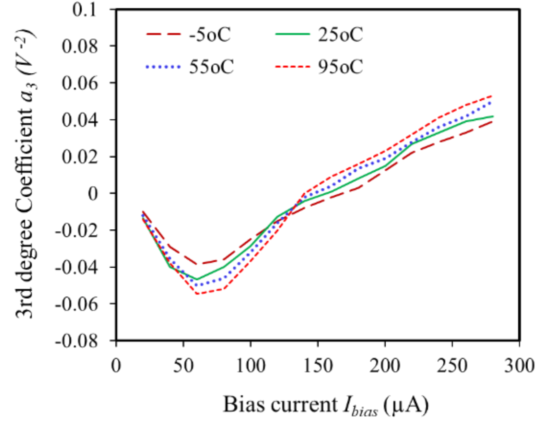


Fig. 3.4. Third degree coefficient a_3 at temperature: -5, 25, 55, 95ºC.

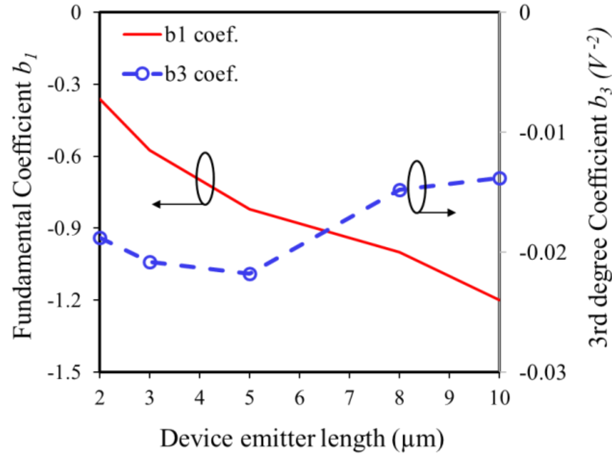


Fig. 3.5. Fundamental and 3rd degree coefficients of the auxiliary device Q_3 at I_{bias} = 100 µA.

The device size is not only chosen to achieve the required b_3, but also to minimize the dc power consumption. Typically, the smaller the device, the less dc power dissipation. Fig. 3.5 shows the b_1 and b_3 coefficients of different device sizes at I_{bias} = 100 µA. Regarding the absolute values, while b_1 increases as the device become larger, b_3 only maintains high absolute values when the device is small. In our proposed design, we choose the auxiliary HBT emitter length to be 5 µm to have the b_3 = -0.022 V^{-2}.

In addition to choosing the auxiliary device size and its dc bias condition, the main signal path can also be optimized to further linearize the gain unit cell. In [50], two degenerated resistors are introduced in

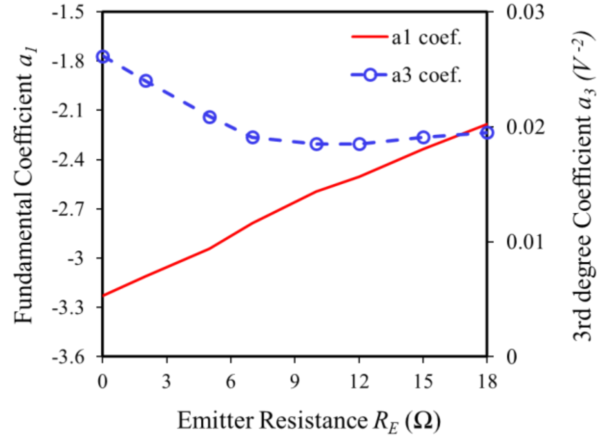


Fig. 3.6. Fundamental and 3rd degree coefficients of the main stacked-HBT cell with emitter degeneration R_E.

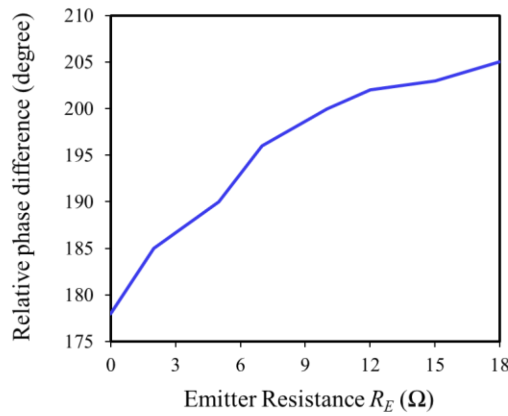


Fig. 3.7. Simulated relative phase difference between the fundamental and 3rd IM3 with emitter degeneration R_E.

both the main and auxiliary arms to optimize just for the amplitude matching. In our proposed design, only in the main arm, an emitter degeneration resistor will be added to modify both the amplitude and phase characteristics of the signal.

Fig. 3.6 and Fig. 3.7 present the simulated amplitude and phase of the stacked-HBT cell (emitter length 10 µm) at I_{bias} = 220 µA with an emitter degeneration resistor R_E. With R_E = 5 Ω, the value of a_3 can be reduced to match with b_3. Moreover, with R_E added, the phase can be changed and optimized for phase

alignment between the main IM3 and auxiliary IM3 to achieve the highest IM3 cancellation over a wide bandwidth. Although adding R_E reduces the overall amplifier gain, it helps to achieve a better alignment for both the IM3 phase and amplitude between the main and auxiliary arms, therefore ensuring that the here proposed linearization technique can perform well over a wide frequency range.

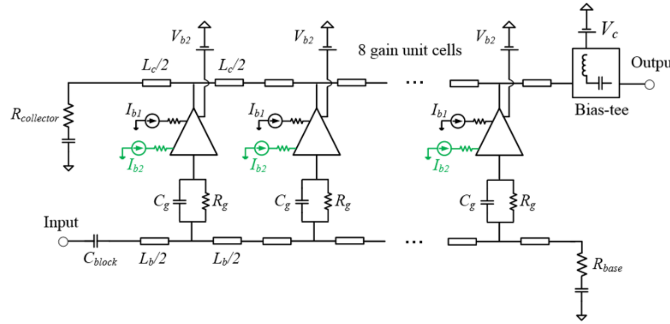


Fig. 3.8. Schematic diagram of the proposed distributed amplifier.

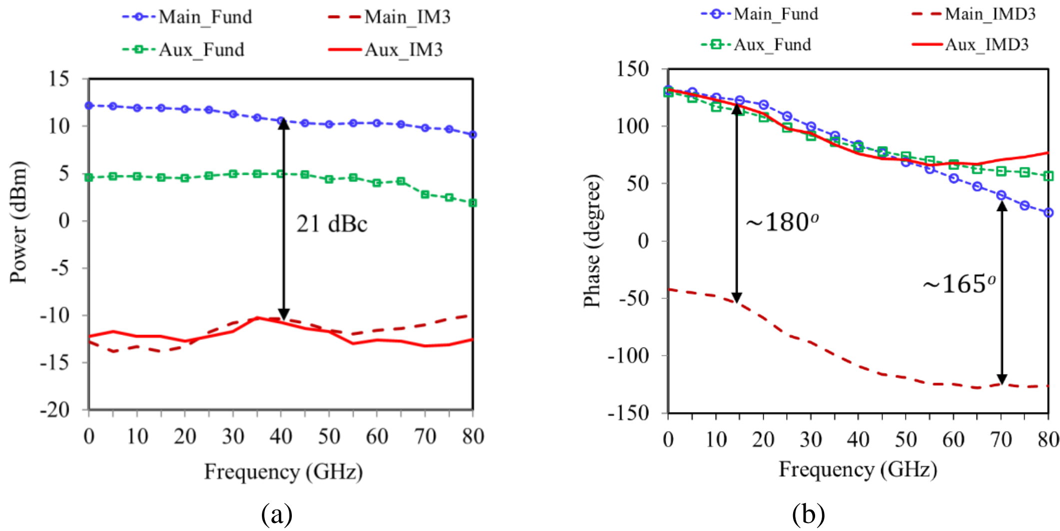


Fig. 3. 9. Simulated amplitude (a) and phase (b) of the fundamental components and 3rd order intermodulation products at the output of the main and auxiliary paths under two-tone excitation.

3.3 Distributed Amplifier Design

To verify the proposed concept, two distributed amplifiers are designed and fabricated. The schematic diagrams of the amplifiers are shown in Fig. 3.8. For the conventional DA, the gain unit cell is

the one in Fig. 3.1(a) and for the linearized DA, the unit cell is shown in Fig. 3.1(b). For the linearized DA, an additional bias current I_{b2} is required. The amplifier employs eight identical gain unit cells. At the input of each gain unit cell, a parallel RC network is added to reduce the overall input capacitance and extend the DA bandwidth up to 90 GHz [11]. The base and collector transmission lines, as well as termination resistors R_{base} and $R_{collector}$ are designed to achieve wideband input and output matching. Since the gain unit cells of the two amplifiers are different, the design parameters of the two DAs are also different and are presented in Table 3.1.

The simulation of the linearized DA shown in Fig. 3.8 was carried out using Keysight Advanced Design System (ADS) to verify the proposed design. The simulation of the full amplifier with eight gain unit cells took into consideration of all the loading effects and parasitics. Current and voltage probes are placed at the output of the main and auxiliary arms to measure the power contributed by each arm separately.

Fig. 3.9 presents the simulated amplitude and phase of the main and auxiliary arms with the input power of the gain unit cell at 0 dBm, which is close to the 1-dB compression point of the main stacked-HBT cell. The fundamental component of the auxiliary path is smaller than that of the main path since it is a smaller transistor. However, the auxiliary device is biased with a lower current and can generate similar IM3 products. Therefore, the IM3 signals of the two arms have equal amplitude. Besides the amplitude, the phase characteristic of the two signals is also critical for linearizing the amplifier. As shown in Fig. 3.9(b), the phases of the fundamental component and IM3 component of the main path are 180° different. On the other hand, the auxiliary path generates the fundamental signal and IM3 signal that are in-phase with each other. As a result, the IM3 signals of the two arms have the same amplitude and 180° out of phase. Ideally, they will cancel and provide a significant improvement in linearity. In practice, the amplitude and phase characteristics of the auxiliary transistor start to deviate from the designed values at frequencies larger than 65 GHz. For instance, at low frequencies, the relative phase difference between the fundamental signal and the IM3 signal of the main arm is well aligned with the theory, which is about 180°. However, at high

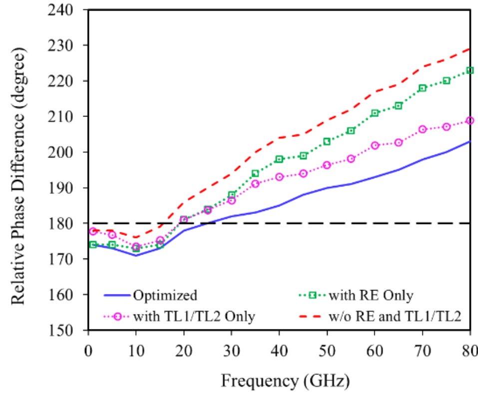


Fig. 3.10. Relative phase difference between the main IM3 and auxiliary IM3 signals versus frequency under the impact of TL1/TL2 and R_E.

Table 3.1. Design Parameters Of The Two Amplifiers

Design parameters		Conventional DA	Linearized DA
Gain unit cell	Topology	Stacked-HBT	Linearized cell
	R_E	0 Ω	5 Ω
Bias conditions	I_{b1}	220 µA	220 µA
	I_{b2}	N/A	100 µA
	V_c	4 V	4 V
	V_{b2}	1.8 V	1.8 V
Input RC network	C_g	90 fF	75 fF
	R_g	1000 Ω	1000 Ω
Inductances	L_b	36 pH	24 pH
	L_c	90 pH	66 pH
Terminations	R_{base}	50 Ω	50 Ω
	$R_{collector}$	50 Ω	47 Ω

frequencies, that phase difference reduces to around 165°. The phase variations in both the main and auxiliary arms make the IM3 cancellation less effective at high frequencies. Hence, two transmission lines TL1 and TL2, along with an emitter degeneration resistor R_E are added to further optimize the phase alignment.

Fig. 3.10 demonstrates the relative phase offset between the main and auxiliary IM3 signals in different cases: without R_E and TL1/TL2, with each of the components separately, and the fully optimized design (include both R_E and TL1/TL2). Ideally, this phase offset needs to be close to 180° to achieve good

IM3 cancellation. The original phase offset without $R_{E,}$ and the two transmission lines deviate far from 180° starting from 30 GHz. The TL1 and TL2 are 200 µm different in physical length. Assuming the physical length is fixed, the electrical length increases proportionally with respect to the frequency. At low frequencies, the 200 µm long transmission line results in very little change in electrical length between the two paths, but it causes a significant phase difference at high frequencies. Such an interesting characteristic, along with the phase changes provided by the degenerated resistor R_E helps bring the phase offset much closer to 180° across the whole frequency band.

Fig. 3.11 presents the simulated fundamental, power gain, and IM3 amplitude of the main arm and auxiliary arm at 40 GHz as a function of input power. All the device sizes, bias conditions, and phase alignment are designed to perfectly match the IM3 amplitude of both arms. The fundamental signal of the auxiliary arm experiences a gain expansion and starts to compress earlier than the main signal. The linearization technique performs well over a wide dynamic range of input power from below -25 dBm up to -3 dBm. As the transistors compress, the IM3 starts to have a dip at a certain power level [51]. However, the technique can still provide excellent linearity enhancement up to 1-dB gain compression point. Simulated P_{1dB} and OIP3 comparison between a conventional DA, a conventional DA with resistive degeneration, and the linearized DA are presented in Fig. 3.12. While the degenerated resistor alone only provides very little linearity enhancement, the proposed linearization technique observes a significant improvement. Compared to the conventional DA, the linearized DA has an average of 1.4 dB higher in the 1-dB compression point P_{1dB} and 4.2 dB higher in the 3rd order intercept point OIP3. The linearity enhancement achieves the best performance from dc to 65 GHz, corresponding to the frequency range where perfect phase alignment is achieved in Fig. 3.9(b).

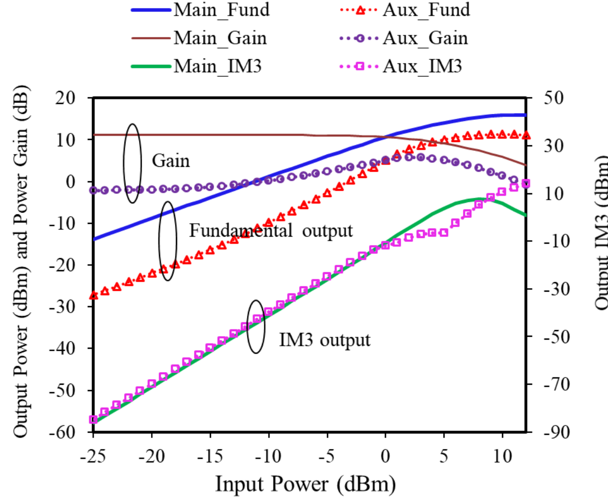


Fig. 3. 11. Fundamental and IM3 amplitude as a function of input power at 40 GHz.

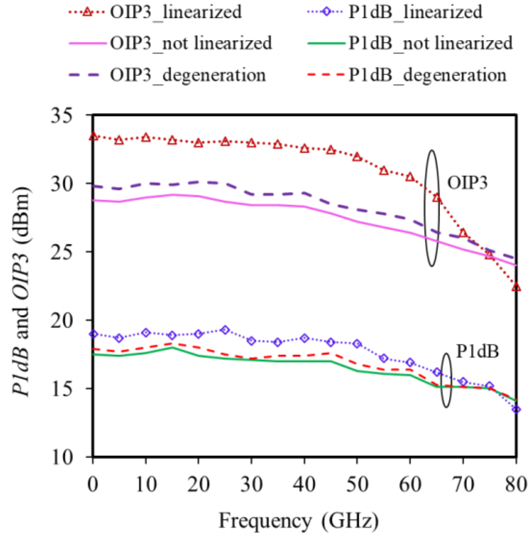
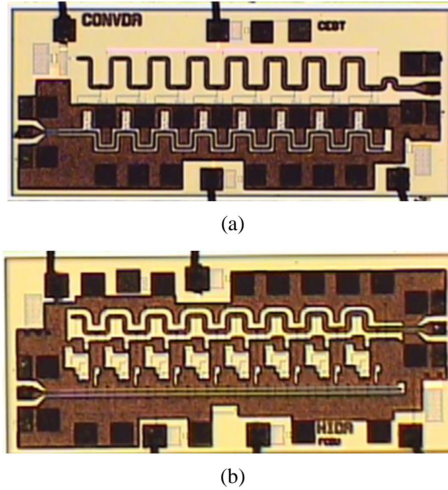


Fig. 3. 12. Simulated P_{1dB} and OIP3 of the linearized DA and conventional DA over frequency.

3.4 Experimental Results

The two distributed amplifiers are designed and fabricated in an InP HBT process. The process has a transition frequency f_T of 250 GHz and a maximum frequency f_{max} of 380 GHz. The chip photos are shown in Fig. 3.13. All the input and output inductances are realized by coplanar transmission lines except the output inductance of the conventional DA uses microstrip lines. The current sources I_{b1} and I_{b2} are provided by two bond pads. Wideband terminations at both the base and collector are designed using several RC



(a)

(b)

Fig. 3. 13. Chip photograph of (a) conventional stacked-HBT DA, and (b) proposed linearized DA.

networks placed in parallel, including a bond pad that connects to a 10 μF off-chip capacitor. Both DAs have a die area of 1.6 x 0.7 mm^2, including all pads. The proposed linearization technique does not increase the chip size. All the measured results are based on the bias condition depicted in Table 3.1. At small signal conditions, both amplifiers draw around 100 mA collector current. In the proposed linearized DA, the collector current increases to 150 mA when the amplifier reaches maximum output power.

Fig. 3.14 illustrates the measured frequency responses of the two DAs. The conventional amplifier has a small signal gain of 14 dB, and the 3-dB gain bandwidth of 75 GHz. The proposed linearized amplifier exhibits an average gain of 10.5 dB. The 3-dB gain bandwidth covers up to 90 GHz, making the gain-bandwidth product of 301 GHz. Compared to the conventional DA, the linearized DA has 3.5 dB lower small-signal gain since the input signal is split into the main arm and auxiliary arm by a factor of γ. However, while the gain of the conventional DA rolls off quickly beyond 75 GHz, the linearized DA can extend the bandwidth up to 90 GHz. Both amplifiers have good input and output return losses over the entire frequency band. Fig. 3.15 presents the measured insertion phase and group delay of the two distributed amplifiers. The two amplifiers exhibit a similar phase and group delay performance up to 65 GHz. Although the conventional DA has a flatter in-band group delay, when the frequency goes above 65 GHz, its group delay starts to deviate and change more abruptly since it has a much stepper gain slope and lower bandwidth than the linearized DA.

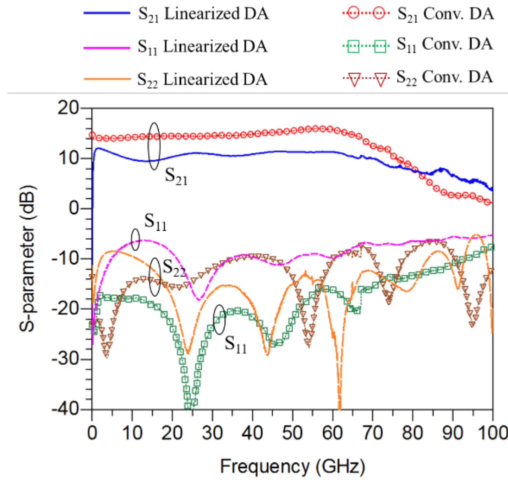


Fig. 3.14. Measured S-parameter of the conventional DA and proposed linearized DA.

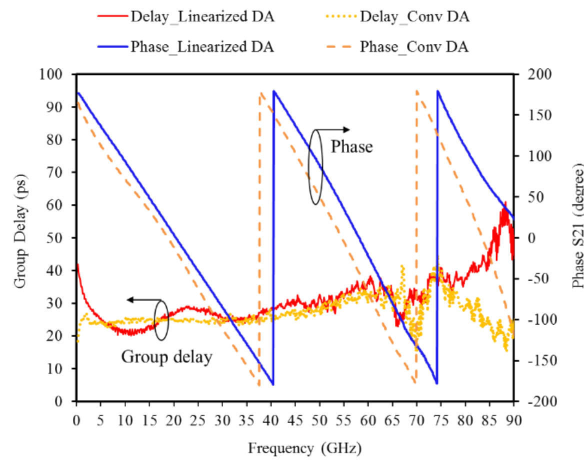
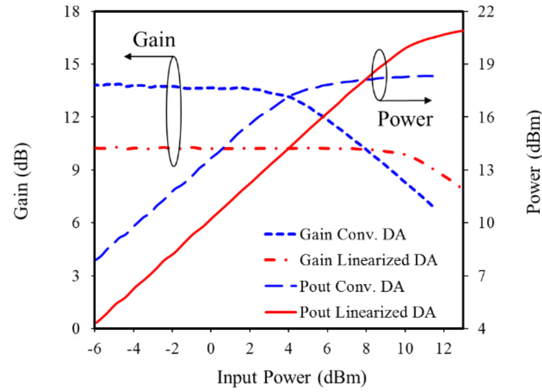
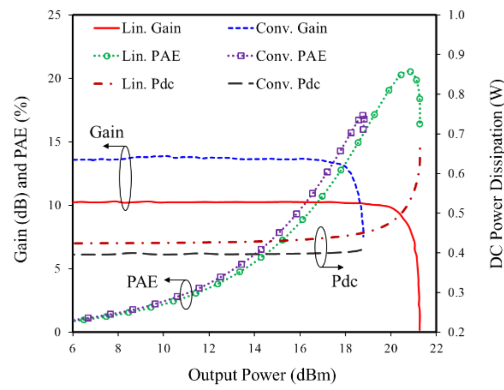


Fig. 3.15. Measured phase and group delay

Fig. 3.16(a) presents the measured large signal output power and gain of the linearized and conventional amplifiers at 20 GHz. Although having 3.5 dB less gain than the conventional design, the proposed linearized amplifier achieves 3 dB higher P_{1dB} and 2.5 dB higher P_{sat}, significantly extend the linear operation region of the amplifier. Fig. 18(b) further illustrates the total dc power dissipation and power added efficiency (PAE) of the two amplifiers. At low power, the linearized DA consumes 20 mW more than the conventional amplifier does, and the total dc current rises up to 150 mA at 21 dBm output power. Both amplifiers reach peak PAE at around its P_{1dB} compression point. Since the linearized DA can achieve higher output power, its peak PAE is 3% higher than the conventional DA despite consuming more dc power.



(a)



(b)

Fig. 3.16. (a) Measured output power and gain at continuous wave (CW) 20 GHz, and (b) dc power dissipation and PAE versus output power of the conventional DA and proposed linearized DA.

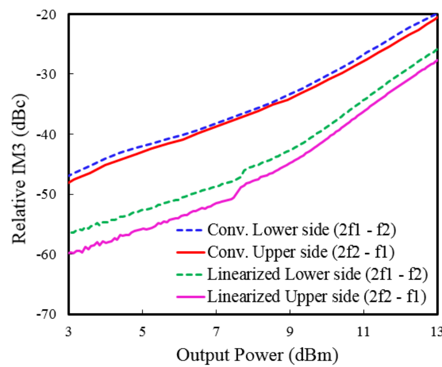


Fig. 3.17. Measured relative IM3 components of the conventional DA and linearized DA at 20 GHz using two-tone excitation with 10 MHz tone spacing.

Fig. 3.17 demonstrates the relative IM3 components from a two-tone measurement of the two distributed amplifiers at the center frequency of 20 GHz and a tone spacing of 10 MHz. The lower side IM3 component, which is the spectrum at frequency $2f_1 - f_2$, is improved by 10 dB in the low power region and

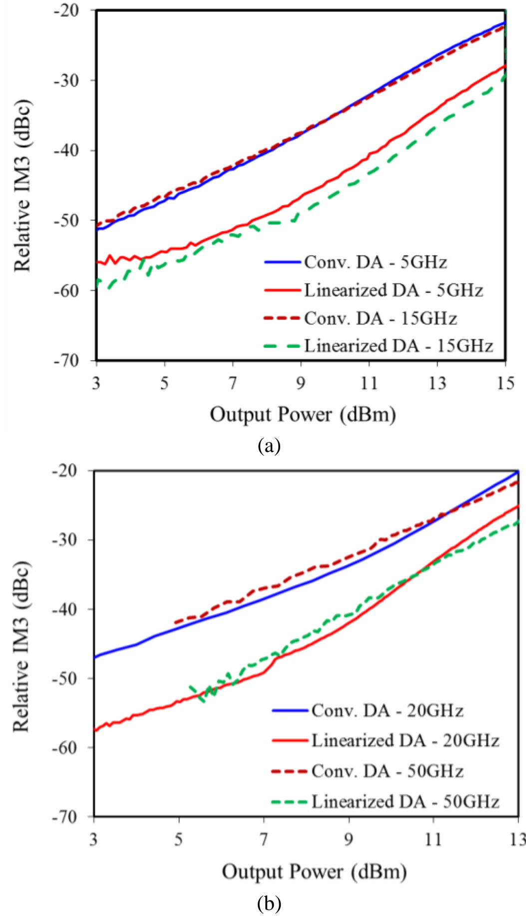


Fig. 3.18. Measured relative IM3 using two-tone excitation with 10 MHz tone spacing of the conventional DA and proposed linearized DA: (a) center frequency 5 GHz and 15 GHz, and (b) center frequency 20 GHz and 50 GHz.

by 6 dB at high output power. Similarly, the upper side IM3 component ($2f_2 - f_1$) is improved by 13 dB in the low power and 7 dB at high power. In both DAs, the lower side IM3 component is always higher than the upper side IM3 component.

Since the linearized amplifier has 3-dB gain lower than the conventional amplifier, the IM3 of the two amplifiers should be measured at the same output power level to provide a fair comparison. Fig. 3.18 shows the relative IM3's of the two amplifiers as a function of output power under two-tone excitation centered at different frequencies across the band with a tone spacing of 10 MHz. To simplify the plots, all the IM3 components shown in Fig. 3.18 are the average of the lower side and upper side IM3 components.

The average IM3 value is also used for OIP3 calculation. The linearized DA shows an average of 10 dB IM3 improvement, with the maximum improvement of 12 dB is observed at 20 GHz. The IM3 is also significantly suppressed from low output power region up to high output power. Most importantly, unlike other conventional linearization techniques having limited bandwidth, the proposed linearization scheme exhibits consistent performance over a very wide frequency range.

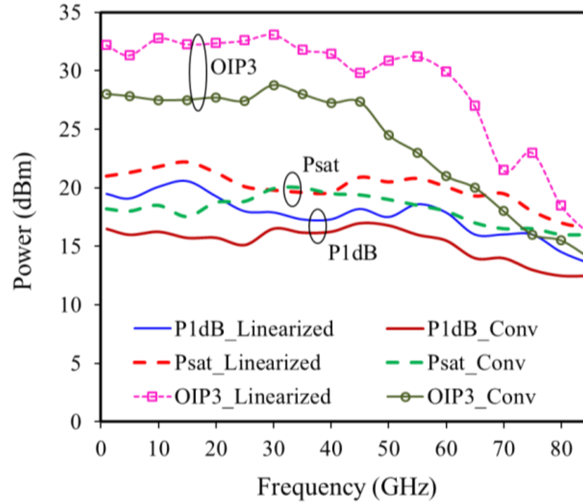


Fig. 3.19. Measured P_{1dB}, P_{sat}, and *OIP3* as a function of frequency (at room temperature, nominal condition).

Fig. 3.19 illustrates the measured power and linearity of the two DAs from 1 to 85 GHz. In the proposed linearized DA, the maximum P_{1dB} is 20.5 dBm, and the highest P_{sat} is 22 dBm, which is 3.5 dB and 2 dB improvement, respectively, as compared to the conventional DA. The measured maximum *OIP3* is 33 dBm achieved from 1 to 30 GHz, showing excellent linearity performance. From dc to 85 GHz, on average, P_{1dB} and P_{sat} are improved by 1.5 dB and 2.5 dB, respectively. The P_{1dB} and P_{sat} also show a flat response and only slightly roll off beyond 65 GHz. Most importantly, big enhancements in *OIP3* are observed from dc to 65 GHz, with 5 dB improvement at low frequencies and up to 7 dB improvement at high frequencies. The *OIP3* of both DAs roll off at high frequency, but the linearized DA still shows higher *OIP3* relative to the conventional design. Fig. 3.20 presents the measured versus simulated P_{1dB} and *OIP3* of the linearized amplifier. The measured results are well correlated with simulation over the entire

frequency band except for faster roll-off in *OIP3* beyond 65 GHz. The sensitivity of the proposed linearization method over temperature and bias variations is demonstrated in Fig. 3.21. According to the measured results shown in Fig. 3.21(a), the OIP3 is slightly decreased when the temperature increases with an average 0.9 dB lower at 55°C and 1.9 dB lower at 95°C.

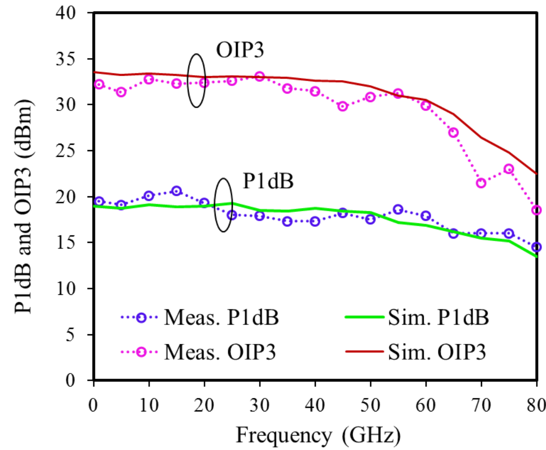


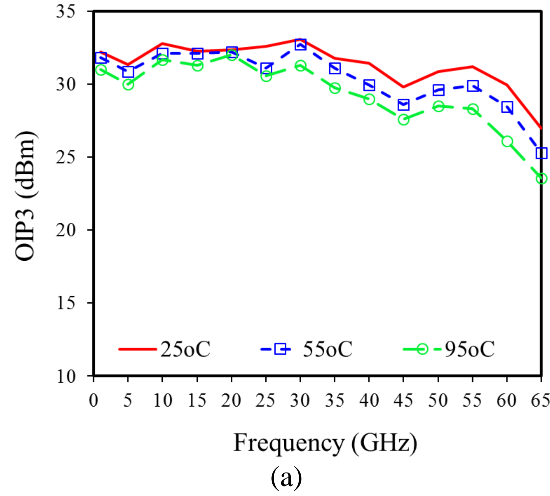
Fig. 3.20. Measured versus simulated P_{1dB} and *OIP3* of the proposed linearized DA.

Fig. 3.21(b) presents the *OIP3* when the bias current of the main arm (I_{b1}) is varied by ±10%, and the bias current of the auxiliary arm (I_{b2}) is varied by ±10% (when I_{b1} is varied, I_{b2} is kept constant and vice versa). While *OIP3* is insensitive to I_{b1} changes, the changes in I_{b2} affect the *OIP3* response over frequency. When I_{b2} increases, the linearity is better at low frequencies and worse at high frequencies due to the shift in the phase and amplitude match curves. The effect is reversed when I_{b2} decreases. At the nominal condition, the bias currents are optimized to achieve flat *OIP3* over the entire bandwidth.

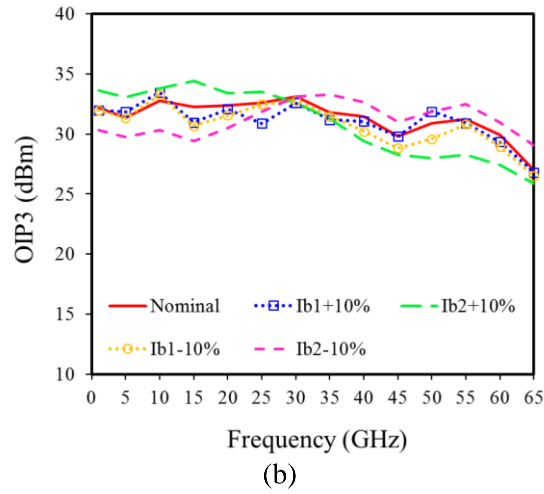
The proposed linearized DA presents a significant enhancement in power and linearity with a trade-off in small-signal gain and little increase in dc power consumption. To provide a fair comparison, we define the figure of merit (FOM) including all critical specifications of an amplifier as followed:

$$\mathrm{FOM} = \frac{\mathrm{Gain} \cdot \mathrm{Bandwidth} \cdot OIP3}{P_{dc}}$$

in which gain is in linear scale, *OIP3* and P_{dc} are in Watt. Performance summary of state-of-the-art wideband distributed amplifiers published in the literature as well as of our prototype is presented in



(a)



(b)

Fig. 3.21. Measured *OIP3* of the linearized DA at (a) different backside temperature and (b) different bias variants.

Table 3.2. It can be seen that the $OIP3/P_{dc}$ ratio is typically highest in GaN technologies, follow by GaAs and InP, and the lowest is Silicon-based technologies.

3.5 Conclusion

A wideband linearization technique for stacked-HBT distributed amplifiers has been introduced and analyzed. The proposed concept is then experimentally illustrated in a dc – 90 GHz InP distributed amplifier. Compared to the conventional approach, the linearized DA exhibits significant linearity enhancement over a very wide bandwidth up to 85 GHz. The amplifier has a measured maximum P_{1dB} of

20.5 dBm and the highest OIP3 of 33 dBm. The OIP3 is improved by more than 5 dB from dc to 65 GHz. Moreover, the power and linearity enhancement is achieved with only a trade-off in small-signal gain and little increase in dc power dissipation.

Table 3.2. Comparison to Other State-of-The-Art Das

Ref	Gain (dB)	BW (GHz)	P_{sat} (dBm)	*OIP3* (dBm)	P_{dc} (W)	*OIP3*/P_{dc}	FOM	Tech.
[2]	12	dc-22	30.8	41	2.5	5	441	GaAs
[3]	10	0.1 - 45	30-33	28-41	5.2	2.4	345	GaN
[4]	13	1-25	20	33.5	0.9	2.5	267	GaN
[7]	12	0.1 - 8	35	48	4.4	11.4	363	GaN
[8]	7	dc - 61	NA	10.9	0.06	0.2	28	CMOS
[9]	7	dc - 70	10	16.3	0.12	0.4	56	CMOS
[10]	7.8	4 - 86	11	15.5	0.13	0.3	55	SOI
[11]	16	1.5 - 88	19.5	27.5	0.48	1.2	636	InP
[12]	11	dc - 90	12	15.5	0.21	0.2	54	SOI
[32]	22	dc - 65	10	NA	0.1	NA	NA	CMOS
[52]	8.6	2 - 41	7.8	16.8	0.02	2.4	251	CMOS
[53]	14	dc – 73	3.2	NR	0.084	NA	NA	CMOS
Conv. DA	**14**	**dc - 75**	**20**	**28**	**0.4**	**1.6**	**593**	**InP**
Lin. DA	**10.5**	**dc - 90**	**22**	**33**	**0.4**	**5**	**1504**	**InP**

3.6 Reference

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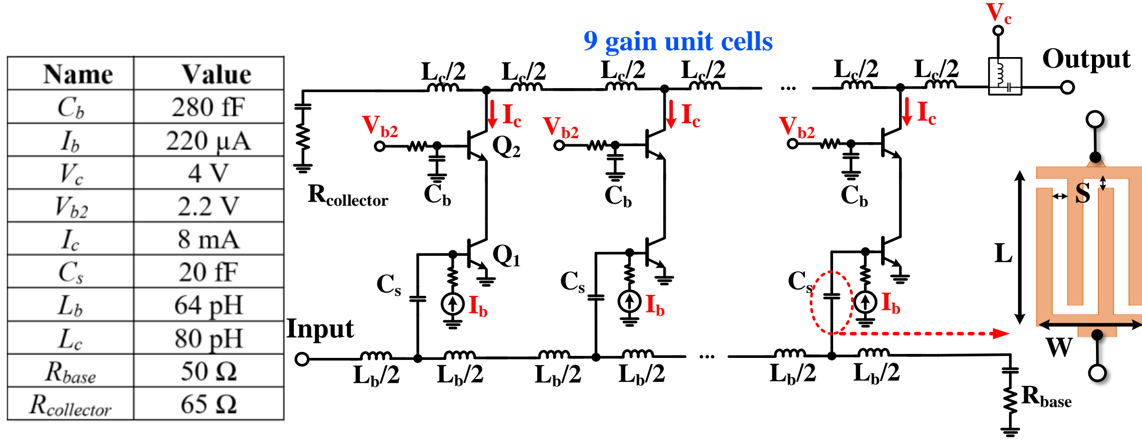
Chapter 4. 160 GHz Wideband, High Output Power Distributed Amplifiers

Distributed amplifiers (DAs) have proven to offer ultra-wideband, flat gain performance at millimeter-wave frequencies. Moreover, DAs can provide low input and output return losses spontaneously thanks to the artificial transmission line structure [1]-[12]. Theoretically, the upper operating frequency of a DA is limit by either the cut-off frequencies of active devices (f_{max}) or passive transmission lines. In recent years, f_{max} of MMIC processes has been improved drastically and exceeded the cut-off frequencies of on-chip transmission lines. Hence, the input and output transmission lines are the main bottlenecks of a DA bandwidth. In particular, the input line is proved to have a higher impact on the DA cut-off frequency due to higher input capacitance and the base resistance of heterojunction bipolar transistor (HBT) devices [2].

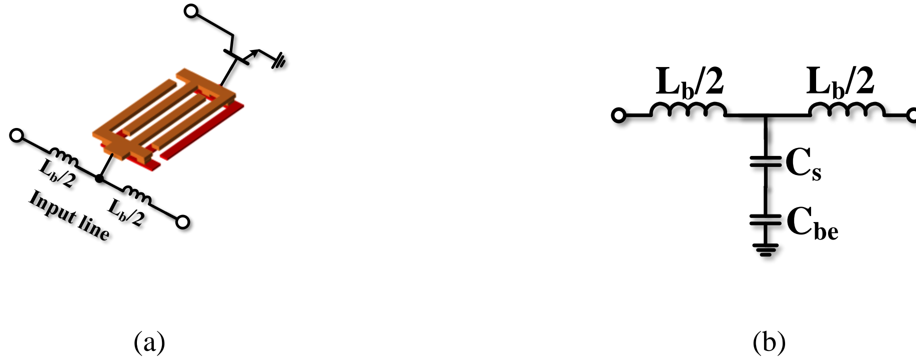
In this chapter, we present the design and development of a distributed amplifier using 3-D interdigital capacitors. Notably, the amplifier employs an interdigitated capacitor at the base of each unit gain cell to maintain a constant input characteristic impedance over the entire DA bandwidth. The amplifier is designed and fabricated in an Indium Phosphide (InP) HBT process to verify the concept. The measured results demonstrate an average gain of 10.5 dB with a 3-dB bandwidth from 1 to 160 GHz, and a low input return loss at high frequencies up to 160 GHz. To the best of the authors' knowledge, this is the first time interdigital capacitors are used to improve the input return loss of a distributed amplifier.

In addition, we present an efficient, high output power double-stacked hetero-junction bipolar transistor (HBT) uniform distributed amplifier with optimized component layouts. The parallel/series metal-insulator-metal (MIM) capacitor configuration is proposed to realize the small input coupling capacitors. Such configuration helps the DA achieve wideband performance while maintaining high reliability and reducing the sensitivity to process variations. The DA is designed and fabricated in an Indium Phosphide (InP) process. The amplifier covers a 3-dB bandwidth from 1 - 150 GHz with an average gain of 11.5 dB. The amplifier exhibits a $\pm$ 15 ps deviation in group delay within the passband. The maximum



Name	Value
C_b	280 fF
I_b	220 µA
V_c	4 V
V_{b2}	2.2 V
I_c	8 mA
C_s	20 fF
L_b	64 pH
L_c	80 pH
R_{base}	50 Ω
$R_{collector}$	65 Ω

Fig. 4.1.1. Schematic diagram of the proposed interdigital capacitors distributed amplifier.



(a)

(b)

Fig. 4.1.2. (a) Proposed 3-D interdigital capacitor, and (b) approximated equivalent T-model of a one-section input transmission line.

saturated output power (P_{sat}) is 18.3 dBm at 50 GHz. At 100 GHz, the amplifier achieves 15.4 dBm P_{sat} with a 10 % maximum *PAE*.

4.1 Proposed 3-D Interdigital Capacitor Distributed amplifier

4.2.1 Circuit Design

Fig. 4.1.1 shows the proposed capacitive coupling DA schematic diagram using the interdigital capacitor C_S. To maximize the bandwidth, the value of C_S can be much smaller than the input capacitance of the unit gain cell. The capacitance is usually on the order of tens of fF. Consequently, the effective capacitance at the input node is dominated by C_S [1], [3]. To realize such small capacitance, either the area

of the MIM capacitor must be reduced, or the dielectric thickness between the metallic plates must be increased.

Therefore, the limits of the process dictate the minimum capacitance value. Hence, we propose the use of 3-D interdigital capacitors for a more robust, high-performance design.

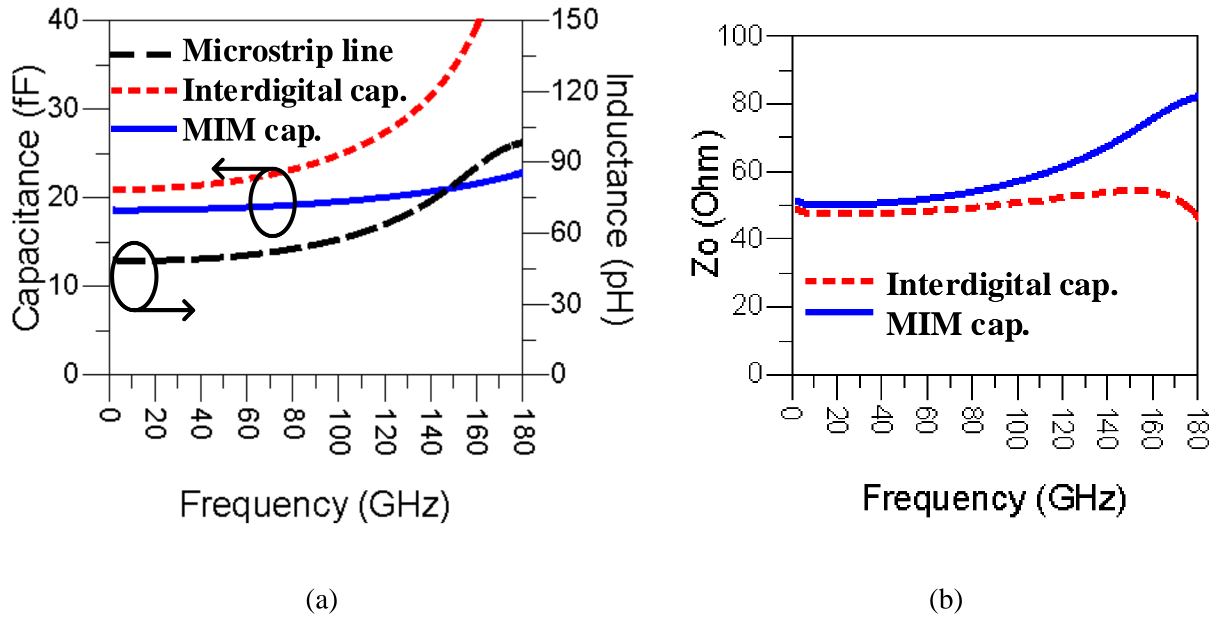
To balance the trade-off between gain and bandwidth in our design, input coupling capacitor C_s is chosen to be 20 fF. To realize 20 fF capacitance in a compact area, two parallel interdigital capacitors are designed using two consecutive metal layers, forming a 3-D interdigitated structure. Fig. 4.1.2(a) presents a one-section of the input artificial transmission line using the proposed capacitor. The simplified one-section T-model of the transmission line is illustrated in Fig. 4.1.2(b), where C_{be} is the base-emitter capacitance of the device. When $C_s << C_{be}$, the characteristic impedance Z_0 and Bragg cut-off frequency f_c of the input artificial transmission line in Fig. 4.1.2(b) are calculated by [1]:

$$Z_0 \approx \sqrt{\frac{L_b}{C_s}} \tag{4.1}$$

$$f_c \approx \frac{1}{\pi\sqrt{L_b C_s}}. \tag{4.2}$$

In practice, the operating frequency of the amplifier is much lower than the cut-off frequency f_c given in (4.2). In addition, the base resistance of the HBT device deteriorates the signal transmission at high frequencies. The base resistance, along with the input capacitance of the device, establish a lower cut-off frequency. Another critical limiting factor is the self-resonant frequency (SRF) of transmission line inductors L_b and L_c.

Due to the SRF of the transmission line inductor, the inductance of L_b is not constant over a wide range of frequencies. In particular, the inductance value increases sharply when the frequency approaches the SRF. On the contrary, MIM capacitors usually have a much higher SRF than that ofa inductors. MIM capacitance is relatively constant over a large frequency range. Therefore, the rise of inductance L_b leads to



(a) (b)

Fig. 4.1.3. Simulated (a) Capacitance and inductance of the proposed 3-D interdigital capacitor, MIM capacitor, and a microstrip line inductor. (b) Characteristic impedance two nine-section T-model transmission lines.

increasing characteristic impedance in (4.1) at high frequencies, hence, degrades the input return loss and lowers the amplifier's gain. To mitigate the problem, the 3-D interdigital capacitor at the input is proposed in our design. The proposed capacitor has the following benefits over the conventional MIM capacitor:

1. An interdigital capacitor can be used to realize small capacitance with high precisions and low susceptibility to process variations.

2. A positive slope of capacitance with respect to frequency can be realized and is governed by the length L of the capacitor [12]. This slope compensates for the inductance slope of the transmission line and improves the return loss bandwidth.

Fig. 4.1.3(a) illustrates the simulated frequency response of the microstrip line inductor, the MIM capacitor, and the proposed interdigital capacitor. The inductance of the transmission line is 50 pH, and the capacitance of both capacitors is 20 fF. The 3-D interdigital capacitor consists of two parallel capacitors

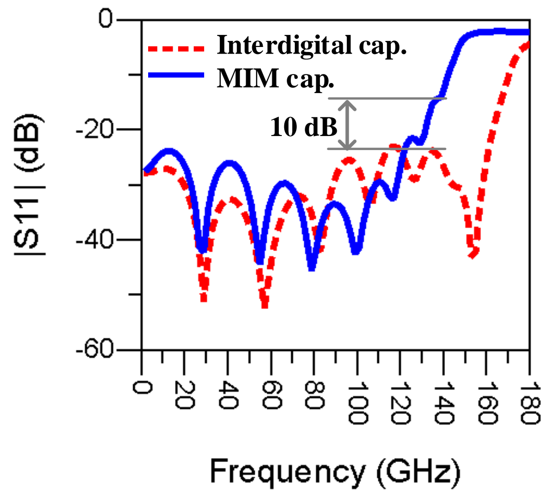


Fig. 4.1.4. Input return loss of the nine-section transmission lines using different capacitors.

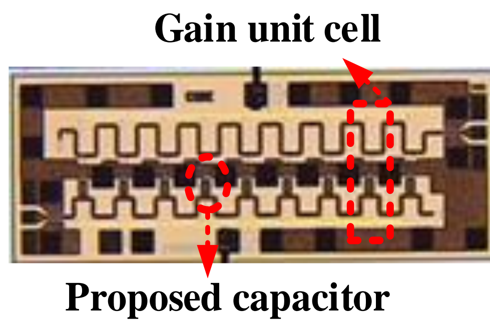


Fig. 4.1.5. Microphotograph of the proposed 3-D interdigital capacitor distributed amplifier (1.6 mm × 0.8 mm, including all pads).

with an approximate capacitance of 10 fF formed on two consecutive metal layers. Each capacitor has four fingers with a width (W) of 30 μm, length (L) of 50 μm, and interdigital spacing (S) of 3 μm as indicated in Fig. 4.1.1. The inductor and the capacitor values are designed to satisfy $Z_0 = 50\ \Omega$ in (1) at 1 GHz.

As illustrated in Fig. 4.1.3(a), the inductance slope of the microstrip inductor is much steeper than that of the MIM capacitance. In fact, the inductance of the microstrip line is almost doubled at 160 GHz. Hence, if capacitance C_s in (4.1) remains constant, characteristic impedance Z_0 will increase significantly at high frequencies. On the other hand, the interdigital capacitor can be designed to have a similar positive

slope as that of the inductor to maintain constant Z_o with respect to frequency, as shown in Fig. 4.1.3(b). The width, length, spacing, and the number of fingers of the capacitor layout can be designed independently [12] to achieve the required capacitance value and slope over frequency. The capacitance slope of C_s needs to be optimized

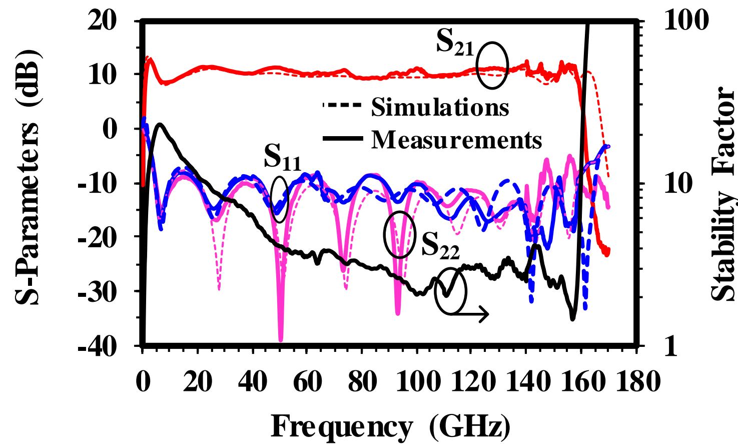
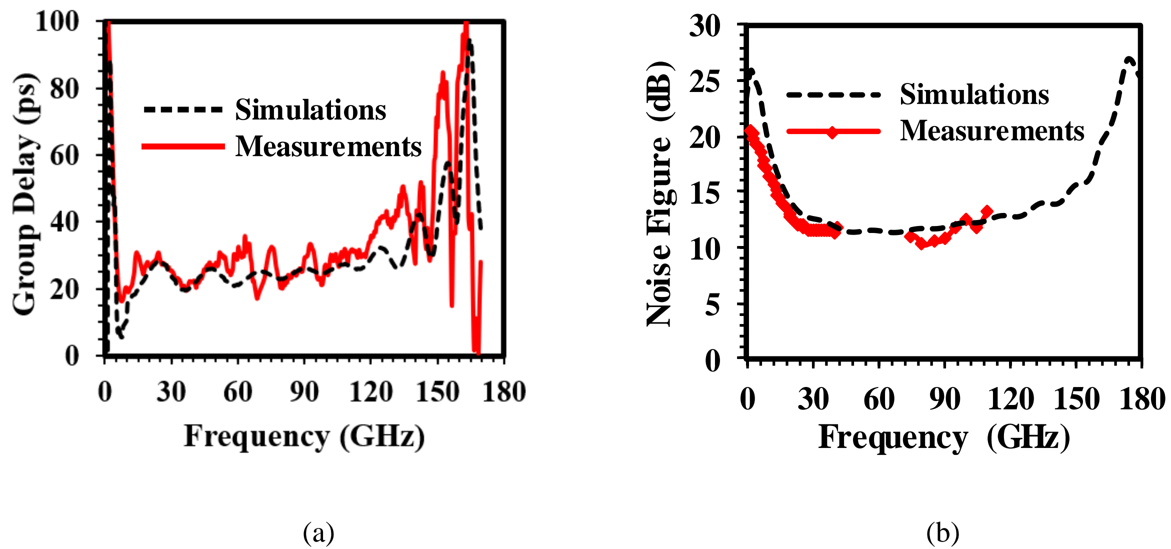


Fig. 4.1.6. Measured and simulated small-signal S-parameters.



(a)

(b)

Fig. 4.1.7. Measured and simulated (a) group delay (ps), and (b) noise figure (dB) of the proposed DA.

such that as the capacitance increases, the cut-off frequency in (2) is still higher than the cut-off frequency of the inductor L_b.

Fig. 4.1.3(b) demonstrates the characteristic impedance of a nine-section T-model transmission line using the proposed 3-D interdigital capacitor and the MIM capacitor configurations with the microstrip line inductor. The characteristic impedance of the transmission line using MIM capacitors is only flat up to 110 GHz. Meanwhile, the transmission line using the proposed design can maintain a relatively constant impedance up to 170 GHz, extending the matching condition up to the cut-off frequency of the microstrip line inductor.

Fig. 4.1.4 illustrates the simulated return loss S_{11} of two artificial transmission lines, both of which consist of nine sections using the proposed 3-D interdigital capacitors and the conventional MIM capacitors. At low frequency, the return losses between the two implementations are not much different. As the frequency reaches the cut-off frequency of the transmission line inductor, the return loss using the MIM capacitor degrades quickly while the proposed capacitor maintains the matching condition. Quantitatively, the proposed capacitor improves the input return loss range from 135 GHz to 170 GHz by a minimum difference of 10 dB.

4.2.2 Experimental Results

To verify the concept, a uniform DA using the proposed interdigital coupling capacitor is designed and fabricated in an InP HBT process [3], [4]. The complete schematic diagram and bias conditions are shown in Fig. 4.1.1. Current I_b and voltage V_{b2} are biased through a 1 kΩ resistor. To achieve a high output power, the double-stacked-HBT topology is used for an individual gain cell to double voltage swing and output power. The amplifier employs nine-unit gain cells with coupling capacitors $C_s = 20$ fF shown in Fig. 4.1.2(a). Both input and output transmission lines are realized using inductive microstrip lines. The input inductance L_b is optimized to 64 pH considering the parasitic of the device and unwanted couplings. Fig. 4.1.5 illustrates the microphotograph of the DA. The die size is 1.6 mm × 0.8 mm, including all RF and dc pads. The collector bias is provided through an external bias-tee.

The measured small-signal parameters are shown in Fig. 4.1.6. The DA achieves an average gain of 10.5 dB with a 3-dB bandwidth covering from 1 to 160 GHz. The amplifier demonstrates well matching

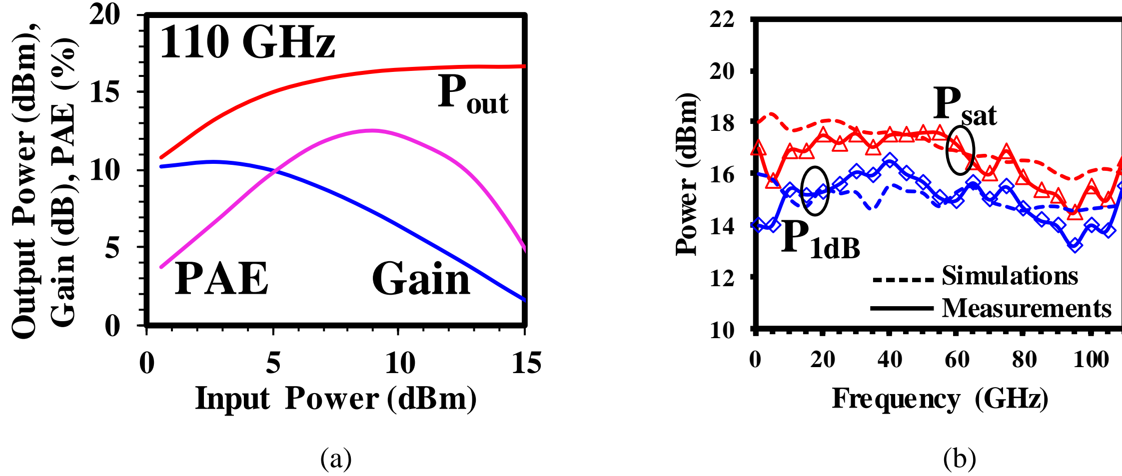


Fig. 4.1.8. (a) Measured large-signal measurement at 110 GHz, and (b) measured saturated output power P_{sat} and 1-dB compression power P_{1dB}.

conditions at the input and output for the entire band. Specifically, the input return loss at high frequencies above 90 GHz maintains well below -10 dB. The gain of the DA maintains approximately at 10.5 dB up to 159 GHz before quickly rolls off due to the high-order transmission lines. The measurements agree well with the simulated results up to 160 GHz. The measured bandwidth is 5 GHz lower than simulation due to the device model inaccuracy at a very high frequency. The DA is unconditionally stable with a minimum stability factor, k, of 1.5 at 157 GHz and $|\Delta| < 1$ for the entire frequency band. The amplifier draws a total collector current of 72 mA in small-signal conditions. Fig. 4.1.7(a) illustrates the measured and simulated group delay of the DA in pico-second. The amplifier achieves a maximum phase deviation of ±12 ps from 5 to 145 GHz. Fig. 4.1.7(b) presents the noise performance of the DA. The simulated noise figure (*NF*) is validated from 1 – 40 GHz and 75 – 110 GHz. The minimum *NF* achievable is 10.1 dB.

Fig. 4.1.8(a) depicts the large-signal measurement of the proposed DA at 110 GHz. The DA achieves a maximum saturated output power (P_{sat}) of 16.5 dBm with a 1-dB compression output power (P_{1dB}) of 15.5 dBm. The maximum power-added efficiency (*PAE*) is 12.5 %. Fig. 4.1.8(b) demonstrates P_{1dB} and P_{sat} across the frequencies from 1 to 110 GHz. The circuit provides a maximum saturated output power (P_{sat}) of 17.8 dBm at 55 GHz. The corresponding 1-dB compression output power (P_{1dB}) is 15 dBm.

Table 4.1. Comparison to State-of-The-Art Distributed Amplifiers

Reference	Technology	Gain (dB)	BW (GHz)	f_{max} (GHz)	NF (dB)	P_{sat} (dBm)*	P_{dc} (mW)**	PAE (%)
[5]	InP	13	dc-140	400	-	11.5@110GHz	129	8@110GHz
[6]	InP	12	dc-175	530	8	13 @20GHz	180	6@145GHz
[7]	InP	13.5	5-207	650	-	3.7 @100GHz	210	-
[8]	SiGe	20	10-170	450	-	13.5 @135GHz	560	1.4@135GHz
[9]	SiGe	8.5	dc-135	500	5.3	11 @20GHz	99	8@20GHz
[10]	GaAs	11	dc-110	500	2.5	11 @75GHz	425	-
[11]	CMOS	16	1.5-103	-	4.1	22@5GHz	485	10@60GHz
This work	**InP**	**10.5**	**1-160**	**390**	**10.1**	**17.8 @55GHz**	**288**	**12.5@110GHz**

*Maximum reported saturated power **Small-signal dc consumption

The minimum achievable P_{sat} and P_{1dB} up to 110 GHz is 14.6 dBm and 13.5 dBm, respectively. These results

are consistent with InP technologies that have high output power densities [13], [14]. The performance of the proposed DA is summarized and compared with other state-of-the-art works in Table 4.1. Only [11] shows a higher output power with trade-offs in bandwidth and efficiency at high frequencies.

4.2.3 Conclusion

A nine-cell double-stacked distributed amplifier using 3-D interdigital capacitors in an InP HBT process is presented. The proposed capacitor improves matching conditions at high frequencies, which makes the amplifier more appealing to wideband, high-frequency applications. The fabricated DA exhibits a 10.5 dB small-signal gain and good input and output return losses from 1 to 160 GHz. The DA delivers a maximum P_{sat} of 17.8 dBm at 55 GHz with a corresponding P_{1dB} of 15 dBm.

4.2.4 Reference

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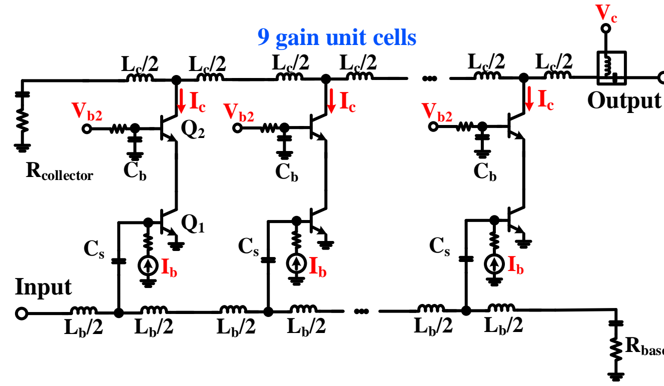
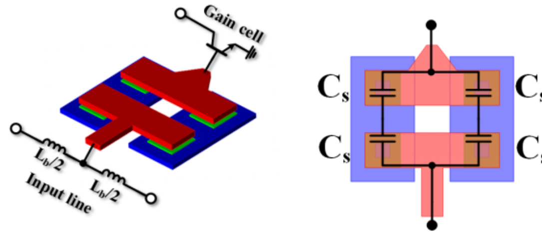


(a)



(b)

Fig. 4.2.1 (a) Schematic diagram of the double-stacked distributed amplifier and (b) layout realization of the parallel/series input coupling capacitor C_s.

Table 4.2. Design Parameters and Biasing Condition

Name	Value
C_b	280 fF
I_b	220 µA
V_c	4 V
V_{b2}	2 V
I_c	8 mA
C_s	20 fF
L_b	60 pH
L_c	80 pH
R_{base}	50 Ω
$R_{collector}$	60 Ω

4.2 A Double-stacked HBT 1-150 GHz Distributed Amplifier

4.2.1 Circuit Design

Fig. 4.2.1(a) shows the circuit schematic diagram of the double-stacked HBT distributed amplifier with input coupling capacitors. The double-stacked topology increases the output voltage swing by two-fold while still maintaining a safe operation region for both transistors. The device size is identical, 5-µm emitter length, for transistors Q_1 and Q_2. The base capacitor C_b of the transistor Q_2 is laid out close to the

base terminal of the device to reduce any parasitic inductances that would degrade the stability of the amplifier. Nine unit gain cells are employed to achieve the required gain. According to simulations, adding more than nine gain stages does not further increase the gain due to the losses of the artificial transmission lines [2].

The design is also optimized to achieve maximum small-signal bandwidth. This bandwidth optimization is achieved through a small coupling capacitor C_s = 20 fF. Such a small capacitor is realized using an innovative parallel/series topology. In particular, four metal-insulator-metal (MIM) capacitors of the same size are placed in series and parallel configuration as shown in Fig. 4.2.1(b). With the proposed capacitor layout, the sensitivity of the capacitance value with process variations is reduced since the total area of the capacitor is increased without increasing the capacitance. Also, this parallel/series structure is particularly useful for high-power applications. Specifically, the series connection creates a voltage division among the capacitors, which reduces the applied voltage across the individual capacitor. Therefore, this technique helps to increase the reliability of the capacitor under large-signal operations.

The input and output lines are realized using meandered microstrip structures. Since the input and output capacitances of the device are different, the input inductance L_b and output inductance L_c are valued at 60 pH and 80 pH, respectively. Both input and output transmission line cut-off frequencies exceed 180 GHz. The termination resistance at two ends of the input and output lines are R_{base} = 50 Ω and $R_{collector}$ = 60 Ω, respectively. The bias current, I_b, and the base voltage of the stacked-transistor Q_2, V_{b2}, are supplied through a 1 kΩ resistor. The collector is biased through an external bias-tee. The designed component values are summarized in Table 4.2. The DA is fabricated in an InP HBT process with a transition frequency f_T of 290 GHz and a maximum frequency f_{max} of 390 GHz. The microphotograph of the die is shown in Fig. 4.2.2. The total chip size is 1.9 mm × 0.8 mm, including all pads. Two dc pads are placed on top and bottom of the chip with a small on-chip by-pass capacitor for V_{b2} and I_b, respectively.

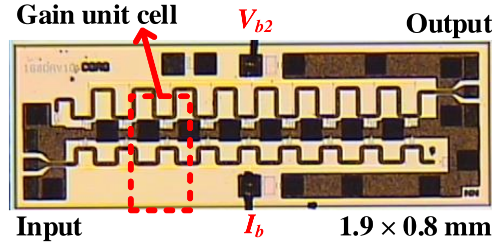


Fig. 4.2.2. Die photograph of the nine-stage double-stacked distributed amplifier (1.9 mm × 0.8 mm including all pads).

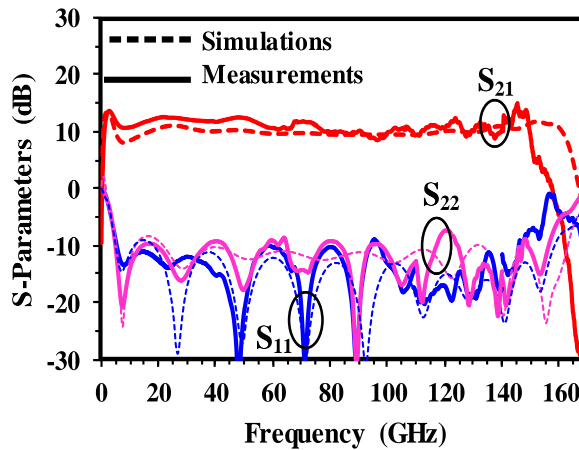


Fig. 4.2.3. Measured and simulated small-signal S-parameters.

4.2.2 Experimental Results

The circuit is measured using die probing on a probe station. To facilitate the measurements, a die is assembled onto a printed circuit board (PCB). A 500-pF by-pass single layer capacitor is mounted off-chip and wire bonded to each dc pad. The dc supplies are probed on the off-chip by-pass capacitors. The DA is biased with the base current I_b for each cell is 220 µA, and the collector voltage V_c of 4 V. The detailed biasing condition of the circuit is summarized in Table 4.2.

Fig. 4.2.3 illustrates the small-signal measurements overlaying with the simulations. The average small-signal gain is 11.5 dB covering a 3-dB bandwidth from 1 GHz to 150 GHz. The input return loss is well match up to 150 GHz with S_{11} is below -10 dB. The output reflection is also below -10 dB, with a peak

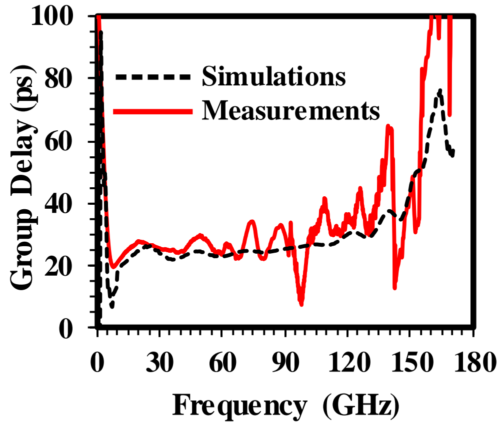


Fig. 4.2.4. Measured and simulated group delay (ps) of the proposed DA.

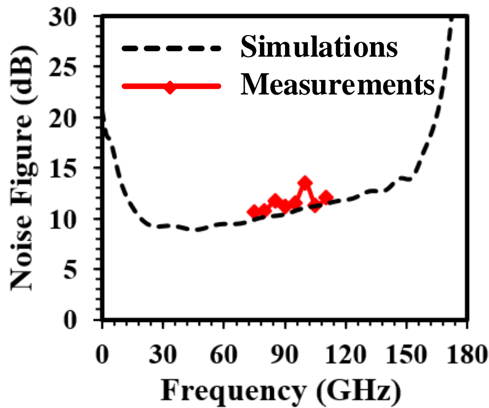


Fig. 4.2.5. Measured and simulated noise figure (dB) of the proposed DA.

of -8 dB at 120 GHz. The gain discrepancy between the simulation and measurement might be due to the process variations of the current gain β. Overall, the simulations closely predict the measurement data. The distributed amplifier consumes approximately 290 mW dc power at small-signal conditions. The measured and simulated group delay in picoseconds (ps) from dc to 170 GHz are presented in Fig. 4.2.4. The amplifier achieves a maximum deviation of ± 15 ps from 2 to 140 GHz. Fig. 4.2.5 illustrates the simulated and measured noise figure (NF) of the proposed amplifier. The DA achieves a minimum NF of 10.3 dB at 75 GHz.

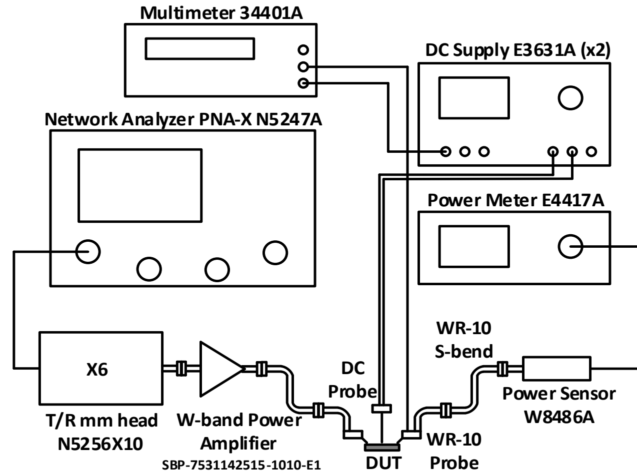


Fig. 4.2.6. W-band power measurement test setup.

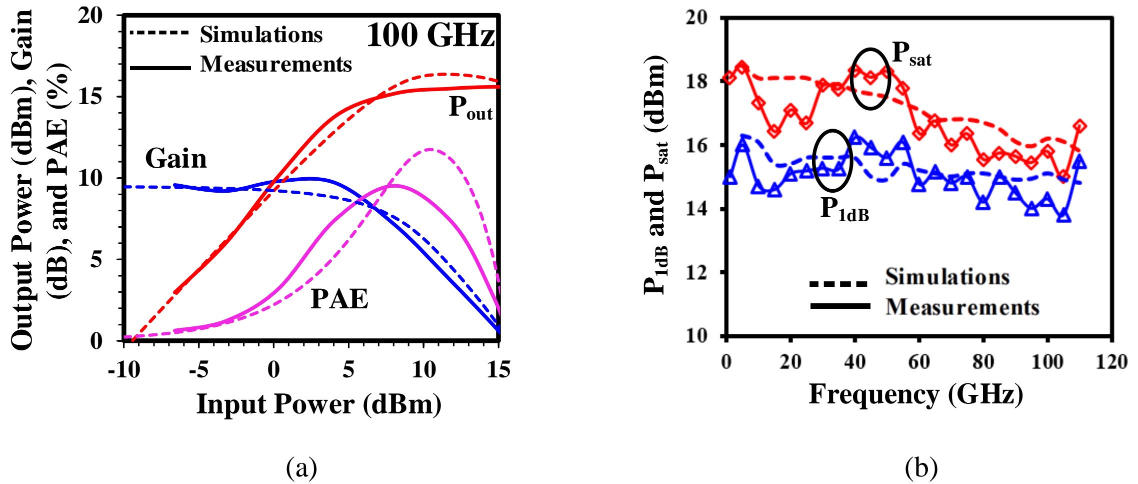


Fig. 4.2.7. Measured and simulated of (a) P_{out}, gain, and *PAE* at 100 GHz and (b) P_{sat}, P_{1dB}, and PAE_{max} over frequencies.

Fig. 4.2.6 illustrates the test setup for large-signal measurement at W-band. The W-band signal is generated using the PNA-X with a frequency multiplier and amplified by a commercial W-band power amplifier. Fig. 4.2.7 depicts the large-signal measurements of the proposed distributed amplifier. Fig. 4.2.7(a) shows the power sweep performed at 100 GHz. The saturated output power (P_{sat}) is 15.4 dBm

Table 4.3. Comparison to State-of-The-Art DAs

Ref.	**[3]**	**[5]**	**[4]**	**[13]**	**[9]**	**[11]**	**This work**
Tech.	GaAs	GaN	SiGe	SiGe	InP	InP	**InP**
Gain (dB)	11	7.3	8.5	14.5	10.5	10.5	**11.5**
BW (GHz)	dc-110	5-125	1-170	52-142	1-160	60-145	**1-150**
f_T/f_{max} (GHz)	380/500	200/400	300/500	-/210	290/390	290/390	**290/390**
NF (dB)	2.5	6	3	10	10.1	10.5	**10.3**
P_{sat} (dBm)	11 @75GHz	20 @20GHz	7.5 @50GHz	1.6 @75GHz	17.8 @55GHz	20.9 @75GHz	**18.3 @50GHz**
P_{dc} (mW)	425	448	108	103	288	440	**290**
PAE (%)	-	6.5 @20GHz	4.9 @50GHz	-	12.5 @110GHz	19.2 @110GHz	**10 @100GHz**

with a 1 dB compression power (P_{1dB}) of 14.3 dBm. The maximum power-added efficiency (*PAE*) is 10%. The measured results correlate well with the simulations.

Fig. 4.2.7(b) illustrate the P_{sat} and P_{1dB} of the proposed DA over frequencies from 1 GHz to 110 GHz with the step of 5 GHz. Overall, the DA achieves a saturated output power of 15 - 18.3 dBm. The data above 110 GHz is unavailable due to the lack of sufficient input power source. The maximum P_{sat} is 18.3 dBm at 50 GHz, with the corresponding P_{1dB} of 15.4 dBm. As the frequency increases, the output power and PAE decrease gradually but still maintain above 15 dBm P_{sat}. Table 4.3 summarizes the state-of-the-art distributed amplifiers from W-band (110 GHz) and above.

4.2.3 Conclusion

A high output power, high efficiency nine-cell double-stacked uniform distributed amplifier in an InP HBT process is presented. The DA exhibits an average 11.5 dB power gain with a 3-dB bandwidth from 1 – 150 GHz and a noise figure of 10.3 dB. The maximum achievable output power is 18.3 dBm at 50 GHz, with the corresponding P_{1dB} of 15.4 dBm. The amplifier obtains a 10 % PAE at 100 GHz.

4.2.4 Reference

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Chapter 5. A Wideband SiGe Power Amplifier Using Modified Triple Stacked-HBT Cell

The demand for high-speed optical communication systems has been increasing significantly [1]. Fig. 5.1 shows a block diagram of an optical transmitter front-end with an external modulator. An optical transmitter configuration typically includes an external Mach-Zehnder modulator (MZM), which requires a large driving voltage of more than 3 V peak-to-peak differential (V_{ppd}) with linearity less than 6 % THD [2]. Such a high voltage swing at high speed put a tremendous challenge on the amplifier design. Therefore, driver amplifiers with high gain and high output voltage swings have become critical components in the system [2]-[6].

Optical driver amplifiers have been demonstrated in different processes, including Indium Phosphide (InP) [3], Gallium Arsenide (GaAs) [4], and Gallium Nitride (GaN) [5], which are costly and difficult to integrate with the digital control components. On the other hand, Silicon Germanium (SiGe) BiCMOS Heterojunction Bipolar Transistor (HBT) technology is a great candidate since the process can offer both high-frequency performance and a high level of integration [2], [6], [7]. However, the low breakdown voltage of Silicon processes has become an impediment in designing high output voltage swing amplifiers. To overcome this challenge, stacking structures have been intensively employed in power amplifiers under a common emitter/source configuration [8]-[12]. Specifically, cascode or double-stacked structures are mostly implemented in optical drivers to date [2], [6], [7], [13], [14].

In this chapter, we demonstrate the design and implementation of a high gain, high output voltage swing differential linear amplifier in a SiGe BiCMOS HBT technology using an innovative modified triple-stacked HBT topology with an emitter degeneration network. Also, a wideband output matching network is employed to improve the output return loss. The amplifier has a measured voltage gain of 13.2 dB with a 3 dB bandwidth of 53 GHz. A measured output return loss below -10 dB is achieved from dc up to 40 GHz. At 25°C, the amplifier provides a measured 4 V_{ppd} output voltage swing with a THD of 1.6 % at

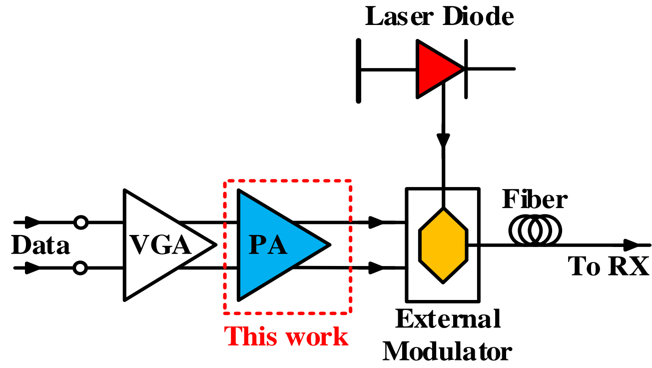

Fig. 5.1. Block diagram of a typical optical transmitter.

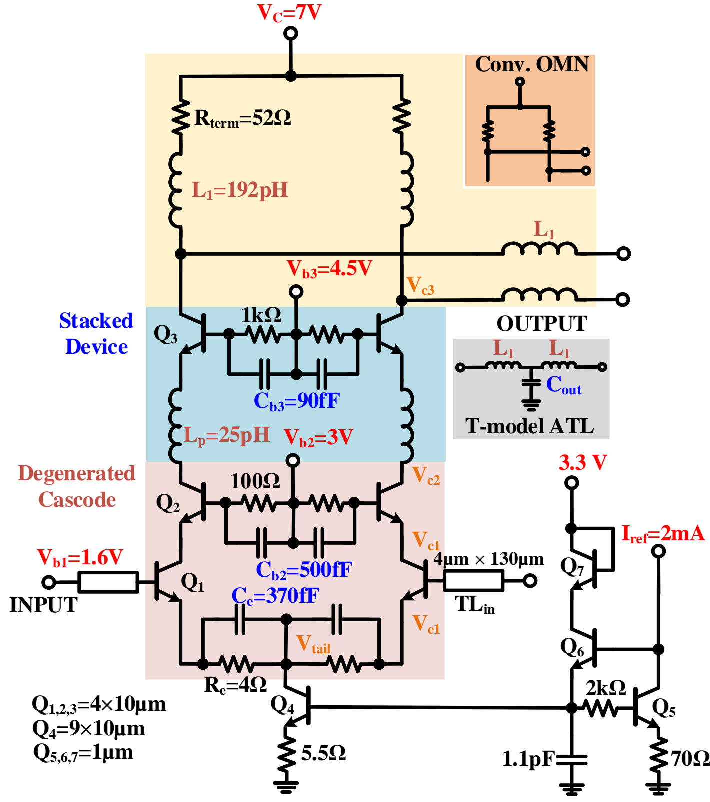

Fig. 5.2. Circuit diagram of the proposed amplifier.

1 GHz and a THD of 3.3 % at 10 GHz. To the best of the authors' knowledge, this is the first time a new triple-stacked HBT with an emitter degeneration network is implemented to achieve a wideband, highly linear driver amplifier for optical modulators.

5.1 Circuit Design and Implementation

Fig. 5.2 illustrates the schematic diagram of the proposed amplifier. A modified triple-stacked HBT with emitter degeneration is proposed to achieve > 4 V_{ppd} at the output. Simultaneously, the collector-to-emitter (V_{ce}) of each transistor is maintained below the breakdown voltage (BV_{CEO}) of the transistor. The key differences between the proposed topology compared to the traditional stacked-HBT are:

1. A parallel resistor/capacitor (RC) of $R_e = 4\ \Omega$ and $C_e = 370$ fF degeneration network is utilized to improve linearity instead of a common emitter structure.

2. Transistors Q_1 and Q_2 are connected in a cascode configuration instead of a conventional stacked structure to reduce V_{ce} across transistor Q_1. Transistor Q_3 is stacked on top of the cascode structure.

In the traditional stacked-HBT topology [8]-[12], the bottom transistor Q_1 is connected in a common-emitter configuration, which makes the emitter voltage of Q_1 remains constant. However, by using an RC degeneration network, a voltage swing V_{e1} at the emitter of the transistor Q_1 is introduced and is out-of-phase with the collector voltage V_{c1}. This out-of-phase characteristic between the collector and emitter voltage enlarges V_{ce} of the bottom transistor Q_1. Therefore, a large voltage swing at the collector of Q_1 in the conventional triple-stacked structure will push Q_1 into the breakdown, while the V_{ce} across Q_2 is much smaller than its maximum voltage swing, as shown in Fig. 5.3(a).

In this work, transistor Q_2 is connected in a cascode topology by using a larger base capacitor C_{b2} to reduce the voltage swing V_{c1} at the collector of Q_1, therefore, keeping Q_1 in the safe region and maximize the performance for Q_2. Transistor Q_3 is stacked on top of the degenerated cascode structure with a finite impedance at the base to equally divide the voltage swing among the transistors, as shown in Fig. 5.3(b). The base capacitors C_{b2} is 500 fF, and C_{b3} is 90 fF. The simulated self-resonant frequencies, including the interconnections of C_{b2} and C_{b3}, are 75 GHz and 155 GHz, respectively.

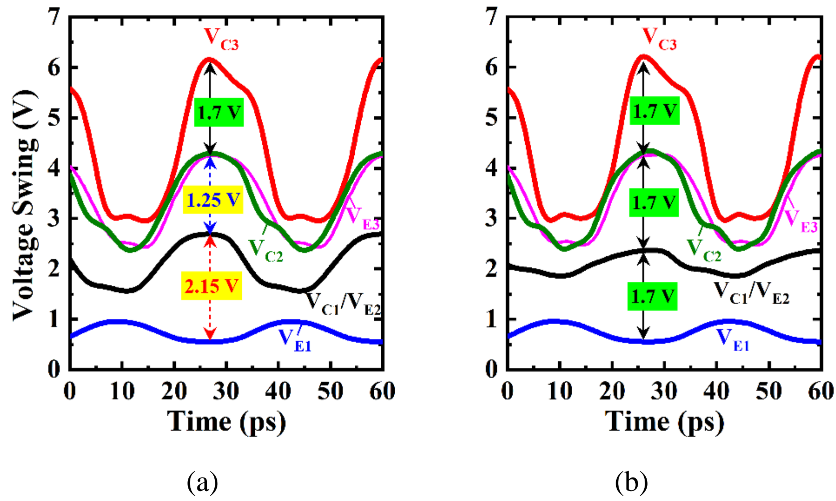

Fig. 5.3. Simulated voltage swings of (a) the conventional triple-stacked and (b) the proposed modified stacked topology at 30 GHz.

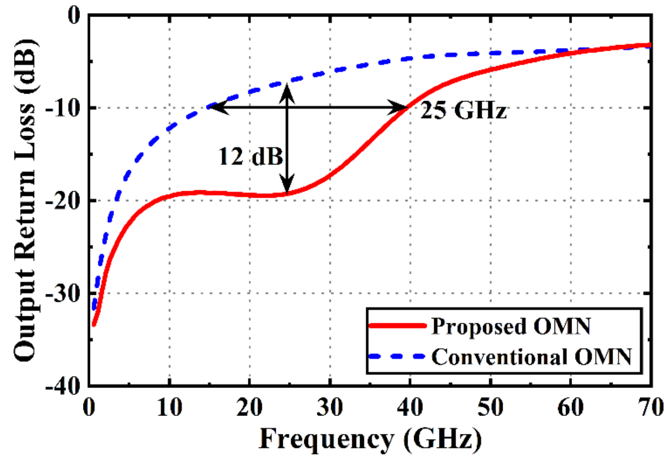

Fig. 5.4. Simulated output return loss using the proposed output matching network (OMN) and the conventional approach.

A 50-pH peaking inductor L_p is employed at an intermediate node between Q_2 and Q_3 to provide a positive gain slope and maintain the voltage phase alignment at each transistors' collector terminal. Fig. 5.3 illustrates the simulated voltage at each transistor at 30 GHz at saturated output power. The collector-emitter voltages across each transistor are equal and below the breakdown voltage of our process. The

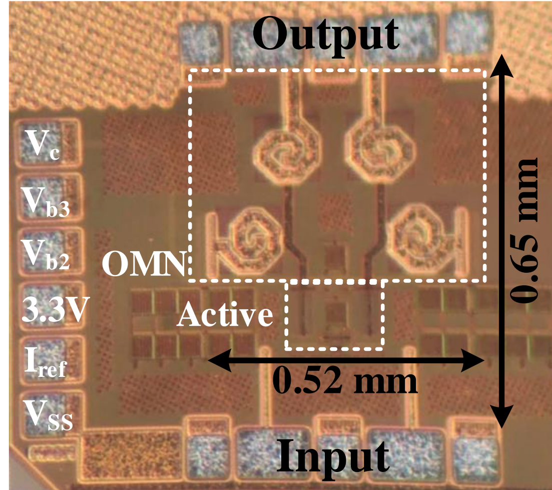

Fig. 5.5. Microphotograph of the amplifier. The core amplifier size is 0.52×0.65 mm^2

collector-base voltage can be calculated as $V_{cb} = V_{ce} - V_{be}$ with $V_{be} \approx 0.9$ V for the HBT process. Since the collector-base breakdown voltage BV_{CBO} is usually greater than the collector-emitter breakdown voltage BV_{CEO}, in most cases, the collector-emitter junction breakdown is more critical.

The amplifier is matched to a 100 Ω differential at the output while the input is connected directly to the signal pads. A single-section T-model LC artificial transmission line is employed since an output matching condition over a wide bandwidth is desirable. The impedance of the transmission line can be calculated as $Z_o = \sqrt{2 \cdot L_1/C_{out}}$, where C_{out} is the effective output capacitance of the gain cell. The output parasitic capacitor of the amplifier, along with two series inductors $L_1 = 200$ pH, creates a wideband matching condition, as shown in Fig. 5.4. The output inductors are realized using spiral coil topology on top metal with sufficient spacing to prevent unwanted couplings.

The base of Q_1 is biased through dc coupling at the input. The base bias voltages V_{b2} and V_{b3} are connected through a 100 Ω and 1 kΩ, respectively. A small resistor is used at the base of transistor Q_2 instead of connecting directly to the voltage source is to stabilize the amplifier. The tail current source is realized using a degenerated current mirror with a β-helper. The total tail current is 90 mA. The collector

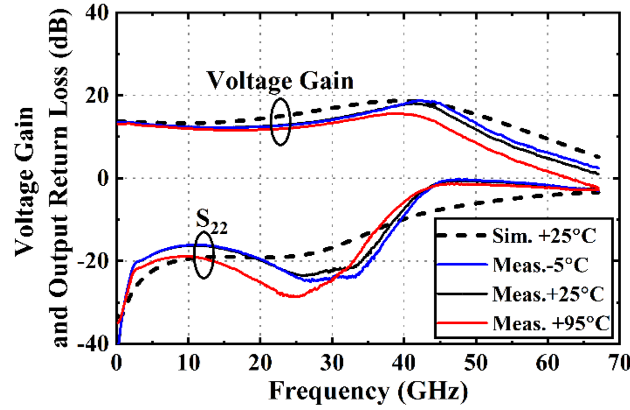

Fig. 5.6. Measured voltage gain and output return loss over temperature.

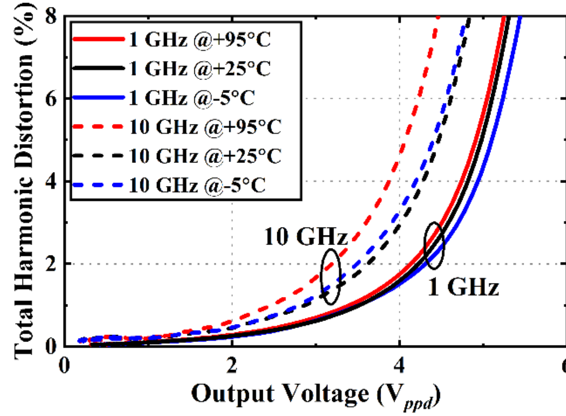

Fig. 5.7. Measured large-signal performance of the proposed power amplifier.

supply voltage is provided through the terminated resistors to eliminate a bulky and high-cost off-chip wideband RF choke.

5.2 Experimental Results

The amplifier is fabricated in a 90 nm SiGe BiCMOS process with an f_T/f_{max} of 300/360 GHz. The high-speed device has a breakdown voltage BV_{CEO} of 1.7 V. The amplifier is biased with 90 mA tail current and a 7 V collector supply through terminated resistors. The bases of the transistors Q_1, Q_2, and Q_3 are biased at 1.6 V, 3 V, and 4.5 V, accordingly. The device size is chosen to balance between f_T and linearity

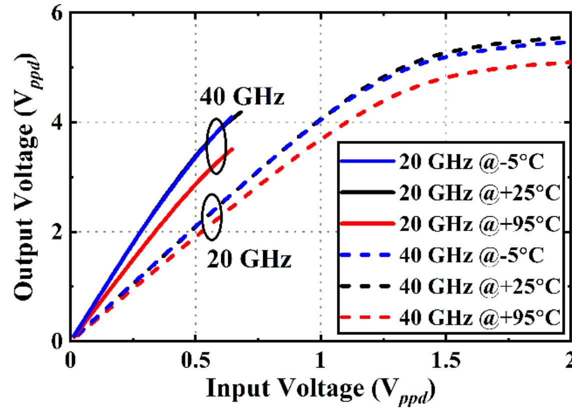

Fig. 5.8. Measured differential output voltage swing of the proposed power amplifier with the swept differential input voltage.

of the amplifier. The final size is 4 × 10 μm for each transistor at 1.13mA/μm current density. The current reference I_{ref} is 2 mA and is supplied through an off-chip resistor. The total power dissipation is approximately 630 mW. The chip microphotograph is shown in Fig. 5.5. The input and output are connected to 125 μm pitch GSGSG pads. The dc pads are 100 μm separated. The core amplifier is 0.52 × 0.65 mm^{2,} and the total chip size, including all pads, is 1 × 0.84 mm^2.

Small-signal measurements are performed using a four-port network analyzer N5247A PNA-X. Differential S-parameters characterization is conducted up to 67 GHz at -5°C, 25°C, and 95°C. Fig. 5.6 shows the simulated and measured voltage gain and output return loss of the amplifier over temperature. The solid lines are the measurements, and the dashed lines are simulations. The amplifier achieves an average voltage gain of 13.2 dB with a 4 dB peaking at 42 GHz at 25°C. The positive gain slope is to compensate for the loss of the modulator at high frequencies. The 3-dB bandwidth covers from dc to 53 GHz at 25°C with 5 GHz variation from -5°C to 95°C. The output return loss is better than 10 dB up to 38 GHz at all temperatures.

Fig. 5.7 depicts the measured total harmonic distortion (THD) at 1 GHz and 10 GHz over output voltage swings (V_{ppd}) at various temperatures. At 1 GHz, the driver can provide 4 V_{ppd} with < 1.7 % THD

Table 5.1. Comparison to State-of-The-Art Modulator Drivers

Ref.	Tech.	f_T (GHz)	Topology	Voltage Gain (dB)*	BW (GHz)	THD (%)	Supply (V)	P_{dc} (mW)
[2]	65 nm CMOS	-	Linear	7-16.5	48	2.2 @1.5V_{ppd}, 1 GHz	2.6	225
[6]	65 nm CMOS	-	Linear	14-24	32	5 @2V_{ppd},1 GHz	-	180
[7]	55 nm SiGe	300	Linear	8.5	57.5	6 @6V_{ppd}, 10 GHz	6	820
[13]	130 nm SiGe	250	Linear	20-30	40	3.6 @6V_{ppd}, 10 GHz	5.5	1000
[14]	130 nm SiGe	300	DA	6.5	90	4.5 @4V_{ppd}, 1 GHz	5.5	550
[3]	100 nm InP	380	Linear	9.1	86.8	6 @1.5V_{ppse},10 GHz	-	1200
[4]**	150 nm GaAs	100	DA	7	40	-@4 V_{ppse}, 10 GHz	3.3	360
[5]**	150 nm GaN	70	DA	6	44	-@8.4V_{ppse}, -	-	-
This work	**90 nm SiGe**	**300**	**Linear**	**13.2**	**53**	**1.6 @4V_{ppd}, 1 GHz 3.3 @1.5V_{ppd}, 10 GHz**	**7**	**630**

*Voltage gain = $|S_{21}|$ - 6 dB for 50Ω reference systems. **Single-ended design.

and 5 V_{ppd} with < 6 % THD across the temperature. At 10 GHz, the THD at 4 V_{ppd} is 3 % at room temperature and increases to 4.4 % at 95°C. Fig. 5.8 demonstrates the measured differential output voltage with swept differential input voltage at 20 GHz and 40 GHz over temperatures. At 20 GHz, the maximum output voltage swing is 5.5 V_{ppd} at room temperature. At 40 GHz, the PNA-X does not provide enough input voltage to drive the amplifier to saturation. As the temperature increases, the maximum output voltage decreases at both frequencies. Table 5.1 summarizes the main performance specifications of this work and other state-of-the-art results.

5.3 Conclusion

This chapter presents the design and implementation of an optical driver amplifier using a newly developed triple-stacked HBT topology with a resistor/capacitor degeneration network in a 90 nm SiGe BiCMOS HBT process. In addition, a single-section artificial transmission line is implemented at the output

to achieve a wideband matching condition. The amplifier achieves a 13.2 dB voltage gain with a 3-dB bandwidth of 53 GHz. The amplifier consumes 630 mW of dc power. The proposed optical driver can provide a 4 V_{ppd} with <1.7 % THD at 1 GHz and < 4.4 % THD at 10 GHz from -5°C to 95°C.

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Chapter 6. Conclusions

The dissertation presents the analysis, design, and measurement results of wideband amplifiers in various processes, including Indium Phosphide (InP) and Silicon Germanium (SiGe). The summary of the designs are listed as follows:

1. A new bandpass distributed amplifier (DA) using a wideband gain-boosting technique is presented. In particular, a feedback network including a series inductor and a shunt capacitor is used to generate two peaks at the lower and upper cut-off frequency of the amplifier's bandpass response. This technique provides a gain enhancement over a wide bandwidth without sacrificing the upper cut-off frequency. A detailed analysis of the two frequencies peaking effect is carried out to support the theory. To verify the concept, a conventional and a gain-enhanced DA are fabricated in an Indium Phosphide (InP) Heterojunction Bipolar Transistor (HBT) process. The gain-enhanced DA exhibits a measured gain of 10.5 dB with a 4-dB gain improvement compared to the conventional one, covering a 3-dB bandwidth from 60 to 145 GHz. The maximum saturated (P_{sat}) is 20.9 dBm at 75 GHz with the measured 1-dB compression power (P_{1dB}) of 18.5 dBm. The dc power consumption is 440 mW and chip size of 1.6 mm × 0.6 mm.
2. A wideband linearization technique for distributed amplifiers is presented. In particular, an auxiliary transistor is employed to create additional intermodulation distortion components that will be feed-forwarded to the output of each gain unit cell to significantly suppress the 3rd order intermodulation distortion (IM3). To verify the concept, two DAs are fabricated in an InP process. One amplifier employs a conventional stacked- HBT gain unit cell, and the other linearized amplifier utilizes the proposed technique. The linearized distributed amplifier exhibits a measured gain of 10.5 dB with a 3-dB gain bandwidth from dc to 90 GHz. The maximum P_{1dB} is 20.5 dBm, and the 3rd order intercept point (OIP3) is 33 dBm. Compared to the conventional amplifier, the two values are improved by 3.5 dB

and 4.5 dB on average, respectively. Moreover, the linearization technique only increases very little dc power consumption at high power and has the same chip size as compared to the conventional design.

3. A wideband monolithic microwave/millimeter-wave integrated circuit (MMIC) DA using a 3-D interdigital capacitor at the input of the gain cell is demonstrated in an InP HBT process. The proposed DA using interdigital capacitors improves the input return loss at high frequencies compared to one implemented with conventional metal-insulator-metal (MIM) capacitors. The fabricated amplifier achieves a measured average gain of 10.5 dB over a 3-dB bandwidth from 1 to 160 GHz. The maximum measured saturated power (P_{sat}) is 17.8 dBm with the corresponded 1-dB compression power (P_{1dB}) of 15 dBm at 55 GHz. The amplifier achieves a minimum P_{sat} of 14.6 dBm up to 110 GHz. In addition, a high output power DA is demonstrated in InP HBT process. The DA employs nine double-stacked HBT gain unit cells with the proposed parallel/series MIM configuration for the input coupling capacitors. The fabricated amplifier achieves a measured average gain of 11.5 dB over a 3 dB bandwidth from 1 to 150 GHz with a noise figure (NF) of 10.3 dB. The maximum measured P_{sat} is 18.3 dBm with the corresponded P_{1dB} of 15.4 dBm at 50 GHz. The PAE of the amplifier is 10 % at 100 GHz.
4. A linear wideband differential optical driver amplifier in a 90 nm Silicon Germanium (SiGe) Bipolar-Complementary-Metal-Oxide-Semiconductor (BiCMOS) process is presented. The amplifier utilizes a modified triple-stacked HBT topology with emitter degeneration to achieve high output voltage swing and high linearity. The amplifier achieves 13.2 dB voltage gain with a bandwidth from dc to 53 GHz. The amplifier can deliver a 4 V peak-to-peak differential (V_{ppd}) with a 1.6 % total harmonic distortion (THD) at 1 GHz. The amplifier consumes 630 mW dc power at the small-signal operation