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Novel RF Analysis and Design Techniques

A dissertation submitted in partial satisfaction
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by

Aliakbar Homayoun

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Abstract of the Dissertation

Novel RF Analysis and Design Techniques

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Aliakbar Homayoun

Doctor of Philosophy in Electrical Engineering

University of California, Los Angeles, 2013

Professor Behzad Razavi, Chair

The design of RF integrated circuits continues to challenge engineers and researchers, demanding new circuit topologies and transceiver architectures. New ideas often require new analysis techniques as well, so that the designer can insightfully quantify the underlying principles.

This research addresses three problems in RF circuits: (1) analysis of phase noise in phase/frequency detectors (PFDs), an essential component in RF synthesizers; (2) analysis of the relation between the phase noise of delay lines and ring oscillators; and (3) design of a new low-power RF CMOS receiver for IEEE 802.11a. The first analysis derives equations for the phase noise and shows that an octave increase in the input frequency raises the phase noise by 6 dB if flicker noise is dominant and by 3 dB if white noise is dominant. The second analysis reveals a simple shaping function and also dispels the commonly-accepted premise that symmetric rise and fall times in a ring oscillator suppress the upconversion of flicker noise. The third part deals with the design of a low-power 5-GHz receiver. While advances in the art have considerably reduced the power consumption of RF oscillators, frequency dividers, and analog-to-digital converters, the main receiver chain in 5-GHz systems draws a disproportionately high power, about 46

mW. It is therefore desirable to develop low-power RX front ends and baseband filters for WiFi applications. This work introduces a complete 5-GHz CMOS receiver that meets the 11a sensitivity, blocking, and filtering requirements while consuming 11.6 mW. This fourfold reduction in power is achieved through the use of a transformer as a low-noise amplifier, passive mixers, and non-invasive baseband filtering. A new analysis of passive current-driven mixers sheds light on their properties.

The dissertation of Aliakbar Homayoun is approved.

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Behzad Razavi, Committee Chair

University of California, Los Angeles

2013

To my parents . . .

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Publications

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A. Homayoun and B. Razavi, "Relation between delay line phase noise and ring oscillator phase noise," *IEEE J. Solid-State Circuits,* vol. 49, no. 2, Feb. 2014.

A. Homayoun and B. Razavi, "A 5-GHz 11.6-mW CMOS receiver for IEEE 802.11a applications," presented at the *IEEE CICC*, Sep. 2013

CHAPTER 1

Introduction

The design of RF integrated circuits continues to challenge engineers and researchers, demanding new circuit topologies and transceiver architectures. New ideas often require new analysis techniques as well, so that the designer can insightfully quantify the underlying principles. In addition, novel analysis of the existing circuits helps the designer to optimize them and sometimes suggests modifications for better performance.

1.1 Organization

This dissertation proposes three novel analyses in RF circuits. The first analysis which is covered in chapter 2, is on the phase noise in phase/frequency detectors (PFDs), an essential component in RF synthesizers. This is the only published work on the subject that derives equations. Using our compact equations, we have optimized two PFDs for minimum phase noise. Chapter 3 is the first analysis of the relation between the phase noise of delay lines and ring oscillators. Knowing the relation, compact equations are derived for the phase noise of ring oscillators which show a factor of 2 correction for the flicker-noise-induced phase noise. In addition, it dispels the commonly-accepted premise that symmetric rise and fall times in a ring oscillator suppress the upconversion of flicker noise. Chapter 4 deals with the design of a new low-power RF CMOS receiver for IEEE 802.11a.

The most interesting part is the replacement of the LNA with a transformer. How do the transformer and mixers provide proper input matching? Why the frequency response is flat across the channel while the loads of the mixers are capacitors? Why the noise figure is not too high? These are all important questions that would not have been answered without our novel analysis explained in chapter 4. Finally, chapter 5 summarizes the future work.

CHAPTER 2

Analysis of Phase Noise in Phase/Frequency Detectors

The phase noise of phase/frequency detectors can significantly raise the in-band phase noise of frequency synthesizers, corrupting the modulated signal. This chapter analyzes the phase noise mechanisms in CMOS phase/frequency detectors and applies the results to two different topologies. It is shown that an octave increase in the input frequency raises the phase noise by 6 dB if flicker noise is dominant and by 3 dB if white noise is dominant. An optimization methodology is also proposed that lowers the phase noise by 4 to 8 dB for a given power consumption. Simulation and analytical results agree to within 3.1 dB for the two topologies at different frequencies.

2.1 Introduction

The phase noise of the phase/frequency detector (PFD) in a phase-locked loop (PLL) directly adds to that of the reference, manifesting itself for a high frequency multiplication factor and/or a wide loop bandwidth.

This chapter investigates the phase noise mechanisms in PFDs and computes the phase noise spectral density due to both white noise and flicker noise. The results are applied to two PFD topologies, one using static NAND gates and the

other employing true single-phase clocking (TSPC). A PFD phase noise simulation technique is also proposed. The objective is to enable the designer to predict the PFD phase noise, and more importantly, design the PFD so as to make its contribution to the overall PLL phase noise negligible.

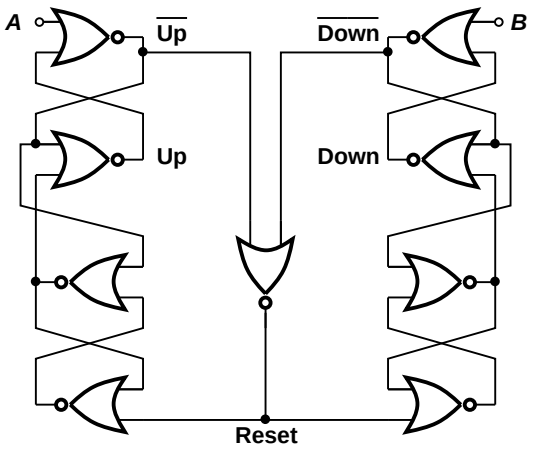
The chapter is organized as follows. Section 2.2 describes the background and motivation for this work. Section 2.3 builds the foundation by calculating the jitter spectrum of an inverter and Section 2.4 extends the results to a NAND gate. Section 2.5 applies these findings to the analysis of two PFD topologies. Section 2.6 discusses the optimization of phase noise for the two PFDs and Section 2.7 presents simulation results. Section 2.8 explains the effect of pulse position modulation of the Up and Down signals and Section 2.9 calculates the phase noise of square wave with uncorrelated jitter on rising and falling edges. Section 2.10 proves that the spectrum of shaped and sampled white noise is white under certain conditions and Section 2.11 concludes chapter 2.

2.2 Background

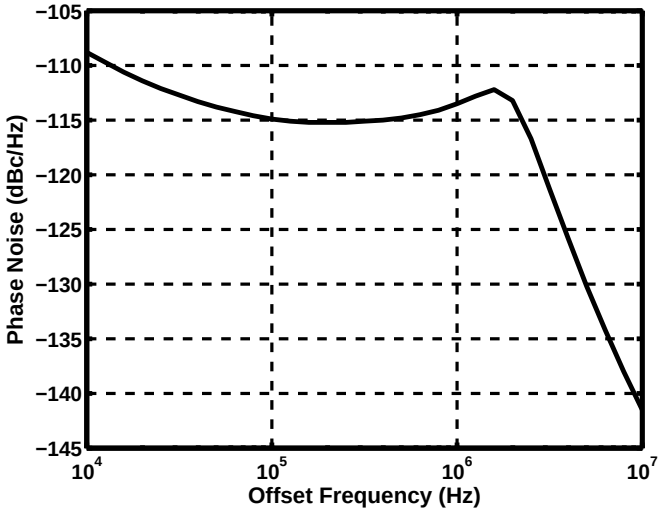
2.2.1 Motivation

The in-band multiplication of a PFD's phase noise can create difficulties in RF synthesizer design [1]-[3]. Consider, as an example, a 5-GHz synthesizer targeting IEEE802.11a applications. To negligibly corrupt the 64QAM signal constellation, the synthesizer must achieve an integrated phase noise of roughly 0.5° rms [4].[1] Now, suppose the standard NOR PFD shown in Fig. 2.1(a) is employed at the input of such a synthesizer with an input frequency of 20 MHz and a loop bandwidth of about 2 MHz. Plotted in Fig. 2.1(b) is the simulated output phase

[1] We assume the transmit and receive synthesizers contribute equal but uncorrelated amounts of phase noise.



(a)



(b)

Figure 2.1: (a) NOR-based PFD, and (b) output phase noise of a 5-GHz PLL due to PFD.

noise of the synthesizer including only the PFD contribution. Here, the PFD incorporates $(W/L)_{PMOS} = 0.3$ μm/60 nm and $(W/L)_{NMOS} = 0.2$ μm/60 nm. The area under this plot from 10 kHz to 10 MHz yields an rms jitter of 0.3°, severely tightening the contribution allowed for the voltage-controlled oscillator (VCO).

As another example, consider a 60-GHz transceiver operating with QPSK signals. A synthesizer multiplying the above PFD phase noise to 60 GHz would exhibit an rms jitter of 3.5°. On the other hand, for negligible corruption of QPSK signals, the rms jitter must be less than about 2.1° [4].

The above examples underscore the need for a detailed treatment of phase noise mechanisms in PFDs. Of course, the charge pump may also contribute significant phase noise and merits its own analysis.

2.2.2 Observations

Consider the generic PLL shown in Fig. 2.2. The PFD generates the Up and Down pulses in response to the rising edges on A and B. The noise in the PFD devices modulates the width and edges of the output pulses, creating a random component in the current produced by the charge pump (CP). We neglect the phase noise of all other building blocks and denote the input frequency by f_{in}.

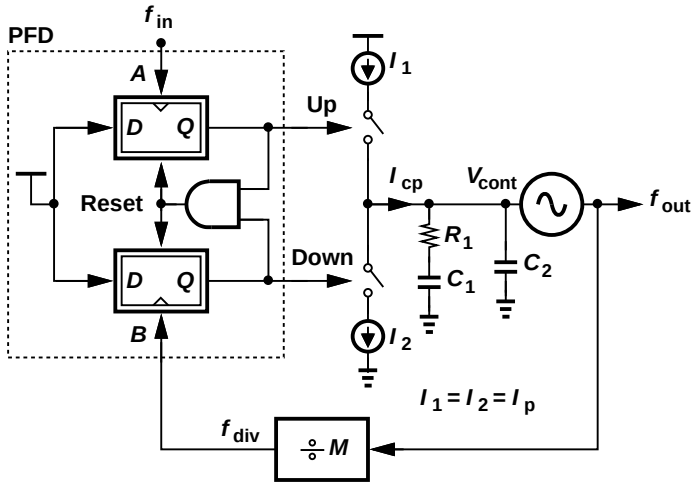


Figure 2.2: A PFD in an integer-N PLL.

The phase noise in Up and Down translates to random modulation of the time

during which I_1 or I_2 is injected into the loop filter. We consider three possible cases. As shown in Fig. 2.3(a), the phase noise may modulate the widths of Up and Down by the same amount, in which case the CP produces no net output. In the second case [Fig. 2.3(b)], the phase noise modulates only the position of Up with respect to Down. As explained in Section 2.8, this effect is negligible. Lastly, the phase noise may modulate the widths of Up and Down pulses *differently* [Fig. 2.3(c)], and it is this case that matters most.

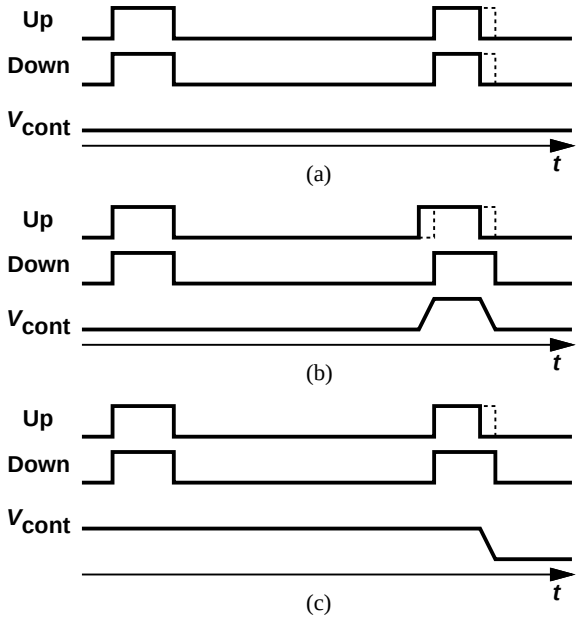


Figure 2.3: Modulation of Up and Down (a) width by the same amount, (b) position, and (c) width differently.

The above observations also reveal that, contrary to a designer's first guess, the PFD phase noise of interest is *not* equal to the phase noise of the Up or Down signals themselves. After all, if the widths of Up and Down pulses vary randomly but exactly in unison, then the net current produced by the CP contains no random component. This point raises the question of how exactly the PFD noise must be simulated, which we address in Section 2.6.

The foregoing points suggest that the phase noise arising from a PFD in fact relates to the random pulsewidth *difference* between the Up and Down signals, ΔT_{UD}. Moreover, four edges, namely, the rising and falling edges of both Up and Down signals, contribute to ΔT_{UD}. Some of the PFD internal transitions displace Up and Down by the same amount and should be ignored (Section 2.5).

The analysis of PFD phase noise in [5], [6] relates the phase noise to the timing jitter, Δt, as $\Delta\phi_{in} = 2\pi f_s \Delta t$, where f_s denotes the operating frequency, but expresses Δt in terms of the (thermal) noise factor and input resistance of the PFD. By contrast, our approach begins with the gates comprising the PFD and determines the jitter in the Up and Down pulsewidth difference, taking into account both flicker and thermal noise. The mismatch between Up and Down currents is neglected here.[2]

2.3 Phase Noise of CMOS Inverter

A good understanding of the phase noise mechanisms in CMOS inverters proves beneficial in the analysis of PFDs as well. Consider the CMOS inverter and its waveforms shown in Fig. 2.4. We wish to study the time envelope of the noise produced by M_1 and M_2. These transistors inject thermal and flicker noise to the output node as they turn on. At the end of the transition, however, the on transistor carries no current and produces no flicker noise. Thus, the thermal noise envelope of each transistor lasts about half of the input cycle, T_{in}, whereas its flicker noise envelope pulsates only during transitions [Fig. 2.4(b)]. Note that in typical PLLs, the transition times within a PFD are much shorter than the input period.

[2]Simulations show 0.2 dB higher phase noise due to a 10% mismatch between the Up and Down currents.

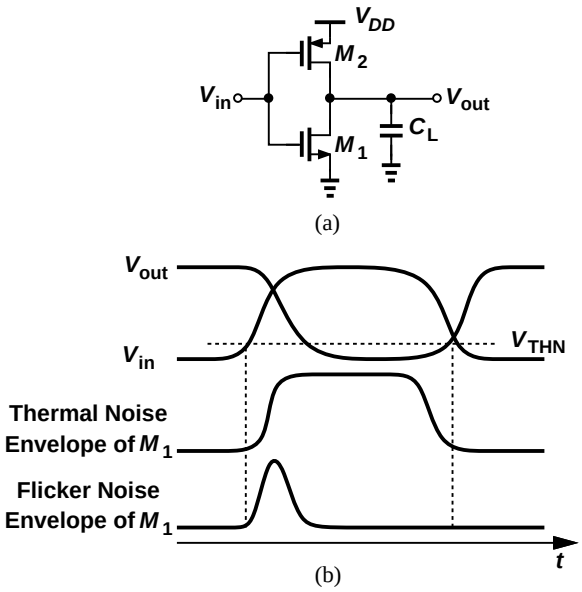


Figure 2.4: (a) CMOS inverter, and (b) thermal and flicker noise envelopes of M_1.

In the analysis that follows, we make numerous approximations based on our intuitive understanding of the circuit's behavior. The soundness of these approximations is ultimately put to test in Section 2.7, where two completely different PFD realizations are simulated and the results are compared with hand calculations.

It is convenient to view the noise injection of M_1 and M_2 as follows: the transistor that is turning on injects thermal and flicker noise during the transition, and the transistor that is turning off (coming out of the deep triode region) deposits kT/C noise at the output.

2.3.1 Noise of Transistor Turning On

In order to formulate the noise contribution by the transistors in Fig. 2.4, we must examine the circuits' waveforms more closely. As depicted in Fig. 2.5 for a rising

transition at the input and for an inverter with a fanout of about 2, the output begins to fall only after V_{in} is relatively close to V_{DD}. Transistor M_1 turns on as V_{in} exceeds its threshold, V_{THN}, at $t = t_1$, and injects increasingly larger flicker and thermal noise as V_{in} rises. The noise envelope reaches a maximum before the transistor enters the triode region, around $t = t_2$. Thereafter, the flicker noise injection subsides, falling to zero at $t = t_3$. The thermal noise current, on the other hand, goes from $4kT\gamma g_m$ to a slightly lower value, $4kT/R_{on}$, where R_{on} denotes the channel resistance of M_1 with $V_{GS} = V_{DD}$.

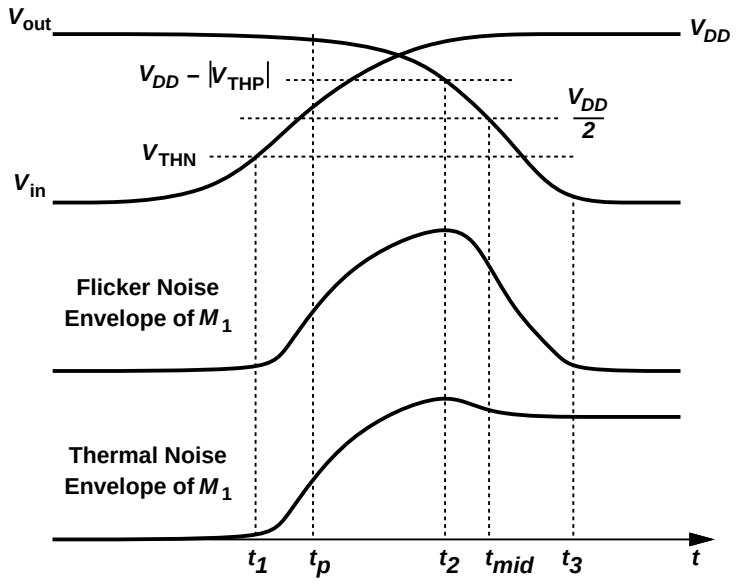


Figure 2.5: Detailed view of thermal and flicker noise envelopes during input and output transitions.

Our next simplifying assumption is that the output phase noise of interest manifests itself while V_{out} in Fig. 2.5 crosses approximately $V_{DD}/2$ and the noise injected by the transistors after this point is unimportant [7]. Thus, in the waveforms of Fig. 2.5, we consider the area under the envelopes for only up to $t = t_{mid}$.

We now wish to approximate the area under the noise envelopes by a simple

function. As shown in Fig. 2.6, the flicker noise envelope is approximated by a rectangular waveform of the same height, h, but lasting from the time the actual envelope reaches half of its height, $t_{h/2}$, to the time V_{out} reaches $V_{DD}/2$, t_{mid}. We expect that the sum of the gray areas is roughly equal to the cross-hatched area. Transient noise simulations in Cadence's Spectre indicate an error of about 4% in this approximation. We apply the same concept to the thermal noise envelope as well. Note that [7] uses a rectangle from the time V_{out} begins to fall (t_p in Fig. 2.5) to t_{mid}, which, according to simulations, underestimates the integrated noise power by 2 to 3 dB.

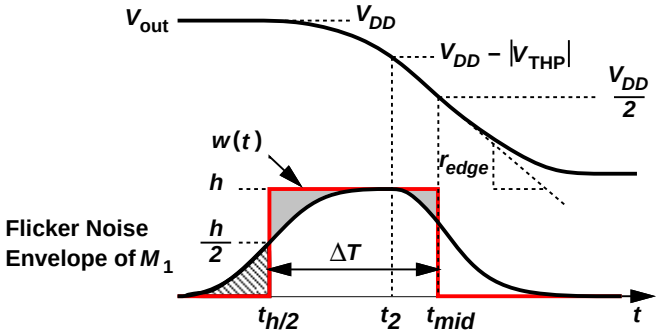


Figure 2.6: Rectangular approximation of noise envelope.

Another simplifying assumption can be derived from the waveforms in Fig. 2.5: at the peak of the noise envelope, one transistor is nearly off. Thus, we consider only the noise of M_1 on the falling edges at the output and only the noise of M_2 on the rising edges.

Based on the foregoing approximations and utilizing the rectangular function, $w(t)$, in Fig. 2.6, we now outline the inverter phase noise analysis as follows. As shown in Fig. 2.7(a), the noise current of each transistor, $i_n(t)$ is equivalently multiplied by shifted versions of $w(t)$. Each product is integrated for a duration of $\Delta T = t_{mid} - t_{h/2}$ and divided by the load capacitance, C_L, yielding the noise

voltage [Fig. 2.7(b)]. These voltages are then divided by the slew rate, r_{edge} (Fig.

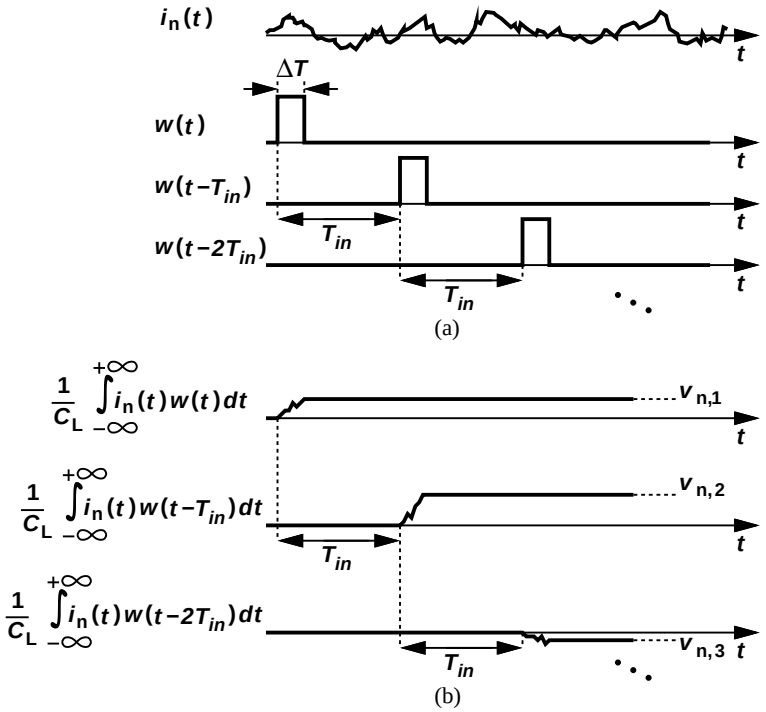


Figure 2.7: (a) Equivalent operation of inverter on noise of one transistor, and (b) conversion of noise current to noise voltage.

2.6), to give the time displacement (jitter), sampled, and summed. We write the noise voltage, $v_{n,1}$, after the first window as

$$\begin{aligned} v_{n,1} &= \frac{1}{C_L}\int_0^{\Delta T} i_n(t)\,dt \\ &= \frac{1}{C_L}\int_{-\infty}^{+\infty} i_n(t)w(t)\,dt. \end{aligned} \tag{2.1}$$

Note that the load capacitance is assumed constant and equal to its value at $V_{out} = V_{DD}/2$. Also, the integration tacitly neglects the effect of the inverter's output resistance, r_O. This approximation is justified because the time constant, $r_O C_L$, at the inverter output is much greater than ΔT. Similarly,

$$v_{n,m} = \frac{1}{C_L}\int_{-\infty}^{+\infty} i_n(t)w(t - mT_{in})\,dt. \tag{2.2}$$

The particular shape of $w(t)$ allows this equation to be rewritten as

$$v_{n,m} = \frac{1}{C_L}\int_{-\infty}^{+\infty} i_n(t)w(mT_{in} - t)\,dt, \tag{2.3}$$

which is the convolution integral [7]. The noise voltage spectrum is therefore given by

$$S_{Vn}(f) = \frac{1}{C_L^2}|W(f)|^2 S_{In}(f), \tag{2.4}$$

where $W(f)$ denotes the Fourier transform of $w(t)$ and $S_{In}(f)$ the spectrum of $i_n(t)$. As shown in Section 2.9, the phase noise spectrum[3] due to noise of NMOS transistor on the falling edges is equal to

$$S_\Phi(f) = \frac{\pi^2}{r_{edge}^2 T_{in}^2}\sum_{m=-\infty}^{m=+\infty} S_{Vn}(f - \frac{m}{T_{in}}). \tag{2.5}$$

It is important to recognize two differences between the above analysis and that in [7]: (1) as mentioned earlier, our window definition (from $t_{h/2}$ to t_{mid}) more accurately predicts the injected noise power, and (2) the sampling phenomenon reveals aliasing even for flicker noise if the $1/f$ corner, f_{cor}, is comparable with the operation frequency, which may be the case for PFDs.

We now simplify Eq. (2.5) if $\overline{I_n^2}$ is white. As shown in Section 2.10, $S_\Phi(f)$ is also white and equal to

$$\begin{aligned} S_\Phi(f) &= \frac{\pi^2}{r_{edge}^2 T_{in}^2}\frac{1}{C_L^2}\frac{\Delta T}{f_{in}}S_I(f) \\ &= \frac{\pi^2}{r_{edge}^2 C_L^2}\frac{\Delta T}{T_{in}}S_I(f). \end{aligned} \tag{2.6}$$

In this expression, the load capacitance appears in both r_{edge} ($= I_D/C_L$, where I_D is the drain current of the on transistor as V_{out} crosses $V_{DD}/2$) and in ΔT. Thus, $S_\Phi(f)$ is *directly* proportional to C_L and f_{in}. The output phase noise due to white noise therefore rises by 3 dB for each doubling of the operation frequency.

[3]Throughout this chapter, all the spectra are two-sided, and the phase noise is denoted by $S_\Phi(f)$.

The flicker noise behavior of the inverter can also be deduced from Eq. (2.5). If f_{in} is well above the flicker noise corner frequency, no aliasing occurs and (2.5) is simplified by choosing $m = 0$:

$$S_\Phi(f) = \frac{\pi^2}{r_{edge}^2 T_{in}^2} S_{Vn}(f). \tag{2.7}$$

Since ΔT is much less than $1/f_{cor}$, we can assume $W(f) = \Delta T^2 sinc^2(\pi f \Delta T)$ is relatively constant for the frequency range of interest and equal to ΔT^2. It follows that

$$S_\Phi(f) = \frac{\pi^2}{r_{edge}^2 T_{in}^2} \frac{\Delta T^2}{C_L^2} S_{1/f}(f), \tag{2.8}$$

where $S_{1/f}(f)$ denotes the noise current spectral density of the on transistor due to its $1/f$ noise. In this case, the phase noise rises by 6 dB for each doubling of f_{in}. It also exhibits a stronger dependence upon ΔT. As mentioned earlier, (2.6) and (2.8) are evaluated for M_1 on the falling edge at the output and for M_2 on the rising edge. Note that [7] does not analyze the effect of flicker noise in CMOS inverters.

2.3.2 Noise of Transistor Turning Off

As illustrated in Fig. 2.5, when the noise envelope reaches its peak, one transistor is near the edge of the triode region and the other is almost off. Before turning off, however, this transistor has acted as a resistor, producing noise across C_L. Turning off once every T_{in} seconds, the NMOS transistor deposits a noise voltage whose spectral density is given by $(kT/C_L)/f_{in}$. As shown in Section 2.9, the falling edges exhibit a phase noise equal to

$$S_1(f) = \frac{\pi^2}{T_{in}^2} \frac{1}{r_{edge}^2} \frac{kT}{C_L f_{in}}. \tag{2.9}$$

Taking the PMOS contribution into account, we obtain the total kT/C-induced phase noise as

$$S_\Phi(f) = \frac{2\pi^2}{T_{in}^2} \frac{1}{r_{edge}^2} \frac{kT}{C_L f_{in}}. \tag{2.10}$$

2.3.3 Total Phase Noise

The total phase noise is given by the sum of five terms: Eqs. (2.6) and (2.8) evaluated for both NMOS and PMOS transistors, and Eq. (2.10):

$$\begin{aligned} S_\Phi(f) &= \left\{ \frac{\pi^2}{r_{edge}^2 C_L^2} [\frac{\Delta T}{T_{in}} S_I(f) + \frac{\Delta T^2}{T_{in}^2} S_{1/f}(f)] \right\}_{NMOS} \\ &+ \left\{ \frac{\pi^2}{r_{edge}^2 C_L^2} [\frac{\Delta T}{T_{in}} S_I(f) + \frac{\Delta T^2}{T_{in}^2} S_{1/f}(f)] \right\}_{PMOS} \\ &+ \frac{2\pi^2 f_{in}}{r_{edge}^2} \frac{kT}{C_L}. \end{aligned} \tag{2.11}$$

2.4 Phase Noise of CMOS NAND Gate

The inverter phase noise analysis can be readily extended to other CMOS gates as well. We briefly consider here the noise behavior of a static NAND gate and use the results in Section 2.5 to study a NAND-based PFD.

Since in a PFD environment, the two inputs do not change simultaneously, we can reduce the gate to an inverter for each transition. Such an inverter incurs an additional capacitance at the output due to the second PMOS transistor, and its output falling edge is produced by the series combination of two NMOS transistors (Fig. 2.8).

In our PFD design, M_1 and M_3 have the same width and minimum length;

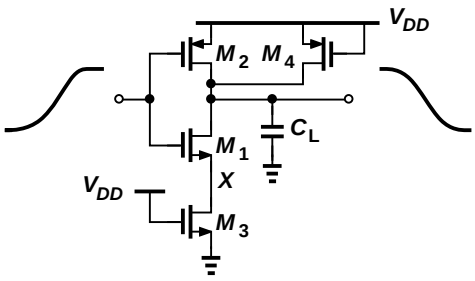


Figure 2.8: NAND gate with one input changing.

thus, they can be replaced with one NMOS device having twice their length.[4] In other words, Eq. (2.11) holds if r_{edge}, ΔT, C_L and $S_{In}(f)$ are modified to reflect the equivalent values in the NAND circuit.

2.5 PFD Phase Noise Analysis

2.5.1 NAND PFD

As suggested by the factors ΔT in (2.6) and ΔT^2 in (2.8), the phase noise rises in proportion to the turn-on time of the transistors in each gate. A worthy effort in PFD design, therefore, is to minimize the rise and fall times. We thus modify the standard NOR-based PFD to the NAND-based topology shown in Fig. 2.9(a). Note that this circuit responds to the *falling* edges of A and B, and its Up and Down outputs are *low* when asserted.

We must now examine the propagation of the edges through the PFD circuit, seeking those whose jitter modulates the pulsewidth *difference* between the Up and Down pulses. To this end, we draw a detailed timing diagram, mark with a certain shade or pattern the jitter contributed by each gate to each transition, carry the jitters on to the final Up and Down pulses, and omit those that are in

[4]The drain and source capacitance at node X introduce a negligible error in this equivalency.

common.

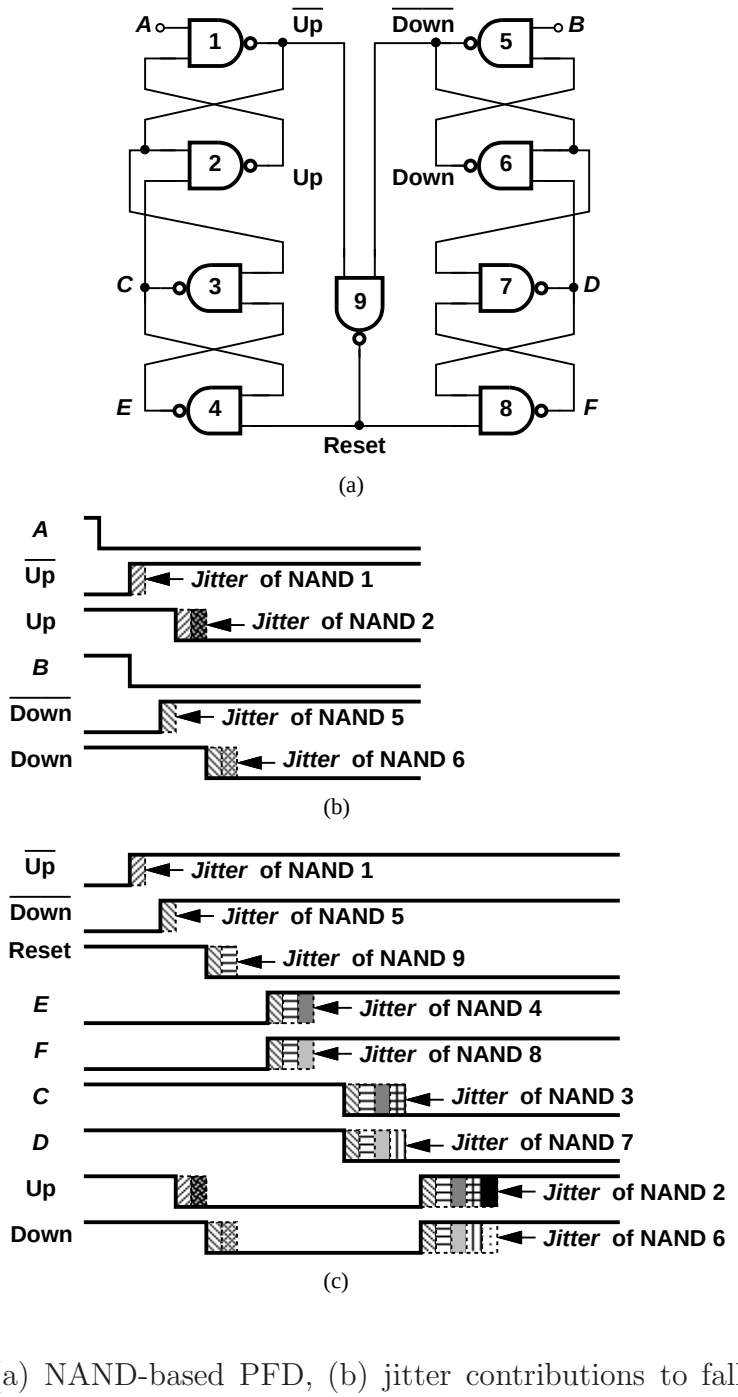


Figure 2.9: (a) NAND-based PFD, (b) jitter contributions to falling edges of outputs, and (c) jitter contributions to rising edges of outputs.

Figure 2.9(b) shows the timing diagram, assuming input A falls earlier than input B. NAND 1 adds jitter to the falling edge of A, producing a rising edge on $\overline{Up}$. This edge experiences additional jitter in NAND 2 and generates the falling edge of Up. That is, each falling edge of Up is corrupted by only the jitters of NANDs 1 and 2. Similarly, when a falling edge of B follows, $\overline{Down}$ rises with NAND 5's jitter and Down falls with both NAND 5's and NAND 6's jitters.

We must also follow the $\overline{Up}$ and $\overline{Down}$ rising edges through the reset path. As illustrated in Fig. 2.9(c), after $\overline{Down}$ goes up, Reset falls, inheriting the jitters of NAND 5 and NAND 9. In response, E and F rise, incurring additional jitter from NAND 4 and NAND 8, respectively. Subsequently, C falls with the jitter of NAND 3 and D with that of NAND 7. Finally, Up and Down rise with the jitters of NAND 2 and NAND 6, respectively.

The Up and Down waveforms in Fig. 2.9(c) merit two remarks. First, NAND 2 contributes jitter to both the rising and falling edges of Up, but the two jitters are uncorrelated because the former is due to a PMOS device and the latter due to an NMOS device (the series combination of M_1 and M_3 in Fig. 2.8). A similar observation applies to NAND 6 contributions to Down. Second, the jitter produced by NAND 9 appears on the rising edges of both Up and Down pulses and hence is immaterial. As seen from Fig. 2.9(c), NANDs 1-8 make a total of 10 contributions to the pulsewidth difference between Up and Down. The phase noise spectral densities of these contributions are summed to obtain the overall PFD phase noise.

In response to the jitter components in the Up and Down pulses (except for those that are in common), the charge pump in Fig. 2.2 produces an error current, ΔI. Adding up the powers of uncommon jitters, T_m, $m = 1, ..., 10$, in the Up and

Down pulses, we have

$$\overline{\Delta I^2} = \frac{I_p^2}{T_{in}^2} \sum_{m=1}^{10} T_m^2. \tag{2.12}$$

It can be shown that the transfer function from this current injection to the PLL output within the loop bandwidth is equal to $\Phi_{out,PLL}/\Delta I = (2\pi/I_p)M$. It follows that

$$S_{\Phi,PLL}(f) = \frac{4\pi^2}{T_{in}^2} M^2 \sum_{m=1}^{10} S_{Tm}(f), \tag{2.13}$$

where $S_{Tm}(f)$ denotes the spectral density of jitter component T_m and is equal to $S_{Vn}(f)/r_{edge}^2$. For roughly similar gates and rise and fall times, the in-band phase noise observed at the PLL output is given by

$$\begin{aligned} S_{\Phi,PLL} \cong 10M^2 [&\frac{4\pi^2 \Delta T}{r_{edge}^2 C_L^2 T_{in}} S_I(f) + \frac{4\pi^2 \Delta T^2}{r_{edge}^2 C_L^2 T_{in}^2} S_{1/f}(f) \\ &+ \frac{4\pi^2 f_{in}}{r_{edge}^2} \frac{kT}{C_L}]. \end{aligned} \tag{2.14}$$

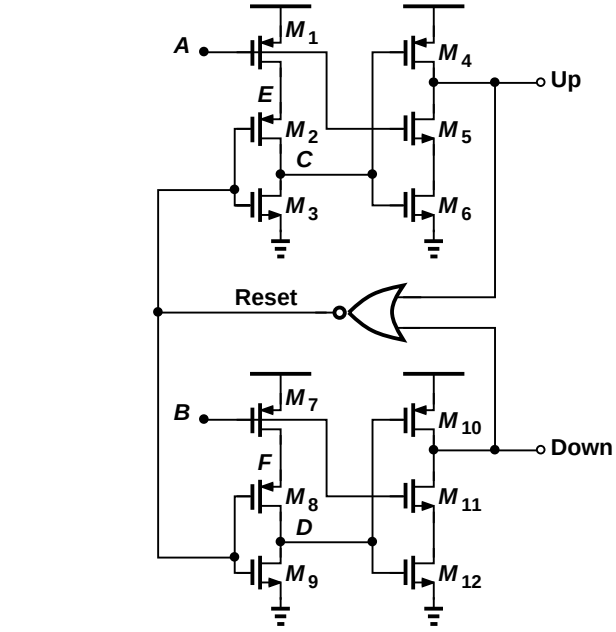
As explained in Section 2.6, however, an optimum design may incorporate different sizings for the gates.

An important point emerging from our analysis is that, to reduce the flicker noise of a PFD, the channel length of its constituent transistors must *not* be increased. This is because longer-channel devices inevitably raise ΔT in (2.14). Instead, the channel area of the transistors can be increased by choosing *wider* devices.

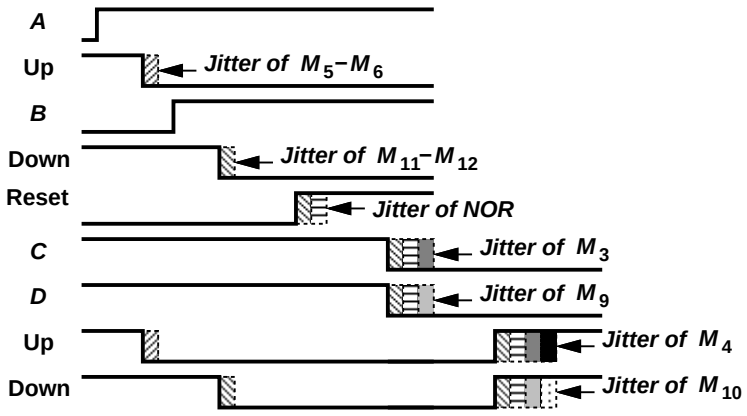
2.5.2 TSPC PFD

The foregoing analysis can be applied to other PFD topologies as well. In this section, we study the phase noise of a TSPC implementation [8] as it can potentially achieve a higher speed and proves useful in cascaded PLLs. Depicted in Fig. 2.10(a), the circuit operates as follows. A rising edge on A turns on M_5,

discharging the Up output. Similarly, a rising edge on B discharges the Down output. Once both Up and Down are low, Reset rises, discharging nodes C and D and forcing Up and Down to go high.



(a)



(b)

Figure 2.10: (a) TSPC PFD, and (b) jitter contributions to the outputs.

In a manner similar to the analysis of the NAND PFD, we follow the transitions through the circuit and mark the jitter contributed by each stage. As

illustrated in Fig. 2.10(b), the falling edges of Up and Down are corrupted by the noise of the series combinations M_5-M_6 and M_{11}-M_{12}, respectively. Next, Reset experiences the jitter due to M_{11}-M_{12} and the NOR gate. The falling transitions at C and D inherit the jitter of Reset and incur additional noise due to M_3 and M_9, respectively. Finally, these edges are corrupted by the noise of M_4 and M_{10}.

Let us draw several conclusions. First, the jitter of the NOR gate modulates the widths of Up and Down equally and hence is ignored. Second, the overall TSPC PFD phase noise arises from six transitions and can be potentially smaller than that of the NAND PFD. Third, the noise injection mechanisms in each stage are similar to those of the inverter and NAND gates studied earlier. For example, when M_5 turns on, its corresponding stage acts approximately like a NAND gate (except that M_4 has been off well before this transition). Also, when node C falls, the series combination M_5-M_6 deposits kT/C noise at the output while M_4 turns on as in an inverter and injects both thermal and flicker noise. Thus, Eq. (2.14) applies here as well if the factor of 10 is replaced by 6 and the gates and rise and fall times are assumed similar.

2.6 Design Optimization

With the insights developed above into PFD phase noise mechanisms, we now seek to optimize each design for minimum phase noise. Of course, one can simply enlarge the widths of all of the PFD transistors by a factor of α so as to reduce the phase noise by the same factor, but at the cost of proportionally higher power consumption. A more methodical approach, however, is to assume a certain power budget and determine the best sizing of the transistors that yields minimum phase noise. This optimization can still be followed by the above scaling technique to

trade power for phase noise. We consider $1/f$ noise here as it dominates for offsets as high as 10 MHz, but optimization for thermal noise is similar.

Since the PFD power dissipation is proportional to the total transistor width in the signal path, W_{tot}, we must determine how a given W_{tot} is apportioned among the transistors so as to minimize the phase noise. Our general procedure is to favor transistors that define the transition time of critical edges. We also make four approximations: (1) The capacitance at a given node is proportional to the width of the "driver" transistor, W_a, and the width of the "driven" transistor, W_b: $C_L \propto \eta W_a + W_b$. The first term on the right accounts for the drain junction capacitance and the Miller multiplication of the gate-drain overlap capacitance at the output node (about a factor of 2). (2) The drain $1/f$ noise current spectrum is given by $S_{1/f}(f) = g_m^2 K_f/(W_a L_a C_{ox} f)$, where $g_m \approx I_D/(V_{GS} - V_{TH})$ and $V_{GS} = V_{DD}$.[5] (3) At the point of interest, namely, $V_{GS} \approx V_{DD}$ and $V_{out} \approx V_{DD}/2$, we have $I_D \propto W_a$ regardless of the transistor (short-channel) characteristics. Thus, the slew rate in Eq. (2.8), $r_{edge} \propto I_D/C_L \propto W_a/C_L$. (4) The window width, ΔT, is proportional to $V_{DD}/r_{edge} \approx V_{DD}C_L/I_D$. Equation (2.8) is now rewritten as

$$S_\Phi(f) \propto \frac{{f_{in}}^2 {V_{DD}}^2 {C_L}^2}{{W_a}^3} \frac{1}{f}. \tag{2.15}$$

For given values of f_{in}, V_{DD}, and f,

$$S_\Phi(f) \propto \frac{(\eta W_a + W_b)^2}{{W_a}^3}. \tag{2.16}$$

The power consumed to charge and discharge such a node once per cycle is approximately equal to $P = f_{in} C_L {V_{DD}}^2$. We now apply these results to the optimization of the NAND and TSPC PFDs.

[5]This g_m equation assumes heavy velocity saturation. For long-channel devices, $g_m \approx 2I_D/(V_{GS} - V_{TH})$. This distinction is not critical in our analysis.

2.6.1 NAND PFD Optimization

As evident from Figs. 2.9(b) and (c), the NAND PFD phase noise arises from five transistors: the PMOS device in NAND 1, the NMOS device in NAND 2, the PMOS device in NAND 4, the NMOS device in NAND 3, and the PMOS device in NAND 2. Denoting the widths of PMOS and NMOS transistors in NAND j by W_{Pj} and W_{Nj}, respectively, we use Eq. (2.16) to express the first PMOS contribution as:

$$S_{\Phi_1}(f) \propto \frac{[\eta(2W_{P1} + W_{N1}) + W_2 + W_3 + W_9]^2}{{W_{P1}}^3}. \tag{2.17}$$

Here, the factor of 2 accounts for the two PMOS devices tied to the output and $W_j = W_{Pj} + W_{Nj}$. The sum $W_2 + W_3 + W_9$ represents the load due to the three NANDs driven by NAND 1. The other four contributions can be expressed in a similar manner, e.g., for the NMOS device in NAND 2:

$$S_{\Phi_2}(f) \propto \frac{[\eta(2W_{P2} + W_{N2}) + W_{P1} + W_{N1}]^2}{{W_{N2}}^3}. \tag{2.18}$$

Note that the proportionality factors relating the right-hand sides of (2.17) and (2.18) to their left-hand side are different as they include the mobility and flicker noise coefficient of PMOS and NMOS devices, respectively. The total power consumption satisfies the relation:

$$P \propto f_{in}{V_{DD}}^2[W_{P9} + W_{N9} + 2\sum_{j=1}^{4}(W_{Pj} + W_{Nj})]. \tag{2.19}$$

As explained in Section 2.5, the jitter of some of the edges does not enter the overall PFD phase noise. The transistors causing these edges can therefore have nearly minimum widths so long as they respond fast enough to avoid circuit failure. The devices falling into this category are the NFETs in NANDs 1, 4, and 9 and the PFETs in NANDs 3 and 9. The sum of the five phase noise contributions

described above must be minimized subject to the power budget imposed by (2.19). This is accomplished using the "fmincon" function in MATLAB. For example, a total width of 162 μm (corresponding to 0.24 mW at 1 GHz) for the transistors yields $W_{P1} = 11$, $W_{N1} = 0.12$, $W_{P2} = 9.1$, $W_{N2} = 5.9$, $W_{P3} = 0.12$, $W_{N3} = 6.22$, $W_{P4} = 7.8$, $W_{N4} = 0.12$, $W_{P9} = 0.12$, $W_{N9} = 0.12$, all in microns. Using transient circuit simulations, we adjust some of the noncritical transistors widths so to minimize crowbar currents and speed up the critical transitions, obtaining $W_{P1} = 10.6$, $W_{N1} = 0.5$, $W_{P2} = 8.5$, $W_{N2} = 5.5$, $W_{P3} = 0.6$, $W_{N3} = 5.84$, $W_{P4} = 7.4$, $W_{N4} = 0.5$, $W_{P9} = 0.12$, $W_{N9} = 2$, all in microns. It is interesting that such a range of widths would not be obvious if we attempted to manually optimize the PFD transistors by trial and error. As shown in Section 2.7, this optimization lowers the phase noise by 4 to 6 dB.

2.6.2 TSPC PFD Optimization

The foregoing procedure can be applied to the TSPC PFD of Fig. 2.10(a) as well. Here the phase noise has three contributions arising from $1/f$ noise:

$$S_{\Phi_1}(f) \propto \frac{[\eta(W_4 + W_5) + W_{P,NOR} + W_{N,NOR}]^2}{{W_5}^3}, \tag{2.20}$$

where W_j refers to the width of M_j and $W_{P,NOR}$ and $W_{N,NOR}$ are the PMOS and NMOS widths in the NOR gate, respectively. The power consumption satisfies the relation:

$$P \propto f_{in}{V_{DD}}^2(2\sum_{j=1}^{6} W_j + W_{P,NOR} + W_{N,NOR}). \tag{2.21}$$

For simplicity, we assume equal widths for the transistors within each cascode structure. Also, M_1-M_2 and M_7-M_8 in Fig. 2.10(a) contribute no jitter to the PFD and hence can have small widths. For example, a total width of 162 μm (corresponding to 0.2 mW at 1 GHz) is apportioned as follows: $W_1 = 0.12, W_2 =$

$0.12, W_3 = 28, W_4 = 25, W_5 = 13.72, W_6 = 13.72, W_{P,NOR} = 0.12, W_{N,NOR} = 0.12$, all in microns. Manual adjustment to improve transition times in the simulations yields $W_1 = 1.4, W_2 = 1.4, W_3 = 12, W_4 = 24, W_5 = 10, W_6 = 10, W_{P,NOR} = 10, W_{N,NOR} = 0.12$, all in microns. As discussed in Section 2.7, this optimization reduces the phase noise by 5 to 8 dB.

2.6.3 Dependence on Operation frequency

Equation (2.14) reveals that the phase noise of PFDs rises in proportion to f_{in} in the thermal regime and ${f_{in}}^2$ in the flicker noise regime. This dependence imposes certain bounds on the in-band phase noise of PLLs. For a feedback divide ratio of M, the first term in Eq. (2.14) yields an output phase noise of

$$\begin{aligned} S_{\Phi,out}(f) &\propto f_{in} M^2 S_I(f) \\ &\propto \frac{{f_{out}}^2}{f_{in}} S_I(f). \end{aligned} \tag{2.22}$$

That is, to minimize the phase noise due to the PFD thermal noise, f_{in} must be maximized. For PFD flicker noise, on the other hand,

$$\begin{aligned} S_{\Phi,out}(f) &\propto {f_{in}}^2 M^2 S_{1/f}(f) \\ &\propto {f_{out}}^2 S_{1/f}(f). \end{aligned} \tag{2.23}$$

Interestingly, this PFD contribution is independent of the input frequency so long as flicker noise does not experience aliasing.

2.7 Simulation Results

This section presents simulation results in 65-nm CMOS technology for the circuits studied in this chapter and compares them with our analytical derivations. The objective is threefold: (a) validate the trends predicted by our analysis, e.g.,

the dependence of phase noise upon the input frequency and node capacitance, (b) check the absolute accuracy of the analytical results, and (c) examine the soundness of our optimization procedure.

A few remarks with respect to the hand calculations are warranted. First, the transistor capacitances, drain bias currents, and drain (1/f and thermal) noise currents are obtained from ac and transient simulations for various values of V_{GS} and V_{DS}. These simulations also reveal the peak noise current and the gate-source voltage, $V_{GS,half}$, at which the noise current is equal to half of its peak. Second, the window width, ΔT, in Eqs. (2.6), (2.8), (2.11) and (2.14) is derived from transient simulations of the stage of interest by finding the time at which the gate-source voltage reaches $V_{GS,half}$.

2.7.1 Inverter and NAND Simulations

Figure 2.11 plots the phase noise of a chain of eight inverters with $W_P = 6$ μm and $W_N = 3$ μm at an input frequency of 1 GHz. (As explained in Section 2.7.2, scaling to other frequencies is straightforward.) In order to investigate the robustness of our analytical approach, the chain is also studied with an additional node capacitance of 20 fF. In each case, the results of Cadence pnoise simulations are compared with those of hand calculations. Figure 2.12 repeats these experiments for a chain of eight NAND gates with one input tied to V_{DD} and $W_P = W_N = 6$ μm. We observe that in all cases, the hand calculations incur an error of less than 2 dB.

2.7.2 PFD Simulations

As argued in Section 2.2, the PFD phase noise cannot be simulated by examining only the Up or Down pulses. For this reason, we embed the PFD within an

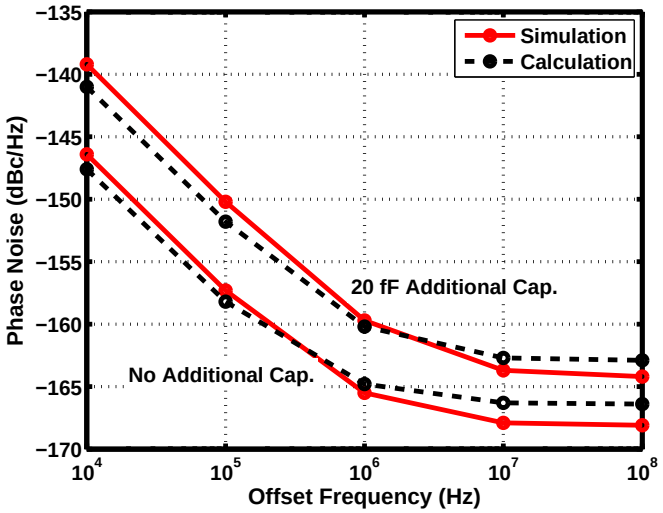


Figure 2.11: Phase noise of a chain of eight inverters running at 1 GHz.

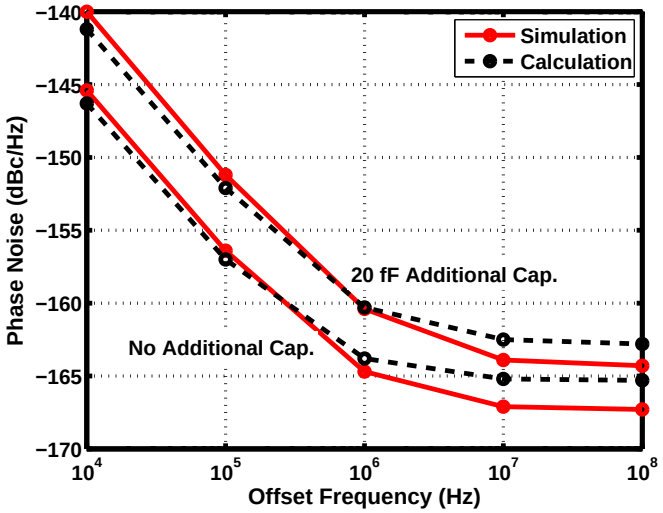


Figure 2.12: Phase noise of a chain of eight NANDs running at 1 GHz (with one input tied to V_{DD}).

otherwise ideal PLL, run a pss and pnoise analysis, allow the PLL to settle, and compute the output phase noise of the PLL in the steady state. If the PLL bandwidth is large enough, the PFD phase noise up to the offset frequencies of

interest passes to the output unattenuated. Such a simulation takes a long time but is necessary here to demonstrate the validity of our approach. The PLL comprises behavioral descriptions of the VCO, frequency divider, and charge pump. The loop filter employs a noiseless resistor. To ensure that the PLL does not attenuate the PFD phase noise for offset frequencies as high as 100 MHz, the reference frequency, f_{ref}, is chosen equal to or greater than 1 GHz. Such a high value is chosen so as to readily observe and validate the effect of flicker noise. For much lower input frequencies, the aliasing of white noise tends to mask the effect of flicker noise, making it difficult to correlate the simulations with the analytical results. For example, if f_{ref} is reduced to 20 MHz, then the effect of flicker noise rises by $10\log(50) = 17$ dB and that of white noise by $20\log(50) = 34$ dB, masking the former.

Figure 2.13 plots the simulated and calculated phase noise of the NAND PFD for different input frequencies. (Each simulation incorporates a different set of PLL parameters[6] commensurate with the reference frequency.) As predicted in Section 2.3, doubling f_{ref} raises the phase noise by 6 dB in the 1/f noise regime and by 3 dB in the white noise regime. The error in the analytical calculations is 3.1 dB. The effect of white noise is overestimated possibly due to assuming that all of the high-frequency noise components experience only a $sinc^2$ envelope before folding, whereas in the actual circuit, these components are also attenuated by the finite bandwidth and hence do not extend to infinity.

Figure 2.14 plots similar results for the TSPC PFD. The maximum error in this case is 2.8 dB. Designed for the same power consumption as the NAND PFD, the TSPC topology exhibits about 6 dB lower phase noise.

Illustrated in Fig. 2.15 are the results of the optimization procedure described

[6]For example, $R_1 = 600\ \Omega$, $C_1 = 200$ pF, $C_2 = 100$ fF, $I_p = 1$ mA, $M = 1$, and $K_{VCO} = 2\pi(1.5 \times 10^9)$ rad/s.

in Section 2.6. For a given power consumption, the phase noise is reduced by 4 to 8 dB for the two PFDs.

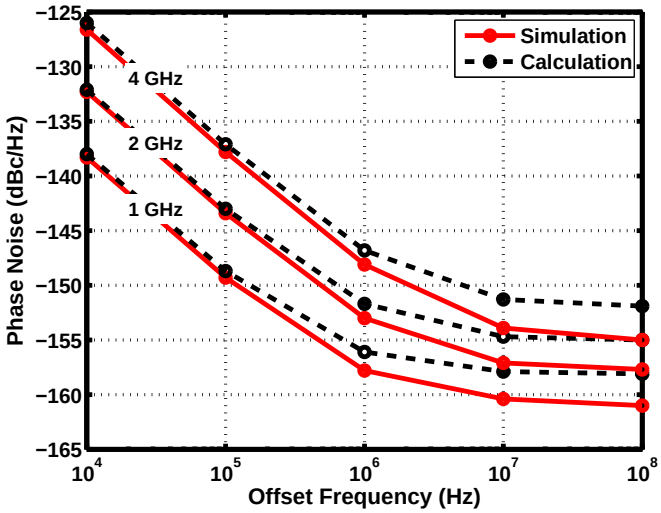


Figure 2.13: Phase noise of NAND PFD at various input frequencies.

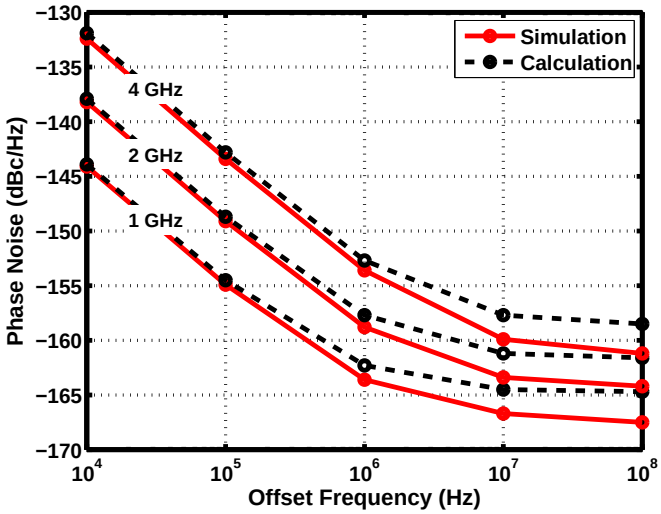


Figure 2.14: Phase noise of TSPC PFD at various input frequencies.

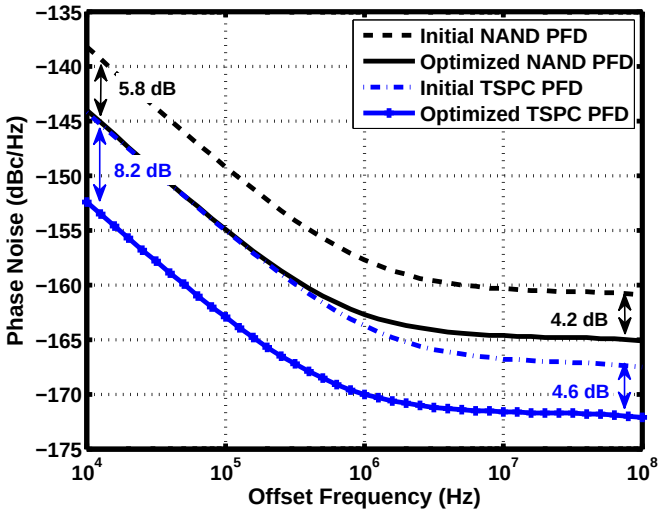


Figure 2.15: Phase noise of NAND and TSPC PFDs before and after optimization.

2.8 Effect of Pulse Position Modulation

In this section, we show that if noise modulates only the position of the Up or Down pulses, the resulting phase noise is negligible. Consider the waveforms depicted in Fig. 2.16(a), where Up and Down have a pulsewidth of T_{RST} and a random skew of T_{skew}. Assuming an ideal charge pump, we note that the disturbance on the oscillator control voltage is in the form of a pulse with a mean width of T_{RST}. By contrast, as shown in Fig. 2.16(b), a pulsewidth difference of T_D between Up and Down manifests itself as a step on the control voltage, producing a much larger phase disturbance.

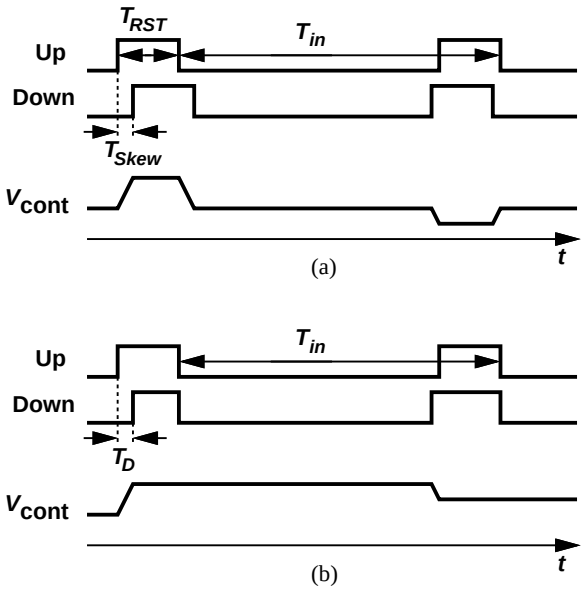


Figure 2.16: Modulation of (a) position, and (b) pulsewidth of Up and Down signals.

2.9 Phase Noise of Square Wave with Uncorrelated Jitters on Rising and Falling Edges

It is usually assumed that an edge displacement of ΔT translates to a phase change of $2\pi\Delta T/T_{in}$, where $T_{in} = 1/f_{in}$ denotes the period. Of course, if *all* of the edges of a square wave are displaced by ΔT, this amount of phase change arises. However, jitter affects the consecutive edges differently, requiring a closer look at the resulting phase noise.

Let us first suppose a sinusoidal jitter, $T_m \cos \omega_m t$, is applied to only the rising edges of an ideal square wave, $p(t)$. As shown in Fig. 2.17(a), the rising edge at kT_{in} is displaced by an amount equal to $T_m \cos(\omega_m k T_{in})$. This jittery waveform can be expressed as the sum of $p(t)$ and a train of pulses that occur at kT_{in} with a width of $T_m \cos(\omega_m k T_{in})$ [Fig. 2.17(b)]. If $T_m \ll T_{in}$, the latter can be

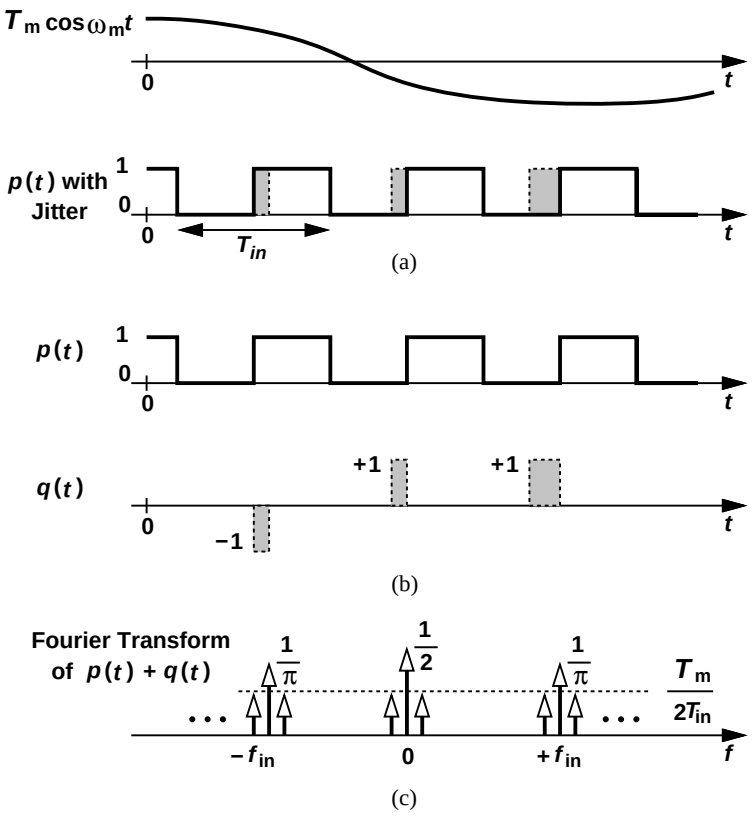


Figure 2.17: (a) Square wave with modulated rising edges, (b) decomposition into two waveforms, and (c) resulting magnitude of Fourier transform.

approximated by a train of impulses and expressed as

$$q(t) \approx T_m \sum_{k=-\infty}^{k=+\infty} \cos(\omega_m k T_{in})\ \delta(t - kT_{in}). \tag{2.24}$$

Adding the Fourier transforms of $p(t)$ and $q(t)$, we obtain the result shown in Fig. 2.17(c), where each harmonic of the square wave is surrounded by two impulses of area $T_m/(2T_{in})$ at frequency offsets of $\pm f_m = \pm\omega_m/(2\pi)$. It can be shown that these sidebands generate only phase modulation (PM).

We thus observe that a jitter spectrum consisting of two impulses having an area of $T_m/2$ produces two PM sidebands around f_{in} whose normalized magnitude is equal to $\pi T_m/(2T_{in})$. That is, a jitter of $T_m/2$ yields a phase disturbance of

$(\pi/T_{in})(T_m/2)$ rather than $(2\pi/T_{in})(T_m/2)$ in this case. One may expect this result because only the rising edges have been displaced.

We now generalize the foregoing observation to random jitter, while still assuming jitter on only the rising edges. If the jitter itself in the time domain is denoted by $\sigma(t)$, then Eq. (2.24) is rewritten as

$$q(t) \approx \sigma(t) \sum_{k=-\infty}^{k=+\infty} \delta(t - kT_{in}). \tag{2.25}$$

Adding the power spectral densities of $p(t)$ and $q(t)$, we obtain the overall spectrum shown in Fig. 2.18. Thus, the jitter spectrum, $S_\sigma(f)$, is shifted to $\pm f_{in}$, $\pm 2f_{in}$, etc., scaled by a factor of $1/{T_{in}}^2$, and normalized to a carrier power of $1/\pi^2$, yielding $(\pi^2/{T_{in}}^2)S_\sigma(f \pm f_{in})$, etc., for the phase noise.[7] MATLAB simulations confirm this result.

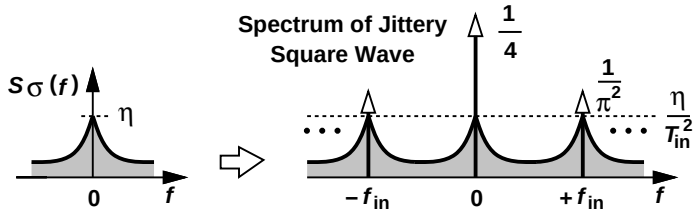


Figure 2.18: Spectrum of jittery square wave.

Since the jitters on the rising and falling edges of a CMOS inverter's output are generated by different transistors and are hence uncorrelated, we write the overall phase noise of the square wave as

$$S_\Phi(f) = \frac{\pi^2}{{T_{in}}^2} \sum_{k=-\infty}^{k=+\infty} [S_{\sigma p}(f \pm k f_{in}) + S_{\sigma n}(f \pm k f_{in})], \tag{2.26}$$

[7]Using Rice's approximation of random noise by a sum of sinusoids [9], it can be proved that the spectra at $\pm f_{in}$ produce only phase modulation.

where $S_{\sigma p}$ and $S_{\sigma n}$ denote the spectra of the jitters produced by the PMOS and NMOS transistors, respectively. Note that S_σ and S_{Vn} are simply related by a factor of r_{edge}^2.

2.10 Spectrum of Shaped and Sampled White Noise

In this section, we examine the phase noise spectrum due to white noise:

$$S_\Phi(f) = \frac{\pi^2}{r_{edge}^2 T_{in}^2} \sum_{m=-\infty}^{m=+\infty} S_{Vn}(f - \frac{m}{T_{in}}). \tag{2.27}$$

Since the Fourier transform of the rectangular window, $w(t)$, is given by $\Delta T \times \sin(\pi f \Delta T)/(\pi f \Delta T)$, we have from (2.4)

$$S_{Vn}(f) = \frac{1}{C_L^2} \Delta T^2 \frac{\sin^2(\pi f \Delta T)}{(\pi f \Delta T)^2} S_{In}(f). \tag{2.28}$$

If $S_{In}(f)$ is white, then $S_{Vn}(f)$ has a $sinc^2$ shape; i.e., $S_\Phi(f)$ consists of $sinc^2$ functions centered at $mf_{in} = m/T_{in}$. We now prove that the sum of these $sinc^2$ functions is a flat line under a certain condition.

Considering only the $sinc^2$ shape itself, we recognize that the inverse Fourier transform of $\Delta T^2 sinc^2(\pi f \Delta T)$ is a triangle, $g(t)$, with a time duration of $-\Delta T$ to $+\Delta T$ and a height of ΔT [Fig. 2.19(a)]. As a result of shifts of $sinc^2$ by mf_{in} in the frequency domain, $g(t)$ is multiplied by $exp(j2\pi m f_{in} t)$ in the time domain:

$$g(t) \sum_{m=-\infty}^{m=+\infty} e^{j2\pi m f_{in} t} \leftrightarrow \sum_{m=-\infty}^{m=+\infty} \Delta T^2 \frac{\sin^2[\pi \Delta T(f - m f_{in})]}{[\pi \Delta T(f - m f_{in})]^2}. \tag{2.29}$$

We also note that

$$\sum_{m=-\infty}^{m=+\infty} e^{j2\pi m f_{in} t} = \frac{1}{f_{in}} \sum_{m=-\infty}^{m=+\infty} \delta(t - m T_{in}). \tag{2.30}$$

In other words, $g(t)$ is multiplied by a train of impulses centered at mT_{in} [Fig. 2.19(b)]. Thus, if the duration of $g(t)$ is short enough to enclose only the impulse

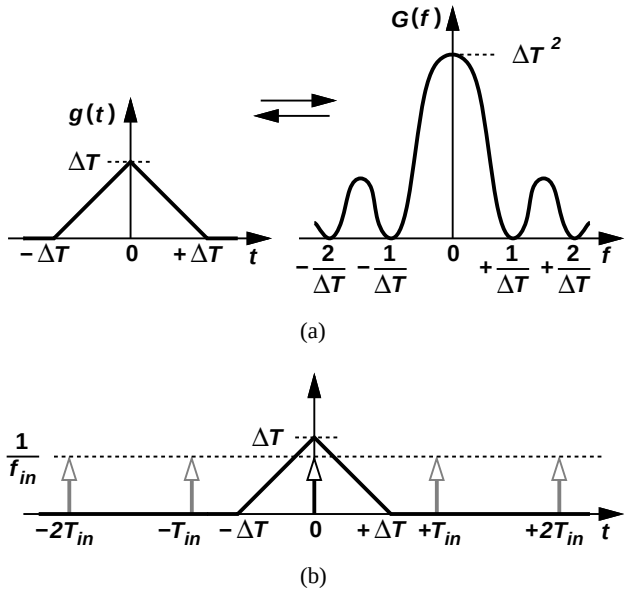


Figure 2.19: Inverse Fourier transform of (a) $sinc^2$ function, and (b) shifted $sinc^2$ functions.

at $t = 0$, we have

$$g(t) \sum_{m=-\infty}^{m=+\infty} e^{j2\pi m f_{in} t} = \Delta T \frac{1}{f_{in}} \delta(t). \tag{2.31}$$

The Fourier transform of this result is equal to $\Delta T / f_{in}$ and hence:

$$\sum_{m=-\infty}^{m=+\infty} \Delta T^2 \frac{\sin^2[\pi \Delta T (f - m f_{in})]}{[\pi \Delta T (f - m f_{in})]^2} = \frac{\Delta T}{f_{in}}, \tag{2.32}$$

which is a flat line.

In summary, if the sampling period, T_{in}, is greater than the rectangular window width, ΔT, then the window-integrated and sampled white noise still has a white spectrum. Note that this result is valid for any shape chosen for $w(t)$ so long as the inverse Fourier transform of $|W(f)|^2$ has a total time duration less than $2T_{in}$, or more generally, so long as the inverse Fourier transform of $|W(f)|^2$ crosses zero at $t = mT_{in}$ except for $t = 0$.

2.11 Conclusion

The phase noise of PFDs can manifest itself within the bandwidth of PLLs, corrupting the transmitted and received signal constellations. This chapter analyzes the phase noise of two PFD topologies based on the approximations made for a CMOS inverter. It is also shown that the PFD phase noise is not merely that of the Up and Down pulses. Simulations using each PFD in a PLL reveal good agreement with analytical predictions, indicating, most notably, the dependence of the phase noise on the frequency of operation.

CHAPTER 3

Relation Between Delay Line Phase Noise and Ring Oscillator Phase Noise

The phase noise of a ring oscillator can be obtained by multiplying its open-loop phase noise by a simple shaping function. The shaping function is computed using first principles and is applicable to both flicker-noise-induced and white-noise-induced phase noise, leading to compact equations for ring oscillators. It is also shown that flicker noise upconversion in ring oscillators is primarily a function of the total gate capacitance and inevitable regardless of the risetime and falltime symmetry. Two oscillator prototypes fabricated in 65-nm CMOS technology verify the validity of the results.

3.1 Introduction

It has been recognized for more than two decades that delay lines exhibit less phase noise than ring oscillators do [10]. This advantage is intuitively explained by the lack of jitter accumulation in the former but has not been quantified analytically.

The phase noise in ring oscillators has been studied extensively [11]-[18]. In this chapter, we offer an analysis that leads to a direct relation between the phase noise of delay lines and that of ring oscillators, allowing comparison of

their performance for a given power dissipation and operation frequency. We begin with first principles and establish a unified relation for both white and $1/f$ noise sources. As a byproduct, our analysis also shows that the flicker-noise-induced phase noise is inversely proportional to the total gate capacitance present in a ring oscillator and relatively independent of the symmetry between rise and fall transitions. The proposed relation is experimentally verified on 9-stage and 19-stage prototypes fabricated in 65-nm CMOS technology.

Section 3.2 deals with the phase noise of delay lines, expressing their jitter as two impulse trains. Section 3.3 analyzes jitter accumulation in a ring oscillator and utilizes the results from Section 3.2 to arrive at the the proposed relation. Section 3.4 derives some useful results, including compact phase noise equations, and Section 3.5 and 3.6 respectively present simulation and experimental confirmations of the equations. Section 3.7 concludes this chapter.

3.2 Phase Noise of Delay Lines

Let us consider the chain of inverters shown in Fig. 3.1(a) as a representative delay line, with the dummy load added to ensure uniform delays. Since the inverters exhibit uncorrelated noise, the overall phase noise (as a power quantity) is equal to that of one multiplied by the number of stages (if they are identical).

For our purposes, we tentatively assume that only the second inverter in Fig. 3.1(a) has noise. We also select the input frequency equal to the oscillation frequency of this chain as if it were reconfigured to become a ring oscillator, i.e., $f_{in} = 1/(6T_d)$, where T_d denotes the average gate delay. Thus, as V_0 propagates to V_3, it experiences three gate delays and the jitter of one inverter [Fig. 3.1(b)]. In other words, the falling edges of V_3 are aligned with the falling edges of V_0 but

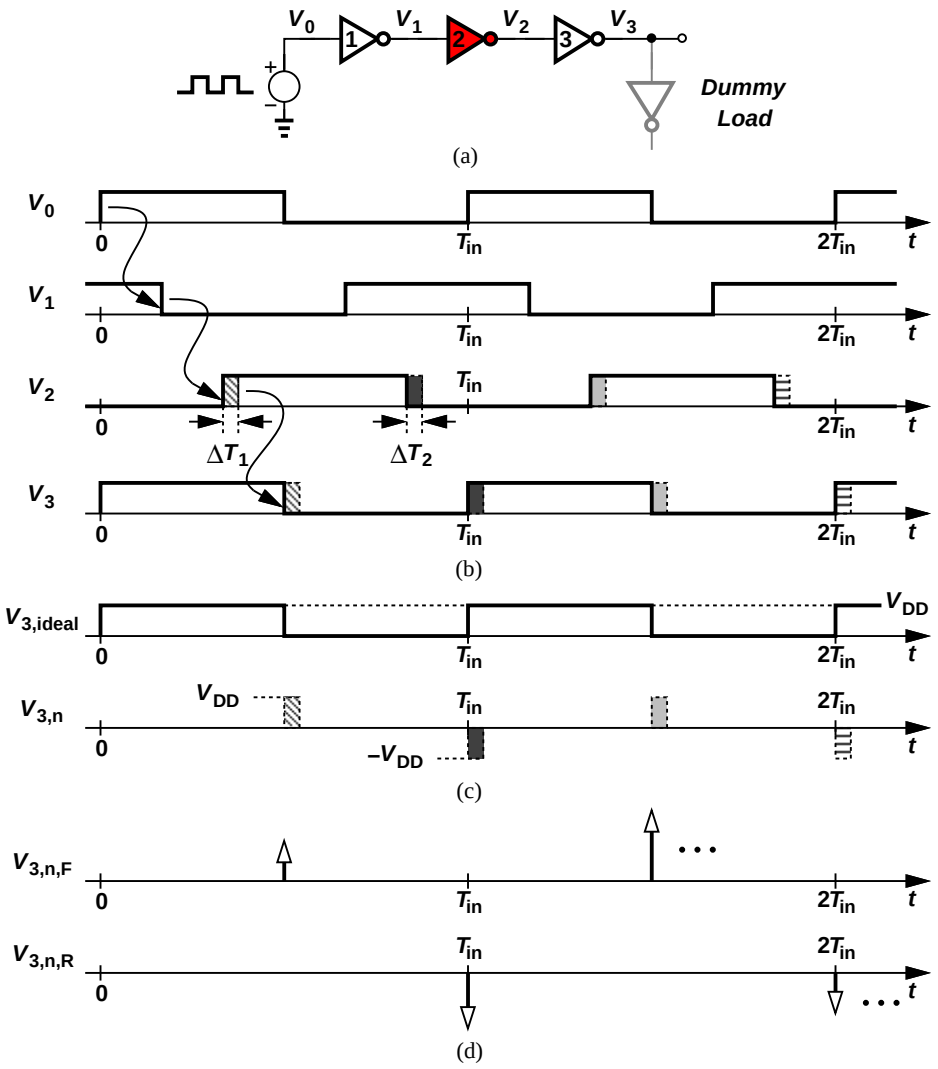


Figure 3.1: (a) Three-stage delay line with only one noisy inverter, (b) node voltages in response to a frequency equal to the oscillation frequency of a three--stage ring oscillator, (c) decomposition of the output voltage to an ideal noiseless square wave and a noise waveform, and (d) approximation of the noise waveform in (c) to two uncorrelated weighted impulse trains.

modulated by the second inverter's jitter.

The output of the third inverter in Fig. 3.1(a) can be decomposed into an ideal

square wave and a train of narrow pulses [19, 20] that occur every $3T_d = T_{in}/2$ seconds [Fig. 3.1(c)]. Since the jitters on the rising and falling edges arise from different noise sources and are uncorrelated [21], we denote them by $\sigma_R(t)$ and $\sigma_F(t)$, respectively. Now, $V_{3,n}$ in Fig. 3.1(c) itself can be approximated as the sum of a positive impulse train weighted by $\sigma_F(t)$ and a negative impulse train weighted by $\sigma_R(t)$ [Fig. 3.1(d)]:

$$\begin{aligned} V_{3,n}(t) &= V_{3,n,F}(t) + V_{3,n,R}(t) \\ &= \sum_{n=-\infty}^{\infty} \sigma_F[(2n+1)\frac{T_{in}}{2}]\ \delta[t-(2n+1)\frac{T_{in}}{2}] \\ &- \sum_{n=-\infty}^{\infty} \sigma_R(2n\frac{T_{in}}{2})\ \delta(t-2n\frac{T_{in}}{2}) \end{aligned} \tag{3.1}$$

With the aid of Fig. 3.1(d), we recognize that the phase noise of the chain is equal to the sum of the power spectral densities of $V_{3,n,F}$ and $V_{3,n,R}$ normalized to the power of the first harmonic of $V_{3,ideal}$ [21]. We derive the phase noise expression in Section 3.4.

3.3 Phase Noise of Ring Oscillators

The perspective described above for the phase noise of delay lines proves useful in the phase noise analysis of ring oscillators as well. Suppose the delay line of Fig. 3.1(a) is reconfigured to form a ring oscillator as shown in Fig. 3.2(a) (without the dummy load).

We perform a "gedankenexperiment" in which (1) the voltage source V_{in} applies a noiseless rising edge to the input of the first inverter at $t = 0^-$ and is disconnected from the circuit at $t = 0$, and (2) the second inverter produces jitter only once (i.e., a single time displacement) as this edge propagates through the chain and remains noiseless thereafter. Thus, the input rising edge arrives

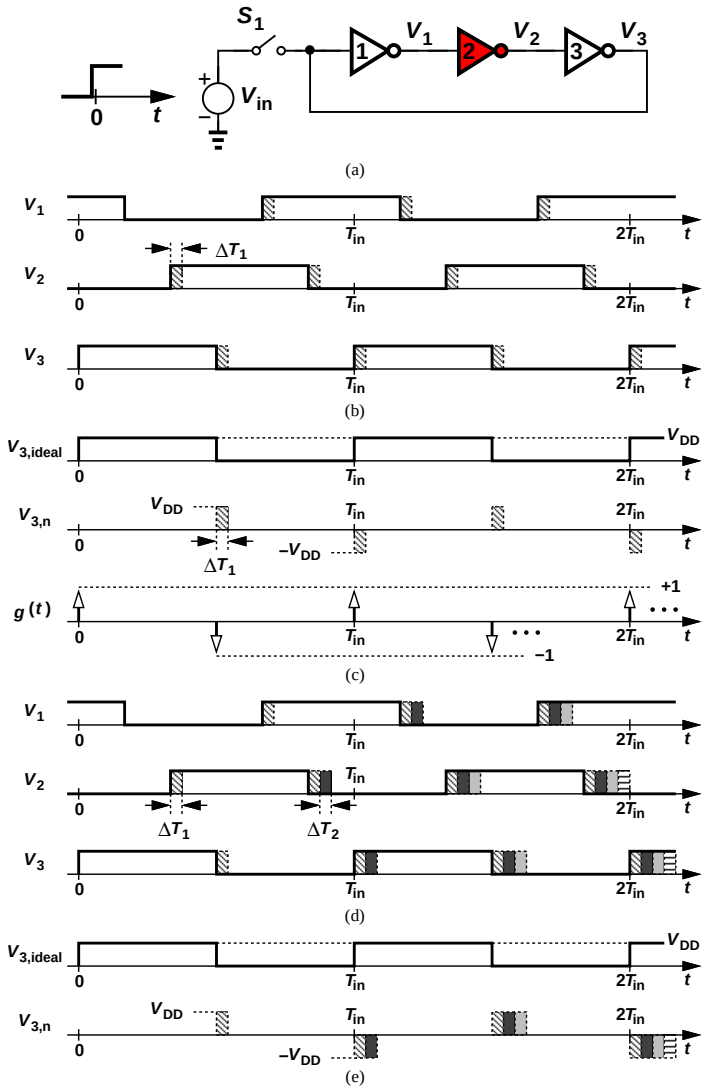


Figure 3.2: (a) Three-stage ring oscillator retimed at $t = 0$ with only one noisy inverter, (b) jitter on all edges due to a single jitter event on V_2, (c) decomposition of V_3 in (b) to an ideal noiseless square wave and a noise waveform, with $g(t)$ serving as a "carrier," (d) jitter on edges when inverter #2 adds jitter on every transition, (e) decomposition of V_3 in (d) to an ideal noiseless square wave and a noise waveform.

at V_3 with a delay equal to $3T_d$ plus the jitter of the second inverter, ΔT_1. As this edge circulates around the ring, it experiences no more jitter; i.e., all of the subsequent edges are simply displaced by a constant equal to ΔT_1. Figure 3.2(b) illustrates this effect.

The output waveform obtained in the above experiment can be decomposed as shown in Fig. 3.2(c) and expressed as a single pulse of width ΔT_1, convolved with an alternating train of impulses, $g(t)$. Note that $g(t) = 0$ for $t < 0$. We can consider $g(t)$ as "carrier" for the time displacements.

We now repeat the above experiment while assuming that the second inverter is noisy at all times. The second time the oscillation edge passes through this inverter, the jitter causes one additional displacement, ΔT_2, as depicted by the dark shading in Fig. 3.2(d). The effect of this shift can be obtained by convolving a pulse of width ΔT_2 with $g(t)$ and adding the result to an ideal, noiseless waveform. Note that this calculation holds valid whether or not ΔT_1 and ΔT_2 are correlated.

The foregoing observations suggest that the ring oscillator output can be decomposed into an ideal square waveform and a noise component [Fig. 3.2(e)] given by

$$\begin{aligned} V_{n,ring}(t) &= \left\{ \sum_{n=-\infty}^{\infty} \sigma_R[(2n+1)\frac{T_{in}}{2}]\ \delta[t-(2n+1)\frac{T_{in}}{2}] \right\} * g(t) \\ &- \left\{ \sum_{n=-\infty}^{\infty} \sigma_F(2n\frac{T_{in}}{2})\ \delta(t-2n\frac{T_{in}}{2}) \right\} * g(t). \end{aligned} \tag{3.2}$$

From (3.1) and (3.2), it follows that the delay line phase noise, $S_{\Phi,DL}(f)$, and the ring oscillator phase noise, $S_{\Phi,ring}(f)$, are related as[1]

$$S_{\Phi,ring}(f) = S_{\Phi,DL}(f)|G(f)|^2, \tag{3.3}$$

[1]Throughout this chapter, all the spectra are two-sided, and the phase noise is denoted by S_Φ.

where $|G(f)|^2$ denotes the spectrum of $g(t)$.

Equation (3.3) is a general result and merits a few remarks. First, (3.3) applies to the phase noise due to both white noise and flicker noise. Second, (3.3) holds for the phase noise arising from *all* of the devices in the delay line and the ring. Third, (3.3) is not limited to CMOS inverters and can be used for differential delay stages and rings as well.

To determine $|G(f)|^2$, we first write

$$g(t) = \left[\sum_{n=-\infty}^{\infty} \delta(t - nT_{in}) - \sum_{n=-\infty}^{\infty} \delta(t - nT_{in} - \frac{T_{in}}{2})\right] u(t), \tag{3.4}$$

and hence

$$G(f) = \left[\frac{1}{T_{in}}\ (1 - e^{-j\pi f T_{in}}) \sum_{n=-\infty}^{\infty} \delta(f - nf_{in})\right] * \left[\frac{1}{j2\pi f} + \frac{1}{2}\delta(f)\right], \tag{3.5}$$

which simplifies to

$$G(f) = \left\{\frac{2}{T_{in}} \sum_{n=-\infty}^{\infty} \delta[f - (2n+1)f_{in}]\right\} * \left[\frac{1}{j2\pi f} + \frac{1}{2}\delta(f)\right]. \tag{3.6}$$

The unit step in (3.4) ensures the causality of jitter accumulation, i.e., the jitter generated at any edge is present for only subsequent edges. Figure 3.3 plots the magnitude of $G(f)$, revealing how the delay line phase noise is shaped to produce the ring oscillator phase noise.

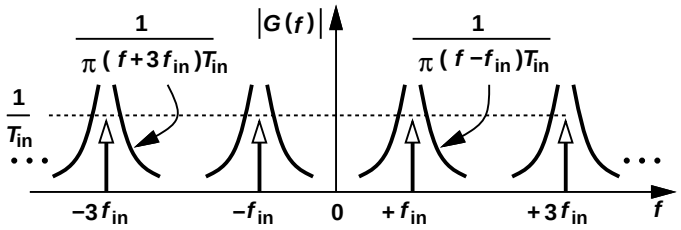


Figure 3.3: Fourier transform of $g(t)$.

At an offset frequency of Δf with respect to the fundamental frequency, $f_{in} = 1/T_{in}$, we have

$$\begin{aligned} G(f_{in} + \Delta f) &= \frac{2}{T_{in}} \sum_{n=-\infty}^{\infty} \frac{1}{j2\pi(\Delta f + 2nf_{in})} \\ &= \frac{1}{j2\pi} \left\{ \frac{2f_{in}}{\Delta f} + \sum_{n=1}^{\infty} \frac{\Delta f / f_{in}}{[\Delta f/(2f_{in})]^2 - n^2} \right\} \\ &= \frac{1}{j2\pi} \left[\pi \cot(\frac{\pi \Delta f}{2f_{in}}) \right]. \end{aligned} \tag{3.7}$$

Thus, Eq. (3.3) can be rewritten as

$$S_{\Phi,ring}(\Delta f) = S_{\Phi,DL}(\Delta f) \frac{1}{4} \cot^2(\frac{\pi \Delta f}{2f_{in}}). \tag{3.8}$$

For offset frequencies much less than f_{in}, we have $\cot^2[\pi \Delta f/(2f_{in})] \approx [2f_{in}/(\pi \Delta f)]^2$. Changing our notation from f_{in} to f_{osc}, we write

$$S_{\Phi,ring}(\Delta f) = S_{\Phi,DL}(\Delta f) \left(\frac{f_{osc}}{\pi \Delta f} \right)^2. \tag{3.9}$$

This simple, fundamental relation holds for phase noise due to both $1/f$ and white noise.

3.4 Useful Insights

Equation (3.9) provides a multitude of interesting and useful insights into the phase noise behavior of ring oscillators. Of course, it confirms that white noise and flicker noise lead to $1/\Delta f^2$ and $1/\Delta f^3$ phase noise profiles because the corresponding delay line phase noise profiles are respectively flat and proportional to $1/\Delta f$ [21]. This section presents some other insights that may benefit the circuit designer.

3.4.1 Comparison of Delay Lines and Ring Oscillators

Equation (3.9) indicates that conversion of a delay line to a ring oscillator shapes the phase noise by an $f_{osc}^2/(\pi\Delta f)^2$ function. Since Δf is usually much less than f_{osc}/π, we observe that $S_{\Phi,ring}(\Delta f) \gg S_{\Phi,DL}(\Delta f)$ for a given power dissipation and fundamental frequency. Why are low noise frequencies scaled by a greater factor? Consider the scenario depicted in Fig. 3.4(a), where one of the noise

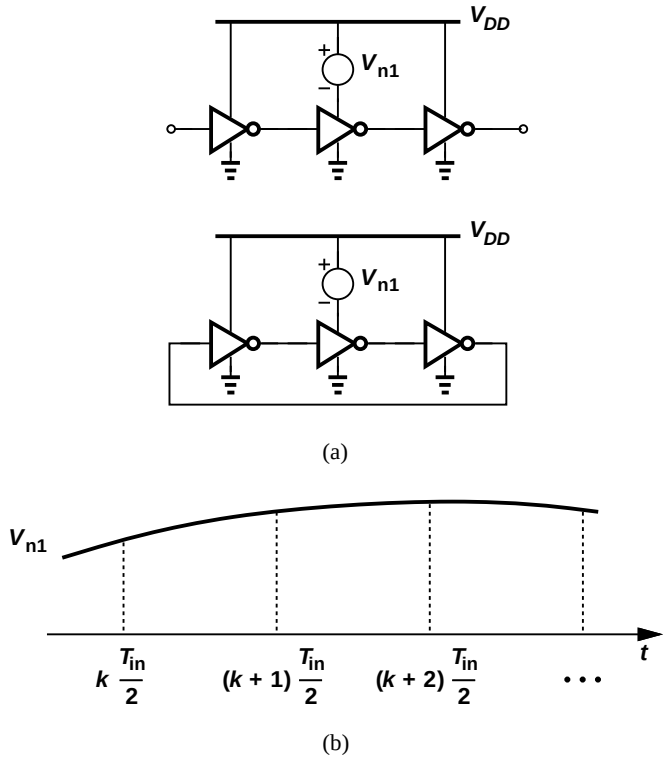


Figure 3.4: (a) Delay line and ring oscillator with one equivalent noise source, V_{n1}, and (b) V_{n1} shown as a low-frequency component.

sources of the second inverter, V_{n1}, is explicitly shown and placed in series with V_{DD}; for example, V_{n1} represents the noise of the PMOS transistor in the inverter. Suppose V_{n1} varies at a rate much lower than the operation frequency, f_{in} [Fig. 3.4(b)]. We observe that the delay line simply experiences a relatively constant

phase shift at $t = kT_{in}/2$, $t = (k+1)T_{in}/2$, etc., so long as V_{n1} changes negligibly. In the ring oscillator, on the other hand, the time displacements caused by V_{n1} at $t = kT_{in}/2$, $t = (k+1)T_{in}/2$, etc., continue to accumulate until V_{n1} changes polarity. The lower the frequency of V_{n1}, the longer and larger this accumulation is, producing the $1/\Delta f^2$ shaping function.

3.4.2 Compact Phase Noise Equations

The phase noise of an inverter is derived in [21] as

$$S_{\Phi,white} = \left\{ \frac{\pi^2 \Delta T}{r_{edge}^2 C_L^2 T_{in}} S_I(f) \right\}_{NMOS} + \left\{ \frac{\pi^2 \Delta T}{r_{edge}^2 C_L^2 T_{in}} S_I(f) \right\}_{PMOS} + \frac{2\pi^2}{r_{edge}^2 T_{in}} \frac{kT}{C_L}. \tag{3.10}$$

for white noise sources and as

$$S_{\Phi,1/f} = \left\{ \frac{\pi^2 \Delta T^2}{r_{edge}^2 C_L^2 T_{in}^2} S_{1/f}(f) \right\}_{NMOS} + \left\{ \frac{\pi^2 \Delta T^2}{r_{edge}^2 C_L^2 T_{in}^2} S_{1/f}(f) \right\}_{PMOS} \tag{3.11}$$

for flicker noise sources, where r_{edge} is the slew rate, C_L the load capacitance, T_{in} the input period, $S_I(f)$ the thermal noise current, $S_{1/f}(f)$ the flicker noise current, k the Boltzmann constant, T the absolute temperature, and ΔT the equivalent "on" time for each transistor [21].

In order to derive a compact expression for the delay line, we make three simplifying assumptions. (1) The equivalent on time, ΔT, is approximately equal to the gate delay, T_d. (2) The slew rate, r_{edge}, can be approximated as I_D/C_L, where I_D denotes the drain current of the on transistor when its gate voltage is near the rail and its drain voltage around $V_{DD}/2$ [21]. (3) The slew rate can also be approximated as $V_{DD}/(2T_d)$ [22].

It follows from Eqs. (3.10) and (3.11) that for M noisy inverters in a delay

line,

$$S_{\Phi,white,DL} = M\frac{\pi^2 T_d}{I_D^2 T_{in}}[S_I(f)|_{NMOS} + S_I(f)|_{PMOS}] + M\frac{4kT\pi^2 T_d}{I_D V_{DD} T_{in}}, \tag{3.12}$$

$$S_{\Phi,1/f,DL} = M\frac{\pi^2 T_d^2}{I_D^2 T_{in}^2}[S_{1/f}(f)|_{NMOS} + S_{1/f}(f)|_{PMOS}], \tag{3.13}$$

where it is assumed I_D is the same for NMOS and PMOS devices. In the special case where the input period is equal to the period of the corresponding ring oscillator, we have $1/f_{osc} = T_{in} = 2MT_d$, and (3.12) and (3.13) reduce to

$$S_{\Phi,white,DL} = \frac{\pi^2}{2I_D^2}[S_I(f)|_{NMOS} + S_I(f)|_{PMOS}] + \frac{2kT\pi^2}{I_D V_{DD}}, \tag{3.14}$$

$$S_{\Phi,1/f,DL} = \frac{\pi^2}{4MI_D^2}[S_{1/f}(f)|_{NMOS} + S_{1/f}(f)|_{PMOS}]. \tag{3.15}$$

With the aid of Eq. (3.9), we can now express the phase noise of an M-stage ring oscillator as:

$$S_{\Phi,white,ring}(\Delta f) = \frac{f_{osc}^2}{\Delta f^2}\left\{\frac{1}{2I_D^2}[S_I(\Delta f)|_{NMOS} + S_I(\Delta f)|_{PMOS}] + \frac{2kT}{I_D V_{DD}}\right\}, \tag{3.16}$$

$$S_{\Phi,1/f,ring}(\Delta f) = \frac{f_{osc}^2}{4MI_D^2\Delta f^2}\left[S_{1/f}(\Delta f)|_{NMOS} + S_{1/f}(\Delta f)|_{PMOS}\right]. \tag{3.17}$$

Note that these spectra are two-sided (i.e., $-\infty < f < +\infty$). Accounting for the factor of 2 difference between one-sided and two-sided spectra, we observe that the phase noise given by Eq. (3.17) is still twice that reported in [7]. As verified by the simulations in Section 3.5, our result is correct. The factor of 2 error in [7] can be explained as follows. For a voltage-controlled oscillator (VCO) sensing a small sinusoidal voltage of peak V_m and frequency f_m, the relative magnitude of the sideband at the output is given by $K_{VCO}V_m/(2f_m)$, where K_{VCO} is the gain in Hz/V. It is tempting, but incorrect, to use this result directly for random noise, i.e., to write $K_{VCO}^2 S_n/(4f_m^2)$ for the phase noise resulting from noise with spectral density S_n [7]. Since phase noise is in fact the spectrum of Φ_n in $\cos(\omega_c t + \Phi_n)$, we

integrate noise with respect to time and multiply the result by K_{VCO}, obtaining $S_{\Phi_n}(f_m) = K_{VCO}^2 S_n / f_m^2$. If S_n denotes a one-sided spectrum, then this result must be divided by a factor of 2 so as to represent a two-sided $S_{\Phi_n}(f_m)$, producing $S_{\Phi_n}(f_m) = K_{VCO}^2 S_n / (2f_m^2)$.

Equation (3.16) reveals that $S_{\Phi,white,ring}$ is independent of the number of stages, as recognized in prior work [7, 13]. To confirm that $S_{\Phi,white,ring}$ is fundamentally related to the power consumption (also recognized in [7, 13]), suppose two rings incorporate identical inverters, but one contains M_1 stages and the other M_2, where $M_1 > M_2$. We add enough capacitance to each node in the second ring so that the gate delays of the two rings, T_{d1} and T_{d2}, respectively, satisfy the relation $M_1 T_{d1} = M_2 T_{d2}$ and thus yield the same oscillation frequency. Since the gate delays are proportional to the load capacitances, it follows that $M_1 C_{L1} = M_2 C_{L2}$ and hence $f_{osc}(M_1 C_{L1}) V_{DD}^2 = f_{osc}(M_2 C_{L2}) V_{DD}^2$. That is, equal oscillation frequencies guarantee equal power consumptions in this case. Since the inverters are identical in the two designs, I_D and $S_I(\Delta f)$ in Eq. (3.16) are the same for the two oscillators, yielding the same $S_{\Phi,white,ring}(\Delta f)$.

Equation (3.17) shows that the phase noise due to flicker noise *falls* as the number of stages increases [7]. This is also observed in the simulation results of Section 3.5.

3.4.3 Effect of Transition Symmetry on Flicker Noise Upconversion

The fundamental relation expressed by Eq. (3.9) implies that if flicker noise is upconverted in a delay line, so is it in a ring oscillator utilizing that delay line. Thus, the upconversion phenomenon can be studied in a simpler delay line environment.

The flicker-noise-induced phase noise of delay lines is formulated by Eq.

(3.11), with ΔT representing a quantity roughly equal to half of the transition time caused by the NMOS or PMOS transistor in each stage. Interestingly, this equation suggests that the flicker noise is upconverted regardless of the relationship between ΔT_{NMOS} and ΔT_{PMOS}, a point in contradiction to the analysis in [13], which predicts zero upconversion if the rise and fall transitions are symmetric. In fact, as shown in Fig. 3.5(a), phase noise simulations of a 9-stage 2.4-GHz ring oscillator reveal that the phase noise changes by only a few decibels as the PMOS-to-NMOS width ratio varies from 1/4 to 4/1 and the risetime-to-falltime ratio from 3 to 0.76. This weak dependence is also verified by examining the upconversion of a 1-MHz tone placed in series with the gate of one NMOS transistor in the ring. Figure 3.5(b) reveals that the FM sideband magnitude varies little.

The flaw in [13] can be explained as follows. Since the flicker noise currents injected by the NMOS and PMOS devices in a ring are uncorrelated, each must be characterized by its own impulse sensitivity function (ISF). Depicted in Fig. 3.5(c), the NMOS and PMOS ISFs cannot have zero time average with any choice of rise and fall transitions, thereby upconverting flicker noise unconditionally.

3.4.4 Effect of Scaling on Phase Noise

The white-noise-induced phase noise appears to be fundamentally related to the power dissipation and not much to the other factors. The effect of flicker noise, on the other hand, can be articulated by rewriting Eq. (3.17) as

$$S_{\Phi,1/f,ring}(\Delta f) = \frac{f_{osc}^2}{8\Delta f^3}\left[\left\{\frac{K}{MWLC_{ox}(V_{DD}-V_{TH})^2}\right\}_{NMOS}+\left\{\frac{K}{MWLC_{ox}(V_{DD}-V_{TH})^2}\right\}_{PMOS}\right], \tag{3.18}$$

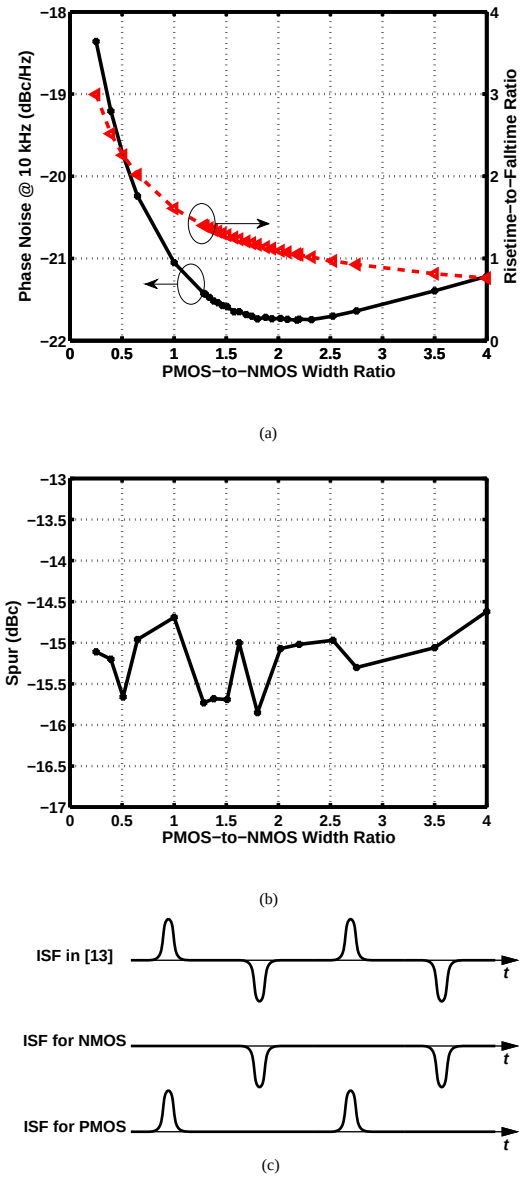


Figure 3.5: (a) Phase noise and risetime-to-falltime ratio versus the PMOS-to-NMOS width ratio of a 9-stage 2.4-GHz ring oscillator, (b) spur power when a small sinusoidal voltage source is put in series with the gate of one NMOS transistor in the ring, and (c) ISF reported in [13] and uncorrelated ISF's for NMOS and PMOS devices.

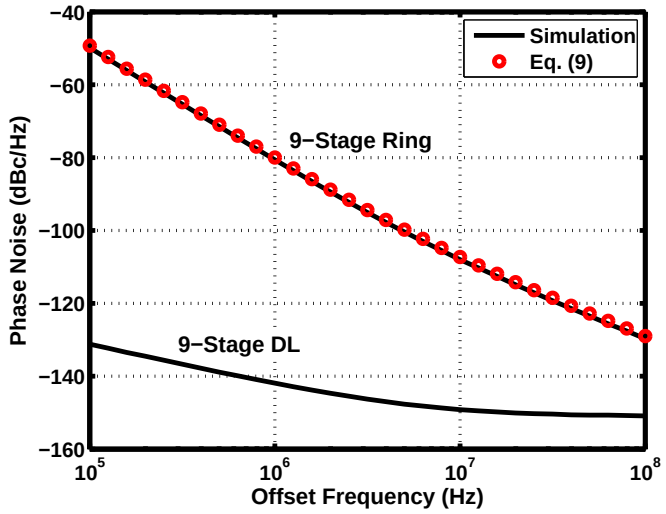
where it is assumed $g_m = I_D/(V_{GS} - V_{TH})$ for velocity-saturated devices and $K/(WLC_{ox}\Delta f)$ is assumed to be one-sided and is therefore divided by 2. It follows that the principal parameter under the designer's control for reducing the phase noise is the total gate capacitance, $MWLC_{ox}$, of the ring oscillator. For example, as simulations confirm, $S_{\Phi,1/f,ring}$ varies by less than 1 dB as M goes from 3 to 16 while MWL and f_{osc} are constant. Notwithstanding changes in K with technology scaling, $S_{\Phi,1/f,ring}$ rises with a lower $V_{DD} - V_{TH}$ if the total gate capacitance is kept constant.

3.5 Simulation Results

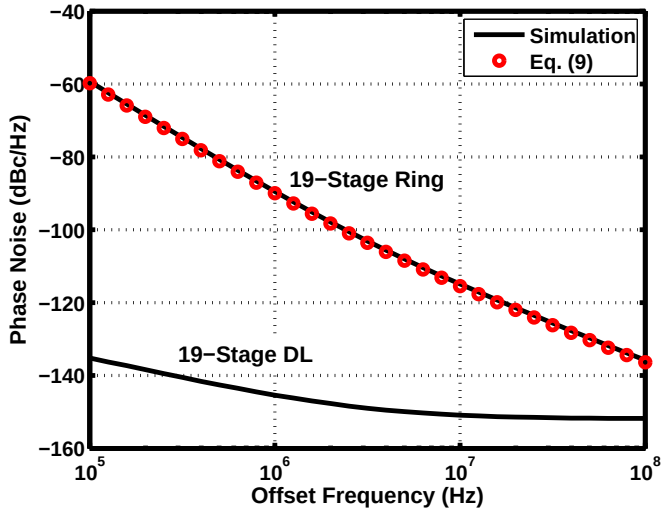
In this section, three sets of simulation results are presented: one to verify the fundamental shaping function, $f_{osc}^2/(\pi\Delta f)^2$, another to show the dependence of the phase noise on the number of delay stages, and the third to check the validity of our compact phase noise equations, (3.16) and (3.17).

In order to verify the relation expressed by Eq. (3.8), we have simulated 9-stage and 19-stage delay lines and ring oscillators in 65-nm CMOS technology. Each inverter incorporates a channel width of 0.6 μm and 1.2 μm for the NMOS and PMOS devices, respectively, and a channel length of 60 nm. The circuits operate with a 1-V supply. In each case, the frequency of the input applied to the delay line is chosen equal to the corresponding ring oscillator frequency.

Figure 3.6(a) plots the simulated phase noise for the 9-stage delay line and the corresponding ring oscillator. The latter's phase noise is obtained using (3.8) as well as direct simulations. We note good agreement in both flicker noise and white noise regimes. The oscillation frequency is 3.8 GHz and the power consumption 0.34 mW. Figure 3.6(b) repeats the results for a 19-stage arrangement operating



(a)



(b)

Figure 3.6: Simulated phase noise of delay lines and ring oscillators as well as calculated phase noise of the ring oscillator using the phase noise of the delay line for (a) 9-stage, and (b) 19-stage configurations.

at a frequency of 1.7 GHz and drawing 0.32 mW. The results agree well in this case, too.

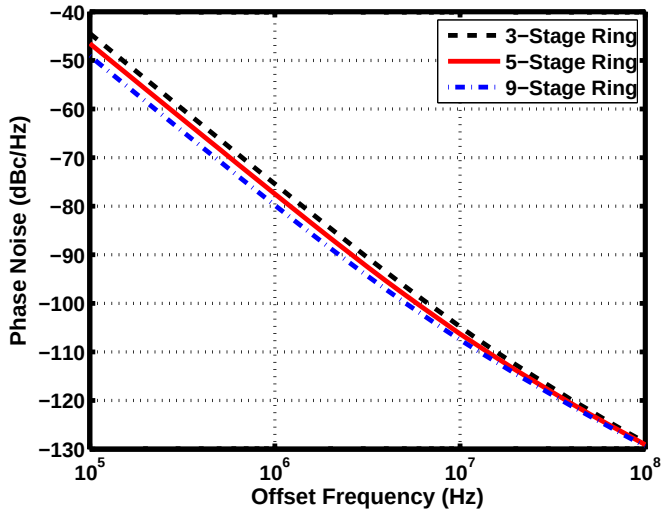


Figure 3.7: Simulated effect of number of delay cells on the phase noise of ring oscillators.

Figure 3.7 plots the simulated phase noise of three ring oscillators operating at 9.54 GHz. Explicit capacitors are added to all nodes of 3-stage and 5-stage rings. Since the power consumption varies slightly, from 1.39 mW to 1.47 mW, as the rings become longer, the phase noise plots are normalized to the corresponding values. We observe that the white-noise-induced phase noise remains unchanged as the number of stages increases, but, as predicted by Eq. (3.17), the flicker-noise-induced component decreases in proportion to M.

Figure 3.8 plots the simulated phase noise of the 9-stage ring oscillator as well as the calculated phase noise using Equations (3.16) and (3.17). (The flicker and white current noise spectra, $S_{1/f}$ and S_I, respectively, are obtained from simulations in Cadence).[2]

[2]The value of I_D is obtained from transient simulations at the point when $V_{DS} \approx V_{DD}/2$. The V_{GS} and V_{DS} values corresponding to this case are then used in a simple noise simulation of a single transistor.

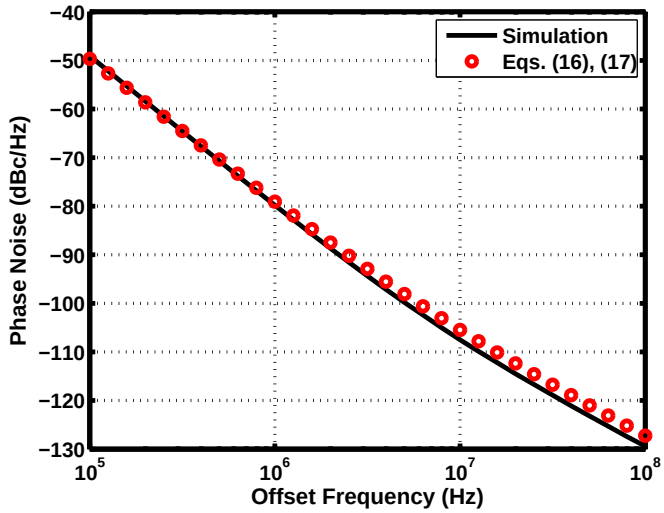


Figure 3.8: Simulated phase noise of a 9-stage ring oscillator and calculated phase noise using compact equations (3.16) and (3.17).

3.6 Experimental Results

The delay lines and ring oscillators described in Section 3.5 have been fabricated in 65-nm CMOS technology and characterized. Figure 4.15 shows a die photograph of the prototypes. Each circuit is followed by an on-chip open-drain buffer for driving 50-Ω instrumentation.

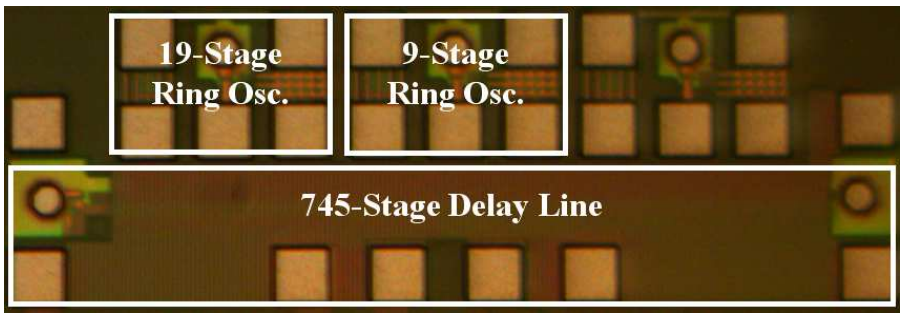


Figure 3.9: Die photograph.

The low phase noise of delay lines poses difficulties in measurement. For this

reason, the delay line prototype in fact incorporates 745 stages rather than 9 or 19, producing a readily measurable phase noise (Fig. 3.10). This value is then scaled down by a factor equal to 745/9 or 745/19 to obtain the phase noise of the respective delay lines.

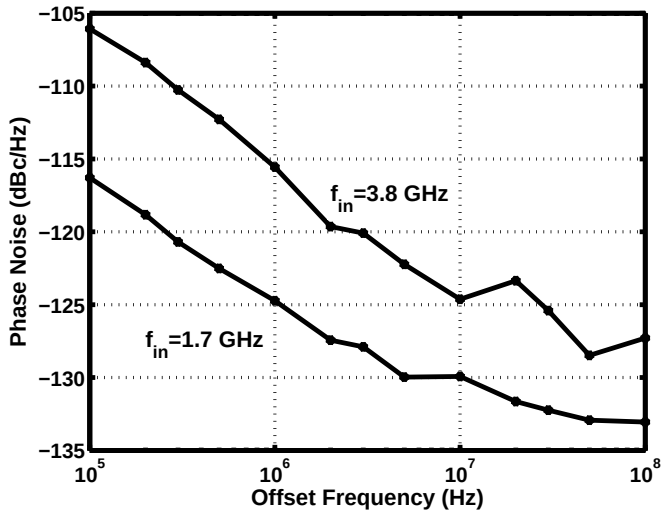


Figure 3.10: Measured phase noise of 745-stage delay line at two different input frequencies.

The phase noise of ring oscillators also proves difficult to measure if low offset frequencies are of interest. The random fluctuations of the free-running center frequency tend to smear the phase noise profile. It is therefore beneficial to phase-lock the oscillator to a low-noise input with a sufficiently small loop bandwidth so as to negligibly affect the phase noise in the offset frequency range of interest. Figure 3.11 shows the test setup constructed around each ring oscillator to create a type-I phase-locked loop (PLL). Here, an off-the-shelf mixer serves as a phase detector, comparing the phases of an external RF signal and the ring oscillator output. The latter's supply line acts as the control voltage. The loop bandwidth is set by the choice of the components in the low-pass filter.

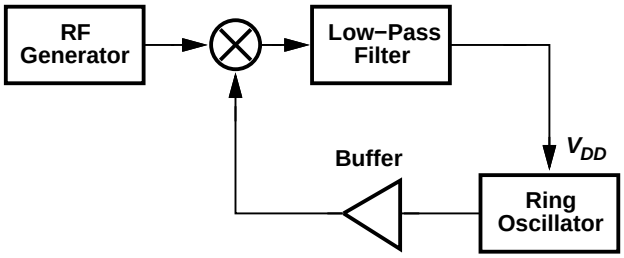
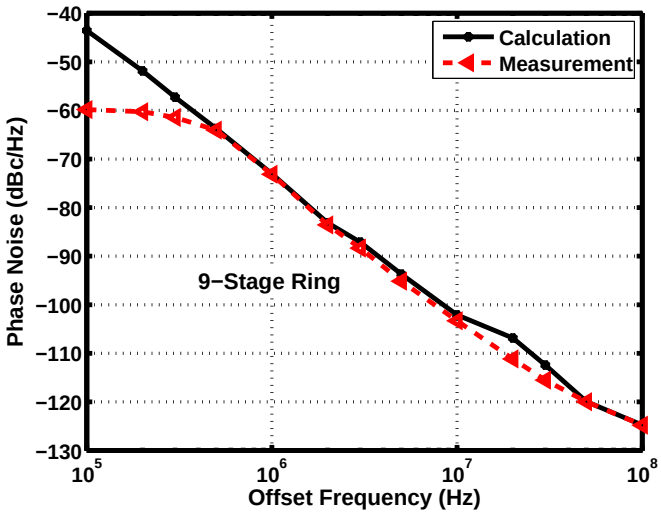


Figure 3.11: Phase-locking of the ring oscillators for phase noise measurements.

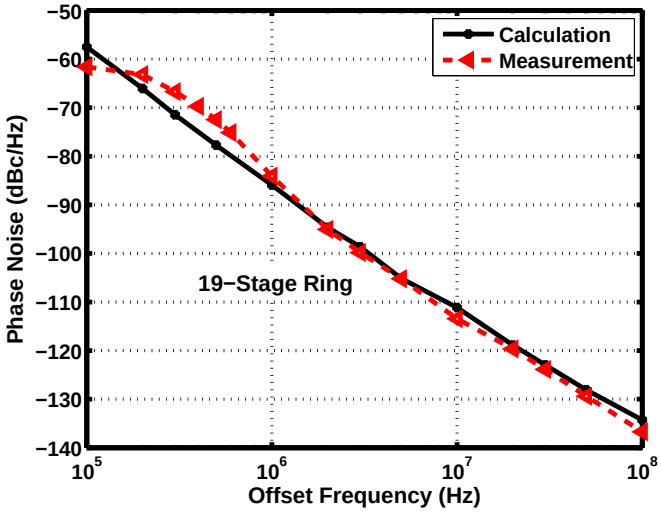
Figure 3.12(a) plots the phase noise of the 9-stage ring oscillator obtained by (a) direct measurement, and (b) by multiplying the measured delay line phase noise by $f_{osc}^2/(\pi\Delta f)^2$. We observe a reasonable agreement. Figure 3.12(b) repeats the results for the 19-stage configuration. In both cases, the effect of the PLL manifests itself at low offset frequencies.

3.7 Conclusion

It is shown that the closed-loop phase noise of a ring oscillator is equal to its open-loop phase noise multiplied by a simple shaping function, $f_{osc}^2/(\pi\Delta f)^2$. This relation reveals why delay lines exhibit much less noise than do ring oscillators. It also leads to compact phase noise equations and shows why flicker noise is upconverted even with symmetric rise and fall times. The flicker-noise-induced phase noise is not a strong function of the PMOS-to-NMOS ratio and the minimum phase noise does not necessarily happen when the rise and fall times are symmetric. The validity of the shaping function has been verified on two ring oscillators designed in 65-nm CMOS technology.



(a)



(b)

Figure 3.12: Measured phase noise of ring oscillators and the calculated phase noise using the measured phase noise of delay line for (a) 9-stage, and (b) 19-stage rings.

CHAPTER 4

A 5-GHz 11.6-mW CMOS Receiver for IEEE 802.11a Applications

4.1 Introduction

In today's mobile devices, the WiFi transceiver still consumes a relatively large amount of power. The receiver power is substantial due to the greater on-time of the receiver compared to the transmitter. Figure 4.1 shows a generic receiver system for 802.11a. While advances in the art have considerably reduced the

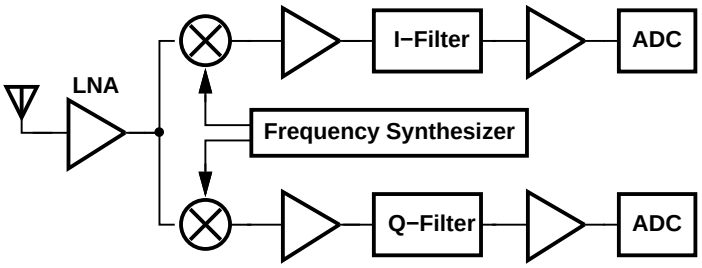


Figure 4.1: Generic 802.11a Receiver.

power consumption of analog-to-digital converters and frequency synthesizers, the main receiver (RX) chain draws disproportionately high power. For example, we can now realize each ADC in Fig. 4.1 with about 3 mW of power and the frequency synthesizer with about 5 mW. On the other hand, the receive path itself draws more than 45 mW [23]. It is therefore desirable to develop low-power RX front ends and baseband filters for WiFi applications.

This chapter introduces a complete 5-GHz CMOS receiver that meets the 11a sensitivity, blocking, and filtering requirements while consuming 11.6 mW. This fourfold reduction in power is achieved through the use of a transformer as a low-noise amplifier (LNA), passive mixers, and "non-invasive" baseband filtering [24].

Section 4.2 elaborates on the design of the transformer and Section 4.3 introduces the receiver architecture. Section 4.4 analyzes the current-driven passive mixers in a general form which is used in Section 4.5 to design the mixers connected to the transformer. Section 4.6 describes the baseband channel-select filters and Section 4.7 presents the experimental results. Section 4.8 concludes this chapter.

4.2 Transformers as LNAs

In the generic receiver of Fig. 4.1, the low-noise amplifier (LNA) provides voltage gain and proper input matching, but dissipates considerable amount of power. In order to realize a low-power receiver, we wish to remove the LNA or at least its power consumption. This becomes possible if a passive device with zero power consumption can serve as an LNA. A 1-to-N on-chip transformer provides voltage gain at the cost of power loss and noise figure degradation. It can also provide input matching as will be explained later. Thus, it seems that a transformer is a viable substitute for the LNA. However, its design is not straightforward. The principal point is to achieve a high voltage gain with low power loss at the frequency of interest. In particular, we would like to obtain a high coupling factor between the primary and the secondary. Consider the stacked structure [25] shown in Fig. 4.2(a) where spirals in high and low metal layers form the secondary and one spiral in middle metal layer forms the primary. This structure

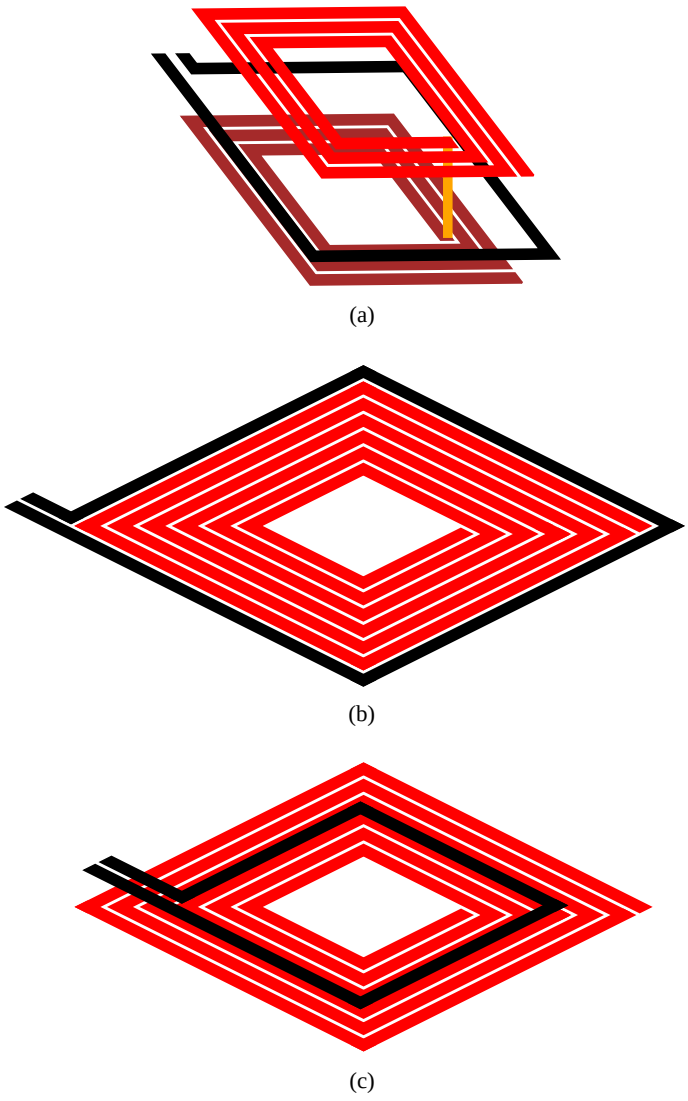


Figure 4.2: Various transformer topologies.

has a high coupling factor but, the high capacitance between the layers and the loss of the lower metal layers limit the performance. Note that the capacitance here sustains a larger voltage difference than in a planar structure [26] shown in Fig. 4.2(b). The self-resonance frequency and conductivity of the planar topology is much higher, but the coupling between the primary and the inner turns of the secondary is quite low. The optimum topology is shown in Fig. 4.2(c) where

a one-turn primary is stacked in the middle of the secondary. It is expected to have reasonable coupling, low loss, and small capacitance to be able to work at 5-GHz band. To reduce the loss, an octagonal shape has been used as shown in Fig. 4.3, with a one-turn primary in metal 8 and a six-turn secondary in metal 9. The outer diameters of the primary and the secondary are 146 μm and 170

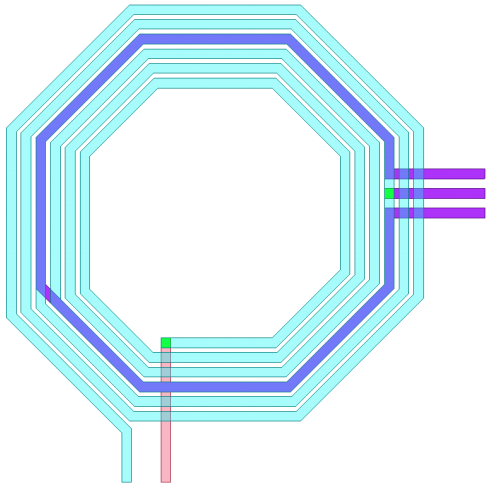


Figure 4.3: Transformer geometry.

μm, respectively. The two thick metal layers have been used to minimize the loss. Since the secondary has already much more parasitics than the primary, it uses the top metal to minimize the capacitance to the substrate. The number of turns, diameter, and metal widths are chosen to provide maximum voltage gain with acceptable loss at the desired frequency. If we increase the number of secondary turns, the voltage gain grows slowly because the new turns are farther from the primary, but the capacitance and loss increase significantly. Also, a higher number of turns reduces the transformer input resistance. According to HFSS simulations, the above transformer has an insertion loss of 2.4 dB at 5.5 GHz, an unloaded voltage gain of 13.4 dB, and an unloaded input resistance of 87 Ω. With a matched load connected to the secondary, the voltage gain and input

resistance drop to 12 dB and 44 Ω, respectively. We then need to understand how the transformer performs when it is connected to the following block, namely mixers.

4.3 Receiver Architecture

Figure 4.4 shows the overall receiver architecture. The transformer described in

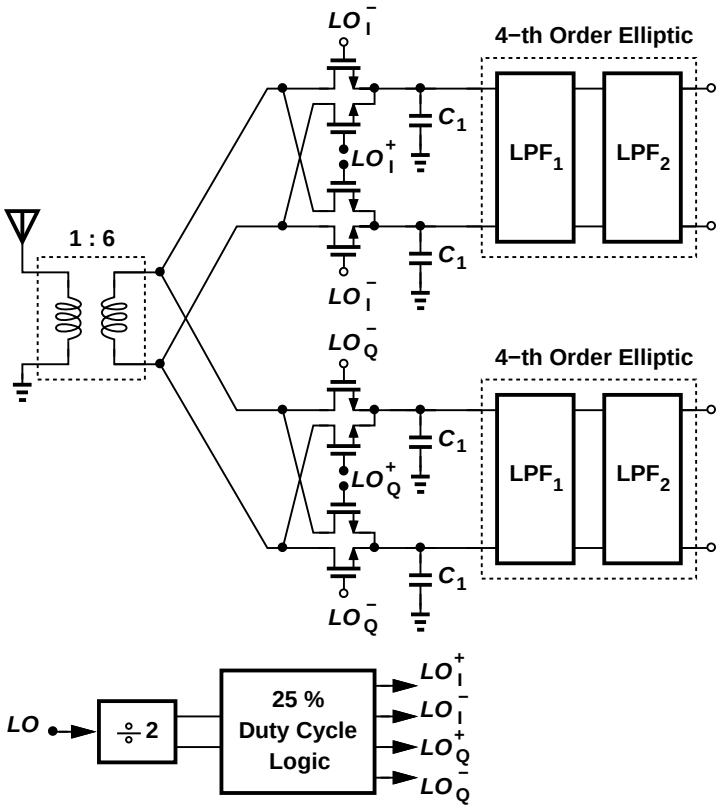


Figure 4.4: Receiver architecture.

the previous section serves as the LNA and single-ended to differential converter at the input and drives two sets of passive mixers with 25% duty cycle LOs. The downconverted baseband signals are then applied to 4-th order elliptic filters for channel selection. A side-benefit is that the transformer also provides ESD

protection. The LO frequency arrives at twice the carrier frequency and is divided by two to generate quadrature phases. We then have some logic to produce the 25% LO waveforms.

We should highlight two advantages of our approach over the LNA-less receiver in [27]. First, the input matching inherent in our receiver provides a robust interface with the antenna in the presence of long external traces. Second, our front end has much less power consumption.

There are three important questions that we need to address. First, how do the transformer and mixers provide input matching? Second, What is the conversion gain of the mixers? It seems that the current is integrated in the load capacitor, C_1. In that case, the trans-impedance conversion gain will not be flat across the channel bandwidth. Finally, how should we calculate the noise figure? To answer these three important questions, a new analysis technique is required. We will study the input impedance, conversion gain and noise figure and see why the trans-impedance conversion gain is flat across the channel.

By virtue of its high turns ratio, the transformer in Fig. 4.4 exhibits a relatively high output impedance, approximating a current source. The switches can therefore be viewed as current-driven mixers, thus contributing less noise than voltage-driven topologies [28]. Moreover, for the sake of analysis, since a capacitor is a good *keeper* of voltage, it is difficult to assume voltage excitations.

4.4 Analysis of Current-Driven Passive Mixers

The 25% duty cycle passive mixers have been used extensively since 2008 [29]. But, their input impedance, conversion gain, and noise figure have not been formulated accurately [30]-[31]. This section proposes an accurate analysis that

helps the designer to insightfully quantify the underlying principles. The method can be extended to other LO schemes as well. Figure 4.5 shows the current-

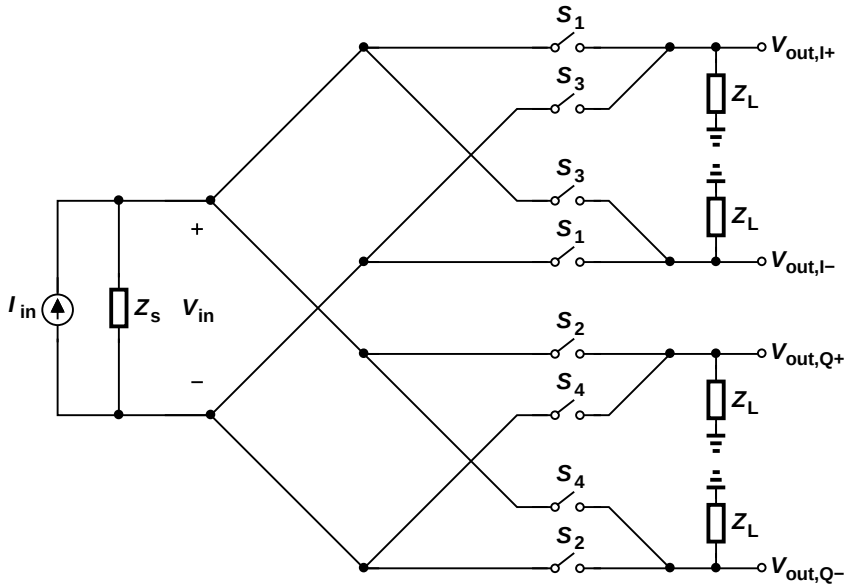


Figure 4.5: Current-driven passive mixer.

driven quadrature passive mixers with a source impedance Z_s. The circuit has been redrawn in Fig. 4.6 for convenience where the LO waveforms controlling the switches, S_1–S_4, are also shown. For simplicity, let us assume that the switch resistance, R_{sw}, is zero. We will add its effect later. The in-phase output voltage can be written as

$$V_{out,I}(t) = [I_{mix} \times (S_1 - S_3)] * 2Z_L. \tag{4.1}$$

The mixer input current, I_{mix}, is chopped by S_1 and S_3 and convolved with the differential load impedance, $2Z_L$. Similarly, the quadrature output voltage would be

$$V_{out,Q}(t) = [I_{mix} \times (S_2 - S_4)] * 2Z_L. \tag{4.2}$$

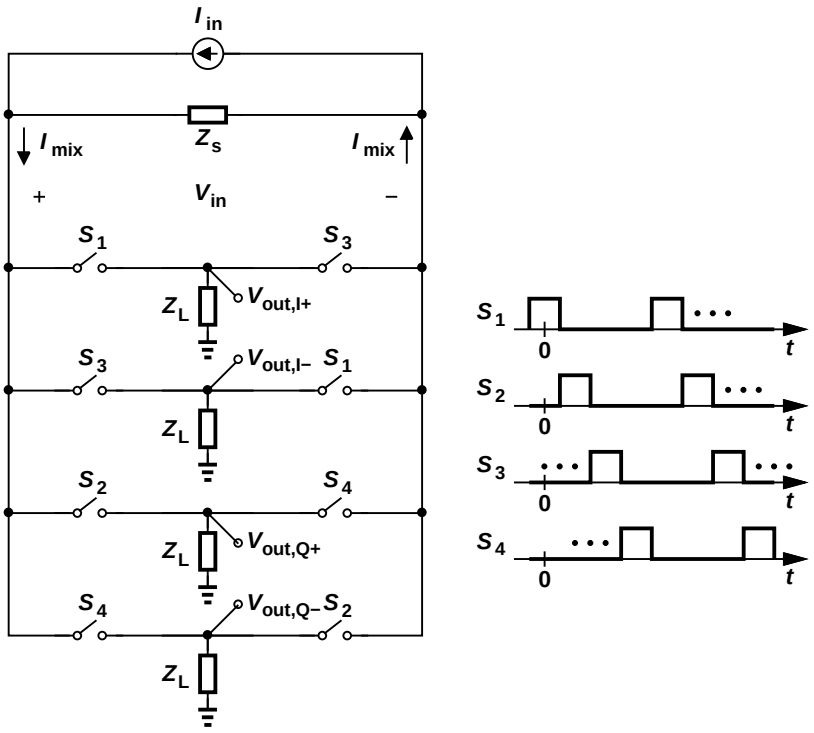


Figure 4.6: Current-driven passive mixer and LO waveforms.

The input voltage is equal to $V_{out,I}$ during S_1, -$V_{out,I}$ during S_3, $V_{out,Q}$ during S_2, and -$V_{out,Q}$ during S_4. Thus,

$$V_{in}(t) = V_{out,I}(t) \times (S_1 - S_3) + V_{out,Q}(t) \times (S_2 - S_4). \tag{4.3}$$

Substituting (4.1) and (4.2) in (4.3), yields

$$\begin{aligned} V_{in}(t) &= \{[I_{mix} \times (S_1 - S_3)] * 2Z_L\} \times (S_1 - S_3) \\ &+ \{[I_{mix} \times (S_2 - S_4)] * 2Z_L\} \times (S_2 - S_4). \end{aligned} \tag{4.4}$$

Taking the Fourier transform of (4.4) leads to

$$\begin{aligned} V_{in}(f) &= \{[I_{mix} * (S_1 - S_3)] \times 2Z_L\} * (S_1 - S_3) \\ &+ \{[I_{mix} * (S_2 - S_4)] \times 2Z_L\} * (S_2 - S_4), \end{aligned} \tag{4.5}$$

which is the key equation to derive the input impedance. Figure 4.7 plots $(S_1 - S_3)$ and $(S_2 - S_4)$ in both time and frequency domains. Let us do a warm-up exercise

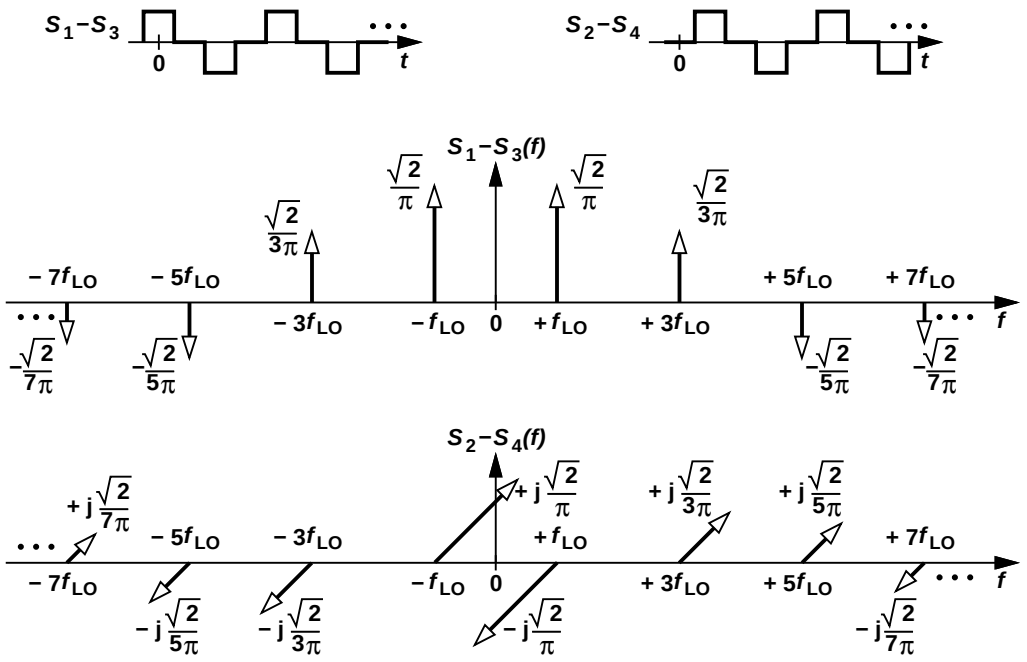


Figure 4.7: $(S_1 - S_3)$ and $(S_2 - S_4)$ in time and frequency domains.

and consider the case where the source impedance is infinite in Fig. 4.6.

4.4.1 Infinite Source Impedance

Infinite source impedance, Z_s, yields $I_{mix} = I_{in}$. This simplifies the calculations as I_{mix} would be single-tone.

4.4.1.1 Input Impedance Calculation

To calculate the input impedance, we apply a tone at $f_{LO} + f_{IF}$ as shown in Fig. 4.8 and would like to calculate the input voltage at the same frequency. Let us first focus on the positive-frequency impulse of I_{mix} and see how it will be shifted

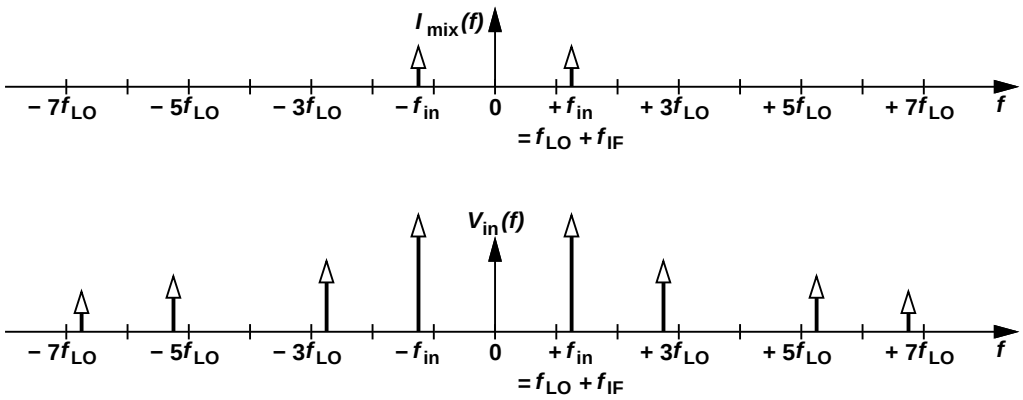


Figure 4.8: A single-tone current applied to the mixer and the resultant input voltage spectrum.

along the spectrum to finally reside at the same frequency. The only way is to shift up and down by the same amount. For example, from the spectrum of $(S_1 - S_3)$, I_{mix} will be shifted up by $\sqrt{2}\delta(f - f_{LO})/\pi$ and down by $\sqrt{2}\delta(f + f_{LO})/\pi$. Another way is to be shifted up by $\sqrt{2}\delta(f - f_{LO})/(3\pi)$ and down by $\sqrt{2}\delta(f + f_{LO})/(3\pi)$. Also, the mixing mechanism can happen with first shifting down and then up. The same power would come from mixing with $(S_2 - S_4)$. Note that because the spectrum of $(S_2 - S_4)$ is odd, one component would be multiplied by $+j$ and the other by $-j$, resulting a real positive value, the same as that of mixing with $(S_1 - S_3)$. An interesting practice is to see if there would be any component at the image frequency, $f_{LO} - f_{IF}$ in the V_{in} spectrum. The sum of the two shifting frequencies has to be $\pm 2f_{LO}$ in order to generate image. For example, the impulse at $f_{LO} + f_{IF}$ would be shifted down twice by $\sqrt{2}\delta(f + f_{LO})/\pi$ to reside at $-f_{LO} + f_{IF}$. However, shifting down twice by $+j\sqrt{2}\delta(f + f_{LO})/\pi$ generates the same amplitude with a negative sign. Similarly, shifting down by $3f_{LO}$ and up by f_{LO} will not generate any image because the I and Q branches cancel each other. It is instructive to see at what frequencies V_{in} has components in response to a single tone that resides at $f_{LO} + f_{IF}$ and $-f_{LO} - f_{IF}$. An interested reader can

prove that those frequencies are $(f_{LO} + f_{IF} + 4kf_{LO})$ and $(-f_{LO} - f_{IF} + 4kf_{LO})$, where k varies from $-\infty$ to $+\infty$ (Fig. 4.8).

Knowing the frequency shifts that happen in (4.5) that contribute to the input voltage at $f_{LO} + f_{IF}$, we can write the mixer input impedance, Z_{mix}, as

$$Z_{mix}(f) = \frac{8}{\pi^2}\left[Z_L(f \pm f_{LO}) + \frac{1}{3^2}Z_L(f \pm 3f_{LO}) + \frac{1}{5^2}Z_L(f \pm 5f_{LO}) + ...\right]. \quad (4.6)$$

If the load impedance is a capacitor, $1/(j2\pi C_L f)$, at the frequencies close to the LO frequency, $Z_L(f - f_{LO})$ dominates the summation in (4.6) and the input impedance would be approximately equal to

$$Z_{mix}|_{C_L}(f) \approx \frac{8}{\pi^2}Z_L(f - f_{LO}) = \frac{8}{\pi^2}\frac{1}{j2\pi C_L(f - f_{LO})}. \quad (4.7)$$

As another special case, if the load impedance is a resistor, R_L, the input impedance would be

$$Z_{mix}|_{R_L}(f) = \frac{16R_L}{\pi^2}\left(1 + \frac{1}{3^2} + \frac{1}{5^2} + ...\right) = 2R_L. \quad (4.8)$$

Since there is no memory in the system, the source would not recognize that the resistor is being switched and at any point of time the differential input impedance is $2R_L$.

4.4.1.2 Conversion Gain Calculation

We are mostly interested in the trans-impedance conversion gain defined as the transfer function from the input current at $f_{LO} + f_{IF}$ to the output voltage at f_{IF}. Since I_{mix} is single-tone, only the fundamental of $(S_1 - S_3)$ matters. Thus, from Eq. (4.1) the trans-impedance conversion gain, A_R, would be

$$A_R = \frac{2\sqrt{2}}{\pi}Z_L \approx 0.9Z_L. \quad (4.9)$$

Note that if Z_L is a capacitor, A_R is *not* constant across the channel bandwidth. Now, let us look at the voltage conversion gain, A_V, defined as the transfer

function from the input voltage at $f_{LO} + f_{IF}$ to the output voltage at f_{IF}. We have

$$A_V = \frac{V_{out,I}}{V_{in}} = \frac{V_{out,I}}{I_{in}} \times \frac{I_{in}}{V_{in}} = \frac{A_R}{Z_{mix}}. \tag{4.10}$$

Substituting (4.6) and (4.9) in (4.10), we get

$$A_V = \frac{\frac{2\sqrt{2}}{\pi} Z_L}{\frac{8}{\pi^2}\left[Z_L(f \pm f_{LO}) + \frac{1}{3^2} Z_L(f \pm 3f_{LO}) + \frac{1}{5^2} Z_L(f \pm 5f_{LO}) + ...\right]}. \tag{4.11}$$

We can simplify A_V for the special cases of load capacitor and load resistor as

$$A_V|_{C_L} \approx \frac{\pi\sqrt{2}}{4} \approx 0.9 \approx 0.9\ dB, \tag{4.12}$$

$$A_V|_{R_L} = \frac{\sqrt{2}}{\pi} \approx 0.45 \approx -6.9\ dB. \tag{4.13}$$

As expected, having a load capacitance is superior than a load resistance. Interestingly, $A_V|_{C_L}$ is greater than 1. It is not surprising, because V_{out} is the cause and V_{in} is the effect here. The power of V_{out} is only at f_{IF}. This power is then spread over the specific harmonics at V_{in}. The same result can be achieved using Eq. (4.3), where V_{out} at f_{IF} will be convolved with the fundamental of $(S_1 - S_3)$ and $(S_2 - S_4)$ to form V_{in} at $f_{LO} + f_{IF}$.

4.4.1.3 Switch Resistance Effect

Because only one switch out of the four switches that share one side is on at a time, we can move the switch resistance to the main path as shown in Fig. 4.9. Then, the switch resistance is in series with the input current source (Z_s is infinite), and the input impedance would be

$$Z_{mix}(f) = 2R_{sw} + \frac{8}{\pi^2}\left[Z_L(f \pm f_{LO}) + \frac{1}{3^2} Z_L(f \pm 3f_{LO}) + \frac{1}{5^2} Z_L(f \pm 5f_{LO}) + ...\right]. \tag{4.14}$$

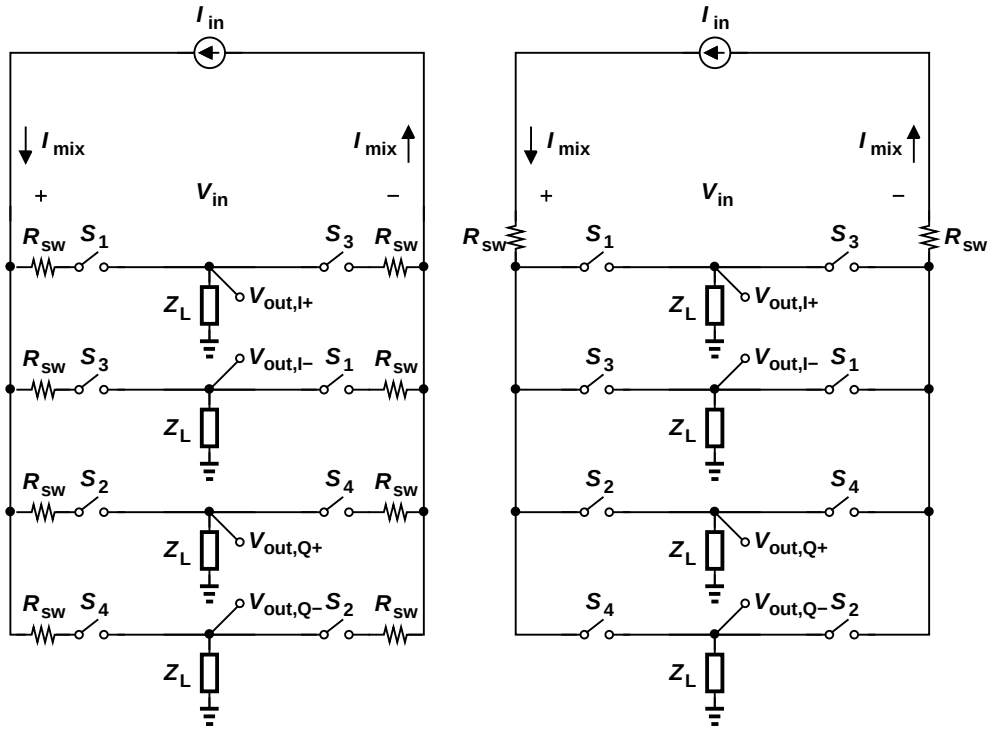


Figure 4.9: Moving the switch resistance to the main path.

The trans-impedance conversion gain does not change, but, the voltage conversion gain needs to be modified according to (4.14) as

$$A_V = \frac{\frac{2\sqrt{2}}{\pi} Z_L}{2R_{sw} + \frac{8}{\pi^2}\left[Z_L(f \pm f_{LO}) + \frac{1}{3^2} Z_L(f \pm 3f_{LO}) + \frac{1}{5^2} Z_L(f \pm 5f_{LO}) + ...\right]}. \tag{4.15}$$

Interested readers can simplify (4.14) and (4.15) for the special cases that we studied before.

4.4.2 Finite Source Impedance

With finite source impedance, Z_s, I_{mix} is no longer equal to I_{in}. Instead,

$$I_{mix} = I_{in} - \frac{V_{in}}{Z_s}. \tag{4.16}$$

Although this might seem a small change to the case with infinite Z_s, the equations become much more complicated. Recall from Section 4.4.1 that V_{in} had components around odd harmonics. It can be shown that in the presence of Z_s, V_{in} has the same frequency content but the amplitudes needs to be modified. Note that (4.16) yields that I_{mix} also has components around odd harmonics (Fig. 4.10).

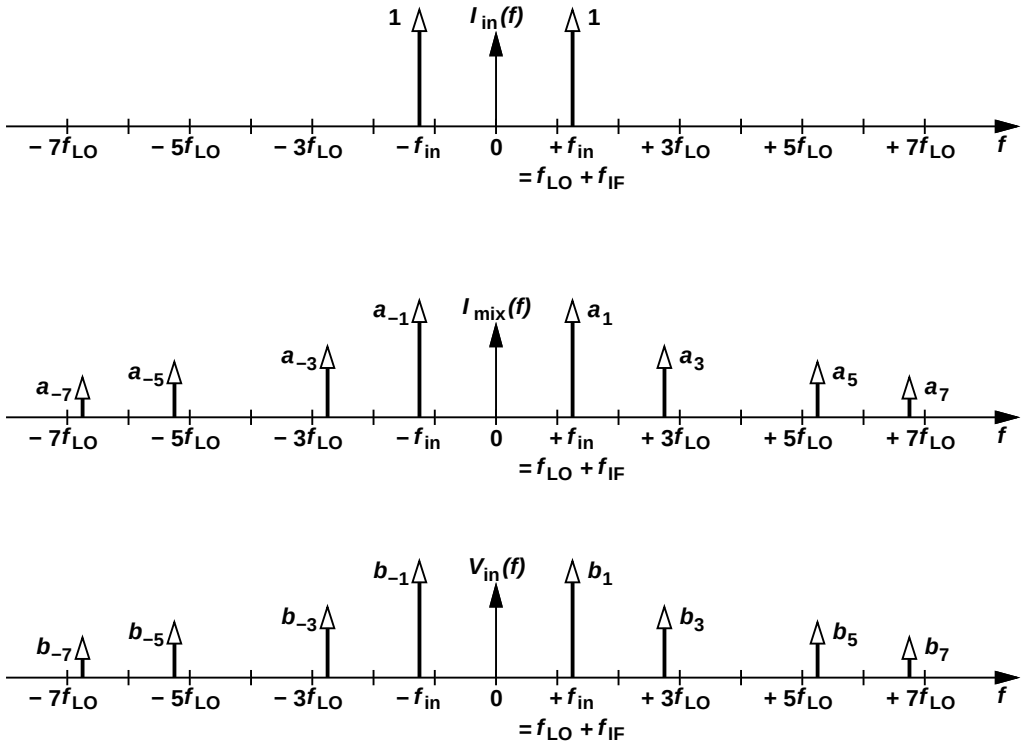


Figure 4.10: A single-tone current applied at the input and the resultant spectrum of the mixer input current and voltage.

4.4.2.1 Input Impedance Calculation

We can still use Eq. (4.5) to derive the input impedance. This time, the harmonics of I_{mix} convolve with the harmonics of $(S_1 - S_3)$ and $(S_2 - S_4)$, and fold

to the baseband frequency. There are also other components around harmonics which we ignore after multiplication by Z_L. Since the mixer is a downconverter, the load impedance, Z_L, would be small at high frequencies. In order to calculate the input impedance, as shown in Fig. 4.10, we assign a_i and b_i as the phasors of I_{mix} and V_{in} around ith harmonic and find their values using (4.5) and (4.16). Since the amplitude of the tone in I_{in} is unity, the input impedance is equal to b_1. Section 4.8 finds the values of a_i and b_i, yielding

$$Z_{in}(f) = \frac{\frac{8}{\pi^2} Z_L(f - f_{LO})}{1 + \frac{8}{\pi^2} Z_L(f - f_{LO}) \sum_{k=-\infty}^{\infty} \frac{1}{(4k+1)^2 Z_s(f + 4k f_{LO})}}. \tag{4.17}$$

If Z_L is a capacitor, we can usually neglect 1 in the denominator of (4.17) for reasonable values of Z_s. Thus,

$$\frac{1}{Z_{in}|_{C_L}(f)} \approx \sum_{k=-\infty}^{\infty} \frac{1}{(4k+1)^2 Z_s(f + 4k f_{LO})}. \tag{4.18}$$

The input impedance is the parallel combination of the scaled source impedance at certain frequencies and independent of the load impedance, Z_L. Moreover, if Z_s is a resistor, R_s, then

$$Z_{in}|_{C_L,R_s} = \frac{8}{\pi^2} R_s \approx 0.81 R_s \tag{4.19}$$

4.4.2.2 Conversion Gain Calculation

As mentioned earlier, we assume that Z_L has a lowpass shape and ignore the harmonics at the output nodes. The voltage conversion gain is the same as the case with infinite Z_s, while we do not include the switch resistance. Thus, for a capacitive load, we have

$$A_V|_{C_L} = \frac{\pi\sqrt{2}}{4} \approx 1.11 \approx 0.9\ dB. \tag{4.20}$$

The trans-impedance conversion gain would be $A_V \times Z_{in}$ and equal to

$$A_R|_{C_L} = \frac{\pi\sqrt{2}}{4} \div \sum_{k=-\infty}^{\infty} \frac{1}{(4k+1)^2 Z_s(f+4kf_{LO})}, \tag{4.21}$$

independent of C_L and f_{IF}.

4.4.2.3 Switch Resistance Effect

If we add the switch resistance, the input voltage is equal to the one in Eq. (4.5) plus $2R_{sw}I_{mix}$. Thus,

$$\begin{aligned} V_{in}(f) &= \{[I_{mix} * (S_1 - S_3)] \times 2Z_L\} * (S_1 - S_3) \\ &+ \{[I_{mix} * (S_2 - S_4)] \times 2Z_L\} * (S_2 - S_4) + 2R_{sw}I_{mix}. \end{aligned} \tag{4.22}$$

Equation (4.16) is still valid and along with (4.22) derives the input impedance. Note that we could assign $a_{sw,i}$ and $b_{sw,i}$ as the phasors of I_{mix} and V_{in} around ith harmonic and find their values similar to section 4.8. However, finding the solution is more difficult in this case. We wish to perform some transforms so that we can utilize the equations that we already have. This is done by the Norton-Thevenin-Norton conversion shown in Fig. 4.11. The circuit in Fig. 4.11(c) is

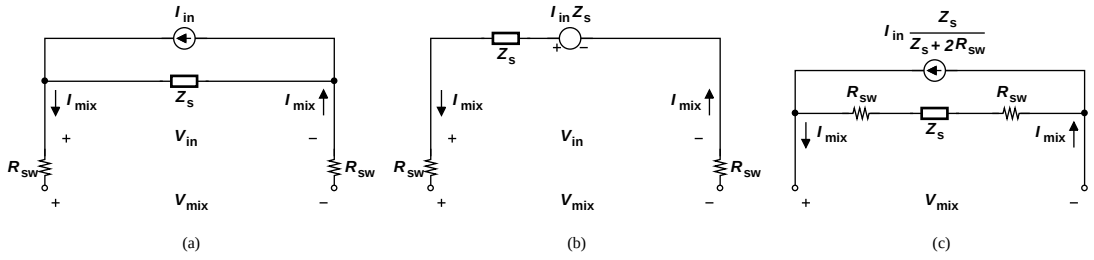


Figure 4.11: Norton-Thevenin-Norton Conversion.

similar to the case without switch resistance, and we can easily find V_{mix} as the

input current times the input impedance seen by the source, i. e.,

$$V_{mix}(f) = I_{in}\frac{Z_s}{Z_s+2R_{sw}} \times \frac{\frac{8}{\pi^2}Z_L(f-f_{LO})}{1+\frac{8}{\pi^2}Z_L(f-f_{LO})\sum_{k=-\infty}^{\infty}\frac{1}{(4k+1)^2[Z_s(f+4kf_{LO})+2R_{sw}]}}. \tag{4.23}$$

Then from the original circuit in Fig. 4.11(a), $V_{in} = V_{mix} + 2R_{sw}I_{mix}$. Replacing I_{mix} with $I_{in} - V_{in}/Z_s$, and using (4.23), we find the input impedance as

$$Z_{in}(f) = Z_s||2R_{sw} + (\frac{Z_s}{Z_s+2R_{sw}})^2 \times \frac{\frac{8}{\pi^2}Z_L(f-f_{LO})}{1+\frac{8}{\pi^2}Z_L(f-f_{LO})\sum_{k=-\infty}^{\infty}\frac{1}{(4k+1)^2[Z_s(f+4kf_{LO})+2R_{sw}]}}. \tag{4.24}$$

For a load capacitance and reasonable source impedance, we can usually ignore 1 in the denominator of (4.24) and write

$$Z_{in}|_{C_L}(f) = Z_s||2R_{sw} + (\frac{Z_s}{Z_s+2R_{sw}})^2 \div \sum_{k=-\infty}^{\infty}\frac{1}{(4k+1)^2[Z_s(f+4kf_{LO})+2R_{sw}]}. \tag{4.25}$$

Again, we see that the input impedance is independent of the load impedance under certain conditions. Now, we wish to find the voltage conversion gain, A_V. We can write

$$V_{in}(f) = \frac{2\sqrt{2}}{\pi}V_{out,I}(f-f_{LO}) + 2R_{sw}I_{mix}(f), \tag{4.26}$$

where only low-frequency component of $V_{out,I}$ has been taken into account. Using Eq. (4.16) and the fact that $I_{in} = V_{in}/Z_{in}$, we get

$$I_{mix} = \frac{Z_s - Z_{in}}{Z_s Z_{in}}V_{in} \tag{4.27}$$

Solving (4.26) and (4.27) yields

$$A_V|_{C_L} = \frac{\pi\sqrt{2}}{4}\left(1 - 2R_{sw}\frac{Z_s - Z_{in}}{Z_s Z_{in}}\right) \tag{4.28}$$

The trans-impedance conversion gain, A_R, is equal to $A_V \times Z_{in}$, and can be found using (4.25) and (4.28). Interestingly, A_R is independent of C_L and f_{IF}. The latter is very important because otherwise, we would not have flat response across the channel.

4.4.3 Noise Figure Calculation

With infinite Z_s, the switch resistance and hence its noise is in series with the input current source. Thus, it does not contribute noise. Now, let us calculate the noise figure with finite purely resistive Z_s equal to R_s. We include the switch resistance, but assume it noiseless first. We add the effect of switch resistance noise later. We also assume that the load impedance is a capacitor and ignore the higher harmonics at the output. If I_{in} is the rms value of the input signal, the signal-to-noise ratio (SNR) at the input would be

$$SNR_{in} = \frac{I_{in}^2}{4kT\frac{1}{R_s}}. \tag{4.29}$$

The signal and noise around f_{LO} will be downconverted at the output nodes with the same trans-impedance conversion gain, A_R. However, the noise around ith harmonics of f_{LO} will also fold on the signal with a conversion gain of A_R/i. Thus, the output SNR would be

$$SNR_{out} = \frac{I_{in}^2 A_R^2}{4kT\frac{1}{R_s}A_R^2\left(1+\frac{1}{9}+\frac{1}{25}+...\right)}, \tag{4.30}$$

where we have assumed the signal is double-sideband (DSB). By definition, the DSB noise figure is

$$NF = \frac{SNR_{in}}{SNR_{out}} = (1+\frac{1}{9}+\frac{1}{25}+...) = \frac{\pi^2}{8} \approx 0.9\ dB. \tag{4.31}$$

Now, let us add the switch resistance noise. For noise analysis purpose, we remove the input signal source and notice that the switch resistance is in series with R_s. Therefore, the noise figure will be degraded by $(1 + 2R_{sw}/R_s)$, i.e.,

$$NF = \frac{\pi^2}{8}(1 + \frac{2R_{sw}}{R_s}). \tag{4.32}$$

Now, let us consider a general source impedance. We still assume that at the vicinity of f_{LO}, $Z_s = R_s$ and the noise current source is $4kT/R_s$. We use the converted model in Fig. 4.11(c). The input signal power is $I_{in}^2 Z_s^2/(Z_s + 2R_{sw})^2$, and the input noise current would be

$$\overline{i_n^2} = \frac{4kTZ_s^2}{R_s(Z_s + 2R_{sw})^2} + \frac{4kT2R_{sw}}{(Z_s + 2R_{sw})^2}. \tag{4.33}$$

Then the output signal is simply

$$V_{out}^2 = \frac{Z_s(f_{LO})^2}{[Z_s(f_{LO}) + 2R_{sw}]^2} I_{in}^2 A_R^2, \tag{4.34}$$

but for the noise we have to consider the noise around harmonics as well. It folllows that

$$\begin{aligned}
\overline{V_{n,out}^2} &= \left\{ \frac{4kTZ_s(f_{LO})^2}{R_s[Z_s(f_{LO}) + 2R_{sw}]^2} + \frac{4kT2R_{sw}}{[Z_s(f_{LO}) + 2R_{sw}]^2} \right\} A_R^2 \\
&+ \left\{ \frac{4kTZ_s(3f_{LO})^2}{R_s[Z_s(3f_{LO}) + 2R_{sw}]^2} + \frac{4kT2R_{sw}}{[Z_s(3f_{LO}) + 2R_{sw}]^2} \right\} \frac{A_R^2}{9} \\
&+ \left\{ \frac{4kTZ_s(5f_{LO})^2}{R_s[Z_s(5f_{LO}) + 2R_{sw}]^2} + \frac{4kT2R_{sw}}{[Z_s(5f_{LO}) + 2R_{sw}]^2} \right\} \frac{A_R^2}{25} + \ldots .
\end{aligned} \tag{4.35}$$

Thus, we have

$$\frac{1}{SNR_{out}} = \frac{4kT\dfrac{1}{R_s}}{I_{in}^2} \frac{[Z_s(f_{LO}) + 2R_{sw}]^2}{Z_s(f_{LO})^2} \sum_{k=0}^{+\infty} \frac{1}{(2k+1)^2} \left[\frac{Z_s[(2k+1)f_{LO}]^2 + 2R_{sw}R_s}{\{Z_s[(2k+1)f_{LO}] + 2R_{sw}\}^2} \right]. \tag{4.36}$$

Using (4.29) and (4.36), we can write the noise figure as

$$NF = \frac{[Z_s(f_{LO}) + 2R_{sw}]^2}{Z_s(f_{LO})^2} \sum_{k=0}^{+\infty} \frac{1}{(2k+1)^2} \left[\frac{Z_s[(2k+1)f_{LO}]^2 + 2R_{sw}R_s}{\{Z_s[(2k+1)f_{LO}] + 2R_{sw}\}^2} \right]. \tag{4.37}$$

Note that (4.37) simplifies to (4.32) if $Z_s = R_s$. If Z_s is an RLC tank resonating at f_{LO} with a parallel resistor R_s, we can neglect the tank impedance at the harmonic frequencies with respect to R_{sw}. Thus, (4.37) simplifies to

$$NF|_{RLC} = 1 + \frac{2R_{sw}}{R_s} + (\frac{\pi^2}{8} - 1)\frac{(R_S + 2R_{sw})^2}{2R_{sw}R_s}. \tag{4.38}$$

Note that if we do not neglect the tank impedance at the harmonics, the noise figure would be better than the one in (4.38). An interesting point is that reducing R_{sw} does not necessarily reduce the noise figure. In fact, with an RLC tank as the source resistance, the optimum switch resistance is

$$R_{sw,opt} = \frac{\sqrt{\pi^2 - 8}}{2\pi} R_s \approx 0.218 R_s. \tag{4.39}$$

Plugging this optimum value of R_{sw} in (4.38) derives the minimum noise figure of the mixer as $2.54 \approx 4.05$ dB.

4.5 Transformer-Mixer Design

Now that we know how to analyze the 25% duty cycle mixers, we get back to the design of our receiver front end. The transformer is designed and optimized first to have maximum voltage gain and low power loss at the 5-GHz band. Then, looking through the secondary of the transformer, we build the Norton equivalent circuit of the antenna-transformer cascade over a wide bandwidth as shown in Fig. 4.12. Our transformer guarantees that if a load impedance of 800 Ω is attached to its secondary, then the input impedance seen from the primary is about 50 Ω. In other words, since Z_s is equal to 800 Ω at the carrier frequency, for proper matching the input impedance of the mixer needs to be 800 Ω too. However, we know that for current-driven mixers, the input impedance depends on the source impedance itself. To avoid confusion, we refer to the impedance seen by

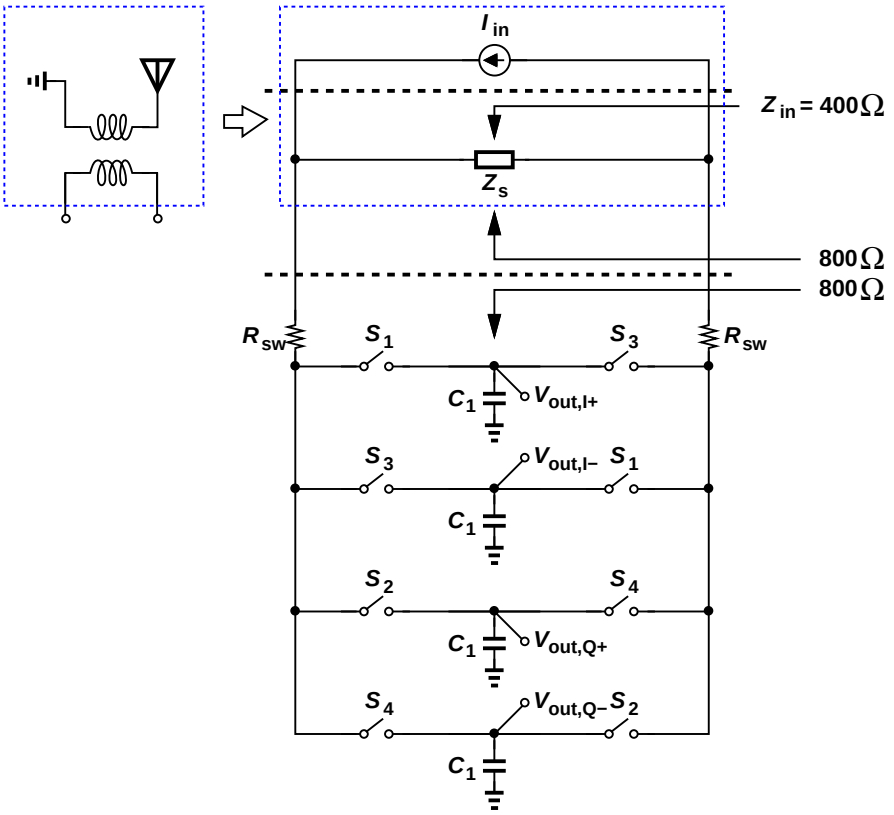


Figure 4.12: Transformer-mixer interface.

I_{in} denoted by Z_{in}. Since I_{in} is ideal, this resistance is unique and independent of I_{in}. Thus, the combination of antenna-transformer and the mixers must have a secondary-referred input impedance of 400 Ω. This composite input impedance is calculated in (4.25) and repeated here as

$$Z_{in}(f) = Z_s||2R_{sw} + (\frac{Z_s}{Z_s + 2R_{sw}})^2 \div \sum_{k=-\infty}^{\infty} \frac{1}{(4k+1)^2[Z_s(f + 4kf_{LO}) + 2R_{sw}]}. \tag{4.40}$$

Due to the bandpass nature of Z_s, the summation on the right-hand side must be carried out for about 14 terms. Ideally, in the range of 5 to 6 GHz, we must have $Re\{Z_{in}(f)\} \approx Z_s(f)/2 \approx 400\ \Omega$ and $Im\{Z_{in}(f)\} \approx 0$. Thus, Eq. (4.40) yields $R_{sw} = 57\ \Omega$ corresponding to W/L =10 μm/ 60 nm for the switches. The

LO buffers driving eight such switches draw a total power of $fCV_{DD}^2 \approx 0.4$ mW at 6 GHz. If $R_{sw} \ll Z_{in}(f)$, Eq. (4.40) can further be simplified to

$$\frac{1}{Z_{in}(f)} = \sum_{k=-\infty}^{\infty} \frac{1}{(4k+1)^2[Z_s(f+4kf_{LO}) + R_{sw}]}. \tag{4.41}$$

Equation 4.41 reveals that the source impedance, Z_s, around integer multiples of $4f_{LO}$ in series with the switch resistance is scaled and put in parallel to form the composite input impedance, Z_{in}. In other words, since the IF port of the mixer has high impedance, the impedance matching is achieved by folding of the source impedance itself.

Simulations indicate that the "zero-power" RF front end consisting of the transformer and the mixers exhibits a noise figure of 4.5 dB, a voltage gain of 12 dB, an input P_{1dB} of -5.2 dBm, and an S_{11} of better than -12 dB across the 5 GHz band. For a target receiver NF of less than 6 dB, all of the subsequent stages must contribute no more than 1.5 dB, demanding additional circuit techniques to build low-noise yet linear baseband filters with low power dissipation.

4.6 Filter Design

In the 11a standard, for the lowest data rate of 6 Mb/s, the adjacent and alternate adjacent channels can be higher than the desired channel by 16 dB and 32 dB, respectively. For the highest data rate of 54 Mb/s, the maximum interferer power levels are reduced by 17 dB, relaxing the filtering requirements. However, we design the baseband filters for the worst case which requires a sharp roll-off to reduce these channels to well below the desired signal level − unless the baseband ADCs offer a dynamic range wide enough and a sampling rate high enough to handle partially-attenuated blockers. Because in OFDM, each subcarrier has a narrow bandwidth, the phase response can be assumed linear across each sub-

channel. Thus, the phase response of the filter is not critical suggesting that an elliptic filter implementation is acceptable. A fifth-order elliptic filter is sufficient for our purpose and can be realized by cascading two biquadratic transfer functions and a single RC pole. Let us focus on designing a biquad section.

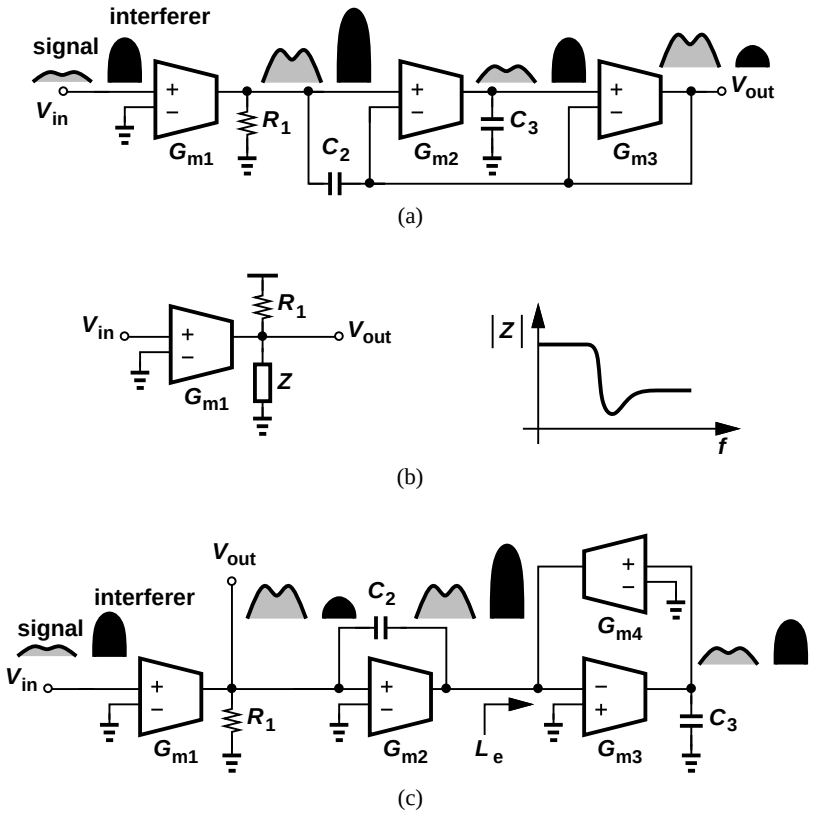


Figure 4.13: (a) Conventional implementation of a biquad, (b) basic idea of noninvasive filtering, and (c) noninvasive implementation of a biquad.

Figure 4.13(a) shows a conventional implementation of such a transfer function using three G_m stages. In order to study the noise behavior, we assume that each G_m has an input-referred noise voltage and calculate its transfer function to the output. The transfer function for the noise of G_{m1} and G_{m2} is proportional to $(s^2+\omega_z^2)/(s^2+as+b)$ and $1/(s^2+as+b)$, respectively, which are both low-pass.

Therefore, their noise is not attenuated in the signal band. The noise of G_{m3}, however, is attenuated through the bandpass shaping function, $s/(s^2 + as + b)$. The circuit also experiences nonlinearity because the signal and interferer are both amplified by $G_{m1}R_1$. As a result, G_{m1} compresses at its output and G_{m2} compresses at its input. Another issue is that this architecture needs 4-input G_m cells for fully-differential implementation. All of these issues are mitigated in the noninvasive filtering architecture. The basic idea is illustrated in Fig. 4.13(b), where a notch impedance similar to an LC trap is placed at the output of a G_m stage [24]. The notch impedance, Z, is high in the signal band and low at the interferer frequency. The filter transfer function follows the shape of Z and shunts the interferer to ground. The actual implementation is shown in Fig. 4.13(c) where G_{m3} and G_{m4} form a gyrator that transforms C_3 to an emulated inductor, L_e. L_e resonates with C_2 and generates a low-impedance path to ground at the interferer frequency. Let us study the noise behavior. The transfer function for the noise of G_{m1} is proportional to $(s^2 + \omega_z^2)/(s^2 + as + b)$ and does not attenuate it in the signal band. But, the noise of G_{m2} and G_{m4} is highpass-filtered by $s^2/(s^2 + as + b)$ and can be made negligible. The noise of G_{m3} is also attenuated by the bandpass shaping function of $s/(s^2 + as + b)$. In summary, compared to the previous case which had two unattenuated noise sources, this case has only one, and we expect to see lower noise. This topology is also more linear since the signal is amplified by $G_{m1}R_1$, but the interferer is attenuated. As a result, G_{m1} does not compress at its output. Note that the interferer is amplified at the output of G_{m2}. This can cause G_{m2} and G_{m4} to compress at their outputs and G_{m3} at its input. The important point here is that the compression of G_{m2}, G_{m3} and G_{m4} only shifts the notch frequency but it does not affect the transfer function in the signal band.[1] Because all the G_m cells have one grounded input,

[1]There is a second-order effect that slightly changes the gain in the signal band and is verified

this architecture readily lends itself to differential implementation.

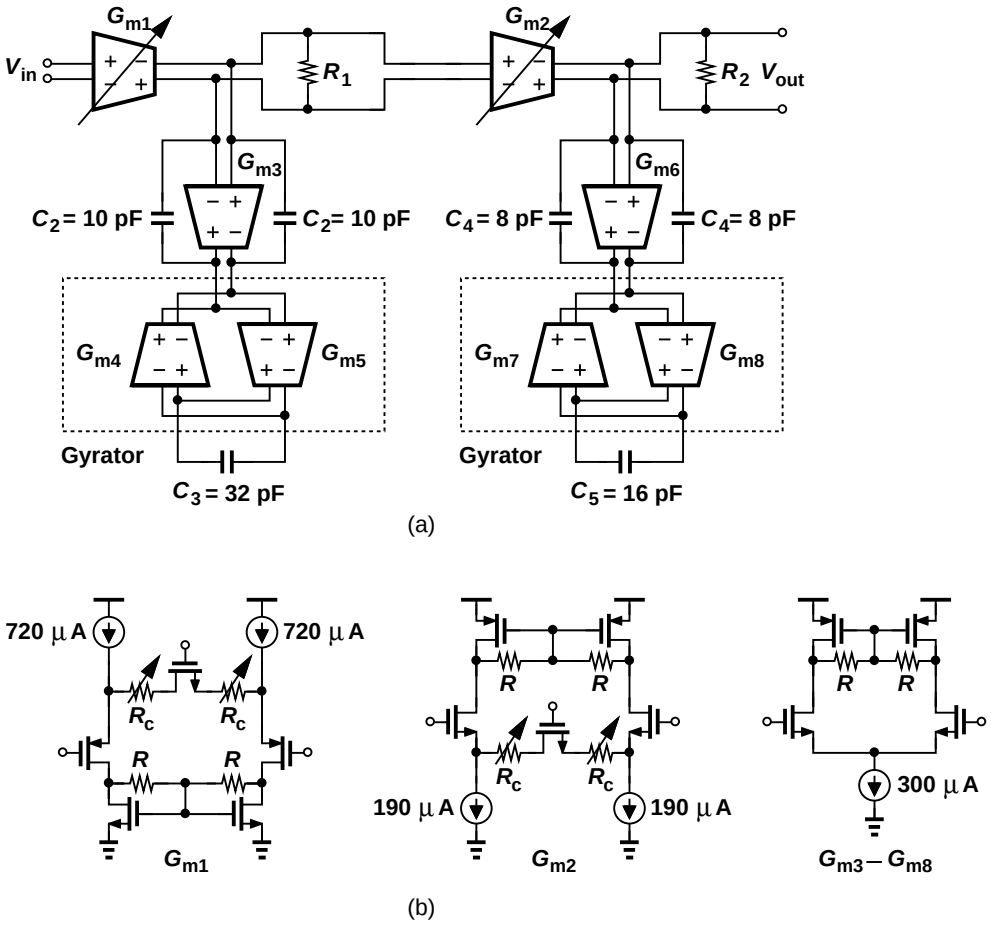


Figure 4.14: (a) Fourth-order elliptic low-pass filter, and (b) G_m implementations.

Figure 4.14(a) shows the realization of the fourth-order elliptic filter. A first-order RC filter is then added on the PCB to reach the fifth order. In this design, G_{m1} and G_{m2} are made variable to provide gain control to accommodate the wide range of input powers specified by 11a. Figure 4.14(b) summarizes the G_m implementations. G_{m1} has a PMOS input for low flicker noise and to work properly with an input common-mode level of 400 mV. Gain control is achieved by changing the source degeneration resistance of the input pair. Each branch

by the measurement results in Section 4.7.

dissipates 720 uA from a 1-V supply. G_{m2} has an NMOS input and consumes less power as its noise is not as important as that of G_{m1}. G_{m3} to G_{m8} are identical simple differential pairs. The fourth-order filter exhibits an input-referred noise voltage of 2 n$V/\sqrt{Hz}$ at 5 MHz, an in-channel IIP_3 of 193 mV_{rms} and a voltage gain of 39 dB while consuming 4.3 mW. The filter voltage gain is programmable in steps of 2 to 3 dB for a total range of 43 dB.

4.7 Experimental Results

The receiver of Fig. 4.4 has been fabricated in 65-nm digital CMOS technology. Figure 4.15 shows the die photograph. The RF section occupies 350 μm $\times$ 240

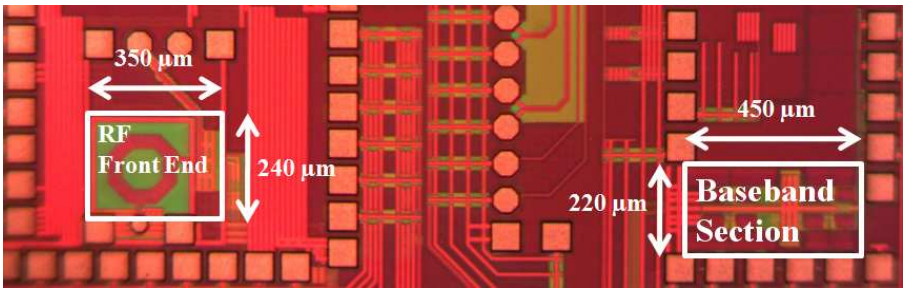


Figure 4.15: Die photograph.

μm and the baseband section 450 μm $\times$ 220 μm.[2] The die is bonded to a printed-circuit board and uses a 1-V supply for the main circuits, a 1.2-V source for the open-drain output drivers, and a 400-mV supply connected to the center tap of the transformer.

Figure 4.16 plots the measured noise figure of the complete receiver as a function of the baseband frequency. The average noise figure is about 5.3 dB. The sensitivity of the receiver is measured with the aid of Agilent's N5182 MXG

[2]Due to limited silicon area, the receiver layout is decomposed and placed within other unrelated circuits, but all of the connections are present on the chip.

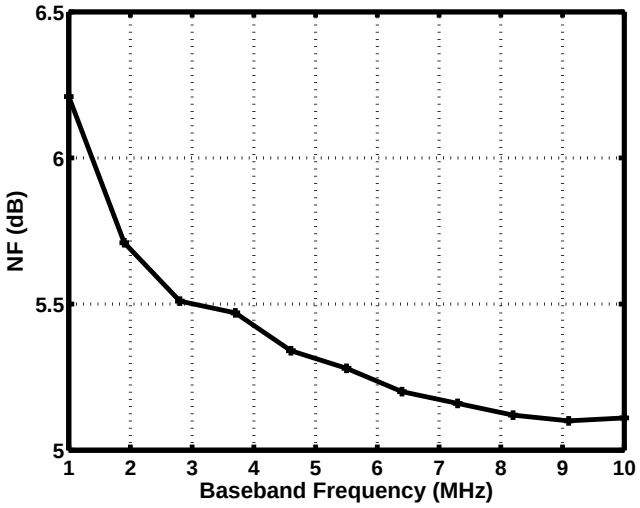


Figure 4.16: Measured noise figure.

vector signal generator and N9020A MXA signal analyzer, which respectively apply a 64-QAM 802.11a signal and sense the baseband outputs to construct the signal constellation. Figure 4.17 shows the results for a −65-dBm 5.7-GHz input at 54 MB/s. The error vector magnitude (EVM) is equal to −28 dB, exceeding the 11a specification by 5 dB, suggesting that the receiver sensitivity would be 5 dB better. As expected, the sensitivity was measured to be −70 dBm with an EVM of −23.4 dB.

Figure 4.18 plots the S_{11} from 5 to 6 GHz, measured at each input frequency, while the mixers switch at the corresponding LO frequency. It is expected that a slightly larger transformer or adding more capacitance can yield $S_{11} < -10$ dB across the band. Figure 4.19 shows the sensitivity of the receiver from 5 to 6 GHz. The sensitivity degrades a little at lower frequencies again because the transformer is mistuned. The receiver gain across the band in Fig. 4.20 also confirms the transformer mistuning.

Figure 4.21 plots the measured receiver transfer function, revealing a passband

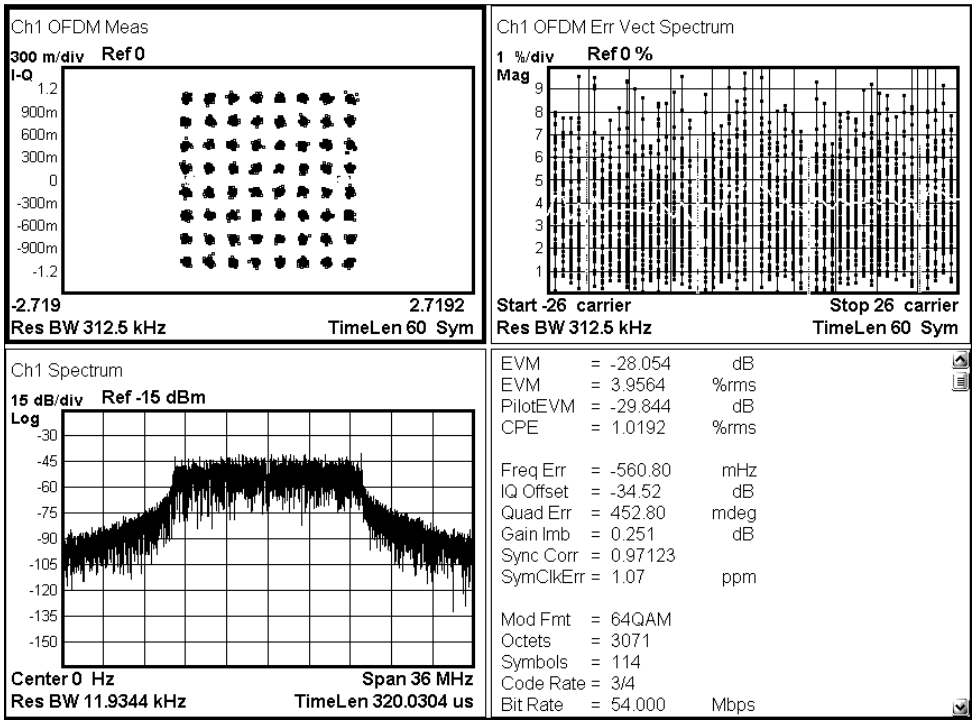


Figure 4.17: Measured EVM at $P_{in} = -65$ dBm.

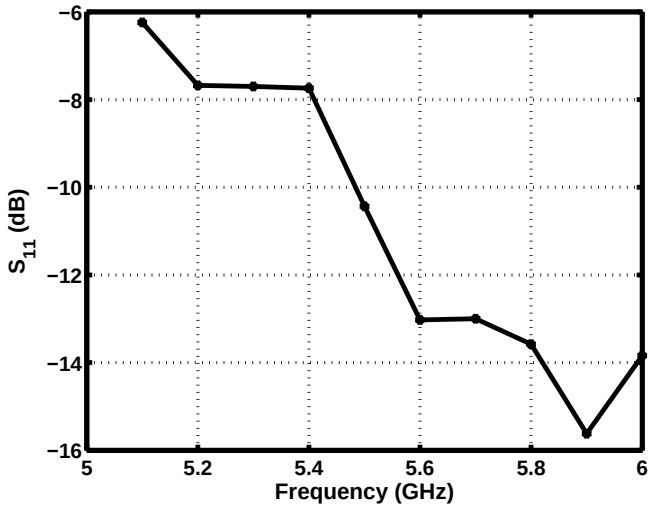


Figure 4.18: Measured input return loss.

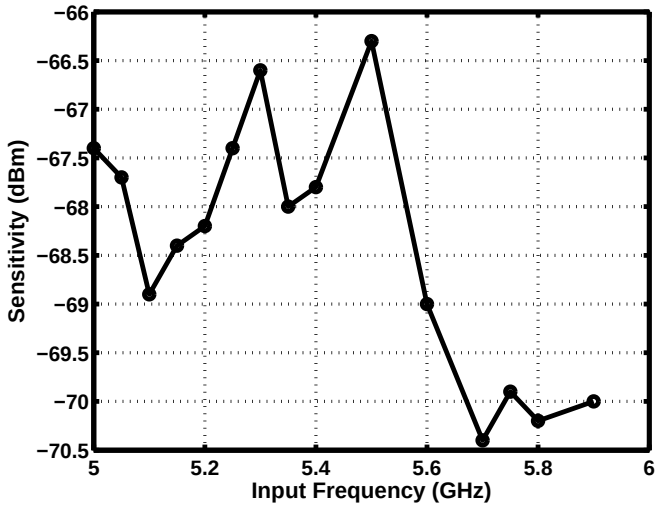


Figure 4.19: Measured sensitivity.

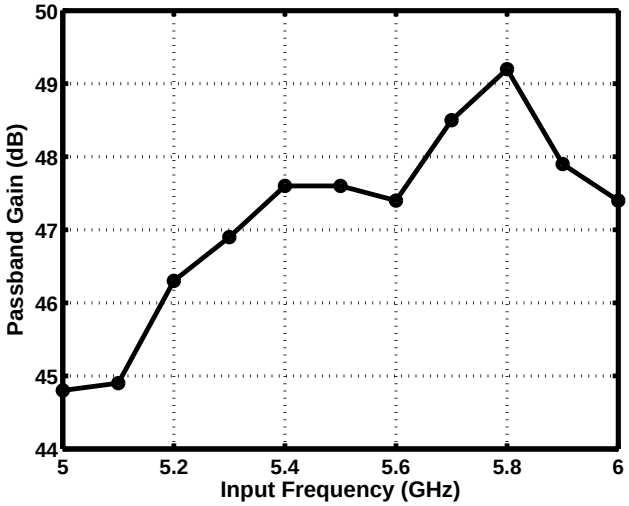


Figure 4.20: Measured passband gain.

peaking of 1 dB and a rejection of 22 dB at 20 MHz and 43 dB at 40 MHz.[3] Owing to the finite output resistance of the G_m cells, the filter does not exhibit the deep notches that are characteristic of elliptic transfer functions. The performance of

[3]In this measurement a first-order RC section follows each output on the PCB.

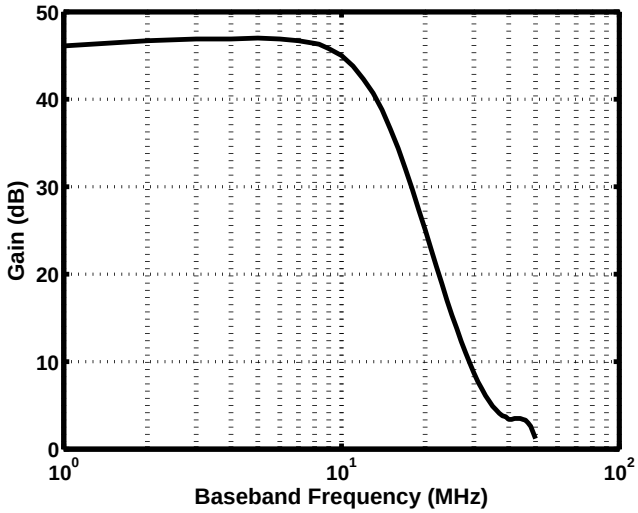


Figure 4.21: Measured receiver transfer function.

the baseband filter is ultimately tested when a large blocker accompanies a small desired signal. In such a case, the filter must remain sufficiently selective and linear so that the desired signal does not experience compression. Figure 4.22 plots the measured passband gain as a function of the power of an RF blocker in the adjacent or alternate adjacent channel. Note that this measurement is done with the maximum receiver gain which corresponds to the signal levels around the sensitivity, e.g. -60 dBm. The maximum adjacent channel interferer would be 1 dB lower or -61 dBm for which the variation of gain is negligible. Even with the maximum 11a power of -30 dBm, the gain variation is only about 1 dB. The peaking of gain with large adjacent-channel interferer is also observed in simulations and is due to the compression in the notch-impedance G_m cells. For the alternate-adjacent-channel interferer the gain variation is much less and totally negligible even upto -30 dBm.

The filter nonlinearity resulting from a blocker may also corrupt the 11a 64-QAM OFDM signal by creating cross modulation among the sub-channels. This

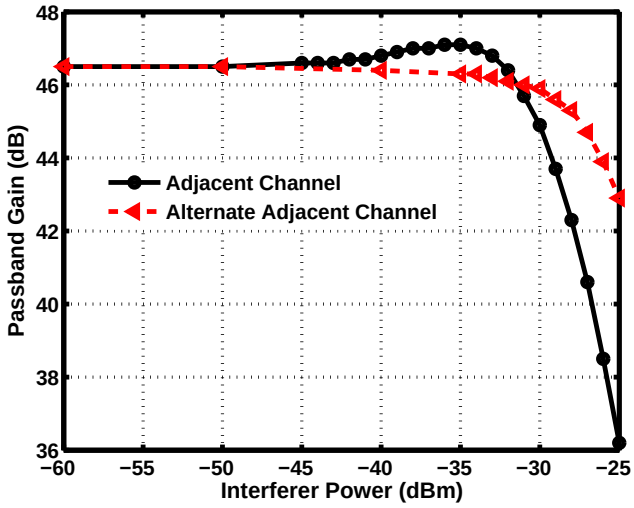


Figure 4.22: Measured passband gain in the presence of a blocker.

effect is characterized by setting the RF input signal level 3 dB above the sensitivity, applying a blocker, and raising its level until the EVM falls to −23 dB. Figure 4.23 plots the relative blocker level as a function of the frequency offset with respect to the desired signal center frequency.

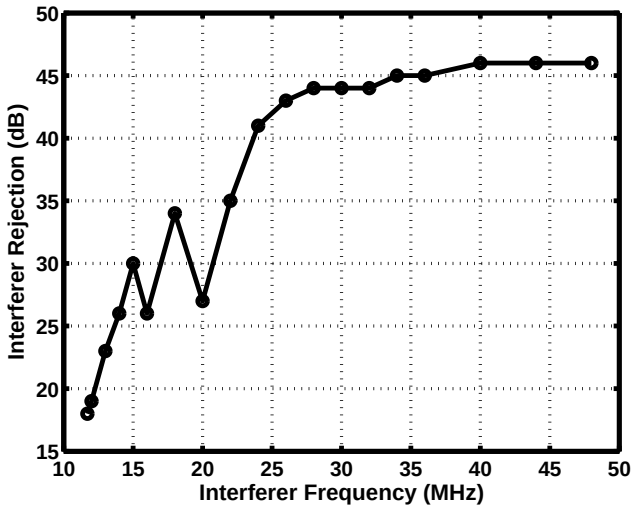


Figure 4.23: Measured interferer rejection.

Figure 4.24 shows the measured EVM and the corresponding passband gain versus input power. As the input signal power increases, a lower gain is chosen for the variable-gain G_m cells. For small input powers EVM is noise-limited and improves with the input power, while at large input powers EVM is nonlinearity-limited and will eventually go up. The variable gain range is such that even with maximum 11a signal of -30 dBm, the EVM is not degraded due to nonlinearity.

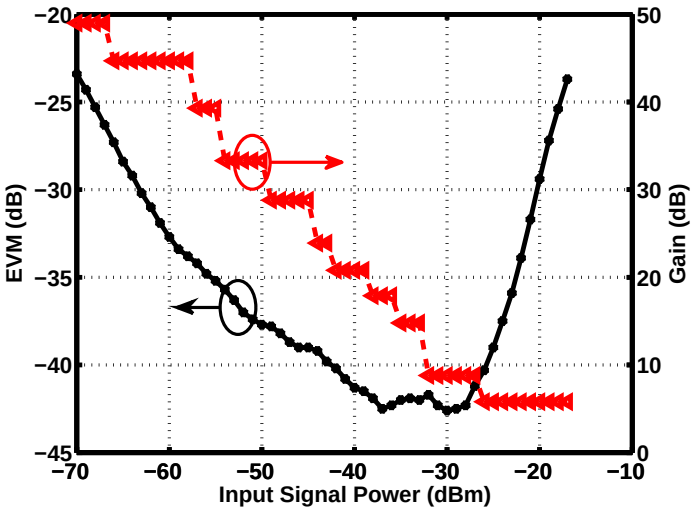


Figure 4.24: Measured EVM and passband gain versus input power.

Table 4.1 summarizes the receiver performance and compares it to that of prior art. This work has reduced the power consumption by about a factor of 4, while demonstrating a sensitivity of -70 dBm.

Table 4.1: Comparison with state-of-the-art.

	This Work	[23]	[32]	[33]
Frequency (GHz)	5.1 – 5.9	5.15 – 5.35	4.9 – 5.95	5.1 – 5.9
NF (dB)	5.3	8.0	4.4	5.5
IIP_3 (dBm)	+ 2.6	−11.2	+ 5	+ 16
Gain (dB)	5 – 48	14 – 94.5	8 – 74	19 – 89
Sensitivity (dBm) at 54 Mb/s	−70	NA	NA	−75.5
Power (mW)	11.6	46	108*	72.7**
LNA	0	11.7		
Mixers	0	9.8		
LO Buffers	0.4	10.8		
Filters, VGAs	10	13.7		
Divider/ 25% Logic	1.2			
CMOS Process	65 nm	0.18 μm	0.18 μm	0.13 μm
Area (mm^2)	0.183	NA	NA	NA

*** Including ADC.**

**** Without LO Buffer.**

4.8 Derivation of Input Impedance with Finite Source Impedance

Using Eq. (4.5), we can find b_1 as

$$b_1 = 2\left(\frac{\sqrt{2}}{\pi}\right)^2 \times 2Z_L(f - f_{LO})\left[a_1 + \frac{a_{-3}}{3} + \frac{a_5}{-5} + \frac{a_{-7}}{-7} + \frac{a_9}{9} + ...\right]. \quad (4.42)$$

Similarly, we can find b_{-3} and b_5 as

$$b_{-3} = 2\left(\frac{\sqrt{2}}{\pi}\right)^2 \times \frac{1}{3} \times 2Z_L(f - f_{LO})\left[a_1 + \frac{a_{-3}}{3} + \frac{a_5}{-5} + \frac{a_{-7}}{-7} + \frac{a_9}{9} + ...\right], \quad (4.43)$$

$$b_5 = 2\left(\frac{\sqrt{2}}{\pi}\right)^2 \times \frac{1}{-5} \times 2Z_L(f - f_{LO})\left[a_1 + \frac{a_{-3}}{3} + \frac{a_5}{-5} + \frac{a_{-7}}{-7} + \frac{a_9}{9} + ...\right]. \quad (4.44)$$

Note that $b_{-3} = b_1/3$, $b_5 = b_1/(-5)$, $b_{-7} = b_1/(-7)$, etc. Another sets of equation comes from (4.16) as

$$a_1 = 1 - \frac{b_1}{Z_s(f)}, \tag{4.45}$$

$$a_{-3} = -\frac{b_{-3}}{Z_s(f - 4f_{LO})}, \tag{4.46}$$

$$a_5 = -\frac{b_5}{Z_s(f + 4f_{LO})}. \tag{4.47}$$

If we substitute b_1, b_{-3}, and b_5, we get

$$a_1 = 1 - \frac{1}{Z_s(f)}\frac{8}{\pi^2}Z_L(f - f_{LO})\left[a_1 + \frac{a_{-3}}{3} + \frac{a_5}{-5} + \frac{a_{-7}}{-7} + \frac{a_9}{9} + ...\right], \tag{4.48}$$

$$a_{-3} = -\frac{1}{3Z_s(f - 4f_{LO})}\frac{8}{\pi^2}Z_L(f - f_{LO})\left[a_1 + \frac{a_{-3}}{3} + \frac{a_5}{-5} + \frac{a_{-7}}{-7} + \frac{a_9}{9} + ...\right], \tag{4.49}$$

$$a_5 = -\frac{1}{-5Z_s(f + 4f_{LO})}\frac{8}{\pi^2}Z_L(f - f_{LO})\left[a_1 + \frac{a_{-3}}{3} + \frac{a_5}{-5} + \frac{a_{-7}}{-7} + \frac{a_9}{9} + ...\right]. \tag{4.50}$$

Then, we can write a_{-3} and a_5 as

$$a_{-3} = (a_1 - 1)\frac{Z_s(f)}{3Z_s(f - 4f_{LO})}, \tag{4.51}$$

$$a_5 = (a_1 - 1)\frac{Z_s(f)}{-5Z_s(f - 4f_{LO})}. \tag{4.52}$$

Substituting the recent values for a_{-3} and a_5 in (4.48), we get

$$\begin{aligned} a_1 \;\; &= \;\; 1 - \frac{1}{Z_s(f)}\frac{8}{\pi^2}Z_L(f - f_{LO}) \times \\ &\left[1 + (a_1 - 1)\frac{Z_s(f)}{Z_s(f)} + (a_1 - 1)\frac{Z_s(f)}{9Z_s(f - 4f_{LO})} + (a_1 - 1)\frac{Z_s(f)}{25Z_s(f + 4f_{LO})} + ...\right]. \end{aligned} \tag{4.53}$$

It follows that

$$(a_1 - 1)\left[1 + \frac{8}{\pi^2}Z_L(f - f_{LO})\sum_{k=-\infty}^{\infty}\frac{1}{(4k+1)^2 Z_s(f + 4kf_{LO})}\right] = -\frac{8}{\pi^2}\frac{Z_L(f - f_{LO})}{Z_s(f)}. \tag{4.54}$$

Note that the input impedance is equal to b_1 and from (4.45) we get $Z_{in} = -(a_1 - 1)Z_s(f)$. Therefore, from (4.54) we write the input impedance as

$$Z_{in}(f) = \frac{\frac{8}{\pi^2} Z_L(f - f_{LO})}{1 + \frac{8}{\pi^2} Z_L(f - f_{LO}) \sum_{k=-\infty}^{\infty} \frac{1}{(4k+1)^2 Z_s(f + 4k f_{LO})}}. \tag{4.55}$$

4.9 Conclusion

This chapter suggests the use of transformers in place of active LNAs to save power and provide ESD protection. The "zero-power" front end consisting of a transformer followed by passive mixers has reasonable performance and combined with noninvasive filtering, exceeds the 11a requirements while consuming only 11.6 mW. The proposed analysis of current-driven passive mixers provides insight into their properties.

CHAPTER 5

Future Work

This dissertation introduced three novel analyses that helps the designer understand the circuits better and optimize their performance. In addition to optimization, it helps us make changes and propose new circuits. For example, the PFD phase noise analysis suggests to use various digital gates in the PFD circuit rather than all-NAND or all-NOR topologies. Another possible research path is to find the relation between the phase noise of LC oscillator and that of a single common-source amplifier with an RLC tank as the load. That might give us more insight and guidelines on the LC oscillator design. Finally, the analysis of current-driven mixers allows us to optimize the mixers for minimum noise figure or may suggest circuit modifications to create new topologies that exhibit lower noise or higher conversion gain or better harmonic rejection.

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