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Development of Integration of Sensors and Circuits for Wearable Electronics

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in

Electrical Engineering (Applied Physics)

by

Namseok Park

Committee in charge:

     Professor Shadi Dayeh, Chair
     Professor Prabhakar Bandaru
     Professor Renkun Chen
     Professor Zhaowei Liu
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2015

The dissertation of Namseok Park is approved, and it is acceptable in

quality and form for publication on microfilm:

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                                                          Chair

University of California, San Diego

2015

DEDICATION

I dedicate this thesis to

my wife, Jihyun and my family

EPIGRAPH

"You will know the truth, and the truth will set you free."

John 8:32

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ACKNOWLEDGEMENTS

I intended this thesis to integrate and extend the knowledge of the truly interdisciplinary character of semiconductor electronics. If I have achieved, it is largely due in part to my academic advisors, Professor Shadi Dayeh and retired Professor Deli Wang. I appreciate their inspirational guidance, timely advice, and constant encouragement throughout my time as their student. Thank both of you for being an inspiration and reminding me of what research and life should be all about. My special thanks go also to the members of my advisory committee, Professors Jie Xiang, Prabhakar Bandaru, Renkun Chen, and Zhaowei Liu for their invaluable insights and discussions.

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ABSTRACT OF THE DISSERTATION

Development of Integration of Sensors and Circuits for Wearable Electronics

by

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Doctor of Philosophy in Electrical Engineering (Applied Physics)

University of California, San Diego, 2015

Professor Shadi Dayeh, Chair

The trend toward increasing device density and decreasing price in the semiconductor electronics predicted by Moore's law has remained consistent for the past four decades. Recently, entirely new classes of applications have emerged and innovations beyond Moore's law scaling have shifted gradually toward the seamless integration of digital computing within our daily lives, commonly termed as More than Moore. To this end, emerging digital technologies in the next generation of digital electronics take the form of flexible, wearable, and printable electronics as well as

smaller and versatile sensing electronics. Electronic devices integrated into a novel system or unconventional form factors attract a lot of attention due to their unique degrees of freedom in flexibility as well as rich features and integrated novel functionalities. They rapidly find a broad range of applications in consumer health and electronic products for display, sensing, lighting, and energy conversion.

This work aims, on the one hand, toward functional materials synthesis and fabrication of devices that are believed to find sensing applications in wearable or flexible electronics. Low cost, energy-efficient solution-based chemical synthesis technique is studied for metal-oxide semiconductor thin films. A transparent, highly sensitive nickel oxide (NiO)/zinc oxide (ZnO) heterojunction ultra-violet (UV) photodetector is demonstrated. In addition, thin films of NiO and ZnO are studied as alternative materials to genuinely rare and valuable metal catalysts for a large-scale and economically viable water splitting system. On the other hand, this study places an emphasis on the monolithic system integration of solar-powered MOSFET circuits for wearable electronics. In order to create wearable electronics featuring flexibility or bendability as well as high performance, they need to be fabricated on a crystalline silicon substrate which is thin enough to flex. To this end, wafer thinning techniques and post-process device layer transfer methods are developed on a silicon-on-insulator (SOI) wafer. The unique approach involves the post-processing wafer removal from wafer backsides followed by a device embedding process in a polymer substrate.

CHAPTER 1: Introduction

1.1 Semiconductor Technology Trends

Ever since the invention of transistors and integrated circuits, digital electronics has made stunning progress. The fundamentally revolutionary character of this technology is well understood by looking at the physical parameters and functionality. The number of transistors on a chip increased exponentially, namely to hundreds of millions or billions of transistors in current sophisticated processors, and also the size of transistor became miniaturized by a factor of 1,000 in the last decades. In fact, 14 nm transistors are available in today's integrated circuits. As Intel's co-founder Gordon Moor made a prediction that 'the number of transistors on a semiconductor chip roughly double every two years', the pace of progress in the semiconductor industry far surpasses that of other industries and also it derives a fundamental shift in digital electronics including computing, communications, storage, and internet. His insight, well-known as Moore's Law, has become the golden rule for innovation of the digital electronics that enables great computing experiences. Although there are increasing controversies over the current exponential growth in semiconductor industry and digital electronics, it is still optimistic that the innovation continues throughout the next decades since there are continuing research and technology developments to fulfill Moore's Law.

The breakthroughs that accompanied the vast evolution of electronics allowed us to live in the third-generation of technology as suggested by Edgar Fleisch where the way we learn, work and communicate is fundamentally changed. During the first-generation of the digital electronics, a few mainframes were developed and shared by many users. And then over the period of time of personal computer, the sales and usages of personal

computer grew exponentially and brought about the needs for network and internet. Beyond this generation of technology, third generation mobile devices such as cell phones, smart phones, and tablets were widely accepted by the consumer and became one of crucial part of our daily life. This technology generation is described as wireless communications with a help of portable devices and wireless communication systems. As a result the inexpensive and mobile computing electronics all around us continue to play a crucial role on changing the paradigm of our modern world. In the emerging fourth generation, a variety of electronic functionalities will be embedded on personal electronics in order to deliver the benefits of omnipresent, ubiquitous computing with our daily lives.

As technology generation evolves forward, innovations beyond Moore's Law shift gradually toward the seamless integration of digital computing within our daily lives. For instance, mobile phones have evolved from gadgets for talking to mobile devices with integrated multiple technologies for internet browsing and interaction, data storage, a camera for taking photos, to name a few. It's not just the technology of mobile phone that has dramatically changed over time, the convergence of all different kinds of functions of digital technology gadgets into single device continues to advance. While the technological advances have been so far focused on the driving forces such as performance and cost in order to empower powerful computing at a lower cost for the end user, emerging digital technologies in the next generation of digital electronics take the form of flexible, wearable, and printable electronics as well as smaller and versatile sensing electronics. Electronic devices integrated into a novel system or unconventional form factors start to attract a lot of attention due to their unique degrees of freedom in

flexibility as well as their rich features and integrated novel functionality. And they rapidly find a broad range of applications in consumer health and electronics products for display, sensing, lighting, and energy conversion.

1.2 Wearable Electronics

A key driver for the emergence of new digital technology is human beings' desire for more efficient handling of ever increasing information about both external world and their own day-to-day activities. An increasing awareness of personal health and daily activities has fueled the necessity of bodily worn digital technology what is called today wearable electronics. Wearable technology refers to any electronic devices or products that can be worn by a user to take an advantage of unique features such as mobile computing in his or her action or work.

Typically wearable devices are attached to bendable, lightweight substrates. As a new class of electronic devices, large-area or minute wearable devices are worn or attached to clothing, accessories, jewelry, and human body. Wearable electronics renders continuous and real-time sensing of vital signs, body motions, and the quality of the environment. In addition, the devices integrated with multiple sensors and mobile computing and wireless networking provide users with analyzed data through visualization. As the devices work simultaneously with human actions and are connected to smart applications in a network, wearable technology is growing rapidly due to increase in market of various applications. Wearable devices can find broader applications in mobile healthcare monitoring (blood pressure, heart rate, body temperature, glucose monitoring), fitness and wellness activity monitoring (fitness

tracking, pedometer, and sleep sensors), and military purposes. It also has an impact on numerous applications including displays, energy collection, storage, and lighting devices.

Wearable electronics may consist of clothing, glasses, jewelry, arm or wrist band, foot wear, and skin patches. The future will be even more promising because it will involve the use of new types of electronics, namely thin, conformal, flexible, invisible, and textile-integrated components that are just beginning to emerge from research labs. For instance, flexible batteries have already enabled companies such as Estee Lauder and BioBliss to bring 'powered' cosmetic skin patches to market, whereby the battery applies a voltage over the skin, opening up the skin pores, allowing the cosmetic materials to go in up to 10 times faster than without a power source. The powered cosmetic patch is being developed to sense the need for medicine and to then release the drug molecules accordingly. Designed for anti-wrinkle treatment, the application would not be practical with a thick, rigid button cell battery.

1.3 Substrate Materials for Wearable Electronics

Since wearable electronics is radically changing its form, many types of novel materials for wearable electronics are also in development. This effort is driven by the fact that emerging wearable electronics such as conformal skin patches [1, 2], smart fabrics, and stretchable devices are difficult to be implemented with the old and conventional approach, namely packaging components in a box. Thus needed materials for wearable electronics are required to allow for unprecedented comfort and freedom in wearable electronics design so that the device could be comfortable enough to be worn

daily for long periods of time. The end result is a thin, conformal, flexible and form-fitting electronics device that can be seamlessly integrated on a wide range of surfaces including human skin, beauty accessories, and clothing and so on. Furthermore, the material has to be durable and be chemically resistant to sweat, artificial skin oils as well as cleaning products.

Polymers can be used in flexible electronics as encapsulation materials, dielectric materials, and substrates. Most widely used passive or substrate materials in wearable electronics are polymeric materials due to their mechanical, electrical, and optical properties that meet materials requirements for wearable devices. Although polymers have their own unique properties, the materials are not compatible with the modern silicon semiconductor device processing because the temperatures can surpass 1000 °C. This limitation lowers the available thermal budget significantly for the device fabrication on a polymer substrate.

DuPont™ Kapton® Polyimide films show excellent mechanical and thermal properties. Cured polyimide films exhibit a desirable combination of film properties such as low stress, low coefficient of thermal expansion (3 ppm/C which is close to that of silicon i.e. 2.6 ppm/C), low moisture uptake, high modulus, and good ductility for microelectronic applications. These properties are ideally suited such as a dielectric layer for semiconductor and multiple-chip module device applications. Due to its high glass transition temperature, the film can be stable up to temperatures as high as 350 °C. The polymer film also can be patterned typically by dry etch or laser ablation techniques. However the substrate is usually used for opaque applications in which a transparency of the substrate does not limit the performance of devices such as light emitting diodes and

photodiodes. For optoelectronic device applications, PET (polyethylene terephthalate) and PEN (polyethylene naphthalate) polymers are good choices for the transparent substrate because not only they are optically transparent to broad spectrum of light but also they exhibit desirable mechanical, thermal and solvent resistance properties [3].

Crystalline silicon is also a good candidate as a substrate material for high performance wearable electronics. In current technology, silicon chips are built on silicon wafers of which thickness ranges from 500 μm to 1 mm. The wafers with this bulk thickness are rigid and stiff enough to remain stable after a series of the silicon micro-fabrication processes. However, its mechanical properties can change as the thickness of bulk silicon is slimmed down. The silicon wafer thinned down to between 100 μm to 50 μm becomes so fragile that the wafer may break under its own weight. But the silicon wafer as thin as 50 μm does not allow enough mechanical flexibility. Also handling and processing of such thin wafers require handle substrates as hard support materials for mechanical support of thinned wafers and thus lead to a considerable number of additional process steps [4]. Interestingly to say, silicon wafers at their final thickness about 30 μm become flexible as well as mechanically stable. Therefore using the ultra-thin, flexible silicon wafers makes it possible to integrate high performance wearable silicon chips.

The ultra-thin silicon wafer is produced mostly by mechanical grinding followed by additional polishing steps such as mechanical polishing (CMP), wet chemical polishing, and dry etching to remove damaged layers. And ultra-thin silicon layer can be prepared using SOI (silicon-on-insulator) technology which uses wafer bonding

technology or oxygen implantation. The ultra-thin silicon device layer of SOI wafers can reach as thin as 10 µm and further down to a few hundred nanometers.

1.4 Novel Methodologies for High-performance Wearable Electronics

Organic and inorganic semiconductor materials appear to be a very promising for flexible or wearable electronic applications, mainly because they can be deposited on a flexible substrate at a low temperature and exhibit desirable mechanical, electrical and optical properties for relatively simple device applications. For instance, photovoltaic cells made of organic and inorganic materials on a flexible format can harvest sun energy. And inorganic metal oxide semiconductor materials such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), and tin-doped indium oxide (ITO) are widely used for thin film transistor and display applications due to their unique optical transparency and relatively high carrier mobility. However, the performance of these wearable devices is still inferior to that of silicon chips. Recently, European researchers have developed an 8-bit logic circuit computer processor made of organic semiconductors [5]. 4,000 organic semiconductor transistors were built on top of PEN substrate (polyethylene naphthalate) to create the microprocessor. A clock frequency of the processor is below 10 Hz which is much slower than world's first single chip process, the Intel 4004, which was invented in 1971. Therefore, silicon still would be ideal for high-performance electronics to circumvent the major disadvantages of wearable electronics mainly based on organic and amorphous semiconductors.

In order to create wearable electronics featuring flexibility or bendability as well as high performance, they need to be fabricated on crystalline silicon substrate which is

thin enough to flex. There are many research developments to flexible, ultrathin chip fabrication such as established wafer thinning technique and post-process device layer transfer methods. Flexible, wearable device integration methods can be classified into two categories, mainly post-process wafer thinning and chip-film process module.

Post-process wafer thinning is a subtractive technique that removes the wafer from the wafer backside after circuit integration. Using this method, thinned and flexible device layers are effectively removed from a bulk silicon wafer via back-side wafer grinding, wet chemical etching and dry etching. CMOS inverters and three-stage ring oscillators on flexible plastic substrates by means of transfer printing of single crystalline silicon ribbons [6]. In their work, CMOS logic circuits made of silicon ribbons are enabled by first removing n-type and p-type doped silicon ribbons from SOI wafers through dry and wet etch processes followed by a PDMS (polydimethysiloxane) transfer printing technique. The transfer process is completed by transferring silicon ribbons from the PDMS surface to an adhesive polymer substrate. Flexible CMOS integrated circuits have been implemented by a mechanical exfoliation from the bulk silicon wafer in which electro-chemical plating of a Ni stressor layer and subsequent thermal annealing steps are involved to release the thin pre-fabricated CMOS circuits from bulk silicon wafers [7]. High-performance and increased packing density of flexible circuits including 100 stage ring oscillator and memory cells on 6 nm thick ultra-thin SOI wafers are obtained using controlled spalling technology [8] for the large-area transfer of the devices to a plastic substrate [9]. This controlled spalling scheme has advantages over subtractive techniques such as back grinding process, wet etching and dry etching processes in that the remaining part of the original wafer can be reused which otherwise would be wasted.

Additional advantage of this process is that the wafer release process is performed at room temperature. Another new approach to minimize the waste of wafer material has been developed. This is achieved by applying an isotropic silicon dry etch process to the preprocessed three dimensional FinFETs on SOI wafers [10].

While established silicon wafer thinning is subtractive in nature, it is possible to define the chip thickness or device layer wafer thickness by using preprocessed wafers with buried cavities within dedicated chip areas prior to transistor or CMOS fabrication. After the device fabrication is completed, trenches are etched along the periphery of the dedicated chip areas down to the buried cavities, which leaves thin chips attached only on top of anchors. Then thin chips are released from the wafer by breaking the anchors [11].

1.5 Energy Harvesting for Wearable Electronics

Wearable electronics have evolved from life-saving devices such as pacemakers and hearing aids to fashion accessories such as activity tracking bands, smart watches and glasses. The primary technical demands placed by these devices on their electronic components are low power consumption, ultra-small size and wireless connectivity. Like many other electronic devices, wearable devices are powered by using replaceable or rechargeable batteries or through wired power. Since batteries for wearable devices need to be ideally thin, flexible and compact in size, battery form factors are as vital as their capacity for the application. However it is very challenging to design and integrate all the components for power, data and sensing in miniature mainly because currently widely used batteries are still large compared to other device components. So the currently used batteries such as lithium ion and coin cell types in wearable devices impose restrictions

due to conventional form-factors that inhibit the miniaturization and integration of components that would allow powerful mobile computing capability. As a result managing the power of the device is a major driving work on energy harvesting systems to power the prevalent devices. Therefore a new approach to power wearable devices using energy harvesting technology is a promising and desirable option in that the system batteries are possible to be charged without wire connection or batteries can be replaced to self-sufficiently power devices using harvested energy from ambient energy sources.

There are many solutions that fall within the broad category of energy harvesting. The energy sources that allow for energy harvesting technologies include solar energy, thermal energy, mechanical energy and electromagnetic energy. The ambient energy stored in energy sources mentioned above is converted into another form of energy to power electronic devices via photovoltaic, thermoelectric, piezoelectric and electromagnetic.

Photovoltaic is an energy harvesting system through which sun light is converted to usable electricity. Photovoltaic energy harvesting is advantageous because photovoltaic cells can be made in small forms since they can be manufactured cheaply and reliably with existing semiconductor processes. A solar cell optimized for sunlight can generate 40 mW/cm^2 and it is the highest energy density available from energy harvesting compared to other technologies.

Piezoelectric materials are a class of dielectric materials which can be polarized by an electric field and by a mechanical stress. A piezoelectric harvester generates electricity in response to applied mechanical stresses. Mechanical deformation of a piezo-crystal material leads to generation of electrical charges that can be measured as voltage

from the electrodes. There are a variety of materials used for piezoelectric energy harvesting including monolithic piezo-ceramic material PZT [12], piezoelectric zinc oxide [13] and perovskite $BaTiO_3$ [14].

Thermoelectric generators harvest energy by using Seebeck effect that converts heat or temperature differences directly to electrical energy. The resulting energy, namely measured voltage resulting from heat flow from hot spots to cold spots and simultaneous free carrier's movement in the opposite direction, depends on these temperature differences. This mechanism can be applied to the human body where the temperature gradients occur between the body skin and surrounding ambient. However, thermoelectric generators can harvest very low electrical energy which is typically 50 mV due to small temperature gradient between the body and surrounding ambient.

1.6 Thesis Outline

The thesis presents a novel methodology to enable wearable electronic devices as well as a study on functional materials and their sensor applications. Focus is made throughout the thesis on the development of monolithic integration of sensors and silicon transistor circuits. Chapter 2 discusses the thin film heterojunction photodiode made of nickel oxide (NiO) and zinc oxide (ZnO) deposited by low cost energy-efficient sol-gel spin coating. It deals with the semiconducting metal oxide precursor synthesis, sol-gel thin films coating process, thin film surface morphology, and thin film optical and electrical characterization. In the remaining part of the chapter, an application of metal oxide thin films for a ultra-violet (UV) photodetector is discussed.

Chapter 3 discusses the energy harvesting application of sol-gel prepared metal oxide semiconducting thin films. Thin films dealt with in the previous chapter find and extend their applications in an energy harvesting sector. Chemical doping process and characterization to modulate material properties are introduced. The rest of the chapter is devoted to the study of photoelectrochemical hydrogen generation by crystalline planar p-Si photocathodes coated with metal oxide thin films.

Chapter 4 covers the fabrication process of silicon n-channel MOSFETs on SOI wafers. The chapter begins with individual processing steps of silicon MOSFETs. Both physics and characteristics of MOSFETs are covered in detail. A part of chapter includes static current-voltage (I-V) characteristics of MOSFETs. At the end of the chapter, attention is focused on radio frequency (RF) measurements of the transistor in order to assess intrinsic frequency response for future RF applications.

Chapter 5 explains the design and circuit integration for wearable devices. Great emphasis is placed upon the monolithic system integration and a transfer method of circuits from SOI wafers to a flexible platform. Finally the thesis closes in Chapter 6 with summary of results obtained and suggestions for the future work in related areas.

CHAPTER 2: Metal-oxide Semiconductor Thin Film UV Detector Sensor

2.1 Introduction

As a newer class of materials, the transition-metal oxides have attracted a lot of research attention due to their unique properties and device applications as alternatives to silicon based devices [15, 16]. A number of research breakthroughs have been made in this important area of research as a result of progress in material synthesis and in-depth understanding of material properties. For example, Tsukazaki et al. created an oxide heterojunction thin film device made of ZnO and $Mg_xZn_{1-x}O$ which exhibited high carrier mobility and quantum Hall effect [17]. It was a ground breaking work that demonstrated heterostructures formed from two different transition-metal oxides exhibit surprisingly comparable properties as in Si or compounds of semiconductors. Because of their emerging functionalities, since then, significant efforts from many research groups around the world have been made in developing thin film devices from different transition-metal oxides and for different emerging functionalities [18, 19], however, it is yet to be achieved the reproducible and high-quality heterostructure thin film devices mainly due to the defects at the interface.

Among the transition-metal oxides studied, ZnO and NiO thin films are of particular interests. ZnO, an intrinsic *n*-type wide bandgap semiconductor, is a widely studied transition-metal oxide material which has a wide range of applications such as chemical sensors [20], memory devices [21], thin film transistors [22, 23], solar cells [24], and piezoelectric actuators [25, 26], etc. On the other hand, NiO, a naturally acting as a *p*-type semiconductor with bandgap of 3.7 eV, also finds a variety of applications in transparent conducting oxides [27], electrochromic devices [28], chemical sensors [29],

and hole transport layers [30]. The *pn* NiO/ZnO heterojunction thin film devices are one of the promising candidates for optoelectronic and photovoltaic device applications. Indeed, a number of *p*-NiO/*n*-ZnO heterojunction based optoelectronic devices such as ultraviolet detectors [31-33] and light-emitting diodes [34] have been realized using aforementioned growth technologies. Mostly, ZnO and NiO thin films are grown or deposited via chemical vapor deposition (CVD) [35, 36], pulsed laser deposition (PLD) [37, 38], or sputter deposition [27, 39], which requires high vacuum and is energy intensive and expensive. The device applications of thin film transition-metal oxides have mainly relied on thin film deposition technologies which require expensive and energy intensive vacuum equipment in order to achieve a high quality interface of the junction. However, there is an increasing need for and high throughput thin film deposition methods and systems. There are recent strong interests in fabricating oxide thin films using non-vacuum processes such as spray pyrolysis [40] and sol-gel methods [41].In this work, we present a NiO/ZnO *pn* heterojunction UV photodiode prepared by a cost-effective, large-area deposition technique of sol-gel spin coating. The active junction area is composed of a stack of transparent thin layers of ZnO and NiO on ITO coated glass substrates. The morphology, optical transmission, and electrical properties of the ZnO and NiO layers and ZnO/NiO junction are characterized. The UV photodetector performance was studied and demonstrated high responsivity.

2.2 Experimental Details

Precursor Synthesis and Thin Film Deposition: Zinc acetate as a starting material for sol-gel ZnO was dissolved in ethanol with existence of monoethanolamine (MEA).

The precursor solution of sol-gel NiO was prepared by dissolving Nickel (II) acetate tetrahydrate in a mixture of Dimethylaminoethanol (dmaeH) and MEA. The dmaeH was chosen as a Nickel (II) acetate solvent and MEA was added as a stabilizer. Further refluxing at 70 °C for 2 hours rendered them clear or dark green solution for ZnO and NiO respectively. The precursor solution was filtered through a syringe filter (Acrodisc® syringe filter with a 0.2 μm membrane) and then aged for 24 hours for use.

For thin film deposition, the prepared precursor solution was spin-coated for 40 sec at 3000 rpm on clean glass substrates at different spin speeds and durations. In order to evaporate solvents, the coated film was dried at 300 °C after each spin coating. And multiple coatings were repeated to reach a certain thickness of thin films. Finally spin-coated thin films were annealed in N_2 and O_2 atmosphere (450 °C) to improve crystallization.

ZnO/NiO Heterojuction Device Fabrication: The p-NiO/n-ZnO heterojunction was fabricated on ITO coated glass substrates in cleanroom environment. A stack of layers of NiO/ZnO thin films was made by spin-coating multiple layers of NiO first on top of an ITO/glass substrate. Subsequently, a 90 nm thick ZnO top layer was deposited by repeating successive layer on layer spin coatings. This as-coated junction was then annealed in N_2/O_2 environment at 450 °C for an hour. In order to complete the device fabrication, Al top contacts were thermally deposited through a polymer mask layer and then lifted off.

ZnO and NiO Thin Films and ZnO/NiO Device Characterization: The study on surface morphology and cross-sectional structure of thin films and thin film junction was performed by using a high-resolution scanning electron microscope (FEI XL30-SFEG)

and atomic force microscopy (Veeco Scanning Probe Microscope). The Agilent B1500 semiconductor analyzer was used to characterize current-voltage (*I-V*) characteristics of NiO and ZnO thin films and diode. The optical transmittance spectra and device spectral response measurements were made using a setup of the monochromator and lock-in amplifier equipped with a 150W Xenon lamp as a light source.
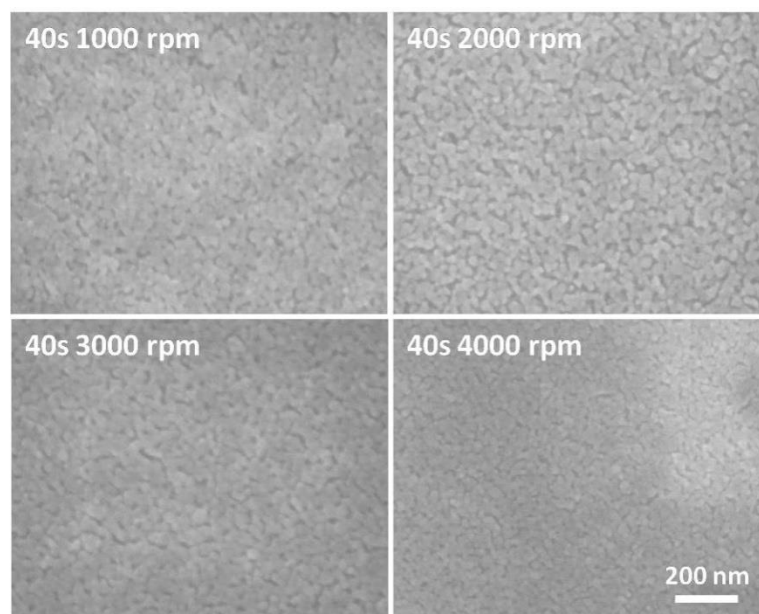
Figure 1. Sol-Gel prepared ZnO thin film surface morphologies vs spin-coating rate. Single-layer coated ZnO thin films were spin-coated on Si substrates by varying the spin-coating speed. The spin coating duration was the same i.e. 40 seconds.

Both NiO and ZnO thin films are elaborated in view of film surface morphology by preparing the films with different coating parameters and post-heat treatment. Unless otherwise mentioned, spin-coated films were pre-heated at 300 °C for 10 minutes after each coating and post-heat treated in N_2/O_2 environment at 450 °C for an hour. In this supporting study, a crystalline Si substrate was used instead of a bare glass substrate, in

that film coatings on a Si substrate facilitated an acquisition of better quality of SEM image than on a bare glass in particular for films with thickness of less than 100 nm for this study.
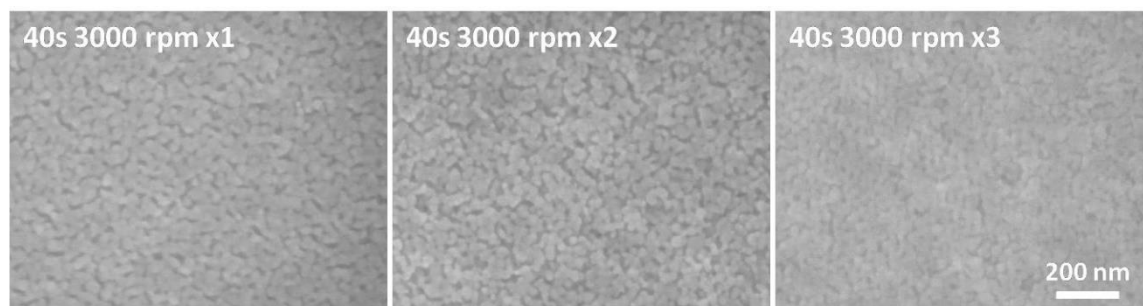
Figure 2. Sol-Gel prepared ZnO thin film morphology dependence on the number of spin-coatings on Si substrate.

No substantial changes in the ZnO thin film surface morphology were observed as spin rates increase from 1000 rpm to 4000 rpm as shown in Figure 1, which in turn determined the thickness of the films. Although the morphological evolution of ZnO films in Figure 1 is difficult to quantify in an absolute term, as the increased spin rate led to continuous and closely interconnected pore structures in coated films. The spin rate was directly related to the thickness of single-layer ZnO thin films. For example, a film spin-coated at 1000 rpm shows a thickness of 75 nm and a film prepared at 4000 rpm becomes thinner about 30 nm. The film thickness measured on each film is indicated in Figure 4 (left).
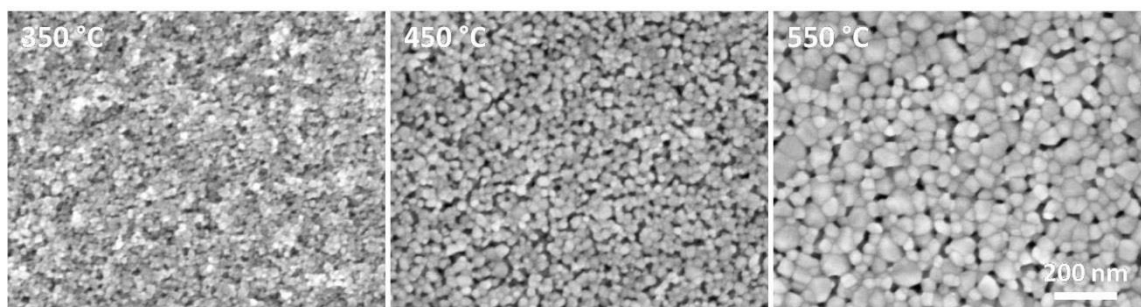
Figure 3. Surface morphology of post-heat treated Sol-Gel prepared double-layer ZnO thin films by spin-coating at 3000 rpm. The films were annealed in N_2/O_2 environment at different annealing temperatures (i.e. 350, 450, and 550 °C)

The number of spin-coatings is another parameter to play a role on the morphological evolution of sol-gel ZnO thin films. As the number of coated layers increases from 1 to 3, film surfaces become more continuous and densely packed as can be observed in Figure 2. By varying the number of coating, in fact, the film thickness increases linearly proportional to the number of stacks of coating as shown in Figure 4.
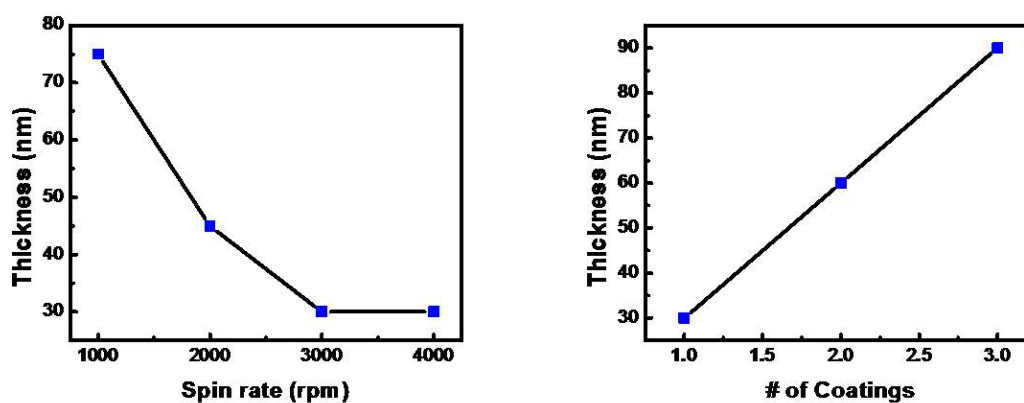
Figure 4. Spin-coating speed versus ZnO film thickness (left) and the number of coatings versus ZnO film thickness (right).

Pre-heat treated films were additionally annealed in a furnace by flowing N_2 and O_2 at different post-heat temperatures. Temperatures changed from 350 °C to 550 °C. The surface morphology changes turn out distinguishable from those mentioned previously. Changes in both interconnected grain sizes and dimensions of pore network are developed during the post-heat treatment at each annealing temperature. The grain size increases at increasingly higher annealing temperatures.
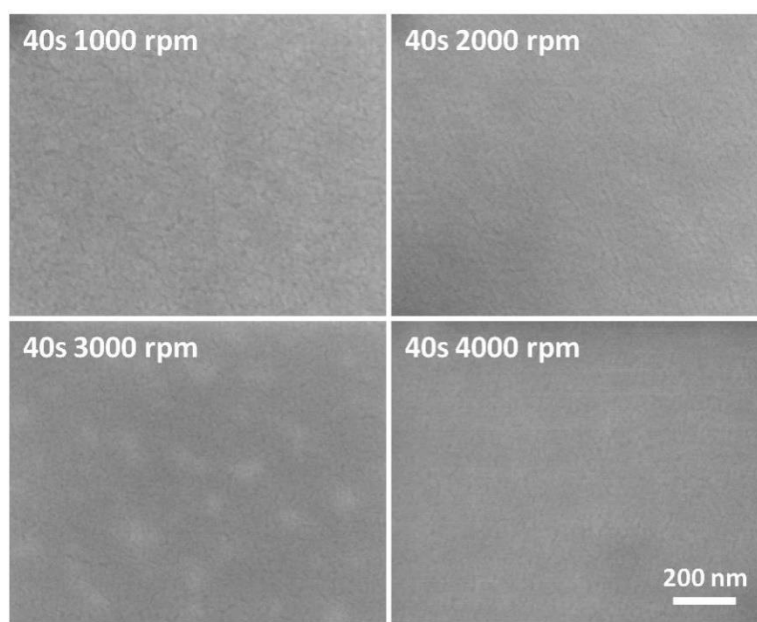
Figure 5. Sol-Gel prepared NiO thin film surface morphologies vs. spin-coating rate. Single-layer coated NiO thin films were spin-coated on Si substrates by varying the spin-coating speed. The spin coating duration was the same i.e. 40 seconds.

As shown in Figure 5 and 6 the morphology of continuous and very dense single-layer NiO thin films by sol-gel is little influenced by both the spin coating rate, as in Figure 5, and the number of spin coatings, as shown in Figure 6. The thickness of coated

films can be controlled by changing the spin speed from about 80 nm to 30 nm. In addition, it shows a linear dependence on the number of coatings, as shown in Figure 8.
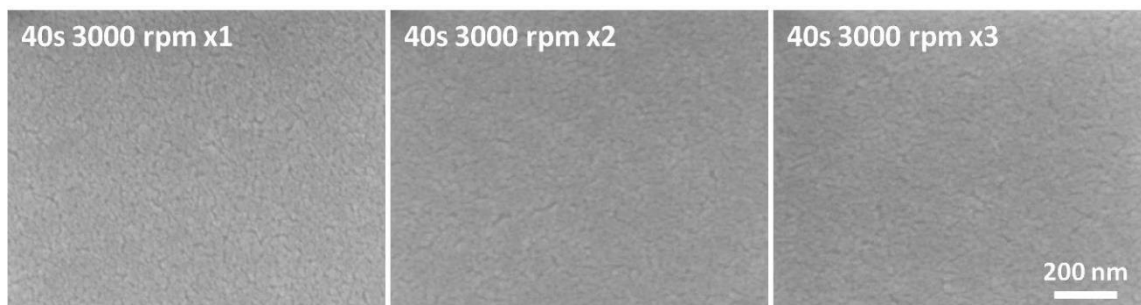
Figure 6. Sol-Gel prepared NiO thin film morphology dependence on the number of spin-coatings on Si substrate.

The post-heat, treatment of the NiO films affects the film morphology in a way that increasing the annealing temperature leads to less porous and continuous film surfaces.

Figure 7. Surface morphology of post-heat treated Sol-Gel prepared double-layer NiO thin films by spin-coating at 3000 rpm. The films were annealed in N_2/O_2 environment at different annealing temperatures (i.e. 350, 450, and 550 °C)
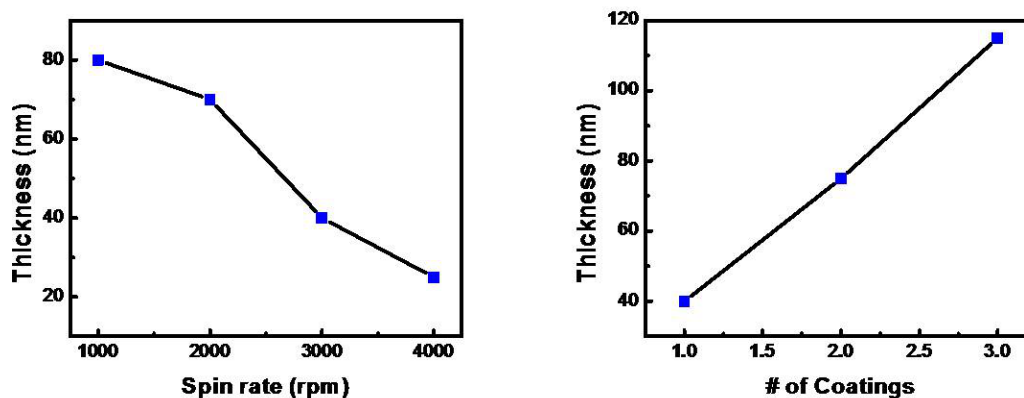
Figure 8. NiO film thickness versus spin-coating speed (left) and the number of coatings versus ZnO film thickness (right).

2.3 Results and Discussion

Thorough study of thin film coating was performed and the thin film quality and thickness was found to be dependent on spin-coating rate, number of coating, and annealing temperature, etc. Film quality remains with multiple coating and almost linear dependence of film thickness vs numbers of spin-coating was observed. In order to achieve certain thickness and eliminate potential pin-hole defects, ZnO and NiO thin films were coated for three times for the *pn* junction devices. Figure 9 shows top view SEM images and AFM images of NiO and ZnO thin films with 3-time spin-coatings. Both NiO and ZnO films exhibit smooth and pinhole free surface in the large scale, and microscopically show a polycrystalline nature with nanoscale grains. However, the grain size of NiO thin film from SEM image is found to be around 25 nm in Figure 9(a), which is much smaller than that of ZnO (about 100 nm) in Figure 9(d), and moreover, NiO thin film exhibits denser packing of the nanoparticles with less spaces between grains and the surface is smoother. A typical 3-time coating NiO thin film has an average thickness of

around 140 nm, while ZnO thin film is about 90 nm thick, measured from cross section SEM. AFM images with a scanned area of 1 μm^2 manifest the relatively surface smoothness of NiO and ZnO thin films. The measured root mean square roughness of NiO and ZnO is about 1.5 nm as described in Figure 9(b) and (c) and 4.2 nm in Figure 9(e) and (f), respectively. It is imperative that the surface of thin films be smooth as well as pin-hole defect free for abrupt junction interface. Through this prism, the nanoscale surface roughness of both films is favorable in device applications.
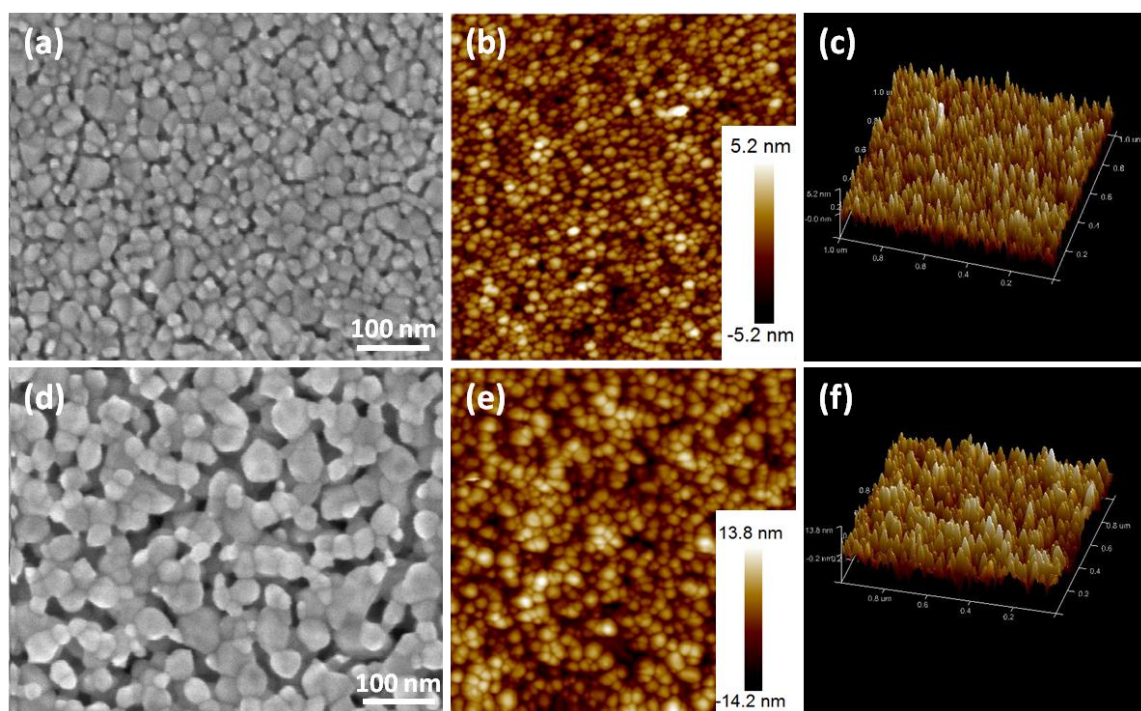
Figure 9. (a) SEM and (b). (c) AFM images of a sol-gel NiO thin film prepared by 3-time spin-coatings on glass substrates. (d) SEM and (e), (f) AFM images of a sol-gel ZnO thin film by 3-time spin-coatings on glass substrates.
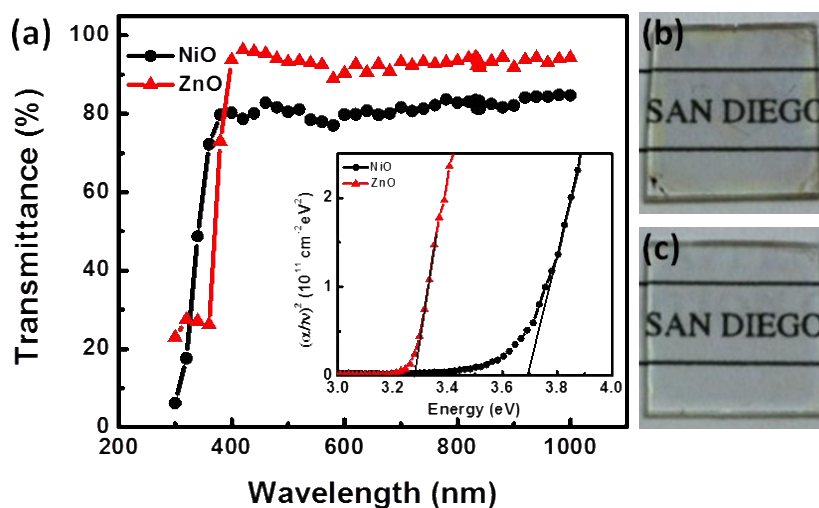
Figure 10. (a) Optical transmission spectra of NiO and ZnO thin films. Inset shows the estimation of the direct energy bandgap (E_g) for sol-gel NiO and ZnO thin films, respectively. (b) and (c) optical images of the NiO and ZnO thin films, respectively.

Figure 10 shows the optical properties of sol-gel processed NiO and ZnO thin films. The NiO thin film (3-time spin-coating and with a thickness of 140 nm) has a transmittance of approximately 80% over the wavelength of 380 nm – 1000 nm (onset absorption at 310 nm), while the ZnO thin film (90 nm thick with 3-time coatings) appears to be highly transparent with an average of greater than 90 % in the wavelength of 400 nm – 1000 nm (onset absorption at 365 nm) in Figure 10(a). The inset shows the optical bandgap (E_g) of sol-gel thin films extrapolated using Tauc plot, which are ~ 3.7 eV and ~ 3.3 eV for NiO and ZnO, respectively. Figures 10(b) and (c) are optical images of the highly transparent NiO and ZnO thin films on a piece of paper where letters underneath the films are very clearly seen. Note that letters underneath the ZnO thin film is slightly clearer than that underneath NiO film, which agrees well with the transmittance measurements in Figure 10(a).
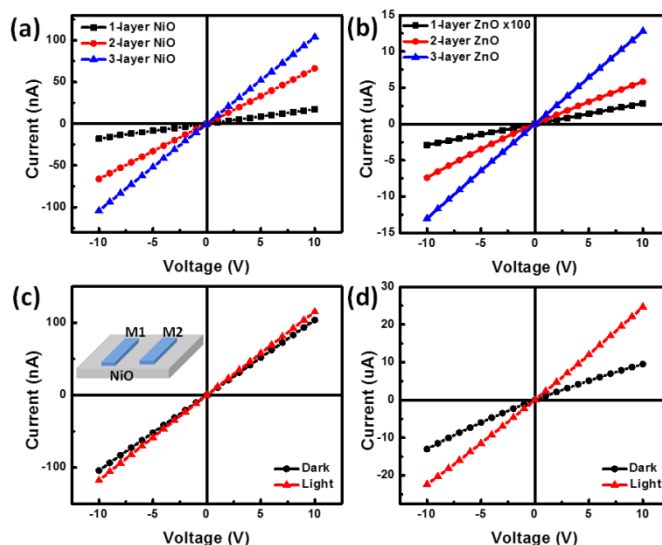
Figure 11. Current-Voltage (*I-V*) characteristics of NiO (a) and ZnO (b) thin films with different film thickness. Inset in (b) shows magnified *I-V* characteristics of single-layer ZnO thin film. (c) NiO and (d) ZnO thin films with 3-time coatings in dark and under illumination.

The effect of thin film thickness on the resistance of sol-gel NiO and ZnO films is shown in Figure 11. Three co-planar and equidistant ITO and Al contacts were deposited on each film by sputtering and electron beam evaporation, respectively. Sputtered ITO is proven to form a good ohmic to NiO thin films, as shown by the linear *I-V* in Figure 11(a), while the e-beam Al forms reasonably good ohmic contacts to ZnO films, as shown by the linear *I-V* characteristic of the ZnO thin films with different thicknesses by applying different numbers of coatings in Figure 11(b). Albeit there exists no consistent linear relationship between resistivity change and thickness change, it is evident that an increase in film thickness results in an increase in film conductance. As the thickness of NiO increased from 50 nm (1-layer NiO) to 140 nm (3-layer NiO), the current measured at an applied 10 V increases by four times. Similar increase in conductance was observed

for ZnO thin films with 2- and 3-time coatings, while the 1-time coating thin film shows much more resistive characteristics as shown in Figure 11(b) with a magnification factor of 100. The reason is not well resolved but we believe that these resistive characteristics might be due to the depletion of carriers arising from a discrete film structure when the ZnO film is very thin. The resistivity of thin films increases with the decrease of thin film thickness, which is in agreement with reported results [42]. The 90 nm ZnO thin film is about 100 to 125 times more conducting than the 140 nm NiO thin film, which is probably due to high carrier concentration and mobility (electrons) in ZnO than those of the holes in NiO, although both films are too resistive to have reliable Hall effect measurements. The NiO nanoparticles have much smaller grain sizes in Figure 9 and thus much larger surface area and much more surface trap states. Note that both of the *I-V* characteristics of ZnO and NiO thin films were measured in dark, due to the photoresponses as shown in Figure 11(c) and (d).

Figure 11 (c) and (d) show the *I-V* characteristics of ZnO and NiO thin film as photoconductors with an metal-semiconductor-metal (MSM) configuration, where two metal pads (ITO on NiO and Al on ZnO) are separated for about 450 μm from each other and light is illuminated from the top (metal contact side) using Xenon lamp. Both NiO and ZnO are prepared by 3-time coating. Both oxide thin films show photoconductor behavior, while current increase due to photogenerated carriers is about 5% and 100% for NiO and ZnO thin films at +10 V, respectively. The very small photocurrent in NiO thin film maybe due to recombination at the surface trap states whose number is much larger compared to ZnO thin film because of the much smaller NiO nanoparticle grain sizes and larger surface area in Figure 9.
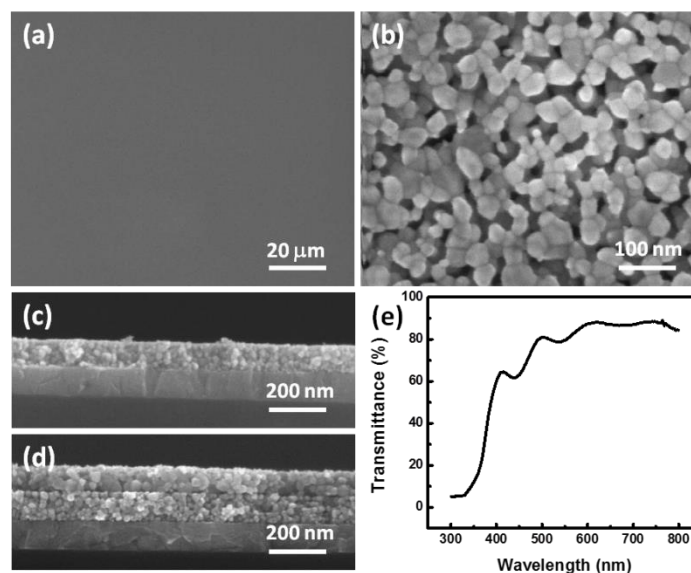
Figure 12. (a – b) Top-view SEM images of sol-gel ZnO thin films deposited on top of NiO. Cross-sectional SEM images of (c) NiO thin film spin-coated 3 times on ITO glass and (d) a stack of layers of ZnO/NiO heterojunction on ITO glass, (e) Optical transmission spectrum of ZnO/NiO heterojunction diode on ITO glass.

The NiO/ZnO heterojunction coated on ITO glass substrates by multiple spin-coating steps and stacking ZnO on the top of NiO layer showed excellent surface smoothness and large area uniformity, as shown in Figures 12(a) and (b) by the top view SEM images of ZnO surface with different, from low to high, magnifications. The grain sizes and morphology of ZnO thin film coated on NiO film in Figure 12(a) and (b) are similar to that of the ZnO thin films directly coated on bare glass in Figure 9(d), indicating reproducible, robust, and substrate independent sol-gel process. Figure 12(c) and (d) compares the cross section of a NiO thin film (3-time spin-coating) and NiO/ZnO heterojunction (3-time coating each). A very smooth interface between NiO and ZnO is clearly identified, which supported the feasibility, capacity, and robustness of low cost large area sol-gel process for the formation of heterostructure and functional devices. The

transmittance spectrum of the NiO/ZnO heterojunction diode shows good transparency of greater than 80% over the visible to infrared (IR) range (500 nm -1000 nm). At short wavelength below 365 nm the *pn* junction absorbs at least 80% of incident light, which agrees very well with optical absorption and bandgap results measured from individual thin films on bare glass in Figure 10(a) and its inset.

Figure 13(a) shows the rectifying *I-V* characteristics of a typical NiO/ZnO heterojunction device in dark. The *pn* diode exhibits a rectification ratio of ~50 (at +/- 5 V bias) in the dark. Figure 13(b) shows the photocurrent and dark current under different biasing voltages. The inset shows the schematic representation of the device under top illumination. An ON/OFF (I_{photo}/I_{dark}) ratio of about 100 was achieved at a reverse bias of -5 V. Note from Figure 13(b) that there is no photovoltaic effect observed, which is most likely due to no direct light illumination to the junction area during testing, as discussed in the following paragraph. The nanocrystalline nature of NiO and ZnO layers and lack of sharp junction interface might also have some effects. Note that in our measurements in Figure 13(b) inset, the incident light was illuminated from the top of the photodiode, which means that the incident light was shined to ZnO layer first and more importantly the majority region of *pn* junction is not illuminated with light, with only small area at the edge are under illumination by diffusion and diffraction of light. The fact that only very small portion of the *pn* junction is under direct light illumination maybe the reason causing no photovoltaic effect observed in the NiO/ZnO device measurement. Apparently, light illumination from the back-side (NiO side of the junction) was favorable from a perspective of device physics, NiO has wider bandgap than ZnO, and more importantly the entire *pn* junction will be illuminated under light. However, we are

limited by the device structure, Al/ZnO/NiO/ITO on glass, where UV light illumination from the glass side is not possible. Current on-going efforts involve making devices on quartz substrates, which are transparent to UV light. The illumination from NiO side possibly renders much larger photoresponse and quantum efficiency not only by allowing more efficient light absorption by junction region and within both NiO and ZnO, but also through increased light absorption by taking advantage of top Al contact as a reflection mirror (Al reflects UV very effectively [43]). An alternative approach will be fabricating devices with reserved structure, such as ITO/NiO/ZnO/Al/glass, which, however, is less desirable due to (i) potential Al_2O_3 formation between Al and ZnO during sol-gel annealing, (ii) possible poorer morphology and film quality because in this case NiO layer is coated on ZnO film and the latter has much larger grain size and porosity in Figure 9.

Figure 13(c) shows the spectral response of a typical NiO/ZnO device under reverse bias of -5 V, which measures the photoelectric sensitivity to incident light energy with the wavelength of interest from 300 nm to 450 nm. The responsivity (R_λ in A/W) measures the ratio of photocurrent to incident-light intensity at certain wavelengths, which was estimated by comparing the photocurrent of the NiO/ZnO device to that of a Si photodetector (Newport 818-UV photodetector), assuming an identical illumination

$$R_\lambda = J_{ph}/ L_{light} = R_{\lambda-}Si_{PD} * J_{ph-NiO/ZnO}/ J_{ph-SiPD} \tag{2.1}$$

where J_{ph} is the photocurrent and L_{light} is the incident light intensity, $R_{\lambda-SiPD}$ is the photoresponsivity of calibrated 818-UV photodetector, and $J_{ph-NiO/ZnO}$ and $J_{ph-SiPD}$ are the

photocurrent densities measured from the NiO/ZnO device and the Si photodetector reference, respectively. A series of specifications for the measurement is available in our pusblished work [44].
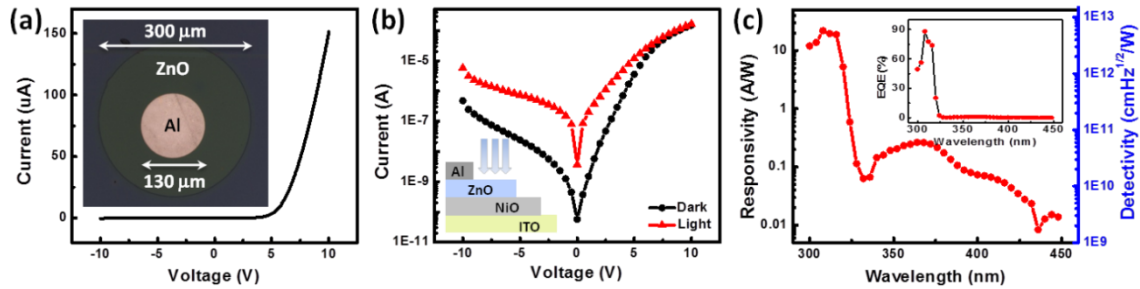
Figure 13. (a) I-V characteristics of the Al/n-ZnO/p-NiO/ITO heterojunction diode on a glass substrate. (b) I-V characteristics measured in the dark (black dots) and under AM 1.5 illumination (red triangles). (c) Responsivity (left y-axis) versus wavelength and calculated detectivity (right y-axis) at a reverse bias of -5V.

NiO/ZnO devices show excellent UV sensitive visible blind photodetection, with the UV-to-visible rejection ratio ($R_{310\,nm}/R_{450\,nm}$) of 1,600 in Figure 13(c). There are two peaks of responsivity at 310 nm and 364 nm, which are associated with absorption edges of sol-gel p-NiO and n-ZnO thin films, respectively. The photoresponsivity peaks at 310 nm and with a value of 21.8 A/W. Note that the photoresponsivity at 310 nm is about 100 times of that at 364 nm, which is due to the fact that during our measurement the incident light is from the ZnO side, both ZnO and NiO absorb light at 310 nm but only ZnO absorb light at 364 nm which generate carriers and contribute to the photocurrent. The fact that the photoresponsivity at 364 nm is so much smaller compared to that at 310 nm possibly indicates very thin effective absorption layer in ZnO considering carrier

concentration might be higher in ZnO and thus smaller depletion and minority diffusion length in Figure 11 and 12.

The right y-axis in Figure 13(c) shows the specific detectivity, which was estimated assuming dark current is the major source of shot noise for the photodiode under a reverse bias of -5 V and using equation (2.2) [45]

$$D^* = R_\lambda / (2qJ_{dark})^{1/2} \tag{2.2}$$

where R_λ is the responsivity, q is the elementary charge of a single electron, and J_{dark} is the dark current at a given reverse bias. The specific detectivity at 310 nm is 1.6×10^{12} $cmHz^{1/2}W^{-1}$ or Jones. The external quantum efficiency (EQE) of the heterostructure PD can be also estimated using equation (2.3)

$$EQE = (R_\lambda/\lambda) * 1240 \text{ (nm·W/A)} * 100 \text{ \%} \tag{2.3}$$

where R_λ is the photo responsivity in A/W at a given wavelength of incident light and λ is the wavelength in nm. The calculated EQE is shown in Figure 13(c) inset with a maximum value of 88% at 310 nm.

2.4 Summary

The thin film *p*-NiO/*n*-ZnO heterojunction photodiode which is formed between two wide bandgap transition-metal oxides has been fabricated using a simple and inexpensive method of sol-gel spin-coating. In dark condition, the *pn* heterojunction

photodiode exhibits a good rectifying behavior at room temperature. Under a reverse bias condition across the junction, the photodiode gives a photoresponse under illumination. The *pn* heterostrucutre operated in the wavelength range of 300 nm to 450 nm gives an exceptional performance in the UV regime. The general characteristics of the heterojunction photodiode reveal a distinct photoresponse with a very impressive maximum responsivity of 21.8 A/W and equivalent external quantum efficiency of 88% at 310 nm. Our results demonstrated that the high responsivity heterojunction photodiodes, and other functional electronic and optoelectronic devices, based on transition metal oxides can be realized by a simple and cost effective sol-gel thin film deposition technique.

This chapter, in part, is a reprint of materials as it appears in the following publications: Namseok Park, Ke Sun, Zhelin Sun, Yi Jing, and Deli Wang, "High Efficiency NiO/ZnO Heterojunction UV Photodiode by Sol-Gel Processing", Journal of Materials Chemistry C, v 1, p 7333 (2013). The dissertation author was the primary investigator and author of this material.

CHAPTER 3: Metal-oxide Enabled Silicon Photocathode

3.1 Introduction

Hydrogen has become one of the most uniquely promising forms of renewable energies for the future generations. Currently, the majority of hydrogen produced by steam reforming depends on fossil fuels, but it defeats the purpose of sustainable, clean energy. Many researches and technologies have been explored to produce hydrogen from renewable sources of energy. A solar-powered electrolysis of water (H_2O), a viable option to split water molecules and harvest the hydrogen, is of great interest because it essentially converts solar energy to usable and storable volumes of hydrogen (H_2) in a sustainable and environmentally friendly way. Photoelectrochemical water splitting based on semiconductor/liquid electrolyte junctions drives chemical water redox reactions at the surface of electrodes of the photoelectrochemical cells (PECs). In order to be able to split water, semiconducting materials must satisfy stringent requirements; the optical energy bandgap has to exceed the minimum energy of 1.23 eV (described by the difference of two redox potentials), band edges must straddle H_2O redox potentials, and must be stable in an aqueous solution. A variety of semiconducting materials including Si, and III-V [46, 47] or II-VI compound semiconductors and oxide materials, are used as a both light absorber and energy converter. Although Si-based electrodes have been used in less efficient PECs, Si does have some practical benefits such as being abundant on earth, being matured in processing technologies and being a relatively good visible light absorber. Interfacial energetics of *p*-Si are suitable for the light-driven hydrogen evolution; the bottom

of conduction band is more negative than the $E°(H_2O/H_2)$. However, p-type Si electrodes upon illumination do not allow efficient H_2 evolution due to several reasons including Fermi level pinning [48], a large overpotential and a poor photoelectrochemical stability [49] in aqueous electrolytes. The catalytic activity and stability of p-Si photoelectrodes have been improved not only by modifying the Si surface with nano-structures [50-52], but also by depositing some metals [53] or metal oxides. A little attention to enhance a solar-to-chemical energy conversion efficiency of p-Si electrodes has been given to the pn junction Si electrodes where the surface of p-Si is heavily doped with an n-type dopant [49]. The most successful hydrogen evolution catalyst on planar or micro/nano-structured p-Si photoelectrodes has been implemented by the deposition of noble metal Pt; nevertheless, this genuinely rare and valuable metal is not favourable to realize a large-scale and economically viable water splitting system.

From this perspective, earth abundant metal oxide semiconducting materials can be a possible candidate in that the materials have versatile electrical and chemical properties as well as stability in aqueous solution in general. Besides unique material properties and stability, a variety of cost-effective and large-area material preparation methods are available in a different forms of geometric structures including polycrystalline thin films and nanostructures. Many research developments have been focused on the metal oxide semiconductors such as n-type TiO_2 [54], WO_3, and Fe_2O_3 as photoanodes and p-type Cu_2O [55] as a photocathode (structural diversity will also be considered). Among many promising oxide materials, zinc oxide (ZnO) in combination with p-type

semiconductors has been used to improve H_2 evolution kinetics at the interface of p-Si and electrolyte by forming a *pn* heterojunction *p*-Si/*n*-ZnO. Sun et al. reported the incorporation of thin film ZnO by RF (radio frequency) sputter deposition on a *p*-Si photocathode help to reduce in overpotential for the onset of the cathodic photocurrent and increase in current density of the *p*-Si photoelectrode [56]. Although the ZnO thin film from their previous studies required additional metal catalyst coating for better catalytic activity and stability against the electrode degradation, the modification of *p*-Si surface by depositing ZnO thin films promotes the photo-generated charge separation as well as minimize carrier recombination so that the overpotential decreases. Paracchino et al. used a ZnO buffer layer in an electrodeposited *p*-type Cu_2O photocathode where an atomic layer deposition (ALD) ZnO or aluminium-doped ZnO thin film not only presumably provides the uniform hydroxylated surface for a protective layer coating but also assists photogenerated charge separation across the *p*-Cu_2O/*n*-ZnO junction [55]. ZnO thin films prepared in aforementioned works require inherently expensive vacuum or plasma equipment, which is a critical issue on a large scale production. In terms of large scale and low cost production of clean energy, non-vacuum or non-plasma thin film coating methods are preferred technologies.

In this work, we present active *p*-Si photocathodes coated with all sol-gel metal oxide thin films. With respect to the low-cost and scalable production of photoelectrodes, large-area coating and non-vacuum thin film deposition method of sol-gel would have advantages over a vacuum deposition such as RF sputtering and ALD. The sol-gel method allowed a uniform coating of ZnO thin films on a *p*-

Si and a facile way of control over electrical conductivity of the films by a chemical doping process. The effects of aluminium doping of ZnO on the material properties and on the H_2 evolution performance of ZnO/p-Si photocathodes were also studied. Here we also report the effects of ultra-thin and highly transparent protective coating of nickel oxide (NiO) on the H_2 evolution reaction of sol-gel ZnO or aluminium doped ZnO (hereafter it is abbreviated as AZO) inserted p-Si photoelectrodes.

3.2 Experimental Details

ZnO thin films were prepared by a sol-gel spin coating method. The details of sol-gel synthesis and thin film deposition conditions can be found in our previous work [57]. The Al doping of ZnO was successfully performed via the same sol-gel method. The doping concentration was controlled by changing the concentration of Al contents during a sol-gel synthesis. Al contents varied 0.5, 1, 2 and 4 (at. %) by the atomic ratio to a Zn atom. The film deposition of AZO on a p-Si followed the same steps like we coated ZnO thin films. As a protective layer of the photocathode, ultra-thin layer of NiO was also deposited by the solution method.

The study of surface morphology of sol-gel thin films was performed using a high-resolution scanning electron microscope (FEI XL30-SFEG). A Hall effect measurement system was used to determine the carrier concentration and Hall mobility of ZnO and AZO thin films. In order to study crystal structures of ZnO thin film on a p-Si, x-ray diffraction (XRD) analysis was made. And x-ray

photoelectron spectroscopy (XPS) provided the elemental composition of ZnO, AZO, and NiO thin films. The XPS spectra of the thin films were taken using a Kratos spectrometer (AXIS Ultra DLD) with a monochromatic Al Kα radiation ($h\nu$ = 1486.69 eV) and a concentric hemispherical analyser. The optical transmittance spectra measurements were obtained using a setup of the monochromator with a combination of lock-in amplifier. 150 W Xenon lamps were used as a light source.

The PEC properties of ZnO|p-Si photocathode were measured in a cycle voltammetry 3-electrode cell consisting of a ZnO|p-Si working electrode, a platinium (Pt) mesh counter electrode, and a silver/silver chloride (Ag/AgCl) reference electrode.

3.3 Results and Discussion

Figure 14 shows results of the electrochemical and photoelectrochemical measurements from different photocathodes made of bare p-Si, sputtered ZnO|p-Si, and sol-gel ZnO|p-Si, respectively. All of the three electrodes compared exhibited negligible current in a dark condition. Without light illumination bare p-Si electrodes showed an exponentially increasing anodic current due to majority carrier of holes in the bare p-Si. The coating of sol-gel or sputtered ZnO thin films on p-Si suppressed the exponentially increasing anodic current in the dark. Upon light irradiation cathodic photocurrents were observed at negative potentials from all of the p-Si based electrodes and the photocurrents were found to be proportional to the light intensity. Figure 14 suggests that sol-gel ZnO thin film coatings on p-Si electrodes can improve cathodic current densities at negative potentials. In terms of the cathodic current density, sol-gel ZnO|p-Si outperforms

the sputtered ZnO|*p*-Si photocathode. However, the effect of sol-gel ZnO coating on the photocathode is negligible because of the series resistance losses through a resistive sol-gel ZnO layer.
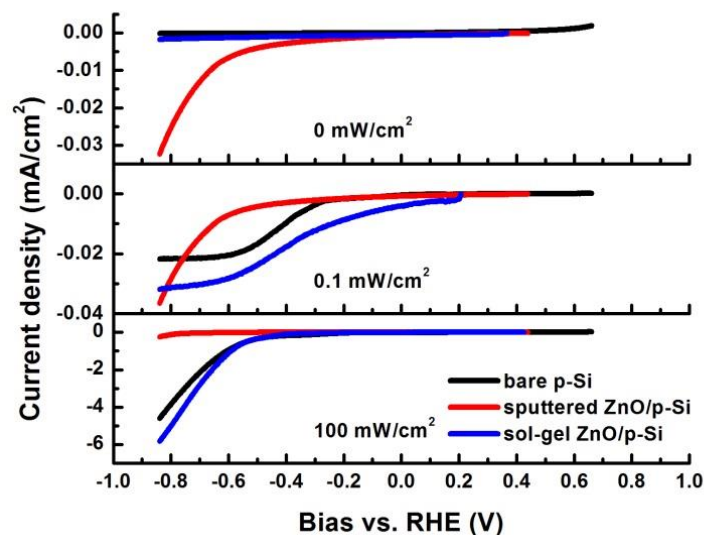
Figure 14. Cyclic voltammetry study on a bare p-Si photocathode and ZnO thin film coated *p*-Si photocathodes. The current-voltage characteristics of the photoelectrodes were recorded in a solution of pH 7 under dark and illumination conditions.

In order to further improve the performance, we first doped sol-gel ZnO with Al atoms and then prepared AZO|*p*-Si photocathode. The effects of doping on thin film surface morphologies, crystal structures, electrical properties, and optical properties were also studied. The surface of undoped and AZO thin films consists of uniformly distributed nano-sized grains. In case of AZO thin films, significant changes in the surface morphology were observed. In contrast to undoped ZnO thin films, the surface of Al doped thin films becomes denser as the grain becomes

smaller. The density of pores is closely related to an added Al concentration. As the doping concentration increases, porosity in thin films decreases.
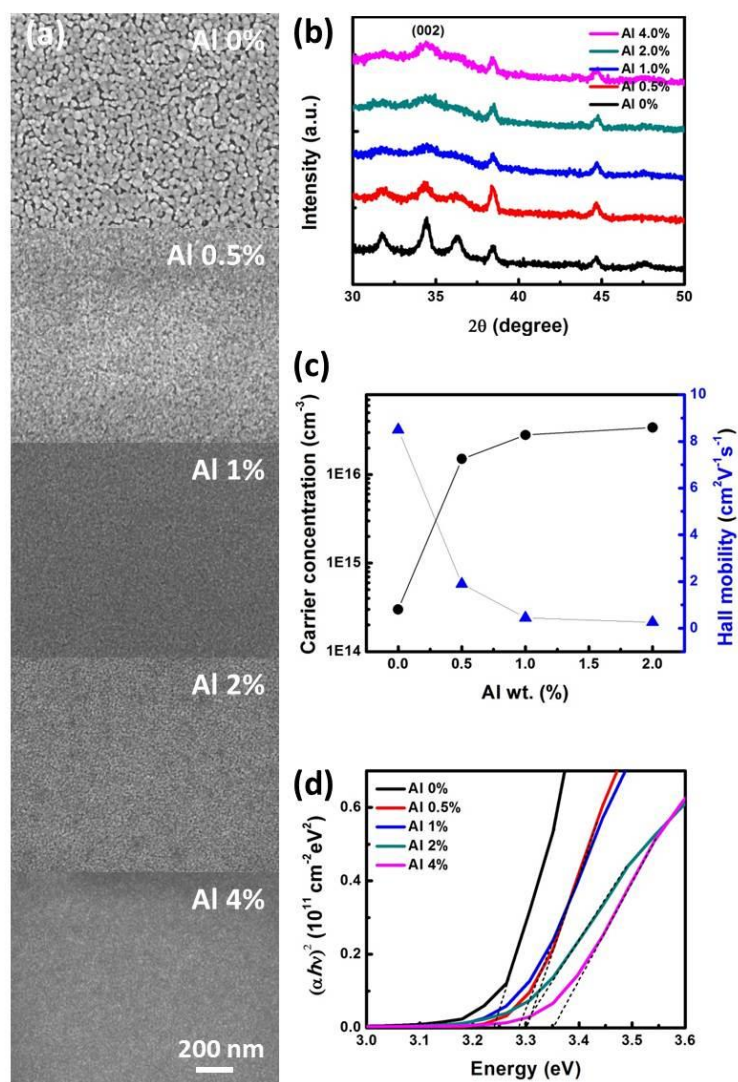
Figure 15. (a) SEM images of ZnO:Al thin films coated on Si surface (b) XRD patterns of AZO thin films with different concentrations of Al (c) Carrier concentration and Hall mobility of Al doped ZnO thin films as a function of Al concentrations (d) Estimated optical energy bandgap of undoped ZnO and AZO thin films.

The XRD patterns identify that ZnO and AZO are polycrystalline with (200) diffraction peaks. The XRD analysis reveals the effects of Al doping and Al concentration on the crystal structure of AZO thin films. The XRD data indicate that peak intensities decrease as a result of Al doping. As a result of the Al doping, appreciable broadening in the x-ray diffraction peaks was observed. This diffraction peak broadening is related to crystallite size or grain size and lattice strain. First, peak broadening is an indication that Al doping into ZnO leads to a smaller grain size in an agreement with the observation of film surface morphology. In addition to the grain size reduction, lattice strain induced by the smaller ion radius of Al dopants ($r_{Zn^{+2}} = 0.074\ n$ and $r_{Al^{+2}} = 0.054\ nm$) can also cause diffraction peak broadening [58].

The electrical properties of AZO thin films by a sol-gel process were studied. The carrier concentration and Hall mobility were measured at room temperature by using a van der Pauw Hall effect measurement system. The carrier concentration of undoped ZnO is 3×10^{14} cm^{-3}. The carrier concentration increases with increasing Al concentration and the concentration reaches its maximum $4 \times 10^{16} cm^{-3}$ at 2 Al wt. %. The data for 4% Al doping are not included because of many inconsistencies of measurement results. The Hall mobility is found to be inversely proportional to the Al concentration. The Hall mobility drops sharply from 8.5 at 0% Al to 1.9 at 0.5% Al and then gradually decreases as low as 0.26 at 2.0% Al. The decrease in Hall mobility is ascribed to the presence of segregated Al atoms at grain boundaries and ionized impurities in the moderately doped ZnO. Although the resistivity of AZO thin film show no linear relation to doping

concentrations, it reaches a minimum at 0.5% Al and then it increases with further addition of Al. Modest values in carrier concentration and resistivity in our study are believed to be due to numerous factors such as limited solubility of precursors, post-annealing temperatures, and annealing atmosphere.

Tauc plots show a direct optical bandgap E_g of the thin films in Figure 15(d). The increase in the energy bandgap is found to continue up to the point of Al at 4% $\left(E_g = 3.35\ eV\right)$ and shows a blue shift of E_g compared to undoped ZnO $\left(E_g = 3.25\ eV\right)$ due to the Al doping about 0.1 eV. It is well known that the increase of carrier concentration in moderately and heavily doped ZnO thin films causes the bandgap widening that is usually explained by Burstein-Moss effect [59, 60]. The optical transmittance of undoped and AZO thin films is always greater than 90% in the visible range.

The chemical state of constituent elements of AZO thin films was studied by X-ray photoelectron spectroscopy (XPS). The narrow scans of Zn *2p*, Al *2p*, and O *1s* spectrum are shown in Figure 16. The core lines of Zn $2p_{1/2}$ and Zn $2p_{3/2}$ show a good symmetry. The binding energy of Zn $2p_{3/2}$ remains at 1021.4 eV in all sample regardless of Al concentrations. Al *2p* peaks show lower peak intensity centered at a binding energy of 74.2 +/- 0.1 eV. And the peak intensity increases as a result of increasing Al concentration, which indicates that Al increases at the surface according to the increasing Al doping concentration.

The XPS spectra of O *1s* for AZO thin films are shown. The O *1s* peaks for samples before and after Al doping show asymmetry and have a shoulder at a

higher binding energy. The lower binding energy peak at 530.0 eV is originated from lattice oxygen in ZnO while higher binding energy peaks are attributed to the presence of hydrated oxides as its peak located at 531.1 eV (OH) or 533.0 eV (H_2O) [61].
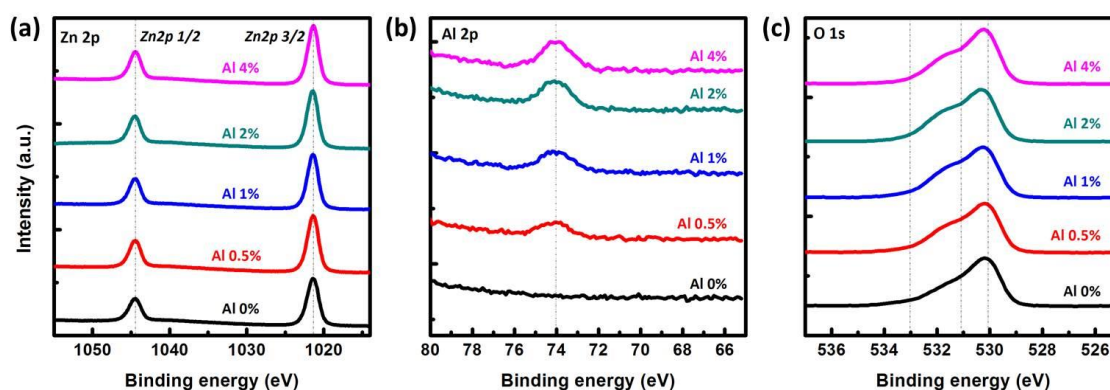
Figure 16. X-ray photoelectron spectra of (a) Zn $2p_{1/2}$ and $2p_{3/2}$ (b) Al 2p, (c) O 1s levels of sol-gel prepared thin films on Si substrates. Al doping concentration (atomic ratio of Al to Zn) increases from 0.5% to 4%.

The photoelectrochemical properties of the sol-gel ZnO|p-Si and AZO|p-Si electrodes were characterized in a pH 7 aqueous electrolyte using a 3-elecrode voltammetry configuration. Figure 17 shows the measured current densities versus applied voltage from the sol-gel ZnO|p-Si and AZO|p-Si photocathode as a function of Al doping concentration in dark and under illumination. The single layer of each thin film was spin coated at various spin speeds in order to have almost same thickness of coatings on a p-Si substrate. Resulting about 30 nm thick AZO thin films transmitted more than 90% of visible range of incident light without a significant loss of incident light energy. In the dark condition, a low

cathodic current was observed from each electrode. A local minimum occurred in the dark current-voltage sweep at which the cathodic current changes from increasing to decreasing. The cause of the sharp changes in the cathodic current is unclear at this point, but it is possibly associated with fast degradation of the AZO thin films in aqueous solution.
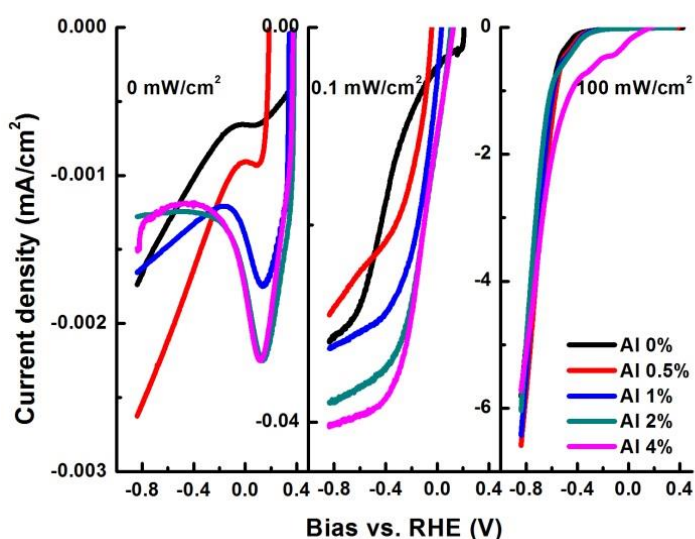
Figure 17. The effects of AZO thin film coating on photoelectrochemical behavior of *p*-Si photocathodes.

Upon illumination of electrodes under the lower light intensity (0.1 mW/cm^2), photocurrent densities increased beyond the dark current densities and they showed a correlation to Al doping concentrations. Under the illumination of lower incident light density, turn-on potentials of cathodic photocurrent slightly shifted to more negative bias. As the illumination intensity increased (100mW/cm^2) photocurrent rapidly increased but its dependence on Al doping concentration

became negligible. In the most favorable conditions, cathodic current densities of the AZO (0.5 wt. % Al)|*p*-Si electrode increased by just 30% compared to that of ZnO|*p*-Si photocathode under illumination at 100 mW/cm^2. This inferior performance of the sol-gel ZnO|*p*-Si photocathodes is possibly attributed to poor stability of AZO thin film layers in aqueous electrolyte solution.

The stability of ZnO in aqueous solution depends on pH values of electrolyte solution as well as UV illumination. ZnO exposed to aqueous media undergoes dissolution under corrosive conditions of extreme pH levels below pH 5 or above pH 11 owing to the relatively high solubility of zinc in these pH ranges [52]. The dark dissolution of ZnO in acidic solution is attributed to both chemical and electrochemical reactions. Chemical dissolution is due to direct reaction with hydrogen ions which can be expressed [62];

$$ZnO + 2H^+ \rightarrow Zn^{2+} + H_2O \tag{3.1}$$

and is also due to the electrochemical reaction as following.

$$ZnO_{surface} + H^+_{solution} \rightarrow ZnO \cdot H^+_{surface} \rightarrow Zn^{2+} + OH^-_{solution} \tag{3.2}$$
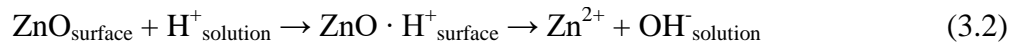
The dark dissolution of ZnO|*p*-Si and AZO|*p*-Si electrodes in pH 7 was found moderate and relatively stable. In contrast to the dark dissolution in electrolyte solution at the neutral pH, ZnO|*p*-Si and AZO|*p*-Si electrodes suffered from rapid dissolution after a series of photoelectrochemical behavior tests. The

degradation of ZnO|*p*-Si and AZO|*p*-Si electrodes was confirmed from surface color changes and SEM surface morphology studies before and after the test.
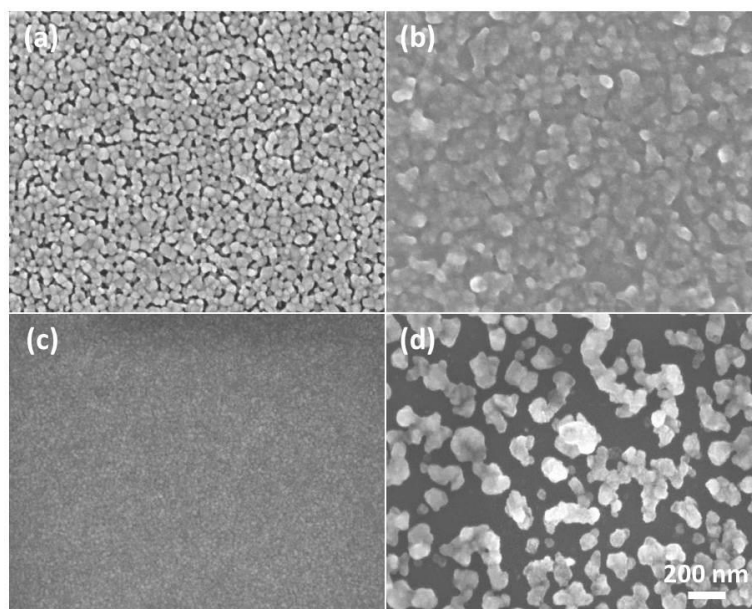
Figure 18. Structural characterization of dissolution behavior of sol-gel ZnO and AZO thin films coated *p*-Si photocathodes. SEM images of ZnO|*p*-Si photoelectrodes (a) before (b) after PEC measurements and AZO|*p*-Si photoelectrodes (c) before (d) after PEC measurements.

SEM images in Figure 18 show that surface morphologies of ZnO and AZO (4 wt. % Al) layers changed significantly before and after PEC test. One can notice that after the PEC measurement, the microstructure of ZnO thin films becomes less fine, although it still maintains porous structure. The thickness of ZnO thin films was not measured after PEC tests but uniform thinning of the sample thickness could occur due to the photo-dissolution. Compared to ZnO|*p*-Si electrodes, the AZO|*p*-Si electrodes exhibited a dramatic photo-dissolution behavior in terms of structural changes or forms of surface damage. Localized attacks on the electrode

surface took place and led to formation of pitting corrosion. The pits were observed from all of AZO|p-Si electrodes after PEC test and the size and density of pits differed among electrodes with various Al doping concentrations as shown in Figure 19.
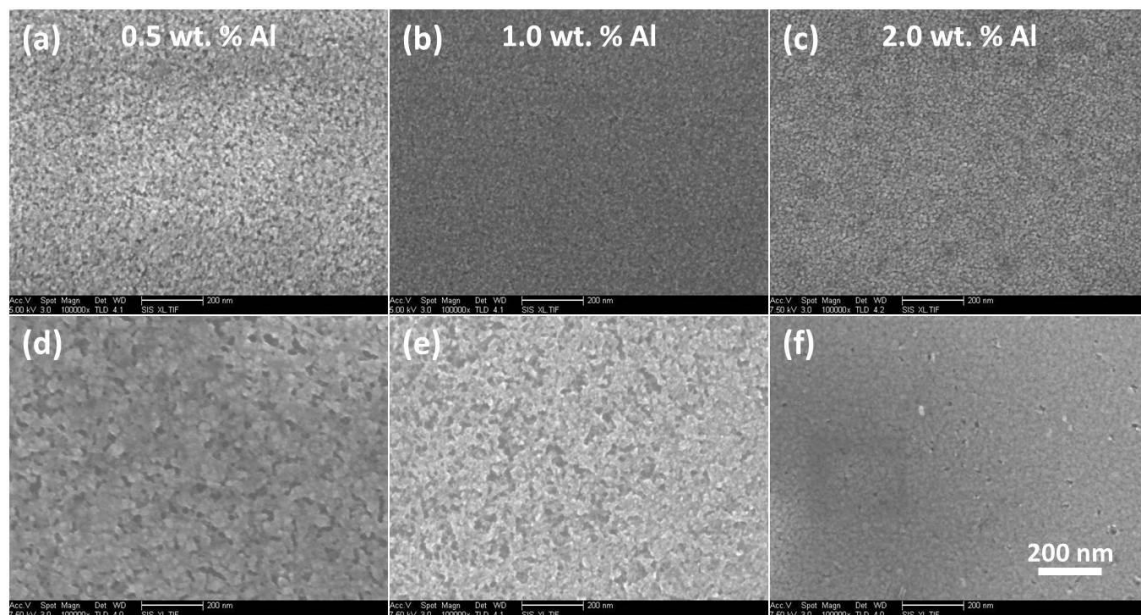
Figure 19. Sol-gel AZO|p-Si electrode surface morphology changes before and after PEC performance tests. SEM images before the PEC test (a) 0.5 % (b) 1.0 % (c) 2.0 % of Al-doped sol-gel AZO|p-Si electrodes SEM images after the PEC test (d) 0.5 % (e) 1.0 % (f) 2.0 % of Al-doped sol-gel AZO|p-Si electrodes.

This localized pitting is caused by differences in potential between different points, which results in non-uniform dissolution rates on the surface. The most obvious and predominant photo-dissolution was observed from the electrode with the highest Al doping concentration (4% wt. Al). Photo-dissolution of ZnO in aqueous solutions has been studied and reported that photo-dissolution is mainly due to photo-generated holes and dissolution rate is higher than dark dissolution

rate at each pH of aqueous solutions [52, 63]. From a thermodynamic perspective, ZnO appears to be stable against cathodic photodecomposition by electron reduction, since the position of the decomposition potential is above the conduction band edge. Thus cathodic decomposition can only occur at high cathodic polarization leading to degeneracy of electrons at the surface. On the other hand n-type ZnO is susceptible to photo-decomposition by photo-generated holes [64]. In order to suppress degradation of sol-gel ZnO|p-Si and AZO|p-Si electrodes upon exposure to sunlight in an aqueous solution environment, a thin layer of NiO was deposited as a protective layer using a solution method. Nickel Oxides are vital materials not only for long established applications such as electrochromic window coatings but also emerging technologies such as environmentally friendly production of chemical fuels. NiO has been found to be useful as water oxidation catalysts for O_2 evolution [65-67] as well as co-catalysts for H_2 evolution. The catalytic activity of semiconductor electrodes [47] and particulate or colloidal photocatalysts [55, 68] for H_2 production has been improved by modifying their surface with NiO co-catalysts. The ultrathin film NiO layer was spin-coated from 0.05M NiO precursor solution prepared by dissolving nickel (II) nitrate hexahydrate [$Ni(NO_3)_2 \cdot 6H_2O$] in ethanol with an additive of Triton X-100 [54]. The as-coated films were heated at 300 °C for 3 min in air. It is believed that the subsequent heat treatment is reasonable to proceed thermal decomposition of nickel hydroxide ($Ni(OH)_2$) into NiO [69, 70]. The coated protective layer uniformly covers the entire surface of ZnO and thin films.
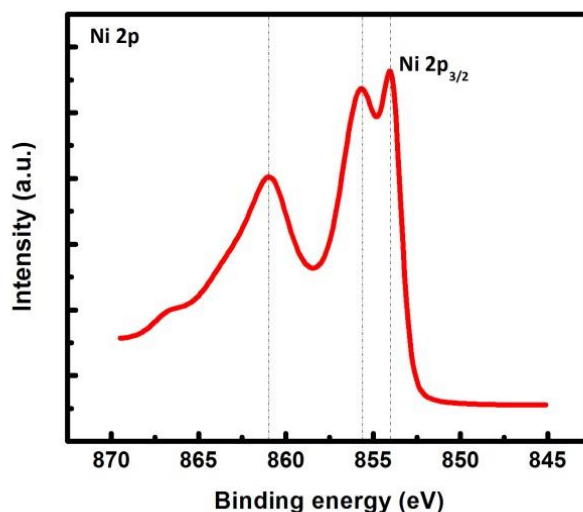
Figure 20. XPS spectra of Ni 2p$_{3/2}$ of NiO protective layer prepared by a solution method.

Figure 20 shows XPS spectra of Ni $2p_{3/2}$ of the prestine NiO on a Si substrate. The spectra show main peaks at 854.0 eV and 856 eV and a broad satellite peak at 861.0 eV. These binding energies of Ni $2p_{3/2}$ are similar to previously reported spectra of the stoichiometric NiO [71]. Although the Ni $2p_{3/2}$ spectrum of protective NiO layer is a similar shape as the stoichiometric NiO, it shows relatively higher intensity at 856 eV. It should be noted that Ni(OH)$_2$ is known to have a peak at 856 eV [72]. In terms of increase in peak intensity, it may indicate the presence of Ni(OH)$_2$ in NiO films after heat treatment.
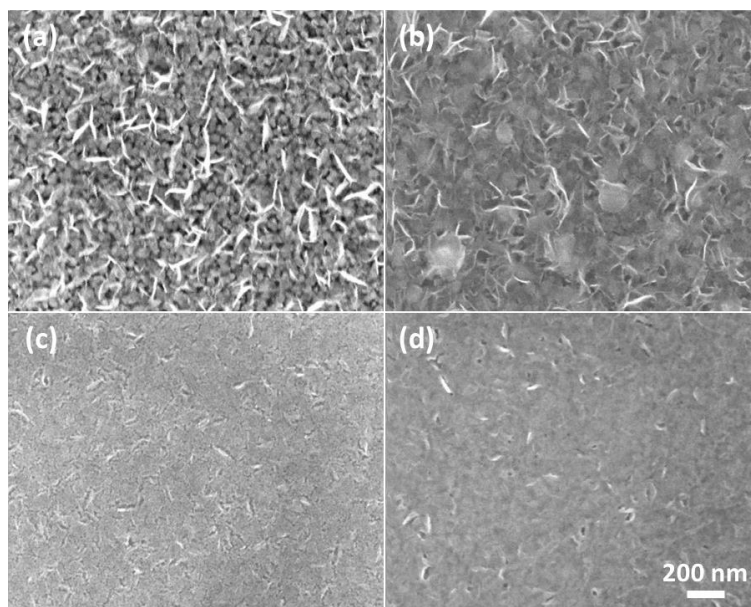
Figure 21. SEM images of spin-cast NiO protective thin films on sol-gel ZnO|*p*-Si (a) and AZO|*p*-Si (c) photocathodes before cyclic voltammetry scans and images after the scan of NiO coated ZnO|*p*-Si (b) and AZO|*p*-Si photocathodes.

The protective oxide layer coating on ZnO|*p*-Si and AZO|p-Si electrodes was confirmed by further studies of surface morphologies of the NiO coated photocathodes. Surface morphologies of the ultra-thin NiO layer on electrodes vary differently among samples. The ultra-thin NiO coating was only a few nanometers in thickness and thus the thin film coating followed a surface finish of underlying layers shown in Figure 21 and 22. For example, NiO coatings on the continuous and smooth surface of (4% wt. Al) AZO thin films showed smooth surface shown in Figure 21(c) whereas coating on the ZnO surface resulted in rough surface profiles as shown in Figure 21(a). After the PEC measurement, SEM images show that a NiO protective layer changes its morphology but still properly covers the surface of ZnO and AZO films as shown in Figure 21(b) and (d).
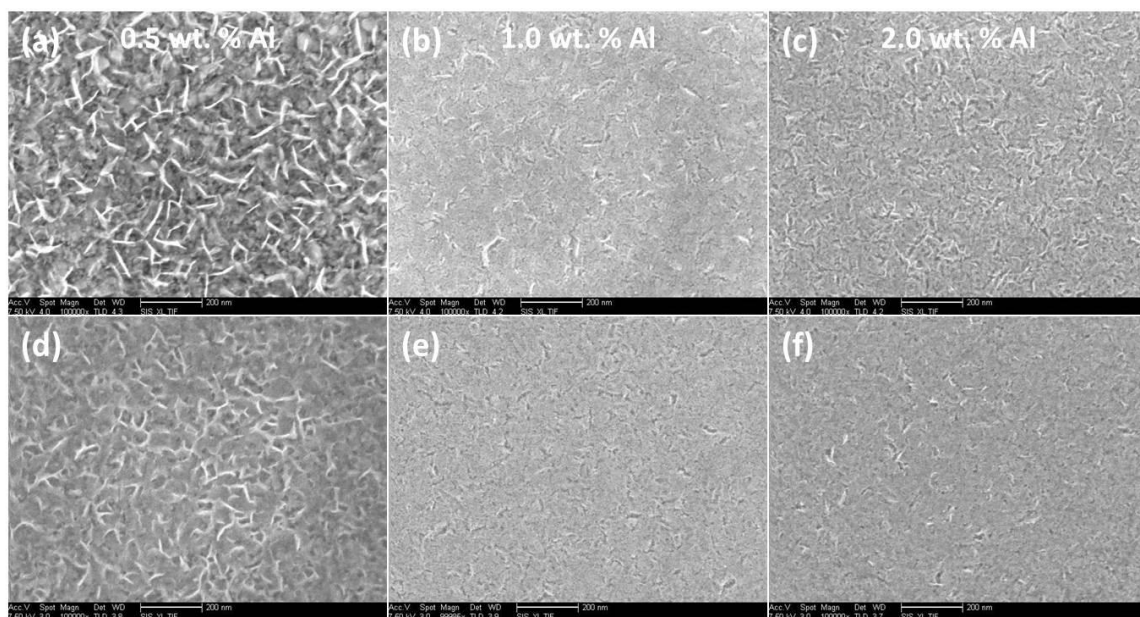
Figure 22. Surface morphologies of ultra-thin monolayer NiO coated on (a) 0.5 wt. % of Al (b) 1.0 wt. % of Al (c) 2.0 wt. % of Al AZO|*p*-Si electrode surfaces. And surface morphology changes after PEC performance tests are shown (d) 0.5 wt. % of Al (e) 1.0 wt. % of Al doped AZO|*p*-Si electrodes, respectively.

HER activities of ZnO|*p*-Si and AZO|*p*-Si photocathodes with NiO protective layer coatings are shown and are compared to a bare *p*-Si photocathode in Figure 24(a). Compared to bare *p*-Si and NiO coated ZnO|*p*-Si, NiO coated |*p*-Si electrodes cyclic voltammetry curves shift in a positive potential direction with linear dependence on the Al concentration. This result indicates the advantages of formation of *pn* junction by coating conducting layers on *p*-Si. Although the HER activity of the cell is still limited by relatively low photovoltages across the *p*-Si and AZO heterojunction, the additional photovoltages play a role on the cathodic current enhancement by facilitating the process of photogenerated charge separation at the *pn* junction. The readers are referred to Figure 23 and Table 1 for the solid-state sol-gel and *p*-Si *pn* heterojunction solar cell performance.
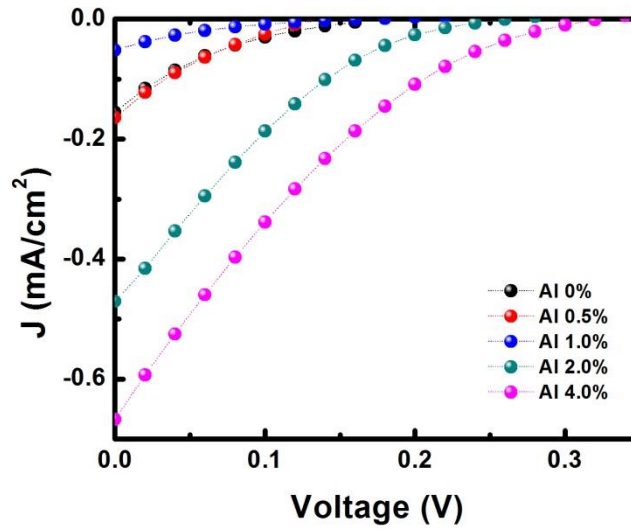
Figure 23. Sol-gel AZO|p-Si solid-state solar cell J-V characteristics of short-circuit current (J_{SC}) and open-circuit voltage (V_{OC}). The solar cell consists of a stack of 80 nm ITO (Ohmic top contact)|30 nm sol-gel AZO|p-Si|Au (Ohmic bottom contact) with the junction area of 0.8×0.8 cm^2.

Table 1. A summary of solid-state solar cell performance parameters based on sol-gel AZO|p-Si heterojunction. I-V characteristics measured under air mass 1.5 global irradiation of 100 mW/cm^2.

Al concentration [wt. %]	V_{OC} [V]	J_{SC} [mA/cm^2]	FF	η [%]
0	0.18	0.15	0.13	0.04
0.5	0.13	0.16	0.18	0.04
1.0	0.17	0.05	0.13	0.01
2.0	0.26	0.47	0.16	0.2
4.0	0.32	0.67	0.16	0.3
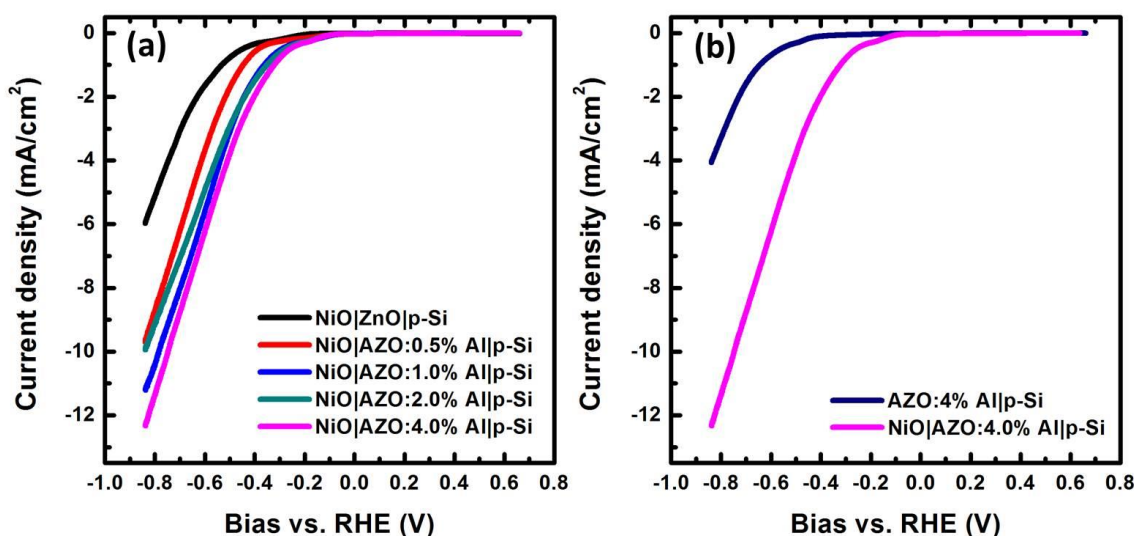
Figure 24. Cyclic voltammetry of the ultra-thin protective NiO layer coated sol-gel ZnO|*p*-Si and AZO|*p*-Si photocathodes under illumination (a) and cyclic voltammetry study of effects of protective NiO layer on AZO|*p*-Si photocathodes with 4% wt. Al doping (b).

In contrast to HER activities of ZnO|*p*-Si and AZO|*p*-Si photocathodes, an overall increase of hydrogen evolving current was observed by the presence of the NiO protective layer coatings. It is substantial evidence that NiO coated photocathodes become stable against photo-dissolution and incorporation of Al into ZnO leads to improvement of HER activity. The resulting photocurrent linearly increased as Al doping concentration increases from Al at 0.5% to 4% except Al at 2% doping in which the photocurrent lies in between Al at 0.5% and 1.0% doping concentration as shown in Figure 24(a). The highest photocurrent was obtained from the Al at 4% AZO|*p*-Si electrode by using a protection strategy with NiO. The current density reached 11mA/cm^2 at -0.8 V vs. RHE which was at least

3 times higher than that of without NiO coating as shown in Figure 24(b) and also higher than that of NiO coated ZnO|*p*-Si electrode. It is noteworthy that the photocurrent density of AZO|*p*-Si electrodes with 4 wt. % Al without the NiO protection was the lowest among the other electrodes due to its poor stability against photo-dissolution. This result indicates that NiO coating provides a protective effect on underlying layers against photo-dissolution. Although the results are promising, the long-term stability of the photocathodes turned out to be poor. The performance of the cell degraded rapidly by 20% within one hour. Thus further studies are necessary to enhance the long-term stability of the electrodes.

3.4 Summary

Despite the limitation of long-term stability, we have shown that active *p*-Si photocathodes for hydrogen evolution reduction can be enabled by means of a cost-effective deposition of ZnO and AZO thin films on a crystalline *p*-Si. Sol-gel ZnO|*p*-Si and AZO|*p*-Si electrodes without a protective coating exhibited negligible effects on hydrogen evolution due to their substantial photo-dissolution in an aqueous environment under illumination. The cell performance was improved by applying a NiO protective layer coating on sol-gel ZnO|*p*-Si and AZO|*p*-Si via a solution method. The ultra-thin protective NiO layer coating gave rise to pronounced improvement on the HER activities of ZnO|*p*-Si and AZO|*p*-S photocathodes. HER activity of AZO|*p*-Si was further improved by increasing Al doping concentration and our results showed a three-fold increase of cathodic photocurrent of 4% Al doped AZO|*p*-Si photocathode compared to bare *p*-Si or ZnO|*p*-Si photocathode. However, *p*-Si electrodes stabilized with all metal

oxide semiconductor thin films showed a poor long-term stability even after 1 hour of photocurrent stability test. Based on our discovery, continuing efforts to demonstrate cost-effective, large area, and stable photoelectrochemical cells are in progress.

This chapter, in part, is currently being prepared for submission for publication of the material. Namseok Park, Ke Sun, and Deli Wang. The dissertation author was the primary investigator and author of this material.

CHAPTER 4: Fabrication of SOI *n*-channel MOSFETs

4.1 Introduction

One of the objectives of this thesis work is to develop an integrated device fabrication approach for solar powered wearable devices. While there are many demonstrations of flexible transistors, organic materials with low charge carrier mobilities are often employed [60, 73-76]. Recently, 2D and 1D transistors using high mobility materials such as graphene [59, 65-67] or InAs [77] have been realized. These recent approaches, however, are far from being developed for production fab-compatible processes. An alternative approach would be to integrate all relevant wearable electronics in thin Si and transfer or embed the system on a flexible platform. There have been many efforts in the past for transferring Si ribbons [78, 79] and sheets [80] to flexible substrates. Our approach differs in that we utilize conventional Si microfabrication process to realize both energy harvesting and computing Si components as will be discussed in this and the following chapters. We therefore utilize Silicon-On-Insulator (SOI) substrates as our starting wafer. Here, we discuss optimization of the fabrication process and realization of RF frequency operation in such devices using an SOI platform. The typical SOI thickness varies from as thin as 10 μm to a few hundred nanometers or even down to a few nanometers through a precise thinning process. Building devices, for example CMOS, on SOI wafers provide some advantages. First of all, it reduces or simplifies the complexity of processing steps by reducing the number of these steps such as the formation of wells and trench isolation. Second, SOI MOSFETs are known to be more immune to the short-channel effects when the device channel length is scaled to shorter dimensions. In this work SOI wafers are chosen as a starting platform to fabricate

MOSFETs. The 2~5 μm Si n-channel MOSFETs are fabricated on a 500 nm thick p-type (100) Si thin film device layer with the doping concentration of 2.2×10^{18} cm^{-3}.

4.2 Experimental Details

4.2.1 Wafer Cleaning

In order to remove impurities on silicon wafer surfaces and generate the high purity of wafer surfaces, SOI wafers were cleaned in hot alkaline and acidic hydrogen peroxide solutions which is called RCA standard wafer clean based on a two-step oxidative desorption and complexing treatment. The first cleaning step (RCA standard clean 1 in short RCA 1) was done in the mixture of H_2O : H_2O_2 : NH_4OH with a volume ratio of 5 : 1 : 1 for the solution. In order for the removal of hydrous oxide film after the RCA1 step, wafers were immersed in 10% HF solution for 10 seconds. The solution for the subsequent RCA standard clean 2 (RCA 2) was prepared by mixing H_2O : H_2O_2 : HCl with a 6 : 1 : 1 volume ratio. This low-pH hydrogen peroxide solution dissolves metallic contaminants from the Si surface and forms complexes to prevent metals from being redeposited on the surface. Each solution was kept at 70 °C during the cleaning treatment. Cleaned wafers were rinsed in high purity and ultra-filtered DI water with resistivity of 18 MΩ·cm and then dried using N_2 blow in order to prevent recontamination.

4.2.2 SOI Wafer Thinning

The SOI wafers used for the fabrication of SOI MOSFETs initially consist of 10 μm silicon thin film device layer overlaying 1 um thick buried oxide layer (BOX) and

thick handler Si. 10 µm device layer films were thinned down to 500 nm using silicon dry etching followed by silicon thermal oxidation and stripping processes.

4.2.3 Source and Drain Junction Formation

First a thick layer of SiO_2 was grown to serve as a diffusion mask for subsequent diffusion step and then source and drain window areas were defined by means of photolithography as shown in Figure 25(b) and (c). The oxide over the source and drain regions were etched in BOE (buffered oxide etch) solution. After trenches for subsequent phosphorus diffusion were formed for source and drain regions, the wafer was cleaned again using the RCA clean procedure.

In our study spin-on dopants (SOD), a mixture of SiO_2 and a certain concentration of dopants (phosphorus) suspended in a solvent, was used as a dopant source. Application of phosphorus solution involved dispensing on a source silicon wafer and subsequent spinning at 3000 rpm to produce a uniform oxide looking film coating. After dopants were spun on, the wafer was heated to 200 °C for 15 minutes to fully evaporate the solvents and to harden the film. It is known that both SOD coating thickness and baking temperature play a role on the doping efficiency in the proximity RTP diffusion [77]. Our optimization of these parameters in this doping process resulted in consistent, acceptable doping results.

The dopant source wafer and device SOI wafers were placed in a rapid thermal process (RTP) system process chamber. The dopant source wafer was in close proximity to each SOI wafer by the quartz spacers between them. In this experiment, the separation gap was 0.4 mm determined by the difference in thickness of a quartz spacer and SOI

wafer. Diffusion was conducted using the RTP system from 800 °C to 1000 °C for 30 seconds depending on process specifications in pure N_2 ambient. At an elevated temperature, vaporized glasses of P_2O_5 are released from the surface of phosphorus SOD source wafer at rates controlled by RTP temperatures and in cumulative amounts controlled by RTP time. The vapors of P_2O_5 are spontaneously transported in the gas phase across the small gap separating the dopant source wafer and adjacent SOI wafers and then uniformly condense on SOI wafer surfaces shown in Figure 25(d). After SOI wafers were unloaded from the process chamber, the wafers were immersed in 10% HF for 1 minute in order to remove the excess un-reacted dopant glass layers from the SOI wafer surface.

Sheet resistance was measured using a four-point probe measurement. In addition, Hall Effects Measurement was conducted after diffusion on 220 nm p-SOI wafers with 1-10 Ω·cm resistivity to estimate the surface doping concentration. The results are summarized in Table 2. Our results agree with previous reports [77, 78].

Table 2. Sheet resistance and surface carrier concentration on 220 nm p-Si SOI wafers as a function of RTP temperature in the phosphorus SOD proximity diffusion.

RTP temperature [°C]	R_S [$\Omega/\square$]	Carrier concentration [cm^{-3}]
800	3400	5.4×10^{16}
850	500	1.2×10^{18}
900	140	9.6×10^{18}
950	78	1.5×10^{19}
1000	33	2.9×10^{19}

4.2.4 Growth of Silicon Dioxide (SiO_2) Gate Dielectrics

After Source and Drain junctions were formed by phosphorus SOD proximity diffusion, SOI wafers were gone through a pre-oxidation cleaning by RCA cleaning steps. And immediately the cleaned wafers were loaded into the oxidation furnace. Dry thermal oxidation was performed in an oxidation furnace in an atmosphere of oxygen at 850 °C. Post-oxidation anneal was performed using rapid thermal annealing in order to reduce the charge trapping and Si-SiO$_2$ interface trap density. The oxide annealing was done in a forming gas ambient (5% H$_2$ / 95% N$_2$) at 450 °C for 15 minutes. After the growth of the gate dielectric layer, its thickness was measured employing a thin film thickness measurement system by the Filmetrics. The thickness of SiO$_2$ was in the range of 5 - 7 nm.

4.2.5 Electrode Metallization

Source and drain metal contact openings to the diffusion areas were formed by photolithography and a subsequent selective wet etch of oxide dielectric layer in buffered oxide etch (BOE) as shown in Figure 25(f). Titanium ohmic contacts to n^+ source and drain regions were formed by electron-beam evaporation through defined source and drain contact opening patterns followed by a lift-off as described in Figure 25(g). In order to form the gate electrode, a lift-off process was used. The area for gate electrode was first patterned using photolithography and then metals, in the different forms of titanium or palladium, were deposited to form the gate electrode. Metal contacts (including source and drain contacts) were annealed at 325 °C in 5% H$_2$ / 95% N$_2$ for 15 min to anneal out x-ray damages during metal deposition by e-beam evaporation and to form an alloy between the metal and Si. At the end of device fabrication process, a layer of SiN$_x$

(silicon nitride) was deposited using PECVD (Plasma-enhanced chemical vapor deposition) as a passivation layer. The passivation layer protects against mechanical damages, moisture, and mobile alkali ions. Finally openings through the passivation layer to access to metal bonding areas.
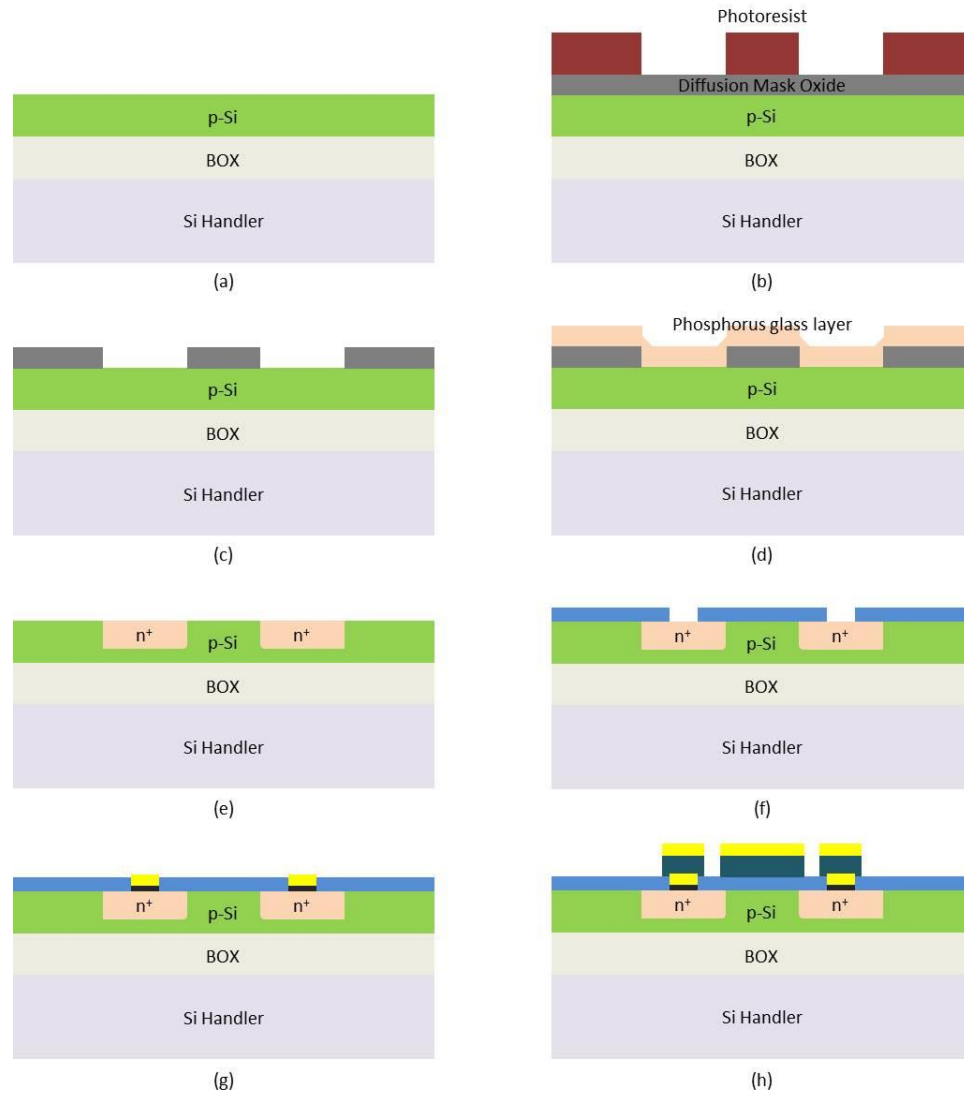
Figure 25. SOI *n*-channel metal gate MOSFET fabrication flow. (a) *p*-Si device layer SOI wafer, (b) and (c) source and drain windows mask, (d) phosphorus diffusion, (e) highly doped *n*-type source and drain junction, (f) gate oxide growth and subsequent contact opening mask, (g) source and drain metallization, (h) gate metallization.

4.3 Results and Discussion

4.3.1 DC Characteristics of *n*-channel SOI MOSFETs

The DC characterization of *n*-channel SOI MOS MOSFETs as shown in Figure 26 is performed using Agilent B1500 semiconductor device analyzer. *I-V* (current – voltage) measurement and *C-V* (capacitance – voltage) are measured at room temperature.
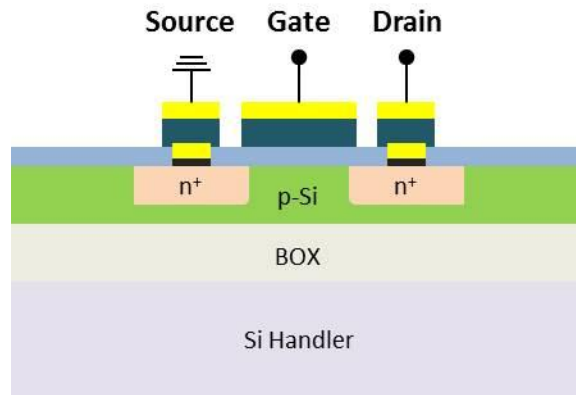
Figure 26. Schematic of the *n*-channel SOI MOSFET cross-section along the channel with typical terminal connections.

The voltages at three terminals, namely source, drain, and gate, are named as source voltage V_S, drain voltage V_D, gate voltage V_G, respectively. By applying a source-reference scheme where source voltage V_S is taken as the reference potential, applied voltages to drain and gate terminals are determined as V_{DS} (drain to source) and V_{GS} (gate to source). The substrate, namely a body terminal, was kept floating. Output characteristics of the SOI MOSFET are shown in Figure 27 for different channel lengths. When the MOSFET is in the 'ON' state, the conduction state is defined mainly by two distinguished operation modes: linear/triode mode and saturation mode. The boundary between these regions is clear in Figure 27. Drain current is expressed in a relatively simple expression as a function of drain and gate voltages.
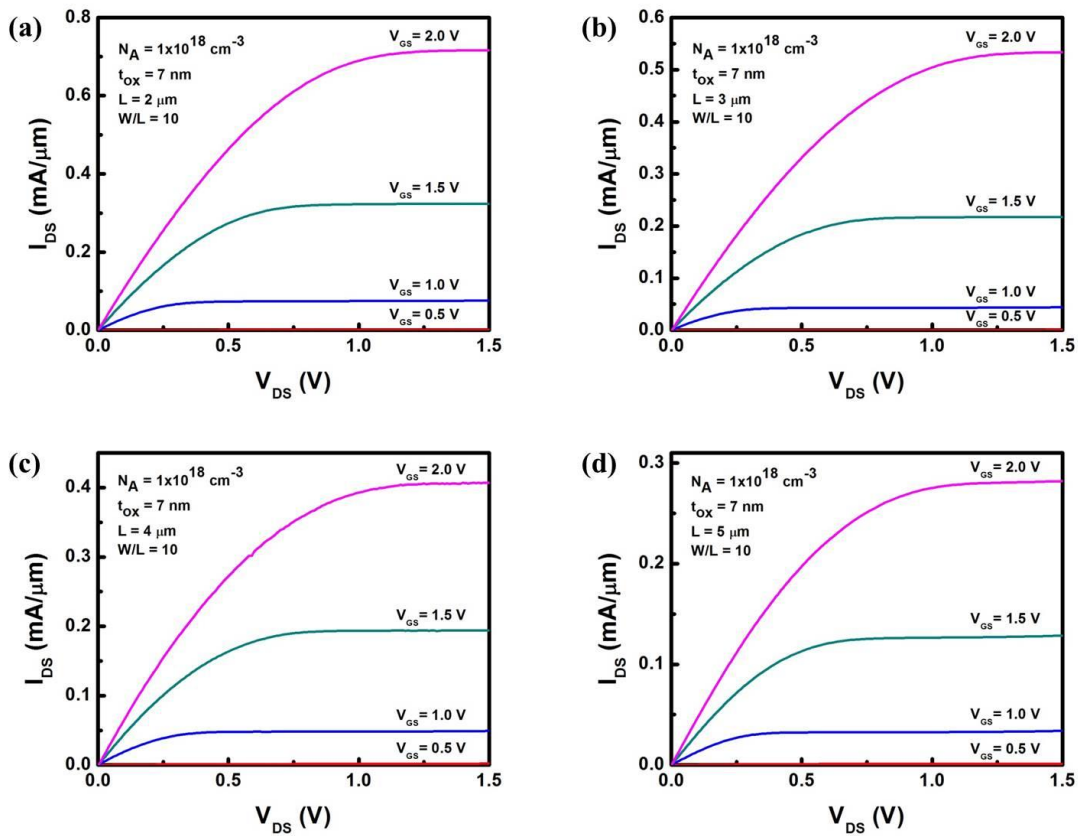
Figure 27. $I_{DS} - V_{DS}$ characteristics for *n*-channel SOI MOSFET for four different channel lengths of (a) 2 μm, (b) 3 μm, (c) 4 μm, and (d) 5 μm, respectively.

For a given V_{GS} the drain current increases linearly with small V_{DS}, and then gradually levels off with increasing V_{DS}. At small V_{DS} values, it is noticeable that drain current changes linearly with the change in the V_{GS} for gate voltages (V_{GS} = 1, 1.5, 2.0 V) larger than 0.5 V. With sufficiently high V_{DS} ($V_{DS} \geq V_{GS}$ - V_{th}), the drain current reaches the maximum saturated value (I_{Dsat}) which is independent of V_{DS} and MOSFETs operate in a saturation region. In saturation region, a couple of features are noticeable. First the saturation current depends on device channel lengths. The shorter channel length is, the higher saturation current occurs. Another important observation is that the spacing of the

I-V curves increases under different V_{GS}. This would be true that I_{Dsat} is proportional to $(V_{GS} - V_{th})^2$ which is namely a square law behavior in saturation. MOSFETs in Figure 27 are long-channel devices and the boundary between non-saturation and saturation regions are distinct.
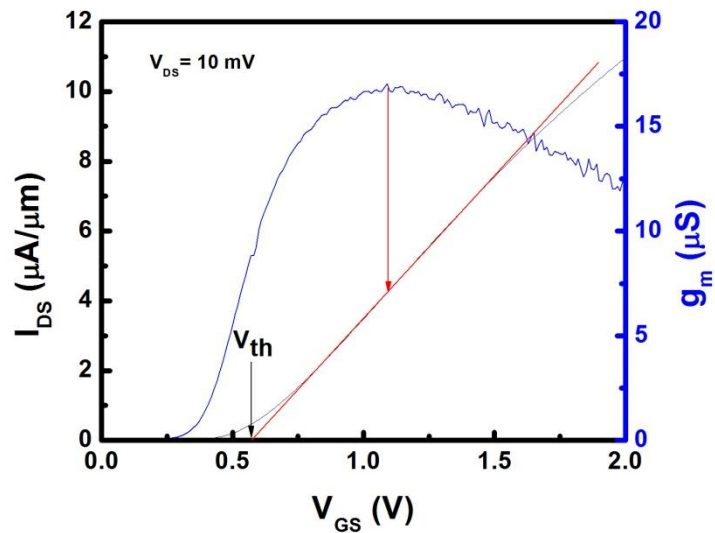
Figure 28. Threshold voltage V_{th} extraction by the linear extrapolation method from linear region transfer characteristics under $V_{DS} = 10$ mV. $I_{DS} - V_{GS}$ is represented by a black solid line and transconductance as a function of gate bias is plotted in blue solid line.

Transfer characteristics of *n*-channel SOI MOSFETs in the linear region are shown in Figure 28. The threshold voltage V_{th} is extracted from the measured transfer curve for very small V_{DS} by the linear extrapolation method. Based on the charge-sheet model, *I-V* characteristics of MOSFETs in the linear region can be expressed by Eq. (4.1)

$$I_{DS} = \mu_{eff} C_{ox} \frac{W}{L} \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{4.1}$$

by assuming the depletion region charge density upon the onset of inversion is negligible [81]. For very small V_{DS} in linear region, Eq. (4.1) is reduced as following Eq. (4.2) by keeping the first-order term of V_{DS}.

$$I_{DS} = \mu_{eff} C_{ox} \frac{W}{L} (V_{GS} - V_{th}) V_{DS} \tag{4.2}$$

Eq. (4.2) suggests that I_{DS} versus V_{GS} for a small V_{DS}, for instance $V_{DS} = 10$ mV, forms a straight line. However, at high gate voltages, I_{DS} deviates from linearity due to degradation of the effective channel mobility since transverse electric fields across the gate oxide increase and pull strongly inversion electrons toward the surface where electrons are subjected to a dominant scattering mechanism due to surface roughness.

As shown in Figure 28, a threshold voltage is determined in a way that a tangent is drawn at the inflection point where V_{GS} corresponds to the maximum output transconductance defined by Eq. (4.3) and then the intercept of the tangent at the horizontal V_{GS} axis is found. It is worth noting that the extrapolated threshold voltage is not to be misinterpreted as the threshold voltage defined by Eq. (4.4). In general, the extrapolated threshold voltage is slightly higher than the threshold voltage calculated from Eq. (4.4) at which the MOS structure enters into strong inversion.

$$g_m = \left(\frac{\partial I_{DS}}{\partial V_{GS}}\right)_{V_{DS}=constant} \tag{4.3}$$

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{4\epsilon_{Si}qN_A\phi_F}}{C_{ox}} \tag{4.4}$$

In order to evaluate variation of V_{th} and subthreshold characteristics for various channel lengths, linear region transfer characteristics $I_{DS} - V_{GS}$ are plotted on linear and logarithmic scales in Figure 29, respectively. Approximate threshold voltages of devices with different channel lengths are determined using the method described in Figure 28 and are around 0.6 V. Subthreshold conduction below the threshold is shown in Figure 29 for each device in a black solid line. In contrast to transfer curves on a linear scale in which the drain current drops to zero as soon as V_{GS} decreases below the threshold voltage V_{th}, subthreshold characteristics clearly show drain current conduction in this region. The curve is nearly straight line as I_{DS} exponentially depends on the gate bias V_{GS}. The origin of the drain conduction and exponential behaviors in subthreshold region can be explained in terms of electron density in a week inversion. The density of electrons enter the channel from the source is related to the surface potential at the source end of the channel and is exponentially proportional to the potential change. Since the surface potential varies nearly linearly with V_{GS} in a weak inversion, the population of electrons entering the channel relies on V_{GS} exponentially. In turn drain current I_{DS} changes exponentially to the V_{GS} changes.
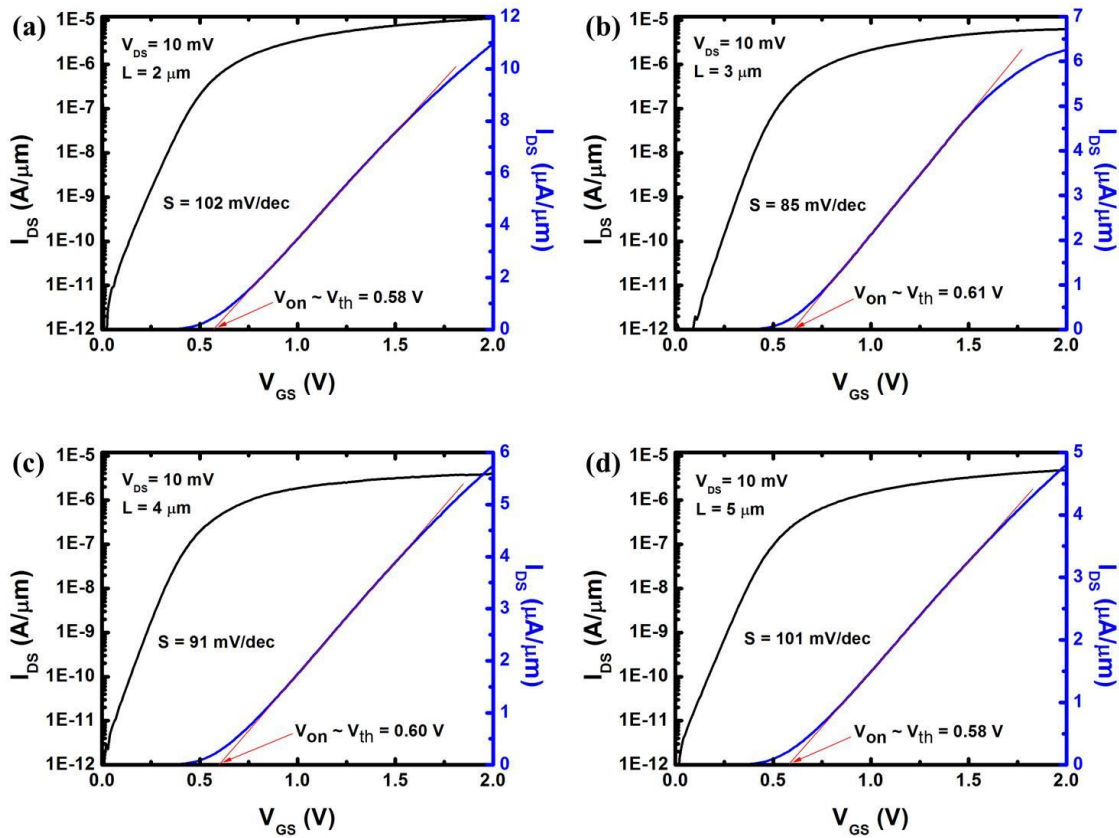
Figure 29. Transfer characteristics $I_{DS} - V_{GS}$ for n-channel SOI MOSFET on both logarithmic and linear scales with $L = 2$ (a), 3 (b), 4 (c), and 5 µm (d) in the linear region ($V_{DS} = 10$ mV $\ll V_{GS}$). A V_{GS} -intercept of the extrapolation of linear portion of the plot indicates the threshold voltage V_{th} of each device.

As a result, as shown in Figure 29 I_{DS} on a logarithmic scale exhibits a linear behavior in the subthreshold regime. The subthreshold swing S, a reciprocal of the slope of transfer curve, varies 85 ~ 102 mV/decade which is higher than 70 mV/decade at room temperature. The large value of subthreshold swing is attributed partly to a higher channel doping of SOI MOSFETs ($N_A = 2.2 \times 10^{18}$ cm^{-3}) and to a high density of Si-SiO$_2$ interface states. The dependence of subthreshold swing on substrate doping concentration

can be explained from the Eq. (4.5). For a high substrate doping concentration, S increases due to the increase in depletion capacitance C_d.

$$S = \left[\frac{\partial(\log_{10} I_{DS})}{\partial V_{GS}}\right]^{-1} = \frac{kT}{q}\ln 10\left(1 + \frac{\sqrt{\epsilon_{Si}qN_A/4\phi_F}}{C_{ox}}\right) = 2.3\frac{kT}{q}\left(1 + \frac{C_d}{C_{ox}}\right) \qquad (4.5)$$

Figure 30 gives an example of influence of substrate doping concentration on subthreshold characteristics of SOI MOSFETs. Figure 30(a) shows subthreshold swings of devices built on p-Si SOI substrates with a higher channel doping, whereas (b) shows small substhreshold swings of devices on a lower channel doping.
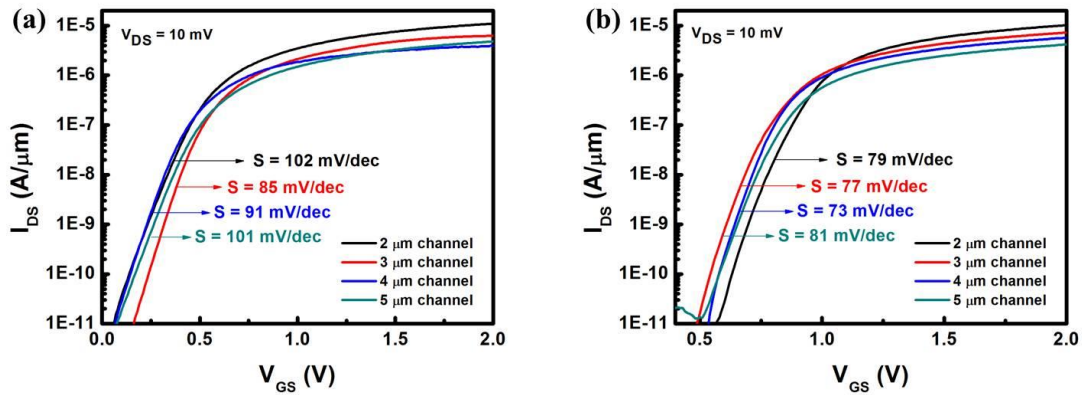
Figure 30. Subthreshold characteristics of SOI MOSFETs as a function of substrate doping concentration (a) substrate doping $N_A = 2.2 \times 10^{18}$ cm^{-3} (b) $N_A = 1.5 \times 10^{15}$ cm^{-3}.

When a high density of Si-SiO$_2$ interface trap states D_{it} ($> 5\times10^{10} \sim 10^{11}$ eV^{-1}cm^{-2}) is present, besides the depletion capacitance another capacitance plays a role in determining the subtheshold slope. This capacitance C_{it} is equal to qD_{it} and is in parallel

with the depletion capacitance C_d. Thus, in the presence of a relatively high interface trap density, a subthreshold swing is given by Eq. (4.6). Eq. (4.6) implies that a high density of interface trap states causes S to increase. In fact, the subthreshold slope can be used to evaluate the quality of Si-SiO$_2$ interface by calculating the capacitance C_{it} from the subthreshold swing equation above. It is favorable for a sharp subthreshold slope to use a low substrate doping and a high quality Si-SiO$_2$ interface with a low interface trap density, and a thin gate oxide.

$$S_{D_{it}} = 2.3 \frac{kT}{q}\left(1 + \frac{C_d + C_{it}}{C_{ox}}\right) = 2.3 \frac{kT}{q}\left(\frac{C_{ox} + C_d + C_{it}}{C_{ox}}\right) \tag{4.6}$$

The effective channel mobility μ_{eff}, one of the important MOSFET parameters, is also studied. It plays a vital role on the performance of device by affecting the carrier velocity and output driving current. In this work, the effective channel mobility is extracted by combining drain current and transconductance transfer characteristics, namely $I_{DS}/g_m^{1/2}$ characteristics that G. Ghibaudo suggested in 1988 [82]. The expression of drain current divided by the square root of the transconductance can be written like Eq. (4.7). It is clear from Eq. (4.7), (4.8) and (4.9) that for given values of W, L, C_{ox} and V_{DS} channel mobility can be determined from the slope of $I_{DS}/g_m^{1/2}$ versus V_{GS} curve as show in Figure 31.

$$\frac{I_{DS}}{g_m^{1/2}} = \left(\frac{W}{L}\mu_{eff}C_{ox}V_{DS}\right)^{1/2}(V_{GS} - V_{th}) \tag{4.7}$$

$$slope = \left(\frac{W}{L}\mu_{eff}C_{ox}V_{DS}\right)^{1/2} \qquad (4.8)$$

$$\mu_{eff} = \frac{L \times slope^2}{WC_{ox}V_{DS}}. \qquad (4.9)$$
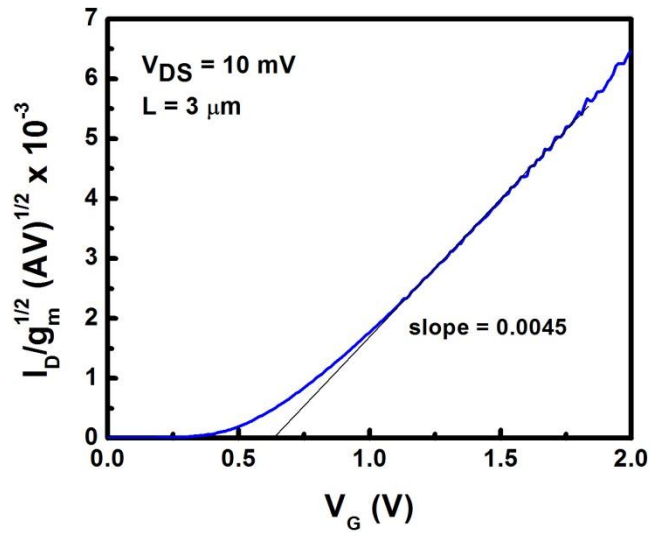
Figure 31. Characteristics of $I_{DS}/g_m^{1/2}$ versus V_{GS} for a MOSFET with a channel length of 3 μm and the illustration of effective channel mobility extraction method from a slope of the plot.

The effective channel mobility values for each device extracted using the $I_{DS}/g_m^{1/2}$ method are summarized in Table 3.

Table 3. A summary of effective channel mobility of MOSFET. μ_{eff} represents the effective channel mobility extracted using $I_{DS}/g_m^{1/2}$ characteristics method. The above parameter extraction methods are tested on *n*-channel SOI MOSFETs with a gate oxide thickness 7 nm, $W/L = 10$, $V_{DS} = 10$ mV.

Channel length [µm]	V_{th} [V]	μ_{eff} [cm²/V·s]
2	0.58	380
3	0.61	382
4	0.60	385
5	0.58	380

4.3.2 RF characteristics of *n*-channel SOI MOSFETs

For a measure of the frequency response such as the high-speed capability, the cutoff frequency f_T and the maximum oscillation frequency f_{max} are widely used. For digital circuits which speed is the primary concern, f_T is a more suitable figure of merit, whereas f_{max} is more of importance for practical and microwave analog circuit applications since it relies not only on the intrinsic transistor performance but also on transistor parasitics. The figure of merit is useful to evaluate and compare different transistor technologies and also for development of guidelines for transistor design. It is preferable to have a figure of merit that depends only on the transistor itself.

The figure of merit evaluated in this work is defined as the unity current gain cutoff frequency, designated f_T. The circuit configuration is described in Figure 32 where the MOSFET is driven by a small-signal current source, input current into the gate due to gate capacitance, and short circuit drain current is taken as the output. MOSFET is assumed to be biased so as to operate in a saturation regime. So the current gain of the intrinsic MOSFET specified in datasheets is the change in the short circuit drain current gain divided by the change in the small-signal input gate current.
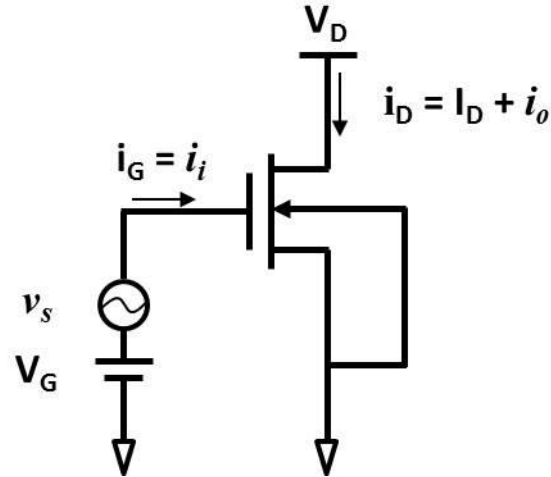
Figure 32. Circuit configuration for the calculation of short circuit current gain.

The current gain can be obtained by analyzing a small-signal equivalent circuit in Figure 33. By applying Kirchhoff's Current Law at nodes 1 and 2, small signal input i_i and output i_o are expressed as following, respectively

$$i_i = v_{gs}j\omega(C_{gs} + C_{gd}) \tag{4.10}$$

$$i_o = v_{gs}(g_m - j\omega C_{gd}). \tag{4.11}$$

Thus, the short-circuit current gain h_{21} is given by

$$h_{21} = \frac{i_o}{i_i} = \frac{g_m - j\omega C_{gd}}{j\omega(C_{gs} + C_{gd})}. \tag{4.12}$$
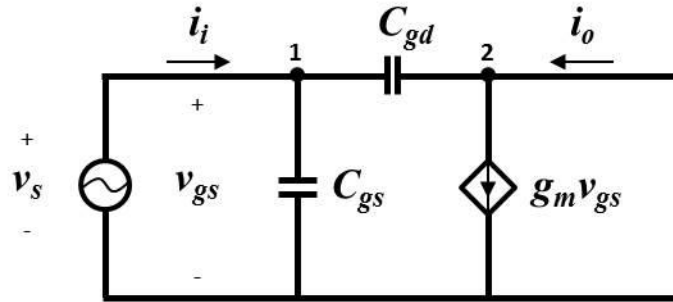
Figure 33. Small-signal equivalent circuit of *n*-channel MOSFET for calculation of f_T.

One can find a frequency ω_T such that the magnitude of h_{21} equals 1. The magnitude of h_{21} is given in equation (4.13)

$$|h_{21}| = \frac{\sqrt{g_m^2 + \omega^2 C_{gd}^2}}{\omega(C_{gs} + C_{gd})}. \tag{4.13}$$

The final solution can be obtained by taking into account both low frequencies and high frequencies, respectively

$$|h_{21}| \cong \frac{g_m}{\omega(C_{gs} + C_{gd})}, \omega \ll \frac{g_m}{C_{gd}} \tag{4.14}$$

$$|h_{21}| \cong \frac{C_{gd}}{C_{gs} + C_{gd}} < 1, \omega \gg \frac{g_m}{C_{gd}}. \tag{4.15}$$

Therefore solving equation (4.14) gives a frequency ω_T or f_T as following

$$\omega_T = 2\pi f_T = \frac{g_m}{C_{gs} + C_{gd}}. \tag{4.16}$$

Then f_T is simply given by

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}. \tag{4.17}$$

The equation (4.17) for f_T provides useful interpretation of the performance of a transistor. The transconductance of MOSFET in saturation regime can be written

$$g_m = C_{ox}\frac{W}{L}\mu_{eff}(V_{GS} - V_{th}) \tag{4.18}$$

where, C_{ox} is gate oxide capacitance [F/cm^2], μ_{eff} is the effective channel mobility, W is a channel width, L is channel length, and V_{th} is the threshold voltage. And the gate to source capacitance C_{gs} is related to

$$C_{gs} = \frac{2}{3}C_{ox}WL. \tag{4.19}$$

Another capacitance component, gate to drain overlap capacitance C_{gd}, in equation (4.17) is considered to be negligible in saturation region compared to C_{gs}, so C_{gd} term can be

ignored. By plugging these two device physics parameters in equation (4.18) and (4.19) into equation (4.17), the cutoff frequency f_T is equal to

$$f_T = \frac{3\mu_{eff}(V_{GS} - V_{th})}{4\pi L^2}. \tag{4.20}$$

This expression is translated into that the intrinsic frequency response of MOSFETs is independent on the device geometry such as channel width and thickness of gate dielectrics. However it depends on the gate length L. As shown in equation (4.20), f_T exhibits $1/L^2$ dependence. Decreasing L leads to the decrease in the overlap capacitance C_{gs}, since the capacitance changes linearly with the channel length. In addition, shrinking the channel length increases the transconductance. Therefore, improvement of the transistor frequency response can be achieved by decreasing the device channel length, which is one of the major driving forces behind the trend toward submicron technology nodes. In fact it is well known that $1/L^2$ dependence of the cutoff frequency of conventional long-channel MOSFETs no longer applies to the short-channel transistors at submicron regime.

Another option to improve the intrinsic frequency of MOSFETs is to increase the channel mobility and $V_{GS} - V_{th}$. But increasing channel mobility is impractical since the channel mobility is determined by a channel material. Increasing $V_{GS} - V_{th}$ trades off the power dissipation which defeats an endeavor to reduce power consumption for low power applications.
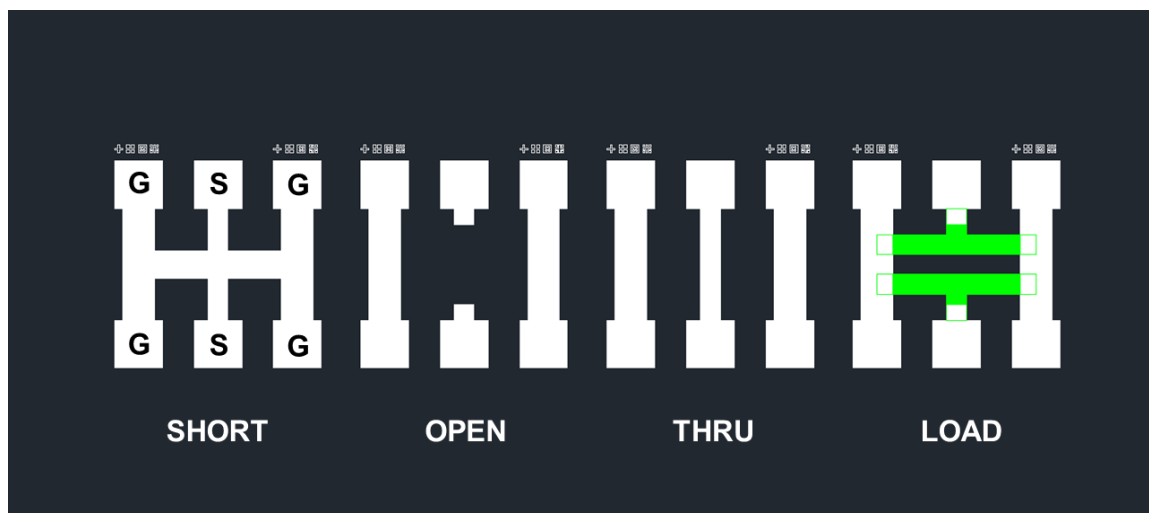
Figure 34. Layouts of on-wafer test structures of short, open, through and load for 2-port measurements and Ground-Signal-Ground (GSG) probes.

In order for the accurate on-wafer device characterization, it is imperative that a robust calibration be conducted in order to accurately deembed the parasitics from the intrinsic transistor response at high frequencies. First of all, a standard 'OPEN' deembedding method is used in this work. By using this method the metal pad capacitance is accounted for and calibrated by employing an 'OPEN' text structure which is laid out for ground-signal-ground (GSG) probes as shown in Figure 34. Additional test structures such as 'SHORT', 'THROUGH or THRU' and 'LOAD' are used to calibrate the pad as well as interconnect parasitics from the device-under-test (DUT).
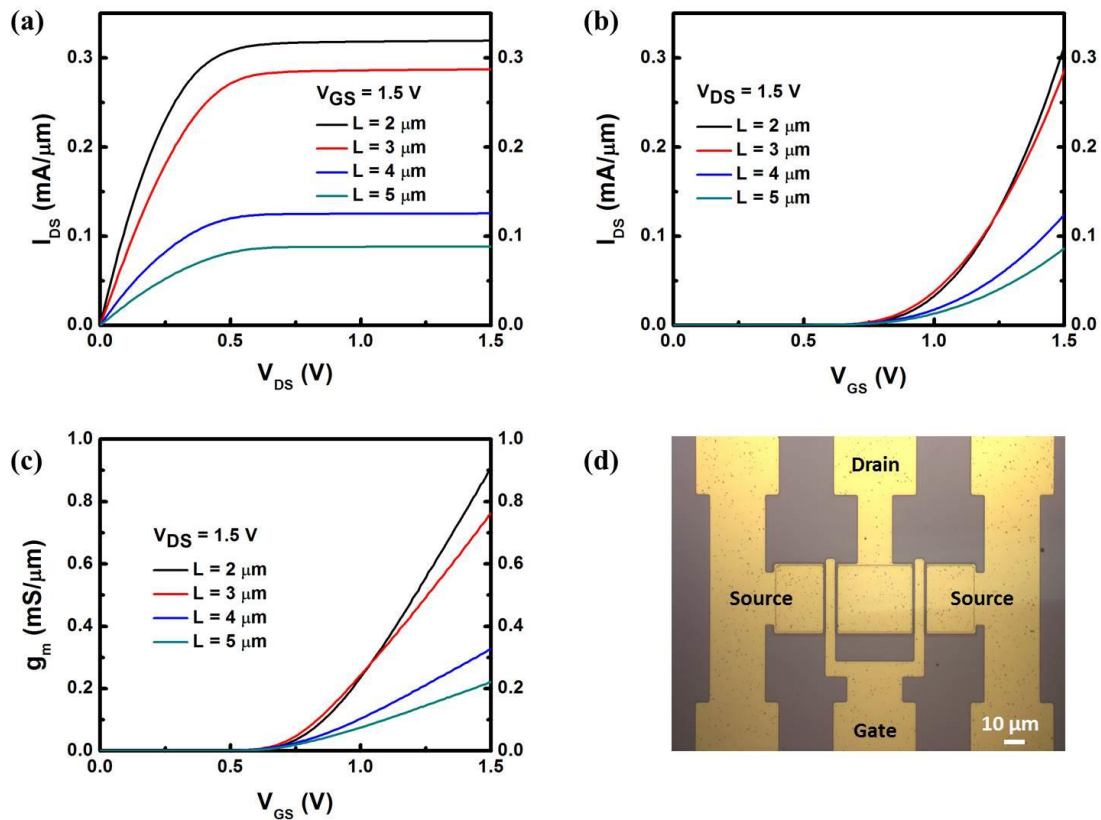
Figure 35. The *n*-channel SOI MOSFET DC characteristics with a channel length 2, 3, 4, and 5 µm, a fixed *W/L* ratio of 10, gate overlap of 1.0 µm and $C_{ox} = 5.35 \times 10^{-7}$ F/cm^2. (a) $I_{DS} - V_{DS}$ (b) $I_{DS} - V_{GS}$ in a saturation region with a $V_{DS} = 1.5$ V, (c) intrinsic transconductance versus V_{GS}, (d) an optical image of MOSFETs.

The accurately de-embedded two-port network scattering S-parameters consisting of 4 scattering coefficients are obtained to assess the frequency response of MOSFET by biasing the devices at $V_{GS} = 1.5$ V and $V_{DS} = 1.5$ V. The measured DC output characteristics and saturation transfer characteristics are included in Figure 35. It is observed that the shorter channel device gives rise to normalized higher saturation drain current and transconductance.
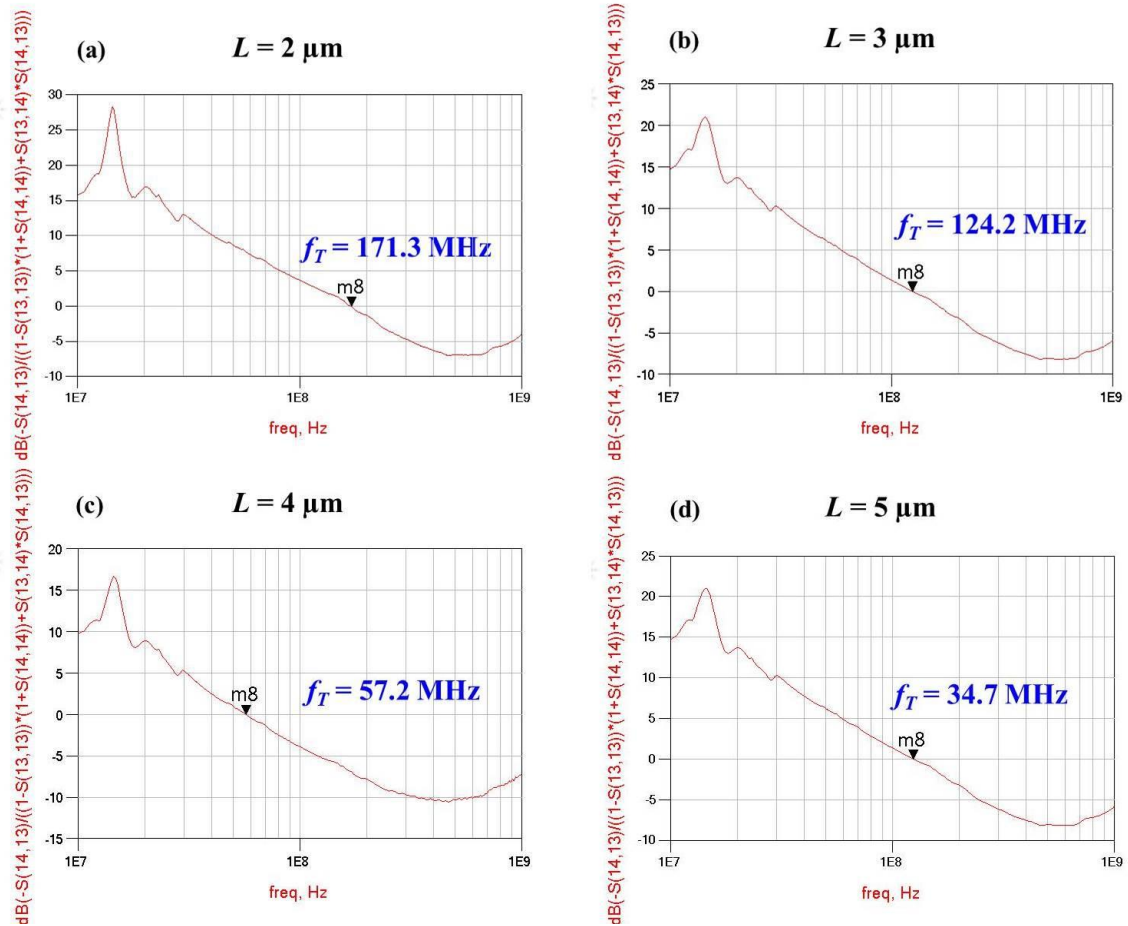
Figure 36. Short circuit current gains versus frequency determined from the full two-port S-parameter measurements on *n*-channel SOI MOSFETs with a channel lengths of 2 (a), 3 (b), 4 (c) and 5 μm (d), respectively. The channel width to length ration is 10 for all devices.

From the S-parameters the short circuit drain current gain h_{21} is obtained for devices with channel lengths of 2, 3, 4 and 5 μm as shown in Figure 36. The current gain h_{21} decays with a slope about -20 dB/decade. And as frequency increases the decay of the current gain starts to level off since the transfer function h_{21} becomes zero. It is worthwhile to note that the cutoff frequency increases as the channel length (or gate length) changes from 5 μm to 2 μm, which is predicted earlier from the equation (4.20).

Table 4. A summary of the unity current-gain cutoff frequency of *n*-channel SOI MOSFETs. f_T^* and f_T represent the calculated cutoff frequency using equation (4.17) and measured cutoff frequency, respectively.

L [μm]	W [μm]	g_m [mA/V]	f_T^* [GHz]	f_T [MHz]
2	20	1.82	2.03	171.3
3	30	2.29	1.14	124.2
4	40	1.31	0.37	57.2
5	50	1.11	0.20	34.7

The cutoff frequency of the SOI MOSFET is summarized in Table 4. The cutoff frequency extracted from S-parameters are found to be at least one order magnitude smaller than typical values of MOSET at typical bias points which range from 5 to 50 GHz. Also estimates of the upper limit of f_T (denoted as f_T^*) assuming an ideal case without the input parasitic capacitance and source and drain series resistances are still smaller than the typical values. It is probably attributed to excessive source and drain series resistances as well as parasitic capacitance.

Figure 37 proves $1/L^2$ dependence of f_T as mentioned in equation (4.20). Decreasing the channel length (or gate length) leads to decrease in the total capacitance and increase in the transconductance, thus ultimately improves f_T.
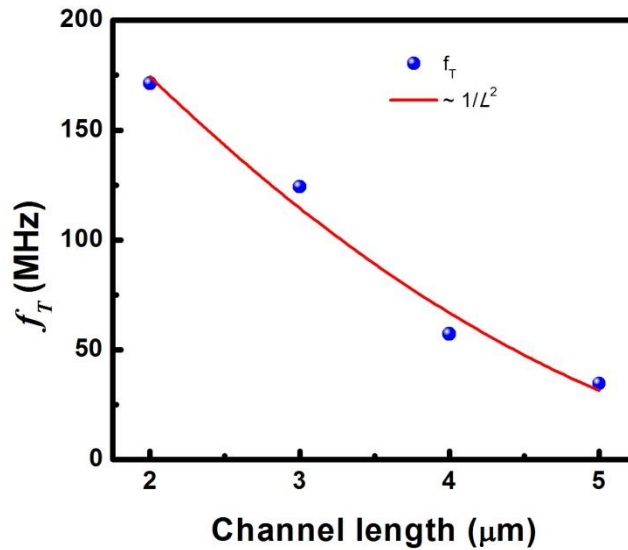
Figure 37. The unity current-gain cutoff frequency f_T for different channel lengths and its $1/L^2$ dependency.

4.4 Summary

In this work, *n*-channel SOI MOSFETs are successfully fabricated and characterized for future radio frequency applications post transfer to flexible substrates. With a background substrate doping concentration of $N_A = 2.2 \times 10^{22}$ cm^{-3}, an gate oxide thickness of $t_{ox} = 7$ nm, and a Ti (titanium) gate electrode, devices with different channel lengths exhibit an enhancement mode operation with a uniform extrapolated threshold voltage at 0.6 V. The extraction of MOSFET parameters are performed using a set of output and transfer characteristics also extracted from DC characteristics. Extracted parameters are subthreshold slope *S*, low field mobility. On top of DC characteristics, the dynamic frequency response of MOSFETs is measured using a 2-port scattering S-parameter measurement method. For a measure of the frequency response, the unity current gain cutoff frequency f_T is evaluated. The measured figure of merits falls behind

f_T of the typical MOSFET which is a range of 5 ~ 50 GHz. SOI MOSFETs show the maximum unity current gain cutoff frequency of 170 MHz.

This chapter, in part, is currently being prepared for submission for publication of the material. Namseok Park, Yun Goo Ro, Cooper Levy, Ahmed Youssef, James Buckwalter and Shadi Dayeh. The dissertation author was the primary investigator and author of this material.

CHAPTER 5: Monolithic Integration of Solar-powered Oscillators

5.1 Introduction

Ubiquitous mobile computing and a push towards the real-time sensing and monitoring of personal health and activities have created an increasing interest in wearable electronics. Flexible electronic components such as flexible displays enable wearable electronics to more seamlessly integrate into everyday life. Flexible or wearable electronics have evolved from life-saving devices such as pacemakers and hearing aids to fashion accessories such as activity tracking bands, smart watches and glasses. Flexible electronics has a long history and the development of flexible electronic components dates back to the 1960s. The flexible silicon solar cell arrays for a space power supply was developed by thinning single crystal silicon cells down to 100 μm and then assembling them on a flexible, plastic substrate [5, 6]. In the mid-1970s and early 1980s, stimulated works on thin-film solar cells brought flexible hydrogenated amorphous silicon (a-Si:H) solar cells on a flexible metal foil [4] and organic polymer substrates [83]. The development of new classes of devices and circuits made of silicon thin film transistors (TFT) had attracted much attention owing to the successful demonstration of amorphous silicon based circuits in large area active matrix liquid crystal displays (AMLCD) and photovoltaics on flexible substrates. In 1994, flexible a-Si:H TFT circuits on polyimide substrates were demonstrated by Constant et al. [7]. Fingerprint sensor arrays consisting of capacitor electrodes and polycrystalline silicon (poly-Si) TFTs were fabricated on polyimide and polyethersulphone substrates using a low temperature process below 250 °C [9]. Two basic approaches have been employed to implement flexible poly-Si or a-Si based electronics. First approach is to fabricate Si devices and

circuits directly on top of flexible substrates. This approach requires and relies on low-temperature process techniques of poly-Si and a-Si such as ink printing [10] and laser crystallization [8] processes since their compatibility with foreign polymer substrates. Second method is a transfer and bond method. In this approach, the entire device is fabricated on the original substrate such as a Si wafer and a glass substrate. After device fabrication is completed, it is transferred to a flexible substrate by using laser exfoliation [11] and sacrificial layer separation methods [82]. Recent progress in flexible and wearable Si electronics has been driven by efforts to enable high-performance Si-based circuits using crystalline Si. Flexible nanoscale FinFETs [84], high-performance flexible memory and ring oscillator circuits [85], and tunable silicon photonic circuits [86] have been successfully demonstrated on plastic substrates.

The primary technical demands placed by these flexible devices on their electronic components are low power consumption, ultra-small size and wireless connectivity. Like many other electronics devices, wearable devices are powered by using replaceable or rechargeable batteries or plugging in wires. Since batteries for wearable devices need to be ideally thin, flexible and compact in size, battery form factors are as vital as their capacity for the application. In the light of the significance of battery form factors for flexible or wearable device applications, currently used batteries such as lithium ion and coin cell types in wearable devices impose restrictions and inhibit the integration and miniaturization of devices that would allow powerful mobile computing capabilities. Therefore, managing power of the wearable device such as sensor networks without batteries is a major driving force on energy harvesting systems.

Recent advancement in semiconductor materials and process technology and transducer technology has rendered energy harvesting from ambient energy sources practical. Enough energy can be captured to power sensor networks and other wearable devices from mechanical strain [12], sun light [87] and human body heat [88]. Thus the novel approach to power wearable devices using energy harvesting technology is a promising and desirable solution in that the operation of device can reduce dependency on battery power and possibly harvested energy may be sufficient enough to remove batteries.

In this work, photovoltaic energy harvesting is suggested as an energy harvesting system to provide power to silicon MOSFET circuits. This study also aims to demonstrate the monolithic system integration process in which energy harvesting silicon micro-wire solar cells and silicon MOSFET circuits are seamlessly integrated on a chip by taking full advantage of the mature silicon integration process technology. Lastly, an established wafer thinning technique and post-process device layer transfer methods are employed to create the solar-powered wearable electronics.

5.2 Experimental Details

Silicon micro-wire solar cells are fabricated on p-type SOI wafers (N_A = 2.2 $\times$ 10^{18} cm^{-3}) by silicon deep reactive-ion etching (DRIE) using fluorine-based gases such as C_4F_8 and SF_6 which is a highly anisotropic etch process. The etch process starts with an SOI wafer with 10 μm thick p-type silicon device layer and etching continues until the wire heights reach about 9.5 μm, namely remaining silicon layer thickness reaches about 500 nm which serves as a substrate for n-channel SOI MOSFETs. Arrays of circular

silicon micro-wires are prepared with well-controlled smooth surface, diameter, length, and density. In addition, DRIE step results in the best possible surface finish and micro-roughness of the wafer surface on the order of less than a few nanometers. To form radial *pn* junction, phosphorus SOD (spin-on-dopant) diffusion method is used and in parallel source and drain junctions are formed during the same step. Subsequent gate oxide growth is carried out using dry O_2 oxidation at 850 °C. The grown ultra-thin SiO_2 oxide provides the passivation layer for silicon micro wires. Al (Aluminum) metal electrode for a *p*-region ohmic contact and Ti/Au (Titanium/Gold) metal electrode for an *n*-region ohmic contact are deposited by electron-beam evaporation, respectively.
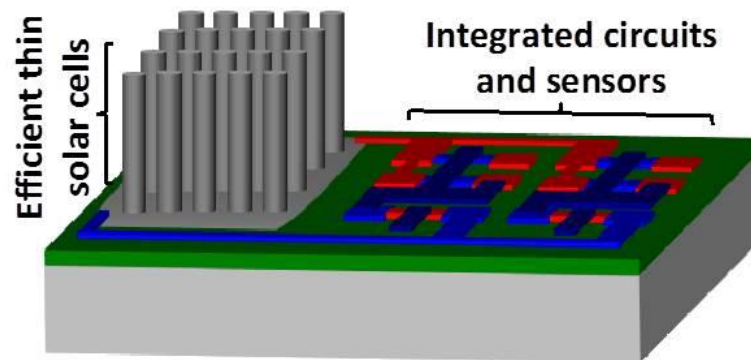
Figure 38. Schematic of hybrid integration of vertical silicon micro-wire solar cell arrays and MOSFET on SOI wafer.

Due to the three-dimensional structures of the hybrid circuit system illustrated in Figure 38, a careful optimization of photolithography process parameters is required to register patterns accurately in order not to cause a significant loss of photolithography resolution. Since both fabrication processes for silicon micro-wire solar cells and silicon

MOSFET circuits are compatible with mature silicon integration process, the unique system scale integration is demonstrated.

5.3 Results and Discussion

Contact and proximity exposure are methods where light patterns are formed in the near filed of the photomask and the patterns which can be described as Fresnel diffraction. The achievable minimum feature size of the Fresnel diffraction pattern is proportional to $\sqrt{\lambda d}$, where λ is the wavelength of the mask aligner light source, d is the proximity gap equal to the sum of the separation distance between photomask and photoresist surface and the thickness of photoresist. While the photomask is mechanically contacted to the photoresist in a contact exposure mode, in a proximity exposure mode a small gap typically 10 ~ 20 μm is introduced between the photomask and the photoresist surface in order to avoid contamination and damages on the surface of photoresist and also on the photomask patterns. However, this gap reduces the usable depth of focus and thus limits the achievable resolution. This implies that a sacrifice of photolithography resolution is inevitable for photolithography process by the presence of high topology structures or three-dimensional circuit structures etched into the wafer or protruding from the wafer. Furthermore, vertical surfaces on the sides of silicon micro-wires can also reflect light into adjacent regions that are protected from the exposure.

In our proximity exposure lithography step, the separation between the photomask and photoresist surface is determined by the height of silicon micro-wires which is 9.5 μm. Mask aligner UV light source wavelength is given i-line 365 nm and thickness of photoresist is 1.2 μm. Thus the resolution limit of the proximity exposure lithography

becomes approximately 2.0 µm which is about 3 times more resolution loss than the contact printing method.

Proximity exposure lithography process is studied to optimize exposure conditions for the best imaging result. The registered patterns are shown in Figure 39. The mask layer of 3 µm channel length source and drain windows is tested. The exposure results show the relationship between achievable line spacing and exposure photon energy doses. Figure 39(a) gives the best result which is a nearly perfect replica of the chrome metal mask patterns for source and drain windows. And as the exposure photon energy doses increase, the minimum feature size increases due to diffractive image blurring at the edge of mask patterns. Even finer imaging results from the proximity exposure lithography are shown in Figure 39(d) and (e) which are top gate electrode and source/drain contact pad openings with a minimum line spacing of 2 µm.
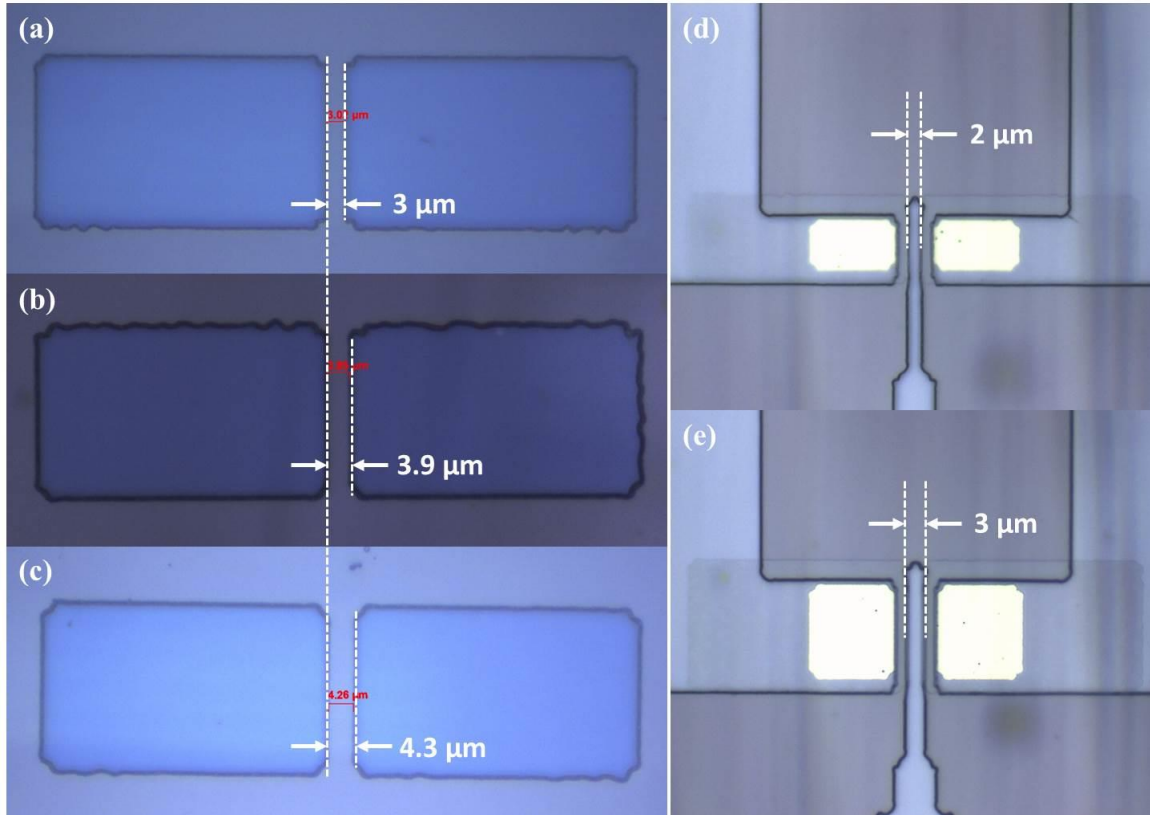
Figure 39. Proximity exposure lithography results. (a) – (c) 3 µm channel source/drain windows openings with UV exposure doses (a) 66 mJ/cm^2, (b) 88 mJ/cm^2 and (c) 121 mJ/cm^2, respectively. (d) and (e) describe top gate electrode and source/drain contact openings of 2 µm channel and 3 µm channel.

Silicon micro-wire solar cell arrays are shown is Figure 44. 1 mm × 1mm size cell consists of 9.5 µm long vertical silicon micro-wires with precisely controlled wire surface and a uniform diameter. The performance of silicon micro-wire solar cell is measured under the illumination of xenon AM 1.5G simulated sunlight with an intensity of 100 mW/cm^2. The silicon micro-wire solar-cells exhibit short circuit current J_{SC} = 21.7 mA/cm^2, open circuit voltage V_{OC} = 0.58 V, fill factor FF = 0.82, energy conversion efficiency η = 10.5 % under 1.5G irradiation of 100 mW/cm^2 as shown in Figure 40(c).

The micro-wire array solar-cell produces the maximum power of 104 µW/mm^2 under illumination.
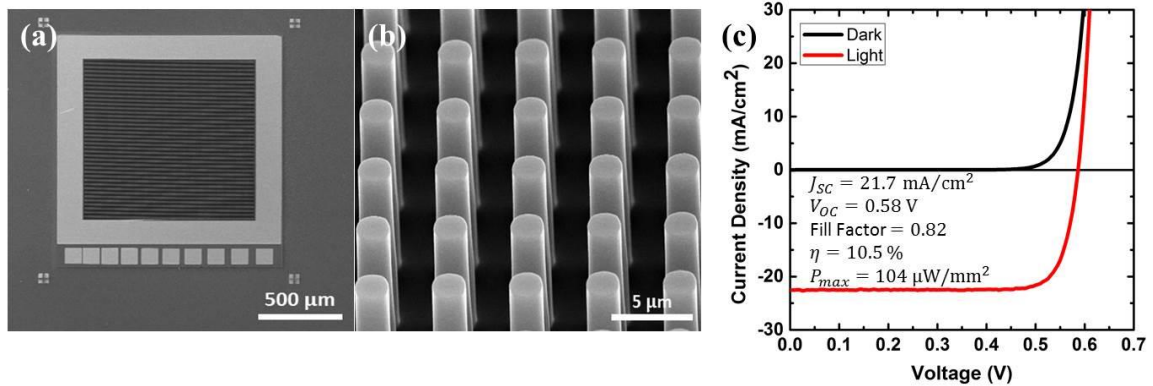
Figure 40. SEM images of silicon micro-wire solar-cells (a) 9.5 um long vertical silicon micro-wire arrays (b) higher magnification SEM image (c) *I-V* characteristics measured under air mass 1.5 global irradiation of 100 mW/cm^2. Courtesy of Yun Goo Ro, unpublished materials.

The cross sectional SEM images and top-view optical image of *n*-channel MOSFET fabricated on a 3D topography SOI wafer are shown in Figure 41. In order to imitate the 3D structure of hybrid integrated system and do proximity exposure lithography, 9.5 µm deep etched pits are formed and then MOSFETs are fabricated at the bottom of the pit as shown in Figure 41(a). The inset of Figure 41(a) describes step heights of the etched pit and its vertical wall. The optical image of final device of 2 µm channel MOSFET is shown in Figure 41(b).
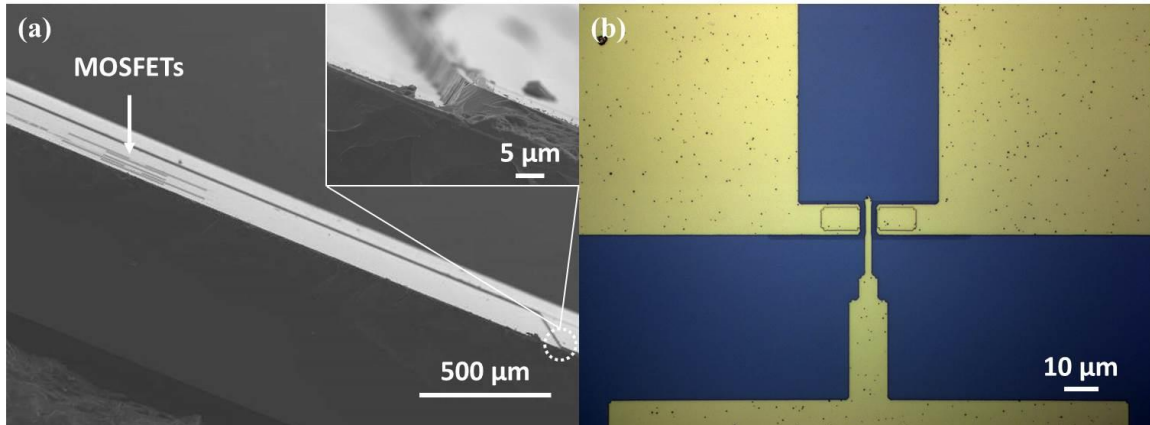
Figure 41. (a) Cross-sectional view SEM images of SOI MOSFETs fabricated using the proximity exposure lithography method and an inset which is a zoom-in image of 9.5 µm step height etched pit. (b) Top-view optical image of 2 µm channel MOSFET shown in (a).

The drain current output curves exhibit a nearly ideal behavior shown in Figure 42 for channel length of devices from 2 µm to 5 µm. Device operation at 'on state' is clearly defined by current saturation and non-saturation regions. The output characteristics appear to be similar to those of fabricated on a planar SOI wafers with the same substrate doping and the same device geometries. It is worthwhile to note that current densities of device shown in Figure 42 decrease for all the channels compared to their counterparts fabricated on a planar substrate and using a contact mode photolithography. For example, the saturation current density at a bias condition $V_{DS} = 2.0$ V and $V_{GS} = 2.0$ V of devices with different channel lengths decreases about 50 % compared to devices fabricated by contact printing exposure on a planar SOI substrate. Thus the decrease of the current density is, in part, attributed to the loss of photolithography resolution.
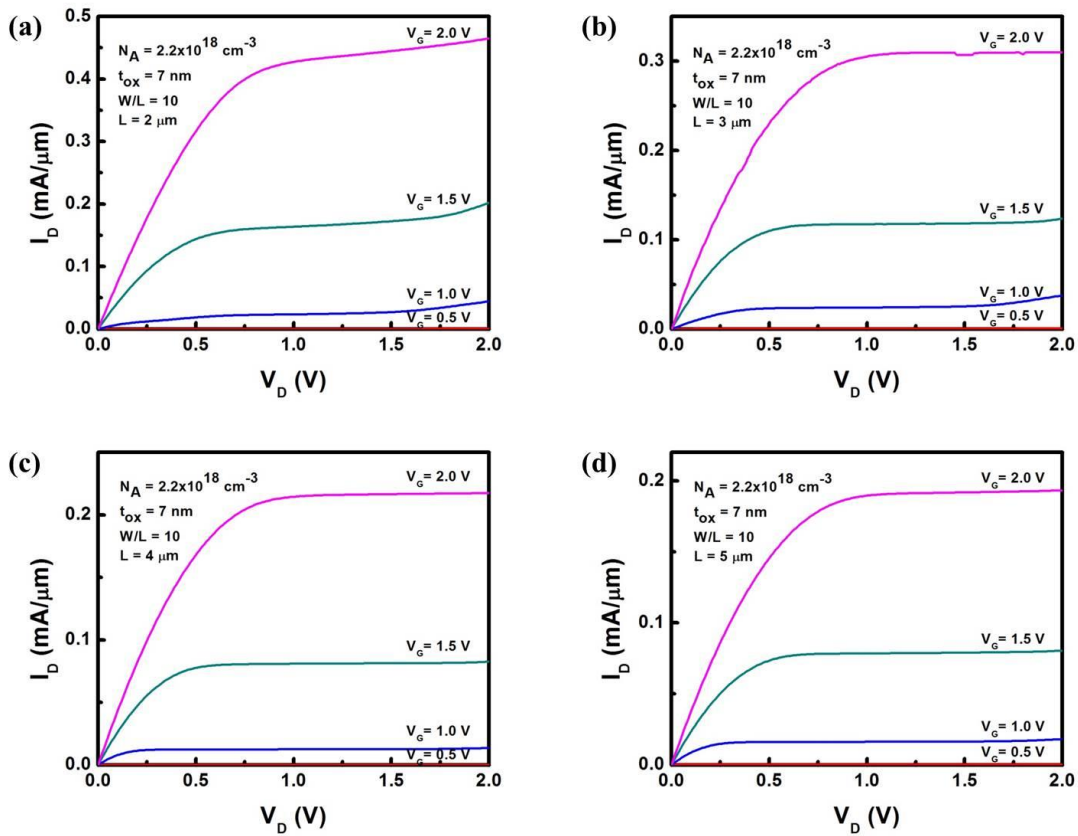
Figure 42. $I_{DS} - V_{DS}$ drain current output characteristics for *n*-channel SOI MOSFET for four different channel lengths of (a) 2 μm, (b) 3 μm, (c) 4 μm, and (d) 5 μm fabricated on a high topography structured SOI wafer.

Typical subthreshold transfer characteristics are obtained for *n*-channel SOI MOSFETs as shown in Figure 43. Also extrapolated threshold voltages are extracted for each channel device. Extracted threshold voltages vary from 0.66 V to 0.79 V, which indicate an increase in threshold voltages as much as 0.2 V compared to those on a planar SOI substrate. From the substhreshold characteristics, furthermore, the gate potential capability in modulating output drain currents is seen degraded as the substreshold slope becomes less sharp. It is observed that the device characteristics are sensitive to the lithography process variations in this proximity exposure lithography. Significant

changes of the driving ability, threshold voltage, and subthreshold swing are attributed to possible loss of lithographic resolution and misalignment. The loss of resolution leads to a larger channel length than an actual mask dimension and thus results in a degrading output driving current. The increase in threshold voltage can be explained in terms of misalignment direction to a drain side. Key device parameter changes due to lithography process variation are summarized in Table 5.
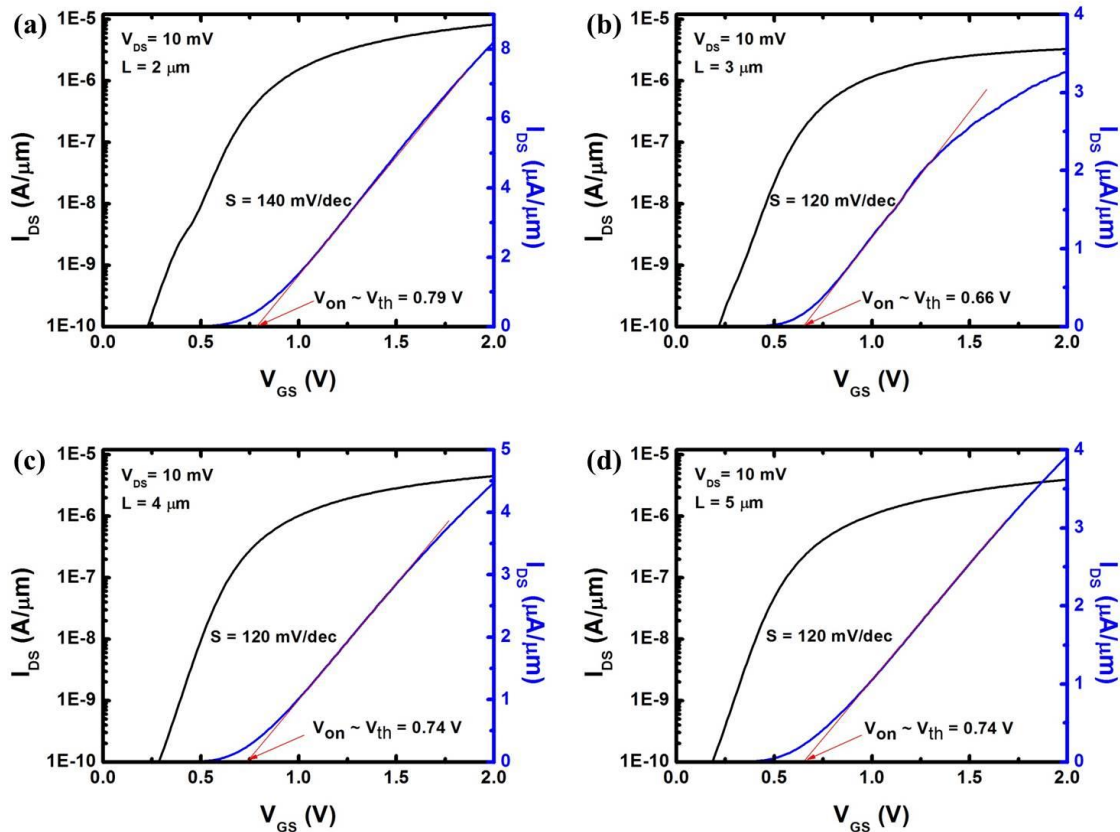
Figure 43. Subthreshold transfer characteristics $I_{DS} - V_{GS}$ for n-channel SOI MOSFET with L = 2 (a), 3 (b), 4 (c), and 5 µm (d) in the linear region (V_{DS} = 10 mV $\ll V_{GS}$). A V_{GS}-intercept of the extrapolation of linear portion of the plot indicates the threshold voltage V_{th} of each device.

Table 5. A summary of the device characteristics for MOSFET devices fabricated using a proximity exposure lithography method and comparison to devices fabricated using contact exposure lithography.

L [μm]	V_{th} [V]	S [mV/dec]	μ_{eff} [cm^2/V·s]	I_{on}/I_{off} ($\times 10^5$)
2	0.79 (0.58)	140 (102)	226 (289)	1.2 (4)
3	0.66 (0.61)	120 (85)	240 (291)	1.3 (4.8)
4	0.74 (0.60)	120 (91)	284 (310)	1.3 (7.3)
5	0.74 (0.58)	120 (101)	296 (303)	1 (3.4)

In order to implement a seamlessly integrated wearable device, post-process wafer thinning is employed. First the whole device structure fabricated on an SOI wafer is covered by a conformal coating of polyimide (PI) precursors followed by thermal curing to protect the PI layer from subsequent harsh process steps. Post-process wafer thinning involves a subtractive Si DRIE process to remove the unprotected 500 μm thick handler silicon substrate from the SOI wafer. After Si DRIE wafer thinning step, as thin as 10 μm device layer is produced and it is attached to an adhesive substrate for easy handling and mechanical support. The etched side is then also coated with another PI layer so that an ultra-thin active Si device layer is placed near the neutral mechanical plane as shown in Figure 44 where no mechanical strain exists. The embedded Si circuits show good mechanical flexibility after it lies on the neutral mechanical plane [89]. PI is chosen as an encapsulation layer of the device due to its high glass transition temperature, relatively small coefficient of thermal expansion (CTE), high elastic modulus, good chemical stability against process chemicals and acceptable optical transparency.
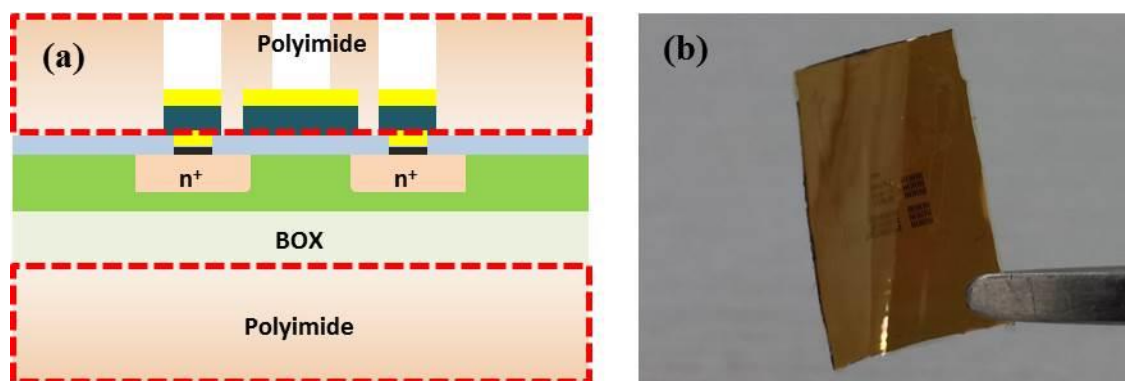
Figure 44. Flexible Si MOSFETs embedded in PI encapsulation layers. (a) A schematic diagram of Si MOSFET after transferred onto PI layers (b) Optical image of flexible Si MOSFET arrays.

5.4 Summary

The integration of energy harvesting solar cells along with Si MOSFET circuits on the same flexible die is of great interest in this work. The process integration for wearable solar-powered MOSFET circuits is developed by fabricating *n*-channel MOSFETs on thinned Si samples using Si micro-wire solar cell fabrication conditions. In order to overcome process challenges arising due to three dimensional structures, proximity exposure lithography process is employed and obtained acceptable imaging results. Complementary Metal-Oxide Semiconductor (CMOS)-compatible manufacturing technique of Si micro-wire solar cells offers a possible solution for the seamless integration of energy harvesting solar cells with Si MOSFET circuits on the same die. Post-process wafer thinning techniques are employed to realize ultra-thin Si based circuits. The resulting ultra-thin Si circuits are embedded in a neutral mechanical plane with polyimide. This polymeric dielectric layer not only protects integrated Si circuits against harsh environments, but also offers superior mechanical flexibility and stability to the circuits. The combination of energy harvesting solar cells and Si circuits in the

CMOS-compatible process provides a system-scale integration solution of self-powered wearable electronics.

This chapter, in part, is currently being prepared for submission for publication of the material. Namseok Park, Yun Goo Ro, Cooper Levy, Ahmed Youssef, James Buckwalter and Shadi Dayeh. The dissertation author was the primary investigator and author of this material.

CHAPTER 6: Conclusion

6.1 Thesis Summary

Due to their unique degrees of freedom in mechanical flexibility as well as rich features including novel functionality, wearable electronics started to attract a lot of attention. And it rapidly finds a wide range of potential markets for personal healthcare medical devices, consumer electronic products, and military purposes since the devices work simultaneously with human actions and are connected to smart applications in a network. In an effort to meet steadily increasing needs for wearable electronics, wearable devices are changing their form radically and many types of new materials and designs for them are in development.

This work has sought to develop a novel approach to integrate electronic devices into a flexible, bendable and wearable substrate. Much of this work is focused on not only the unprecedented design for a thin, flexible, conformal, and form-fitting high-performance silicon MOSFET circuits, but also an efficient power management solution to solve challenges imposed by the conventional battery. In addition, functional materials synthesis and optoelectronic device applications are covered for the potential sensor applications in wearable electronics.

6.1.1 Functional Materials Synthesis and Optoelectronic and Green Energy Applications

The thin film heterojunction photodiode made of nickel oxide (NiO) and zinc oxide (ZnO) deposited by low cost energy-efficient sol-gel spin coating. Cost-effective, large-area deposition technique of sol-gel spin-coating method is successfully implemented to deposit metal oxide thin films exhibiting smooth and pin-hole defect free

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surface with the nanoscale surface roughness. The highly visible-transparent heterojuction photodiode with smooth junction interface gives rise to a good photoresponse and quantum efficiency under the ultra-violet (UV) light illumination. With an applied reverse bias of 5V, very impressive peak photo responsivity of 21.8 A/W and external quantum efficiency (EQE) 88% at an incident light wavelength of 310 nm are accomplished.

The NiO/ZnO UV sensitive photodetector developed in this work can lead to entirely new avenues to explore in the future studies such as solid state UV image sensors.A silicon UV image sensor has been demonstrated to develop using a standard CMOS (complementary metal-oxide semiconductor) process [90]. Due to its high UV sensitivity and compatibility with a standard CMOS process, NiO/ZnO UV photodetector can be a promising candidate for UV image sensors integrated monolithically on CMOS readout circuit.

As discussed in Chapter 3, above mentioned functional earth abundant metal oxide thin films are investigated for green, renewable energy generations. Crystalline planar p-Si photocathodes coated with metal oxides by a low-cost sol-gel spin-coating method are investigated for efficient photoelectrochemical hydrogen generation which is the most promising forms of renewable energies for the future generations. As an alternative approach to overcome obstacles of poor photoelectrochemical stability of crystalline p-Si photocathodes, the surface modifications of crystalline p-Si photocathodes with sol-gel ZnO and aluminium doped ZnO thin films and protective layer coating of NiO are suggested. Under the 100 mW/cm^2 of Air Mass 1.5 solar simulation, the surface modified p-Si electrodes generate increased photocurrents at

potentials 0.17 V vs. RHE more positive than that of a bare *p*-Si electrode. This improvement of hydrogen evolution reaction suggests that earth abundant metal oxides prepared by a simple, cost-effective method can be alternative materials to enable the low-cost production of renewable hydrogen from water and sunlight as the energy source.

6.1.2 Monolithic Integration Process of Solar-powered Oscillator Circuits

A new ultra-thin silicon MOSFET circuit fabrication and integration process for wearable solar-powered oscillator circuits is presented in Chapter 5. The monolithic integration process consists of the fabrication of silicon micro-wire array solar cells and MOSFET circuits on a chip and subsequent device transfer process including wafer thinning at a chip level and device embedding in a flexible polymer substrate for a mechanical support. This study takes advantage of a silicon integration process to achieve the monolithic integration of energy harvesting silicon micro-wire array solar cells and MOSFET circuits on single chip. This monolithic integration bears a promise for higher circuit integration density and accuracy than a hybrid assembly method. This study shows that combining SOI MOSFET integration process and silicon solar cell process is compatible by fabricating both SOI MOSFETs and silicon micro-wire array solar cells using the standard CMOS integration process.

After fabricating MOSFET devices and solar cells on SOI wafers, post-process wafer thinning by silicon DRIE and subsequent polymer layer coating follow to seamlessly transfer devices from a rigid SOI wafer to a flexible substrate. This study demonstrates a die scale process for high performance, flexible, single crystalline MOSFETs and solar cells. DC and RF characteristics of both devices are used for the

circuit modeling, simulation, and design for wearable solar-powered oscillator circuits. This work has a practical significance in that it enables silicon based flexible and conformal integrated circuits and provides an energy harvesting solution for wearable electronics.

This finding is focused on a die scale integration process which can be transferable to the wafer scale integration process. For the continuing future work, an integration process at a wafer scale for high performance, flexible, single crystalline silicon circuits is suggested.

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