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Authors
Levi, M.
Bebek, C.
Ely, R.
et al.

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Lawrence Berkeley Laboratory
UNIVERSITY OF CALIFORNIA

Physics Division

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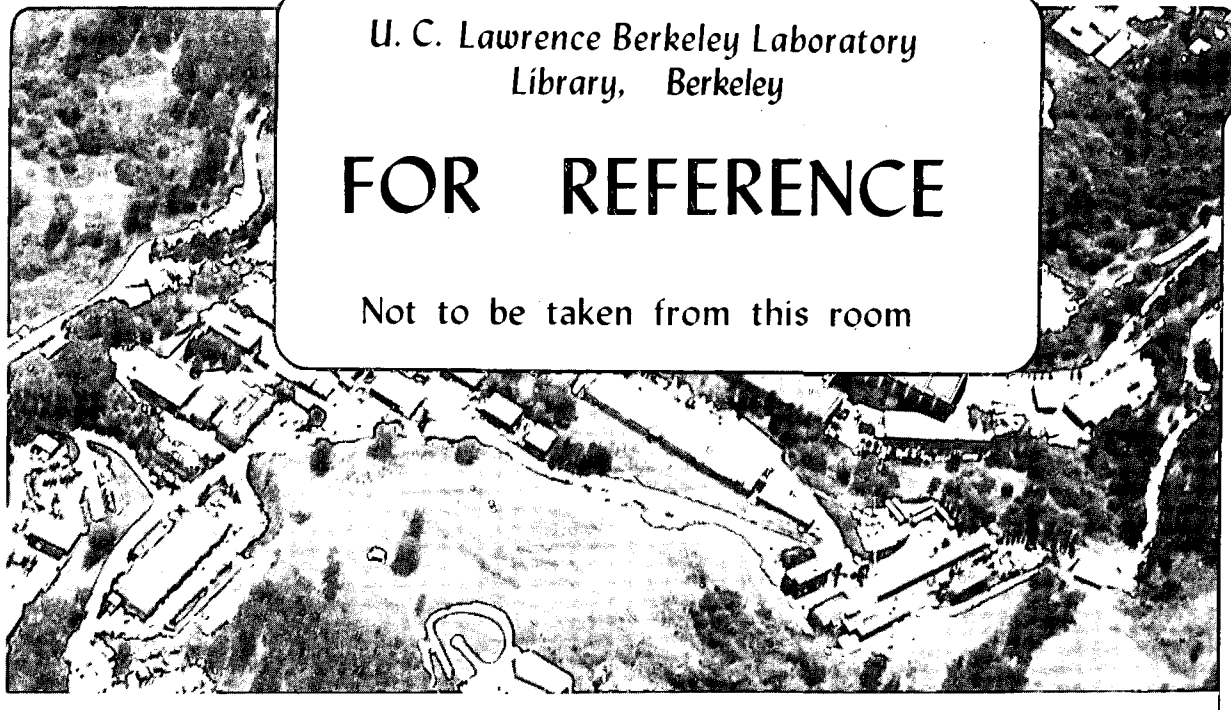

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Physics Division
Lawrence Berkeley Laboratory
University of California
Berkeley, California 94720

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A Switched Capacitor Array Based System for High-Speed Calorimetry†

M. Levi, C. Bebek, R. Ely, R. Jared, I. Kipnis,
F. Kirsten, S. Kleinfelder, T. Merrick, and O. Milgrome
Lawrence Berkeley Laboratory
1 Cyclotron Road, Berkeley, California 94720

ABSTRACT

A sixteen channel analog transient recorder with 256 cells per channel has been fabricated as an integrated circuit. The circuit uses switched capacitor array technology to achieve simultaneous read/write capability and twelve bit dynamic range. Combined with highly parallel analog-to-digital converter and readout control circuitry being developed this system should satisfy the demanding electronics requirements for calorimeter detectors at the SSC. The system design and test results are presented.

1. Introduction

We report here on the development of Integrated Circuit (IC) building blocks for an SSC calorimeter front end. We discuss the outline of the work on that part of the signal processing chain immediately following the amplification of the analog signals. It is contemplated that a single front end board will contain all the functions for event buffering, trigger sums, timing and control, calibration, and readout. This is made possible by the high level of integration achieved using custom integrated circuits that are currently in fabrication and are described in this report. This work is based on low power CMOS circuits and uses switched capacitor array technology to achieve a large dynamic range and high speed readout.

2. Calorimetry Readout and Signal Processing

Under the auspices of this project several specialized integrated circuits have been developed.[1] An integrated CMOS high dynamic range preamplifier/shaper for scintillation calorimetry has recently been fabricated. A low-power sixteen channel 12-bit ADC has been implemented on a single IC. A sophisticated control chip for managing the buffer contents during trigger decisions and readout is currently in fabrication. Most importantly, a switched capacitor array (SCA) which retains the data during trigger decision has had repeated successful fabrications. The SCA will provide for 256 memory cells per channel of electronics, allowing up to 4 μsecs of analog information to be stored at SSC crossing rates.

It is impractical (if not impossible) to move the data from every channel off the detector for every interaction. It is desirable to filter the data through multiple levels of triggering to reduce the bandwidth and digitization requirements. In the

most likely scenario, data is stored during two successive levels of triggering prior to event readout. The general task to be accomplished is the temporary storage, followed by slower readout, of brief but high speed analog transients. Acquisition with sampling frequencies up to the beam crossing rate of 62.5 MHz are needed. Usually, a trigger decision of a 2-4 μsecs latency is made to judge the value of the stored signals. These signals are then either discarded or digitized, processed, and transferred to computer systems. Thus, these systems usually require time delay via temporary storage and time stretching of the stored signal to match the bandwidth of the data processing system.

The data are sampled at 16 nsec intervals and stored in analog form. No known techniques for analog storage and fast analog-to-digital conversion can cover the large dynamic range required (16 to 18 bits). Thus at least two data storage channels per signal channel with partly overlapping scales are needed, each covering 12 bits.

The analog pipelines are controlled by a specialized integrated circuit. This chip is responsible for keeping track of the stored data during the successive levels of trigger decision. The circuit is able to manipulate stored addresses (pointers) through a series of bookkeeping lists. This circuit, the address list processor, is described in section 5.

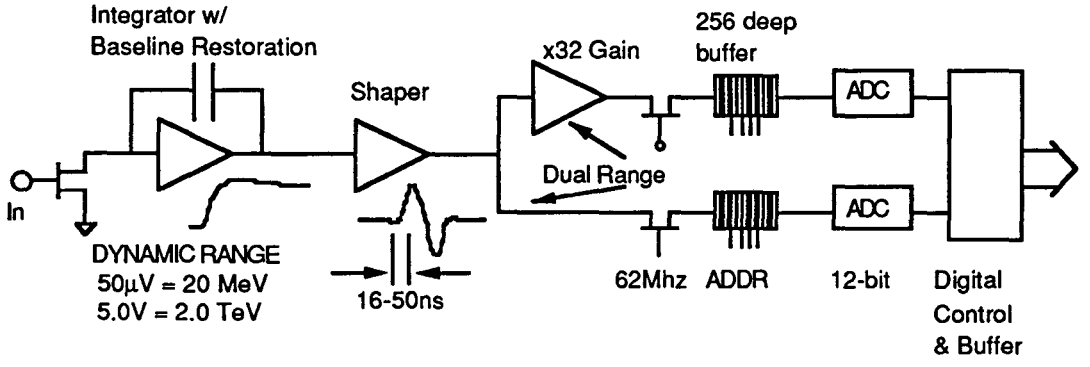

Fig. 1. Shown in the figure is a conceptual design for an SSC calorimeter front end electronics architecture. Signals are preamplified, shaped, split into high and low-range channels, and then stored during the level 1/2 trigger decision in an analog memory. After a Level 2 accept analog data are digitized and readout.

3. Switched Capacitor Array

The switched capacitor array (SCA) has 256 memory cells per channel to store up to 4 microseconds of analog information at the SSC. The number of cells be easily extended beyond 256. Two types of analog memory cells have been pursued: a single-ported, single-ended memory,[2] and a dual-ported, single-end memory with simultaneous read/write capability. Two variations of this cell, inverting and noninverting, have been pursued.[3]

The dual-ported, single-ended memory has four digital clock inputs, reset control input, and two sets of 8 address inputs. There are 16 channels on the IC. A channel consists of an input bus, 256 sample and hold cells, a readout bus, and a

reconstruction amplifier, as shown in Fig. 1. Each sample and hold cell consists of a complementary CMOS transmission gate (complementary switch) and a 0.7 pF double polysilicon capacitor. The capacitors use a high quality silicon-oxide dielectric of 70 nm thickness. An externally supplied reference voltage is applied to the bottom plate of all capacitors. The voltage stored on each sample and hold capacitor then corresponds to the difference between the input signal and the applied reference at the time its sample and hold switches are opened. During the readout sequence each sample capacitor is placed in the feedback path of the reconstruction op-amp. A device with full simultaneous read/write capability has been fabricated at ORBIT semiconductor in a 1.2 μm double-metal double-poly technology. The device is 4 mm x 6 mm.

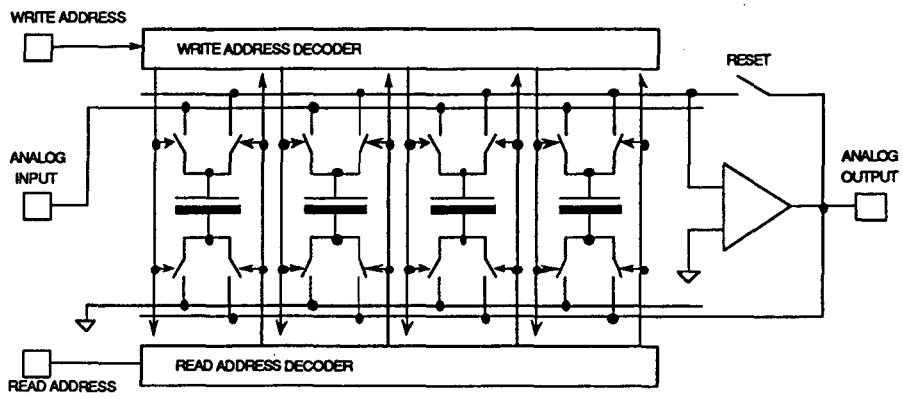

Fig. 2. A simplified block diagram of a single ended dual-ported analog memory cell structure as discussed in the text.

In order to achieve 12 bit dynamic range without correction the pedestal variation of each of the storage elements in a channel must be less than 1 mV of the 4 volt full scale voltage range. Variations in gain and offset between the various storage locations be sufficiently small that they may be ignored. Also, 8.3 time constants must fit in each 16 nsec write operation to charge the sample and hold capacitors. These are a very desirable goals for any system utilizing analog storage to avoid the need for calibration constants for each cell in the storage array. In a 1.2 μm CMOS version with 256 cells per channel with a 1.5 nsec charging time constant, the cell to cell variation at a 50 MHz acquisition rate was measured to be 0.6 mV rms. The cell to cell variation of the SCA is given by the quadrature sum of systematic noise sources (pedestal variation) and incoherent noise sources (op-amp noise, kT noise). Thus, the useable range is 0.6 mV to 6 V. This corresponds to a total dynamic range of 1:8000 or 13 bits.

The on-chip, reconstruction amplifiers developed were based on a published design in a different technology.[4] The single supply op-amp operates to within 20 mV of either voltage rail. The non-linearity of this op-amp is ± 1 mV out of 5 volts or $\pm 0.02\%$ of full scale. Currently the noise of the operational amplifier is one of the dominant incoherent noise sources in the SCA circuit. This noise can be easily

rectified by a number of methods which are under study.

The non-linearity of the overall SCA circuit is dominated by the voltage dependent parasitic capacitance of the readout switches. This is measured to be ±4 mV or ±0.01% of full scale and is shown in Fig. 3. The largest inaccuracy is 0.5% of value. The measured parameters of the SCA are summarized in Table 1.

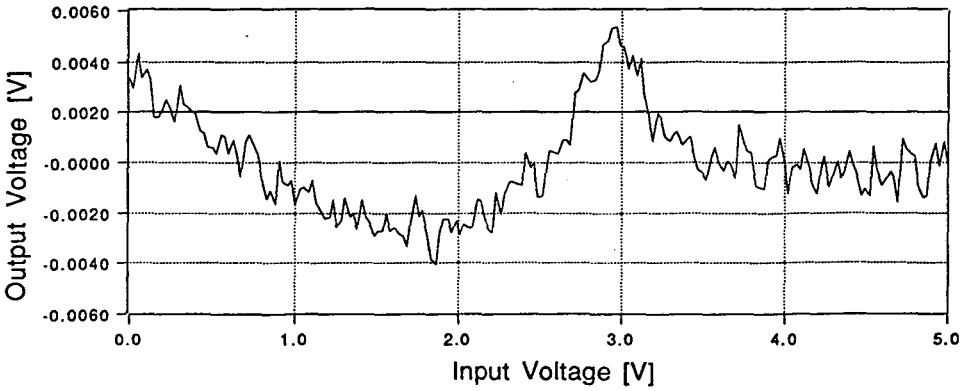

Fig. 3. Non-linearity of the 1.2 μm CMOS 256 cells per channel switched capacitor array. Shown is the deviation from a best fit line.

Analog Store Parameters	Achieved Performance
No. channels/chip	16
No. of elements/channel	256
Power consumption/channel	10 mW
Non-linearity	±0.1% (full scale) ±0.5% (value)
Cell to cell variation	0.6 mV rms
Charging time constant	1.5 ns
Channel dynamic range	8000
Maximum sample rate	90 MHz
Maximum readout rate	200 KHz
Input voltage range	0.0-6.0 Volts
Capacitor droop rate	0.1 mV/msec
Output settling time (0.02%)	1.2 µsec

Table 1. Measured performance parameters of a simultaneous read-write switched capacitor array integrated circuit. The array has been implemented in 1.2 μm CMOS, has 16 channels, and 256 storage cells per channel. Measurements were performed at a 50 MHz acquisition rate.

4. High Dynamic Range Analog to Digital Converter

A 12 bit linear analog to digital converter has been fabricated and tested in a 2 μm CMOS technology. The ADC uses a single slope conversion technique and therefore features small silicon area and low power consumption. The tested chip contains a reference voltage ramp, a comparator to detect when the input signal exceeds the reference ramp, a counter to provide a digital code versus time, and a latch to record the counter code when the comparator trips. The counter and ramp

can be shared by all digitizer channels across the chip. A complete conversion on all channels requires 4096 clock cycles. Each incremental converter requires only an additional comparator and readout latch at 300 μm pitch (180 μm in 1.2 μm CMOS). Conversion frequency is above 40 KHz for 12 bits. Conversion rate is above 160 KHz for 10 bit conversions, and the input range is within 200 mV of either supply. The integrated circuit successfully combines high speed CMOS digital frequencies in excess of 70 MHz, with analog signals smaller than 1 mV. Crosstalk and substrate coupling effects have been successfully minimized in this mixed analog and digital chip. These interactions appear as noise in the ramp and comparators. Improvements in bias filtering in the analog section and synchronization between the counter and ramp are being implemented in the next layout.

5. The Address List Processor Circuit

The Address List Processor (ALP) manages a list of all possible SCA storage location addresses, sorting them into FIFO's that identify the contents of the address as empty, pending a Level 1 trigger decision, pending a Level 2 trigger decision, or pending readout to the data acquisition system. In essence, the ALP circuit substitutes movement of digital pointers for movement of analog data. The length of each pipeline is inherently unrestricted up to some fixed maximum so that the length of each pipeline adjusts dynamically, changing as trigger conditions change.

An ALP with 256 deep FIFO's and incorporating the design choices described has been submitted for fabrication. It is a 1.2 micron CMOS device, approximately 4 mm by 3 mm, and contains 60,000 transistors.

6. References

1. C. Bebek, *et.al.*, *Front End Electronics for SSC Calorimetery Progress Report*, Aug. 16, 1991. C. Blocker, *et.al.*, *Front End Electronics Development for SSC Detectors*, UPR-208E, October 1, 1991. A. Bhattacharya, *et.al.*, *Front End Electronics Development for SSC Detectors*, October 1, 1990. A. Bhattacharya, *et.al.*, *Front End Electronics Development for SSC Detectors*, October 2, 1989.

2. G. Rai, *et.al.*, IEEE Trans. Nucl. Sci NS-37 (1990) 56.

3. S. Kleinfelder, IEEE Trans. Nucl. Sci NS-37 (1990) 1230. S. Kleinfelder, M. Levi, O. Milgrome, *Test Results of a 90 MHz Integrated Circuit Sixteen Channel Analog Pipeline For SSC Detector Calorimetry*, LBL-30222. S. Kleinfelder, M. Levi, O. Milgrome, *Toward a 62.5 MHz Analog Virtual Pipeline Integrated Data Acquisition System*, Nucl. Phys. B23A (1991) 382. O. Milgrome, S. Kleinfelder, M. Levi, *A 12 Bit Analog to Digital Converter for VLSI Applications in Nuclear Science*, submitted to IEEE.

4. J. Babanezhad, IEEE Journal of Solid State Circuits, 23 (1988) 1414.

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LAWRENCE BERKELEY LABORATORY
UNIVERSITY OF CALIFORNIA
INFORMATION RESOURCES DEPARTMENT
BERKELEY, CALIFORNIA 94720