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# ErAs island-stacking growth technique for engineering textured Schottky interfaces

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We demonstrate a molecular beam epitaxy growth technique to create intentionally textured interfaces between semimetallic ErAs and GaAs that result in interface orientations that are different from the substrate. To grow the textured interfaces, ErAs is deposited on (100) GaAs and islands form in an island growth mode. Enough GaAs is then deposited to fill the space between islands with semiconductor. More ErAs is deposited on the ErAs/GaAs surface and the new ErAs islands are thought to nucleate on the exposed top surface of the partially covered islands. The process is repeated to "stack" the islands. By quadratically increasing the amount of ErAs deposited in each repetition, the islands form into cones/pyramids that coalesce into a complete film with an intentionally roughened interface. Compared to a smooth interface between ErAs and GaAs, the Schottky barrier height between textured ErAs and *n*-GaAs can be reduced from ~0.81 to ~0.52 eV, and the Schottky barrier height between ErAs and *p*-GaAs can be increased from ~0.38 to ~0.63 eV. © *2006 American Vacuum Society.* [DOI: 10.1116/1.2203642]

## I. INTRODUCTION

Complete films of semimetallic ErAs on semiconductors and particles of ErAs within semiconductor films have been used in a wide variety of applications such as photomixers,[1] low noise Schottky diodes,[2] thermoelectrics,[3] and diffusion barriers.[4] Although this materials system has been used for many different applications, several aspects are not fully understood. Among these unexplained phenomena are particle-size effects on the Fermi level alignment observed for particles in bulk InGaAs,[1] and quantum size effects in very thin films and small particles. A better understanding of the physics of the materials system and a method for growing structures that are more complicated would be helpful for future advanced devices; we present a growth technique that may provide a method to achieve both of these goals.

ErAs is a semimetal that is thermodynamically stable on GaAs and other III-As compound semiconductors.[5] ErAs has the rocksalt crystal structure with a lattice constant of 5.7427 Å, corresponding to 1.6% compressive strain when grown on GaAs. On III-V semiconductors, ErAs grows via an island growth mode, where islands nucleate directly on the semiconductor surface without forming a wetting layer. Previous work using transmission electron microscopy has shown that these islands grow to a height of ~4 monolayers (ML) before growing laterally and coalescing into a complete film after ~4 ML of deposition.[5–7] The film then grows via a traditional layer by layer growth mode. The ErAs films are single crystal, share a continuous arsenic sublattice with the GaAs, and have low interface defect densities.[2,8] The electrical resistivity of ErAs is 60–70 $\mu\Omega\,\mathrm{cm}^2$, with electron and hole concentrations of $\sim 3.3\times 10^{20}$.[5,9,10] The semimetal-semiconductor interface behaves like a traditional Schottky diode with the Schottky barrier height (SBH) dependent on both the deposition conditions and the crystallographic orientation of the interface. Palmstrøm *et al.* investigated the orientational dependence of the SBH for $Sc_{0.32}Er_{0.68}As$:GaAs, a closely related lattice-matched system. They deposited $Sc_{0.32}Er_{0.68}As$ on *n*-GaAs between 500 and 620 °C, and found that the SBH is ~0.9 eV for the (100) interface, ~0.69 eV for the $(0\bar{1}1)$ interface, and ~0.63 eV for the $(\bar{1}\bar{1}1)$ interface. They showed that between the (100) and $(\bar{1}\bar{1}1)$ interfaces, the change in SBH is linearly proportional to the angle from the (100) direction. This linear change in SBH results because a crystallographic plane, {*h*11}, is a combination of terraces of {100} type interface and ledges of {111} type interface, as described in Ref. 11 Although it has not been studied, it is expected that the SBH for *p*-GaAs would follow the opposite trend, with the $(\bar{1}\bar{1}1)$ type interfaces having the largest SBH and (100) interfaces having the smallest SBH.

Here, we demonstrate a growth technique that allows stacking of ErAs islands to create interfaces with engineered roughness or texture. We grow a layer of islands, fill semiconductor around the islands (without overgrowing them), deposit another layer of ErAs islands which should nucleate on the top surface of the previously deposited ErAs islands to minimize interfacial energy, and repeat. By increasing the amount of ErAs and reducing the amount of GaAs deposited in each repetition, cones are formed that eventually coalesce into a complete film of ErAs. The resulting crystallographic orientation of the interface between the GaAs and ErAs is different than the (100) substrate and has characteristics of the {011} and {111} type interfaces; compared to (100) interfaces, this should reduce the SBH to *n*-GaAs and increase the SBH to *p*-GaAs.

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A previously demonstrated method of changing the SBH with interface morphology uses an anisotropic wet etch to roughen the surface of the semiconductor, followed by the deposition of metal.[12] When compared to a smooth surface, this technique shows a reduction in SBH for a dendriticlike semiconductor surface. This *ex situ* preparation technique allows an unwanted surface oxide layer to be formed, which alters the properties of the interface and results in poor ideality. Our technique is unique because it allows the roughness to be adjusted by the growth conditions, uses a single crystal epitaxial metal with a coherent interface, is not limited by available wet etches, and eliminates the possibility of oxidation of the semiconductor prior to metallization. A similar growth technique to the one described in this article has been used to stack InAs quantum dots in GaAs. The procedure is used to increase the quantum dot thickness and redshift the emission wavelength.[13]

## II. PROCEDURE

Previous growth techniques have allowed deposition of both complete films and isolated particles.[1,5,6,9] Complete films can be grown by terminating the GaAs growth, letting the interface smooth, and depositing ErAs at temperatures between 350 and 630 °C. Particles can be formed in two ways: by depositing less than 4 ML of ErAs and overgrowing with semiconductor,[6,7] or by incorporating erbium above the solubility limit, causing precipitates to form.[14] Both of these growth techniques create small islands ~4 ML in thickness. We have modified the growth procedure to produce islands that exceed 4 ML in thickness. $X$ ML (where $0<X<4$) of ErAs is deposited, then $4-X$ ML of GaAs is deposited to fill between the islands so that the total amount of material (ErAs+GaAs) deposited is 4 ML. More ErAs is then deposited; we expect that the new ErAs islands will nucleate on the top surface of the existing ErAs islands to reduce interfacial energy. The procedure is then repeated to create islands of desired dimensions.

Two similar growth technique variations were used to create the textured interfaces. First, islands were stacked in 4 ML thick repetitions as described above. The textured interfaces grown for this study can be described as a layer of inverted cones where the bases of the cones have coalesced into a complete film. In order to achieve a linear increase in the cone radius, a quadratic increase in the amount of ErAs deposited in each repetition is required. The amount of ErAs deposited in each repetition was increased quadratically from 0 to 4 ML where

$$X = 4(i/m)^2 \ [\mathrm{ML}], \tag{1}$$

where $m$ is the total number of repetitions and $i$ is the repetition number which increases from 1 for the first repetition to $m$ for the final repetition. This creates cones that eventually coalesce into a complete film (samples A–E in Table I). This method results in each repetition of the growth process totaling 4 ML in thickness; these samples are identified as $m\times4$ ML. A schematic of the cross section of the resulting structure is seen in Fig. 1(d). In the second method (samples F–P in Table I), less than a single monolayer of ErAs ($X$ ML) was deposited followed by GaAs to fill between the islands. Only enough GaAs was deposited to cover the remaining GaAs surface with 1 ML of GaAs (thus, $1-X$ ML). This results in each repetition of the growth process totaling 1 ML in thickness; these samples are identified as $m\times1$ ML. The process was repeated to stack the islands. This creates cones in the same quadratic manner as before, when the amount of ErAs deposited in each repetition ($X$) is increased from 0 to 1 ML. $X$ is described by

$$X = (i/m)^2 \ [\mathrm{ML}]. \tag{2}$$

For both growth methods, the cones will coalesce into a complete film when $i=m$. The resulting cross section of the $m\times1$ ML structures can be seen in Figs. 1(b) and 1(c). We believe that the first method may produce cones with steplike or irregular sides and the second method should create cones with smoother sides.

TABLE I. Summary of all samples presented and their SBH extracted by both the *I-V* method and the *C-V* method, where applicable. The poor ideality values observed at high currents are given in parenthesis.

| | Sample | SBH (*I-V*) | SBH (*C-V*) | Ideality |
|---|---|---|---|---|
| A | *n*-reference | 0.83 | | 1.12 |
| B | *n*-5×4 ML | 0.72 | | 1.05(1.95) |
| C | *n*-10×4 ML | 0.67 | | 1.05(4.57) |
| D | *n*-15×4 ML | 0.61 | | 1.06(4.37) |
| E | *n*-15×4 ML | 0.56 | | 1.05(5.87) |
| F | *n*-60×1 ML | 0.56 | | 1.04(5.70) |
| G | *n*-reference | 0.81 | 0.86 | 1.05(5.27) |
| H | *n*-20×1 ML | 0.65 | 0.62 | 1.03(6.16) |
| I | *n*-40×1 ML | 0.59 | 0.54 | 1.05(5.68) |
| J | *n*-60×1 | 0.56 | 0.50 | 1.08(7.87) |
| K | *n*-90×1 ML | 0.52 | 0.30 | 1.07(5.93) |
| L | *n*-120×1 ML | 0.57 | 0.25 | 3.79(14.8) |
| M | *p*-reference | 0.38 | 0.39 | 1.16(1.51) |
| N | *p*-20×1 ML | 0.53 | 0.55 | 1.13(1.63) |
| O | *p*-40×1 ML | 0.58 | 0.60 | 1.21(1.71) |
| P | *p*-60×1 ML | 0.63 | 0.63 | 1.22(1.95) |

All samples were grown in a Varian Gen II molecular beam epitaxy (MBE) system on semi-insulating GaAs substrates. For this work, growth rates of ~1 ML/s for GaAs and ~0.04 ML/s for ErAs were used. Each growth was performed at 580 or 590 °C. The GaAs was grown with an $As_2$:Ga flux ratio of 15:1, and the ErAs was grown with an $As_2$:Er flux ratio of 600:1. The layer structure consists of a 750 nm degenerately doped GaAs contact layer, a 100 or 250 nm lightly doped GaAs depletion region, the ErAs–GaAs interface grade, an additional 7.5 nm of ErAs, and a 75 nm aluminum cap to prevent oxidation of the ErAs.

Schottky diodes were fabricated using standard lift-off lithographic techniques. Ti/Pt/Au mesas were deposited to define the active diode area. The exposed aluminum and ErAs were removed with wet etches. Ohmic contact areas were defined, the degenerately doped contact layer was ex-

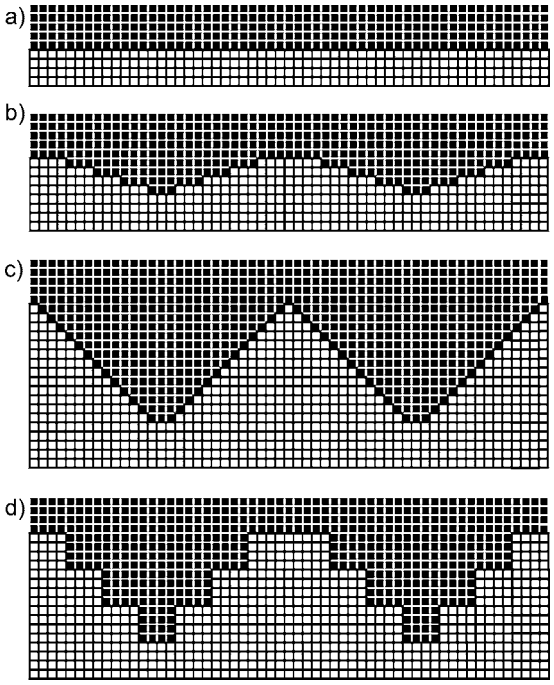


FIG. 1. This schematic diagram shows cross sections of four different interfaces, and shows how the angle of the cone, and thus the crystallographic orientation of the interfaces, changes with the number of growth repetitions. Each square in the picture represents a unit of material consisting of a single GaAs or ErAs pair of atoms. The ErAs is depicted with black squares and the GaAs with white squares. The scale of the drawings is not accurate for the growth temperatures used in this work, but is used for illustrative purposes. Four different interfaces are shown: (a) a smooth interface grown by traditional techniques, (b) an interface consisting of cones that coalesced into a complete film in $5\times1$ ML repetitions, (c) an interface consisting of cones that coalesced to a complete film in $15\times1$ ML repetitions, and (d) an interface where the cones coalesced in $4\times4$ ML repetitions. Some diffusion might occur in this sample, which might reduce the steplike nature of the interface.

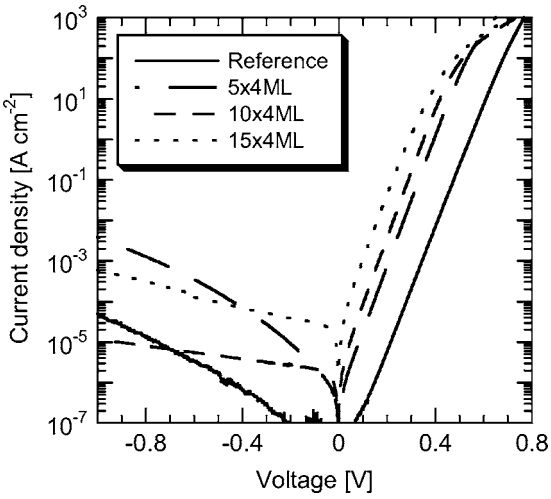


FIG. 2. *I-V* curves of samples having different cone heights are shown. The SBH is reduced for more repetitions, and the nonideal behavior at high currents can be seen in the $10\times4$ ML and $15\times4$ ML samples. Series resistance has been removed.

posed with a wet etch, and Ohmic contact metals were deposited (Ti/Pt/Au for *n*-type contacts and Pd/Ti/Pd/Au for *p*-type contacts.).

*I-V* curves were measured with a Keithley 2400 sourcemeter controlled with MATLAB code, and *C-V* data was obtained using an HP4192A LF impedance analyzer. A description of the methods used to extract SBH values using these methods can be found in Refs. 15 and 16.

## III. RESULTS AND DISCUSSION

The first set of samples was grown with repetitions 4 ML in thickness at 590 °C on *n*-GaAs. Samples B–D have 5, 10, and 15 repetitions, in addition a reference sample (sample A) was grown with a traditional planar interface. For each sample, the depletion region is a 100 nm thick layer of $1\times10^{16}$ cm$^{-3}$ Si-doped GaAs. Because the depletion width would be much greater than 100 nm for this doping level and SBH, the depletion width remains relatively constant (at $\sim$100 nm where the degenerately doped semiconductor begins) even when voltage is applied. *I-V* data are shown in Fig. 2, which shows that the diodes with deliberately roughened interfaces have an increased saturation current; this is attributed to a reduction in the SBH, as seen in Table I. One particularly interesting feature of these diodes is their ideality—the smooth, traditional Schottky diode has an ideality of $n\cong1.12$ while the roughened diodes all have idealities of $n\cong1.05$. This improvement in ideality is not fully understood but may be associated with the reduction of fringing fields near the edges. While the diodes are highly ideal at low bias, they exhibit a very defined change to poor ideality at forward biases greater than 0.4 V. This effect is not understood but is probably due to changes in the shape of the depletion region conduction band caused by the high electric fields near the tips of the cones or variations in SBH that occur at the interface.

A comparison of two different repetition lengths was performed to determine the best growth procedure. The diodes were grown at 580 °C on a 100 nm depletion region doped with $1\times10^{16}$ cm$^{-3}$ of Si. Samples were grown with 15 repetitions 4 ML in thickness (sample E) and 60 repetitions 1 ML in thickness (sample F). The SBHs of the two samples are almost identical (0.56 eV for both), but the portion of the curve showing poor ideality has been pushed to higher current levels and the leakage under reverse bias is slightly reduced for the $60\times1$ ML sample. It is also noted that there is a slight curvature in the slope of the ln(*I*)-*V* plot (i.e., the ideality changes with applied bias) for the $15\times4$ ML sample when compared to the $60\times1$ ML sample. At low current levels the $60\times1$ ML sample has a slightly better ideality and a better exponential fit with a constant ideality factor. This comparison shows that the 1 ML repetition length results in higher quality diodes. It is assumed that the improvement is a result of the $60\times1$ ML sample having cones with smoother sides.

To allow for *C-V* measurements to be performed, a third set of *n*-type diodes was grown with the depletion regions doped with $1\times10^{17}$ of Si for 250 nm. A smooth reference sample and samples with 20, 40, 60, 90, and 120 repetitions

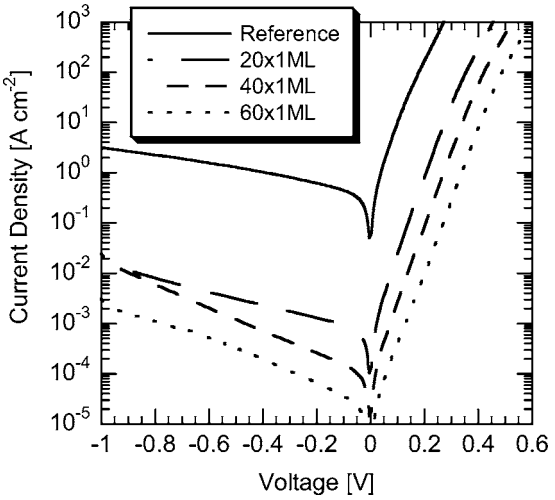


FIG. 3. *I-V* curves for the *p*-type diode samples are shown. In contrast to the *n*-type samples, roughening the interface increases the SBH. Series resistance has been removed.

were grown to see if a maximum SBH reduction could be found; the *I-V* and *C-V* extracted SBH values can be seen in Table I. It appears from the *I-V* data that the SBH is minimized in the sample with 90 repetitions (sample K), but the *C-V* data show the trend continuing to lower SBHs for the sample with 120 repetitions (sample L). The SBHs extracted from *C-V* data on samples K and L is thought to be in error, because the textured surface may be affecting the capacitive characteristics of the semimetal surface. The poor ideality factor observed at high currents is much worse in this sample set—the poor ideality begins at a lower current level. The diodes with 120 growth repetitions (sample L) show no region of the *I-V* with ideality near unity. This may be due to the nonuniformity of the electric field and associated distortions to the depletion region conduction band, combined with the fact that the depletion length changes with applied bias (it did not in samples A–F). The maximum reduction in SBH was ~0.29 eV for sample K.

The final set of diodes (samples M–P) is shown in Fig. 3. To show the effects of interface texturing on *p*-GaAs, these diodes have a 250 nm layer doped with $1\times10^{17}$ cm$^{-3}$ of Be. As expected, texturing the interface increases the SBH by up to ~0.25 eV. As seen in Table I, diodes with the same number of iterations show a similar magnitude of change in SBH, but of opposite in sign, for *p*-GaAs and *n*-GaAs.

Using a simple model for the average SBH of a round cone and the SBH variation in Ref. 11, we predict that the SBH for *n*-GaAs should decrease by a maximum of ~0.22 eV and the SBH for *p*-GaAs should increase by a maximum of ~0.22 eV for cones with a half angle of ~45°–55°.

The change in SBH by 0.25–0.29 eV is interesting because it is larger than the predicted change of 0.22 eV. This could be due to the elongation of the cones in the $[0\bar{1}1]$ direction, causing the cones to have proportionally more {111} type interface and less {110} type interface; this is probable because in previous work, islands have been observed to elongate in the $[0\bar{1}1]$ direction.[7] The effect may also be explained by a large portion of the conduction occurring through the lowest SBH regions of the interface. The 0.29 eV reduction in SBH between samples G and K is larger than the maximum reduction observed in Ref. 11, but is probably within measurement errors and growth variations.

## IV. CONCLUSIONS

We have shown that the SBH of the ErAs:GaAs junction can be changed by creating interfaces that have different crystallographic orientation than the substrate. By texturing the surface we demonstrate a decrease in SBH of up to ~0.29 eV for *n*-GaAs and an increase in SBH of up to ~0.25 eV for *p*-GaAs. This could potentially be applied to ideal Ohmic contacts to $In_{0.53}Ga_{0.47}As$; a similar reduction in SBH would be expected for InGaAs, where the Schottky barrier is only ~100 meV.[17] This could create a materials system without an oxide or depletion region through which electrons must tunnel, creating the possibility of very low resistance contacts. If the growth of the ErAs cones is stopped before the cones coalesce and is then overgrown with semiconductor, islands could be formed with the desired SBH; thus, this growth method should provide a technique to engineer the shape and thus the Fermi alignment of metal particles in bulk semiconductors. This technique is not limited to the ErAs:GaAs system, but should be applicable to other rare earth group-V compounds and compound semiconductor systems as well as other materials systems with island growth modes that undergo similar phase separations such as $BaTiO_3/CoFe_2O_4$ (Ref. 18) and related materials.

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