Fabrication and performance of nanoscale ultra-smooth programmed defects for EUVL Lithography

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Small particle contaminants, pits, and scratches on the substrate are a serious concern in extreme ultraviolet lithography (EUVL) since they can nucleate printable defects in the multilayer-based mask blanks. In order to develop processes to mitigate the effects of this substrate particles as well as to develop better defect metrology tools, it is necessary to be able to fabricate relatively smooth test substrates with known, controllable defects that can then be coated with a multilayer. We have developed several processes for producing ultra-smooth nanoscale programmed substrate defects for this purpose. Particle, line, pit, and scratch defects on the substrates between 40 and 140 nm wide 50 to 90 nm high have been successfully produced. These programmed defect substrates have several advantages over those produced previously using gold nanoparticles or polystyrene latex spheres, as will be discussed in the presentation.

The procedure for fabricating the particles and lines entails using a hydrogen silsesquioxane (HSQ) resist in an electron beam lithography process. Fig. 1 shows a typical 70 nm x 70 nm line defect coated with a multilayer using the *Ion Beam Thin Film Planarization (IBTFP)* process. Particles as large as 80 nm (height and width) have been smoothed to below 1 nm in height with this process, rendering them nonprintable.

The procedure for producing substrate pit and scratch defects is more challenging than it was for particles and has undergone several process iterations. Fig. 2 shows a 70 nm scratch defect smoothed below the detectable limit using the IBTFP process. This scratch was patterned in cured HSQ using E-beam patterned ZEP-520 and subsequent dry etching. The low roughness (< 0.3 nm) sputtered Cr is employed as an etching stop. The relatively high roughness of the surface HSQ layer (~ 0.7 nm) necessitated a new pit fabrication method to be developed to demonstrate the pit smoothing technique's ultimate capability as well as to enable the production of test masks for defect metrology development (higher roughness leads to a higher haze and more noise in defect inspection tools).

Taking advantage of our ability to produce ultra-low roughness thin films for EUVL-based applications, we have fabricated pits and lines in polysilicon (Fig. 3) as small as 40 nm and with roughness below 0.2 nm rms (Fig. 4). Fabrication issues will be discussed and smoothing results for these pits will also be presented.

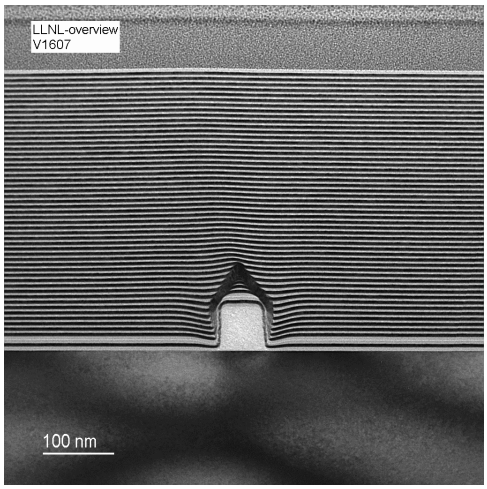

Fig. 1. TEM cross-section of 70 nm smoothed HSQ bump.

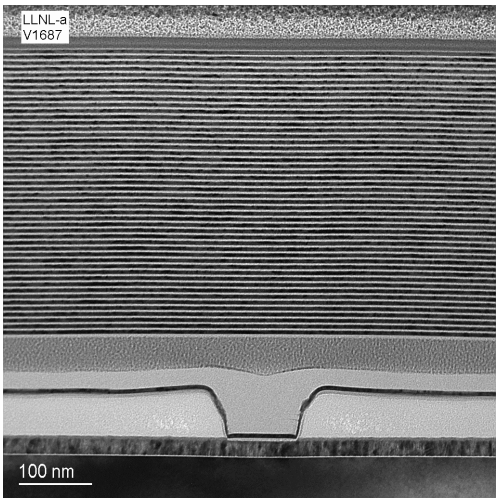

Fig. 2. TEM cross-section of 70 nm smoothed HSQ pit.

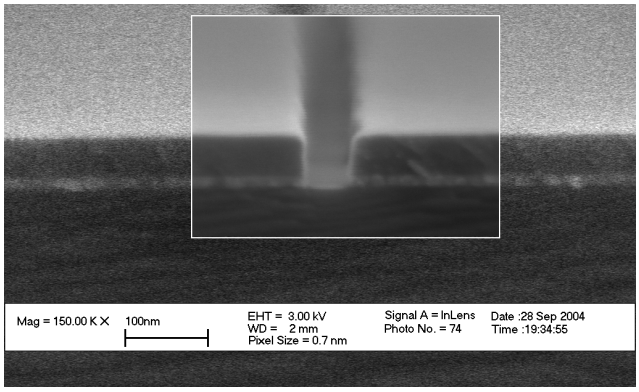

Fig. 3. SEM cross-section of 60 nm pit in 60 nm of polysilicon.

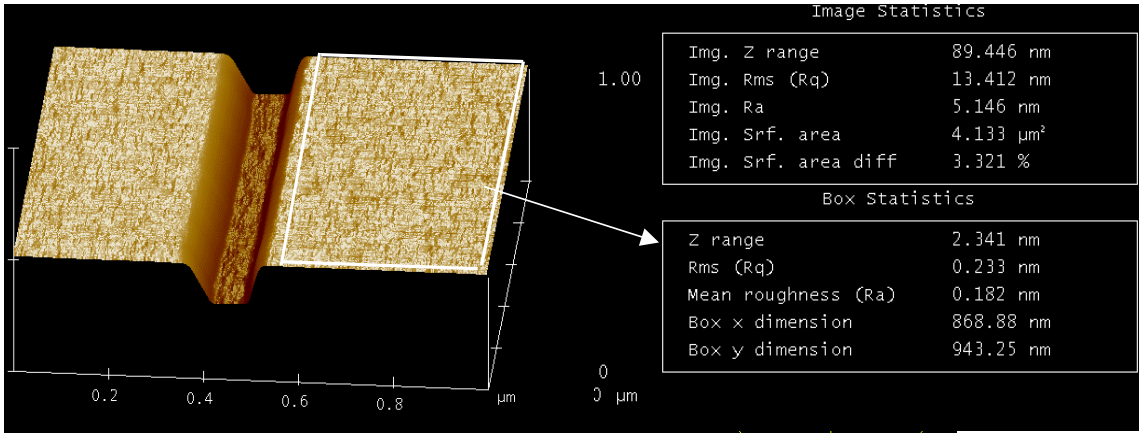

Fig. 4. AFM of 140 nm line in 60 nm polysilicon.