A 144MHz Integrated Resonant Regulating Rectifier with Hybrid Pulse Modulation

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Abstract

This paper presents a CMOS fully-integrated resonant regulating rectifier (IR^3) for inductive power telemetry in implantable devices. Employing PWM and PFM feedback, the IR^3 achieves 1.87% of $\Delta V_{DD}/V_{DD}$ ratio despite a tenfold change in load with a 1nF decoupling capacitor. At 1V regulation of a 100μW load from a 144MHz RF input, the measured voltage conversion efficiency is greater than 92% at under 5.2mV_{pp} ripple and 54% power conversion efficiency. Implemented in 180nm SOI CMOS, the IR^3 circuit occupies 0.078mm^2 active area.

Introduction

Transcutaneous wireless power transfer (WPT) links are often used to power implantable devices due to its completely wireless operation. Conventionally, WPT techniques operate at 13.56 MHz or lower, requiring a bulky external resonator. After rectification, a low drop out (LDO) regulator is typically employed to stabilize the supply voltage [1]. Due to varying LDO performance, the total efficiency of the rectifier and regulator depends on the RF input voltage. To eliminate the need for an LDO altogether, a regulating rectifier was proposed in [2]. However, less than 10% efficiency could be achieved when driving loads below 10mW as typical in implantable applications, and a large external coil was required [2]. For high spatial resolution in implanted systems, a bulky external resonator should be avoided. Addressing applications calling for mm-sized implants requiring a few tens or hundreds microwatts [3], this paper presents an efficient 144MHz integrated resonant regulating rectifier (IR^3) with on-chip antenna for powering implant devices.

Regulation by Pulse Width and Frequency Modulation

To regulate the output voltage V_{DD} in Fig. 1, pulse width modulation (PWM) analog feedback and pulse frequency modulation (PFM) digital feedback are employed. PWM controls the pulse width of V_{GU} and V_{GD} based on an output voltage of the error amplifier, A_{ERR}, that has two inputs: a reference voltage, V_{REF}, and the sensed voltage, V_{SEN}. Owing to large loop gain in analog feedback, PWM offers accurate regulation of V_{DD}. However, due to stability requirements, the response time of PWM analog feedback ranges several microseconds. Furthermore, due to high resonant frequency, the time duration when a RF input, V_{UP} or V_{DN}, is higher than V_{DD} is very short at approximately 1.6ns, so that the PWM cannot cover wide range regulation with high bandwidth. To address these challenges, an auxiliary feedback loop employing PFM is used featuring rapid digital feedback. Using the latch enabler and the upper latch in the PFM part in Fig.1, the digital feedback can monitor whether the pulse duration of V_{GU} is too long leading to reverse current loss. If this occurs, the PFM block will command the pulse generator to increase its operating digital frequency, by asserting V_{WAKE}. Conversely, if the pulse width is too short, V_F exceeds V_{REF_DN} thereby decreasing the digital frequency of the pulse generator. The bidirectional shift register has 5 output bits, Q<0:4>, selecting the digital frequency of the pulse generator. For example, Q<0> leads to 144MHz operation; Q<1> leads to 144MHz/4; Q<2> to 144MHz/8 and so on. To cover an even wider range of regulation, 9 parallel power switches can be turned on/off by commands from outside the body through ASK and a Serial Peripheral Interface bus (SPI).

Event-driven pulse-width generator and PFM logic

Achieving high end-to-end efficiency in the IR^3 requires careful design to manage high frequency losses at small output powers. As a result, conventional comparators that operate at 13.56 MHz and consume over 100μW [2] are not applicable here. The proposed upper (lower) comparator in Fig. 2 is active only when both the V_{WAKE} output of the PFM module, and the V_{UP} (V_{DN}) signal are high. When V_{UP} reaches its peak, V_{ON_PRE} also increases to its own DC bias point, similar to V_{PX}, which is near the logic-threshold of the inverter. Finally, when V_{UP} exceeds V_{DD}, V_{ON} is asserted. To compensate the gate driver delay (~200ps in simulation), the logic threshold of the inverter is adjusted for a faster decision. As such, the simulated power consumption of the comparator reduces to 0.15 ~ 1.5μW at a 0.8V supply across all digital frequencies. To generate a variable pulse width, the delay of the latch is controlled by V_{CON}, output of PWM. For a sufficiently high V_{CON} to provide large current to the latch, the pulse width of V_{PL} can be reduced, and vice versa.

Fig. 3 shows key building blocks for the PFM module that monitors the pulse width of power pMOS gate voltages regularly with a safety-check clock, V_{SAFE}, changeable from 0.88μs (CLK128: 144MHz/128) to 7.1μs (CLK1024: 144MHz/1024). If V_{SAFE} is high, the latch enabler turns on both latches when V_{GU}<0> turns back to V_{DD}. To save power, clock-gated true single phase clocked (TSPC) D-flip flops are employed. By clock gating, the latch enabler operates only when events occur. The same rule applies to a 5-bit bidirectional shift register: if the latches make a decision to change the digital frequency, the shift register generates a clock to update the digital frequency, as illustrated in Fig. 3. Owing to event-driven design, the latch enabler and the shift register consume under 0.5μW.

Measured Results and Concluding Remarks

Fig.4 shows measurements of the IR^3 regulating V_{DD} at 0.8V within 5mVpp ripple for various frequency modulations under varying RF inputs. A tenfold change in I_{LOAD} incurs less than 15mV variation in V_{DD} as shown in Fig. 5. Fig. 7 shows voltage and power conversion efficiency greater than 92% and 54%, respectively, at 1V regulation under 100μA load. Wireless inductive power transfer through the on-chip 2.5mmx2.5mm loop antenna over 10mm distance with greater than 2% overall power conversion efficiency is demonstrated in Fig. 8. The active area of the IR^3 design, shown in Fig. 6, is 0.078mm^2 in 180nm SOI CMOS. Table I summarizes key performance measures in comparison to the state of the art. The unique combination of RF inductive resonant power transfer, rectification, and hybrid PWM-PFM regulation of the IR^3 offers superior voltage and energy conversion efficiency alleviating severe powering conditions of deep mm-size biomedical implants.

References

[1] H. Lee et al., *ISSCC Dig. Tech. Papers*, pp. 286-287, 2012
[2] J. Choi et al., *ISSCC Dig. Tech. Papers*, pp. 63-65, 2013
[3] R. Muller et al., *IEEE JSSC*, Vol. 50(1), pp. 344-359 2015

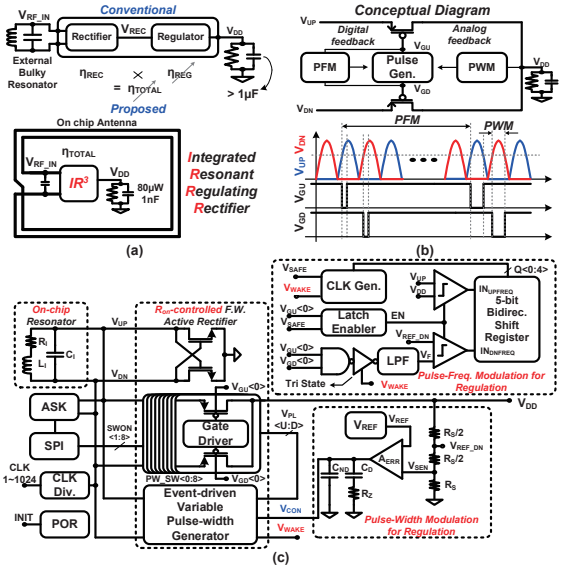

Fig. 1 Integrated resonant regulating rectifier (IR³) (a) Principle of operation. (b) Conceptual diagram. (c) Simplified circuit diagram.

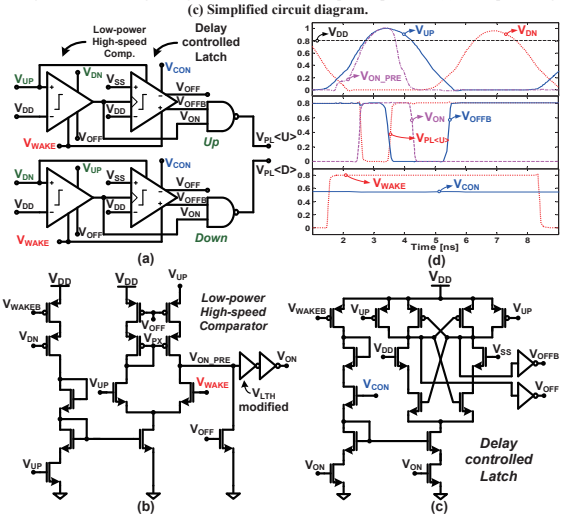

Fig. 2 Level-crossing event-driven variable pulse generator for pulse width control in up and down regulation. (a) Simplified schematic. (b) Low-power high-speed comparator circuit for pulse triggering (shown for UP). (c) Delay controlled latch circuit for pulse width control (shown for UP). (d) Simulated timing waveforms.

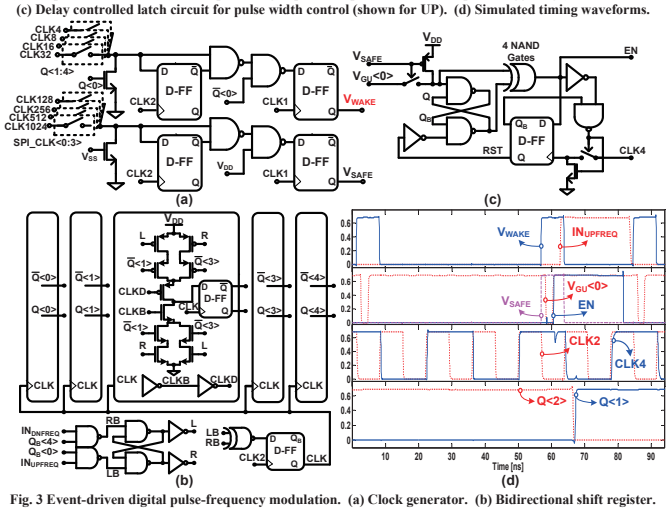

Fig. 3 Event-driven digital pulse-frequency modulation. (a) Clock generator. (b) Bidirectional shift register. (c) Latch enabler. (d) Simulated timing waveforms.

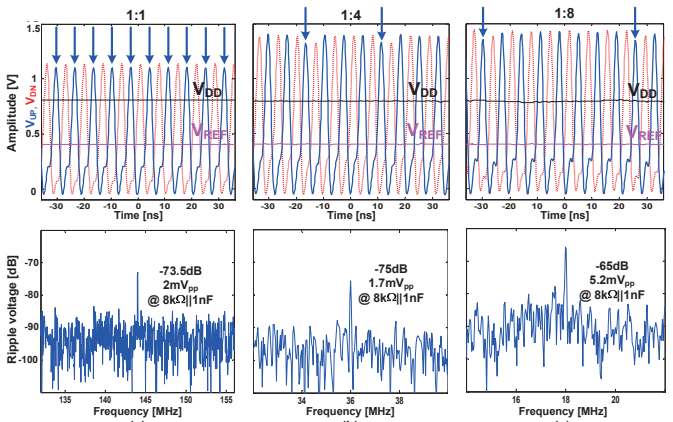

Fig. 4 Measured RF input V_{RF_IN} and DC-regulated output V_{DD} under 8kΩ|| 1nF load operating in (a) Q<0> (144MHz) mode, (b) Q<1> (144MHz/4) mode, and (c) Q<2> (144MHz/8) mode. Arrows indicate active cycles and show RF input loading at the regulation pulse frequency. Spectra for voltage ripple in the regulated output V_{DD}, peaking at the pulse frequency, are shown below for each.

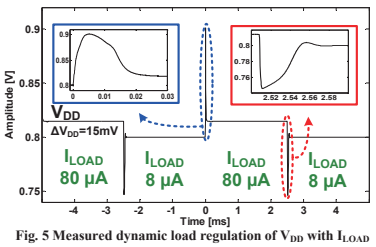

Fig. 5 Measured dynamic load regulation of V_{DD} with I_{LOAD} alternating between 8uA and 80uA with a 1nF decoupling capacitor at V_{DD} node.

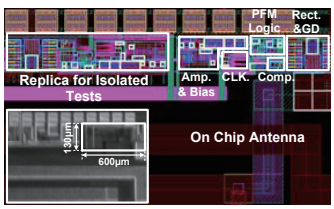

Fig. 6 Chip layout and microphotograph with the IR³ circuit and a replica used for further test of isolated building blocks. Dimensions of the on-chip coil are 2.8 mm × 2.8mm

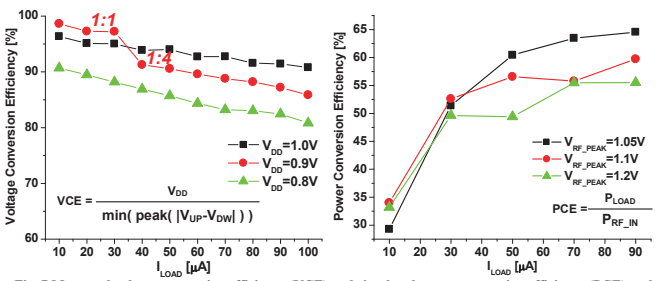

Fig. 7 Measured voltage conversion efficiency (VCE) and simulated power conversion efficiency (PCE) under varying load current, regulation voltage, and RF input conditions.

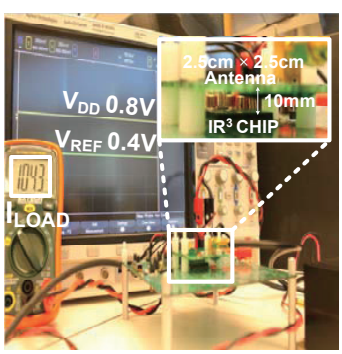

Fig. 8 Test setup for wireless power transfer. Dimensions of TX antenna are 2.5cm × 2.5cm.

Table I Performance Comparison

	ISSCC12 [Lee]	ISSCC13 [Choi]	JSSC14 [Muller]	This work
Structure	Voltage Doubler /Rectifier	Regulating Rectifier	Passive/ Active Rectifier	Regulating Rectifier
Coil	Off-chip/ 410 nH	Off-chip/ -	Off-chip/ 32nH	On-chip/ 23.7nH
Freq. [MHz]	13.56	6.78	300	144
Regulation ($\Delta V_{DD}/V_{DD}$)	-	3.3[a] [%]	-	1.87 [%]
Decoupling Cap. [μF]	1	30	0.004	0.001
Process	0.35 μm 2P3M CMOS	0.35 μm BCD	65 nm 1P7M CMOS	0.18 μm 1P4M CMOS SOI
PCE from TX to V_{DD}	-	-	1.19[b] [%]	2.04[c] [%]
VCE	83.7 [%]	-	-	> 92[d] [%]

[a]decoupling Capacitance: 30μF (C_{OUT}:20μF, C_{PL}:10μF)
Load change: 70mA↔700mA
[b]estimated from provided data including transmit PW: 13mW, reveived PW: 0.225mW and P_{LOAD}: 0.160mW at distance: 12.5mm
[c]measured TX power: 7.87mW and P_{LOAD}: 0.160mW at distance: 10mm
[d]VDD=1V